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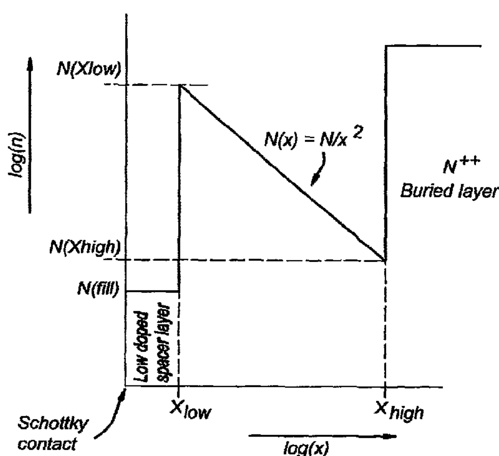
(54) Title: VARACTOR ELEMENT AND LOW DISTORTION VARACTOR CIRCUIT ARRANGEMENT



(57) Abstract: Varactor element (Dl; D2) having a junction region, in which the depletion capacitance of the varactor element varies when a reverse bias voltage is applied to the varactor element. The varactor element (Dl; D2) has an exponential depletion capacitance- voltage relation, e.g. obtained by providing a predetermined doping profile in the junction region. The varactor element (Dl; D2) can be used in a narrow tone spacing varactor stack arrangement, in which two varactor elements (Dl; D2) are connected in an anti-series configuration. A low impedance path for base band frequency components between a control node and each of two RF connection nodes is provided, while for fundamental and higher order harmonic frequencies, a high impedance path is provided.

WO 2007/061308 A1

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

Varactor element and low distortion varactor circuit arrangement

Field of the invention

The present invention relates to a varactor element having a junction region, in which the depletion capacitance of the varactor element varies when a reverse bias voltage is applied to the varactor element. Such a varactor element is also known as varactor diode, tunable diode, or voltage controlled capacitor.

Prior art

Such varactor elements are known, and the behavior is well understood. In textbooks, it can be found that for diode based varactor elements, the capacitance voltage characteristic is in the form of $C(V) = \frac{K}{(\phi + V)^m}$, in which C(V) is the capacitance as function of the total (reverse) voltage V across the diode, ϕ is the built-in potential of the diode, m is the power law exponent of the diode capacitance and K is the capacitance constant. For a diode with a uniform doping profile, m=0.5, and for a diode with a hyper-abrupt junction, m≈1.5. Such a characteristic however limits the application of varactors in certain high quality applications, such as low distortion varactor stacks, especially when used in devices designed for operation with narrow tone spacing signals, such as in many modern day communications systems (see e.g. K. Buisman, L.C.N. K. Buisman, L. C. N. de Vreede, L. E. Larson, M. Spirito, A. Akhnoukh, T. L. M. Scholtes and L. K. Nanver, "'Distortion free' varactor diode topologies for RF adaptivity," in 2005 IEEE MTT-S Int. Microwave Symp. Dig., Long Beach, California, June. 2005).

In order to overcome these drawbacks, recently varactor diode-based circuit topologies and a high performance varactor diode process technology has been presented, which, for a given diode power-law capacitance coefficient (m≥0.5), can act as variable capacitors with extremely low distortion. However, the proposed solutions have linearity constrains for modulated signals or signals with narrow tone spacing when considering practical implementations. The invention presented here aims to overcome these limitations, in terms of linearity for narrowband signals, sensitivity to leakage currents of the varactors, high control voltage and capacitance tuning range.

Summary of the invention

According to the present invention, a varactor element according to the preamble defined above is provided, in which the varactor element has an exponential depletion capacitance-voltage relation, as defined in the appended claim 1. Such a capacitance
5 voltage relation, in the form of $C_{BBshort}(V) = a_1 e^{a_2 V}$, in which C(V) is the depletion capacitance as function of the total (reverse) voltage V across the varactor element, and a_1 and a_2 are predefined constants, allows to design many applications in which linearity for narrowband signals, sensitivity to the varactor leakage current, high control voltage and capacitance tuning range are important design constraints.

10 The exponential depletion capacitance-voltage relation is obtained by providing a predetermined doping profile in the junction region. By selecting a predetermined doping profile different from the known uniform or hyper-abrupt doping profile, the exponential capacitance-voltage relation of the varactor element may be obtained.

The junction region comprises, in a further embodiment, a filling layer in an
15 interval of distances lower than x_{low} with a doping concentration N_{fill} lower than the doping concentration at distance x_{low} ($N(x_{low})$). This allows to maintain the N/x^2 doping versus depth relation with respect to the junction position. The low doping concentration in the filling layer results in a lower contribution to the electric field in order not to lower the intended breakdown voltage of the diode or unnecessary increase
20 the required control voltages.

The junction region comprises a single sided junction, e.g. a Schottky diode or a PN junction diode with the one side of the junction doped significantly higher then the intended region for depletion, and the varactor element is e.g. provided with a doping profile substantially defined by $N(x) = N/x^2$, N(x) being the varactor element's doping
25 concentration in one dimension as a function of x, x being a distance from the (effective) junction, and N being a predefined doping concentration constant. Especially in electronic circuit design for modulation of RF signals, in which third order inter modulation should be suppressed, such varactor elements can be advantageously applied, even when narrow tone spacing signals are involved.

30 In a further embodiment, the doping profile is substantially equal to N(x) at least in the interval $x_{low}...x_{high}$, in which x_{low} is nearer to the junction than x_{high}. This allows to obtain a profile having a doping concentration of feasible values (the above formula

would become singular for x=0). The ratio of x_{high} and x_{low} defines the useful capacitance tuning range.

The junction region of the varactor element may also be a two sided or double sided junction. To obtain the exponential relation in this case is more complicated, but certainly attainable in many different manners, e.g. using a more complex doping profile. An example of a double sided junction could be for example the use of a low P-type doping for the filling layer, which in normal varactor operation is completely depleted. Note that in such a implementation although the doping junction is moved, the resulting C(V) relation can still show the desired exponential dependency on the voltage.

In known circuit arrangements, low distortion varactor operation for larger tone spacing is accomplished by utilizing two back to back varactor diodes utilizing a uniform doping, or for hyper abrupt varactors (grading coefficient $m > 0.5$) utilizing a parallel configuration of two anti-series varactor diodes. The known varactors configurations behave only linear if the impedance connected to the center tap is significantly higher than the impedance offered by the varactor diode capacitances itself, this condition should be satisfied for all frequency components involved. In practice this proves to be very problematic for two tone signals with narrow tone spacing or modulated signals. The above can be easily understood by considering a two-tone test signal with a tone spacing approaching zero. As consequence the impedance offered at the difference frequency (f_2-f_1) by the varactor diodes will approach infinity when f_1 approaches f_2. It is obvious that this yields an unrealistic condition for the center tap impedance which has to be larger then the impedance offered by the diodes. Typically very high center tap impedances are required in the conventional solution. This give rise to various problems, since the center tap is more or less “floating”. When using a high valued resistor for the center-tap impedance also any leakage current of the varactor diodes becomes problematic due to resulting DC offsets of the center tap in respect to the control voltage. Some improvement can be obtained for this situation by using an anti parallel diode configuration in the center tap path in order to increase the AC center-tap impedance. Although good results have been achieved in simulation with this configuration for moderate tone spacing, the use of narrow tone spacing remains problematic and also this configuration is still relative sensitive to leaking currents of the varactor diodes.

The solutions above might provide reasonable performance of the resulting tunable capacitor where static loading conditions are required, but are less suited when fast modulation of the tunable capacitor is needed. Note that these conditions typically apply in modulators, dynamically varied phase shifters, or adaptive matching networks for dynamic load line modulation mixers, etc. Other short comings are the limited capacitance tuning range and high control voltage when using a uniform doping profile. When using the hyper abrupt varactors the linearity is somewhat degraded compared to uniformly doped varactor implementation.

In a further aspect of the present invention, it is therefore proposed to provide a varactor stack circuit arrangement, comprising two varactor elements according to an embodiment of the present invention, each having two terminals, in which the two varactor elements are connected in an anti-series configuration, such that a control node is provided by two interconnected terminals and two RF connection nodes by the other terminals. Such an arrangement, also called narrow tone spacing varactor stack (NTSVS), provides an improved performance compared to existing arrangements. The two varactor elements may be connected to each other using a common cathode, or using a common anode. This allows the possibility to choose what kind of control voltage (positive or negative relative to the RF terminals) can be used in the varactor circuit arrangement. The varactor elements used in this arrangement may be identical.

In a further embodiment, the varactor circuit arrangement further comprises a center tap impedance connected to the control node, the center tap impedance providing a low impedance path for base band frequency components between the control node and each of the two RF connection nodes. A high impedance path for fundamental and higher order harmonic frequency components may also be provided. The indications low and high impedance refer to the impedance offered by the varactor circuit arrangement itself for the frequency component under consideration. This results in a varactor circuit arrangement having a high linearity for modulated signals and narrow tone spacings, and a high tuning range compared to uniform doped varactors. Only low control voltages are needed, and the arrangement is not sensitive for leakage current of the varactor diodes. Furthermore, no high impedance condition is required at the base band frequencies making it more suitable for the implementation of modulators, mixers and dynamic/adaptive matching networks.

The low impedance path has an impedance lower than the one offered by the varactor element capacitances for the base-band frequency component, which allows for a very efficient suppression of third order inter modulation distortion in the varactor circuit arrangement.

5 The NTSVS may be applied in numerous applications, as part of more complex circuitry. In an even further aspect, the present invention relates to a four port electronic device, comprising two series capacitors and two cross connected capacitors, in which one of the two series capacitors is connected between a first input port and a first output port, the other of the two series capacitors is connected between a second 10 input port and a second output port, one of the two cross connected capacitors is connected between the first input port and the second output port, and the other of the two cross connected capacitors is connected between the second input port and the first output port. At least the two series capacitors or the two cross connected capacitors comprise a varactor stack arrangement according to an embodiment of the present 15 invention. The other capacitors may then be fixed capacitors. In a very advantageous embodiment, all four capacitors are voltage controlled variable capacitors implemented using the varactor stack arrangement according to the present invention. Such a four port electronic device, or differential varactor amplitude modulator (DVAM), may be applied directly as amplitude modulator, but may also be applied in more complex 20 circuitry, such as a transmitter, polar amplifier circuit, and a direct modulator.

In a further embodiment, the four port electronic arrangement further comprises a first shunt inductor connected between the first and second input port, and a second shunt inductor connected between the first and second output port. This allows this circuitry to be used as an amplitude modulator or as an adaptive matching network. 25 Compared to conventional designs, far less components are needed. Also, in combination with an RF amplifier stage, this arrangement may be advantageously used in a transmitter, allowing a very high power added efficiency (PAE) for modulated signals or (slowly) varying output power conditions. Also, polar amplifiers may be designed in which the amplifier efficiency is boosted by saturated operation of the 30 active components in the polar amplifier. At the output of the amplifier, square wave like signal conditions result. Using the four port electronic arrangement of the present invention in this case, allows to obtain a highly efficient polar amplifier.

In an even further aspect, the present invention relates to a direct polar modulator, comprising a four port electronic arrangement according to the present invention, in which the first and second output ports are further connected to a series of phase shift sections, each phase shift section comprising a varactor stack arrangement according to an embodiment of the present invention. Each of the varactor stack arrangements (in the amplitude modulator and in the phase shift sections) can be controlled using control voltages. E.g. a digital to analogue converter may be used to set all control voltages of the varactor stack arrangements. Such a modulator structure can be part of a transmitter which is directly capable to serve many different modulation formats, such as QPSK, BSK, FSK, OFDM, etc. Also, multiple frequency bands can be accommodated by offsetting the varactor stack arrangement values in a proper way.

The present invention also relates to the use of a varactor stack arrangement according to an embodiment of the present invention, in adaptive or dynamic matching networks, in adaptive or tunable phase shifter devices, in direct modulators arrangements, as up converting mixer or modulator, in RF switches, in tunable filters or multiplexers, etc. A further example includes the use of a varactor stack arrangement in antenna array systems, such as phased arrays to perform adaptive beam forming.

Short description of drawings

The present invention will be discussed in more detail below, using a number of exemplary embodiments, with reference to the attached drawings, in which

Fig. 1 shows a doping profile diagram of an embodiment of the varactor element according to the present invention having a single sided junction;

Fig. 2a shows a doping concentration versus depth profile of a further embodiment of the varactor element according to the present invention (in this doping profile the effective junction is located at 0.2 μm), and Fig. 2b shows the associated capacitance-voltage characteristic;

Fig. 3a shows a general symbol for a controlled variable capacitor, and Fig. 3b and c show embodiments of such a capacitor using an anti-series arrangement of two variable capacitance varactor diodes;

Fig. 4 shows a schematic circuit diagram of an embodiment of the anti-series arrangement using varactor diodes, as used for various simulations;

Fig. 5 shows the resulting spectrum of the capacitive current flowing through the varactor stack in the circuit of Fig. 4 using conventional varactor diodes, when the node c' is modulated by 3 MHz signal, while applying a 1 MHz two-tone signal on a carrier wave of 1 GHz to the RF terminal(s);

5 Fig. 6 shows the resulting spectrum under the same conditions as in Fig. 5 when using varactor elements according to an embodiment of the present invention;

Fig. 7 shows a circuit diagram of a differential varactor amplitude modulator according to an embodiment of the present invention;

Fig. 8 shows the resulting spectrum of a 2 GHz sinusoidal source signal

10 modulated by a 1 MHz base band signal, using conventional varactor diodes as variable capacitor in the circuit diagram of Fig. 7;

Fig. 9 shows a similar spectrum when using an embodiment of the varactor element according to the present invention;

Fig. 10 shows a circuit diagram of an amplifier circuit using an embodiment of

15 the four port electronic device according to an embodiment of the present invention;

Fig. 11a shows the efficiency plotted versus output power for single tone operation of the amplifier circuit of Fig. 10 using loss-less components, Fig. 11b shows the efficiency versus output power when assuming a Q factor of 100 for the passive components, and Fig. 11c shows the required DC control voltages for the varactor

20 elements;

Fig. 12 shows a schematic diagram of an embodiment of a transmitter architecture using a direct modulator based on varactor elements according to embodiments of the present invention;

Fig. 13 shows a circuit diagram of an embodiment of a direct polar modulator as

25 used in the transmitter of Fig. 12;

Fig. 14 shows a doping profile diagram of a further embodiment of the varactor element according to the present invention having a single sided junction;

Fig. 15 shows a low distortion configuration for varactor tuned / modulated narrowband (transmitter) applications of varactors according to an embodiment of the

30 present invention;

Fig. 16 shows a possible configuration of a varactor stack device according to an embodiment of the present invention comprising two Schottky diodes;

Fig. 17 shows a top view of terminals of a varactor stack circuit according to an embodiment of the present invention;

Fig. 18a shows a sectional view of a semiconductor structure of a varactor stack assembly according to a further embodiment of the present invention; and

5 Fig. 18b shows a op view of the varactor stack arrangement of Fig. 18a.

Detailed description of exemplary embodiments

According to the present invention, a varactor element is provided having an exponential capacitance voltage relation, according to

10 $$C_{BBshort}(V) = a_1 e^{a_2 V} \qquad \text{equation 1}$$

in which C(V) is the capacitance as function of the total (reverse) voltage V across the varactor element, and a_1 and a_2 are constants which value can be chosen based on the application considerations (tuning range, quality factor of the NTSVS, voltage range).

The capacitance voltage relation of commonly used diode varactors is known to

15 the skilled person as being equal to

$$C(V) = \frac{K}{(\phi + V)^m} \qquad \text{equation 2}$$

in which C(V) is the capacitance as function of the total (reverse) voltage V across the diode, ϕ is the built-in potential of the diode, m is the power law exponent of the diode capacitance (m=0.5 for a diode with a uniform doping profile) and K is the capacitance

20 constant.

It has been found that the desired relationship (equation 1) can be achieved by modifying the doping profile of the varactor element, especially the doping profile of the junction region of the varactor element.

For this purpose a one-side junction (e.g. a Schottky diode) is assumed and solve

25 for the doping profile using the known relation

$$N(x) = \frac{C(V)^3}{q\varepsilon}\left(\frac{dC(V)}{dV}\right)^{-1}$$

with

$$x = \frac{\varepsilon}{C(V)}$$

Making use of the above relations, it can be proven that the required doping profile for

30 an exponential capacitance voltage relation in this case is:

$$N(x) = \frac{N}{x^2} \qquad \text{equation 3}$$

in which N is a doping concentration constant to be defined. It should be noted that the upper formulation of the doping profile is singular for x=0, consequently, measures to avoid this singularity must be taken. In order to explain how the doping profile for a
5 first embodiment of a varactor element according to the present invention should be defined we consider Fig. 1, which shows the required varactor doping profile for a single sided junction of the varactor element to achieve the exponential C(V) relation.

As become clear from Fig. 1 the N/x^2 doping relation appears as a straight line on logarithmic plot of the doping concentration versus the logarithm of the distance (x).
10 Since an infinitely high or extremely low doping concentration cannot be provided, this relation has to be broken off at the distances x_{low} and x_{high}. Doing so, automatically the useful capacitance tuning range (C_{ratio}) is defined since the capacitance is inversely proportional with the distance x.

$$C_{ratio} = x_{high} / x_{low}$$

15

To achieve the exponential C(V) relation for a single sided junction a filling or "spacer" layer is required in order to satisfy the N/x^2 doping versus depth relation with respect to the junction position (e.g. a doubling of the distance with the junction should result in a four times lower doping concentration). This spacer or filling layer, which in
20 the useful varactor diode operation is depleted, preferably does not increase the electric field significantly to avoid reduced device breakdown and capacitance tuning range. To achieve this, the doping concentration of this filling layer must be kept low in respect to $N(x_{low})$. $N(x_{low})$ must be chosen in such a way that in combination with the desired tuning range and control voltage, the zero bias varactor quality factor is maximized
25 without exceeding the critical electric field at the varactor junction for the maximum operation voltage intended. Since the slope of the doping concentration is fixed by the required exponential capacitance voltage relation, the doping profile is basically defined with the choice of: x_{low}, x_{high} and $N(x_{low})$.

As one would expect there is a trade-off in capacitance tuning range, control
30 voltage en Q-factor of the varactor element. For this reason the use of III-V materials or wide band gap materials is recommended for this structure. E.g. when using GaAs the intrinsically higher electron mobility (~ a factor 5) of this material compared to silicon,

yields a 5x Q improvement for an identical structure. However, for low control voltages good results can be also obtained using silicon.

Simulations have been performed for a varactor element having a doping profile as shown in Fig. 2a. In this doping profile, the complete doping profile is shown, including the highly doped region (1e+19) left of the filling layer (5e+16). The lightly doped filling layer in the doping profile avoids a rapid increase of the electric field near the junction. This relaxes the device voltage breakdown conditions. Note that for a one sided junction, this filling layer is provided in combination with the doping concentration of equation 3 to obtain the desired C(V) characteristic (equation 1), which when plotted on a log scale should results in a substantially straight line as shown in the plot of Fig. 2b. It must be mentioned that this behaviour is characteristic for the proposed doping profile. Any deviation of the straight line in Fig. 2b will result in an increase of the IM3 distortion level. The related zero bias Q of this particular example is limited to ~20 for a silicon device. By selecting an other choice for the parameters of Fig. 1, the voltage range or capacitance tuning ratio can be adjusted, consequently one can improve for the Q (values > 300 are feasible in silicon), breakdown voltage (values > 100V are feasible in silicon for a constrained capacitance tuning range and quality factor) or tuning range (values > 15 are feasible in silicon for a constrained breakdown voltage and Q factor). Clearly there is a trade off between the Q factor, breakdown voltage and tuning range. One can improve for this trade of by using other technologies with a higher mobility like GaAs, which due to its roughly 5x higher mobility compared to silicon, will yield an approximately 5 times higher Q factor for a given varactor doping profile. When considering the device in Fig. 2 the zero bias Q factor would be approximately 100 when implemented in GaAs. Also the use of wideband gap materials can be beneficial since this allows the use of higher doping concentrations and electric field conditions at the device junction. The exact doping profile of the filling layer is normally not of great significance to the desired exponential C(V) relation. However, due to the fact that in real devices the abrupt depletion approximation is not very accurate, one can utilize the doping structure of this spacer layer to improve on the intended exponential C(V) relation for the low voltage range.

In the above example description, a one sided junction has been used. In a one sided junction the doping level on one side of the junction is much higher than on the other side. As a result the depletion region will only effectively extend in one-direction.

However, to obtain the exponential capacitance voltage dependence according equation 1, other solutions to realize this behaviour are possible if one utilizes two or double-sided junction solutions. In this case there are in principle an unlimited number of solutions possible for the doping profile which can yield the desired behaviour of equation 1.

A varactor element according to any of the embodiments described above, may be advantageously applied as a variable voltage controlled capacitor. In Fig. 3a, a general schematic symbol is shown of such a variable voltage controlled capacitor as a three terminal device. Between nodes a and b (or RF connection nodes), a variable capacitance C_{ab} is present, and node c is used as control voltage input. Actual implementations using varactor diodes are shown schematically in Fig. 3b and 3c, which show two varactor diodes D1, D2 each having two terminals, connected in anti-series configuration between nodes a and b. Node c is formed by the connecting point of two of the terminals of the diodes (cathode of the diodes in Fig. 3b, anodes of the diodes in Fig. 3c). Fig. 3b shows a common cathode implementation, intended for a positive control voltage at node c relative to the nodes a and b and Fig. 3c shows a common anode implementation, intended for a negative control voltage at node c relative to the terminals a and b. Using varactor elements having the desired characteristic of equation 1 as described above, it is possible to build various applications which beneficially exploit this characteristic.

In a first exemplary embodiment, the varactor elements are used to provide a narrow tone spacing varactor stack device. Such an NTSVS device may be advantageously used in all sorts of amplitude and phase modulators, which in turn may be used in adaptive or dynamic matching networks, adaptive or tunable phase shifter devices (e.g. in phased array systems), direct modulators, up converting mixers or modulators, RF switches, tunable filters or multiplexers, etc.

The invention introduced here, the “Narrow Tone Spacing Varactor Stack” (NTSVS), is a low distortion tunable capacitor which provides excellent linearity for narrowband or modulated signals, making it very attractive for transmitter or modulator applications. The tunable capacitor is based on two back-to-back varactors with a very

specific (N/x^2) based doping profile (assuming a single sided junction). The configuration utilizes base-band shorts at the center tap and external pins. Such an NTSVS features a high linearity for modulated signals and narrow tone spacings, a high tuning range compared to uniform doped varactors, low control voltages, is not
5 sensitive for leakage current of the varactor diodes, and no high impedance conditions required at base-band or IF impedance making it more suitable for the implementation of modulators, mixers and dynamic/adaptive matching networks.

A schematic circuit diagram of a NTSVS is shown in Fig. 4. The NTSVS is used in a common cathode configuration, and the node b of bottom diode D2 is connected to
10 ground. The node a of the upper diode D1 is connected to a signal source V_s via a resistor R_g. The signal source V_s is grounded at the other side, and provides a two tone signal (indicated by s_1 and s_2) with a narrowband spacing. A control voltage $V_{control}$ is applied to the control node c' of the varactor stack, by means of a center tap impedance $Z_c(s)$ of which the other terminal is connected at node c. The diodes D1 and D2 may be
15 identical.

In known arrangements using a stack of varactor diodes, it is assumed that Z_c can be considered as infinitely high impedance for all frequency components. When solving for this situation the third order inter modulation (IM3) component of the voltage on the connecting terminal of the varactor configuration the following
20 expression is found:

$$IM3_{Z_c=\infty} = \frac{3(2s_1 - s_2)(2c_1{}^2 - c_0c_2)g_s{}^2 A^2}{4c(2g_s + s_1c)(2g_s - s_2c)((2s_1 - s_2)c + 2g_s)} \qquad \text{equation 4}$$

in which:

$$c_0 = \frac{dq(v)}{dv}$$

$$c_1 = \frac{1}{2}\frac{d^2q(v)}{d^2v}$$

$$c_2 = \frac{1}{6}\frac{d^3q(v)}{d^3v}$$

25 are the Taylor coefficients of the varactor diode, g_s is the source conductance ($1/R_g$) and s_1 and s_2 are the complex frequencies, while A is the amplitude of the voltage signal source. It can be observed from equation 4 that the IM3 distortion is cancelled when we satisfy the following condition for the varactor Taylor coefficients.

$$c_0 c_2 - 2c_1^2 = 0$$

Solving this differential equation for the capacitance function, while assuming an equal area of the varactor diodes in Fig. 4 yields, the well known C(V) textbook relation (equation 2 above), with m=0.5.

$$C(V) = \frac{K}{(\phi + V)^m}$$

When solving the IM3 component of the arrangement of Fig. 4 (again assuming an equal area of the varactor diodes) but now using the condition $Z_{c(f2-f1)}=0$ (base band short), while Z_c is infinitely high for all other frequency components, the following IM3 cancellation condition is found for very narrow tone spacing $(\Delta f \to 0)$:

$$IM3_{BBshort} = \frac{(2c_1^2 - 3c_0 c_2) g_s^2 s_c A^2}{4c(2g_s - s_c c)(2g_s + s_c c)^2}$$

The resulting C(V) relation, which can be found by solving the differential equation,

$$3c_0 c_2 - 2c_1^2 = 0$$

proves now to be an exponential relation rather then the well known text book C(V) relation (equation 2), and is given by:

$$C_{BBshort}(V) = a_1 e^{a_2 V}$$

In this relation a_1 and a_2 indicate the integration constants, which add some flexibility to our solution. Note that any choice of a_1 and a_2 will satisfy the differential equation, yielding perfect cancellation of the IM3 distortion component also for narrow tone spacing. The varactor element embodiments as described above fulfil this exponential relation and may advantageously be used in an NTSVS arrangement as shown in Fig. 4 to obtain the desired IM3 distortion cancellation.

For this IM3 cancellation, a low AC impedance path at the base-band frequencies (this is relative to the AC impedance offered by the varactor capacitance itself) between the center node c and the RF terminals a and b is needed. Simultaneously, for the high frequency components (fundamental, and higher harmonics) the AC impedance between the node c and node a, or node c and node b must be high (this again relative to the AC impedance offered by the varactors itself at these frequency components).

Using the configuration of Fig 4 we have simulated the Voltage IP3 of the capacitance currents as function of tone spacing, for an existing solution using a distortion free varactor stack (DFVS) and for a solution using the now proposed NTSVS. In the DFVS, the ratio of cross sectional areas of the two diodes are adapted to minimize third order distortion. It has been found that while the conventional DFVS provides the highest linearity for large tone spacing for a given center tap impedance, the NTSVS provides the best results for small values of Δf. The cross sectional areas of the two diodes may be the same in the case of the NTSVS. It is important to note that there must be a low impedance (relative to the impedance offered by the varactor diodes) path for the base-band frequency component between the center tap and the external pins. The corner frequency where the linearity starts to degrade is related to how well one succeeds to provide low impedance for the base-band frequencies and simultaneously provide high impedance for the fundamental and higher harmonic frequency components. As a result a more sophisticated network can provide improvements.

All impedance levels indications are relative to the varactor diode impedance at the harmonic component under consideration. The NTSVS can be effectively used for static conditions e.g. to tune out antenna mismatch condition, adaptive matching, switching, phase shifting etc., but can also be used dynamically to implement modulator or mixing functions.

In order to create a useful linear mixing function using the arrangement of Fig. 4, two basic conditions should be fulfilled, namely:

1) The capacitive current flowing though the effective capacitance of the varactor stack c_{ab} should be linearly related to the applied RF voltage over the nodes a and b. In most practical (telecommunication) applications this requires a zero value for the 3rd order Volterra kernel of c_{ab} with respect to the applied RF signal over the nodes a and b. Consequently, no third-order intermodulation distortion products arise in the resulting current through c_{ab}.
2) For the desired mixing action, the effective capacitance c_{ab} must be modulated in such a way that the desired transfer function of the total circuit is modulated in a linear fashion. This has as consequence that one should compensate (pre-distort) for the non-linear C(V) relation of c_{ab} with respect to the center tap voltage at node c, as well for how a capacitance change relates to transfer function of the total circuit.

Condition 1) is the most important one, since distortion at the RF signal level can not easily be encountered for. Condition 2) is less critical since the controlling voltage in a modulator is typically a base-band signal, which can be accurately controlled or pre-distorted in a rather arbitrary fashion.

5 In the following examples, a two-tone RF voltage source V_s is connected to node a. The capacitance is modulated by an independent voltage source ($V_{control}$) connected to node c. Depending on the C(V) relation, this modulating voltage is pre-distorted using a set of equations and a non linear pre-distorting element. As a result a linear variation of c_{ab} with the modulating base-band signal is obtained and consequently the

10 desired capacitive mixing action. It must be mentioned that this mixing is perfectly linear under the constraint that c_{ab} does not generate any inter modulation distortion due to the applied RF voltage at the nodes a and b.

When using the Distortion Free Varactor Stack (DFVS) configuration in the schematic of Fig. 4 the resulting spectrum of the capacitive current as shown in Fig. 5

15 is obtained. The AM side bands around the center frequency are visible, but the result is rather bad in terms of the IM3 components, which appear around the two-tone signals.

In contrast to the DFVS, the NTSVS requires a base-band short in order to guarantee its low distortion operation. Consequently, for its correct operation low impedance paths at base-band frequencies (BB-shorts) have to be provided between the

20 center tap (node c) and the *a* and *b* nodes, and high impedances for the fundamental and higher harmonics. The resulting spectrum of the capacitive current is given in Fig. 6. For a fair comparison the two-tone signal conditions, the effective capacitance value c_{ab} and its relative change, are chosen the same as in the DFVS simulation experiment. The spectrum of the capacitive current is significantly improved compared to the results for

25 the DFVS in this mixing experiment. It should be noted that the minimum inter modulation levels achieved in this experiment are now basically depending on, how well one can meet the short conditions at the base-band frequencies and the open conditions at the fundamental and higher harmonics.

In summary, the NTSVS topology provides, as compared to the previous state of

30 the art, a high linearity for modulated signals and narrow tone spacings, a high tuning range compared to uniform doped varactors. Furthermore, only low control voltages required for large capacitance variation, and the arrangement is not sensitive for leakage current of the varactor diodes. Also, no high impedance conditions are required

at IF impedance making it more suitable for the implementation of modulators, mixers and dynamic/adaptive matching networks.

A further advantageous use of the varactor element according to the present invention can be found in the following exemplary embodiment. The differential varactor based Amplitude Modulator (DVAM) is based on the combination of direct and cross wise connected capacitive coupling of the in- and output, as shown in the schematic diagram of Fig. 7. One of the two series variable capacitors (Cseries1) is connected between a first input port and a first output port, the other of the two series variable capacitors (Cseries2) is connected between a second input port and a second output port. One of the two cross connected variable capacitors (Ccross1) is connected between the first input port and the second output port, and the other of the two cross connected variable capacitors (Ccross2) is connected between the second input port and the first output port. Furthermore, the input ports and output ports are connected to each other using shunt coils (Lshunt). At the input ports, a voltage source Vsource is connected (e.g. providing a 3V 2 GHz signal) and at the output ports, a load (Rload) is connected.

The principle of this configuration is based on the fact that the displacements currents through the directly connected capacitors (Cseries1, Cseries2) are in opposite phase with those of the cross coupled capacitor pair (Ccross1, Ccross2). When the circuit is driven differentially and all the capacitive elements have the same value, the capacitive currents will cancel. By varying the value of the cross wise connected capacitors (Ccross1, Ccross2) in respect to the direct connected capacitors (Cseries1, Cseries2), the displacement currents will not cancel and energy will be transferred from the differential input to output port or visa versa. By combining this capacitive quad with two shunt inductors (Lshunt) and proper dimensioning of its element values, some very special properties can be achieved for this circuit configuration, which makes it attractive as amplitude modulator in RF applications and in special applications, such as adaptive matching network in combination with a RF power amplifier stage. Note that such a combination facilitates in principle very high power added efficiency (PAE) for modulated signals or (slowly) varying output power conditions.

Although the above described embodiment uses varactor elements for all four capacitors, embodiments are also possible in which either the cross connected

capacitors or the series connected capacitors are formed by fixed capacitors (not variable).

The unique behaviour of this circuit can be best studied by enforcing that the input impedance is ohmic. The input impedance of this configuration is given by:

5

$$Z_{in} = \frac{(s^2 * Lc_{series} + s^2 Lc_{cross} + 2g_1 sL + 2)sL}{(2s^4 L^2 c_{series} c_{cross} + s^3 L^2 c_{series} g_1 + 2s^2 Lc_{series} + s^3 L^2 c_{cross} g_1 + 2s^2 Lc_{cross} + 2g_1 sL + 2)}$$

Enforcing the imaginary part of Z_{in} to be zero yields the following relation for the series and cross connected capacitors

$$c_{cross} = \frac{-(\omega^2 Lc_{series} - 2)}{(\omega^2 L)}, \qquad c_{cross} = \frac{-(-\omega^2 Lc_{series} + 1 + g_{load}{}^2 \omega^2 L^2)}{(\omega^2 L(\omega^2 Lc_{series} - 1))}$$

in which:

10 c_{series} = series capacitor value

c_{cross} = cross connected capacitor value

g_{load} = single ended load conductance

L = shunt connected inductor

By now changing the value of the c_{series} versus c_{cross} while satisfying the above

15 condition for the values of c_{series} and c_{cross}, the following properties are achieved.

- The transfer (s_{21}) can be continuously varied between -j and +j ;
- The input impedance is always ohmic.

As a result, this circuit will not introduce any AM to PM (phase modulation) distortion, since the phase of s_{21} is always on the imaginary axis. The phase reversal

20 indicates the potential operation as multiplier. The fact that the circuit is lossless results in a reflection of all energy ($s_{11}=s_{22}=1$) when no power is transferred ($s_{21}=s_{12}=0$) from in- to output ($c_{series} = c_{cross}$), yielding an infinitely high impedance at the ports. (Note that an inverse behaviour ($s_{11}=s_{22}= -1$) is also possible if one uses series inductors rather then shunt inductors yielding short circuit conditions at the ports). The fact that

25 the input impedance varies with the power transfer makes the network interesting for dynamic load line applications. Furthermore, the operation frequency of this network can easily customized by adjusting the values of the variable capacitances c_{cross} and c_{series}.

Above, the small signal behaviour of the DVAM has been studied. Its principle is

30 based on the use of tunable capacitances for the implementation of the series and cross connected capacitors. It is therefore logic to consider varactors for this purpose. In the following simulation experiment we will compare the large signal performance of the

DFVS and the NTSVS for this amplitude modulator. It will be shown, that the proposed varactor structure of the present invention, using base band shorts will provide superior performance over the DFVS in this application.

When using ideal variable capacitors, applying a 2 GHz sinusoidal voltage with 3 V signal amplitude at the input of the DVAM, and modulating the values of c_{series} and c_{cross} using a low frequency (base band) sinusoidal signal of 1 MHz, would result in a perfectly multiplied signal, i.e. a two tone signal with an ideal spectrum (1.999 GHz and 2.001 GHz) without any inter modulation effects (especially third order IM).

When using the earlier described distortion free varactor stacks (DFVS) as variable capacitors, the spectrum shown in Fig. 8 is obtained. In terms of third order inter modulation (IM3) this spectrum is very bad.

When using NTSVS devices according to one of the embodiments of the present invention (with an N/x^2 doping profile), again, a low impedance path for the base-band frequencies between the center tap node and RF terminals of the NTSVS devices is provided. If a high valued inductor is used to connect the modulating voltage to the center tap of each NTSVS, these conditions are automatically fulfilled. This is a big advantage in controlling the capacitance to its desired value. The spectrum of the two-tone signal generated using this circuit topology for the same signal conditions as before is given in Fig. 9. As can be noted from this experiment now a very clean two-tone signal is obtained of more than 70 dBc using a 3V amplitude swing at is input. This is an important result since it indicates that using a varactor device with a special but realistic doping profile a close to ideal non dissipative amplitude modulator can be implemented.

In a further embodiment of the present invention, NTSVS varactor elements are used in a polar amplifier circuit, of which the schematic diagram is shown in Fig. 10. Currently, people are considering polar amplifiers concepts to improve on spectral noise, efficiency and flexibility in terms of serving multiple communication standards. One of the common characteristics of these amplifiers is the saturated operation of the active device(s) in order to boost the amplifier efficiency. This saturated operation results in square wave like signal conditions at the output of the amplifier. However, due to the saturated operation of the amplifier, the output power is no longer linearly related to the input power. To solve for this problem currently in polar amplifier implementations, dynamic supply voltage modulation is considered to control the

amount of output power. Although, having some advantages there are the following complications with this approach:

- A highly efficient DC to DC converter is required;
- Switching noise of the DC-to-DC converter requires extensive filtering resulting in the use of unrealistically large circuit implementations;
- Voltage modulation results in AM-PM modulation by the active devices, consequently pre-distortion is required.

An alternative for the dynamic voltage modulated polar amplifier concept is to make use of dynamic loading of the output stage in order to control the amount of output power. Using the DVAM topology as described in the embodiments above, it is quite easy to implement this. Although this can be done in various ways, an exemplary embodiment is shown in Fig. 10. In this Fig. 10 the DVAM (comprising varactor elements D1…D8, shunt inductors Ls1…Ls4, in which the control points of each NTSVS stack are indicated by Vcsd1, Vccd1, Vccd2, and Vcsd2, respectively) performs the dynamic matching and modulation function. The DVAM is controlled by base-band signals which ensure the desired capacitance modulation of the NTSVS devices. All components levels and control signals can be chosen in respect to the desired output power, supply voltage and capacitance tuning range. Additional stubs Z1 and Z2 at the output of transistors T1 and T2 are for the biasing and to provide short conditions for the even harmonics. Additional series resonators are provided using inductances L1, L2 and capacitors C1, C2, respectively. The additional series resonators (center frequency fo) are added to provide a high impedance for the odd harmonics, both are required in order to obtain the highest power added efficiency (PAE). The PAE versus output power when ideal transistors (Default Gummel Poon model) with lossless inductors and varactors are assumed are given in Fig. 11. The power sweep is obtained by changing the static voltages of the varactor in DVAM structure. The graph of Fig. 11a shows the efficiency plotted versus output power for single tone operation of the amplifier using loss-less components. The graph of Fig. 11b provides the results when assuming a Q of 100 for the passive components. In the graph of Fig. 11c the required DC control voltages for the NTSVS elements are plotted against the power (upper trace for the cross connected varactor elements and the lower trace for the series connected varactor elements). It can be observed that a very high efficiency can be obtained over a large power control range. Also the required control

voltages are limited in value Further optimization of the circuit in terms of component values and or impedance levels can reduce the required control voltages even more.

In a further embodiment of the present invention, a direct modulator is proposed which combines a DVAM with a variable phase shifter, as shown in the schematic diagram of Fig. 12 and 13. In this embodiment, the amplitude and phase shift can be set by the control voltages of the NTSVS elements, yielding a polar modulator. Note that such a configuration, can considerably simplify the traditional architecture of a transmitter while still capable of generating the desired complex modulated signals, which are typically in use in wireless communication.

The newly proposed transmitter architecture, using a direct modulator based on NTSVS elements, is given in Fig. 12. A voltage controlled oscillator (VCO, e.g. based on a phased locked loop PLL) 21 provides a carrier wave to a power amplifier (PA) 22. The output of the PA 22 is provided to a direct modulator 23, of which an implementation is shown in Fig. 13 described below. The direct modulator 23 receives control voltages for the NTSVS elements from a digital to analogue converter 24 (D/A), which in its turn is supplied with digital input data for modulating the carrier wave. The output of the direct modulator 23 then provides the modulated signal.

As can be noted from this figure, the NTSVS elements in the modulator are controlled for their capacitance value by the voltages delivered by the digital to analogue converter 24, which operates at, or at a multiple of the base-band frequency. This concept eliminates the need for many RF function blocks in conventional transmitter designs. By controlling the transfer of the polar modulator in a time variant way, the constellation diagram of the desired modulation can be obtained. By also accurately controlling the transitions between the constellation points in the proper fashion, the resulting frequency spectrum at the output of the polar modulator can be adjusted to meet the communication standard requirements under consideration. Note that this basically eliminates the need of intermediate filters in conventional amplifier implementations. Consequently, the resulting transmitter structure is directly capable to serve many different modulation formats, depending on the desired communication standard (e.g. QPSK, BSK, FSK, OFDM etc) by just changing the input of the digital input of the D/A converter 24. Note that now complex modulation schemes can be generated without the need of linear RF circuit blocks for the mixers and power amplifier. This will result in a power reduction of the total transmitter.

Since the NTSVS elements are tunable, also multiple frequency bands can be easily addressed by offsetting the NTSVS values in the network in a proper way (e.g. as discussed above in relation to the DVAM embodiments). The phase shifter, when based on all pass networks or on an artificial transmission line concept, composed out off 5 many LC sections in which the capacitive elements are implemented by NTSVS elements, is wide band in nature itself, yielding a frequency reconfigurable network. Note that such a network can have considerable advantages when aiming for multi-communication standards or multi-frequency band transceivers since no intermediate filters or other (reconfigurable) RF functions are required. The proposed setup can also 10 be useful for low power very high frequency transmitter implementations, since less power for the otherwise power hungry RF circuit blocks are required.

A potential implementation example of such a direct modulator is shown schematically in Fig. 13. In this schematic the DVAM (see embodiment of Fig. 7) is followed by an artificial transmission line composed out off *n* LC sections, each 15 comprising four transmission inductances (Ltrans1...Ltrans4) and a capacitance element Cshunt. The capacitive elements Cshunt are implemented by NTSVS elements. By changing the control voltages of the NTSVS elements, any phase shift or amplitude can be achieved. In this configuration benefit is obtained once again from the properties of the DVAM network that the input impedance tracks with the desired output power, 20 facilitating again the implementation of a highly efficient amplifier but now using a direct modulator with base-band control. It must be mentioned that many network topologies are possible for the amplitude and the phase modulator that result in similar properties as shown here. Also single-ended versions are possible. Essential in all these solutions is a tunable capacitive element that allows fast tuning and that does not cause 25 any inter modulation distortion, the NTSVS device according to embodiments of the present invention being such a component.

Using a DVAM implementation with NTSVS devices according to the present invention, a number of advantages may be achieved:

- Provides low Q impedance transformation (matching) between in and output;
30 - Signal transfer (s_{21}) can be controlled between -1 through 0 to 1;
- Structure can be easily customized for the available tuning range of the varactor;
- Low control voltages required;
- The 180 phase reversal in S_{12} makes it a perfect up-converting mixer;

- No phase variation during tuning (no AM-PM distortion);
- Yields ohmic loading conditions at in- and output over whole tuning range;
- Tuning range can be selected between a fixed impedance and infinity;
- Tuning range can be selected between a fixed impedance and short circuit conditions at fundamental;
- Operating frequency can be easily tuned by changing the bias conditions of the varactors;
- Perfectly linear in combination with NTSVS diode for both sinusoidal as well square wave input signals.

Although the examples given in this document are mostly differential in nature, also single ended versions are very well possible to realize the desired circuit functions (namely, static or dynamic loading / output power control as well phase shifting trough the used of NTSVS based elements). This can serve many actual applications in telecommunication and radar systems.

In Fig. 14, a more detailed view is shown of a Q optimized varactor doping profile for varactor tuned or modulated linear narrowband applications. In these embodiments, the following profile constraints are applied:

- The useful capacitance tuning ratio which is defined by ratio X_{high}/X_{low} ranges for practical and useful implementations from 2 to 15, or even higher ratios.
- Region 1) **Spacer layer.**
  - Spacer layer thickness

    The spacer layer is required to ensure the proper doping relation versus distance in region 2. The thickness of the spacer layer is in principle equal to X_{low}:
    - X_{low} can range from 0.03 μm for low voltage applications ($V_{breakdown}$ <5V) to 0.3 μm for high voltage applications ($V_{breakdown}$ > 40V) (see also table 1). Significantly lower or higher voltage ranges might widen the above constraints

    In practical implementation the exact location of the junction is important in order to avoid linearity degradation when the varactor is applied in the appropriate circuit configuration. The exact location of the junction needs to be at x=0 within a tolerance of +/- $0.2*X_{low}$.
  - Spacer layer doping / sheet resistance

The exact doping of the spacer layer has not too much effect on the intended linearity rather than a shift in control voltage. However the doping of the spacer layer will give rise to an undesired increase in the electric field causing restrictions on the achievable compromise in device breakdown-tuning range-quality factor. For this reason the doping concentration in the spacer layer needs to be restricted. If we assume set that the increase in electrical field due to the doping of the spacer layer should not exceed half the value of the critical electrical field e.g. in silicon $\Delta E = \frac{1}{2} E_{crit} = 3\times10^{5} V/cm$, the related sheet resistance of this layer should be higher then $2385\Omega/\square$. For materials with other values for the critical field strength similar considerations can be made.

- Region 2) **Graded doping profile.**

  This region is responsible for the intended approximated exponential C(V) relation, which in combination with the appropriate circuit configuration yields the highly linear operation. For highly linear operation the grading coefficient m should be between 1.7 and 2.3. The highest linearity in for practical implementations is achieved with m=2.1 rather then 2. This is caused by a cancelling effect that occurs between third and fifth order distortion components. It is very important that the C(V) function does not exhibit any humps and is purely monotonic.

  The doping concentration $N(X_{low})$ follows from the equations 3.7 to 3.11 as given in the detailed description below, and offers the best quality factor for a given breakdown and capacitance tuning range. The value of the effective (activated) doping is typically between 4e18 for devices with a breakdown voltage of <5V and 1e17 for devices with a breakdown voltage of >40V (see table I)

- Region 3) **Buried Layer**

  The buried layer should directly connect to the graded doping profile without introducing significant series resistance. Varactor implementations from the prior art suffer from the low doped connection (series resistance) between the graded profile and the buried layer, lowering the quality factor of the varactor. The capacitance voltage relation in these implementations when the depletion

region extends to this region is not relevant for our application since the intended approximated exponential C(V) relation is violated, yielding a higher distortion. The series resistance offered by the buried layer should be significantly lower than the intrinsic sheet resistance offered by the region 2.
5 Consequently, for high Q varactor implementation we require that the sheet resistance of the buried layer is lower than the intrinsic sheet resistance of region 2 (e.g. see table I in the detailed description below).

In Fig. 15, an exemplary embodiment is shown of a low distortion configuration for varactor tuned / modulated narrowband (transmitter) applications of varactors
10 according to the present invention (with a doping profile as given in Fig. 15) utilizing baseband "shorts" and harmonic "open" conditions for the fundamental and 2nd harmonic between the nodes a and c, and between nodes b and c.

In order to create a low distortion varactor for narrowband modulated signals, the varactor configuration of Fig. 15 should be utilized. The intended tuneable component
15 is connected with its RF terminals a and b to the appropriate place in a tuneable network e.g. adaptive matching network or filter. In difference to the know low distortion varactor configurations, this varactor configuration utilizes baseband "shorts" and "open" conditions for the fundamental and 2nd harmonics between node a and c and node b and c and only works well when using varactors with a doping profile as given
20 in Fig. 14.

In view of Fig. 15 the conditions on the terminal impedance for low distortion operation of narrowband modulated signals (<200MHz band width) are:

$|Z_{Baseband}| \times 10 < |Z_{diode}| @ f_{baseband}$

$|Z_{fundamental}| > 10 \times |Z_{diode}| @ f_{fundamental}$

25 $|Z_{second}| > 10 \times |Z_{diode}| @ f_{2nd\ harmonic}$

in which Z_{diode} is the impedance offered by the varactor diode in reverse bias at the indicated frequency.

These conditions apply for both diodes and should be satisfied simultaneously the individual impedance values offered to D1 and D2 may differ, however they should
30 satisfy the upper requirements. The control voltage $V_{controlD1}$ and $V_{controlD2}$ can also differ in value but should keep the diodes in reverse bias.

In Fig. 16, a simple implementation of a varactor stack is given. Two Schottky diodes (or varactor elements) are formed on top of a buried layer 2, in which each

Schottky diode comprises a metal layer 4a, 4b on top of a doped semiconductor layer 3a, 3b. The doping profile of each doped layer 3a, 3b is according to the embodiments described above (see e.g. Fig. 1, 2a or 14), in which x=0 at the Schottky interface (between metal layer 4a, 4b and doped layer 3a, 3b). A buried layer 2, connecting the
5 two Schottky diodes by a low impedance material, is provided having a low sheet resistance to achieve a high quality factor for large varactor capacitance values. The distance between the two Schottky diodes (indicated by d_S in Fig.16) should be kept to a minimum, to be able to keep the impedance between the two Schottky diodes as low as possible. It is noted that for correct operation, the correct harmonic terminations
10 should be provided at terminals a, b and c indicated in Fig. 16, as described above.

In an integrated process technology to optimize the Quality factor (Q) of a varactor diode with a large capacitance value, typically a finger structure is applied to reduce the influence of the sheet resistance of the buried layer 2. In Fig. 17 a top view of the terminal structure of such an embodiment is shown. It will be apparent to the
15 skilled person that the areas indicated by a, b, and c (corresponding to the terminals a, b, and c of the embodiment shown in Fig. 3a, b and c) correspond to the Schottky diode and control node layers as shown in e.g. Fig. 16. This approach is favoured since the sheet resistance of the buried layer 2 in a integrated process technology can not easily reduced to any extent without rising problems of isolating devices from each other.
20 When implementing a varactor stack for RF applications using the finger approach this method works reasonable well for capacitors with a not too high capacitance value (e.g. below 5pF). Since the conditions for the center tap impedance (terminal c) are less strict than for the RF path the connection scheme for this terminal is more relaxed and can be limited to one or two contacts of the total structure.

25 When considering discrete implementations of the varactor stack with a highly doped substrate the effective resistance of the buried layer 2 and doped substrate between the diodes can be reduced to such an extend that the finger structure can be omitted. The resulting device is no longer isolated, but this is no longer a concern since after cutting the wafer the component can be flip chipped on a hybrid circuit
30 implantation. Note that the harmonic termination of the center tap connection (terminal c, e.g. an inductor) can be placed on the discrete varactor stack component or the hybrid board.

A drastically way to reduce the effective sheet resistance of the buried layer in an integrated process technology which requires isolation between individual components is the use of a backside metal contact in combination with micromachining. The intended structure is shown in Fig. 18a. The varactor stack device is indicated by reference numeral 10, and is formed on a silicon or III-V material wafer 11. As in earlier embodiments, the varactor stack device 10 is formed by providing a buried layer 2 having a low sheet resistance, on which two Schottky diodes are formed by doped layers 3a, 3b and metal layers 4a, 4b, respectively. Between the Schottky diodes and surrounding the metal layers 4a, 4b, a layer of oxide 12 is provided. Note that in this figure the backside of the wafer 11 is etched away until the buried layer 2 is reached. This etching can be controlled using an etch stop layer e.g. buried oxide in the case of using a silicon on isolator wafer or by similar techniques in III-V materials. By making contact holes in the etch stopping layer and directly contacting the buried layer 2 or the lightly doped N region with a thick metal (back metal layer 15), the effective resistances between the diodes in the RF path can be seriously reduced (the two varactor elements being connected by a low impedance (combination of) material(s). Consequently, the sheet resistance of the buried layer 2 is less an issue since the back metal layer 15 takes care for the conduction of the RF signal. The control terminal 5 (control node c of the equivalent diagram of Fig. 3a-c) can be connected to the frontside of the wafer through a via. As a result no finger structures are anymore required on the front side resulting in an effective reduction of the required wafer area and an improved Q factor. Note that in this approach there are no high quality vias to the front side of the wafer required The only connection to the front side of the wafer is for the implementation of the center tap terminal 5 but since this terminal should only provide a connection for the DC and baseband signals the impedance requirements are quite relaxed for this connection. In Fig. 18b a top view of the varactor device 10 of Fig. 18a is shown, indicating the positions of the metal contacts 4a, 4b, 5. Note that finger structures (such as in the embodiment of Fig. 17) at the top side are no longer needed due to the reduced resistance of the backside metal connection 15. The structure can be further improved and customized by taking measures to improve the mechanical stability, e.g. by gluing or growing mechanical support layers.

The present invention, its implementations and theoretical background may be understood in more detail from the following.

Novel High-Linearity Narrow Tone Spacing Varactor Stack

Abstract: Two varactors with an identical "exponential" C(V) relation in anti-series configuration will, in combination with the proper harmonic terminations for the device terminals, exhibit for narrow band signals a very high linearity and range in combination with a low control voltage. The resulting component proves to be an enabling component for the implementation of tuneable matching networks, filters, phase shifters and amplitude modulators. It is shown that specific N/x^2 doping profile is required for exact IM3 cancellation. In practical implementations however, the linearity at high signal levels is limited by a combination of third-order and fifth-order non-linearities. With this knowledge the doping profile constrains to obtain high linearity for practical implementation of these devices are investigated. Also the specific requirements on the harmonic terminations in relation to the realized tunable capacitance are investigated in terms of the maximum bandwidth of the modulated signal for which the proposed configuration behaves linear. The requirements on the doping profile to achieve and good compromise between Q-factor, tuning-range and breakdown voltage is discussed in detail. In conclusion the influence of the device layout on the Q-factor is investigated.

I. Introduction

Next-generation wireless systems, such as multi-mode transceivers and "cognitive radios," require circuit techniques that facilitate RF adaptivity. Some examples of adaptive circuits include tunable filters, tunable matching networks for low-noise and power amplifiers. An ideal tuning element for these applications will exhibit extremely low loss, low dc power consumption, high linearity, ruggedness to high voltage and high current, wide tuning range, high reliability, very low cost, low area usage, and be continuously tunable, with a high tuning speed.

PIN Diodes or GaAs PHEMTs are widely used today for these challenging applications. However, these solutions are considered to be too expensive, or consume too much dc power, to be an acceptable long term solution for cost and performance sensitive applications.

This limitation has triggered an intensive search for alternatives that do not suffer from the drawbacks of traditional approaches. One example is the MEMS capacitor,

which in its most popular implementation is able to switch between two fixed capacitance values. MEMS capacitors provide a very high Quality Factor (Q) and extraordinarily high linearity, but they require non-standard processing and packaging techniques, high control voltages, and their reliability and switching speed are still poor compared to semiconductor-based solutions. Other proposed tuning techniques, based on voltage-variable dielectrics, exhibit similar drawbacks of manufacturability and performance.

In view of this urgent need, more simple tunable elements like varactor diodes would seem to be a logical choice for implementing RF adaptivity. However, their inherently nonlinear behavior disqualifies them for use with modern communication standards characterized by high peak-to-average power ratios, and their related Q factors are usually too low at the microwave frequencies of interest for the most demanding applications.

In order to overcome these drawbacks, recently varactor diode-based circuit topologies and a high performance varactor diode process technology has been presented [2-3], which, for a given diode power-law capacitance coefficient ($n \geq 0.5$), can act as variable capacitors with extremely low or - in the special case of $n=0.5$ - theoretically no distortion [1,2,4]. However, the proposed solutions have linearity constrains for modulated signals or signals with narrow tone spacing when considering practical implementations. The novel high-linearity narrow tone spacing varactor stack (NTSVS) presented here aims to overcome these limitations, in terms of linearity for narrowband signals, sensitivity to leakage, high control voltage and capacitance tuning range.

The operation theory of this IM3 distortion free varactor stack is given in Section II. The requirement of doping profile and compromise of tuning range, breakdown voltage and Q-factor are discussed in Section III. The influence of fifth order intermodulation distortion on the linearity is considered in Section IV. The practical implementation issues like process deviation and layout are discussed in Section V and VI respectively.

II. Theory of Operation

The novel high-linearity narrow tone spacing varactor configuration is based on a Volterra analysis of the circuit in Fig. 1.

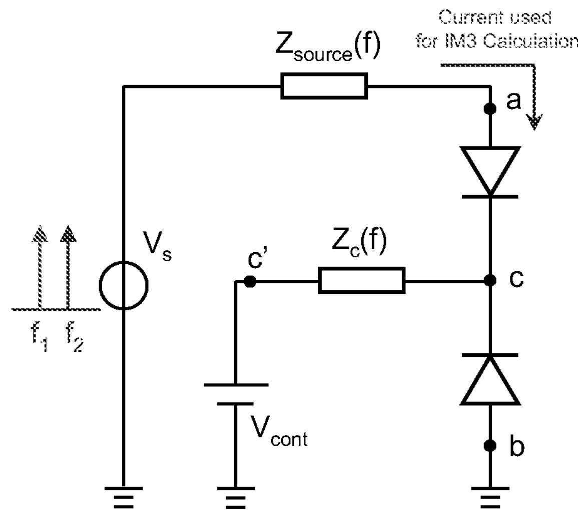


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Fig. 1. Schematic used for the Volterra analysis of the anti-series varactor diodes circuits

When solving the IM3 component of Fig.1., assuming $Z_{c(f2-f1)}$=0, while $Z_c(f)$ is infinitely high for all other frequency components, we find after some manipulations
25 the following IM3 cancellation condition for very narrow tone spacing $(\Delta f \to 0)$:

$$IM3_{BBshort} = \frac{(2c_1^{\ 2} - 3c_0c_2)g_s^{\ 2}s_c A^2}{4c(2g_s - s_c c)(2g_s + s_c c)^2} \qquad (2.1)$$

in which: $c_0 = \frac{dq(v)}{dv}, \quad c_1 = \frac{1}{2}\frac{d^2q(v)}{d^2v}, \quad c_2 = \frac{1}{6}\frac{d^3q(v)}{d^3v} \qquad (2.2)$

are the Taylor coefficients of the varactor diode, g_s is the source conductance ($1/Z_{source}(f)$) and s_1 and s_2 are the complex frequencies while A is the amplitude of the
30 voltage signal source.

By solving the differential equation, $3c_0c_2 - 2c_1^{\ 2} = 0$, an exponential C(V) relation is found that satisfies the IM3 cancellation condition by providing the optimum Taylor coefficients,

$$C_{BBshort}(V) = a_1 e^{a_2 V} \qquad (2.3)$$

35 In this relation a_1 and a_2 indicate the integration constants, which add some flexibility to our solution. Note that any choice of a_1 and a_2 will satisfy equation (2.1) yielding perfect cancellation of the IM3 distortion component for narrow tone spacing. It should be stressed that for this IM3 cancellation, it is essential that for the base-band frequencies there is a low AC impedance path (this is relative to the AC impedance
40 offered by the varactor capacitance itself) between the center node c and the RF terminals a and b. Simultaneously, for the high frequency components (fundamental,

and higher harmonics) there the AC impedance between the node c and a or node c and b must be high (this again relative to the AC impedance offered by the varactors itself at these frequency components).

5

III. Doping Profile and Performance Compromise

A. Doping Profile

Based on Volterra series and differential equation (Eq.(2.1)), the desired capacitance function has been found. Now we need to determine the related doping profile. For this purpose we assume a one-side junction (e.g. a Schottky diode) and 10 solve for the doping profile using [5]

$$N(x) = \frac{C(V)^3}{q\varepsilon}\left(\frac{dC(V)}{dV}\right)^{-1} \qquad (3.1)$$

With,

$$x = \frac{\varepsilon}{C(V)} \qquad (3.2)$$

Making use of the upper relations, it can be proven that the required doping profile 15 for an exponential capacitance voltage relation is

$$N(x) = \frac{N}{x^2} \qquad (3.3)$$

In which N is a doping concentration constant to be defined. It should be noted that the upper formulation of the doping profile is singular for x=0, consequently, measures to avoid this singularity must be taken. In order to explain how the doping profile for 20 the base-band shorted varactor stack should be defined, we consider Fig. 14 as attached to the present application.

In this figure, the idealized doping profile is indicated by the black drawn line. Since we can not provide an infinitely high or extremely low doping concentration we have to break-off this relation at x_{low} and x_{high}. Doing so we automatically define the 25 useful capacitance tuning range (C_{ratio}) since the capacitance is inversely proportional with the distance x.

$$C_{ratio} = x_{high} / x_{low} \qquad (3.4)$$

To achieve / maintain the “exponential” C(V) relation a “spacer” layer is required in order to satisfy the N/x^2 doping versus depth relation with respect to the junction 30 position (e.g. a doubling of the distance with the junction should result in a 4 times lower doping concentration). This layer, which in the useful varactor diode operation is depleted, preferably does not increase the electric field significantly to avoid reduced

device breakdown and capacitance tuning range. To achieve this, the doping concentration of this filling layer must be kept low in respect to $N(x_{low})$ In appendix E this is analyzed resulting in a lower bound on the effective sheet resistance of this spacer layer. Making use (for simplicity reasons) of the assumption that low doped
5 “spacer” layer consumes the total built-in voltage, while the applied voltage is completely used to deplete the N/x^2 region, the exponential C(V) relation can be achieved in terms of the technology parameters (See Appendix A), which is given by

$$C_j(V_R) = \frac{A \cdot \varepsilon_s}{x_{low}} \cdot \exp\left(-\frac{\varepsilon_s}{q \cdot N(x_{low}) \cdot x_{low}^{\ 2}} \cdot V_R \right) \qquad (3.5)$$

where V_R is the reversely applied voltage and the constant ($A \cdot \varepsilon_s / x_{low}$) is the zero
10 bias capacitance value.

In the practical situation, we can always choose an appropriate doping concentration of the “spacer layer” to make the assumption above valid. However, significant doping of the spacer layer will increase the electric field at the varactor junction, resulting in a lower maximum operation voltage lower Q than intended.
15 Hence, for the sake of breakdown voltage and Q optimization, the doping concentration of “spacer” should be kept a low value (Restrictions at this point are evaluated in Appendix E). In this situation, the depletion distance (x'_{low}) at zero applied voltage can be larger than x_{low} and consequently the C(V) relation has to be modified to (Also see Appendix A):

20
$$C_j(V_R) = \frac{A \cdot \varepsilon_s}{x'_{low}} \cdot \exp\left(-\frac{\varepsilon_s}{q \cdot N(x_{low}) \cdot x_{low}^{\ 2}} \cdot V_R \right) \qquad (3.6)$$

The formulation above indicates that the zero biased capacitor value is now $A \cdot \varepsilon_s / x'_{low}$, which will reduce the tuning range by a factor of x'_{low} / x_{low} for the same junction depth (x_{high}). It should be noted that although the tuning range is reduced, the exponential C(V) relation remains, which make the IM3 distortion cancellation
25 condition still valid. In addition, due to the same doping profile in the N/x^2 region, the coefficient a_2 in Equation (2.3) has no change also. At a later stage in this document we investigate on the doping profile constrains for practical implementations.

B. Performance Compromise

30 Based on the equations above, we can optimize the maximum operation voltage (V_{max}), tuning range and Q-factor of the varactor. For simplicity, we assume that the lowly doped “spacer” region consumes the total built-in voltage without increasing the

electric field and then V_{max}, tuning range and Q-factor at zero applied voltage of the varactor are given by

$$Tuning_range = \frac{x_{high}}{x_{low}} \qquad (3.7)$$

$$V_{max} = \frac{q \cdot N(x_{low}) \cdot x_{low}^2}{\varepsilon_s} \cdot \left(\ln \frac{x_{high}}{x_{low}} \right) \qquad (3.8)$$

5

$$R(V_R = 0) = \int_a^b \rho(x) \cdot \frac{dx}{A} = \frac{1}{A \cdot q \cdot \mu_n \cdot N(x_{low}) \cdot x_{low}^2} \left(\frac{x_{high}^3}{3} - \frac{x_{low}^3}{3} \right) \qquad (3.9)$$

$$Q(V_R = 0) = \frac{\left| \frac{1}{j\omega C} \right|}{R} = \frac{3 \cdot q \cdot \mu_n \cdot N(x_{low})}{\omega \cdot \varepsilon_s \cdot \left[\left(\frac{x_{high}}{x_{low}} \right)^3 - 1 \right]} \qquad (3.10)$$

Since we assumed the electric field initiated from the lowly doped “spacer” layer can be omitted for the sake of simplicity, we can use the electric field at the edge of lowly doped region and the N/x^2 region to estimate the maximum electric field, which
10 is given by

$$E_{max} = \frac{q \cdot N(x_{low}) \cdot x_{low}^2}{\varepsilon_s} \left(\frac{1}{x_{low}} - \frac{1}{x_{high}} \right) \leq 6 \times 10^5 V/cm \qquad (3.11)$$

Based on the Equation (3.7)-(3.11), one can improve for the Q-factor (values > 300@2GHz are feasible in silicon), breakdown voltage (values > 100V are feasible in silicon for a constrained capacitance tuning range and quality factor) or tuning range
15 (values > 15 are feasible in silicon for a constrained breakdown voltage and Q factor). The maximum achievable Q-factors at zero bias for different V_{max} and tuning ranges are listed in Table 1. In this table also the related profile parameters are given which result in the optimum Q factor for a given breakdown voltage and capacitance tuning range. The mobility used in this optimization is $1000 cm^2/V{\cdot}s$ representing a silicon
20 implementation. One can improve the Q-factor by using other technologies with a higher mobility like GaAs, which due to its roughly 5x higher mobility compared to silicon will yield an approximately 5 times higher Q-factor for a given doping profile. Also the use of wideband gap materials can be beneficial since this allows the use of higher doping concentrations and electric field conditions at the device junction.
25

Table1. Optimized Q-factor @ 2GHz for given tuning range and V_{max} ($\mu_n = 1000 cm^2/V \cdot s$), also the related doping profile parameters are indicated.

Tuning Range	Parameters	V_{max}=5V	V_{max}=10V	V_{max}=20V	V_{max}=40V
3	$N(x_{low})$	$1.18e18$	$5.87e17$	$2.95e17$	$1.451e17$
	x_{low}	$0.05\mu m$	$0.1\mu m$	$0.2\mu m$	$0.4\mu m$
	x_{high}	$0.15\mu m$	$0.3\mu m$	$0.6\mu m$	$1.21\mu m$
	C_{jo}	$2.07 ff/\mu m^2$	$1.04 ff/\mu m^2$	$0.52 ff/\mu m^2$	$0.26 ff/\mu m^2$
	R_{sheet} (intrinsic)	$3.5k\Omega/\square$	$3.55k\Omega/\square$	$3.5k\Omega/\square$	$3.6k\Omega/\square$
	$N(fill)_{max}$ (50% of E_{max})	3.88e17	1.94e17	9.7e16	4.85e16
	Q	1634	817	408	205
6	$N(x_{low})$	$1.2e18$	$6.14e17$	$3e17$	$1.51e17$
	x_{low}	$0.039\mu m$	$0.077\mu m$	$0.155\mu m$	$0.31\mu m$
	x_{high}	$0.233\mu m$	$0.46\mu m$	$0.93\mu m$	$1.86\mu m$
	C_{jo}	$2.65 ff/\mu m^2$	$1.33 ff/\mu m^2$	$0.67 ff/\mu m^2$	$0.33 ff/\mu m^2$
	R_{sheet} (intrinsic)	$7.3k\Omega/\square$	$7.1k\Omega/\square$	$7.2k\Omega/\square$	$7.1k\Omega/\square$
	$N(fill)_{max}$ (50% of E_{max})	4.97e17	2.49e17	1.24e17	6.22e16
	Q	206	103	51.5	26
9	$N(x_{low})$	$1.3e18$	$6.48e17$	$3.24e17$	$1.62e17$
	x_{low}	$0.034\mu m$	$0.067\mu m$	$0.134\mu m$	$a = 0.27\mu m$
	x_{high}	$0.303\mu m$	$0.607\mu m$	$1.21\mu m$	$2.42\mu m$
	C_{jo}	$3.05 ff/\mu m^2$	$1.53 ff/\mu m^2$	$0.77 ff/\mu m^2$	$0.39 ff/\mu m^2$
	R_{sheet} (intrinsic)	$10.7k\Omega/\square$	$11k\Omega/\square$	$10.7k\Omega/\square$	$10.8k\Omega/\square$
	$N(fill)_{max}$ (50% of E_{max})	5.71e17	2.85e17	1.43e17	7.13e16
	Q	65.6	32.8	16.4	8.2
12	$N(x_{low})$	$1.38e18$	$6.84e17$	$3.47e17$	$1.72e17$
	x_{low}	$0.031\mu m$	$0.062\mu m$	$0.123\mu m$	$0.246\mu m$
	x_{high}	$0.369\mu m$	$0.74\mu m$	$1.47\mu m$	$2.95\mu m$
	C_{jo}	$3.34 ff/\mu m^2$	$1.67 ff/\mu m^2$	$0.84 ff/\mu m^2$	$0.42 ff/\mu m^2$

	R_{sheet} (intrinsic)	$14.6k\Omega/\square$	$14.3k\Omega/\square$	$14.2k\Omega/\square$	$14.3k\Omega/\square$
	$N(fill)_{max}$ (50% of E_{max})	6.26e17	3.13e17	1.56e17	7.82e16
	Q	29.5	14.7	7.4	3.7
15	$N(x_{low})$	$1.45e18$	$7.24e17$	$3.62e17$	$1.81e17$
	x_{low}	$0.029\mu m$	$0.057\mu m$	$0.115\mu m$	$0.23\mu m$
	x_{high}	$0.43\mu m$	$0.86\mu m$	$1.72\mu m$	$3.45\mu m$
	C_{jo}	$3.57 ff/\mu m^2$	$1.79 ff/\mu m^2$	$0.895 ff/\mu m^2$	$0.448 ff/\mu m^2$
	R_{sheet} (intrinsic)	$18k\Omega/\square$	$18k\Omega/\square$	$17.9k\Omega/\square$	$18k\Omega/\square$
	$N(fill)_{max}$ (50% of E_{max})	6.69e17	3.34e17	1.67e17	8.36e16
	Q	15.6	7.8	3.9	2

IV. The Influence of IM5 distortion on the Linearity

A. Fifth-order Volterra Series Analysis of the varactor stack

Although the exponential C(V) relation is very effective to cancel the third order intermodulation (IM3), fifth-order intermodulation (IM5) is still present and will form the most troublesome distortion component in this varactor stack. In order to study the influence of IM5 on the linearity, we developed the fifth-order Volterra Series. For the sake of IM3 cancellation, we keep the same termination conditions at the center tap for the various frequency components ($Z_{c(f2-f1)}$=0, while Z_c is infinitely high for all other frequency components)

Substituting C(V) relation expressed as Equation (2.3) into the IM5 formulation yields, for the general case ($\Delta f \neq 0$), quite troublesome relations, however when we take the extreme situation, $\Delta f \to 0$ and $Z_{source}(f) \to 0$, the expression for the IM5 products that appear at the IM3 frequencies, $2f_1$-f_2 and $2f_2$-f_1, can be drastically simplified yielding:

$$IM5 = \frac{5}{48 \times 2^4} \cdot a_2^{\ 4} \cdot A^4 \qquad (4.1)$$

where $a_2 = -\frac{\varepsilon_s}{q \cdot N(x_{low}) \cdot x_{low}^{\ 2}}$ is the exponential coefficient of C(V) relation and A is the amplitude of the two-tone test signal at the fundamental frequencies. In order to be consistent with our further discussions, we replace A by V_{RF_peak}, which represents

the peak amplitude of the two-tone input voltage signal. Consequently in a two-tone test, V_{RF_peak} equals two times A. So, Equation (4.1) can be modified as

$$IM5 = \frac{5}{48 \times 2^4} \cdot a_2^{\ 4} \cdot \left(\frac{V_{RF_peak}}{2} \right)^4 \qquad (4.2)$$

Based on Equation (4.2), the fifth-order input intercept point (IIP5) can be

5 expressed as

$$IIP5(V) = 4 \times \left(\frac{48}{5} \right)^{1/4} \times \frac{1}{a_2} = \frac{7.04}{a_2} \qquad (4.3)$$

Note that the IIP5(V) is independent of the applied control voltage at the center pin but only depends on the grading coefficient a_2, which can be chosen freely to adjust the tuning range.

10

B. Linearity Comparison with Distortion Free Varactor Stack (DFVS)

We claimed in the very beginning that our varactor stack is distortion “free” (through IM3 cancellation) at narrow tone-spacing, however, in practice, the IM5

15 distortion is the limiting factor. The task now is to compare the linearity of our novel varactor stack with the existing ones and check the achievable improvement in linearity. For this purpose, we use the distortion free varactor stack (DFVS) [4], which is also aiming for high linearity performance. Before comparing the linearity, the tuning range and maximum operation voltage should be chosen comparable. According

20 to [4], for distortion free operation, the power law exponent must be equal to 0.5 and the center tap resistance should be as large as possible. Here we use the example of 5pf (stack structure) with V_{max}=8V and Tuning range=3 for comparison. Consequently, the corresponding exponential coefficient for our narrow tone spacing varactor stack (NTSVS) should be equal to 0.137 (see Equation (2.3) and (3.8)). The center tap

25 impedances are 1Mohm for the DFVS and 10nH for NTSVS as shown in Fig. 3. Although IIP3(V) and IIP5(V) are the generally accepted figure of merit for linearity, it is not appropriate to apply these two parameters here since we are comparing IM3 with IM5 (Due to the finite impedance applied in the center tap for DFVS, IM3 is still the dominant factor for nonlinearity at narrow tone spacing, while IM5 constrains the

30 linearity of NTSVS there). Note that even if the IIP3(V) and IIP5(V) are the same, the dBc between fundamental signal and third or fifth (it depends on which distortion is the main factor for nonlinearity) distortion signal will be variant in the operation voltage

range due to different slope. Hence, we will monitor dBc as function of the RF operation voltage for comparison. To avoid the clipping through device breakdown and forward bias of the diodes (see Fig. 5 later), we choose the control voltage (4V) to half of V_{max} (the diode breakdown voltage) consequently the maximum allowable peak
5 magnitude RF input voltage (V_{RF_peak}) is 8V. The comparison of the results are shown in Fig. 4 with V_{RF_peak} of 2V, 4V, 6V and 8V.

Fig.4 indicates that when a full swing (V_{RF_peak}=8V) RF input signal is applied on the varactor stack, 26.4dBc improvement can be achieved; when V_{RF_peak} equals to 2V, an improvement of -49.3dBc is achievable. One may find that the improvement is only
10 available when tone spacing is smaller than 5MHz for V_{RF_peak}=2V and 300kHz for V_{RF_peak}=8V (This value depends on the relative value between the center tap inductor and the capacitance of varactor stack.), since our linearity optimization is aiming for the narrow tone spacing. For large tone spacing situations, DFVS will be a good alternative.

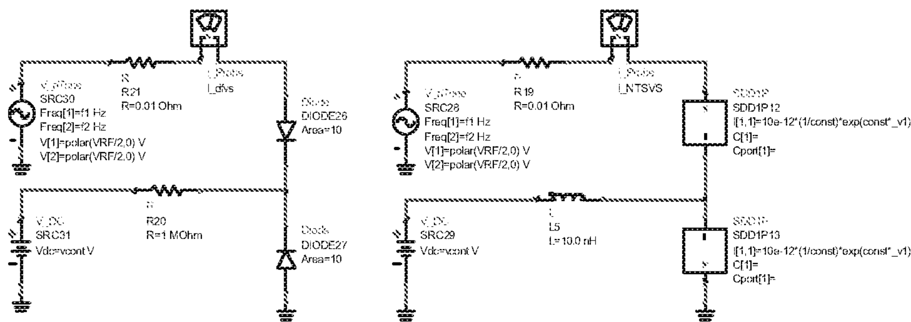

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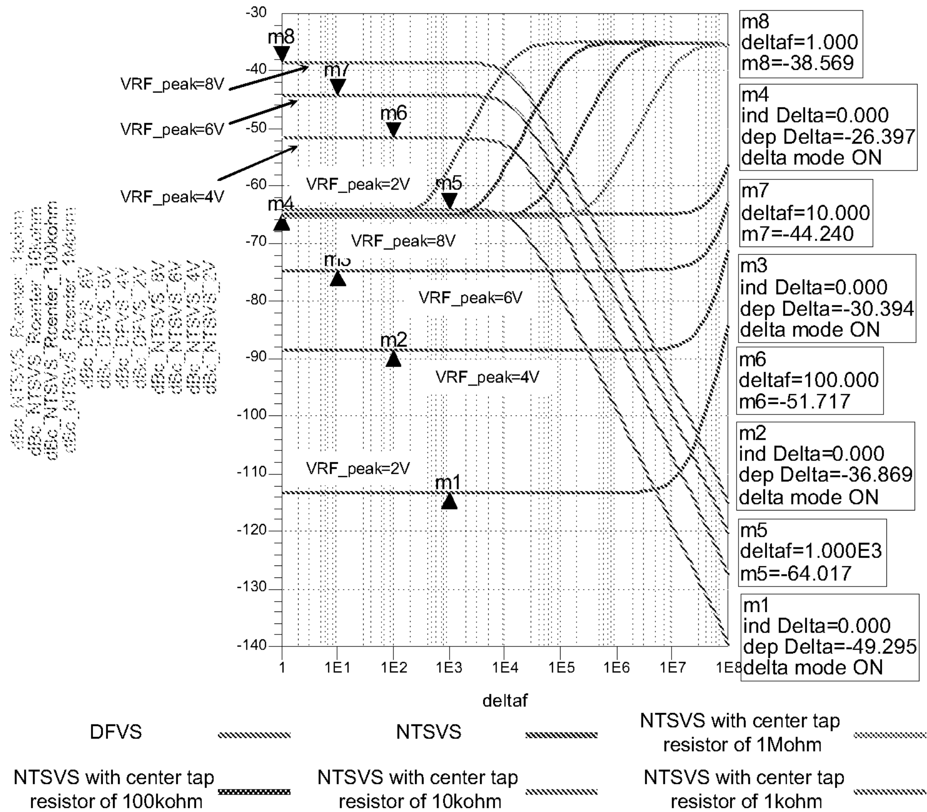
Fig. 3. Schematic of linearity comparison
(a) Conventional "Distortion Free Varactor Stack" based on uniformly doped varactors.
(b) New "Narrow Tone Spacing Varactor Stack" stack based on N/x^2 doped varactors.



20 **Fig. 4. Two-tone linearity comparison (f_{center} = 2GHz) between DFVS and NTSVS using a control voltage of 4V**

The ideal center tap impedance, as mentioned in Section II, is zero at baseband and infinitely high for all other frequency components. An inductor, which offers low
25 impedance at baseband frequency and high impedance at RF frequencies, is a good alternative. However, a 10nH inductor as we applied above normally consumes a larger chip area than a resistor, even if a low Q-factor inductor is acceptable. Actually, a carefully selected resistor can also approximately satisfy the requirement of the center tap impedance since the capacitance of the varactor exhibits a very high impedance at
30 baseband frequency and low impedance at RF frequencies. Fig. 4 shows the simulation results with V_{RF_peak}=8V for different center tap resistances. Comparing with the result of the 10nH center tap inductance with the same control voltage, V_{RF_peak} and varactor parameters (including the capacitor value and grading coefficient), one may find that the linearity with these center tap resistance has the same linearity as that of the
35 inductance at narrow spacing frequency, while the baseband frequency increases, the

linearity becomes worse. Since the lower the center tap resistance the wider bandwidth, we may say the baseband center tap impedance requirement is the limitation for the achievable linearity. As indicated in Fig.4, the widest bandwidth can be achieved with a 1kohm center tap resistor, which will restrict the Q-factor at zero bias to 250 for a 5pf capacitance (stacked value) and the Q-factor will become worse with the increase of the control voltage (for the case tuning range=3, the Q-factor will be reduced to 83 when $V_{cont}=V_{max}$). Consequently, it can be concluded that the center tap resistor can be applied for narrow band (below 500kHz) applications with a reasonably high Q-factor (roughly 100).

C. Compromise of Linearity, Q-factor, V_{max} and Effective Tuning Range

In Section III, linearity wasn't taken into account and the tuning range was not restricted by the RF voltage swing, and therefore the varactor stack is regarded as an ideally linear component with no constrains on the applied signals at all. For these reasons, it is useful to repeat this analysis for the tuning range including constrains related to breakdown, forward biasing and linearity.

In order to maintain acceptable linearity, each of the individual varactor diodes in the stack must remain sufficiently reversed biased during large-signal operation and consequently the useful range of capacitance variation will be reduced by the magnitude of the applied RF signal. For this reason, the tuning range in the Section III is replaced by the effective tuning range, which is a function of V_{max} and V_{RF_peak}. Since the peak magnitude of the RF input signal is V_{RF_peak} and the RF impedance between node c and c' in Fig.1, the RF peak magnitude obtained by each individual diode is half of V_{RF_peak}. Hence, the DC bias voltage at the center tap must be higher than $V_{RF_peak}/2$ to avoid the forward bias and lower than $V_{max}-V_{RF_peak}/2$ to keep away from the clipping or device breakdown. For simplicity, the "switch on voltage" at which the varactor component starts to exhibit its desired exponential capacitance voltage behavior is defined as zero here.

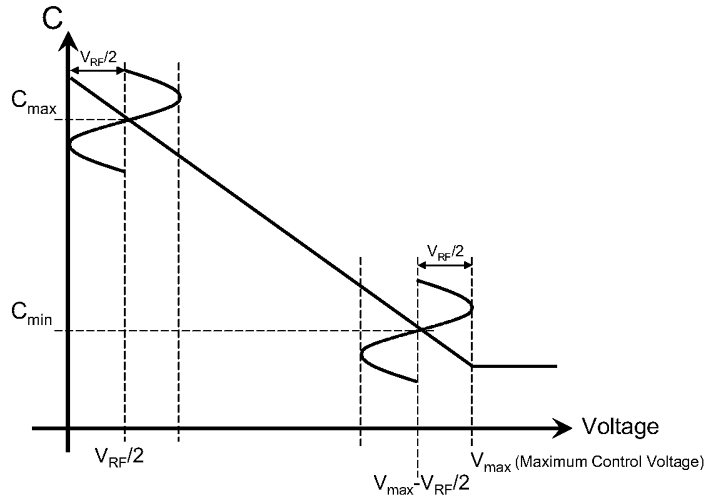


Fig. 5. Illustration of the definition of effective tuning range

As illustrated in Fig. 5, when the diode is biased at $V_{RF_peak}/2$, the corresponding capacitor value is C_{max}; when the diode is biased at V_{max}-$V_{RF_peak}/2$, the corresponding capacitor value is C_{min}. Therefore, the effective tuning range can be written as

$$Eff_Tuning = \exp\left[a_2 \cdot \left(V_{\max} - V_{RF_peak}\right)\right] = Tuning_range \cdot \exp\left(-a_2 \cdot V_{RF_peak}\right) \quad (4.4)$$

where *Tuning_range* is the original tuning range defined in Equation (3.7).

From Equation (4.4), the C(V) exponential a_2 can be expressed as a function of V_{max}, V_{RF_peak} and *Eff_Tuning*,

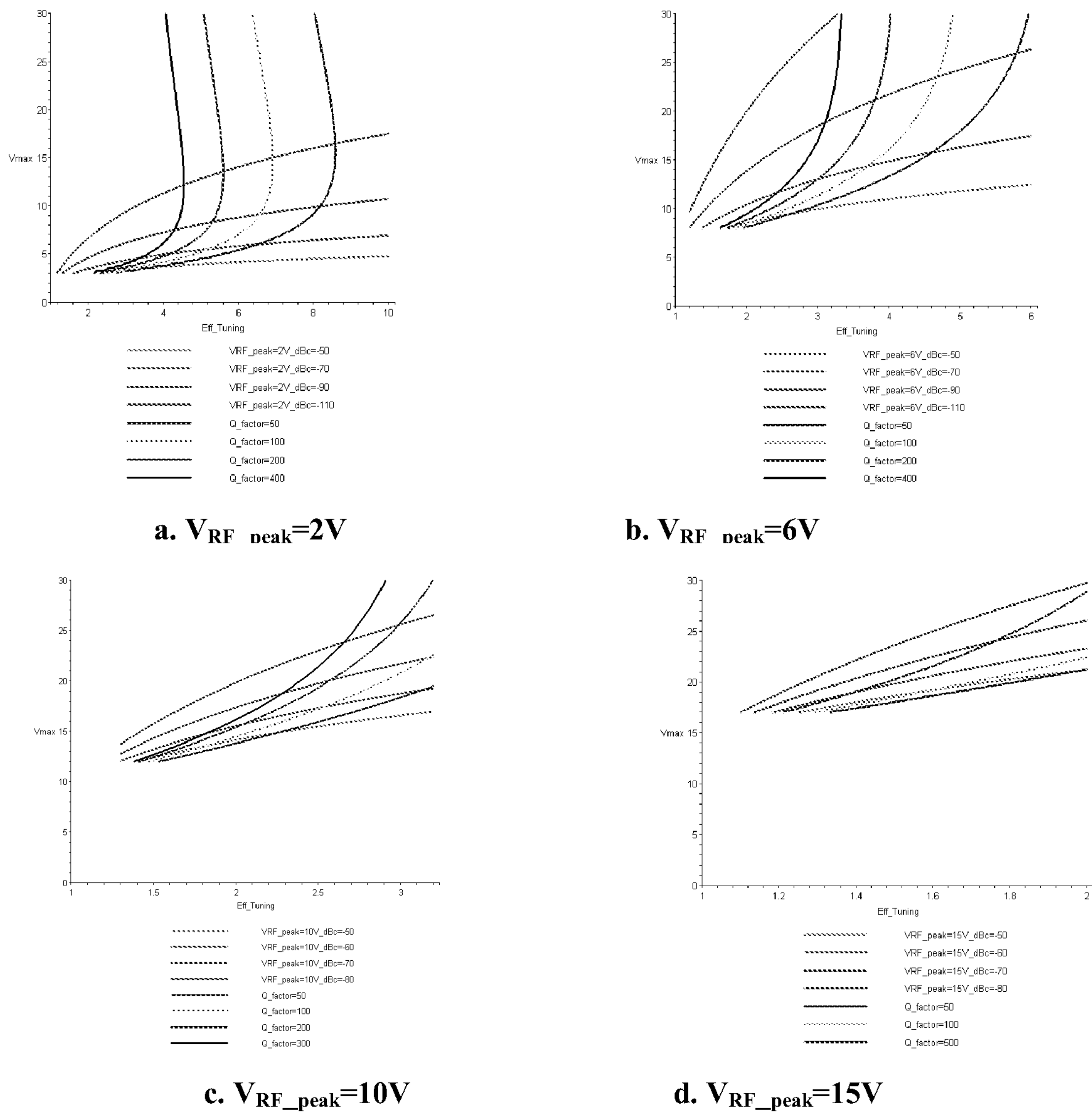
$$a_2 = \frac{\ln\left(Eff_Tuning\right)}{V_{\max} - V_{RF_peak}} \quad (4.5)$$

Substituting the formulation above into Equation (4.2) and taking the dB, the IM5 in dBc can be written as

$$IM5_in_dBc = 4 \cdot 20 \cdot \lg\left(\frac{1}{7.04} \cdot \frac{\ln\left(Eff_Tuning\right)}{V_{\max} - V_{RF_peak}} \cdot V_{RF_peak}\right) \quad (4.6)$$

Based on Equation (4.4), (3.10) and (3.11), the Q-factor of varactor can be rewritten as a function of V_{max}, V_{RF_peak} and *Eff_Tuning* also. Therefore, we can plot a set of new figures including the effective tuning range, Q-factor and V_{max} for different V_{RF_peak} values as shown in Fig. 6. In order to give an indication on the achievable performance when using GaAs technology, the calculation of Fig. 6 is based on the mobility of GaAs ($\mu_n = 6000 cm^2 / V \cdot s$). For the silicon situation, one can simply divide the Q-factor by a factor of 5-6.

Fig.6 shows that the performance of the varactor should be traded off. For those case that V_{RF_peak} is small, a Q-factor of 400, IM5 of -110dBc, effective tuning range of 4 and breakdown voltage of 12V varactor is achievable (See Fig.6.a). In the case of a large signal input, high Q-factor, high linearity and high breakdown voltage can still be 5 achieved at the cost of effective tuning range as indicated in Equation (4.4).



a. V_{RF_peak}=2V **b. V_{RF_peak}=6V**

c. V_{RF_peak}=10V **d. V_{RF_peak}=15V**

Fig. 6. Compromise of linearity, Q-factor, V_{max} and effective tuning range (GaAs material with $\mu_n = 6000 cm^2 / V \cdot s$) Note that Vmax must be larger than V_{RF_peak} to avoid clipping and 30 forward bias. A reasonably large effective tuning range, Vmax and Q-factor can be achieved on the condition that VRF_peak is small, which is consistent with Eq. (4.6).

V. The Influence of Process Deviation on the Linearity

A. Process Deviation

Besides the required harmonic termination the main issue for the linearity of our narrow tone spacing varactor stack is the exponential C(V) relation, which requires a
5 N/x^2 doping profile as shown in Fig.2. However, during practical implementation, the real doping profile can / will deviate somewhat from the desired profile.

In Section II, we found as long as the C(V) relation can be written as Equation (2.3), the IM3 distortion will be cancelled. Recalling the derivation of C(V) relation in Appendix A, there are two logic deviations of the profile that will cause a violation of
10 the exponential C(V) relation:

1. The slope of the doping concentration is not equal to $1/x^2$.
2. The thickness of "spacer" layer is not equal to x_{low}, resulting in an offset of the origin of the N/x^2 region. Note that a doubling of the distance with the junction should result in a 4 times lower doping concentration. If the origin of N/x^2
15 region changes, this condition is violated consequently and the N/x^2 doping relation will not appear as a straight line on the logarithmic plot of the doping concentration versus the logarithm of the distance (x).

For the first case, we can assign an arbitrary power (m) for the slope in doping concentration, and consequently the C(V) relation (see Appendix B) can be written in
20 an explicit form:

$$C_j(V_R) = A\frac{\varepsilon_s}{x_0(V_R)} = \frac{A\cdot\varepsilon_s}{\left[\dfrac{\varepsilon_s\cdot(m+2)\cdot V_R\cdot x_{low}{}^{m}}{N(x_{low})} + x_{low}{}^{m+2}\right]^{\frac{1}{m+2}}} \qquad (5.1)$$

For the second case, we can assume the origin of the distance (x) is offset by a factor of Δx, and consequently the C(V) relation (see Appendix C) can only be written in an implicit form:

25

$$V_R = \frac{q\cdot N(x_{low})\cdot x_{low}{}^{2}}{\varepsilon_s}\left[\ln\left(\frac{\dfrac{C_j}{A\cdot\varepsilon_s}-\Delta x}{x_{low}}\right) + \frac{\Delta x}{x_{low}} - \frac{\Delta x}{\dfrac{C_j}{A\cdot\varepsilon_s}-\Delta x}\right] \qquad (5.2)$$

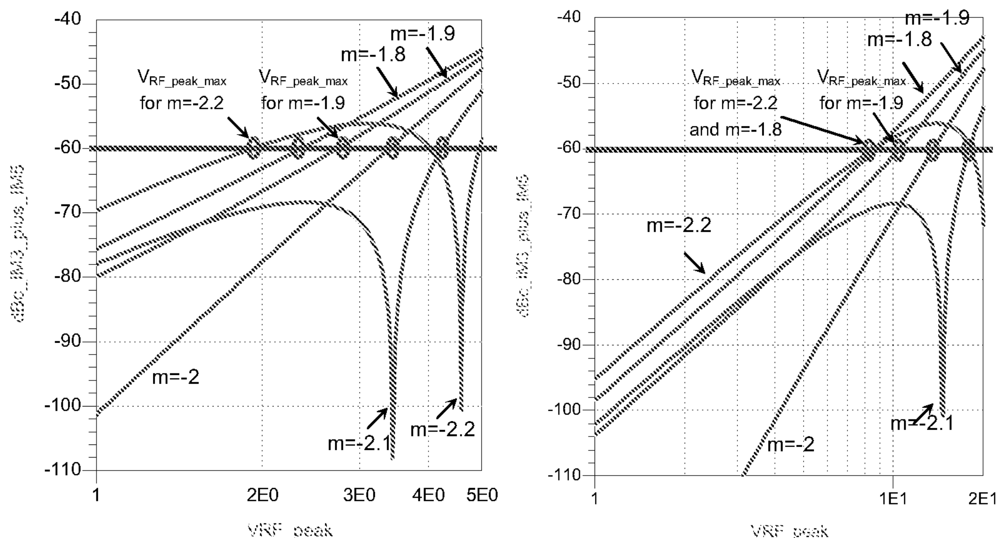
If we combine these two process deviation together, the new C(V) relation (see Appendix D) can be written in the following implicit form:

$$V_R = \frac{q\cdot N(x_{low})\cdot x_{low}{}^{-m}}{\varepsilon_s}\cdot\left[\frac{\left(\dfrac{C_j}{A\cdot\varepsilon_s}-\Delta x\right)^{m+2} - x_{low}{}^{m+2}}{m+2} + \frac{\Delta x}{m+1}\left(\left(\frac{C_j}{A\cdot\varepsilon_s}-\Delta x\right)^{m+1} - x_{low}{}^{m+1}\right)\right] \qquad (5.3)$$

B. Influence of Process Deviations on the Linearity of the NTSVS

B.1 The influence from process deviation of the power law exponent (m)

Based on the Equation (5.1), we can analyze the influence of a deviation of the power coefficient from m=-2 case using the ADS Harmonic Balance simulator. Fig. 7 shows the simulation results of IM3+IM5 in dBc (ADS does not separate the IM3 and IM5 contributions, but one may distinguish them by the slope) versus the peak magnitude of the input RF signal (V_{RF_peak}). In Fig. 7, the slope of the line with m=-2 is -80dBc/decade as predicted by Equation (4.2). The slope of the lines with m=-1.8 and m=-1.9 is roughly -40dBc/decade when is V_{RF_peak} small, which indicates that IM3 is dominant factor for nonlinearity there; with the increase of V_{RF_peak}, the slope becomes larger and finally the slope is similar as that of the line with m=-2. One may find that the lines with m=-2.1 and -2.2 are obviously different from the others. It can be explained like this: when V_{RF_peak} small, IM3 constrains the linearity; when V_{RF_peak} becomes larger, cancellation between IM3 and contributions IM5 occurs since IM5 increases with V_{RF_peak} by a power of 4 and it has an opposite sign. Consequently, when V_{RF_peak} continues to increase, IM5 dominates the nonlinearity resulting in a similar slope as the line for the m=-2. The IM3 and IM5 cancellation phenomenon doesn't happen to the line with m=-1.9 and -1.8, because IM3 and IM5 have the same sign all the time for these two cases.



(a) Vmax=5V, Tuning range=6 and control voltage=2.5V **(b) Vmax=20V, Tuning range=6 and control voltage=10V**

Fig. 7. The simulated IM3+IM5 in dBc versus the peak magnitude of the input RF signal when m is unequal to -2

Before analyzing the linearity, let's consider the relationship between maximum allowable RF input signal and the center tap control voltage. As shown in Fig. 8, the center tap DC control voltage is V_{cont} and the peak amplitude RF input voltage is V_{RF_peak} which means the RF voltage assigned to each varactor, V_{diode}, is half of
5 V_{RF_peak}. As we mentioned before, there exists a maximum control voltage, V_{max} which yields full depletion of the varactor . The corresponding C-V curve is also shown in Fig.6. If V_{cont} is smaller than the $V_{max}/2$, the input RF signal is limited by the forward bias condition and one may find the peak amplitude of the maximum allowable RF signal is the double of V_{cont}. Similarly, as V_{cont} larger than $V_{max}/2$, the input RF signal is
10 limited by the clipping condition and the peak amplitude of the maximum allowable RF signal is the double of V_{max}-V_{cont}. In the extreme case that V_{cont} equals to $V_{max}/2$, the peak amplitude of the maximum allowable RF signal can reach V_{max}.

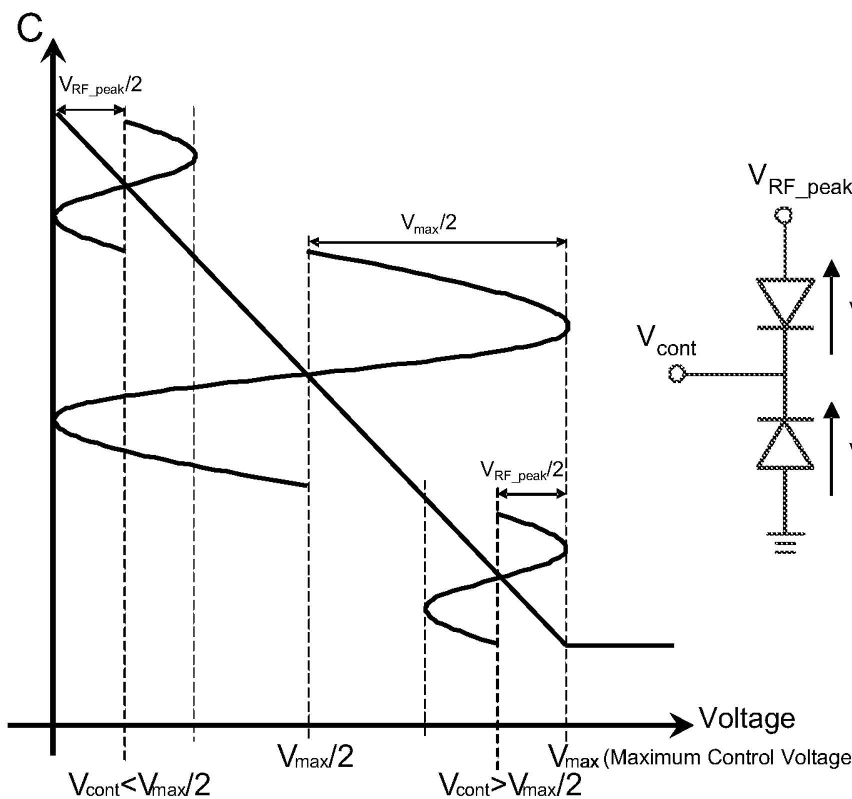
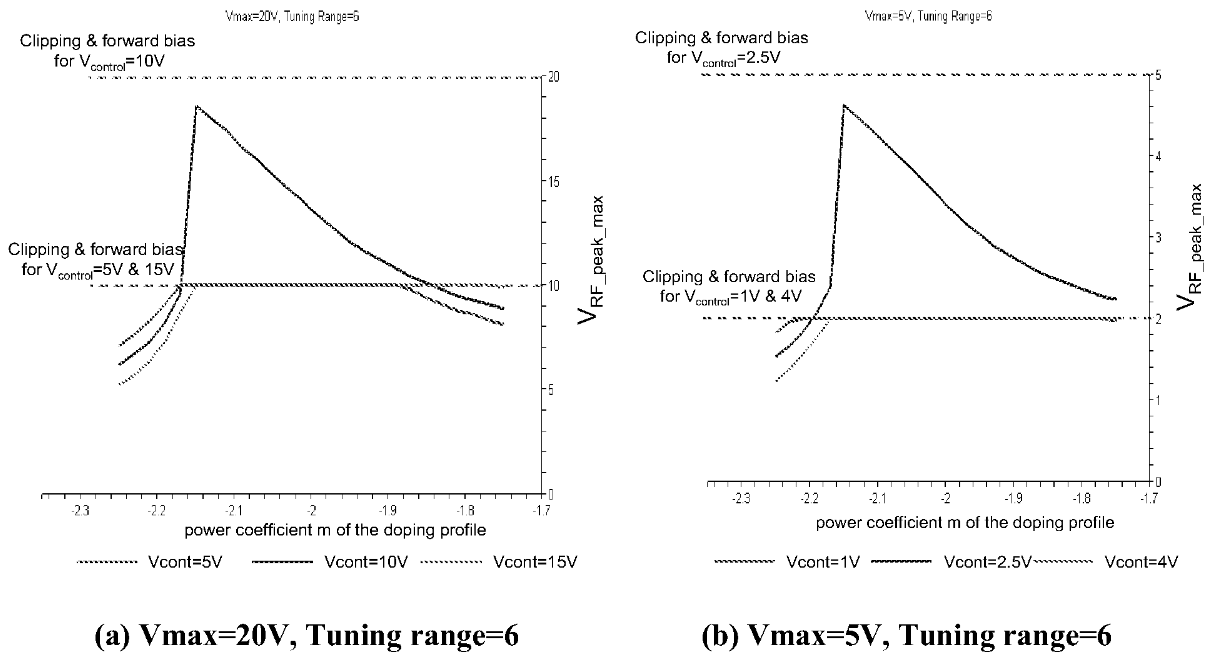


Fig. 8. The relationship between maximum allowable RF input signal and the DC center tap control voltage

We may specify our linearity requirement as -60dBc (which is sufficient for most applications) and check the acceptable range of m and V_{RF_peak}. Fig. 9 plots the maximum V_{RF_peak} for a linearity of -60 dBc versus m, where for a given m and DC control voltage, any voltage below $V_{RF_peak_max}$ (as illustrated in Fig. 7) should result in
5 an IM3 component smaller than -60dBc. The maximum allowable peak magnitudes of the RF input signal for different DC center tap control voltages are also included in Fig.9, where one may find when the DC control voltage is small or close to V_{max}, the $V_{RF_peak_max}$ is normally limited by the forward bias or clipping condition. For the situation where the DC control voltage is equal to half V_{max} the linearity becomes better
10 and better when m approaches -2.15, due to the IM3 and IM5 cancellation which occurs in the interval -2.15<m<-2, while instead, the existence of IM3 with the same sign as IM5 will degrade the linearity for m>-2. The abrupt change at m=-2.15 is due to the hump in IM3 which exceeds the -60dBc limit (Fig. 7). In summary, we can conclude that when m is in the range of -1.85 and -2.15, a reasonably high linearity can
15 be achieved with the best results when m is in the interval -2.15<m<-2.



(a) Vmax=20V, Tuning range=6 **(b) Vmax=5V, Tuning range=6**

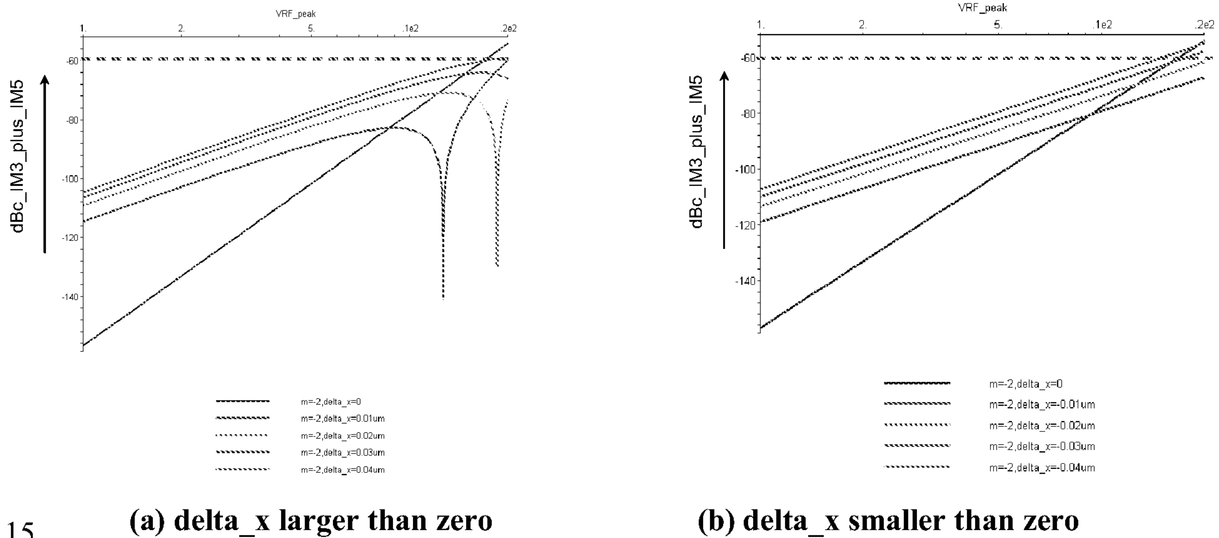
Fig 9. The maximum V_{RF_peak} for the linearity of -60 dBc versus m

30

B.2 The influence from the process deviation of "spacer" layer thickness (x_{low})

Based on the Equation (5.2), we can analyze the influence of the "spacer" layer thickness deviation on the linearity with the aid of ADS Harmonic Balance simulator and MAPLE software. Fig. 10 shows the calculated results of IM3+IM5 in dBc versus

the peak magnitude of the input RF signal (V_{RF_peak}) by MAPLE. Fig. 10 demonstrates that when the "spacer" layer thickness is larger than x_{low} (delta_x>0), IM3 and IM5 cancellation takes place; when the "spacer" layer thickness is smaller than x_{low} (delta_x<0), no cancellation occurs and IM3 dominates the nonlinearity.



15 **(a) delta_x larger than zero** **(b) delta_x smaller than zero**

Fig. 10. The calculated IM3+IM5 in dBc versus the peak magnitude of the input RF signal when "spacer" layer thickness unequal to x_{low} (Vmax=20V, Tuning range=6 and control voltage=10V)

Table2 listed the acceptable range of Δx for different control voltages, where the linearity requirement of IM3 component is still specified as -60dBc. For the case of

20 V_{max}=20V and Tuning range=6 (x_{low} is $0.2\mu m$ and the original depletion thickness is $0.336\mu m$ at zero bias), the acceptable range of Δx is from $-0.04\mu m$ to $0.03\mu m$, while for the case of V_{max}=5V and Tuning range=6 ($x_{low} = 0.03\mu m$), this range is from $-0.006\mu m$ to $0.006\mu m$ instead.

Control Voltage	Acceptable range of Δx
V_{cont}=5V	$-0.04\mu m \rightarrow 0.136\mu m$
V_{cont}=10V	$-0.04\mu m \rightarrow 0.03\mu m$
V_{cont}=15V	$-0.17\mu m \rightarrow 0.136\mu m$

(a) Vmax=20V, Tuning range=6

Control Voltage	Acceptable range of Δx
V_{cont}=1V	$-0.006\mu m \rightarrow 0.306\mu m$
V_{cont}=2.5V	$-0.006\mu m \rightarrow 0.006\mu m$
V_{cont}=4V	$-0.03\mu m \rightarrow 0.306\mu m$

5 **(b) Vmax=5V, Tuning range=6**

Table 2. The acceptable range of Δx for different control voltages

Consequently, it can be concluded that a deviation of 20% related with the original thickness of the "spacer" layer is acceptable for a linearity requirement of -60dBc.

10

VI. Layout Optimization

The optimized values listed in Table 1 only take the intrinsic part into account. In the case that a dedicated silicon-on-glass varactor technology is applied, the influence of the layout on the Q-factor can be almost omitted because the intrinsic varactor can be directly contacted by thick metal on both sides and no buried layer or finger
15 structure is required. If this varactor is implemented in conventional silicon or GaAs technology, a buried layer under the intrinsic area must be used for the connecting device, which will mitigate the Q-factor a lot. The generally accepted solution to reduce the resistance of buried layer is to use an interdigital electrode structure. In such a situation, several factors lowering the achievable Q-factor, like the resistance of the
20 electrodes, buried layer and contact as shown in Fig. 11, should be taken into account. For this purpose, we optimize the layout of the electrodes based on the distributed model of the varactor with interdigital electrodes as shown in Fig. 12. The parameters of the interdigital electrodes and the intrinsic silicon can be achieved by ADS momentum simulator and MEDICI respectively, while the resistance of the contact and
25 the buried layer can be estimated by equations.

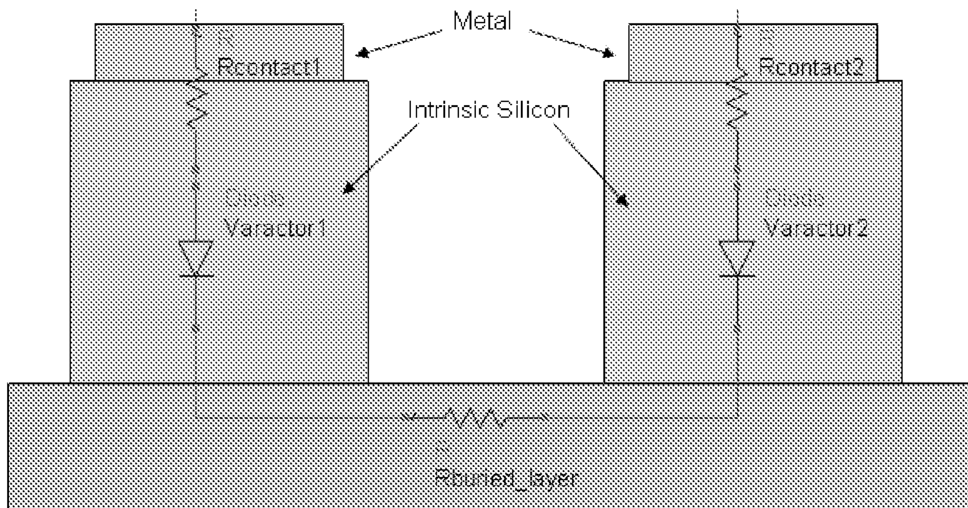


Fig. 11. Cross section of the interdigital electrode structure

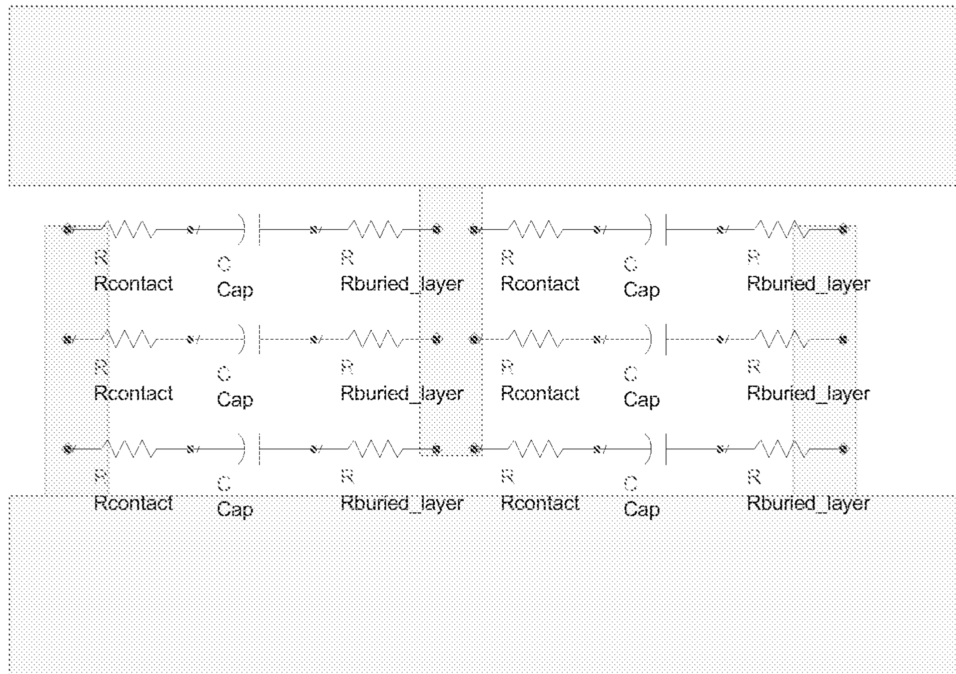


Fig. 12. The distributed model of the varactor with interdigital electrodes

In order to give an impression on achievable Q-factor including the layout issue, we listed the optimization results in Table 3 and Table 4 for the varactor stack with the original (V_{RF_peak}=0) tuning range of 6 and V_{max} of 5V. The Q-factor of the intrinsic part simulated by MEDICI is 848 at 2GHz and 56.6 at 30GHz for GaAs material.

Capacitor value (stack structure)	0.25pf	0.5pf	1pf	2.5pf	5pf	10pf	20pf
Q-factor	203	200	189	143	88	47	15.6

Table 3. Optimized Q-factor taking the layout parasitics into account at the frequency of 2GHz for GaAs material (The thickness of gold metal is 2µm and the sheet resistance of buried layer is 1ohm.)

Capacitor value (stack structure)	0.05pf	0.1pf	0.25pf	0.5pf	1pf	2.5pf	5pf
Q-factor	17.6	17.5	19.8	18.8	16.3	10.7	6.4

Table 4. Optimized Q-factor taking the layout parasitics into account at the frequency of 30GHz for GaAs material (The thickness of gold metal is 2µm and the sheet resistance of buried layer is 1ohm.)

Table 3 and Table 4 indicates, for the wireless communication applications, a 1pf GaAs varactor (stacked structure) with V_{max}=5V and the tuning range of 6 can be realized with a Q-factor of 190 at zero bias for 2GHz, while for the millimeter applications, a 0.5pf GaAs varactor (stacked structure) with V_{max}=5V and the tuning range of 6 can be realized with a Q-factor of 18.8 at zero bias for 30GHz.

For the case of silicon, the layout is optimized for the varactor stack with the original (V_{RF_peak}=0) tuning range of 4 and V_{max} of 4V. The Q-factor of the intrinsic part simulated by MEDICI is 15.5 at 30GHz. As listed in Table 5, a 0.5pf varactor (stacked structure) can be realized with a Q-factor of 10.3 at zero bias for 30GHz.

Capacitor value (stack structure)	0.25pf	0.5pf	1pf	2.5pf	5pf
Q-factor	10.4	10.3	9.5	7	4.4

Table 5. Optimized Q-factor taking the layout parasitics into account at the frequency of 30GHz for Silicon material (The sheet resistance of aluminum and buried layer is 0.0133ohm and 2ohm respectively.)

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[3] K. Buisman, L. C. N. de Vreede, L. E. Larson, M. Spirito, A. Akhnoukh, Y. Lin, X. Liu and L. K. Nanver, "Low-distortion, low-loss varactor-based adaptive matching networks, implemented in a silicon-on-glass technology," in Proc. 2005 Radio Frequency IC Symp., Long Beach, California, Jun. 2005.

[4] K. Buisman,, L. C.N. de Vreede,, Lawrence E. Larson,, M. Spirito, A. Akhnoukh, Y. Lin, X. Liu, and L. K. Nanver, High-Linearity Varactor Diode Circuits for RF Adaptivity, submitted for publication to the IEEE MTT.

Appendix A: Derivation of the doping profile for the exponential C(V) relation

In order to develop the analytical relationship between the doping profile as shown in Fig. 2 and the C(V) relation, we assume:

5 1. The N-type region has an abrupt boundary between low doped "spacer" region and N/x^2 region.
2. The donor doping concentration is the same as the electron concentration in the N-type region.
3. Due to the high doping level at the start of N/x^2 region, low doped "spacer" region
10 consumes the total built-in voltage, while the applied voltage is completely used to deplete the N/x^2 region.

The doping concentration of the varactor is defined as follows:

$$Doping_Concentration(x) = \begin{cases} N_1(x) = N(fill) \cdots\cdots\cdots\cdots (0 < x < x_{low}) \\ N_2(x) = \dfrac{N(x_{low})}{\left(\dfrac{x}{x_{low}}\right)^2} \cdots\cdots\cdots (x_{low} < x < x_{high}) \end{cases} \qquad (A.1)$$

15 The electric field is determined from Poisson's equation which, for a one-dimensional analysis, is

$$\frac{d^2\phi(x)}{dx^2} = \frac{-\rho(x)}{\varepsilon_s} = -\frac{dE(x)}{dx} \qquad (A.2)$$

where $\phi(x)$ is the electric potential, $E(x)$ is the electric field, $\rho(x)$ is the volume charge density, and ε_s is the permittivity of the semiconductor.

20 The electric field in the n-region is found by integrating Equation (A.2). We have that

$$E_2(x) = \frac{q}{\varepsilon_s}\int_{x_0}^{x} \frac{N(x_{low})\cdot x_{low}^{\ 2}}{x^2}dx = -\frac{q\cdot N(x_{low})\cdot x_{low}^{\ 2}}{\varepsilon_s}\left(\frac{1}{x} - \frac{1}{x_0}\right) \cdots\cdots (x_{low} \le x \le x_0) \quad (A.3)$$

$$E_1(x) = \frac{q\cdot N(fill)}{\varepsilon_s}(x-a) - \frac{q\cdot N(x_{low})\cdot x_{low}^{\ 2}}{\varepsilon_s}\left(\frac{1}{x_{low}} - \frac{1}{x_0}\right) \cdots\cdots (0 \le x \le x_{low}) \quad (A.4)$$

Due to the Schottky contact, the potential at x=0 can be defined as zero. Based on
25 Equation (A.3) and (A.4), the potential at x_0 can be determined,

$$\phi(x_0) = \int_0^{x_0} -E(x)dx$$

$$\phi(x_0) = \frac{q \cdot N(fill)}{2\varepsilon_s} \cdot x_{low}^2 + \frac{q \cdot N(x_{low}) \cdot x_{low}^2}{\varepsilon_s}(\ln x_0 - \ln x_{low}) \quad (A.5)$$

The magnitude of the potential at $x=x_0$ is equal to the sum of applied voltage and built-in voltage. Then from Equation (A.5), we have

$$\phi(x_0) = \frac{q \cdot N(fill)}{2\varepsilon_s} \cdot x_{low}^2 + \frac{q \cdot N(x_{low}) \cdot x_{low}^2}{\varepsilon_s}(\ln x_0 - \ln x_{low}) = V_{bi} + V_R \quad (A.6)$$

5 The first item in Equation (A.6) is the built-in voltage, and then we have

$$\frac{q \cdot N(x_{low}) \cdot x_{low}^2}{\varepsilon_s}(\ln x_0 - \ln x_{low}) = V_R \quad (A.7)$$

Differentiation to V_R can be taken in both sides of Equation (A.7), we obtain

$$1 = \frac{q \cdot N(x_{low}) \cdot x_{low}^2}{\varepsilon_s} \cdot \frac{1}{x_0} \cdot \frac{dx_0}{dV_R} \longrightarrow \frac{dx_0}{dV_R} = \left(\frac{q \cdot N(x_{low}) \cdot x_{low}^2}{\varepsilon_s} \cdot \frac{1}{x_0} \right)^{-1} \quad (A.8)$$

The junction capacitance is defined as

10 $$C_j(V_R) = \frac{dQ}{dV_R} = qN(x)\frac{dx}{dV_R} = A \cdot q \cdot \frac{N(x_{low})}{\left(\frac{x_0}{x_{low}}\right)^2} \cdot \left(\frac{q \cdot N(x_{low}) \cdot x_{low}^2}{\varepsilon_s} \cdot \frac{1}{x_0} \right)^{-1} = A\frac{\varepsilon_s}{x_0} \quad (A.9)$$

$$\ln(C_j(V_R)) = \ln(A \cdot \varepsilon_s) - \ln(x_0) \quad (A.10)$$

Then, substituting Equation (A.7) into Equation (A.10), we have

$$\ln(C_j(V_R)) = \ln\left[\frac{A \cdot \varepsilon_s}{x_{low}} \cdot \exp\left(-\frac{\varepsilon_s}{q \cdot N(x_{low}) \cdot x_{low}^2} \cdot V_R \right) \right] \quad (A.11)$$

Hereby, we obtain

15 $$C_j(V_R) = \frac{A \cdot \varepsilon_s}{x_{low}} \cdot \exp\left(-\frac{\varepsilon_s}{q \cdot N(x_{low}) \cdot x_{low}^2} \cdot V_R \right) \quad (A.12)$$

where the constant ($\frac{A \cdot \varepsilon_s}{x_{low}}$) is capacitor value of the depletion region.

The derivation of C(V) relation above assumes that the low doped “spacer” region consumes the total built-in voltage, while the applied voltage is completely used to deplete the N/x^2 region. However, even if the start of N/x^2 region is highly doped
20 (normally from $2e17cm^{-3}$ to $5e17cm^{-3}$), it still consumes part of built-in voltage. Now, let’s consider the more general situation. We assume that the depletion width at zero applied voltage is x'_{low}, which is larger than x_{low}.

In this situation, Equation (A.6) is still valid since there is no change of the doping profile. The only difference is built-in voltage doesn't equal to the first item of Equation (A.6) any more. In stead, it should be written as

$$\phi(x'_{low}) = \frac{q \cdot N(fill)}{2\varepsilon_s} \cdot x_{low}^{\ 2} + \frac{q \cdot N(x_{low}) \cdot x_{low}^{\ 2}}{\varepsilon_s}\left(\ln x'_{low} - \ln x_{low}\right) = V_{bi} \quad \text{(A.13)}$$

5 As done previously, we substitute Equation (A.13) into Equation (A.6), we have

$$\frac{q \cdot N(x_{low}) \cdot x_{low}^{\ 2}}{\varepsilon_s}\left(\ln x_0 - \ln x'_{low}\right) = V_R \quad \text{(A.14)}$$

where x'_{low} can be obtained by Equation (A.13) and V_{bi} is given by

$$V_{bi} = \frac{kT}{q} \ln\left(\frac{N_a \cdot \frac{N_{d1} \cdot a^2}{c^2}}{n_i^2} \right) \quad \text{(A.15)}$$

Similarly, the C-V relation can be written as

10 $$C_j(V_R) = \frac{A \cdot \varepsilon_s}{x'_{low}} \cdot \exp\left(-\frac{\varepsilon_s}{q \cdot N(x_{low}) \cdot x_{low}^{\ 2}} \cdot V_R \right) \quad \text{(A.16)}$$

where the constant $(\frac{A \cdot \varepsilon_s}{x'_{low}})$ is capacitor value of the depletion region.

To check the difference between Equation (A.12) and (A.16), we give an example as follows. $N(fill) = 1 \times 10^{16} cm^{-3}$, $N(x_{low}) = 4 \times 10^{17} cm^{-3}$, $x_{low} = 0.1 \times 10^{-4} cm$, $A = (10^{-4} \times 10^{-4}) cm^2$. The C-V curves for Equation (A.12) (marked by red) and
15 Equation (A.16) (marked by blue) are shown in Fig. A. The calculated original depletion width for this case is $0.115\,\mu m$, which can be used to explain the deviation between the red line and the blue line in Fig. A.

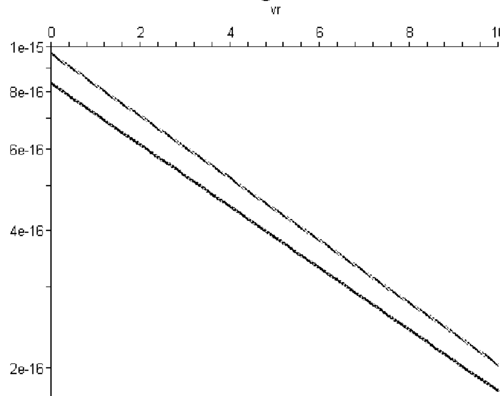


Fig. A. C-V curves for Equation (A.12) and (A.16)

Appendix B: Derivation of C(V) relation for the process deviation on the power

Here, we keep the three assumption mentioned above in Appendix A. Now the doping concentration of the varactor should be modified as

5

$$Doping_Concentration(x) = \begin{cases} N_1(x) = N(fill) \cdots\cdots\cdots\cdots (0 < x < x_{low}) \\ N_2(x) = N(x_{low}) \cdot \left(\dfrac{x}{x_{low}} \right)^m \ldots (x_{low} < x < x_{high}) \end{cases} \quad \text{(B.1)}$$

Note that only the power of the doping profile is changed here.

Making use of the Poisson equation, the electric field in the N region can be written as

10

$$E_2(x) = \frac{q}{\varepsilon_s} \int_{x_0}^{x} N(x_{low}) \cdot \left(\frac{x}{x_{low}} \right)^m dx = \frac{q \cdot N(x_{low}) \cdot x_{low}^{-m}}{\varepsilon_s \cdot (m+1)} \left(x^{m+1} - x_0^{m+1} \right) \cdots (x_{low} \le x \le x_0) \quad \text{(B.2)}$$

$$E_1(x) = \frac{q \cdot N(fill)}{\varepsilon_s} (x - a) + \frac{q \cdot N(x_{low}) \cdot x_{low}^{-m}}{\varepsilon_s \cdot (m+1)} \left(x_{low}^{m+1} - x_0^{m+1} \right) \cdots (0 \le x \le x_{low}) \quad \text{(B.3)}$$

Still defining the potential at x=0 as zero, based on Equation (B.2) and (B.3), the potential at x_0 is given by

$$\phi(x_0) = \frac{q \cdot N(fill)}{2\varepsilon_s} \cdot x_{low}^2 + \frac{q \cdot N(x_{low}) \cdot x_{low}^{-m}}{\varepsilon_s \cdot (m+2)} \left(x_0^{m+2} - x_{low}^{m+2} \right) = V_{bi} + V_R \quad \text{(B.4)}$$

15 Similarly, the first item above cancelled with the build in voltage V_{bi}. Consequently, the C(V) relation can be written as

$$C_j(V_R) = A \frac{\varepsilon_s}{x_0(V_R)} = \frac{A \cdot \varepsilon_s}{\left[\dfrac{\varepsilon_s \cdot (m+2) \cdot V_R \cdot x_{low}^m}{N(x_{low})} + x_{low}^{m+2} \right]^{\frac{1}{m+2}}} \quad \text{(B.5)}$$

Note that the result above only valid when m isn't equal to -2.

20

Appendix C: Derivation of C(V) relation for the process deviation on the origin

Here, we keep the three assumption mentioned above in Appendix A. Now the doping concentration of the varactor should be modified as

5

$$Doping_Concentration(x) = \begin{cases} N_1(x) = N(fill) \cdots\cdots\cdots\cdots (0 < x < x_{low} + \Delta x) \\ N_2(x) = \dfrac{N(x_{low})}{\left(\dfrac{x-\Delta x}{x_{low}}\right)^2} \ldots (x_{low} + \Delta x < x < x_{high}) \end{cases} \quad (C.1)$$

Making use of the Poisson equation, the electric field in the N region can be written as

$$E_2(x) = -\frac{q \cdot N(x_{low}) \cdot x_{low}^2}{\varepsilon_s}\left(\frac{1}{x-\Delta x} - \frac{1}{x_0 - \Delta x}\right) \cdots\cdots (x_{low} + \Delta x \le x \le x_0) \quad (C.2)$$

10 $$E_1(x) = \frac{q \cdot N(fill)}{\varepsilon_s}(x - a - \Delta x) - \frac{q \cdot N(x_{low}) \cdot x_{low}^2}{\varepsilon_s}\left(\frac{1}{x_{low}} - \frac{1}{x_0 - \Delta x}\right) \cdots (0 \le x \le x_{low}) \quad (C.3)$$

Defining the potential at x=0 as zero and canceling the build in voltage, based on Equation (C.2) and (C.3), $x_0(V_R)$ relation can be written as

$$V_R = \frac{q \cdot N(x_{low}) \cdot x_{low}^2}{\varepsilon_s}\left(\ln\frac{x_0 - \Delta x}{x_{low}} + \frac{\Delta x}{x_{low}} - \frac{\Delta x}{x_0 - \Delta x}\right) \quad (C.4)$$

Consequently, the C(V) relation is given by

15 $$V_R = \frac{q \cdot N(x_{low}) \cdot x_{low}^2}{\varepsilon_s}\left[\ln\left(\frac{\dfrac{C_j}{A \cdot \varepsilon_s} - \Delta x}{x_{low}}\right) + \frac{\Delta x}{x_{low}} - \frac{\Delta x}{\dfrac{C_j}{A \cdot \varepsilon_s} - \Delta x}\right] \quad (C.5)$$

Note that the C(V) relation is only possible to be written in an implicit form.

Appendix D: Derivation of C(V) relation for the process deviation on both power and the origin

Here, we keep the three assumption mentioned above in Appendix A. Now the
5 doping concentration of the varactor should be modified as

$$Doping_Concentration(x) = \begin{cases} N_1(x) = N(fill) \cdots\cdots\cdots\cdots (-\Delta x < x < x_{low}) \\ N_2(x) = N(x_{low}) \cdot \left(\frac{x}{x_{low}} \right)^m \ldots (x_{low} < x < x_{high}) \end{cases} \quad (D.1)$$

Note that the expression above indicates that the origin of the N-region is offset by Δx.

10 Making use of the Poisson equation, the electric field in the N region can be written as

$$E_2(x) = \frac{q \cdot N(x_{low}) \cdot x_{low}^{-m}}{\varepsilon_s \cdot (m+1)} \left(x^{m+1} - x_0^{m+1} \right) \cdots (x_{low} \le x \le x_0) \quad (D.2)$$

$$E_1(x) = \frac{q \cdot N(fill)}{\varepsilon_s} (x - a) + \frac{q \cdot N(x_{low}) \cdot x_{low}^{-m}}{\varepsilon_s} \left(x_{low}^{m+1} - x_0^{m+1} \right) \cdots (-\Delta x \le x \le x_{low}) \quad (D.3)$$

Defining the potential at x=0 as zero and canceling the build in voltage, based on
15 Equation (D.2) and (D.3), $x_0(V_R)$ relation can be written as

$$V_R = \frac{q \cdot N(x_{low}) \cdot x_{low}^{-m}}{\varepsilon_s \cdot (m+2)} \left(x_0^{m+2} - x_{low}^{m+2} \right) + \frac{q \cdot N(x_{low}) \cdot x_{low}^{-m}}{\varepsilon_s \cdot (m+1)} \cdot \Delta x \cdot \left(x_0^{m+1} - x_{low}^{m+1} \right) \quad (D.4)$$

Consequently, the C(V) relation is given by

$$V_R = \frac{q \cdot N(x_{low}) \cdot x_{low}^{-m}}{\varepsilon_s} \cdot \left[\frac{\left(\frac{C_j}{A \cdot \varepsilon_s} - \Delta x \right)^{m+2} - x_{low}^{m+2}}{m+2} + \frac{\Delta x}{m+1} \left(\left(\frac{C_j}{A \cdot \varepsilon_s} - \Delta x \right)^{m+1} - x_{low}^{m+1} \right) \right] \quad (D.5)$$

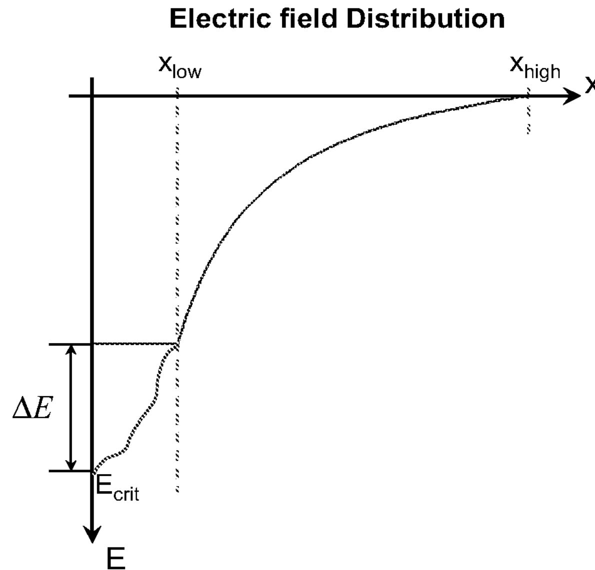
Note that the C(V) relation can only be written in an implicit form.

20

Appendix E: Increase of Electric field due to the doping of the spacer layer

Here we give the restrictions on the doping level of the spacer layer in order not to seriously degrade the optimum in tuning range, breakdown voltage and quality factor.

5



10

15

Figure E. Typical electric field distribution of the graded varactor, the blue line represents the situation that the spacer layer (up to xlow is not doped). The purple line represents the situation when doping in the spacer layer is present (increasing the electric field).

20

The restriction on the doping content of the spacer layer can be developed by the following derivation.

Assume that the spacer layer is arbitrarily doped and the doping concentration is defined as $N_{fill}(x) \cdots\cdots\cdots\cdots (0 < x < x_{low})$

25 The electric field due to the spacer layer can be expressed as

$$\Delta E = \frac{q}{\varepsilon_s} \int_0^{x_{low}} N_{fill}(x) dx$$

The sheet resistance of the spacer layer can be written as

$$R_{sheet_spacer_layer} = \frac{1}{q \cdot \mu_n \cdot \int_0^{x_{low}} N_{fill}(x) dx} = \frac{1}{\mu_n \cdot \varepsilon_s} \cdot \frac{1}{\Delta E}$$

Consequently, if we assume that the increase in electric field must be limited to:

30 $\Delta E = \frac{1}{2} E_{crit} = 3 \times 10^5 V/cm$, we can derive that the sheet resistance of the spacer layer

equals $2385\Omega/\square$. As result practical implementations of the Q-optimized varactor diode should exhibit a sheet resistance for the spacer layer higher than this number.

CLAIMS

1. Varactor element having a junction region, in which the depletion capacitance of the varactor element varies when a reverse bias voltage is applied to the varactor element, characterized in that the varactor element has an exponential depletion capacitance-voltage relation,
in which the junction region comprises a single sided junction, and the varactor element is provided with a doping profile substantially defined by $N(x) = N/x^m$, $N(x)$ being the varactor element's doping concentration in one dimension as a function of x, x being a distance from the junction, N being a predefined doping concentration constant, and m being an exponential factor, and
in which the junction region comprises a filling layer in an interval of distances lower than x_{low} with a doping concentration N_{fill} lower than the doping concentration at distance x_{low} ($N(x_{low})$).

2. Varactor element according to claim 1, in which the exponential factor has a value in the range $1.7 < m < 2.3$.

3. Varactor element according to claim 1 or 2, in which the doping profile is substantially equal to N(x) at least in the interval $x_{low}\ldots x_{high}$, in which x_{low} is nearer to the junction than x_{high}.

4. Varactor element according to any one of claims 1-3, in which the junction region is a two sided or double sided junction.

5. Varactor stack circuit arrangement, comprising two varactor elements according to any one of the claims 1-4, each having two terminals, in which the two varactor elements are connected in an anti-series configuration, such that a control node is provided by two interconnected terminals and two RF connection nodes by the other terminals.

6. Varactor stack circuit arrangement according to claim 5, in which the two varactor elements are connected by a low impedance material.

7. Varactor stack circuit arrangement according to claim 6, in which the low impedance material comprises a back side metallization.

8. Varactor stack circuit arrangement according to claim 6 or 7, in which the varactor circuit arrangement further comprises a center tap impedance connected to the control node, the center tap impedance providing a low impedance path for base band frequency components between the control node and each of the two RF connection nodes.

9. Varactor stack circuit arrangement according to claim 8, in which the low impedance path has an impedance lower than the varactor element capacitances for the base-band frequency components.

10. Varactor stack circuit arrangement according to claim 8 or 9, in which the base band frequency is the separation frequency of a signal having a narrow tone spacing or the modulation frequency of a modulated (RF) signal.

11. Four port electronic arrangement, comprising two series capacitors and two cross connected capacitors, in which one of the two series capacitors is connected between a first input port and a first output port, the other of the two series capacitors is connected between a second input port and a second output port, one of the two cross connected capacitors is connected between the first input port and the second output port, and the other of the two cross connected capacitors is connected between the second input port and the first output port, in which at least the two series capacitors or the two cross connected capacitors comprise a varactor stack arrangement according to any one of the claims 6 through 10.

12. Four port electronic arrangement according to claim 11, further comprising a first shunt inductor connected between the first and second input port, and a second shunt inductor connected between the first and second output port.

13. Direct polar modulator, comprising a four port electronic arrangement according to claim 11 or 12, in which the first and second output ports are further connected to a

series of phase shift sections, each phase shift section comprising a varactor stack arrangement according to any one of the claims 6 through 10.

14. Use of a varactor stack arrangement according to any one of the claims 6 through 10 in adaptive or dynamic matching networks.

15. Use of a varactor stack arrangement according to any one of the claims 6 through 10 in adaptive or tunable phase shifter devices.

16. Use of a varactor stack arrangement according to any one of the claims 6 through 10 in direct modulators arrangements.

17. Use of a varactor stack arrangement according to any one of the claims 6 through 10 as up converting mixer or modulator.

18. Use of a varactor stack arrangement according to any one of the claims 6 through 10 in RF switches.

19. Use of a varactor stack arrangement according to any one of the claims 6 through 10 in tunable filters or multiplexers.

20. Use of a varactor stack arrangement according to any one of the claims 6 through 10 in antenna array systems.

******

Fig 1

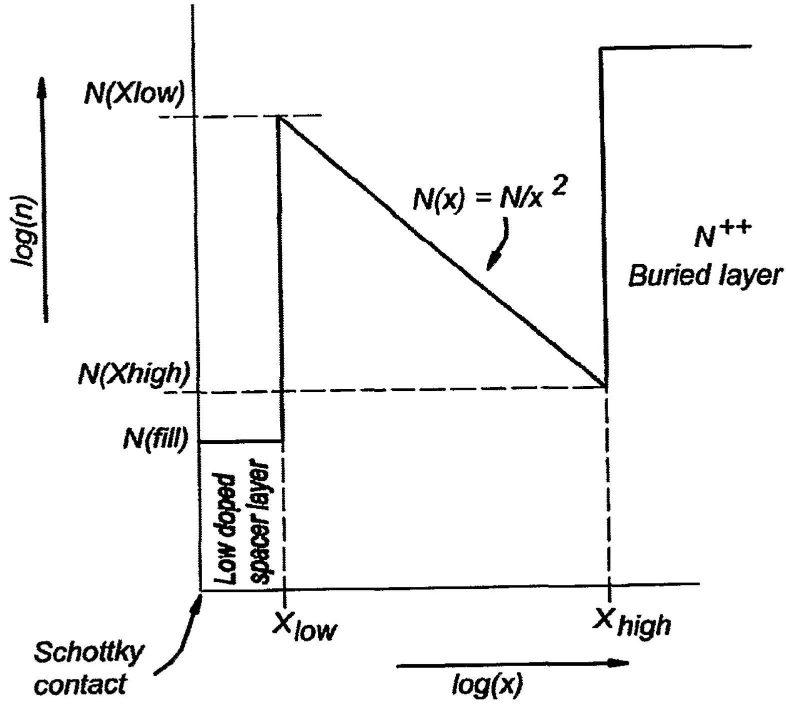


Fig 2a

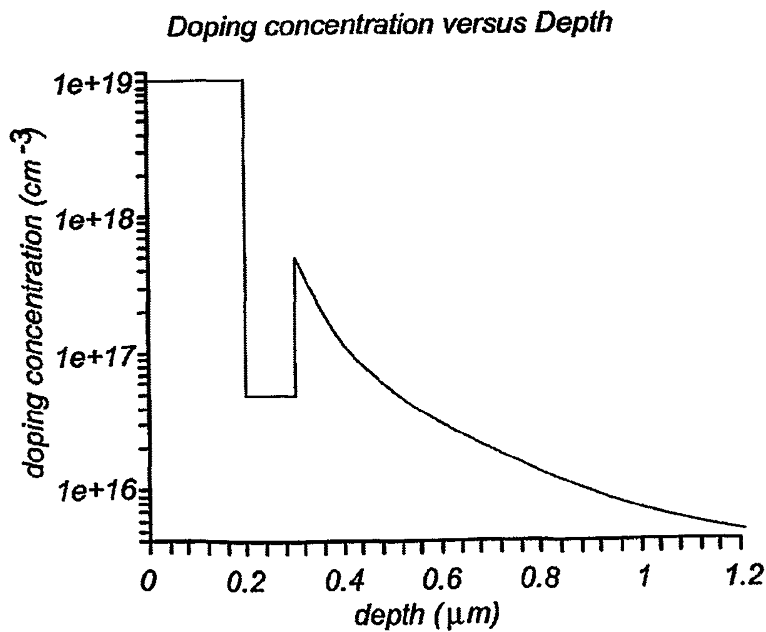


Fig 2b

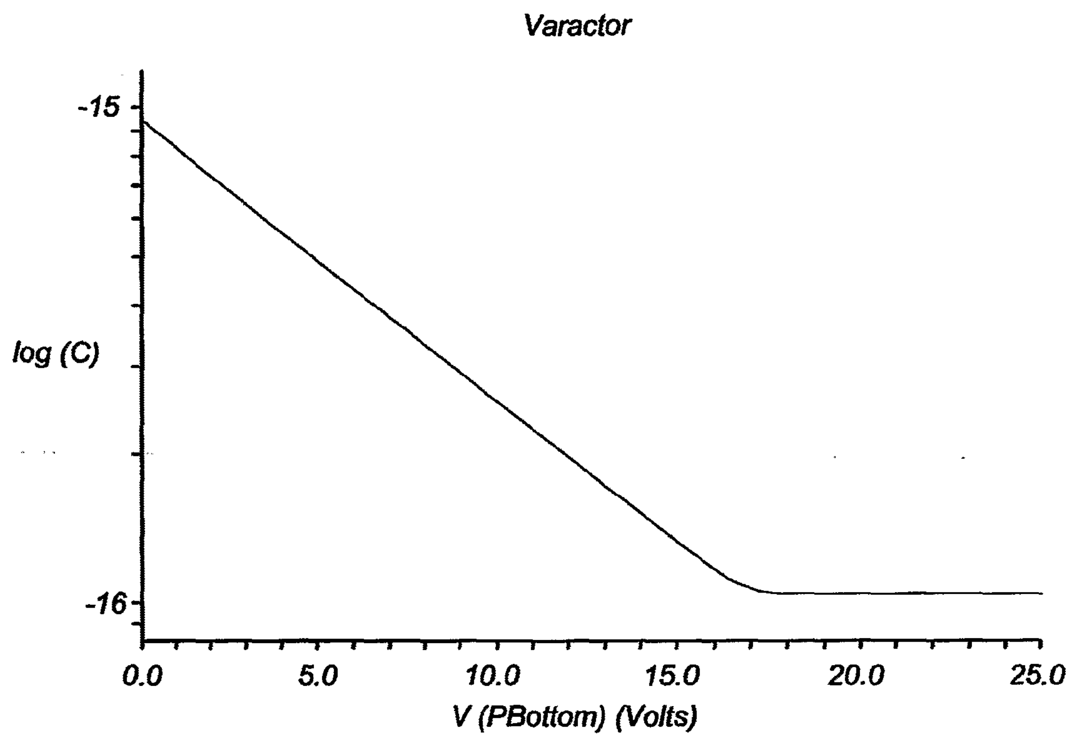


Fig 3a

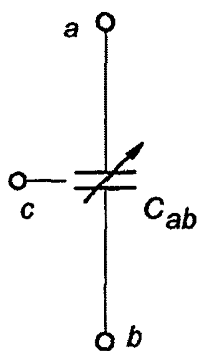


Fig 3b

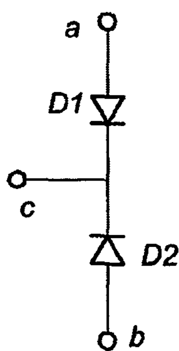


Fig 3c

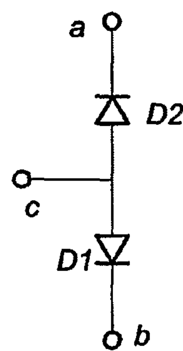
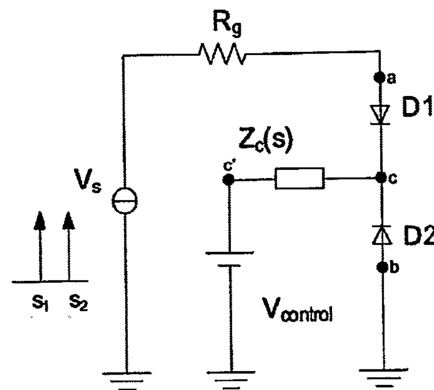


Fig 4



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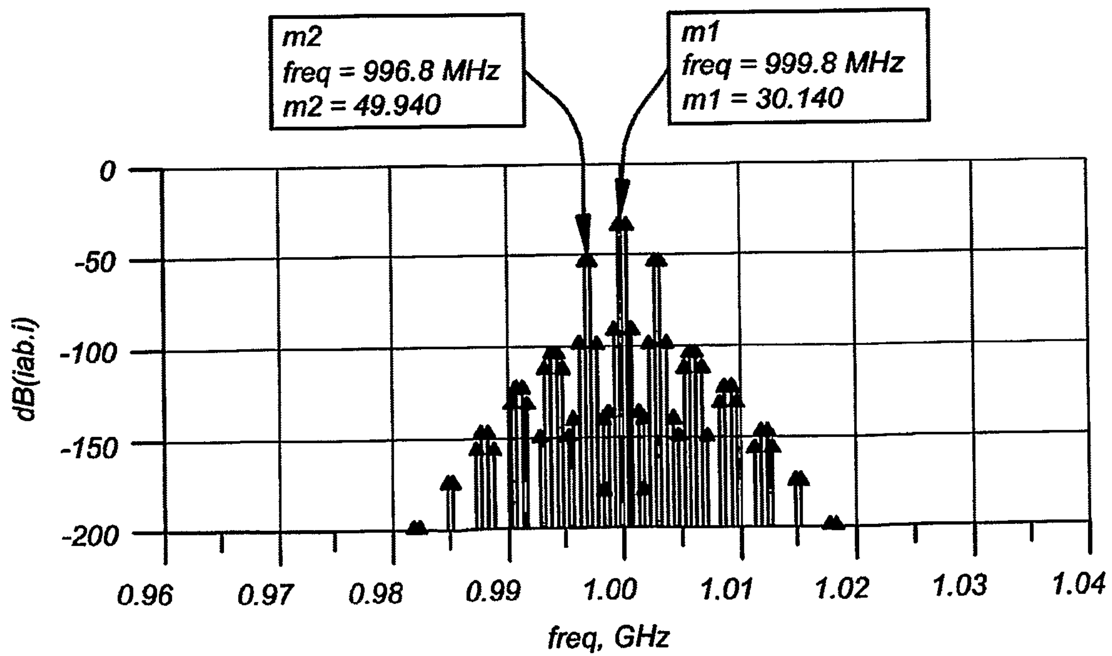


Fig 6

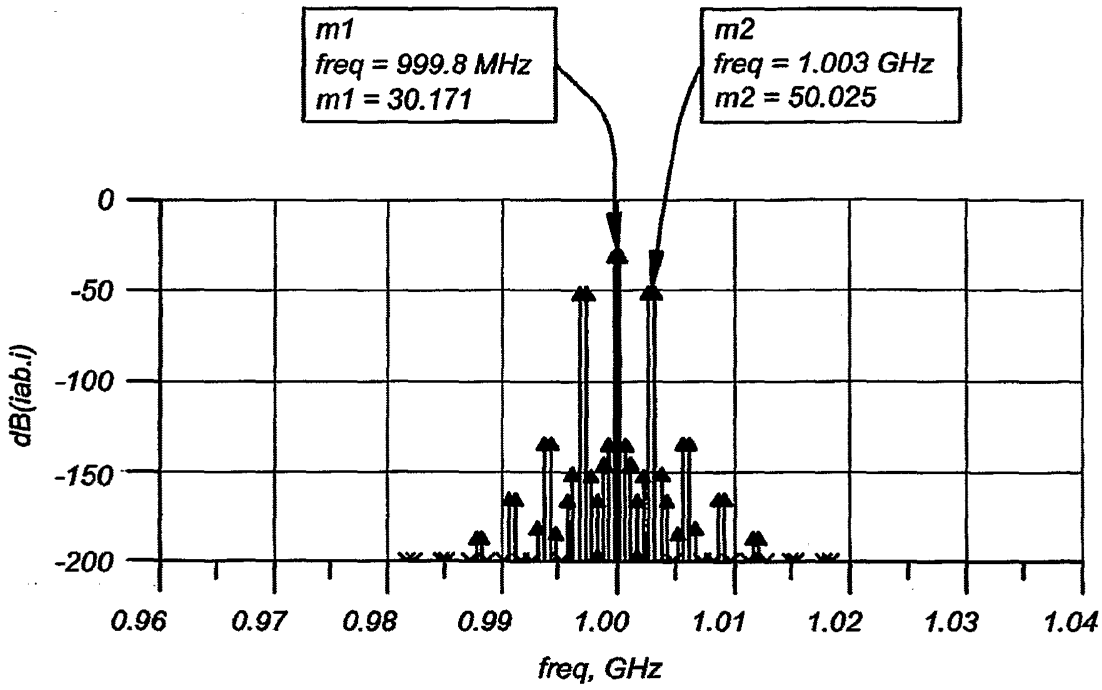


Fig 7

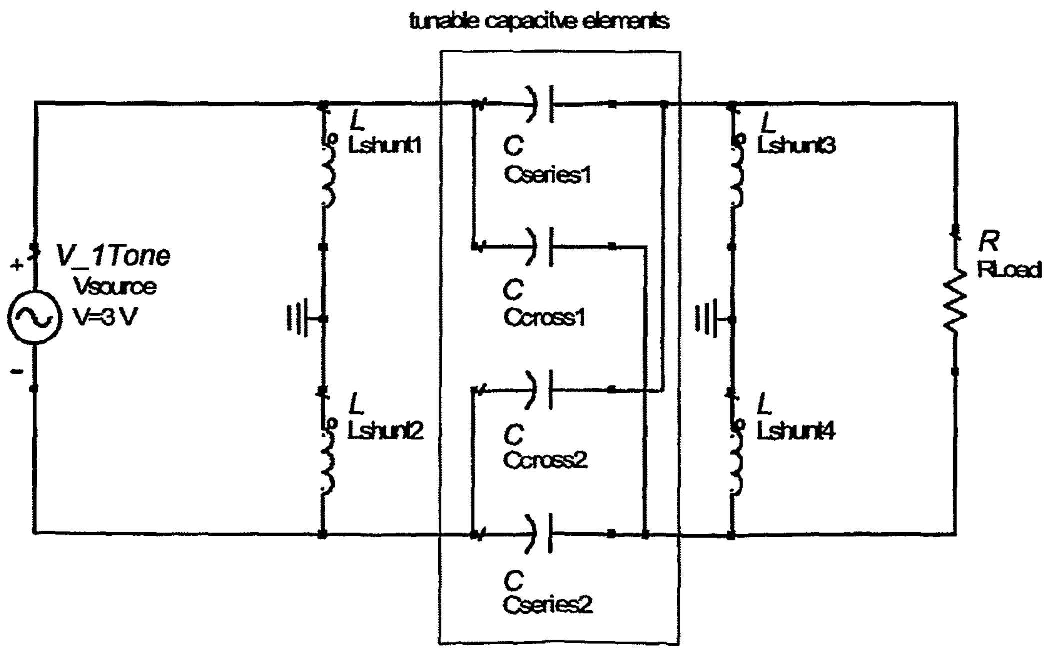


Fig 8

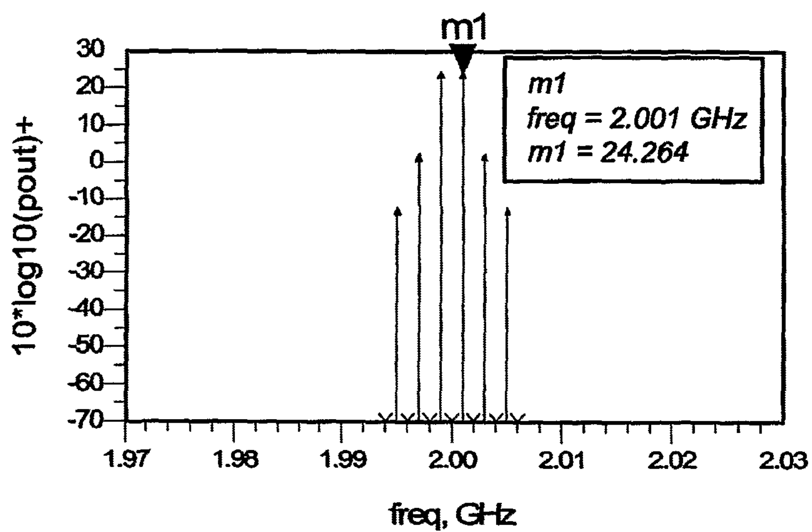
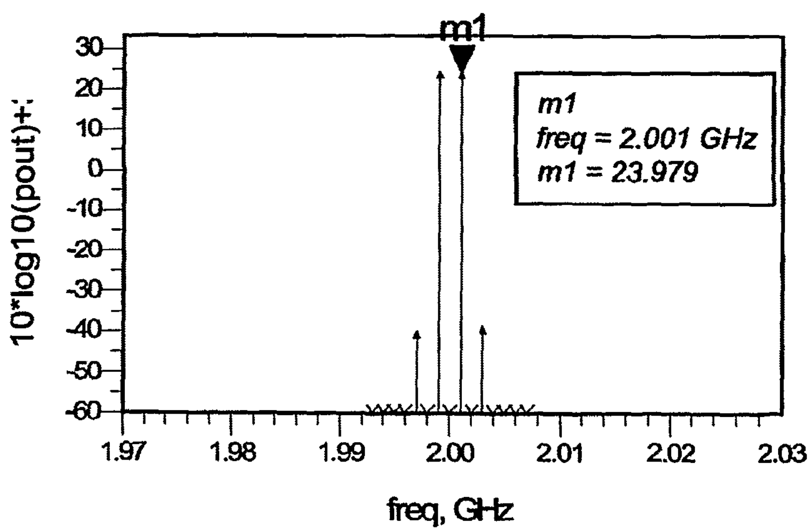


Fig 9



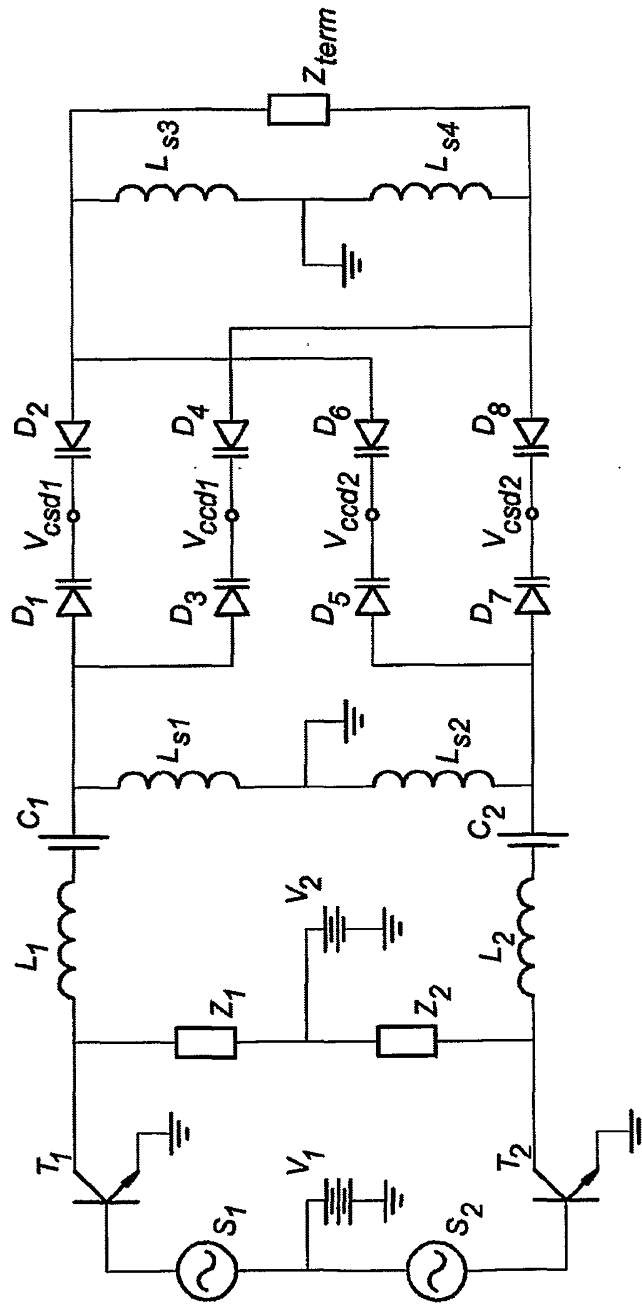


Fig 10

Fig 11a

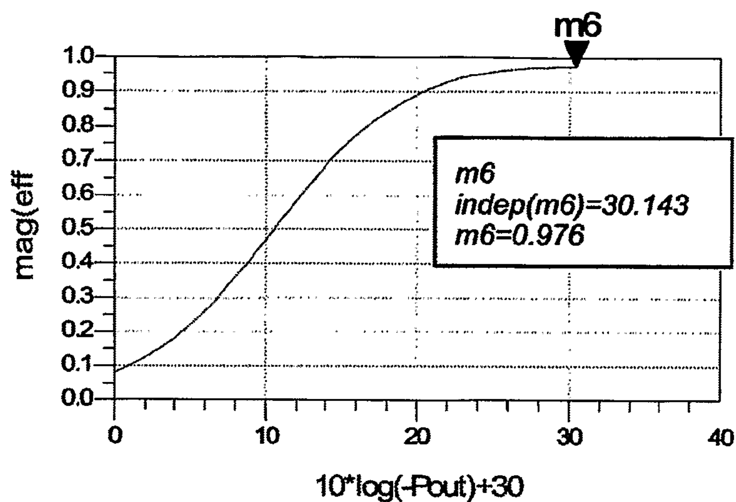


Fig 11b

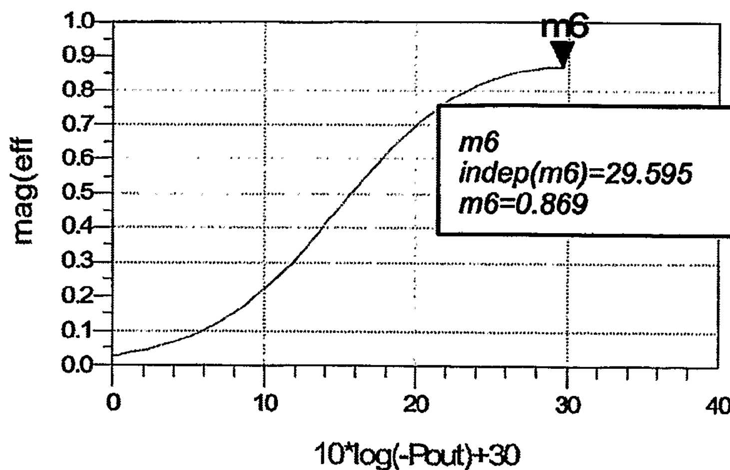


Fig 11c

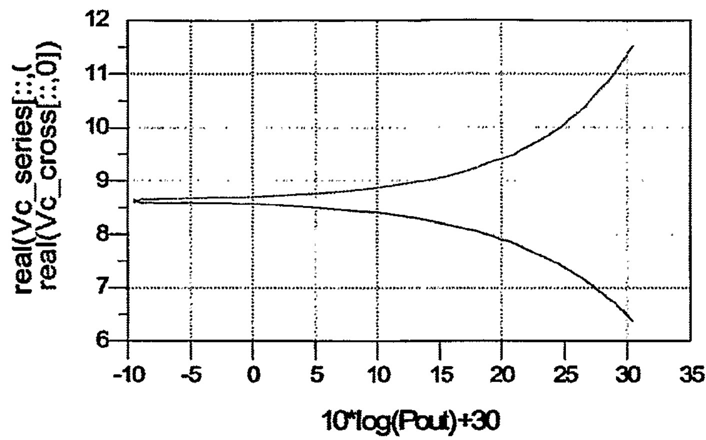
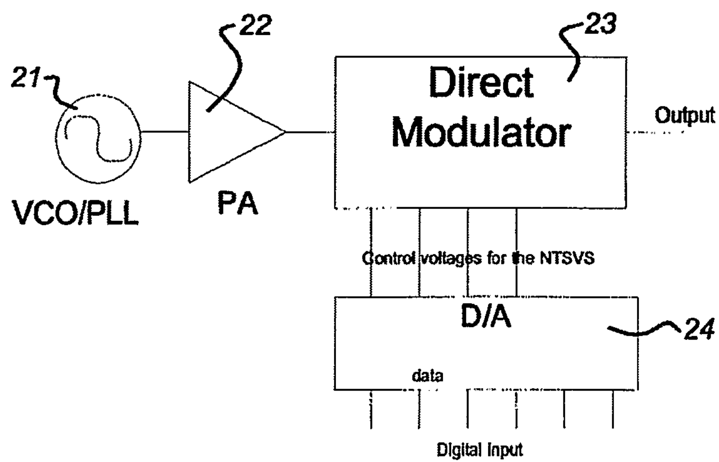


Fig 12



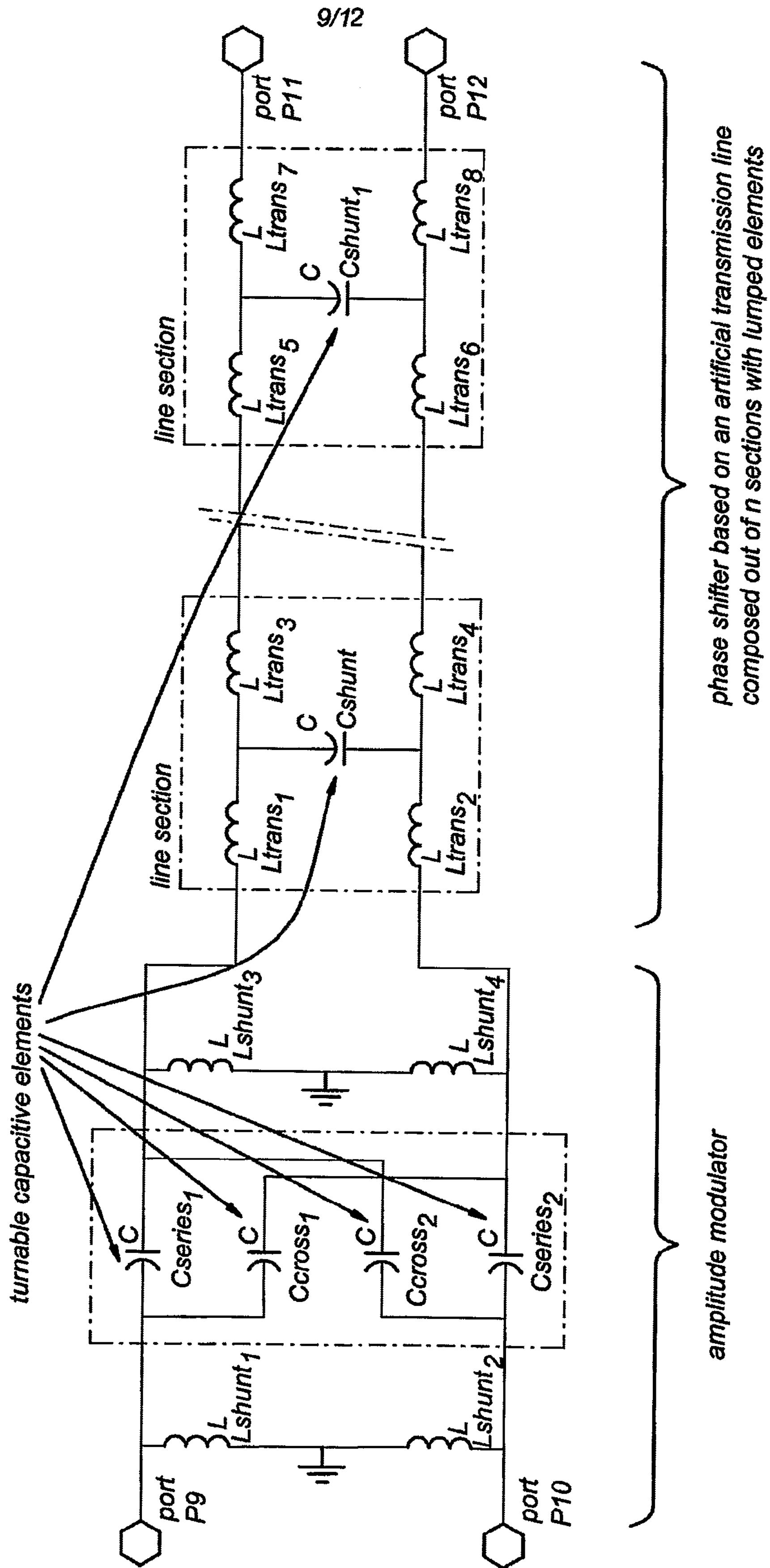


Fig 13
turnable capacitive elements
port P9
port P10
port P11
port P12
Lshunt1
Lshunt2
Lshunt3
Lshunt4
Cseries1
Cseries2
Ccross1
Ccross2
line section
line section
Ltrans1
Ltrans2
Ltrans3
Ltrans4
Ltrans5
Ltrans6
Ltrans7
Ltrans8
Cshunt
Cshunt1
amplitude modulator
phase shifter based on an artificial transmission line
composed out of n sections with lumped elements

Fig 14

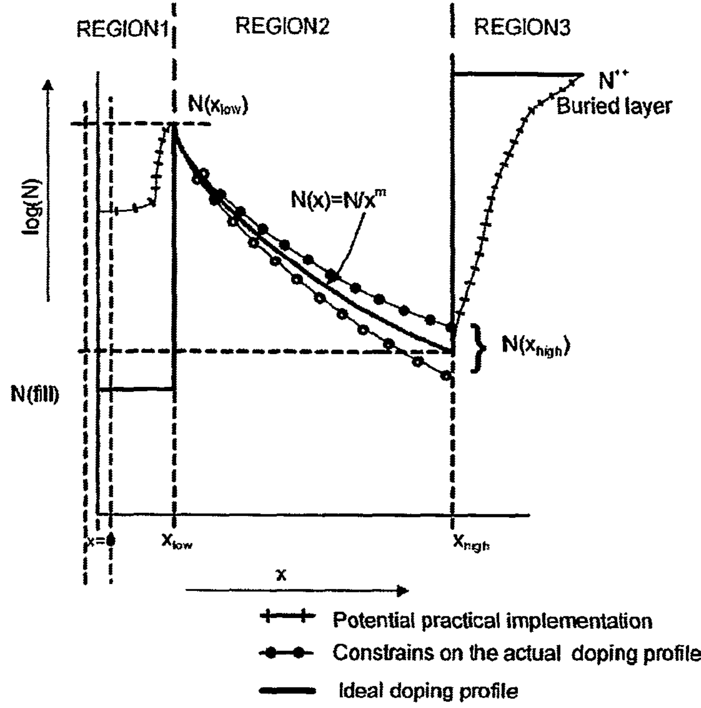


Fig 15

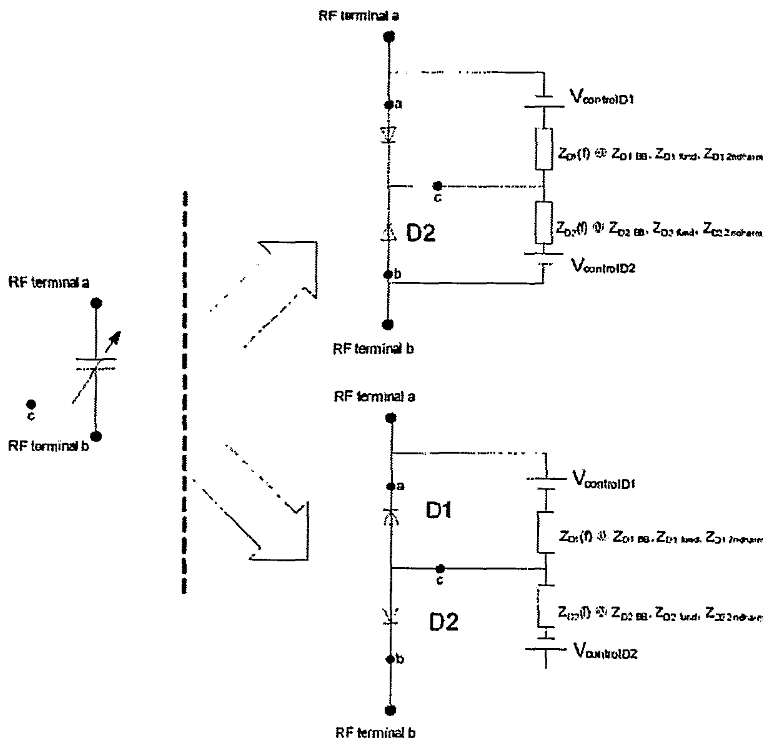


Fig 16

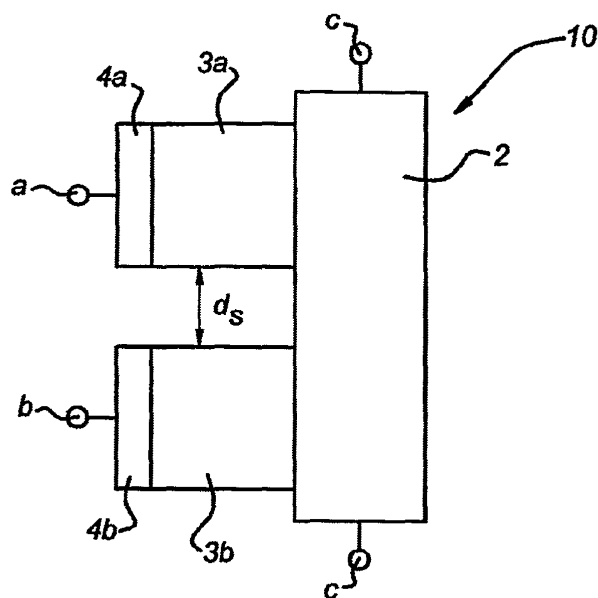


Fig 17

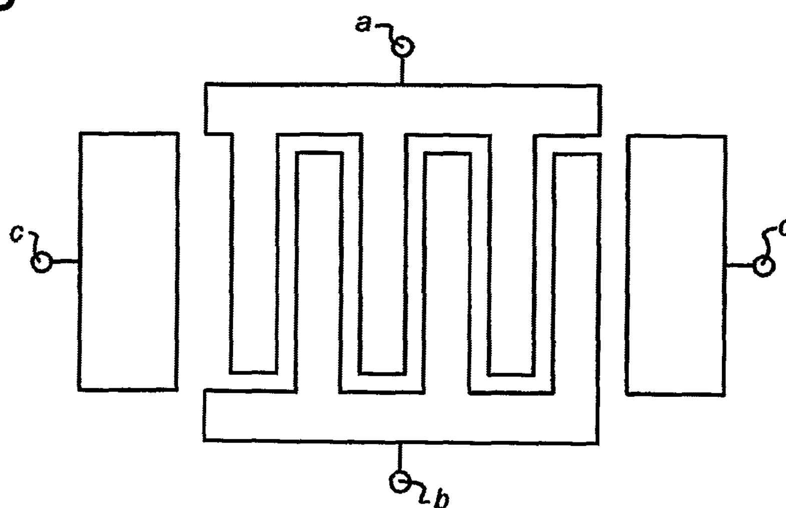


Fig 18a

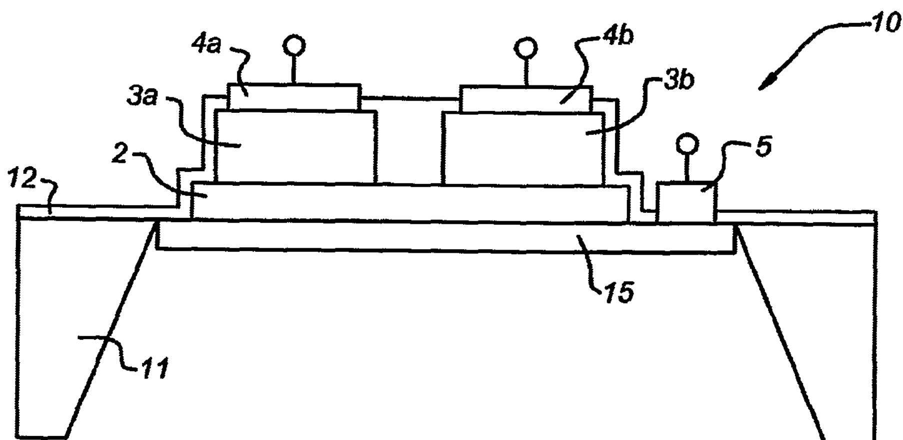
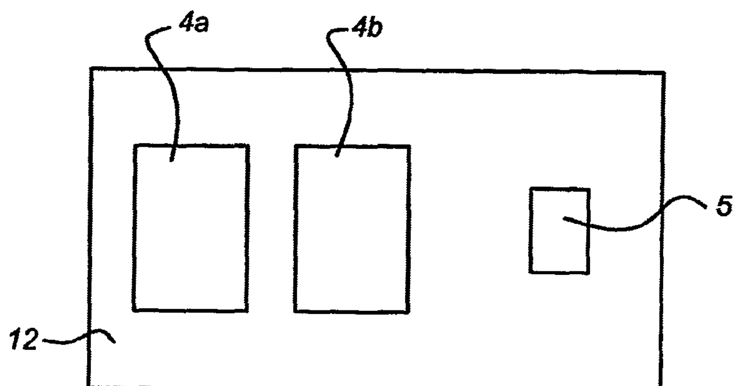


Fig 18b



INTERNATIONAL SEARCH REPORT

International application No
PCT/NL2006/050298

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L29/93 H03J3/20

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L H03J

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 97/18590 A (IOFFE VALERY MOISEEVICH [RU]; MAKSUTOV ASKHAT IBRAGIMOVICH [RU]) 22 May 1997 (1997-05-22)	1-4
Y	abstract figures 1-4	5-13
Y	BUISMAN K ET AL: "Distortion-Free Varactor Diode Topologies for RF Adaptivity" MICROWAVE SYMPOSIUM DIGEST, 2005 IEEE MTT-S INTERNATIONAL LONG BEACH, CA, USA 12-17 JUNE 2005, PISCATAWAY, NJ, USA,IEEE, 12 June 2005 (2005-06-12), page 157160, XP010844455 ISBN: 0-7803-8846-1 cited in the application the whole document	5-13

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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"P" document published prior to the international filing date but later than the priority date claimed

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
7 February 2007	15/02/2007

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Baillet, Bernard

INTERNATIONAL SEARCH REPORT

International application No
PCT/NL2006/050298

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2002/070815 A1 (TRAUB JOHANN [DE]) 13 June 2002 (2002-06-13) figure 1	11-13
A	DD 281 486 A5 (UNIV LEIPZIG [DD]) 8 August 1990 (1990-08-08) abstract; figures 1,2	1-4
A	US 3 764 415 A (RAABE G ET AL) 9 October 1973 (1973-10-09) abstract; figures 1-4	1-4
A	EP 0 452 035 A (UEYAMA KEN ICHI [JP]) 16 October 1991 (1991-10-16) column 2, lines 54-56; figures 4,6	1-4

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
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