Improved current matching in all-silicon triple-junction solar cells for wireless photo-electrochemical devices

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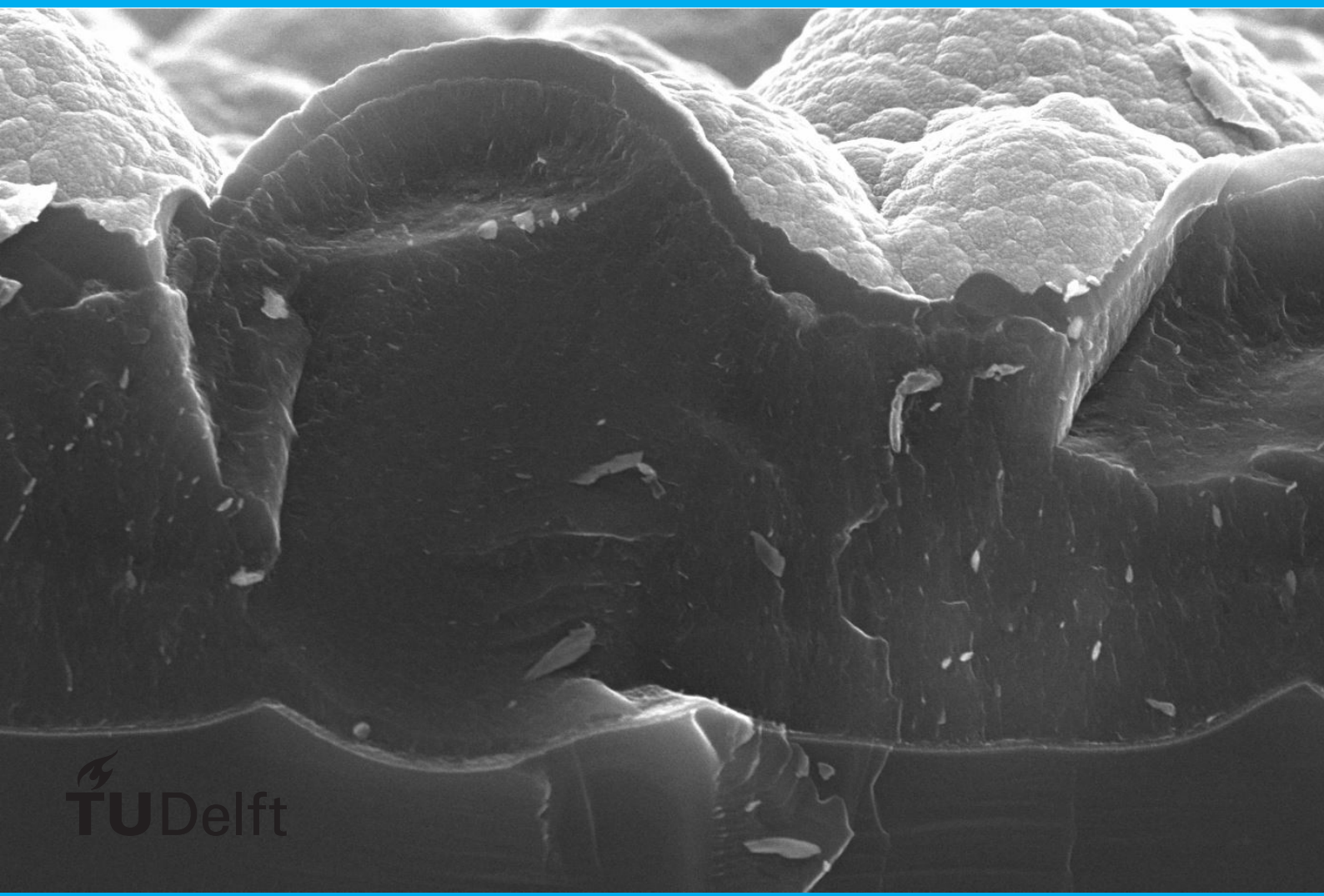

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by

Sander Miedema

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PVMD

Preface

When I started this project the initial goal was to further optimise the solar cell stack designed earlier, and to further process these into ”porous membrane photo-electrochemical cells”, or PMPs, capable of hydrogen production from sunlight and water only. This project appealed to me as I find both solar energy and hydrogen technology quite interesting personally, and I think these two technologies will play a leading role in the future energy system.

due to technical issues the time available for processing electrochemical devices was too short to make significant progress, so the focus shifted towards the solar cell optimisation. Still, I managed to get some decent work done, and have here a thesis I can be satisfied with. For this achievement I owe thanks to all the people that have, directly or indirectly, helped me these past 9 months.

First of all I want to thank my supervisor, prof. Arno Smets, for letting me do this project in his group, and for the feedback on the experimental results. I also want to thank my daily supervisor, Thierry, who was always ready to suggest one more measurement to add to the whole, but still managed to keep things a little ”chilled out”. I also want to thank Thijs for out collaboration, and for keeping me company on the exciting 3 hour journey that is wafer cleaning. I furthermore want to thank all the students from the DISCO and FLAMINGO projects, as well as Gianluca for the discussions and feedback during the biweekly meetings. I also want to thank Martijn, Stefaan and Daragh for keeping the equipment working, and for spending days looking at oscilloscope screens to make sure my EQE spectra looked as good as they do. Finally I want to thank my thesis committee, which besides Arno and Thierry consists of Dr. Rudi Santbergen and Dr. Mohamad Ghaffarian Niasar.

Furthermore I want to thank all my friends, the lovely people at Outsite, and my family for the video calls, zoom drinks and evening walks, and generally the much-needed distractions from sitting at home, typing.

Abstract

In a future energy system, chemical energy carriers that can easily be stored, like hydrogen, are of vital importance. One possible way of producing carbon-neutral hydrogen is by direct solar to hydrogen conversion in a photoelectrochemical cell (PEC). Silicon based multijunction solar cells are a possible candidate for the photovoltaic stack of these PEC devices. To make high efficiency PEC devices, the photovoltaic stack has to be optimised, especially with respect to reaching high current densities in the middle (nc-Si) cell.

In this work it was attempted to increase the current density of a triple junction device based on c-Si/nc-Si/a-Si absorber layers by varying the nc-Si absorber thicknesses and implementing various intermediate reflecting layers (IRLs) between the middle and bottom cell. These layers were based on silicon oxide, transparent conducting oxides (TCOs) and thin silver films. For each method it was attempted to give a quantitative comparison of how much the electrical performance is affected per unit of current gained in the middle cell.

Both increasing the nc-Si absorber thickness and the silicon oxide reflector thickness were found to be feasible methods of increasing the middle cell current density. The nc-Si absorber thickness leads to an initial rapid current gain, of about 2.6mA/cm^2 between 2.5 and 3.75 µm, reducing to just 0.8mA/cm^2 between 3.75 and 5 µm.

The electrical performance cost between 2.5 and 3.75 µm was calculated as a 2% reduction in V_{oc}*FF product per mA/cm^2 current gain. This cost increased to about 5% per mA/cm^2 between 3.75 and 5 µm. Increasing the absorber thickness beyond 5 µm is not considered feasible due to reducing current gains and mounting electrical performance losses.

Increasing the silicon oxide thickness can result in a current gain of about 1mA/cm^2. This comes at an electrical loss of 3% V_{oc}*FF product per mA/cm^2.

TCO based IRLs were found to quickly result in shunting, and in the case of indium doped tin oxide (ITO) based IRLs also damage to the surrounding cell structure resulting in poorly performing cells. Aluminium doped zinc oxide (AZO) based reflectors with proper electrical isolation from the edges gave only slightly reduced electrical performance, but failed to lead to a current gain in the middle cell.

Thin silver films were found to quickly rearrange into nanoparticles, effectively forming a plasmonic IRL. This IRL however suffered from high parasitic absorption, and as a result also did not lead to a current gain. A very thin silver film was however shown to slightly improve the electrical performance, at the cost of bottom cell current density.

Finally, a device was fabricated with both a thick nc-Si absorber as well as a silicon oxide IRL. The resulting device achieved a current density of 9.5mA/cm^2, a V_{oc} of 1.947V and a FF of 0.789, giving an efficiency of 14.6%. To the knowledge of the author this is the highest efficiency reported for this device configuration to date.

Furthermore, attempts were made to incorporate these stacks into PEC, by fabricating an microstructured anode, cathode and ion-conducting pores, to form a porous membrane PEC (PMP). The cathode and anode were successfully demonstrated, but the pore etching is yet to be optimised.

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1 Introduction

This chapter provides the context in which this research project took place, and introduces in detail the research carried out within this project. In section 1.1, the drivers for the current energy transition are briefly explained, and in section 1.2 renewable energy sources are introduced and the need for energy storage is explained. Section 1.3 outlines energy storage methods, and some of the motivators for using chemical fuels as storage medium. Section 1.4 introduces electrochemical fuel production methods and devices. Finally, section 1.5 introduces the DISCO project, of which this thesis was a part, defines the scope of this thesis and outlines the structure of the rest of this thesis.

1.1. Developments in the energy sector

1.1.1. Energy and the climate

Since prehistoric times mankind has used energy, which for most of (pre-)history was obtained in the form of biomass (e.g. wood), and sometimes wind and water. With the advent of the industrial revolution fossil fuels became widely available and for the first time people started to use non-renewable energy sources. With ever increasing energy use large amounts of CO_2 started to be released into the atmosphere. Since then the atmospheric CO_2 concentration has risen from around 280ppm to about 410ppm [27, 99].

Already in 1896 Arrhenius predicted that increasing atmospheric CO_2 concentrations would lead to warming of the global climate, based on the infrared absorption properties of CO_2 [97]. It has since been confirmed that the climate has warmed by about 1°C, largely due to fossil fuel derived CO_2 emissions [52, 66, 94, 98]. But in contrast to Arrhenius' perception [2], we now consider the effects of global warming to be particularly detrimental to human well-being, with sea-level rise, increasingly damaging weather events and lasting damage to ecosystems as just some of the consequences [66].

1.1.2. Drivers for change

Because of these considerations, there is now a growing political consensus that actions need to be taken. This is evidenced by the signing by most countries of the Paris climate agreement, making a commitment to limiting global warming to below 2°C [62]. More recently, several major economies have made statements committing to eliminating CO2 emissions before 2050 or 2060 [57, 91, 92].

Another important driver for the energy transition is an economic one. The cost of renewable electricity is falling rapidly, with LCOE of utility scale solar energy falling by 82% between 2010 and 2019 on average globally (see Figure 1.1). As a result the price of solar energy has, in many places around the world, dropped to values similar or lower than those of fossil fuels [26].

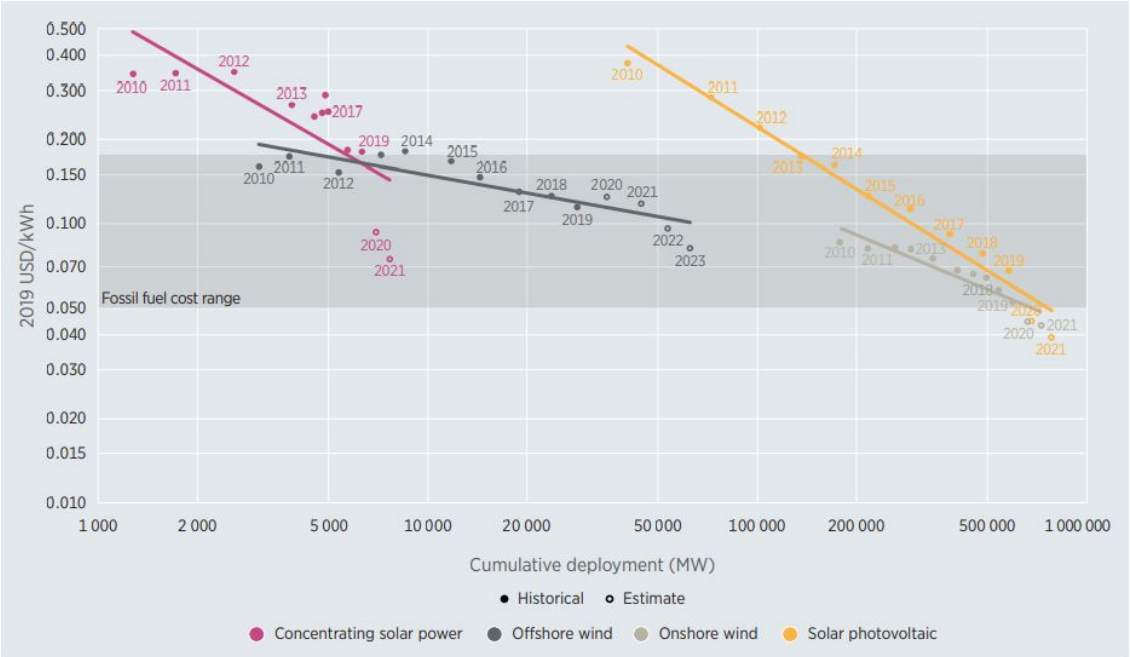

Figure 1.1: Global average LCOE of various types of utility scale power plants, plotted versus the cumulative deployment of the technology [26]. Solar energy costs can be seen to approach the lower end of fossil fuel costs.

Due to these two drivers it is almost inevitable that the coming years will see a major increase in renewable energy investments, and the eventual elimination of fossil fuels as energy source.

1.2. Carbon neutral energy sources

Eliminating fossil fuels requires completely overhauling the energy system, and tapping in to a completely different set of primary energy sources [24]. As mentioned, carbon neutral fuels and energy sources such as biomass and hydro-power have been used long before fossil fuels. However, with the rapid growth of the world population and standard of living that has occurred over the last centuries, the energy demand has likewise risen tremendously[89]. As a result biomass and hydro-power cannot be expanded to a sufficient capacity to meet the current energy demand [22].

Fortunately, there are other sources of renewable energy which have a higher potential, solar energy having the largest potential [22]. Direct solar energy to electricity conversion (photovoltaics, PV) has been applied since the 1950s, but in recent years has expanded rapidly. Over the past few years solar energy capacity has grown 20-40% per year [25], reaching a total capacity of almost 600GW, or 2.8% of the total global electricity production in 2019 [29].

From an environmental perspective this is good news, but there is a downside to using PV as the main energy source. Namely, PV is an uncontrollable energy source. PV generates most electricity when the sun is shining, which is mainly during summer days. But energy should be available whenever there is a demand, and the demand for energy is to a large degree not flexible (for instance, electricity for residential lighting is needed during the night time, so it is inherently mismatched with the PV output). Therefore, to ensure a continuous supply of energy, electricity storage needs to be introduced [61].

1.3. Electricity storage

1.3.1. Storage methods

At the moment, methods to store electricity are poorly developed [35]. Electricity cannot be stored as is, and has to be converted reversibly to another form of energy, such as the charge in a battery or movement of a flywheel. The most widely deployed storage method has historically been pumped hydro-storage [95]. This technology is however limited in its scale by constraints on the geography [35].

Several other storage technologies for electricity exist, the most well-known probably being batteries. Battery storage is highly efficient, but is not suitable for long term storage applications (for instance seasonal energy storage), mainly due to the high cost, which in 2018 was estimated at 380$/kWh capacity [30]. This is a huge value compared to the cost of easily storable fossil fuels. For instance, typical oil storage costs are estimated at around 7ct/barrel/month [10], which, based on an energy content of 1700kWh, corresponds to about 0.004ct/kWh/month. If we assume a battery has a life span of 10 years (optimistic for Li-ion [16]), battery storage costs 3.17$/kWh/month, almost 10000 times more (ignoring conversion losses). Because of the ease of chemical fuels storage over electrochemical storage, long term and large scale energy storage is more economically done in chemical form.

1.3.2. Chemical energy storage

As described above, chemical energy storage is in itself cheap and relatively easy. The more challenging step is obtaining the chemical fuels in a carbon-neutral manner. Globally speaking this can be done in two ways, one being to derive chemical fuels from biomass, and the other is using electrochemical processes.

Biomass is, as mentioned a resource with limited availability. Nevertheless, some estimates suggest that it could be expanded sufficiently to meet a significant part of the energy demand [36]. Furthermore, obtaining biofuels from biomass is a fairly well-established process that is (almost) competitive with fossil fuel prices [33]. Nevertheless, the use and promotion of biofuels has come under increasing scrutiny due to the fact that biofuel production competes with food production, and could thus potentially lead to food shortages [85].

Electrochemical fuel production does not face these problems, as it only requires inputs like electricity, water and air to produce chemical fuels. For this reason it is expected to become the method of choice in the future [9]. Hydrogen in particular has attracted attention, due to hydrogen production using electrolysis already being a relatively well established technology [31, 45], and water being an abundant safe feed stock. Furthermore, via well established processes it is possible to combine hydrogen electrolysis with carbon dioxide conversion [90] or ammonia production [100] to obtain even higher energy density fuels and important industrial feed stocks.

1.4. Electrochemical hydrogen production

Electrochemical water splitting consists of 2 half reactions, the oxygen and hydrogen evolution reactions (OER and HER), taking place on the anode and cathode respectively. The two half reactions are (in acidic conditions) given by:

$$2H_2O \longrightarrow O_2 + 4H^+ + 4e^- \qquad (anode, E^0 = 1.23V) \tag{1.1}$$

$$2H^+ + 2e^- \longrightarrow H_2 \qquad (cathode, E^0 = 0V) \tag{1.2}$$

A system for producing hydrogen using electricity is called an electrolyser. A standard electrolyser consists of an anode and a cathode where the oxygen and hydrogen evolution reactions (OER and HER) take place, respectively. Between the electrodes an electrolyte is placed, which allows for ion transport between the electrodes. Furthermore the hydrogen and oxygen should be separated to avoid explosive mixtures from forming, which is usually done with a membrane [12].

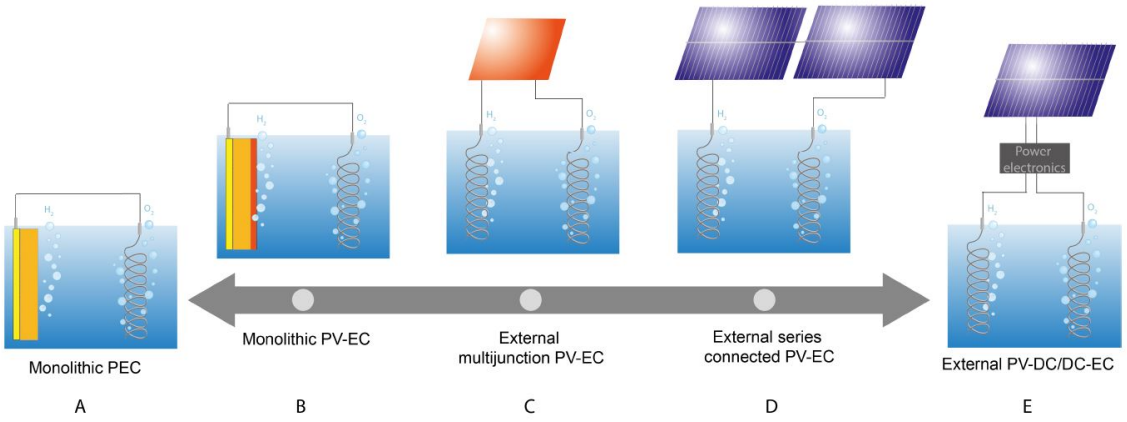

Figure 1.2: Different designs for a photovoltaics-driven water electrolyser [70]. (A) indicates an integrated PEC where the photovoltaic cell doubles as electrolyser electrode. (E) is a fully separated system where the PV and electrochemical cell are connected via power electronics.

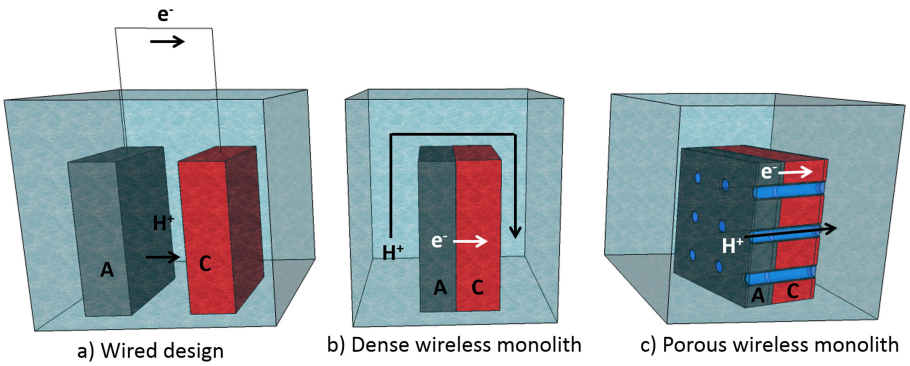

Figure 1.3: 3 different designs for PECs [96]. Moving from the wired design (a) to the monolith (b) eliminates wiring and a gas separating membrane, but results in a long diffusion pathway for the protons. The porous monolith (c) reduces the diffusion pathway by introducing ion transport channels (pores)

1.4.1. Photo electrochemical cells

Not part of the electrolyser but still necessary is a power source, for instance a solar cell. Although the power source can be separate from the electrolyser it is also possible to integrate the solar cell with the electrolyser, to form a photo-electrochemical cell (PEC). An advantage of integrating these two is the elimination of the connecting components like cabling and transformers, which can reduce the capital cost [58, 73, 96]. Integration can be done to a lesser or larger extent, as shown in figure 1.2, Thus there is not a sharp distinction between a PEC and an electrochemical cell driven by PV.

In figure 1.3b and c even further integrated devices is shown. These designs eliminate all wiring, and the photovoltaic cell doubles a a gas separating membrane. In figure 1.3 b the generated protons (see eqs. 1.1 and 1.2) have to travel around the cell. This can lead to issues when scaling up to larger cell areas, which can hamper scaling of the technology as a whole [39, 63]. To minimise the diffusion distance of the protons, pores can be included in the design. The porous design is called a porous monolithic photo-electrochemical cell, or PMP cell [23].

The PMP is the device type that is investigated in the DISCO project, of which the thesis is a part. This device consists of a multijunction solar cell, required to generate the potential for electrochemical reactions, a metal catalyst (platinum in this case) on front and back side to act as current collectors and catalysts for the electrochemical reaction, and finally the pores to facilitate

ion transport. The motivation for using this device structure and its operation are explained in more detail in chapter 2.

1.5. This project

1.5.1. Context of the thesis: the DISCO project

This thesis project was carried as part of the DISCO project. DISCO stands for direct solar to CO (carbon monoxide), and the goal of the project is to fabricate a device capable of converting carbon dioxide to carbon monoxide using sunlight. Although the focus lies on carbon monoxide, hydrogen can just as easily be produced using very similar device designs.

As part of the DISCO project, several thesis projects have already been carried out. These have worked on developing new absorber materials[8, 77], optimising the photovoltaic stack [5, 67, 101], developing new surface texturing [101] and investigating the pores [23].

1.5.2. The scope of this thesis

This thesis builds on this previous work, most directly the work by van der Nijen [101] and El Makkaoui [23]. This thesis attempts to further optimise the photovoltaic stack by investigating the effect of absorber thickness and intermediate reflecting layers on the current matching and electrical performance. Additionally some progress is reported on the fabrication of structural components of the PMP device.

1.5.3. Outline of the report

This report is build up as follows: in chapter 2 the theoretical framework for the relevant photovoltaic and electrochemical processes is explained. In chapter 3 the experimental methods and tools are introduced. In chapter 4 the experimental results for optimising the photovoltaic stack are reported, and in 5 the progress for fabricating the different components of the electrochemical device is reported. In chapter 6 the conclusion is reached, and the most important results are highlighted.

2

Theory

This chapter introduces the theoretical background needed for understanding the working of PV and PEC devices, in particular PMPs. Section 2.1 deals with the theory of photovoltaics, section 2.2 with the theory of electrochemical reactions and the relevant transport phenomena. Section 2.3 combines the information in the previous 2 sections to explain the PMP device design relevant for this thesis.

2.1. Photovoltaics

This thesis describes a PEC device based on a triple-junction (3J) photovoltaic device. To understand how such a device is created, here a short general introduction to photovoltaics is given. Following this a description is given of what determines the ”quality” of a solar cell, or in other words, how a PV device can be optimised. Finally a more detailed introduction to multi-junction PV devices is given.

2.1.1. The photoelectrical effect and semiconductors

The discussion of solar cells starts with considering the interaction of light with semiconductors. Like all bulk materials the energy levels in semiconductors can be described as energy bands which are filled with electrons from low energy bands up to high energy bands. The defining property of a semiconductor is that there is a ”small” gap between the highest occupied energy levels and the lowest unoccupied energy levels (the valence and conduction band, respectively). ”Small” in this context is somewhat arbitrary, but is usually considered between apprixomately 0.5 and 3eV [55, 71]. This gap is called the ”bandgap”, and its size is indicated as E_{g}. Without exposure to light, almost all electrons reside in the valence band, since thermal energy is insufficient to excite electrons across the band gap.

The interaction of light with a semiconductor is governed for a large part by this E_{g}. Since electrons can only transition between allowed energy levels, an electron can only be excited from the valence to the conduction band by absorption of a photon with an energy greater than or equal to E_{g}. Lower energy photons are not absorbed, and the material is transparent to these photons.

Once a photon has been absorbed the electron is moved to the conduction band, leaving behind an empty space in the valence band called a ”hole”. Both the electron and hole are free to move around the material, until they recombine and the electron falls back to the valence band.

2.1.2. Doping and electric fields: towards devices

Up until this moment nothing interesting has happened, merely the basic interaction of light with semiconductor materials. These materials become a lot more interesting however, when impurities are introduced. In a process called doping, impurity atoms are introduced into the semiconductor that have either one electron more or fewer in their valence shell. This introduces either

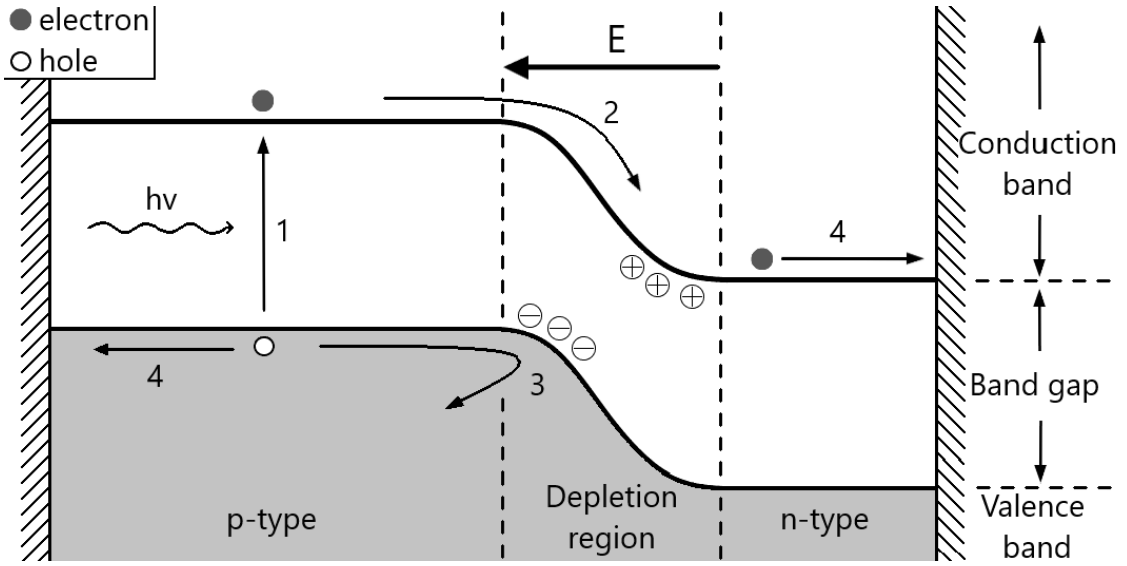

Figure 2.1: Illustration of the processes around a p-n junction represented in a band diagram. The vertical axis represents the energy level, the horizontal represents the position along a cross-section of the device. In the middle is the depletion region, with on one side positive donor ions and on the other side negative acceptor ions. The electric field points from the n-side to the p-side. Within a solar cell light is absorbed, creating an electron-hole pair (1). The minority carrier, in this case the electron as the absorption takes place on the p-side, is drawn across the pn junction by the electric field (2). The majority carrier on the other hand is deflected away from the junction by the field (3). As a result the charge carriers are collected at the contacts on opposite sides of the device (4)

an electron into the conduction band or a hole in the valence band. It is important to note that the dopant atoms are still present, and when they are separated from the electron or hole they acquire a net charge. Doping with electrons is called n-type doping, and is done with donor-atoms that become positively charged, while doping with holes is called p-type doping and is done with acceptor atoms that become negatively charged [88].

When two regions of different doping are brought together, a so-called p-n junction is formed. In this region the electrons from the n-type material will diffuse into the p-type material and the electrons and holes will recombine. This leaves behind a region with fewer charge carriers, which is called the depletion region. But as mentioned the dopant atoms remain in place, and have acquired a charge. Now the opposite sides of the junction contain free ions with a net charge, which is why this region is also called the space-charge region. Between these charged regions an electric field is formed, which is quintessential to the operation of solar cells [14]. An illustration of a p-n junction is shown in figure 2.1.

Also shown in figure 2.1 is what happens when light is absorbed near the p-n junction. In this case both the electron and the hole can diffuse towards the junction, but when they arrive at the junction they will feel an opposite force due to the electric field. As a result the charges are separated, with the electron ending up in the n-type region and the hole in the p-type region. At this point it is possible to introduce electrical contacts to both regions in the device. This provides a path for the electron to recombine with the hole, while donating the excess energy that it acquired from photon absorption to any appliance connected to the two contacts.

2.1.3. Figures of merit in solar cells

With the junction and contacts in place a functional solar cell is created. It is now useful to give a mathematical expression for the current-voltage characteristics of the device. An expression for the current-voltage behaviour for an ideal device (not taking series and shunt resistances and diode non-ideality into account) is given by equation 2.1[88]:

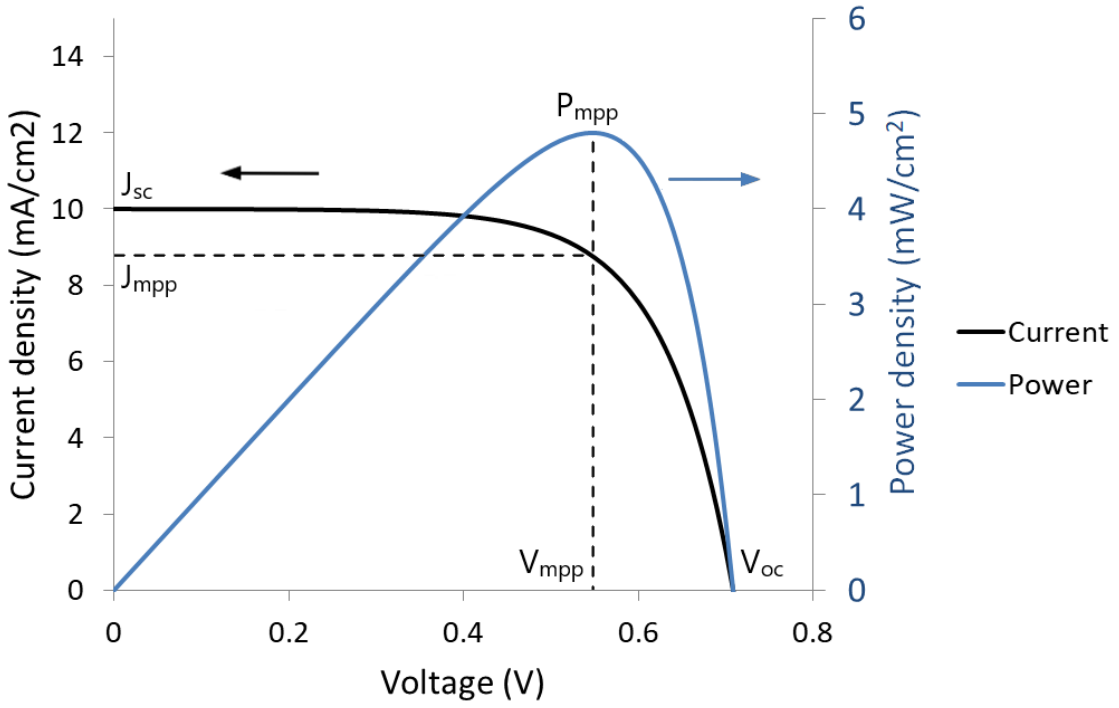

Figure 2.2: An example of a JV curve and a power output of a solar cell.

$$J(V) = J_{ph} + J_0(e^{\frac{qV}{kT}} - 1) \tag{2.1}$$

Here the J_{ph} is the photo-current, which corresponds to the amount of electrons excited by light absorption, J_0 is the reverse saturation current density which has an opposite sign to the photo-current, q the elementary charge, n the ideality factor, which describes the diode "ideality"and is 1 for an ideal diode, and k is the Boltzmann constant and T the temperature in Kelvin. The J-V curve can be seen as sum of the photo-current and a diode current (the 2nd term). An example of the J-V curve is shown in figure 2.2.

There are a few figures of merit used to quickly assess a solar cell that can be extracted from the JV curve. The short circuit current density J_{sc} is given by $J(0)$, or the intersect with the vertical axis. The open circuit voltage is the voltage V_{oc} at which $J(V_{\text{oc}}) = 0$, indicated by the crossing of the horizontal axis. The P_{MPP} is the power at the maximum power point (MPP), which is the point on the curve where the $J * V$ is highest. The final figure of merit is the fill factor (FF) which describes the ratio between the maximum power and the short circuit current density and the open circuit voltage as $FF = \frac{P_{\text{MPP}}}{J_{\text{sc}} * V_{\text{oc}}}$.

Before going into the "quality" of a solar cell, it is important to reconsider the importance of the band gap. As mentioned in section 2.1.1, only photons with an energy great than or equal to the band gap energy can be absorbed. Thus the bandgap defines the amount of photons that can be absorbed, and thereby the maximum achievable photo-current. At the same time, any excess energy that the electron acquires on top of the band gap energy is quickly lost as heat via thermalisation, limiting the achievable V_{oc}. Thus a trade off must be made, where the band gap is chosen such that the highest power output is obtained. For this to occur, the optimal band gap is around 1.3eV, and the conversion efficiency is around 33%, a limit called the Shockley-Queisser limit [86].

2.1.4. Optimising PV devices

Optimising a photovoltaic device is mainly a task of optimising the previously mentioned figures of merit by minimising all loss mechanisms. Starting with the J_{sc}, it is mostly determined by how efficiently all light falling on the solar cell is converted to electron-hole pairs, and the efficiency with which these reach the separate electrodes. Several factors can limit this value, most importantly reflection, shadowing, non absorption, parasitic absorption and carrier recombination.

Reflection arises at the interface between materials with a different refractive index. One method used to limit reflection is applying an anti reflective coating with a refractive index between that of air and the bulk semiconductor [72]. Another method is the use of surface texturing which lets light hit the material multiple times before being completely lost, thus offering multiple chances for being transmitted into the cell [38].

Shadowing occurs because of contacts placed on the front surface of the solar cell. The metal contacts block a part of the incoming light, reducing the cell current. This can be minimised by making the contacts as small as possible, or by placing them at the back of the solar cell in a design called the interdigitated back contact (IBC) cell [47].

Non absorption occurs especially at photon energy just above the band gap energy. These photons are usually weakly absorbed by the semiconductor, meaning the photons can pass through the semiconductor without being absorbed. Surface texturing can also reduce non absorption by allowing light to enter the solar cell at an angle, extending the path that light travels through the material without having to make the absorber layer thicker [38, 72].

Parasitic absorption occurs when the photons are absorbed, but not by the materials making up the p-n junction. Carrier recombination occurs when the carriers are absorbed in the active material, but cannot diffuse to the junction before recombining. Both these processes result in the loss of the charge carriers, and a decrease in current density.

The V_{oc} can be extracted from equation 2.1 by setting the current to 0. By manipulating the equation and assuming ideal diode behaviour it can be found that

$$V_{oc} = \frac{kT}{q} \log(\frac{J_{ph}}{J_0}) \tag{2.2}$$

Thus the V_{oc} is optimised when the photo-current is maximised, which was already discussed above, and the J_0 is minimised. This J_0, or the saturation current, depends on recombination of minority carriers before they can be separated at the junction. Its value is higher when the device has more defects, and is lowered by high material quality and good passivation [74, 83]. As a result, a great deal of effort is put into reducing the recombination in devices. A number of recombination mechanisms exist in semiconductors, being radiative, Auger and Shockley-Reed-Hall (SRH) recombination. Radiative and Auger recombination depend only on the material type and carrier concentration, and they cannot easily be reduced. Thus the focus lies on SRH recombination.

SRH recombination, also called trap-assisted recombination is recombination occurring via defects in the material that trap carriers. Methods to minimise this recombination are using high purity semiconductor materials, and not using excessively high doping in the absorber regions (as dopant atoms are also impurities).

Surface recombination is a special type of SRH recombination where the carrier traps are energy states at the surface of the material. Two general strategies for passivating surfaces are reducing the amount of surface trap states, for instance by coating the material with a selected blocking layer with a low level of interface defects [75, 87], and using doping to create an electric field that steers minority carriers away from the surface, a method called field-effect passivation [19, 20].

Finally, the fill factor is mainly affected by resistances in the material, and to lesser extend the V_{oc} and ideality factor. The optimisation of the V_{oc} was already described above. The ideality factor n is influenced by recombination in the junction, and in general when the V_{oc} is carefully

optimised the ideality factor n should be 1, but in low quality materials different values can be found, lowering the FF and V_{oc}

Two types of resistances that can be found in a solar cell are series and shunt resistance [88]. Shunt resistance is a resistance parallel to the cell. It forms for instance when a large defect penetrates the junction region, forming an electrical connection between the two sides of the cell. It causes a reduction of the cell current by the shunt current of VR_{sh}.

The series resistance is, as the name suggests, in series with the junction. The series resistance is caused by anything that impedes the current on its way through the device, for example by ohmic resistance in the wiring, the contacts and the different layers of the solar cell itself. The series resistance causes the voltage to be reduced by the drop across the resistance of IR_s (note that we now use I instead of J to indicate a current of a device rather than a current density, to correspond with the series resistance of the device)

2.1.5. Multi-junction devices

It was mentioned in section 2.1.3 that the band gap of a solar cell should be optimised to absorb sufficient carriers, but also minimise thermalisation losses. This was however a simplification, as it was assumed there to be only 1 absorber material. It is possible to stack multiple junctions, made from different absorber materials on top of each other, and to optimise every layer for a different part of the solar spectrum. Such a device is called a multi-junction solar cell.

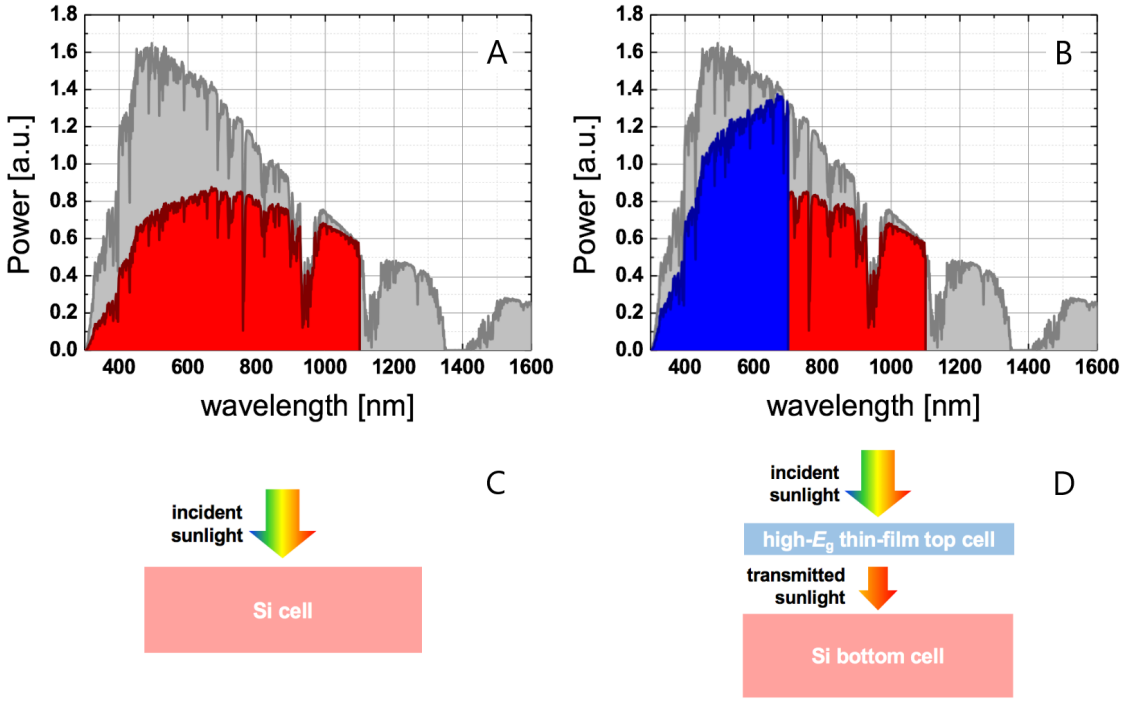

Figure 2.3: (A) energy absorbed by a silicon solar cell as a function of wavelength, minus thermalisation losses. In grey the energy density of the solar spectrum is shown. (B) energy absorbed by a tandem cell with a silicon bottom cell, minus thermalisation. In blue the absorption minus thermalisation by the top cell is seen, which is higher than that of the c-Si cell in the same spectral range. (C) in the single junction cell, light of all wavelengths enters the c-Si cell. (D) in the tandem cell, the short wavelengths are absorbed in the top cell, leaving only longer wavelength light for the c-Si bottom cell. Adapted from [108]

The reason why this is useful is illustrated in figure 2.3. In the single junction, high energy photons are absorbed but lose most of their energy via thermalisation. The higher bandgap cell in the tandem device can absorb the higher energy photons without losing as much energy to

thermalisation. The lower energy photons are not absorbed in the top cell, and are absorbed in the bottom cell. Because of this more efficient utilisation of photon energy, multi-junction cells can reach higher efficiencies that single junction devices [65, 88].

There are a few considerations that need to be made when building such a solar cell. The first is that the two cells both need to be contacted electrically. The most common electrical configuration, and the one used in the devices in this thesis (for reasons explained in section 2.3), is the 2-terminal configuration. This configuration has the two junctions stacked directly on top of each other, with a front contact on the top cell and back contact on the bottom cell. This means that electrons coming out of the n-side of one junction have to recombine with the holes from the p-side of the other junction by tunnelling (moving from one place to the other across a forbidden region) from the conduction to the valence band.

Tunneling across the bandgap occurs in a very narrow p-n junction called a tunnel recombination junction (TRJ). To reduce series resistance, the tunnelling current can be facilitated by introducing trap states inside the junction, for instance by introducing a very thin metal layer or highly doped semiconductor [43, 68, 107]. These layers will also influence the optical properties of the device by absorbing or reflecting light, and when optimising a TRJ these different aspects have to be taken into account [11, 43, 80].

The second consideration is that in this configuration the current that is generated in one junction has to pass through the other junctions. But each junction can only allow as much current to pass through as there is carrier excitation by light. Thus the current of the whole device is limited to that of the one with the lowest current. For optimal performance each cell should have exactly the same current, a condition called current matching [88]. In this configuration the voltage of the device is approximately the sum of the voltages of the individual sub cells.

2.2. Electrochemistry

A silicon 3J PEC device is a combination of a photovoltaic and electrochemical device. This section provides the background for explaining the design of the PEC device from an electrochemical perspective. To do so, first a general description of electrochemical reactions (red-ox reactions) and devices is given. Then a more detailed discussion is provided on what determines the current-voltage behaviour of an electrolyser.

2.2.1. Reduction and oxidation reactions

Electrochemistry is the branch of chemistry that describes reactions involving electron transfer. These reactions involve a reagent that gives off (an) electron(s), called a reductor, which is oxidised, and a reagent that takes up (the) electron(s), called an oxidiser, which is reduced. The oxidation and reduction reactions are separately called half reactions. Together they form the redox reaction.

Each half reaction is characterised by a standard potential, which describes how much energy is released per electron when the half reaction proceeds. Because a half reaction cannot occur separately these energies cannot easily be determined absolutely. Instead they are calculated relative to a reference half reaction, usually the standard hydrogen electrode [69].

Taking the difference between the standard potentials of the two half reactions making up the redox reaction gives the standard potential of the redox reaction, E^0. The standard potential for the system is related to the Gibbs free energy change of the reaction by [42]:

$$E^0 = -\frac{\Delta G^0}{zF} \tag{2.3}$$

Here ΔG^0 is the Gibbs free energy change per mol of reaction under standard conditions, z is the number of electrons supplied by the voltage source per converted molecule and F is Faraday's constant. Standard conditions are in this case defined as solids and liquids being in the state as they are found at 298K, 1 atmosphere pressure, all dissolved reagents at 1M and all gasses at 1 atmosphere [42]

2.2.2. Electrolysers

Although an oxidation half-reaction cannot occur without a reduction and vice-versa, it is possible to separate the reactions spatially. This is the basis of many technological applications such as batteries, fuel cells and electrolysers. An electrolyser is a device in which a potential difference is used to drive the red-ox reaction against the thermodymically favourable direction [69].

Although different designs are available, all electrolysers share the same basic components. The oxidation and reduction half reactions take place on the anode and cathode respectively. These electrodes are connected electrically such that charge transfer can occur. Furthermore, to close the electrical circuit, there is also a flow of ions possible through the electrolyte, which can be a liquid or a solid.

The magnitude of the required potential depends on the Gibbs free energy change ΔG of the reaction via equation 2.3. For water electrolysis the equilibrium potential is thus 237.1 kJ/mol / (2*96485) = 1.23V [78]. In general a higher potential is used as this is needed to drive the reaction at appreciable rates. This additional potential is called the overpotential η and is discussed in further detail in section 2.2.3.

2.2.3. Current voltage behaviour of electrolysers

The current-voltage relation of an electrochemical system depends on many parameters, such as the applied potential, catalyst material, reagent concentrations, system layout, temperature and pressure. In any case, a high reaction rate at a low potential is desired, as a low potential results in a high efficiency, and a high reaction rate in a compact, and thus less expensive, system.

This thesis will not delve into the effects of catalysts, temperature, pressure and reagent concentrations, but will instead focus on the system layout.

As mentioned in section 2.2.2, the standard potential of water electrolysis is 1.23V, which is the equilibrium potential at standard conditions. In reality the electrolyser will not operate at standard conditions, and this can have an influence on the cell potential. An important parameter that can change within the cell is the concentration of reagents, specifically of the ionic species (protons or hydroxyl ions for water electrolysis). The electrode potential at non-standard concentrations can be calculated with the Nernst equation [84]. The result for different ion concentrations is shown in figure 2.4.

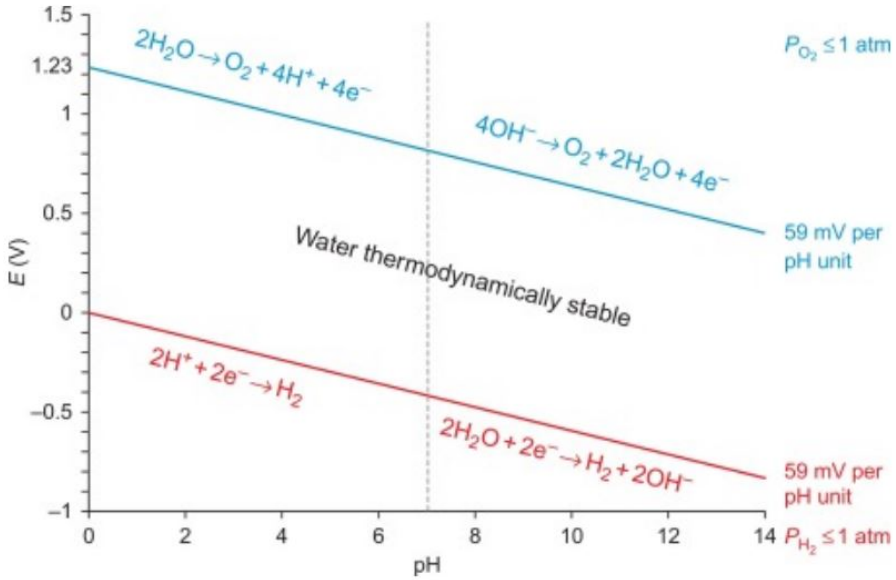

Figure 2.4: A Pourbaix plot showing the equilibrium potentials as a function of pH for the oxidation and reduction half reactions in a water electrolysis system, shown in blue and red respectively [84].

During operation protons are produced at the anode and are consumed at the cathode. This will cause the pH to decrease at the anode and increase at the cathode, causing the equilibrium potential to increase. A consequence is that, in order to reach acceptable conversion efficiencies, the transport of protons from the anode to the cathode should be very efficient [44]. One way to increase the rate of ion transport is to increase the mobile ion concentration by operating at either a high or low pH [40, 44, 102, 105]. Another important strategy is to reduce the distance that the diffusing species needs to cover [63].

On top of the Nernst potential the overpotential consists of the ohmic losses (e.g., in wiring) and the activation potential [64, 69]. The magnitude of the activation potential depends on the properties of the system, such as the catalyst [34, 79]. Applying a higher activation-potential results in a higher current density, which, for cases where the current is limited by the catalyst, is described by the Butler-Volmer equation (equation 2.4) [64]:

$$J = i_0(e^{(1-\beta)(F/RT)\Delta V_{\text{act}}} - e^{-\beta(F/RT)\Delta V_{\text{act}}}) \tag{2.4}$$

Here i_0 is the exchange current, which is determined by the catalyst, reagent concentration, temperature and cell design. The parameter β is called a symmetry factor and has a value between 0 and 1. V_{act} is the activation potential, F, R and T and the Faraday constant, gas constant and temperature, respectively.

At over-potentials close to zero the current is seen to drop to zero, while at higher currents it increases exponentially. The relation breaks down at high over-potential, when ohmic losses and concentration differences become dominant loss mechanisms [69].

Together these over-potentials cause the operating potential to be in the range of 1.5 to 2V in practical electrolyser systems [12]. This means that in a wireless PEC the photovoltaic component has to provide an operating voltage in this range.

2.3. Photoelectrochemical devices

In the previous two sections the properties of photovoltaic and electrochemical systems have been introduced separately. In this section the two systems are combined. Here the design choices that lead to the device structure used in this work are explained step by step.

The PMP design

As there are many different ways to design a system that converts solar energy to hydrogen, it is useful to start with defining a ”wish list”. This list defines some properties that the system should have and can help to constrain the design. One ”wish” that was mentioned in the introduction was the desire to design a system with the least amount of components. This means no cabling and inverters. Another important requirement is safety, especially important is avoiding explosive mixtures of hydrogen and oxygen.

The design then starts from the basis: capturing solar energy. This is done with a solar cell, for now with an unspecified photovoltaic stack. The solar cell is fundamentally a large flat area with two electrical terminals, front and back or both on the same side (for IBC solar cells). This solar cell now has to be modified to contain the 4 components of an electrochemical system mentioned in section 2.2.2, namely the voltage source, the anode, the cathode and the electrolyte.

Starting with the voltage source, it was mentioned in section 2.2.3 that the potential difference needed to drive water electrolysis is around 1.5 to 2V. Without inverters and cabling this potential has to be generated entirely by a single photovoltaic stack, which puts a constraint on the PV technology used. In particular, this voltage is too high to be achieved with single bandgap solar cell while retaining a appreciable current density. Thus a 2-terminal (2-T) multi-junction device is needed. Again this puts a constraint on the design as a back contacted 2-T multi-junction solar

cell would be challenging to fabricate and, to the authors knowledge, has not yet been realised[1]. Thus the design is constricted to a flat PV cell with electrical terminals on the front and back side.

Since no wiring is used, the anode and cathode have to be applied directly to the p and n side of the solar cell. On the back side the array can be fully covered with catalyst, but on the front side light should still be able to penetrate the device. The front side can thus be covered with a transparent conductive oxide (TCO) for lateral charge transport, on which the catalysts is deposited in a µm-scale dot pattern (from here on called microdots).

With these in place the final component is the electrolyte. As described in section 2.2.3, the electrolyte should provide an easy and fast pathway for transporting ions between the anode and the cathode. Both mentioned strategies, increasing the mobile ion concentration and shortening the transport distance, can and should be used to limit the overpotential. The first strategy is straightforward to apply by operating at either high or low pH. The second strategy is more problematic. Earlier the solar cell was described as a (large) flat area. In fact, most solar cell technologies are wafers-based which are at least 10cm in diameter. This means ions need to diffuse over up to 10cm, which would lead to a very low current or high overpotential [39, 63].

While it is possible to cut the solar cell into smaller fragments to reduce the distance, this can make the production process less cost-efficient. Smaller devices come with the issue of more complicated manufacturing when all these mm size components[63] have to be assembled in the final PEC module.

An alternative is to keep the solar cell intact, but introduce pores through the device through which ion conduction can take place [7]. These pores should be closely spaced to allow quick ion transport, yet small enough to still leave enough active material in the solar cell to collect sunlight.

The other item on the wish list, the safety concern, can now be solved fairly easily. The solar cell itself already forms a physical barrier between the anode and cathode, keeping most of the hydrogen and oxygen separated. Literature reports indicate that in this configuration there is still some gas-crossover however [105]. To prevent this diffusion of gas through the pores an ion conducting membrane can be used, like Nafion.

Now that the design is more or less complete, the final steps are to choose the photovoltaic stack, to decide whether the device should operate at high or low pH, and to choose the catalyst. An attractive choice for the photovoltaic material is a silicon based multijunction material. Silicon based photovoltaic materials (crystalline, nanocrystalline and amorphous, c-Si, nc-Si and a-Si respectively) are relatively cheap [50] and more stable in the harsh electrolyte conditions than other multijunction photovoltaic materials [60, 104]. Still, the choice of a Si-based device makes the use of basic electrolytes complicated, as exposed silicon is etched under basic conditions [105]. Thus either the exposed silicon should be chemically passivated completely, or acidic conditions should be used. In this thesis the latter option is used.

The choice for acidic reaction conditions also determines the choice of catalyst. Under acidic conditions the Pt/IrO_2 catalyst couple is the most efficient [56]. In this work IrO_2 was not used as it is not available in the lab where this project was carried out. Instead Pt was used for both the anode and cathode.

To summarise, the design features a silicon based 3J solar cell, with Pt contacts and nafion-filled pores for ion transport. The electrolyte is a concentrated acid, for high ionic conductivity. The complete design is also illustrated in figure 2.5.

[1] A metal wrap-through tandem solar cell has been realised [81]. Although this device has both contacts on the back side one could argue that, strictly speaking, this is a front-back contacted cell where a wire connects the front side contact with a current collector on the back side. This wiring would conflict with the stated desire to eliminate wiring. Regardless, such a design is very complicated to realise, and will not be considered in this thesis

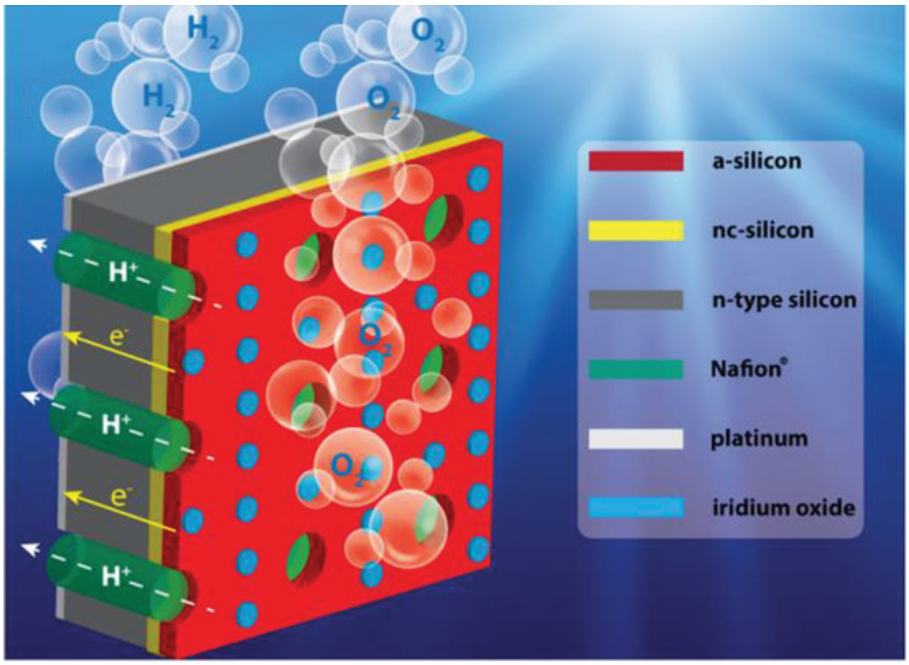

Figure 2.5: PMP design used in this work, as reported by [104]. Note that for this thesis no iridium oxide was used as this was not available. Pt was used instead to test the microdot deposition procedure.

3

Experimental procedures and equipment

This section explains the experimental processes used to fabricate devices, and provides more detailed information on the individual processing techniques used. Section 3.1 gives the overview of the fabrication process. Section 3.2 explains the different processing techniques used, and section 3.3 discusses the measurement techniques used.

3.1. Overview of the fabrication process

Solar cell fabrication starts with the silicon wafer. These wafers are textured to give a smooth pyramid texture. Details on this texturing process can be found in [101].

Subsequently, these wafers are cleaned of contaminants and surface oxide, and put in a plasma enhanced chemical vapour deposition (PECVD) cluster tool. In this tool the photovoltaic stack is deposited. The photovoltaic stack is then introduced into a sputtering tool for depositing indium-tin oxide (ITO) on the front and back side. Finally the metal contacts are deposited on front and back side by evaporation. A schematic of the process is shown in figure 3.1. Care is taken between each step to limit the exposure of sample to air. The solar cell is then ready to be characterised by JV and EQE measurements.

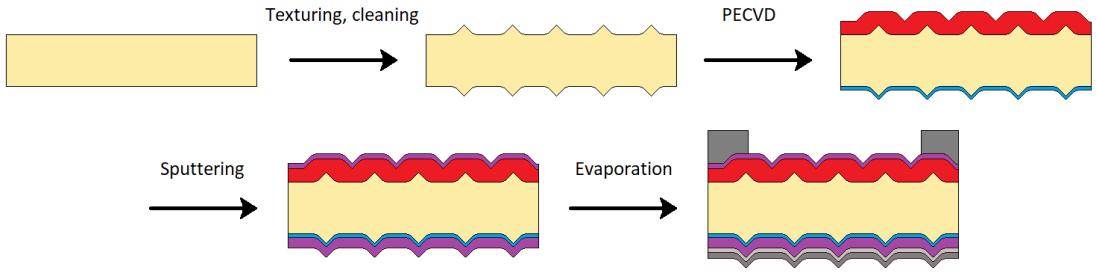

Figure 3.1: The process flow of solar cell fabrication. The silicon wafer is shown in beige, n-side PECVD stack in blue, p-side stack in red, ITO in purple, aluminium dark grey and silver light grey.

Fabricating the PMP device starts with the solar cell as fabricated in the description above, but without the metal contacts. Testing of the DRIE process as well as anode deposition were performed on cleaned flat wafers.

The first processing step is photolithography to make a mask for pore etching. This consists of spincoating a photoresist, exposing the photoresist through a mask, and developing. The result

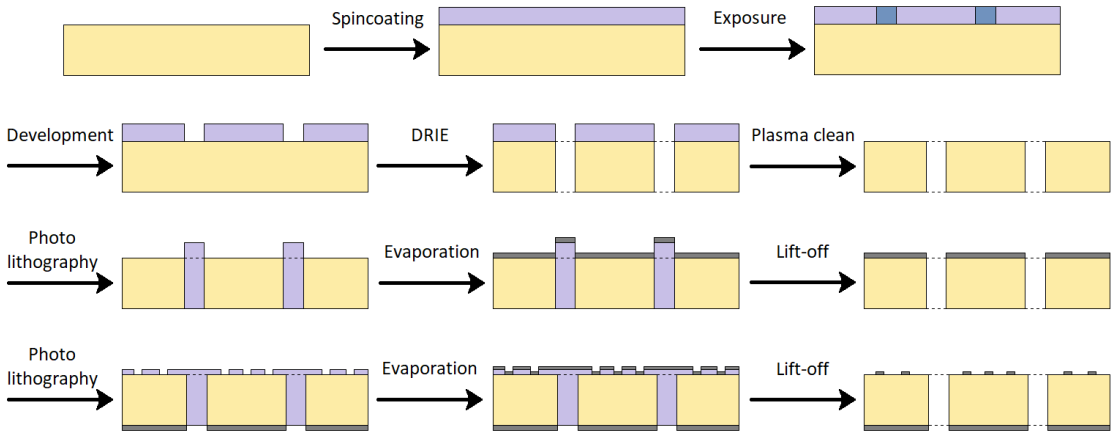

Figure 3.2: The process flow for fabricating the porous membrane devices. Silicon substrate is shown in beige, photoresist in lavender, metal in grey. Note that the photo-lithography step consists of a spincoating, an exposure and a development step, but it is shown as one step for simplicity

is a coating of resist with holes in it, which defines where the pores will be etched. The next step is the deep reactive ion etching (DRIE) of the holes, and once the holes are completely etched through an oxide plasma etch to remove the remaining resist (in the same machine).

The final step is the catalyst coating, both front and back. Each of these requires a photolithography step to define the pattern, and a deposition step. The platinum deposition is done using an evaporator. Finally the remaining photoresist is removed via lift-off in N-Methyl-2-Pyrrolidone (NMP).

3.2. Processing techniques

The individual steps in the process described above are explained in more detail in the following section. All processing steps were carried out in the cleanroom facilities of the Else-Kooi laboratory (EKL).

3.2.1. The cleanroom environment

The cleanroom is a type of processing room where airborne dust concentration is limited[41]. This is of vital importance to semiconductor processing, as dust or contaminants can easily destroy devices when micro- or nano-scale layers and features are present.

Cleanrooms come in different classes, to indicate the airborne particle concentration achieved inside. The EKL cleanrooms are divided up into class 100 and 10000. The class X classification indicates the amount of particles larger than 0.5 µm per cubic foot of air [1]. This classification is now replaced with the ISO 14644-1 classification. The class 100 and 10000 correspond to ISO 5 and ISO 7 according to the ISO 14644-1 standards[28], respectively.

This work was carried out in both cleanrooms. The wafer cleaning, photo-lithography and DRIE was carried out in the class 100, while the other actions took place in the class 10000.

3.2.2. Wafer cleaning

Cleaning was done with every sample before processing. For sample cleaning nitric acid (HNO_3, 99%), boiling HNO_3 (69%) and hydrogen fluoride (HF, 0.55%) were used. For both nitric acid treatments the residence time was 10 minutes, for the HF treatment 4 minutes. The HF treatment can also be done in a Marangoni drying setup to ensure complete removal of contaminants and liquid residues from the wafer surface[51].

The cleaning procedure followed for this research depended on the type of substrate. Clean wafers taken from a newly opened box were assumed to be free of contaminants, and only required the HF and Marangoni treatment. Other flat wafers were treated with 99% nitric acid and 69% boiling nitric acid before the HF and Marangoni treatments. After each nitric acid treatment the wafers are rinsed in DI water.

Textured wafers are more difficult to clean, and were therefore cleaned by repeating the procedure for flat wafers 3 times, but with Marangoni drying only after the last HF treatment. After the other HF steps the wafers were dried with spin-drying. The final HF treatment was done immediately before further processing to avoid formation of a new surface oxide layer.

Besides the samples themselves, any holders that came into contact with the samples were also cleaned, using a tissue with IPA. Glass plates were cleaned by sonication in aceton (10 min) and IPA (10 min).

3.2.3. Solar cell fabrication by PECVD

All layers of the photovoltaic stack (except the wafer itself) were deposited using plasma enhanced chemical vapour deposition (PECVD). In PECVD the material that is to be deposited, for instance silicon, is introduced into the deposition chamber as a gaseous molecule, like silane (SiH_4). Subsequently a plasma is generated in which the gas breaks down, causing the material to be deposited on the substrate [13].

The PECVD tool used for this thesis, called AMIGO, consists of a load lock, a transport chamber, 5 PECVD deposition chambers and one chamber for AZO sputtering (more info on sputtering in section 3.2.4). The first four chambers are each dedicated to a specific material type to avoid cross contamination. chambers 1-4 are, in order, designated for p-type, n-type, amorphous (a-Si) and intrinsic nanocrystalline silicon (nc-Si), respectively.

To deposit these different materials a number of gasses are available. Foremost are silane and hydrogen, both needed to deposit different (hydrogenated) silicon materials. To deposit silicon oxide CO_2 can be added. Finally, B_2H_6 and PH_3, both diluted with hydrogen, can be added to obtain p- and n-doped layers, respectively. The 5th chamber which is not used in the thesis also allows for deposition of silicon carbide and germanium alloys using methane and GeH_4 gasses.

Although these gasses determine for a large part what material is deposited, the exact structure depends on additional factors like the mixing ratio, temperature, pressure and generator power during the deposition. These parameters determine for instance whether a-Si or nc-Si is deposited, the density of the film, the defect density, and the resulting optical and electronic properties of the layer.

As described above there are many factors that can influence the deposition. To make depositions in AMIGO as reproducible as possible, the following procedure was maintained:

- Before introducing the sample, the deposition is tested. The reflected power is observed, and if necessary the load and tune values are adjusted so that the reflected power is <10% of the forward power.
- The sample is introduced into the deposition chamber.
- The sample is left for 30 minutes to allow the sample holder to stabilise at the deposition chamber conditions.
- The chamber is purged with nitrogen for 3 minutes.
- The reactant gasses are introduced to the reaction chamber and left to equilibrate for 3 minutes. The pressure is also set.
- The radio frequency (RF) or very high frequency (VHF, only in chamber 4) generator is turned on, 2 seconds later the plasma is ignited and the timer is started.

- When the timer is finished the plasma is turned off.
- If another deposition is done in the chamber the new process starts with introducing the new gas mixture.
- Before the sample is removed from the deposition chamber the chamber is purged for 3 minutes with nitrogen again.

An overview of the parameters used for each layer is given in appendix A. Here are also listed the layers deposited with sputtering and evaporation discussed in the next sections.

To increase sample throughput, first the silicon hetero-junction (SHJ) bottom cells were deposited on whole wafers. Next these cells were broken in half, and each half was used as a separate sample for the middle/top cell depositions. Since subsequent steps in the PMP processing require whole wafers, this cannot done for cells designated for this purpose.

3.2.4. TCO deposition using sputtering

The front and back contacts both contain ITO deposited on the solar cell surface. On top of this, some experiments were carried out to assess the influence of ITO, aluminium zinc oxide (AZO) and indium tungsten oxide (IWO) in the TRJ layer between the bottom and middle cell. All these materials were deposited by sputtering, the precise deposition parameters can be found in appendix A.

Sputtering is the process of bombarding a target material with ions to knock off small particles, which can then be deposited on the substrate [4]. For this thesis two sputtering tools were used, the one in AMIGO mentioned before and a dedicated ITO and IWO sputtering tool, a cryofox cluster UHV 6, also called ZORRO. ZORRO has a dedicated deposition chamber for each target material.

The ITO layer deposited on the back side is 150nm thick and and the front side 75nm. The front side ITO is patterned with squares, used to define the cell areas. For solar cell samples these are 24 cells measuring 4x4mm on each sample.

3.2.5. Metal deposition by evaporation

Evaporation is the process of heating the target to the point where it evaporates. This vapour is then deposited on the substrate. Two methods of evaporation were used for this work. For deposition of silver resistive heating was used to evaporate the material. For the other metals (aluminium, chromium, tantalum and platinum) E-beam evaporation was used. E-beam evaporation uses an electron beam focused on the metal target to generate a hot-spot with a sufficiently high temperature to evaporate the material [37].

Two evaporator tools were used for this thesis, the PROVAC pro 500s for aluminium, chrome and silver, and a CHA solutions std. evaporator for tantalum and platinum. Both systems use a quartz crystal microbalance to monitor the film thickness and deposition rate. The film thicknesses and deposition rates used for devices in this thesis are given in appendix A. During this thesis, the thicknesses reported are the target thicknesses, which may not correspond to a physical layer thickness (especially in the case of thin silver films).

The front contact of the solar cells consists of aluminium. The back contact uses a layer of silver as it has a higher reflectance. On top of the silver layer a chromium layer is deposited as an adhesion layer, followed by an aluminium layer.

The platinum is used as catalyst for the water electrolysis. To improve adhesion to the solar cell surface, an adhesion layer is needed. For this Tantalum is used. Tantalum is used for its high resistance to sulphuric acid electrolytes [76].

3.2.6. Photo-lithography

Photo-lithography is a method for patterning large areas with small feature sizes, and is therefore ideal for patterning the wafer-sized areas with µm scale patterns as required for this thesis.

Photo-lithography can be divided into 3 steps: coating, exposure and development. The first step, coating, involves coating a homogeneous layer of photosensitive material (photo-resist) on the substrate. The next step is to illuminate the sample through a mask with the desired pattern. The final step is the development, where the (non-)illuminated resist is selectively removed. This is done using a developer, a solvent that only dissolves either the exposed positive resist, or the non-exposed negative resist.

For this thesis the coating was done using a manually operated spin-coater. exposure was done using a SUSS MA/BA 8 mask aligner. Before applying photo-resist the wafers were heated in an oven at 110°C for 10 minutes to remove moisture, and treated with HMDS vapour for 10 minutes to improve resist adhesion.

For this thesis three patterning steps were done with photo-lithography, two steps for patterning the metal catalyst layer and one step for defining the holes. For the metal deposition a negative resist, AZ nLof 2020 is used, which is developed in AZ MF 322 developer. After metal deposition the remaining photo-resist was removed by sonicating at high frequency in hot (75-80°C) N-methyl-2-pyrrolidone (NMP) for 15 minutes.

For the hole pattern a positive resist is used, AZ12xT. This resist is developed in AZ400K developer. The AZ12xT resist is used for two reasons: first of all, using a positive allows for making a pattern complementary to the catalyst, which is patterned with negative resist, by simply using the same mask. Secondly, AZ12xT is a fairly thick resist, which is necessary to provide a strong enough blocking layer against the pore etching process. After the DRIE the remaining resist is removed by an O_2 etch.

The details of the photo-lithography process were optimised as part of this thesis. The details of the optimised processes are listed in appendix B.

3.2.7. Deep Reactive Ion Etching (DRIE)

DRIE is a process that allows for etching features in silicon with a very high aspect ratio and selectivity [46, 48, 54]. The DRIE machine consists of a low pressure chamber in which the plasma is ignited using an inductive coil, and a capacitive plate generator that directs ions from the plasma towards the sample. The power delivered by the coil and plate generators are indicated as source and bias power respectively.

The reason that DRIE can achieve such a high aspect ratio and selectivity is the combination of an isotropic, but selective chemical etch with an an-isotropic non-selective physical etch and a chemical passivation step. These processes are illustrated in figure 3.3. This figure shows a 3-step DRIE process, which consists of an-isotropic etching (A), followed by chemical passivation (B), breakthrough by ion bombardment (C) and subsequently the next etching step (D). The chemical passivation of the side wall remains intact because it is inert to the chemically etching gasses, and is not impacted by the ion bombardment that is directed perpendicular to the sample surface.

The 3-step DRIE process requires exact timing of gas flows with the bias power for the ion bombardment [46], which is technically challenging and is not applied in this thesis. Instead, a 2-step process is used that alternates between passivating gasses and etching gasses. The bias power is present during the entire etching process.

The systems used for this thesis was an ADIXEN AMS 110. This system is a single wafer etcher that has a 3kW ICP source and 300W bias power supply, and helium backside cooling. The gasses used in the chamber are SF_6, C_4F_8, O_2 and Argon. SF_6 is the main etching gas. Within the plasma it is partially broken up into fluor radicals which react with silicon to form gasseous

Figure 3.3: A schematic representation of a 3-step DRIE process. Adapted from [54]

SiF_4. O_2 has the purpose of reducing free fluorine radicals, forming the sidewall passivation layer and can be used to clean the sample of resist once the process is done. C_4F_8 is the passivating agent, when it is broken up it forms CF and CF_2 radicals that deposit as a teflon-like substance on the substrate [48]. Argon was used only to modify the plasma characteristics as argon addition can facilitate C_4F_8 plasma ignition [106].

The samples for DRIE consist of a 300µm silicon wafer, with additional silicon layers deposited on top, and a 150nm and 75nm ITO layer on front and back. As mentioned, a 12 µm AZ12xT resist was used as a masking layer. To protect the machine from damage once the pores were etched through, the wafer was mounted on a 500 µm carrier wafer with a 15 µm SiO_2 layer. The wafers were stuck together using Fomblin oil.

To achieve the high aspect ratios that are possible with this technique, the process parameters need to be tuned properly. The process development done for this thesis is described in more detail in chapter 5. The reference process, developed in [23] is listed in appendix C.

3.3. Measurement Techniques

The measurements were carried out in the facilities of the Electrical Sustainable power (ESP) lab, and the Kavli nanolab (only SEM imaging). As with the processing, the time samples spent exposed to air before the measurements was limited as much as possible.

3.3.1. Current voltage (*JV*) measurements

The JV measurements are carried out with a WACOM solar simulator. This device uses a xenon and a halogen lamp to reproduce the solar spectrum. The solar simulator is class AAA. The sample is cooled to maintain standard test conditions (AM 1.5 spectrum, 1000W/m^2, 25°C).

The WACOM measures the current as a function of voltage, and from the $J(V)$ curve it extracts the solar cell parameters J_{sc}, V_{oc}, FF, R_s and R_{sh}. The J_{sc} measured by the WACOM is however not taken as exact, as it depends on the cell area illuminated. A mask is used to ensure only a single cell is illuminated, but the exposed area is not exactly reproducible. Thus to obtain a reliable J_{sc} value the EQE measurement is used.

3.3.2. External quantum efficiency (EQE)

The EQE setup measures for wavelengths from 300 to 1200nm what fraction of photons incident on the cell is converted to current. Combining this data with the spectral photon flux allows for determination of the J_{sc} with much higher accuracy than JV measurements.

The EQE setup used consists of a xenon-arc lamp and a monochromator to provide the monochromatic light source. This light source is chopped with a frequency of 123Hz and focused in a spot on the cell. The current output of the cell is measured and the signal is filtered by a lock-in amplifier to isolate the 123Hz signal and filter out any background and bias light. The setup is calibrated with a reference silicon diode.

When measuring multijunction cells bias light is used to saturate the cells not measured, and make the target cell current limiting. This allows for the determination of the current generation in each cell separately. Bias light was provided by 8 LEDs ranging from 365 to 935nm.

3.3.3. Scanning electron microscopy (SEM)

For imaging the photovoltaic stack and the layer thicknesses, SEM was used. SEM imaging uses an electron beam focused on the sample to image its topography. The microscope used for this thesis was a FEI Nova NanoSEM 450 located in Kavli nanolab Delft.

3.3.4. Ellipsometry

Ellipsometry was used for accurately determining film thicknesses and deposition rate of PECVD processed films that are too thin to accurately image using SEM. To determine the deposition rate a test deposition was done on a glass plate. The tool used for determining the thickness was a J.A. Woollam Co. ESM-300. The analysis was performed with the CompleteEase software package.

3.3.5. Reflectance measurements

Reflectance measurements were performed on a PerkinElmer Lambda 1050+ UV/VIS/NIR spectrometer. The measurements work by placing the sample in the back side of a highly reflective integrating sphere. The sample is then illuminated and the reflected light is reflected in the integrating sphere until it reaches the detector. The setup is calibrated before measuring with a dark baseline and a reflective reference (a spectralon disc).

For each sample the same cell was measured as was measured by EQE, to allow for a direct comparison of the reflection and conversion spectra. This can for instance help identify parasitic absorption losses.

4

Results from optimising the solar cell stack

This section describes the results of the optimisation of the photovoltaic stack of the c-Si/nc-Si/a-Si 3J cell, the structure of which is shown in figure 4.1. The photovoltaic stack developed in previous work [101] led to a 3J device with adequately high V_{oc} and FF for hydrogen production, but a uneven current distribution across the different sub-cells. A shift of current from the bottom cell to the middle and top cells could increase the overall device current and thereby the efficiency and hydrogen production rate of a PEC.

Optimising the current distribution was done by varying the i-nc-Si absorber thicknesses, reported in section 4.1, and by adding reflecting layers to the TRJ connecting the middle and bottom cell. The layers tested are SiO_x, which is already present in the reference device and is reported in section 4.2, transparent conducting oxides (TCOs) reported in section 4.3 and thin metal (silver) layers in section 4.4.

Each of the methods mentioned above can in theory increase the current density in the middle cell at the expense of the current density of the bottom cell. The methods however also come at a price in terms of electrical performance. The goal of this chapter is to obtain a quantitative picture of not only how current can be gained with each method, but also how (much) the electrical performance is affected.

Finally, section 4.5 reports on a top performing device fabricated based on the results from the previous 4 sections.

The different concepts were first tested in tandem cells with a SHJ c-Si bottom cell and a top cell with an i-nc-Si absorber. Next these concepts were implemented in the c-Si/nc-Si/a-Si 3J devices. Tandems cells were used first because they are simpler to fabricate and characterise, and thus allow for the effects of different layers to be identified more easily.

Unless stated otherwise, the J_{sc} is derived from EQE measurements, and V_{oc}, FF, R_s and R_{sh} from JV measurements. For the results from JV measurements, the values listed are the average and standard deviation calculated for the 5 best performing 4x4mm cells in terms of V_{oc}*FF product.

4.1. The nc-Si and a-Si absorber layer thicknesses

The first layer that is investigated is the intrinsic (i-)nc-Si absorber layer in the SHJ/nc-Si tandem. Increasing the thickness of the i-nc-Si absorber layer is the most straightforward method to increased the current generation in the nc-Si cell. The absorber layer thickness however also influences the electrical properties of the material. This trade off was analysed by varying the i-nc-Si absorber thickness from 2.2µm to 4.4µm. The cells were analysed with JV and EQE mea-

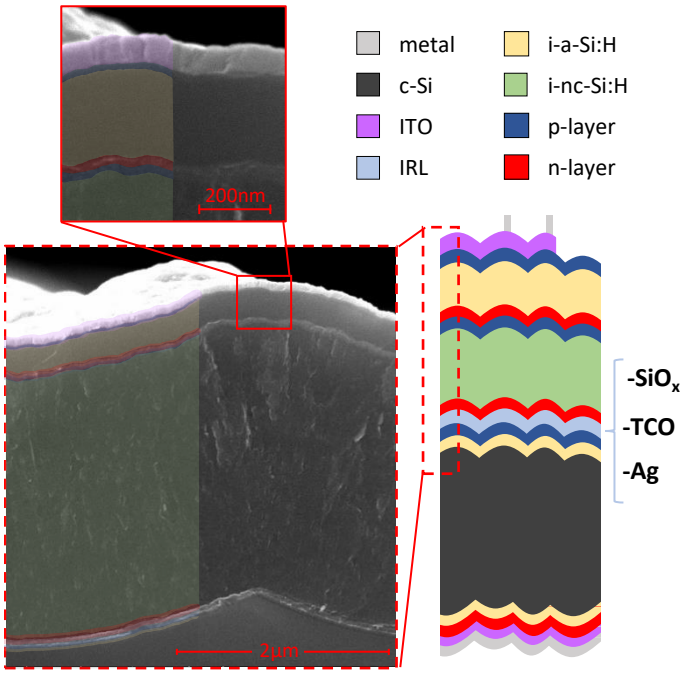

Figure 4.1: The cell structure investigated in this thesis, with the different layers indicated on a SEM image of the structure.

surements.

The most important results are shown in figure 4.2. In figure 4.2**A** the V_{oc} and FF are shown. The V_{oc} shows a gradual decrease with increasing thickness, which can be explained by increasing recombination as charge carriers have to travel further to reach the p- and n-layers.

The FF does not show a clear trend, but does show significant variation. A possible source of this variation is the series resistance, which shows more or less the inverse behaviour of the FF. This high and variable series resistance most likely stems from improper p-layer deposition in these samples. This occurred due to a communication error in the software resulting in the wrong parameters being communicated to the generator, leading to the wrong plasma conditions being used.

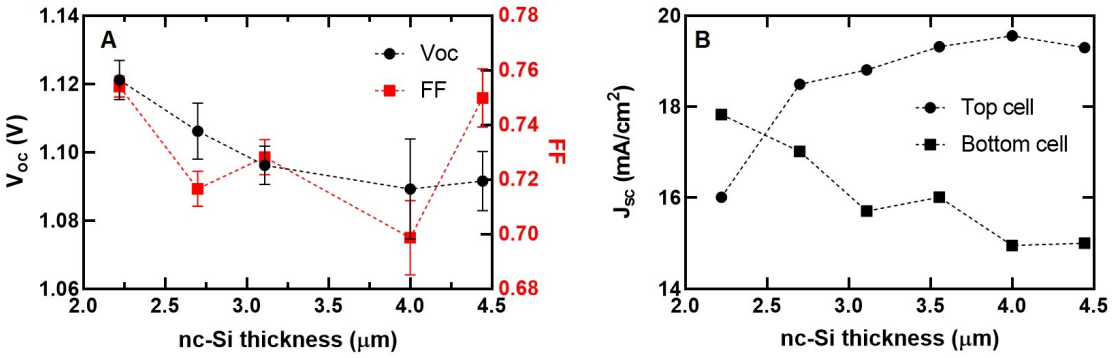

Figure 4.2: Measurement results for the nc-Si thickness series in tandem cells, showing the V_{oc} and FF (A) and the top and bottom cell J_{sc} (B). The sample that was fabricated with 3.6µm nc-Si was fabricated in a different series. The V_{oc} and FF of this sample deviated from the trend, possibly due to different chamber conditions or storage time before processing, and was left out of the graph for this reason.

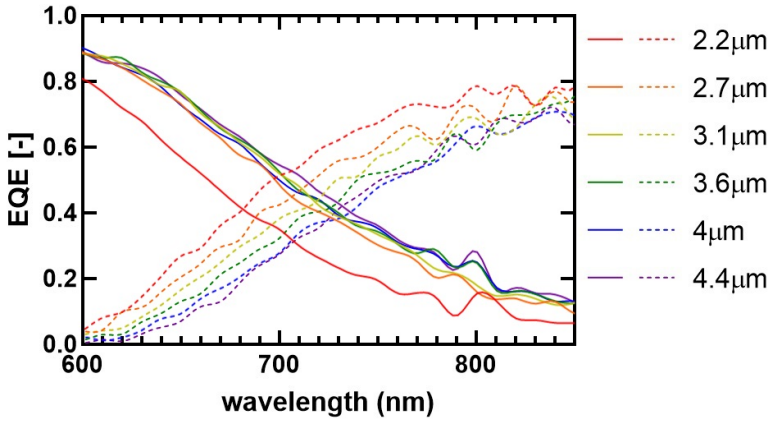

Figure 4.3: The EQE of c-Si/nc-Si tandem cells with varying i-nc-Si absorber thicknesses, in the region where both top and bottom cell show significant absorption. The solid line represents the top cell and the dashed line the bottom cell. It can clearly be seen that the shift between the 2.2 µm and 2.7 µm cells is substantial, while the 4 µm and 4.4 µm curves overlap closely, indicating diminishing gains in top cell current density with increasing absorber thickness

The J_{sc} is shown in figure 4.2**B**. The increase in current density from the top cell can clearly be seen, as is the corresponding decrease in bottom cell current density. In total going from the 2.2µm 4.4 µm, about 3 mA/cm^2 is shifted from the bottom to the top cell. Most of this gain is found between 2.2µm 2.7µm, while the increase levels off almost completely once the thickness reaches 4µm. This can also be seen in the EQE spectrum shown in figure 4.3.

What is clearly shown is that, regardless of the nc-Si absorber thickness, the current density in the bottom cell remains fairly high at around 15 mA/cm^2. This value is more than a third of the current that a Si-based 3J cell can collect. Since adding an a-Si cell will mostly divert current away from the nc-Si cell, the c-Si cell will maintain a high current density even in 3J configuration and will probably not be current limiting.

The nc-Si thickness was then varied in the 3J cells. The resulting V_{oc} and FF results are shown in figure 4.4**A**. In this case it is clear that both the V_{oc} and FF decrease with increasing absorber thickness. Again, the V_{oc} may be explained by the increase recombination in the thicker absorber layer. The FF also decreases, which could be partially due to the increased current matching.

Poor current matching commonly results in a high FF because the high-current density cell is performing closer to open-circuit conditions even when the tandem cell is at maximum power point. This leads to an operating voltage closer to the V_{oc} than in current matched conditions, and thus a higher FF.

The current density shown in figure 4.4**B** shows that the current density in the bottom cell is reduced by 3.5mA/cm^2 when doubling the i-nc-Si thickness from 2.5µm to 5 µm. This current density is effectively moved to the middle and top cells. It is worth mentioning that the a-Si top cell deposition is not spatially homogeneous, and thus the thickness can vary between cells measured. This can explain the variability in the J_{sc} reported in the top cell, and since the middle cell receives the light filtered by the top cell, also the variability in the middle cell J_{sc}.

What is also observed is that the total current density amounts to only 32mA/cm^2, compared to about 35mA/cm^2 for the tandems. This could be the result of the presence of another TRJ between the top and middle cell, with another SiO_x layer that can reflect light. Reflectance measurements, shown in figure 4.5 show that the tandem cell reflection has a minimum around 650nm. The reflection is highest around 400nm where the photon flux density of the solar spectum and EQE are much lower, and near 1200nm where the cell does not effectively absorb light anymore. The 3J cell in contrast has a much higher reflectance around 750nm and around 1000-1100nm, and

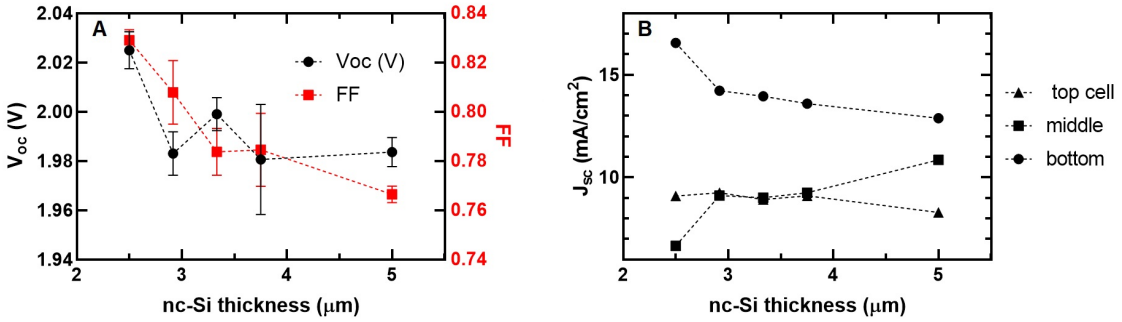

Figure 4.4: Measurement results for the nc-Si thickness series in 3J cells. V_{oc} and FF are shown in (A) and the top and bottom cell J_{sc} in (B)

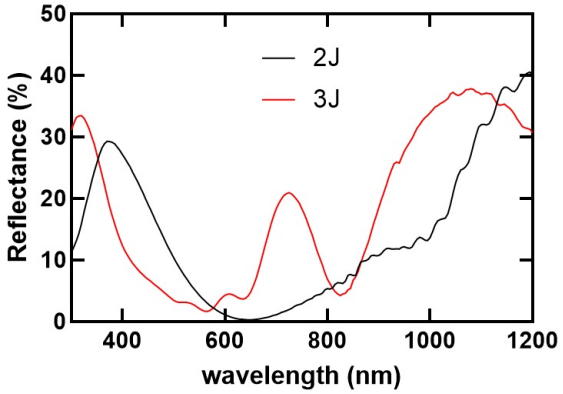

Figure 4.5: The reflection spectra for a tandem and a 3J solar cell. The nc-Si absorber thickness of the cells is about 3.6 µm for the tandem cell and 3.75 µm for the 3J cell.

consequently is able to absorb less light and produce a lower current density.

This specific series also suffered from an excessively thick front side TCO and window layer. The front side TCO thickness was tuned via the deposition time, using a measured deposition rate. However, the deposition rate can vary as the sputtering target is consumed, and as a result the ITO thickness may not be completely reproducible. It may thus be useful to deposit a test layer to determine the deposition rate before depositing the front side ITO.

With this data it can be determined that a shift in current of 3.5mA/cm^2 can be achieved with respect to a 2.5µm i-nc-Si absorber layer by doubling the absorber thickness. This comes at the cost of reducing the electrical performance, charaterised by the $V_{oc} * FF$ product from 1.68 to 1.52, a reduction of about 10%.

An important note to this is that as the nc-Si absorber becomes thicker the current gain becomes smaller. The gain between 2.5 µm and 3.75 µm is 2.6mA/cm^2, while adding a further 1.25 µm adds only 0.8mA/cm^2.

It can however also be seen that the loss in electrical performance between 3.75 µm and 5 µm is smaller than between 2.5 µm and 3.75 µm. Nevertheless, based on literature reports it can be assumed that further increasing the thickness will lead to more rapid loss of electrical performance due to the increasing series resistance and recombination [6, 103]. Furthermore, depositing a nc-Si layer that is too thick on a smooth textured wafer will eventually lead to cracks in the film resulting in a lower electrical performance.

A possible explanation for the rapid initial FF loss is that the 2.5 µm cell is quite far from current matched, while the subsequent cells (except for the 5 µm cell) have the top and middle

cell current matched, which can contribute to a lower FF. In nc-Si based single junction cells fabricated within our group [101] a more linear drop in FF with increasing absorber thickness has also been observed.

Based on the above it can be assumed that an increase in i-nc-Si absorber thickness beyond 5 µm is not feasible as the minor current gain is outweighed by a much larger electrical performance loss. It can then also be concluded that the 3J device cannot be made current matched by increasing the a-Si and i-nc-Si absorber thicknesses alone. If current matching is to be achieved, more advanced current matching schemes will be required.

When generalising these results it may be useful to compensate for the current matching influence on the FF, by assuming a more or less linear loss of about 0.025 per µm of absorber. If this is assumed, the cost of shifting 1mA/cm^2 can be calculated. When increasing the absorber thickness from 2.5 to 3.75µm, the V_{oc}*FF drops by about 5.9%, while between 3.75 and 5 µm it drops bout 3.8%.

Based on this, the cost of shifting current from the bottom to middle cell when increasing the absorber thickness from 2.5 to 3.75µm is about 2% V_{oc}*FF product per mA/cm^2. When increasing the absorber thickness from 3.75 to 5µm, this cost increases to about 5% V_{oc}*FF product per mA/cm^2.

4.2. Varying the SiO_x thickness

This section explores the effect of the thickness of the n-nc-SiO_x layer in the TRJ between the bottom and middle cell. The SiO_x layer is already present in the reference device, as it has been found to be an effective material as n-layer for TRJs in thin film devices [18].

Besides having an electrical effect, the lower refractive index of the SiO_x layer relative to the surrounding layers causes light to reflect at the interfaces. This is the working principle of using SiO_x as an intermediate reflective layer (IRL) as has been reported in literature on silicon based multijunction devices [11, 21]. This IRL can shift current from the bottom cell to the middle cell to further approach current matching conditions.

All these effects depend on the thickness of the SiO_x layer. To test these effects a set of SHJ/nc-Si tandem cells were made where the SiO_x thickness was varied from 10 to 60nm.

The results of this series are shown in figure 4.6. What is seen clearly is that the FF is lowest for the 10nm sample. This can have two reasons: either the SiO_x layer is too thin to effectively function as n-layer result in poor band allignment on opposite sides of the SiO_x layer [18], or the other cells have a higher FF because they are less current matched. The first possibility is confirmed by a higher series resistance value being measured for this sample. Nevertheless, the second explanation likely also has a minor contribution to the lower FF.

The V_{oc} shows more or less an opposite trend to the FF, with the 10nm sample having a higher V_{oc} than the other samples. The reason for this is unclear to the author. It is possible that for the thinnest SiO_x layer the crystal growth is not yet fully established, giving different interface properties, possibly leading to better passivation (but still with poor current collection). The opposite trend in FF and V_{oc} has been observed within out group before [101]. The variation in V_{oc} is however smaller than the variation in FF, so this gain in V_{oc} for the thin SiO_x layer does not result in better overall performance.

The J_{sc} shown in figure 4.6**B** show an increase in top cell current density with increasing SiO_x thickness. This shift is also visualised in the EQE spectra shown in figure 4.7. By increasing the thickness from 20 to 50nm about 1.4mA/cm^2 is shifted from the bottom to top cell. An additional 0.5mA/cm^2 is lost, presumably by reflection. The 10 nm sample again shows deviating behaviour, possibly because the thin SiO_x layer is unable to block holes generated in the top cell from reaching the TRJ, causing a current loss. This is also demonstrated in the EQE spectra where the top cell of the 10nm sample has a much lower EQE than of the 20nm sample, while the bottom cell EQEs overlap closely.

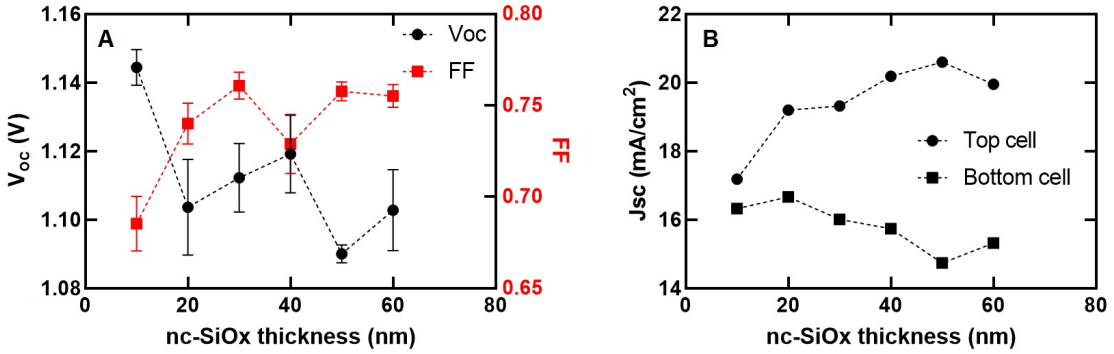

Figure 4.6: The V_{oc} and FF (A) and top and bottom cell J_{sc} (B) for the SiO_x thickness series with tandem cells.

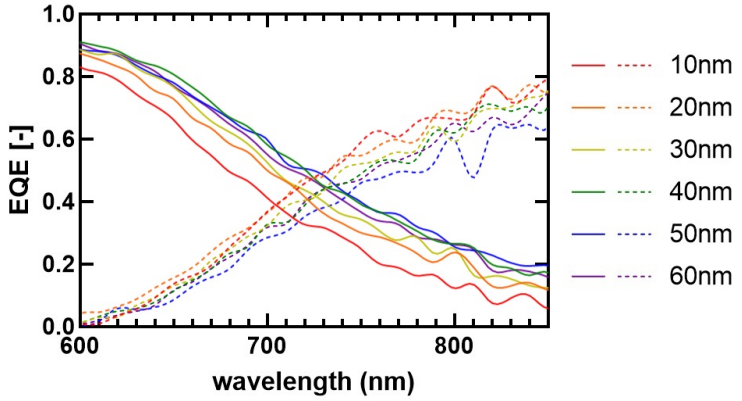

Figure 4.7: The EQE spectra of the SHJ/nc-Si tandem cells with varying SiO_x thickness in the range where both sub cells show significant absorption. Solid lines indicate top cells, dashed lines bottom cells. As intended, the EQE of the top cell increases with increasing SiO_x thickness, while the bottom cell EQE decreases. Increasing the SiO_x thickness from 10 to 20nm increases the top cell EQE singificantly, while the bottom cell does not lose much, indicating that reflection is not a major contribution to this shift.

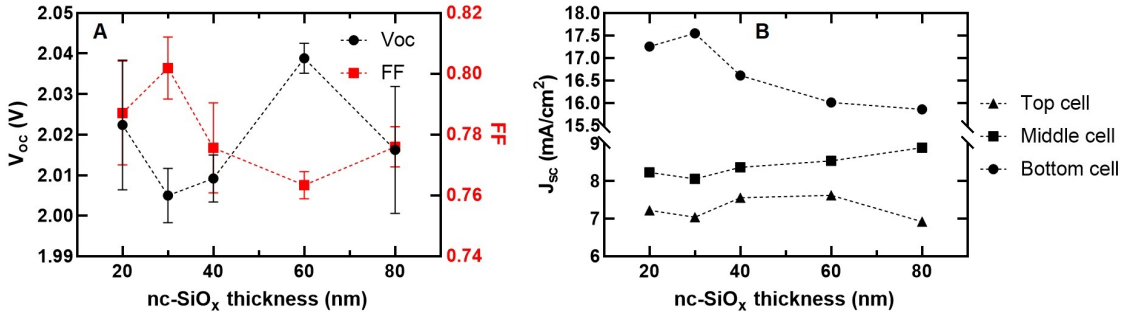

Figure 4.8: The V_{oc} and FF (A) and top, middle and bottom cell J_{sc} (B) for the SiO_x thickness series with 3J cells.

A series of 3J cells with SiO_x thickness varying from 20 to 80nm was deposited next, the results of which can be seen in figure 4.8. It can be seen that, as was the case for the tandems, the sample with 30nm SiO_x has the highest FF. Different than in the tandems series is the decrease in FF with thicker SiO_x layers, which was not significant in the tandems. This difference can be explained by noting that, while in the tandem series the ticker SiO_x samples were *less* current matched, in the 3J series they are *more* current matched.

The V_{oc} has, as was the case for the tandems, a somewhat irregular trend opposite to the FF trend. Considering that this trend has been observed in 3 different multijunction systems it is most likely a genuine trend, although it is unclear what the exact cause is.

Regardless of this trend, just as was the case with the tandem series, the relative variation in the FF is larger than that of the V_{oc}. Together, the $V_{oc} * FF$ looses about 3% between 30 and 80nm thickness.

The J_{sc} shown in figure 4.8**B** shows again the effect of light reflecting away from the bottom junction, which sees a decrease of 1.7mA/cm^2 between 30nm and 80nm SiO_x. The top and middle cells collectively gain 0.7mA/cm^2. This is less than in the tandem cells, which could be because a thinner ncSi layer was used in this series. A thinner ncSi layer can absorb a smaller fraction of the reflected light.

In general, the fraction of reflected light that is absorbed, and therefore the effectiveness of the IRL, depends on the path lenght that light travels through the absorber after it is reflected. This is influenced by the thickness of the middle and top cell absorber thicknesses, but also for instance by the texture since light reflected at an angle by a texture travels a longer distance through the absorber material, giving it a higher chance of being absorbed.

Based on the two series it is plausible that a current gain of 1mA/cm^2 can be achieved using SiO_x as IRL.

Altogether it was shown that depositing 30nm of SiO_x yields cells with superior electrical properties. A current gain of about 1mA/cm^2 in the middle cell can be obtained by using a thicker SiO_x layer, at a cost of about 3% of the $V_{oc} * FF$ product.

4.3. Adding a TCO to the TRJ

A second material type that was investigated as IRL layer were TCOs. Like SiO_x, TCOs are transparent and have a lower bandgap than silicon. The benefit of a TCO is its low activation energy, which ensures high tunnelling probability and high conductivity, combined with transparency. This together allows for the use of thick layers while keeping the series resistance and parasitic absorption low. This could in theory enable the use of interference to reflect specifically those wavelengths the are likely to be absorbed by the middle junction, while allowing longer wavelength light to pass through to the bottom junction.

For the first attempt ITO was used in tandems, in various configurations. These configurations were

- Only ITO
- ITO with a thin n-a-Si buffer layer
- ITO with a 5nm AZO layer
- ITO with 3nm silver and 5nm AZO layer

In each configuration 10nm ITO was used, and for the configuration with n-a-Si buffer layer a thickness series of 5, 10 and 80nm was done. The electrical performance in terms of the V_{oc}*FF product for the thickness series is given in figure 4.9**A**. Clearly the addition of ITO to the junction leads to a major loss of performance. This can readily traced back to the shunt resistance, shown

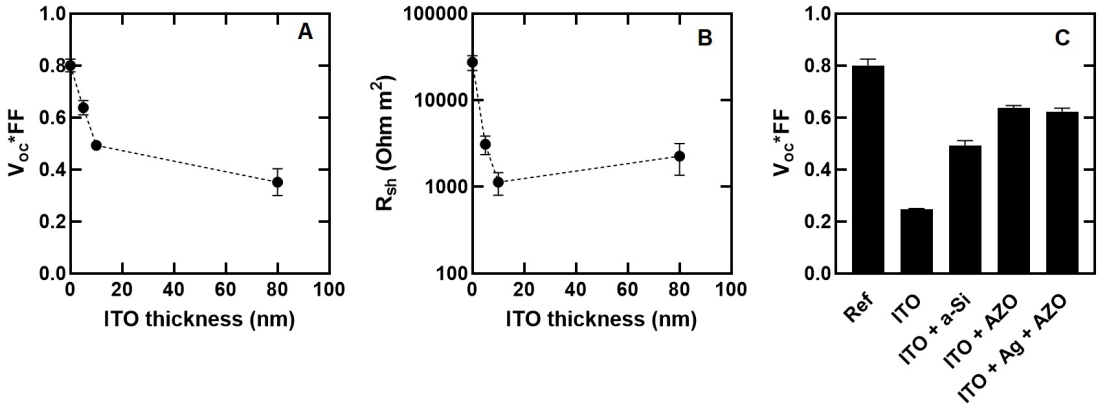

Figure 4.9: The effect of adding ITO in various thicknesses with a-Si capping layer to the TRJ on the V_{oc}*FF product (A) and shunt resistance (B). In (C) the V_{oc}*FF product for cells with several TRJ stacks with 10nm ITO is shown.

in figure 4.9**B**. In figure 4.9**C** it can be seen that different configurations of ITO all show some degree of performance loss with respect to the reference cell.

A likely explanation for this is that the high lateral conductivity of ITO causes shunting pathways to be connected throughout the cell. It should be noted that the bottom cell consists of a 300 µm wafer and the top cell of about 3 µm nc-Si, both of which are very unlikely to be shunted due to their thickness. Rather it is likely that the shunting takes place around the edges of the wafer.

This explanation cannot fully account for the results from figure 4.9**C**, as here it is seen that, paradoxically, the addition of even more conductive layers (Ag and AZO) results in a reduction in shunt resistance. A possible explanation for this is that either the deposition of ITO on the SHJ, or the deposition of the nc-Si cell on the ITO causes damage to the TRJ layers. Such damage could for instance lead to an electrical connection between the SHJ absorber and the n-side of the nc-Si based cell via the TCO causing poor current collection.

To test this second hypothesis, different TCOs were used. AZO was used as it was shown in the previous run to increase the performance of the ITO-based TRJ, and IWO was used as it could be deposited at room temperature, lowering the risk of damage to the underlying layers.

The results are shown in figure 4.10**A** and **C**. It can be clearly seen that both materials still give low shunt resistance, although for thin AZO layers the shunt resistance is similar to the reference samples. This suggests that at least for AZO, junction damage is not a major issue, but (edge-)shunting is the cause of efficiency loss.

The shunting was believed to be along the edge of the wafer, so to block these pathways the front side of the AZO-wafers were inscribed with a diamond-tip pen around the cells. Next the JV measurements were repeated, the results of which are shown in figure 4.10**B**. As can be seen, no significant improvement in the shunt resistance was achieved.

It is possible that the scribe did not effectively block the shunting pathway, so to be more thorough, the wafer edges of the 60nm sample were broken off entirely. This action is difficult to control, so it led to the area with cells being broken up as well. This yielded a single cell on an isolated fragment with high shunt resistance ($> 10^5 \Omega$ m^2), while the other larger fragments saw a more modest improvement.

Thus it was concluded that the shunting pathways are not via the edge, but via the bulk. Assuming the shunting path does not penetrate the entire wafer, the shunting pathway must then be through the nc-Si top cell, and through the p-side of the SHJ. Since the SHJ is build up off an n-type wafer, connecting the front contact with the front side of the wafer could be enough to cause the shunting. Nevertheless, dividing up the TCO layer in small patches can limit the amount of shunting pathways connected to a single cell, allowing for a performance improvement.

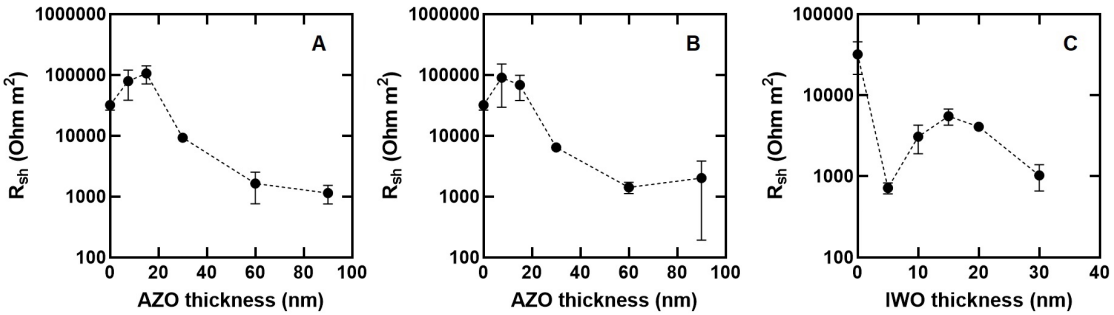

Figure 4.10: Shunt resistances for c-Si/nc-Si tandem cell with AZO in the TRJ (A), AZO in the TRJ after scribing with a diamond pen to isolate cells from the edges (B), IWO in the TRJ (C).

With this knowledge a new procedure was established, in which the deposition of the TCO, as well as the subsequent middle and top cell, would be done through a mask. By doing this there can be no current-conducting TCO connecting the cell with the rest of the wafer area.

A series of 3J cells with AZO as TRJ material was fabricated and characterised. The shunt resistance (figure 4.11) still decreases with addition of AZO, but does not show a clear correlation with increasing AZO thickness. Most importantly, the values observed are of the same order of magnitude as obtained in other 3J cells.

The V_{oc} and FF shown in figure 4.12**A** do show a drop with insertion of TCO, but not nearly as large as the drop in the initial series (figure 4.9). Furthermore, as with the shunt resistance, the V_{oc} and FF do not drop strongly with increasing AZO thickness. This could allow for the use of thick AZO layers that use interference to reflect light to the middle junction.

With a reasonable electrical performance achieved, the next thing to assess is how the AZO affects the current distribution. In figure 4.12**B** the J_{sc} of the cells are shown. From this figure it can be seen that there is no significant increase in top and middle cell J_{sc}. In fact, the sample with the thickest AZO layer has the lowest top cell + middle cell current density of the series, while there is a major decrease in bottom cell J_{sc}.

The reason for this is shown in the EQE spectra shown in figure 4.13. Here the EQE and 1-R spectra of the 80nm AZO sample is compared with a sample without AZO. For the 80nm AZO sample a much bigger offset between the 1-R and total EQE can be seen. This indicates parasitic absorption or poor charge carrier collection is happening here.

To test if a different TCO would give better results a series was fabricated with ITO, which has better electrical properties [59]. A series of tandem and 3J cells was fabricated using the same procedure as in the AZO series mentioned above, with ITO as TRJ material. Unfortunately the electrical performance of this series was significantly worse than for the AZO series, with efficiencies (far) below 5%. This can have several reasons.

One reason could be that ITO is more conductive than AZO, allowing for more efficient electrical connections of shunting pathways. However if the conductivity of the TCO was the limiting factor on the shunt resistance, the shunt resistance for the AZO series should be more strongly correlated with TCO thickness. Another option would be that ITO induces more shunts through the i- and p-layers of the SHJ, forming more shunting pathways, although the mechanism by which this would happen is unclear. A final suggestion is that the deposition chamber was simply more contaminated during the deposition of the ITO series, resulting in more shunting pathways in the top cell, middle cell and SHJ p-layer.

Based on the results above it appears the TCOs cannot be used as IRL. All TCOs lead to shunting, with ITO and IWO performing significantly worse than AZO. AZO does give electrically

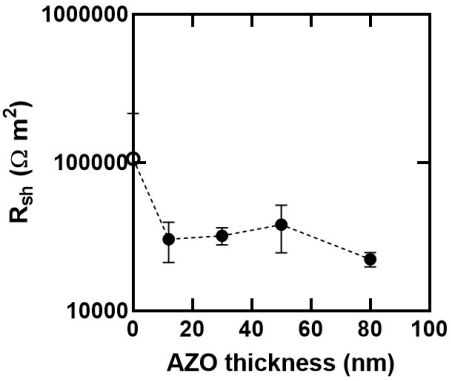

Figure 4.11: The shunt resistance for the 3J series with AZO deposited through a mask. The data point at 0nm represent a sample deposited without a mask and is provided as a quick comparison. Since the mask can influence the plasma close to the sample surface and thus influence the sample performance this sample should not be interpreted as a reference sample for the masked AZO series.

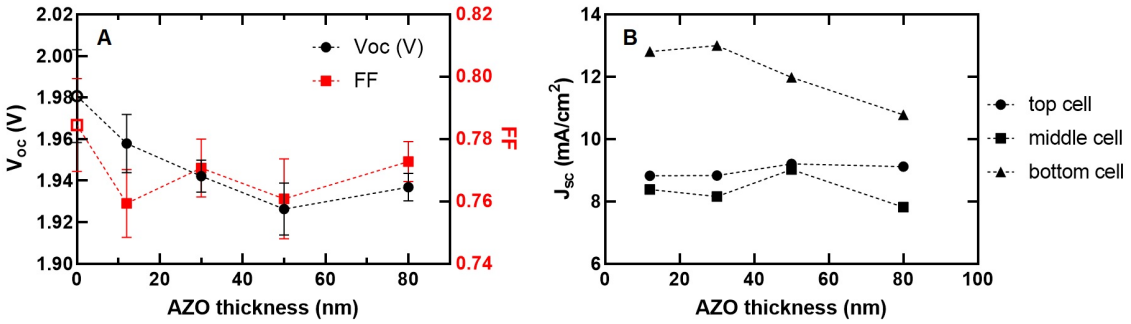

Figure 4.12: The V_{oc} and FF (A) and J_{sc} (B) for the 3J series with successfully isolated AZO layers. Again, the data points at 0nm represent a sample deposited without a mask and is provided merely for comparison.

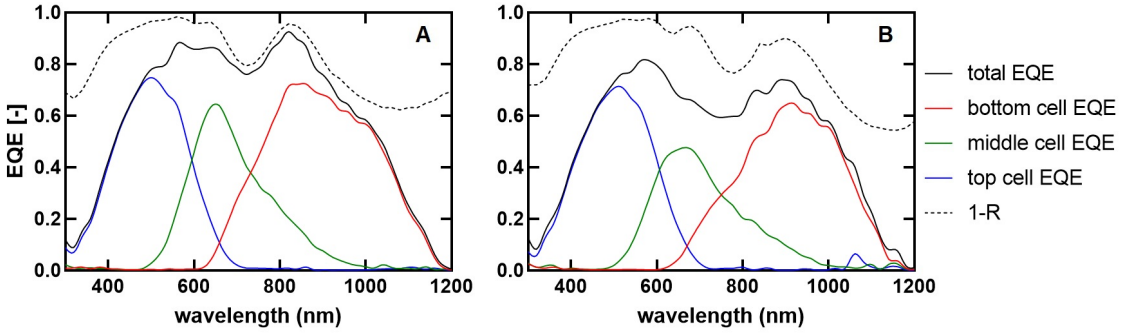

Figure 4.13: The EQE spectra of a sample without AZO (A) and with 80nm AZO (B). The total EQE (sum of top, middle and bottom EQE) of the sample without AZO closely follows the 1-R line, indicating low parasitic absorption and efficient charge collection. The sample with 80nm AZO has a much greater offset between these two curves.

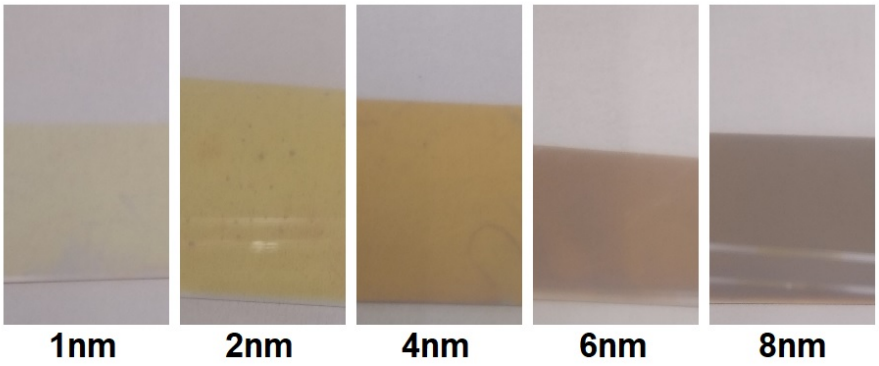

Figure 4.14: Ag films of various target thicknesses deposited on glass substrates. This set of thicknesses was used in the 3J series.

well-performing cells, but either parasitic absorption or poor carrier extraction prevents any positive impact on the current density in the middle cell from being reported.

4.4. Adding a silver layer to the TRJ

A third suggestion for a IRL material type that could enhance the multijunction performance is a metal layer. The function of a metal layer is twofold; it can enhance the electrical conductivity of the TRJ by introducing a high density of states accessible for tunnelling [43], and it can reflect additional light away from the bottom cell to the middle cell. In theory the amount of light reaching the middle and bottom junction can then be tuned by varying the metal thickness. Silver was used due to its high reflectivity and conductivity. To give an indication of the optical effects of the layer a series of Ag films deposited on glass substrates is shown in figure 4.14. It was noted that the colour of the films did not resemble that of bulk silver, and thus the optical properties of the films may not be comparable.

Nevertheless a series of c-Si/nc-Si tandem cells with Ag was fabricated. The V_{oc} and FF are shown in figure 4.15**A**. It can be seen that the V_{oc} is reduced slightly in the cells with a thicker Ag layer, but the FF is much higher. The lower V_{oc} could be caused by some loss of passivation when depositing silver on the SHJ surface. The higher FF can be caused by improved electrical performance by the TRJ, as well as by the increasing current mismatch, shown in figure 4.15**B**. It was also noted that all Ag samples had a higher shunt resistance than the reference, and the 4 and 6nm sample also had a lower series resistance, possibly explaining the higher FF for these samples.

What is clear from figure 4.15**B** is that the Ag layer blocks light from reaching the bottom cell, as expected. However, the top cell current does not increase significantly, with a slope of 0.05 ± 0.08 mA/cm^2/nm Ag. This would suggest that the silver film does not effectively reflect light, but rather absorbs it.

Due to the improvement in electrical properties, and the fact that the current loss only affects the bottom cell which is not current limiting, it was deemed useful to implement the silver layers in 3J solar cells as well. The V_{oc} and FF are shown in figure 4.16**A**. As before a small decrease in V_{oc} of about 10mV can be seen with thicker Ag layers, but this decrease is not statistically significant. Interestingly, an initial increase in the FF when adding 2nm Ag is still present, despite these cells moving closer to current matched conditions with increasing Ag thickness.

In figure 4.16**B** the sub cell current densities are plotted, and again no significant increase is found in the middle cell J_{sc}. The bottom cell current density does decrease strongly between the reference sample and the sample with 4nm Ag, and levels off somewhat after.

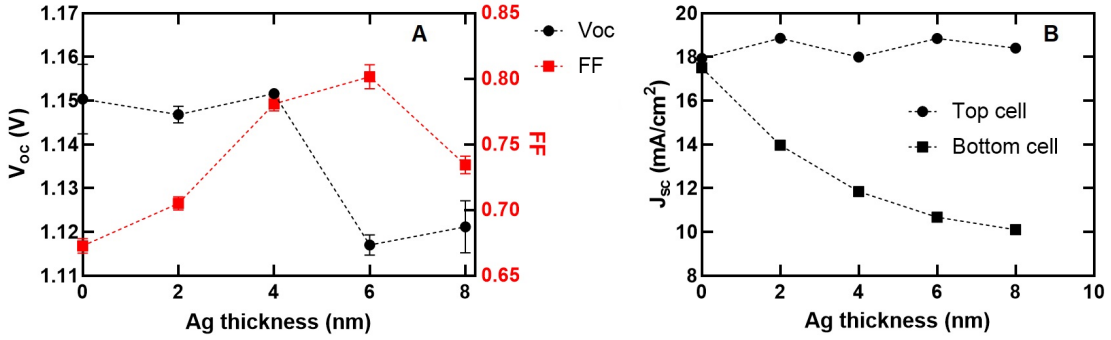

Figure 4.15: V_{oc} and FF (A) and top and bottom cell J_{sc} (B) for c-Si/nc-Si tandem cells with silver in the TRJ.

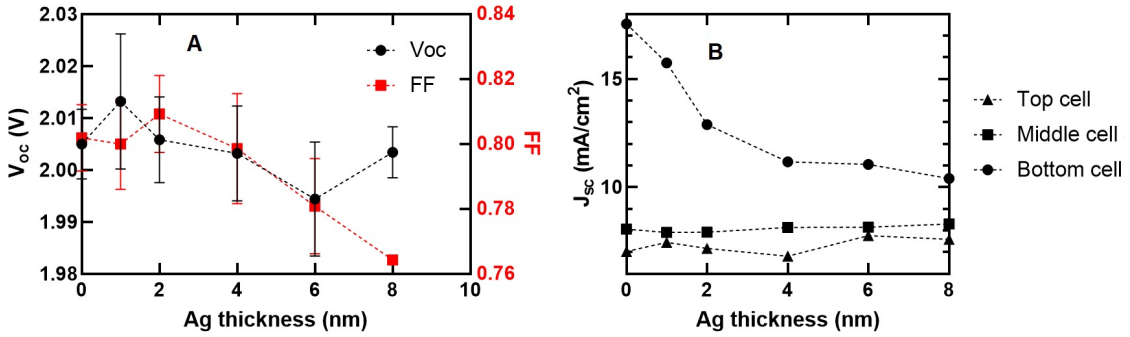

Figure 4.16: V_{oc} and FF (A) and top, middle and bottom cell J_{sc} (B) for c-Si/nc-Si/a-Si 3J cell with silver in TRJ

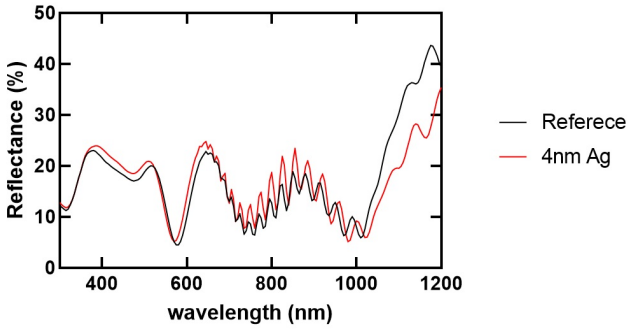

Figure 4.17: Comparison of the reflectance spectra of 3J cell with 4nm Ag deposited in the bottom TRJ with that of a reference 3J cell. The 4nm Ag sample was chosen for comparison as the interference pattern in the reflectance closely matches that of the reference, allowing for an easy visual comparison.

From the results above the conclusion can be drawn that the silver layer does not increase the current density in the nc-Si cell. To assess whether the light is then reflected or absorbed, reflection spectra were measured of the Ag series. The reflectivity spectra of the reference sample and the 4nm Ag sample are shown in figure 4.17.

The reflectivity of the 4nm Ag sample is only slightly higher than that of the reference beyond 700nm, which is the light that can reach the Ag layer. Beyond 1000nm the reflectivity of the 4nm Ag sample is even lower that that of the reference. Furthermore, the reflectivity of the 4nm Ag sample is also slightly higher also for wavelengths below 700nm which do not reach the TRJ. This suggests that the higher reflectivity may not be caused by the silver at all but rather by some difference in the upper layers like the TCO, or even by some dust on the cell surface.

Considering that the bottom cell current density decreases by about 6mA/cm^2 between these samples, this difference must be explained largely by parasitic absorption. When the EQE spectra of these two samples are compared to the 1-R spectra, the magnitude of the parasitic absorption can be seen.

In figure 4.18 the EQE spectra of the 3 sub cells of the reference device and the 4nm Ag device are shown, along with the total utilisation (the sum of the 3 sub cell EQEs), and 1-R. In the range from 700 to 1000nm, the difference between the total EQE and 1-R increases from 4% of incoming light in the reference case, to around 27% for the 4nm Ag sample. Since the electrical performance of these samples in terms of both V_{oc} and FF is fairly similar it is reasonable to assume that most of this additional loss is due to parasitic absorption, and not due to additional recombination.

The low reflectivity of the evaporated Ag film could be explained by the fact that thin silver films grow according to the Volmer-Weber growth model [3]. This growth mechanism involves the formation of nano-scale islands, which grow higher as more material is deposited rather than covering the entire substrate evenly. Additionally, the samples are effectively annealed at 180°C for 30 minutes before the next PEVCD deposition. This can further promote the rearrangement of the Ag into discrete nanoparticles.

To assess if this is the case in the fabricated Ag layers, a set of Ag films was deposited on smooth-textured wafers and characterised using reflectance and transmittance measurements and SEM imaging, shown in figure 4.19.

The reflection/transmission measurements show a peak in the reflection spectra that shifts to longer wavelengths with increasing target thickness, corresponding to the plasmon resonance. Furthermore, in the IR range at wavelengths >1100nm a decrease in both transmission and reflection is seen. This wavelength light has energies below the bandgap energy of silicon, indicating that absorption must be parasitic absorption by the nanoparticles. This may also take place at

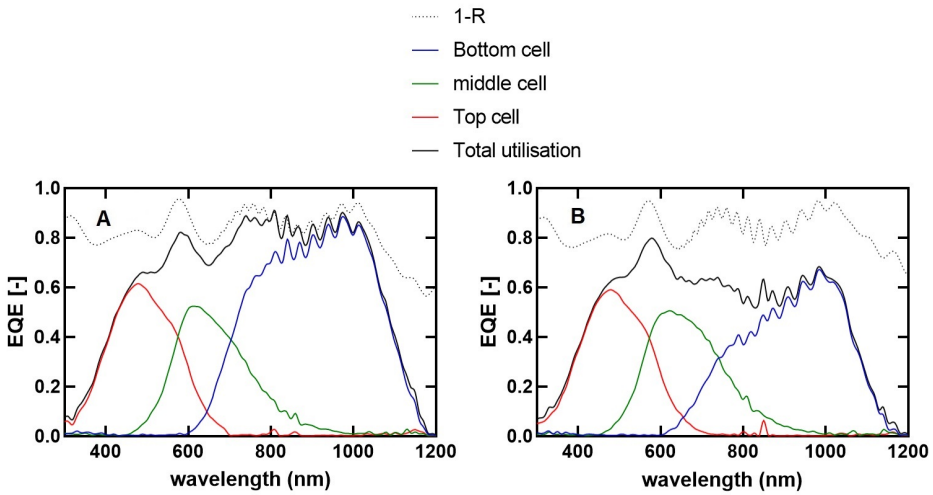

Figure 4.18: The EQE of the top, middle and bottom cell, the total spectral utilisation and the 1-R of a reference 3J cell (A) and a cell with 4nm Ag (B)

shorter wavelengths, but from this measurement this cannot be differentiated from absorption in the wafer.

The SEM images show that, as expected, the silver layers have completely coalesced into nanoparticles. Furthermore, SEM images of a sample with 4nm target thickness showed no visible difference with or without anneal, indicating that the nanoparticles already form during deposition at room temperature.

The particle size was determined from SEM images, and was found to vary from 14±3nm for the 2nm sample to 113±26nm for the 8nm sample.

A nanoparticle array has different optical properties than bulk silver, governed by plasmon resonance [49]. For these particles the absorption and scattering properties depend on the size, shape and embedding medium of the particles [15, 93]. For the small and irregularly shaped particles obtained in this report the absorption cross-section is relatively large compared to the scattering cross-section [82, 93]. This explains the poor performance of these samples in terms of current redistribution and high parasitic absorption.

The nanoparticles can also explain the drop in V_{oc}. As reported earlier [93], the metal nanoparticles form an uneven surface for other layers to grow on. This unevenness can cause cracks and a higher defect density in the overlying nc-Si films, increasing the recombination and lowering the V_{oc}.

Since the growth mechanism of metal films depends mainly on the metal properties, using a different metal like aluminium could give a more interesting result. To test if aluminium would be a good substitute, a 3J cell with 4nm Al was fabricated. Unfortunately the electronic performance of this cell was significantly reduced, with a V_{oc} of only 1.95V and FF of 0.71, compared to the reference cell V_{oc} of 2.03V and FF of 0.82. Furthermore, EQE measurements showed no increase in current generation in the middle cell.

In conclusion, the metal layers used in this research did not provide an effective way of increasing the middle-cell current density significantly. Using a thin (1-2nm) silver layer did however yield a small increase in electrical performance, at the cost of some current density in the bottom cell. If the bottom cell is providing sufficient current, as is the case in this 3J system, this can be a feasible way of obtaining a small performance boost.

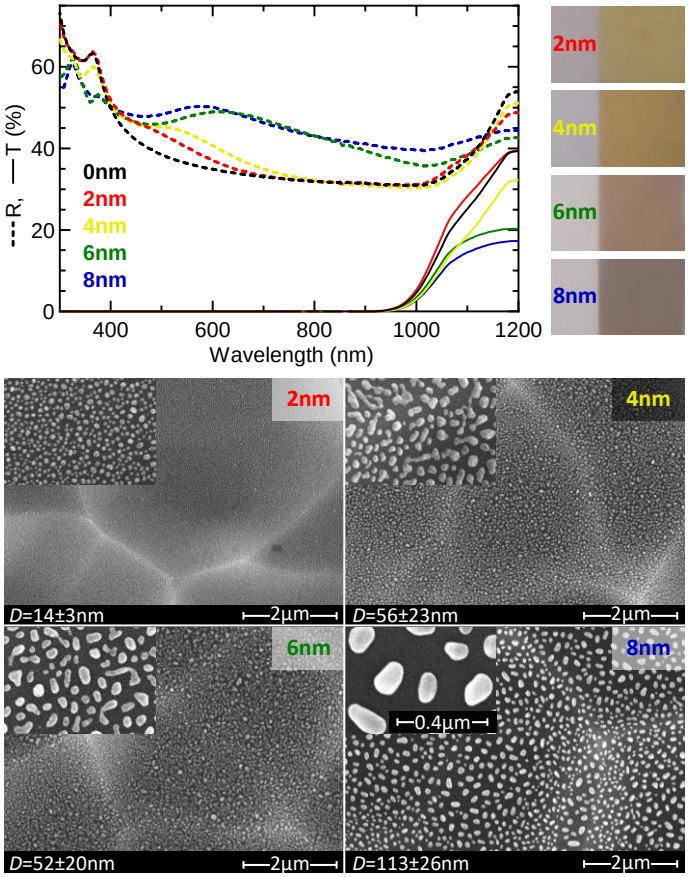

Figure 4.19: Results from the analysis of the Ag films on textured wafers. Reflection and transmission data shows a peak in reflection for the thicker films, corresponding to the plasmon resonance. Adjacently a photo of the films on glass is shown. SEM images below show the increasing particle size upon increasing target thickness of the film.

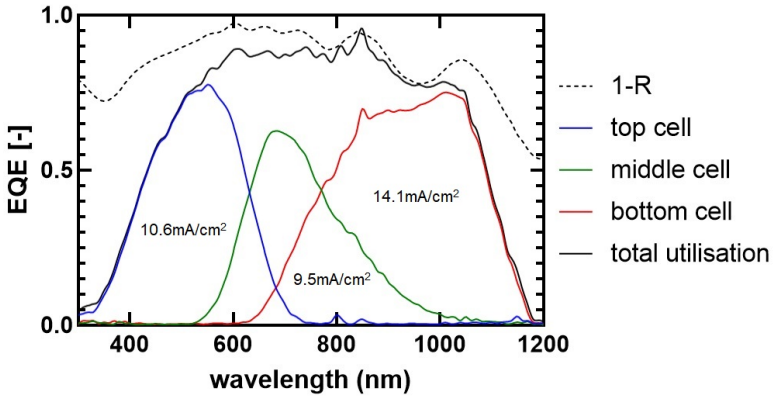

Figure 4.20: The EQE and 1-R spectrum for the top performing cell.

4.5. Top performing device

In the previous sections it was found that increasing the i-nc-Si absorber thickness and the SiO_x thickness were both feasible methods of increasing the middle cell current generation. The next step is to apply both these methods in a device to test what cell efficiencies can be obtained.

A top performing device was fabricated using a 400nm a-Si absorber, a 4.5µm i-nc-Si absorber and a 60nm SiO_x IRL.

The result was a cell with V_{oc} of 1.947V, FF of 0.789 and a J_{sc} of 9.51mA/cm^2, giving an overall efficiency of 14.6%. The EQE spectrum of this device is shown in figure 4.20. The EQE can be seen to have a small peak above 1-R at 850nm, this is caused by an emission peak of xenon lamp used in the setup that is difficult to calibrate.

It is clear that increasing the nc-Si absorber thickness and implementing the thick SiO_x IRL shifted additional current density to the middle cell. Increasing the a-Si thickness furthermore had the consequence of shifting some of this current from the middle to top cell again.

Another observation that can be made is that the overall current utilisation is higher than in the earlier devices, 34.2mA/cm^2 compared to 31.9 - 32.6mA/cm^2 for the 3J nc-Si thickness series. It can be seen in the 1-R graph in figure 4.20 that value of 1-R stays above 0.9 between 510 and 880nm, which is the range where the AM1.5 spectrum has the highest flux density. This can be attributed to the proper front side ITO thickness, resulting in a reflection minimum in the range mentioned above. This efficient light management is an important factor in reaching such high EQE values, and a high total J_{sc}.

In the end the a-Si absorber was thicker than intended, which led to the somewhat exessive current generation in the top cell. It possibly also caused a drop in V_{oc} and FF, for the same reasons as why a drop was observed for these values with increasing nc-Si absorber thickness. Reducing the a-Si thickness should thus be a straightforward way to obtain even higher efficiencies.

5

Results on fabricating PMP devices

Due to time constraints and technical issues, no full PMP devices were fabricated. Instead, the process of fabricating the individual components was tested. Back side metallisation was already optimised in previous work [23]. The front side micro-dot process is reported in section 5.1. The process development for the pore fabrication is reported in section 5.2

5.1. Micro-dot optimisation

While the backside metallisation was already optimised previously [23], the front side metallisation was not yet adequately established. The anode microdot pattern consists of 2 µm diameter circular dots, with a pitch of 8 µm, for a coverage of 4.9%.The existing process yielded poor coverage, with about 50% of the wafer adequately covered.

For this thesis it was attempted to improve the photolithography process to obtain samples with full micro-dot coverage. The micro-dot patterns consists of 2 µm circles of catalyst, arranged in a square matrix. On each wafer there are 32 cells of 1x1cm that are covered with micro-dots. The quality of each tested process was compared in terms of the number of fully covered cells, with 32 being a perfect result.

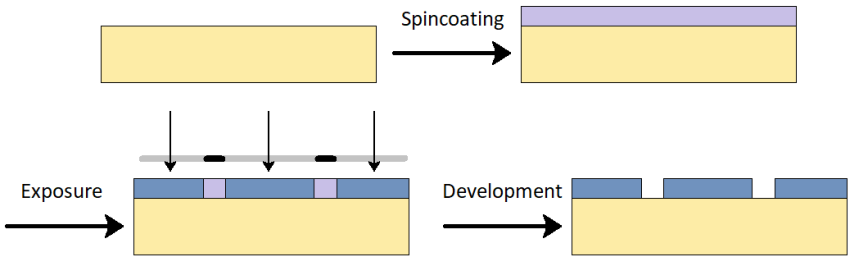

Figure 5.1: A flowchart of the photolithography process for micro-dot processing. For more details on the process, see section 3.2.6.

The first variable tested was the development process. The reference process used the puddle method, in which a single dose of developer is decanted on the wafer with exposed resist. This method was compared to a puddle method where several doses of resist are added to avoid developer saturation and create some stirring effect, and the immersion method, in which the wafer is immersed in developer.

The result was that the reference single dose puddle obtained 17 complete cells, compared to 19 for the immersion and 21 for the multiple dose puddle process. This last process was used

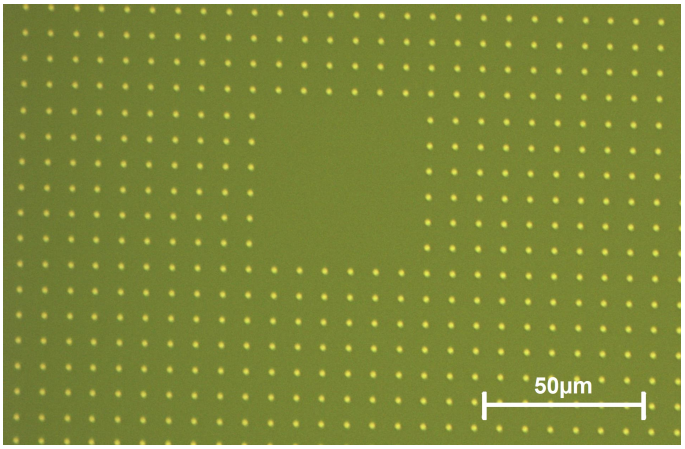

Figure 5.2: optical microscopy image of the microdots. The empty area is where the micropore is intended to be etched (from the back side).

in subsequent steps.

The next variation was to increase the development time from 110 seconds to 130 and 150 seconds. Both of these steps led to a lower coverage of just 10 and 12 cells. Thus the original development time was assumed not to be limiting for the cell coverage.

The 3rd variation implemented was to spincoat a thinner resist layer by increasing the spin-speed. The original resist thickness of 3.5µm was reduced to 2 µm. The exposure energy was scaled accordingly. The result was a coverage of 31 cells, compared to the reference process with 21 cells. This almost fulfils the goal of complete coverage.

The final change that was implemented was optimising the exposure time. Since this process uses a negative resist, *decreasing* the exposure time *increases* the amount of resist that is removed and thus the amount of metal deposited on the wafer. It was found that reducing the exposure time by 25%, reducing the dose from 18mJ/cm^2 to 13.5mJ/cm^2 (i-line dose) yielded all 32 cells covered. Optical microscopy images also showed the microdot size to be as intended, as shown in figure 5.2.

Thus the micro-dot photolithography was successfully optimised, with complete coverage achieved. The optimised process is described in appendix B.

5.2. Developement of a micro-pore fabrication process

This section describes the experimental work done on micro-pore fabrication and testing. This section details the adaptations made to the DRIE process to make the process compatible with the available equipment.

As mentioned before, a DRIE process for micro-pore drilling was developed previously [23]. This process however was not fully compatible with the available equipment due to high reflected power during the passivation step. This high reflected power is caused by poor plasma ignition for the given process conditions.

The ability of a plasma to form depends on various factors, such as the pressure [32], component gasses [53] and applied voltage or power [17, 32]. To adapt the existing process to the available equipment, it is needed to change the process conditions to one where a plasma can form. These changes however will influence the properties of the process (in terms of taper and etch rate for instance), which is undesirable as these are already optimised in the reference process. Thus it was attempted to find suitable conditions as similar as possible to the reference

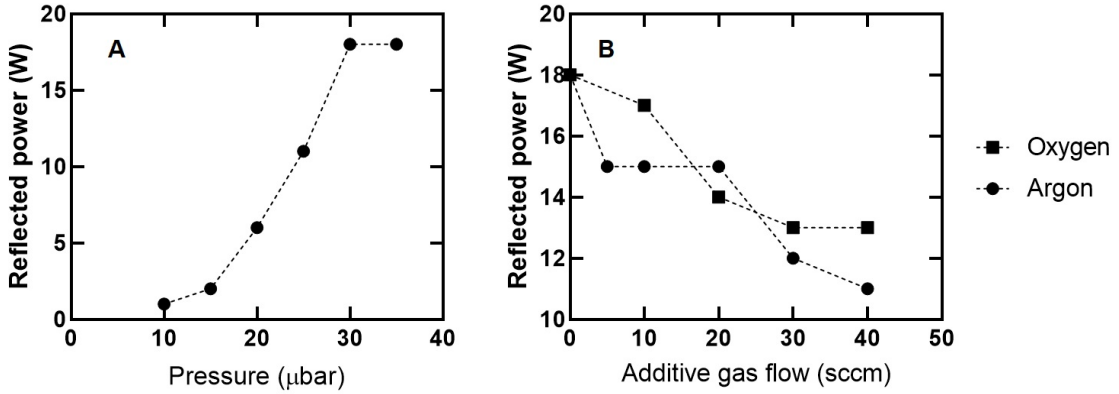

Figure 5.3: Results for testing plasma conditions by varying the passivation step pressure (A) and argon and oxygen gas flow rate (B). This specific DRIE system has a reflected power warning limit set at >7W for 5 seconds, and the process automatically switches off at >10W for 5 seconds. The reference process pressure is 30 μbar. The C_4F_8 gas flow rate during the passivation step is 85sccm.

conditions.

Three different strategies were attempted to establish suitable plasma conditions: changing the operating pressure, adding argon gas to the mixture, and adding oxygen to the mixture. Both of these last two involve gasses that form a plasma more easily than C_4F_8 [53]. The ”quality” of the plasma was quantified by recording the highest reflected power value reached during a 2-minute test process.

The results for the three strategies are shown in figure 5.3. All three methods can be seen to successfully lower the reflected power, with the reduced pressure being the most effective.

It was noticed that the argon flow was somewhat slow to respond, causing initial high reflected power values, until the argon flow started after about 2 seconds. If this were not the case the reflected power would be 2-3W lower for this series.

The method that was chosen for further testing was the reduced pressure. Besides being the most effective method, this method has the advantage of not changing the plasma chemistry, but only the plasma density and thereby the passivation layer deposition rate. This can be compensated for more easily than a change in plasma chemistry due to addition of additive gasses. Furthermore, oxygen was considered less suitable as an oxygen plasma can react with the photoresist mask, leading to faster mask erosion.

With suitable plasma conditions established, the pore process could be tested. Since the conditions during the passivation step have changed, the passivation layer deposition rate may be higher or lower than in the reference process. To assess whether this was the case the process was run for 1 hour using the reference step length. The wafer was then imaged with optical microscopy, which revealed that no etching had taken place, but a layer appeared to have been deposited on the mask, reducing the contrast between mask and silicon (see figure 5.4). This layer is the passivation layer deposited during the passivation step, that is not adequately etched away.

The increased passivation layer deposition rate is due to the better plasma ignition which leads to an increase in decomposition of C_4F_8, and thus a higher passivation layer deposition rate. The passivation layer then becomes so thick that the etching due ions accelerated by the bias voltage cannot remove the layer. To compensate for this a shorter passivation step length is necessary. The passivation step length was subsequently reduced down to 2 seconds, but this did not lead to etching.

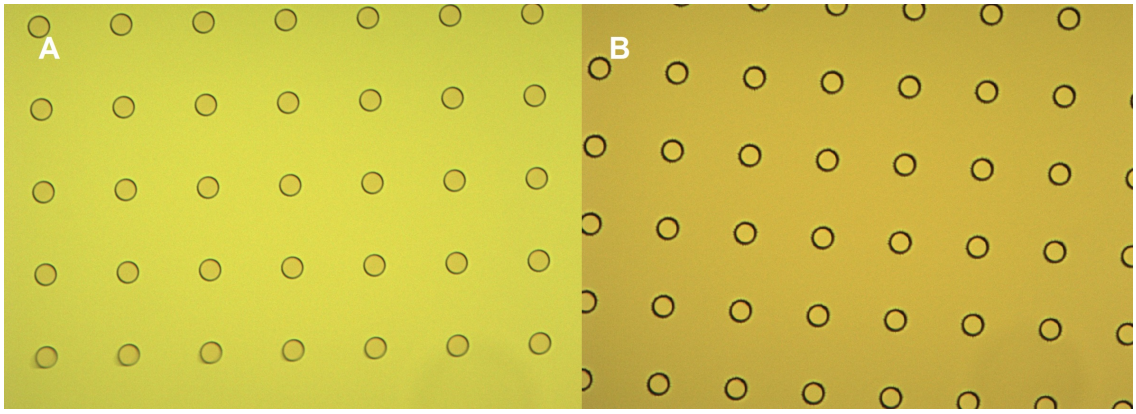

Figure 5.4: The photolithography mask on a silicon wafer after coating, exposure and development (A), showing a colour contrast between the mask and the wafer (in the circles), and after 1 hour of etching using the standard process with reduced passivation step pressure (B), showing a reduced colour contrast.

At this stage technical issues with the etcher, as well as time restrictions prevented further test from being done. If more time was available a next step would be to increase the bias power, or increase the passivation step pressure slightly to again reduce the passivation layer deposition rate. A small further reduction in passivation step length is also possible, although 2 seconds is already approaching the switching time of the machine.

6

Conclusion

This report described the optimisation of a 3J cell based on c-Si/nc-Si/a-Si absorbers. A particular focus is placed on achieving current matching by shifting current from the bottom to the middle cell.

This was done by varying the nc-Si absorber thickness, as well as implementing various IRLs based on SiO_x, transparent conducting oxides and thin metal layers. For each of these methods it was determined if, and how much current can be gained in the middle cell, and how much the electrical performance was affected.

Increasing the nc-Si absorber thickness led to a current gain, but after 5 µm the electrical performance loss out-weights the current gain. The cost of current gain in terms of electronic performance loss between 2.5 and 3.75 µm is about 2% $V_{oc} * FF$ product per mA/cm$_2$, and between 3.75 and 5 µm about 5%.

For the IRLs, only SiO_x was found lead to a current gain, with a gain of 1mA/cm^2 possible at a cost of about 3% of the $V_{oc} * FF$ product per mA/cm^2.

Cells with TCO based IRLs suffered from performance loss due to various reasons, such as (edge-)shunting, parasitic absorption and/or poor carrier collection, and as a result no configuration tested resulted in a middle cell current gain.

Metal based (plasmonic) IRLs failed to increase the current density due to parasitic absorption being dominant over reflection. A small increase in electrical performance was noted for cells with very thin (≤2nm) silver layers, at the cost of bottom cell current density. This could be employed to improve cell performance when the bottom cell is far from current limiting.

Using the two successful methods of current shifting, a cell was fabricated with 60nm SiO_x IRL, with a nc-Si absorber thickness of 4.5 µm, and an a-Si absorber thickness of 400nm, resulting in a cell with a J_{sc} of 9.5mA/cm^2, and V_{oc} of 1.947V and a FF of 0.789, giving an efficiency of 14.6%. To the knowledge of the author this is the highest value obtained for this type of solar cell.

A

Deposition parameters for PECVD, Sputtering and Evaporation

The following section lists the parameters used during the depositions to create the solar cells and PMP devices per deposition category. As most samples only differed by the length of time of a deposition, only the parameters for the reference process are reported. The changes in deposition time are reported in the main text.

Table A.1: Deposition/treatment parameters of PECVD depositions and treatments of a 3J device in AMIGO, with the layers ordered from back to front. "Varied" indicates layers where the thickness was varied in this thesis.

layer/ treatment	dpc #	Temp.[a b] (°C)	SiH_4	H_2	CO_2	B_2H_6	PH_3	Pressure (µbar)	Power (W)	Time (s)	thickness (nm)
				Gas flow (sccm)							
n-side of SHJ											
n-a-Si	2	300	40				11	0.6	4	86	4
i-a-Si	3	273	40					0.7	3	76	10
p-side of SHJ											
i-a-Si	3	273	10	30				1.4	3	75	10
HPT	1	300		200				2.2	9	120	-
i-nc-Si	4	200/170	1.2	120				4	13	120	2-3
p-nc-SiO_x	1	300	0.8	170	2.2	10		2.2	12	560	18
p-nc-Si	1	300	0.8	170		40		2.2	12	238	3-5
HPT	1	300		200				1.2	8	30	-
nc-Si middle cell											
n-nc-Si	2	300	1	120			2	1.5	11	373	5
n-nc-SiO_x	2	300	1	120	1.6		2	1.5	11	varied	varied
n-a-Si	2	300	40				11	0.6	4	168	5-10
HPT	2	300		200				1.2	8	120	-
i-nc-Si	4	200/170	1.2	120				4	40	350	(seed)
i-nc-Si	4	200/170	3.3	120				4	40	varied	varied
i-nc-SiO_x	1	300	0.8	170	1.6			2.2	12	60	2-3
p-nc-SiO_x	1	300	0.8	170	2.2	10		2.2	12	350	12
p-nc-SiO_x	1	300	0.8	170	2.2	50		2.2	12	240	4
HPT	1	300		200				1.2	8	30	-
a-Si top cell											
n-nc-Si	2	300	1	120			2	1.5	11	373	5
n-nc-SiO_x	2	300	1	120	1.6		2	1.5	11	1800	30
n-a-Si	2	300	40				11	0.6	4	168	5-10
HPT	2	300		200				1.2	8	120	-
i-a-Si	3	200	2	200				10	9	varied	varied
i-nc-Si	1	300	0.8	170				2.2	35	120	2-3
p-nc-SiO_x	1	300	0.8	170	1.8	25		2.2	12	550	2-3
p-nc-Si	1	300	0.8	170		20		2.2	35	70	2-3
HPT	1	300		200				1.2	8	30	-

[a] This indicates the set temperature. In situ measurements showed for dpc 1-3 a substrate temperature of $Ts = 0.714 * Tset - 74.95°C$.

[b] The 200/170 for dpc 4 corresponds to the heater and electrode temperature. This corresponds to a substrate temperature of about 165°C

Table A.2: Deposition parameters for sputtering in AMIGO and ZORRO

layer	Machine	dpc #	Temp. (°C)	Power (W)	Pressure (µbar)	Ar (sccm)	1% O_2 (sccm)	Time (s)	Thickness (nm)
AZO	AMIGO	6	200[a]	200	2.6	20	0	100	15
ITO	ZORRO	2	300	60	3.2	20	0	4108	75
IWO	ZORRO	1	25	40	4.0	15	20	3740	75

[a] A set temperature of 200°C in dpc 6 corresponds to substrate temperature of 97°C

Table A.3: Deposition parameters for evaporation in PROVAC and CHA solutions std.

layer	Machine	evaporation method	deposition rate (nm/s)	thickness (nm)
Ag (back contact)	PROVAC	Resistive heating	0.1	300
Cr (back contact)	PROVAC	E-beam	0.1	30
Al (back contact)	PROVAC	E-beam	1	800
Al (front contact)	PROVAC	E-beam	1	500
Pt	CHA	E-beam	0.1	50
Ta	CHA	E-beam	0.1	10

B

Details of the photo-lithography procedure

This section lists the parameters used for photo-lithography.

Table B.1: Parameters for photo-lithography steps

Purpose	DRIE mask	Pt/Ta catalyst mask
Photoresist	Az12xT	Nlof2020
Target thickness (µm)	12	2
Spin speed (time)	200rpm (30s) 950rpm (60s) 4000rpm (2s)	1000rpm (10s) 3240rpm (30s)
Pre-bake time (s)	90	60
Pre-bake temperature (°C)	115	100
Exposure dose (mJ/cm^2)	225 (i-line)	13.5 (i-line)
Post-bake time (s)	-	60
Post bake temperature (°C)	-	115
Developer	AZ400K (1:2 DI water)	MF322
Development time (s)	240	110

C

Parameters of reference DRIE process

This chapter lists the parameters of the reference DRIE process used for pore fabrication.

Table C.1: Parameters for the reference DRIE process

Parameter	During Etch step	During passivation step
Source power	600	
Bias power	15	
Chuck temperature (°C)	20	
Source-sample distance (mm)	120	
Time (s)	8	5
Chamber pressure (µbar)	15	30
SF_6 flow (sccm)	150	0
C_4F_8 flow (sccm)	0	85
O_2 flow (sccm)	13	0

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