12.1 A 74fs-Jitter, –59dBc-Spur Fractional-N DPLL Using a Supply-Resilient Time-Amplifying Dual-Ramp DTC

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Abstract

This work presents a fractional-N digital PLL that employs a supply-resilient, time-amplifying dual-ramp DTC, which offers 8× time amplification and maintains its linearity under supply variations. Additionally, a DTC code-randomization technique is included to enhance the DTC gain-calibration accuracy and convergence speed at near-integer channels. The PLL achieves <-59dBc fractional spurs and 74fs rms jitter for a stable supply and 88.5fs rms jitter for a 29mV$_{rms}$, 10MHz-bandwidth supply noise.

Exploiting narrow-input-range phase detectors (PDs), such as bang-bang (BBPD) [1-3] or subsampling [4,5] architectures, improves the jitter–power FoM of PLLs by enhancing the PD linearity and gain, thereby suppressing noise from subsequent loop components. To implement this in fractional-N PLLs, a digital-to-time converter (DTC) [6-12] is typically used to cancel the ΔΣ-modulator (DSM) quantization error before the PD, with its gain K_{DTC} estimated by correlating the PD output to the DSM error sequence using a least-mean-square (LMS) calibration technique [6,7]. However, for near-integer channels, PLL dynamics strongly attenuate errors originated from inaccurate K_{DTC} estimation at the PD output, prolonging calibration, reducing K_{DTC} calibration accuracy, and elevating fractional spurs [13]. Frequency-control-word (FCW) subtractive dithering [14] and cascaded-fractional-divider [15] techniques have been proposed to mitigate this issue; however, the former requires an additional calibration to compensate for digitally controlled oscillator (DCO) duty-cycle error, while the latter requires an extra full-range DTC, thereby degrading the PLL jitter.

The second issue is the sensitivity of prior-art variable-slope [6,16], constant-slope (CS) [17,18], and inverse-constant-slope (ICS) [1,14] DTC architectures to dynamic in-band supply voltage variations, which can couple to the PD from other circuits in real-life applications. Given the low-jitter performance of modern DTCs and PDs, PLL bandwidths (BWs) are typically in the MHz range to optimize the PLL jitter-power FoM. Consequently, DTC and PD distortions caused by supply variations in the 10kHz-to-1MHz range cannot be compensated either by the PLL, as they lie within the loop BW, or by K_{DTC} gain calibration, which is too slow to track fast supply changes, leading to significant spur degradation.

This work presents a fractional-N digital PLL (DPLL) that achieves <–59dBc fractional spurs and 74fs rms jitter at near-integer channels by introducing: 1) a time-amplifying dual-ramp (TADR) DTC that offers 8× embedded time amplification to suppress the PD noise and maintains its linearity under in-band supply variations, and 2) a DTC code-randomization technique that enhances the K_{DTC} calibration accuracy and convergence speed at near-integer channels with minimal hardware overhead and jitter penalty.

Figures 12.1.1 and 12.1.2 illustrate the evolution and operating principles of the proposed TADR DTC. As a baseline, the resistor-based ICS DTC from [1] is adopted due to its excellent jitter and linearity performance under stable-supply conditions. The circuit consists of a capacitor (C) precharged to the supply voltage (V_{DD}) before each phase-detection cycle, along with two resistors, R and R/M, that discharge C in two steps.

In the first step, C discharges with a time constant $\tau_{in} = RC$, triggered by an input pulse (IN_P) of width mT_{DCO}, where T_{DCO} is the DCO period and m is a programmable integer determined from the accumulated DSM quantization time error (T_Q). In the second step, the divider rising edge (t_{div}) acts as the DTC input, further discharging C with a time constant $\tau_o = RC/M$. When the capacitor voltage (V_C) falls below the comparator threshold (V_{th}), the comparator generates the DTC output edge (t_o). The phase comparison is then performed between the reference edge (t_{ref}) and t_o using a time-to-digital converter (TDC). In this scheme, the DTC delay (T_{DTC}) equals $\tau_o\ln(V_{DD}/V_{th}) + t_d - (\tau_o/\tau_{in})mT_{DCO}$, where t_d is the comparator delay. The term mT_{DCO}/M cancels the deterministic T_Q and remains largely insensitive to PVT, since T_{DCO} is precisely stabilized by the PLL. Meanwhile, a Type-II PLL adjusts t_{div} to compensate for T_{DTC} time offset: $\tau_o\ln(V_{DD}/V_{th})+t_d$. However, because this offset is strongly V_{DD} dependent, in-band supply fluctuations directly modulate T_{DTC}, producing spurs that the PLL cannot suppress.

To mitigate this, a dual-ramp DTC is proposed, comprising two ICS DTCs—main and auxiliary—as shown in Fig. 12.1.1b. The main branch retains the original ICS structure with $\tau_{in,M} = RC$ and launches an output rising edge: $t_{O,M} = t_{div} + \tau_o\ln(V_{DD}/V_{th}) + t_d - mT_{DCO}/M$. In the auxiliary branch, the first discharge having time constant $\tau_{in,A} = RC/M$, is triggered by an input pulse (IN_{PD}) spanning the divider and reference rising edges, yielding a pulse width of $t_{div}–t_{ref} = T_Q+t_n$, where t_n denotes the random jitter. Next, t_{div} initiates the discharge of the auxiliary capacitor with the same RC/M time constant, after which the auxiliary comparator generates an output edge: $t_{O,A} = t_{div} + \tau_o\ln(V_{DD}/V_{th}) + t_d – (T_Q+t_n)$. The phase error is now encoded in the time difference between the main and auxiliary outputs. Since the output discharging step is common to both branches, the terms $\tau_o\ln(V_{DD}/V_{th}) + t_d$ are naturally canceled, suppressing supply-induced variations and resulting in-band spurs. Furthermore, since $\tau_o/\tau_{in,M} = 1/M$ and $\tau_o/\tau_{in,A} = 1$, the condition $m=MT_Q/T_{DCO}$ is preserved, leaving only t_n at the PD output.

Although the dual-ramp DTC reduces supply sensitivity, adding the auxiliary branch doubles the power consumption (P_{DC}) and KT/C-induced jitter power ($\sigma^2_{j,c}$), degrading the jitter-power FoM ($\sigma^2_{j,c}P_{DC}$) by 4×. However, since $\sigma_{j,c}$ scales with the DTC maximum required delay, the PLL locking point is adjusted so that T_Q can assume both positive and negative polarity [20]. This effectively halves the maximum delay, reducing $\sigma^2_{j,c}$ by 4× and restoring the FoM. As shown in Fig. 12.1.2a, the additional negative time shifts are achieved by introducing extra discharge branches and swapping IN_P and IN_{PD} based on T_Q polarity. With the maximum delay halved, all time constants are scaled by reducing the resistors by 2×, while capacitors remain unchanged to preserve DTC jitter.

After achieving supply immunity and preserving the DTC FoM, an implicit time-amplification gain of M is incorporated to suppress TDC quantization noise. As shown in Fig. 12.1.2b, this is achieved by increasing $\tau_o/\tau_{in,M}$ and $\tau_o/\tau_{in,A}$ by a factor of M. This modification increases the maximum delay of both the main and auxiliary branches by M times, raising the KT/C-induced jitter power at the TADR-DTC output by M^2. However, due to the time-amplification factor M, the input-referred KT/C-induced jitter power remains unchanged. Meanwhile, the slopes of the main and auxiliary ramps during the output discharging phase decrease by M, which increases the contribution of comparator noise to the output jitter power by M^2 [13]. Nevertheless, when referred back to the input, this contribution remains unchanged, realizing time amplification with no jitter penalty.

The proposed TADR DTC is integrated into a DPLL, as shown in Fig. 12.1.3a. The phase-frequency detector (PFD) [19] extracts the IN_{PD} pulse, and the T_{DCO}-Scaler [14] provides programmability of the IN_P pulse width. The phase error is extracted using a differential vernier TDC [13], whose multi-bit output signal improves the LMS convergence speed compared to a BBPD [10], and its resolution, determined by difference of delay elements, exhibits resilience to supply variations. The TADR DTC offers a dynamic range of $\pm T_{DCO}$ to cover the quantization error introduced by the MASH 1–1 DSM controlling the PLL division ratio. However, its coarse resolution of T_{DCO}/M (≈16ps at f_{DCO}≈8GHz with M=8) is insufficient to suppress the DSM quantization noise below the PLL in-band noise floor. Therefore, a fine variable-slope DTC [6] is inserted in the reference path, covering the T_{DCO}/M range with an ≈125fs resolution. Because the fine DTC has a narrow dynamic range, its nonlinearity has a negligible impact on the PLL spur performance. Its gain, $K_{DTC,f}$, however, is PVT sensitive and must be continuously tracked by a background LMS calibration loop. Monte Carlo simulations in Fig. 12.1.3b show that device mismatch in the TADR DTC causes $\tau_o/\tau_{in,M}$ and $\tau_o/\tau_{in,A}$ to deviate from their nominal values. This results in distinct gain errors for positive and negative T_Q cancellations, since different circuit branches are active in each case. Two additional LMS calibration loops estimate these gain errors.

For the near-integer channels, the PLL dynamics strongly attenuate errors originated from an inaccurate K_{DTC} estimation at the PD output, degrading the LMS loop accuracy and convergence speed. To address this, a pseudo-random 0–1 sequence (R_n) is added to the TADR-DTC codeword in each reference cycle ($1/f_{ref}$), while a scaled version, R_n/M, is subtracted from the fine DTC quantization error residue ($Q_{n,f}$). This shifts the phase error components to $0.5f_{ref}$ and enables accurate and fast calibration even for the near-integer channels, as shown in Fig. 12.1.3c. Figure 12.1.3d shows the DTC code sequences before and after dithering. When R_n=1, the TADR DTC generates an additional delay of T_{DCO}/M, and the fine DTC produces the corresponding negative delay, leaving overall T_Q cancellation unaffected. The TADR DTC range thus increases by 6.25% with a negligible linearity impact, while the fine DTC range doubles from T_{DCO}/M to $2T_{DCO}/M$ yet remains sufficiently narrow to maintain its linearity within acceptable limits. Consequently, compared to prior art [14,15], the proposed technique achieves a high-accuracy calibration but with a minimal hardware overhead, while increasing the total DTC range by only 12.5%.

The DPLL, fabricated in 28nm CMOS, occupies 0.2mm^2 of active area (Fig.12.1.7) and consumes 23mW. It operates from 8 to 9.7GHz with f_{ref}=125MHz. Figure 12.1.4 shows the measured output spectra and phase-noise (PN) performance under different conditions.

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With dithering disabled and $FCW_{FRAC} = 2^{-11}$, the worst spur of -42.4dBc appears at the 8th harmonic of the fractional frequency, indicating inaccuracies in $K_{DTC,f}$ calibration. Enabling dithering improves the LMS convergence, reducing the worst-case fractional spur to -59dBc. Similar suppression is observed across other in-band fractional-N channels, with spur levels consistently <-59dBc. The rms jitter is 72fs with spurs and 68.2fs without.

Supply resilience was evaluated (Fig. 12.1.5) by injecting both wideband noise and single-tone ripple into the TADR DTC, PFDs, T_{DCO} scaler, and TDC supply. With a $29mV_{rms}$ wideband noise (10MHz BW), the rms jitter increases only to 88.5fs, confirming the robustness of the TADR DTC. The injected wideband noise also elevates the PLL phase noise even outside the loop bandwidth, as the DTC noise—due to absence of additional IIR filtering—is comparable to the DCO contribution in this region. A $20mV_{PP}$ ripple at 100kHz produces a -58.9dBc spur, corresponding to a DTC supply pushing factor, K_{sup} = 4ps/V. Compared with prior-art PLLs (Fig. 12.1.6), the jitter, spur, and FoM of this work remain highly competitive, while also demonstrating notable resilience to supply variations.

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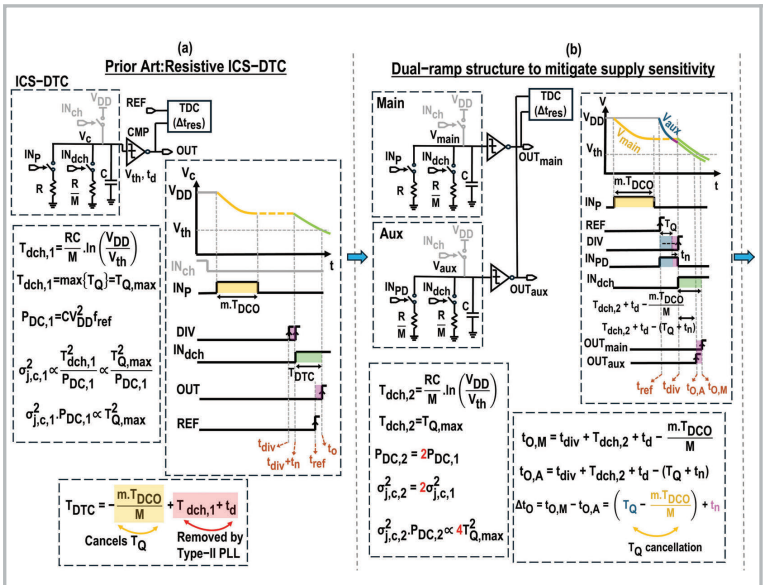


Figure 12.1.1: (a) Operating principle and timing diagram of the prior resistor-based inverse-constant-slope DTC [1]; (b) the dual-ramp DTC.

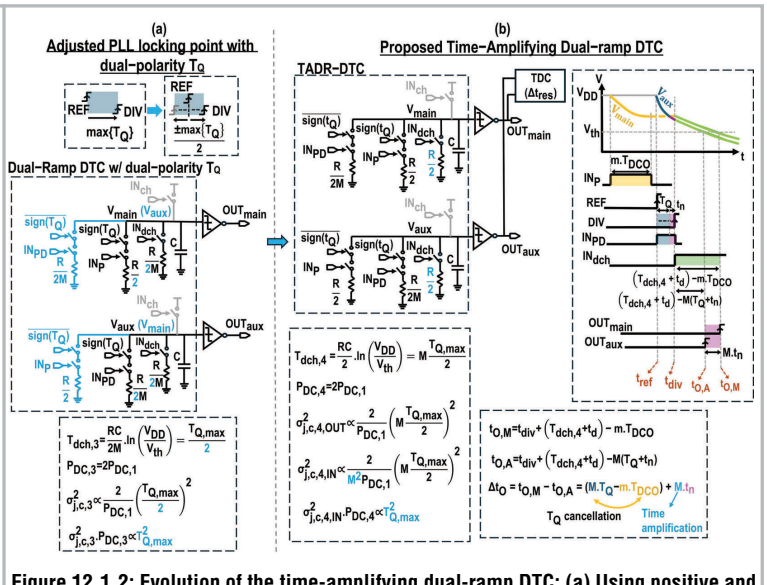


Figure 12.1.2: Evolution of the time-amplifying dual-ramp DTC: (a) Using positive and negative time shifts to reduce DTC noise; (b) employing time amplification to suppress the TDC quantization noise.

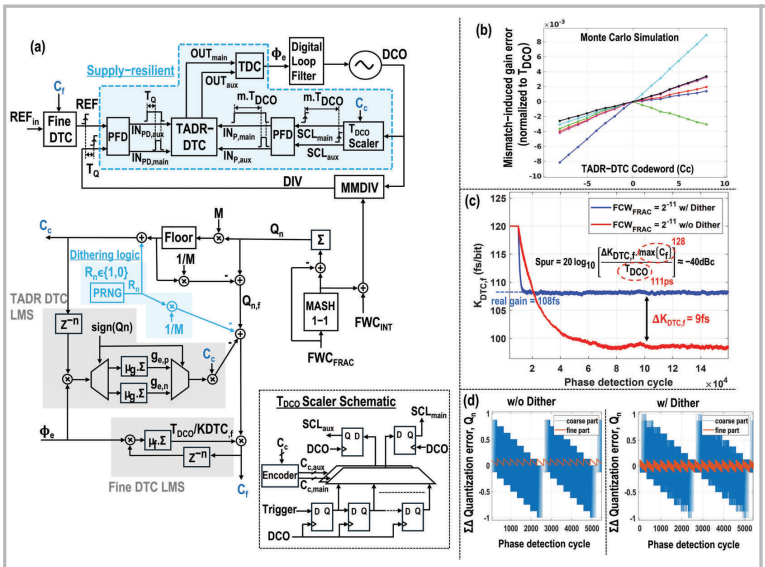


Figure 12.1.3: (a) Simplified block diagram of the proposed digital PLL; (b) simulated TADR-DTC gain error; (c) LMS loop accuracy and convergence; (d) TADR and fine-DTC ranges with and without the randomization technique.

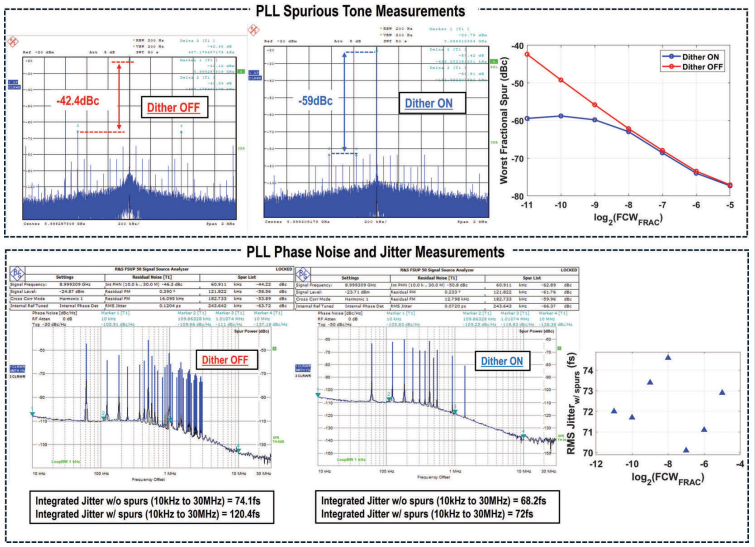


Figure 12.1.4: Measured fractional spurs and phase noise for $FCW_{FRAC} = 2^{-11}$ and worst fractional-spur level and rms jitter across FCW_{FRAC}.

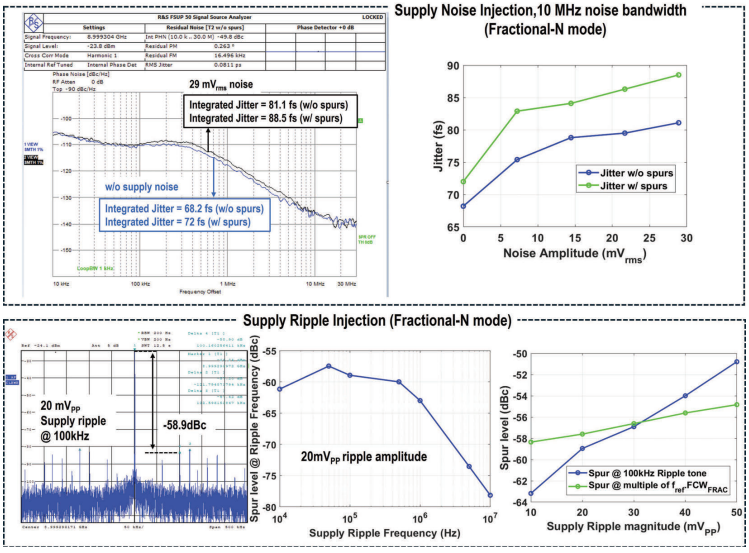
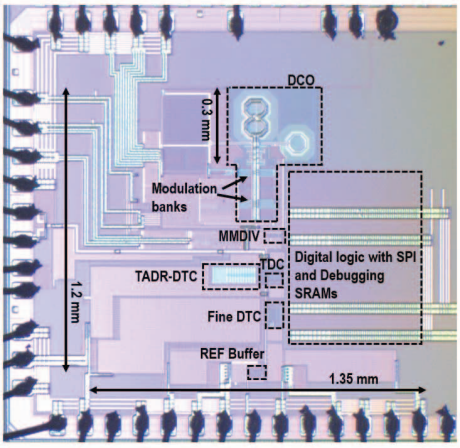


Figure 12.1.5: Measurement results showing robustness of the TADR DTC against wideband supply noise (top) and single-tone ripple injection (bottom).

	Supply-Resilient PLLs			Regular PLLs				
	This Work	Chen [23] JSSC'22	Rossoni [21] VLSI'25	Salvi [1] JSSC'25	Chae [20] ISSCC'25	Xu [15] ISSCC'24	Dartizio [14] ISSCC'23	Gao [22] ISSCC'22
PLL Architecture	DPLL	DPLL	DPLL	BBPLL	QEC-BBPD	DPLL	BBPLL	DPLL
Supply Disturbance Cancellation Method	TADR DTC	Ripple Pattern Estim. & Canc.	PGRO w/ FSL	-	-	-	-	-
Output Freq (GHz)	8 to 9.7	4.47 to 5.14	9 to 10.25	8.75 to 10.25	10 to 11.5	6.5 to 7.5	9.25 to 10.5	2.56 to 4.1
Reference Freq (MHz)	125	50	250	125	100	100	250	40
Supply Ripple Amplitude (mV_{pp})	20	50	3	-	-	-	-	-
Ripple Output Spur# (dBc)	-58.9	-48.9##	-50.2	-	-	-	-	-
Supply Noise Amplitude (mV_{rms})	29	-	2.5	-	-	-	-	-
Jitter w/ Supply Noise (fs)	88.5	-	81	-	-	-	-	-
Jitter w/o supply noise (fs)	72	422	72.2	66.7	65	143.7	76.7	182
K_{sup} (ps/V)	4	9.1	70.8	-	-	-	-	-
Power Dissipation (mW)	22.65	3.25	19.5	16.7	14.4	8.89	17.2	3.48
FoM (dB)	-249.3	-242.4	-249.9	-251.3	-252.2	-247.4	-249.9	-249.4
FoM_N (dB)	-267.9	-262.2	-265.6	-270	-272.2	-265.9	-265.6	-267.7
Fractional Spur (dBc)	-59	-55	-57.9	-63.8	-62.8	-62.1	-71.9	-59
DTC Calibration Type	Gain	Gain (DAC) + DCO Duty cycle	-	Gain + DCO Duty cycle	Polynomial DPD	Gain	Gain + DCO Duty cycle	LUT DPD
DTC Calibration Time (us)	40	64	-	-	262	-	-	-
Active area (mm^2)	0.2	0.39	0.27	0.21	0.12	0.23	0.33	0.31
CMOS Process (nm)	28	40	28	28	40	65	28	40

FoM = $10.\log_{10}((Jitter_{w/\ spurs}/1s)^2.(Power/1mW))$ $FoM_N = FoM + 10.\log_{10}(f_{ref}/f_{osc})$ #Normalized to 9GHz ##Known Ripple Frequency

Figure 12.1.6: Performance summary and comparison with prior art.



Power and Area Breakdown

Block	Power (mW)	Area (mm^2)
REF Buffer	0.25	0.002
Fine DTC	0.3	0.004
TADR-DTC	2.7	0.02
TDC	0.2	0.002
Digital	1.2	0.03#
MMDIV	6	0.002
DCO	12	0.14
Total	**22.65**	**0.2**

#Excluding debugging SRAMs

Figure 12.1.7: Die micrograph; breakdown of power consumption and area.

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