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Design, modelling and evaluation of a GaN based motor drive for a solar car

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***Abstract*—In recent years, electrical vehicle (EV) starts showing its unique advantages that the conventional combustion vehicles do not have. Together with the increasing interests on EV, the motor drive with higher efficiency and lighter weight also becomes more attractive. A promising solution is to apply the wide band gap (WBG) components including gallium nitride (GaN) and silicon carbide (SiC) in the motor drive. Thus, the performance of the GaN, SiC and Si based motor drive in this application are compared. Besides, as the current maximum current rating of the GaN and SiC MOSFET is limited and insufficient to satisfy the large phase current in the acceleration and braking process, the inverter topology that adds the parallel MOSFETs in one position is considered.**

To reduce the time and cost for the development, this paper proposes the modelling of the motor drive, with which the voltage and current stress, power loss, thermal and electromagnetic performance can all be evaluated. The modelling to be introduced consists of the 1-D power loss, simplified thermal modelling of the motor drive and the 3-D modelling of the electromagnetic performance, detailed thermal performance of the motor drive. In the 3-D modelling, to make the heat transfer simulation closer to the realistic, computational fluid dynamic (CFD) is used to evaluated the heat transfer coefficient on the surface with forced air-cooling.

I. Introduction

With the development of the novel GaN and SiC power semiconductors, they are available for wider motor drives with higher power ratings [1]. There is a possibility of applying the novel semiconductor into the motor drive for the solar car. Nevertheless, the efficiency improvement of applying the novel semiconductor into the motor drive for the solar car is not clear thereby evaluated. In order to increase the current capability of the inverter to meet the demand, adding the parallel MOSFET in one position is considered. Beside the maximum current rating of the inverter, the thermal performance of the inverter is crucial for the feasibility of the design as well.

For the thermal performance evaluation, there are the approach using thermal circuit model [2], [3] and the approach using the finite element method (FEM) [4]. For the first approach, it needs small computational cost but less accuracy compared with the latter one. Besides, it fails to show the temperature distribution on the power stage which is important for such a inverter using the parallel MOSFET in one position.

To thoroughly evaluate the performance of the motor drive but not sacrifice the computational time and cost. The modelling of the motor drive starts with the 1-D modelling which uses Cauer thermal circuit model. After the preliminary design using the 1-D models, a detailed 3-D multi-physical model that couples the CFD, electromagnetic and thermal performance of the inverter is established. The current sharing between the parallel MOSFETs, temperature distribution and maximum junction temperature of the MOSFET belonging to the power stage with three different layouts are compared in the 3-D simulation.

II. Overview on the Methodology

A design flow chart of the project is shown in the figure 1. As it is shown, it starts with the 1-D power loss and thermal performance modelling. The established models are used as the design tools for the preliminary design.

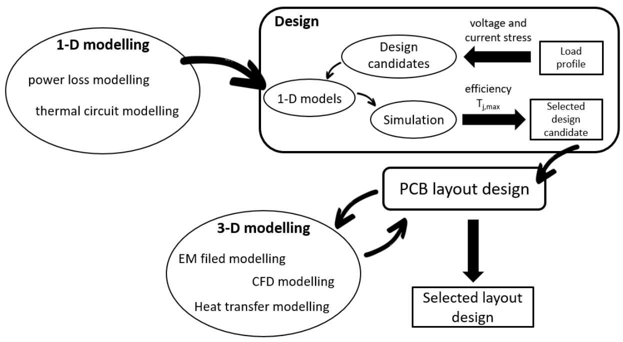

Fig. 1. Design flow chart of the project

For the preliminary design, it starts with the load profile analysis which contains the voltage and current stress of the motor drive under certain driving condition of the solar car. Based on the maximum voltage and current stress, several design candidates that use different MOSFETs, inverter topology and switching frequency are proposed. Their performance are evaluated by simulation using 1-D models. The one with the

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highest efficiency and acceptable operating junction temperature of the MOSFET is selected for an initial PCB layout design.

After the initial design of the PCB layout, the 3-D modelling proceeds. The electromagnetic and thermal performance of the motor drive are evaluated by 3-D simulation. Based on the evaluation, the layout design is improved. This process happens iteratively until the satisfying layout is obtained.

III. 1-D Modelling and Preliminary Design

A. Electro-thermal modelling

The main power loss of the inverter is the sum of the conduction and switching losses of the MOSFETs. Thereby, the modelling of the inverter loss is given as

$$\begin{aligned} P_{loss,inv} &= \sum_{i=a,b,c} P_{loss,pha} = \sum_{i=a,b,c} \\ N \frac{1}{T_0} &(2 \int_0^{T_0} P_{cond,i}(t)dt + \sum_{j=1}^{m} P_{sw,i}(jT_s)T_s) \end{aligned} \tag{1}$$

where i is the phase number, $P_{loss,pha}$ is the power loss of one phase, T_0 is the fundamental period, T_s is the switching period, N is the number of the parallel MOSFETs and $m = \frac{T_0}{T_s}$. The conduction loss can be estimated based on the datasheet. However, to precisely estimate the switching loss, a method [5] using double pulse test with SPICE model is used. The influence of the parasitic elements on the switching loss is considered by using the empirical value of the parasitic elements based on an estimation on the PCB routing.

To evaluate the junction temperature of the MOSFETs when the inverter is operating, the Cauer-model [2], [6] together with the estimated MOSFET power loss is sufficient. However, for the efficiency evaluation which is based on a long term load profile, the small time step need to be removed to reduce simulation time. Thereby, a 3-D look-up table of the inverter loss $P_{loss,inv}(i_{phase(amp)}, v_{dc}, T_j)$ based on the detailed modelling is established, where $i_{phase(amp)}$ is the amplitude of the phase current, v_{dc} is bus voltage and T_j is the MOSFET junction temperature. Given that the car cruises in most of the time, the junction temperature of the MOSFETs is assumed to be constant in the efficiency evaluation.

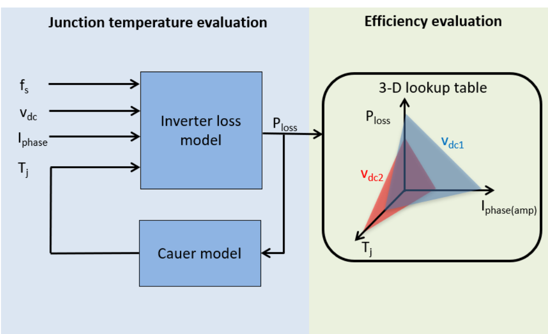

Fig. 2. Modelling of the inverter loss for the junction temperature and efficiency evaluation

B. Load profile analysis

The load profile is analyzed for evaluating the voltage and current stress on the motor drive. Based on a data recorded during a 5-day running of the solar car, some general information that indicates the working status of the motor drive is obtained and shown in the table I.

TABLE I
LOAD PROFILE ANALYSIS RESULTS: GENERAL INFORMATION

Maximum phase current (A)	DC link voltage (V)	Cruising speed (km/h)
117	147-126	80-90

Phase current(RMS) at the cruising speed (A)	Power rating at the cruising speed (W)
10-20	800-900

For over 80% time in the 5-day (8 hours per day) racing, the solar car cruises at a constant speed with a phase current lower than 20A. The large phase current occurs only in the accelerating and braking processes whose proportion is rather limited in the 5 days.

C. Preliminary design candidates

Based on the maximum voltage and current rating requirements obtained from the load profile analysis, several MOSFET candidates are selected. As the current GaN and SiC MOSFET can hardly satisfy the required maximum current rating, topologies with double, triple and quadruple parallel MOSFET in one position are considered. As for the switching frequency, 20kHz and 50kHz are selected for comparison.

In the table II, the design candidates are listed. For simplicity, the topology with double parallel MOSFET is called D whereas the one with triple and quadruple parallel MOSFET is called T and Q respectively. Besides, the maximum current rating I_D (when $T_j = 100°C$) and voltage rating (V_{ds}) are shown as well.

TABLE II
PRELIMINARY DESIGN CANDIDATES

MOSFET				f_s(kHz)		topology		
Part No.	type	I_D (A)	V_{ds} (V)					
GS66516B	GaN	47	650	20	50	D	T	Q
SCT3022AL	SiC	65	650					
C2M0025120D	SiC	60	1200					
SCTWA50N120	SiC	50	1200					
IPT60R028G7	Si	47	600					

D. Evaluation on the efficiency and temperature

Based on the 1-D modelling of the motor drive, the efficiency and MOSFET junction temperature of the preliminary design candidates are evaluated. To evaluate the junction temperature $T_{j,cruise}$ when the car cruises, a 3000-second load profile, in which the car cruises and the phase current stays stable, is used. As for the maximum junction temperature $T_{j,max}$ evaluation, a 600-second load profile, in which the car accelerates and brakes several times and large surge current occurs, is selected. The evaluation results are shown in the figure 3 and figure 4. For simplicity, the abbreviations used in the figures are listed below:

- 20k_d: $f_s = 20kHz$ and dual parallel MOSFET topology
- 20k_t: $f_s = 20kHz$ and triple parallel MOSFET topology
- 20k_q: $f_s = 20kHz$ and quadruple parallel MOSFET topology
- 50k_d: $f_s = 50kHz$ and dual parallel MOSFET topology
- 50k_t: $f_s = 50kHz$ and triple parallel MOSFET topology
- 50k_q: $f_s = 50kHz$ and quadruple parallel MOSFET topology

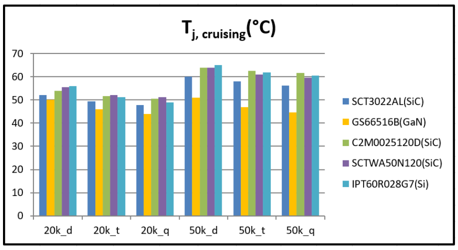

Fig. 3. Statistics of the $T_{j,cruising}$ for all the design candidates

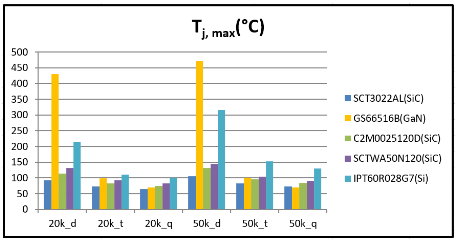

Fig. 4. Statistics of the $T_{j,max}$ for all the design candidates

Apparently, some of the design candidates are not feasible because of the too high maximum junction temperature. Assuming the junction temperature stays constantly at the $T_{j,cruise}$, the efficiency of the design candidates in one day (8 hours) operation are predicted and shown in the figure 5.

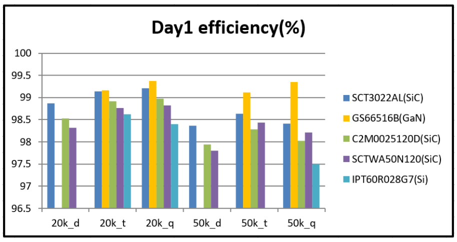

Fig. 5. Statistics of the efficiency for all the design candidates

Among all the design candidates, the GaN based 20k_q motor drive has the highest efficiency. However, 50k_q is selected because a higher switching frequency probably brings a higher efficiency of the whole power-train which includes the motor losses. Thereby, the GaN based 50k_q motor drive is selected. However, it should be noticed that the switching loss of the GaN MOSFET is probably underestimated as the parasitic inductance is assumed to be very small.

IV. Layout Design and 3-D Modelling

Based on the preliminary design, the PCB layout is designed. For such a inverter with four parallel GaN MOSFETs and 50kHz switching frequency, the layout of the gate driver and power stage needs to be compact and symmetrical to reduce the influence of the parasitic inductance. In a reference design [7], the gate driver and power stage are separated on two different PCB to achieve the goal.

Given that the power stage which consists of a half bridge circuit for one phase is the part where most of heat is generated, only the 3-D modelling of the power stage are of interest. For the 3-D simulation, COMSOL Multiphysics is selected as the simulator. In the design, three different layouts are proposed. Their current and temperature distribution and temperature swing are compared by simulation.

A. Layout design candidates

Based on the preliminary design in the section III, the three different layouts proposed are shown in the figure 6, figure 7 and figure 8. The type-one layout is modified from the reference design [7]. Apparently, there is enough space for the gate driver to make the gate driver loop same for the each parallel MOSFETs. However, the power loop is not same for each one of them.

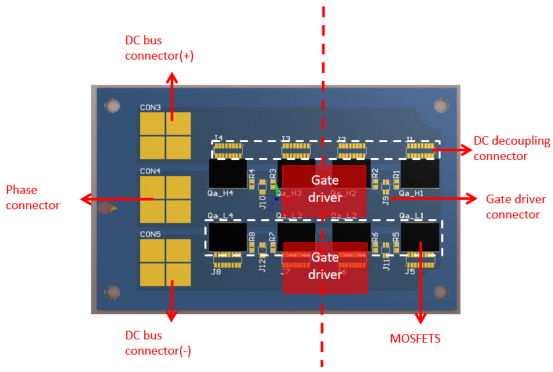

Fig. 6. Type-one layout

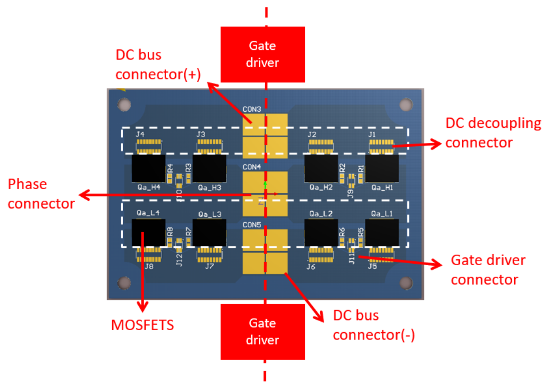

Fig. 7. Type-two layout

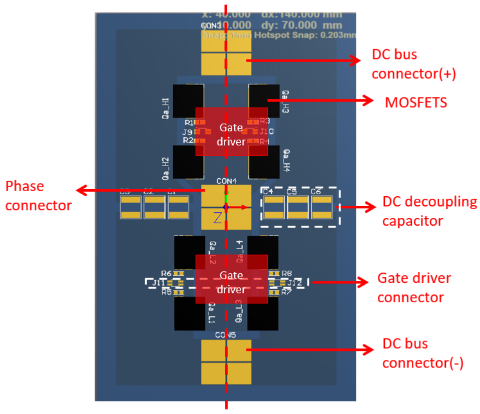

Fig. 8. Type-three layout

In the type-two layout, both the gate driver loop and the power loop are closer to be same for the parallel MOSFETs. However, the gate driver loop is longer in the type-two layout than in the type-one layout. In the type-three layout, the distance of the gate driver loop is reduced but the symmetry of the layout is not sacrificed.

B. 3-D modelling method

In the figure 9, the structure of the coupled multi-physics in the 3-D modelling is shown. Basically, the 3-D multi-physical modelling consists of:

- 3-D modelling of the electromagnetic field coupled with the electric circuit (EM+electric circuit). The simulation outputs the current distribution on the power stages and the current sharing between the parallel MOSFETs.
- 3-D modelling of the computational fluid dynamic coupled with the heat transfer (CFD+heat transfer). The simulation outputs the heat transfer coefficient $h(v)$.
- 3-D stationary heat transfer modelling. The simulation outputs the temperature distribution on the power stage when the car is cruising.
- 3-D time dependent heat transfer modelling. The simulation outputs the temperature distribution on the power stage under the large surge current condition. The 223-second load profile used for this simulation is selected because the peak junction temperature appears during this period in the simulation with 1-D models.

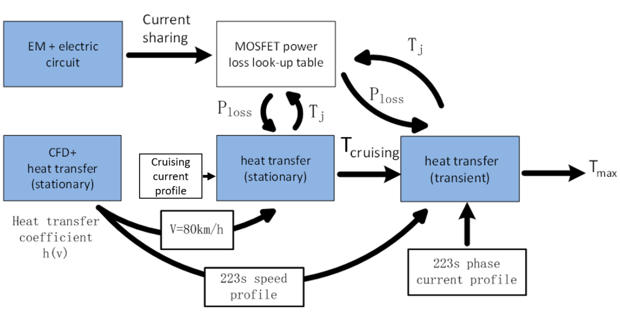

Fig. 9. Structure of the coupled multi-physics in the 3-D modelling

In the figure 10, the geometry of the 3-D modelling is illustrated. For a better cooling of the power stage, the insulated metal substrate (IMS) PCB is used. To reduce the computational cost, the motor drive is partitioned and only the performance of the power stage in the middle (i.e. power stage B in the figure 10) is evaluated because of its worst cooling condition.

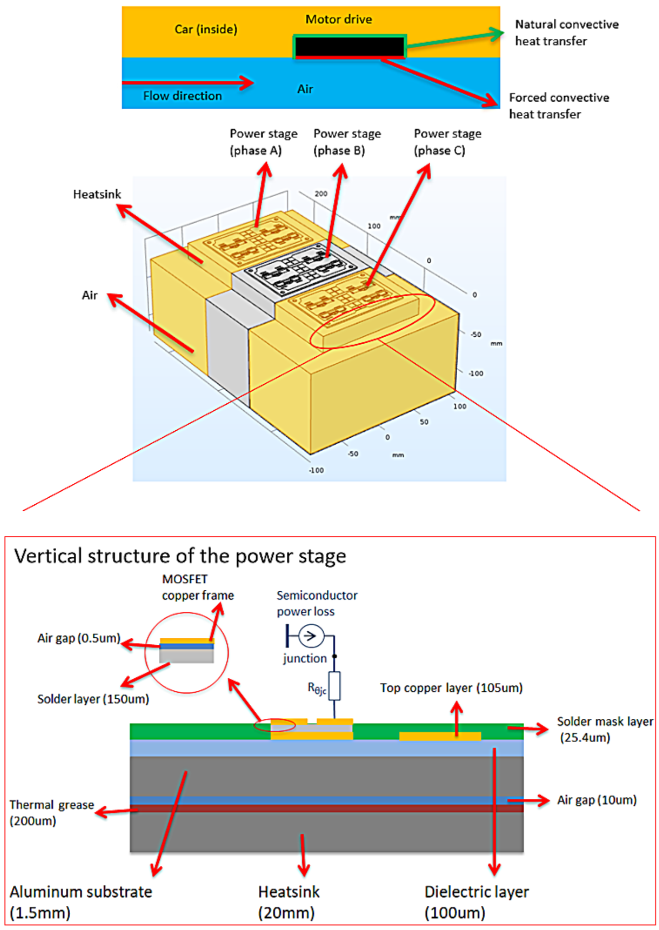

Fig. 10. Geometrical shape of the 3D modelling

For the numerical modelling of the fluid domain, the $k-\epsilon$ turbulence model is selected because of its good convergence rate and low memory requirements [8]. The heat source is assumed to be only the MOSFETs, which is modelled in the subsection III-A. With the current profile, assumption $V_{dc} = 150V$ and current sharing information from the 'EM+electric circuit' simulation, the power loss of a single MOSFET can be evaluated. Then, given the heat transfer coefficient $h(v)$ obtained from the 'CFD+heat transfer' simulation and the current and speed profile, the stationary and time dependent heat transfer can be simulated.

C. Simulation results

The simulation results consist of three parts that are current distribution and sharing, stationary temperature distribution and time dependent junction temperature of the MOSFET.

The current distribution when the low-side MOSFETs (Q5-Q8) are turned on and the phase current amplitude equals 20A is shown in the figure 11, figure 12 and figure 13. The current sharing between the parallel MOSFETs is listed in the table III. Apparently, the current sharing in the type-two and type-three power stage is more balanced.

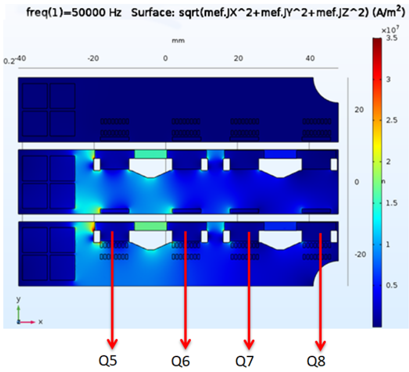

Fig. 11. Current distribution in the type-one power stage

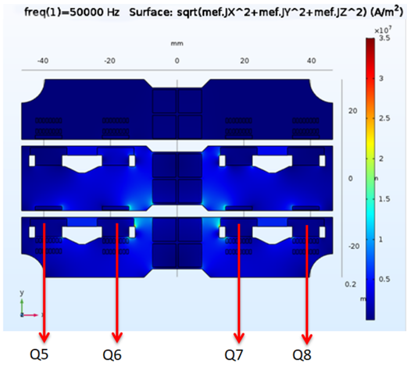

Fig. 12. Current distribution in the type-two power stage

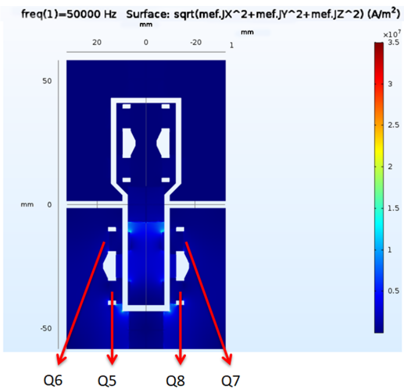

Fig. 13. Current distribution in the type-three power stage

In the figure 14, figure 15 and figure 16, the temperature distribution in the cruising situation are shown. The resultant temperature is assumed to be the initial temperature in the time dependent heat transfer study.

TABLE III
CURRENT SHARING OF THE 4 PARALLEL MOSFETS IN THE THREE TYPES OF POWER STAGES

	Current (A)			
	Q5	Q6	Q7	Q8
Type 1	5.22	5.01	4.92	4.85
Type 2	4.97	5.03	5.03	4.97
Type 3	4.98	5.02	5.02	4.98

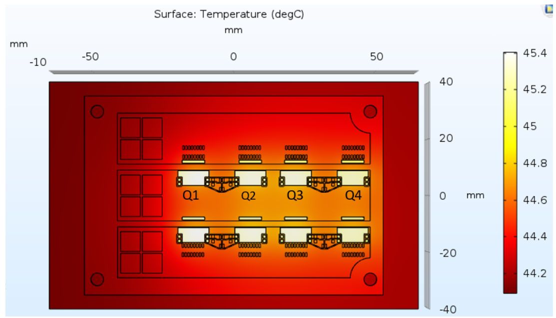

Fig. 14. Temperature distribution in the type-one power stage

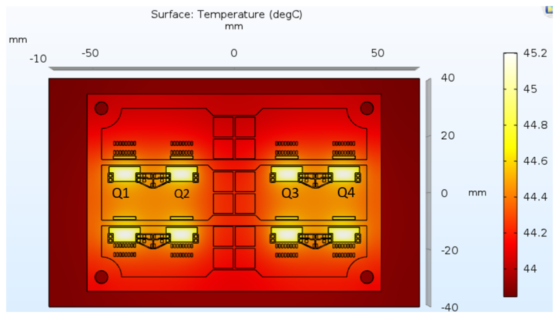

Fig. 15. Temperature distribution in the type-two power stage

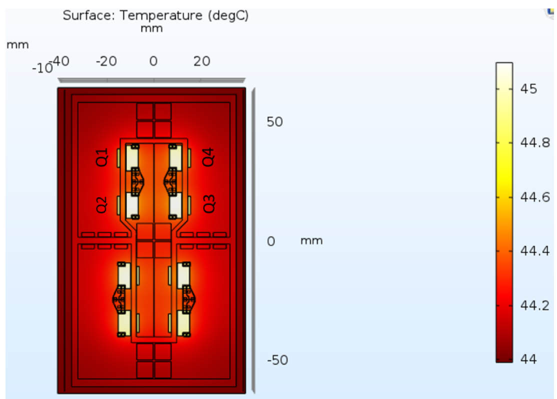

Fig. 16. Temperature distribution in the type-three power stage

The 233-second phase current (RMS) profile, which is used for the transient thermal simulation, is shown in the figure 17. In the figure 18, the junction temperature of the 4 parallel MOSFETs on the type-one power stage in the 233-second simulation is shown. Similarly, the figure 19 and the figure 20 show the temperature of the MOSFET on the type-two and the type-three power stage respectively.

According to the simulation result, it is obvious that the type-two and type-three power stage have a more evenly distributed temperature and current. It shows that a more symmetrical layout design is helpful for a more balanced current and temperature distribution. Besides, the GaN MOSFET has serious thermal run-away problem. A closer placement of the MOSFET will significantly increase the junction temperature in high current condition, which is shown in the result that type-two power stage has a smaller temperature swing.

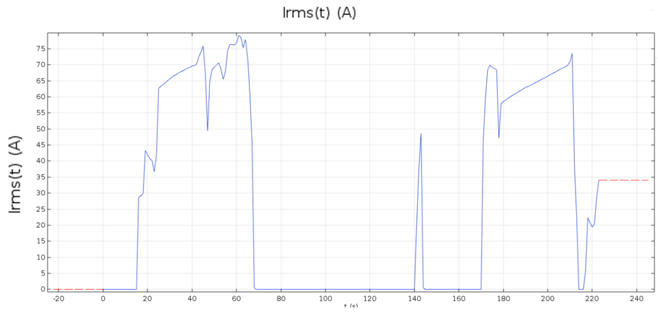

Fig. 17. 233-second I_{phase} profile

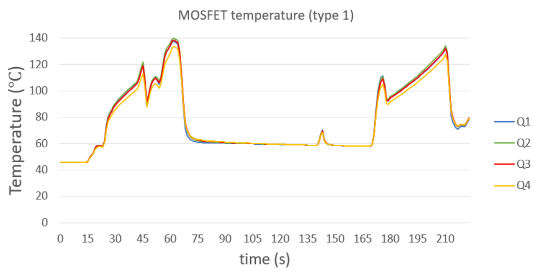

Fig. 18. MOSFET temperature of the type-one power stage

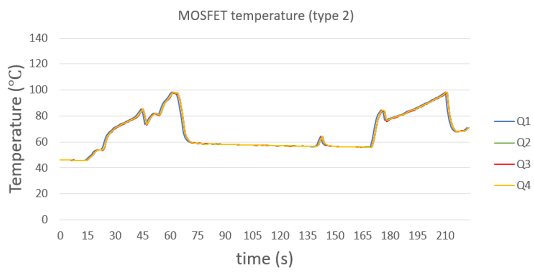

Fig. 19. MOSFET temperature of the type-two power stage

V. Conclusion

In this paper, a systematic approach for the design of the GaN-based 4-parallel MOSFET motor drive is introduced. 1-D models for the efficiency and junction temperature evaluation and 3-D multi-physical models for the temperature and current distribution evaluation of the motor drive are presented. From the evaluation based on the 1-D models, it shows that the GaN based motor drive has lower loss compared with the

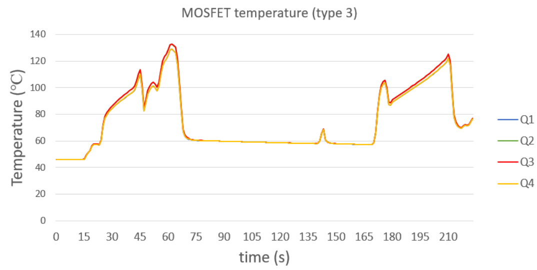

Fig. 20. MOSFET temperature of the type-three power stage

SiC and Si based motor drive. Besides, it also shows that using parallel MOSFET in one position can increase the efficiency within some extend. For the maximum efficiency, there is an optimized number of the parallel MOSFET in one position in this application. Then, based on the selected preliminary design, three kinds of layout of the power stage are proposed. The MOSFET temperature behaviour under the cruising and large surge current condition are evaluated by the simulation based on the 3-D multi-physical models. To make the temperature distribution more even, the layout should be made more symmetrical. Besides, the GaN MOSFET has serious thermal run-away problem. Thereby, enough space between the GaN MOSFETs is needed to decrease the thermal run-away risk induced by the mutual heating between each other.

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