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DOI
10.23919/EPE20ECCEEurope43536.2020.9215838

Publication date
2020

Document Version
Accepted author manuscript

Published in
2020 22nd European Conference on Power Electronics and Applications (EPE'20 ECCE Europe)

Model Predictive Control for the Reduction of DC-link Current Ripple in Two-level Three-phase Voltage Source Inverters

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Keywords

≪MPC (Model-based Predictive Control)≫, ≪Modulation strategy≫, ≪Pulse Width Modulation (PWM)≫, ≪Voltage Source Converter (VSC)≫.

Abstract

In the applications of three-phase two-level voltage source inverters (VSIs) relatively large energy storage capacitors are used to absorb the high DC-link current ripples mainly caused by the circulating reactive power, the switched AC phase current flowing to the DC-link, and other dynamic and/or asymmetric operating conditions. Especially for electrolytic capacitor technology the typically high current stress and consequent losses is known to limit the power electronics lifetime, thus the design and selection of this component is critical for the whole system. To alleviate this problem, a new model predictive control (MPC) cost function which enables DC-link capacitor current ripple reduction is proposed in this paper. Based on the DC-link current mathematical model and the available VSI switching states, the future DC current ripple can be predicted, and then the optimized space vectors that best tracks the sinusoidal output current and minimizes the DC-link current ripple are chosen. Compared with conventional DC-link capacitor current reduction methods, the proposed approach has the advantage to incorporate an outstanding fast current control dynamics as well as being of relatively simple implementation because there is no need to adjust the switching signals or space vectors in the modulation as function of operational conditions of the system. Simulation and experimental results are presented verifying the effectiveness of the proposed MPC method.

Introduction

Three-phase two-level voltage source inverters (VSIs) have been widely used in industrial applications such as in AC motor drives, traction of electric vehicles, battery energy storage systems, grid-tied photovoltaic systems, and other renewable energy generations [1]-[3]. In these applications, a large energy buffer comprising of several DC electrolytic capacitors are usually applied to stabilize the DC voltage, while guaranteeing a minimal acceptable lifetime of the VSIs. The latter occurs because the DC-link capacitor is subject to a relatively high current stress caused by the switching action of the impressed AC current, the circulating reactive power, and dynamic or asymmetric operation of the system. Therefore, the consequent operational losses and rise of temperature across the DC-link electrolytic capacitors are

Table I: Switching States ($x = a, b, c$)

Switching State (S_x)	Converter output (v_{xo})	Gate signal (S_{x+}, S_{x-})
1	$V_{\mathrm{dc}}/2$	(1,0)
0	$-V_{\mathrm{dc}}/2$	(0,1)

often judged as the defining factor for the lifetime of the power electronic system. Therefore, the derivation of a feasible control technique which can reduce the current ripple and minimize the size of DC-link capacitors in VSIs has been of research interest in both industry and academia [5]-[10].

Prior efforts have been made in existing literature to implement pulse width modulation (PWM) techniques which are able to reduce the DC-link current ripple in VSIs. In [5], a discontinuous pulse width modulation (DPWM) method to reduce the DC-link capacitor current is applied into a back-to-back converter. The DPWM technique is also known to advantageously reduce the semiconductor switching losses. Two different control strategies to reduce the DC-link capacitor harmonic current in two-level back-to-back converter are studied in [6, 7]. A new PWM strategy has been proposed in [8], which not only reduces the current ripple across the DC-link capacitor but also preserves the power quality delivered to the load. Based on the strategy in [8], an extended double carrier PWM strategy is proposed in [9], where the current ripple in the DC-link capacitor can be effectively reduced for all operational modulation index. For the sake of simplifying the implementation, a scalar PWM method with the ability to reduce the DC-link current ripple and common-mode voltage is studied in [10].

Most of the aforementioned methods which are effective on reducing the DC-link capacitor current stress in the VSI need to adjust the conventional space vector sequence or switching signals based on the load operation condition. Therefore, the robust implementation of these techniques are difficult in practice. Recently, with the advancement in digital signal processor technology [11, 12], a model predictive control (MPC) with finite switching states has been introduced as a method to control the VSI load current [13]. Additionally, MPC can achieve other interesting objectives in the control of power converters, all in an unified and simple optimization strategy, for example, common-mode voltage suppression [14], reduction of the equivalent switching frequency and improvement on the balance in the partial DC-link voltage of neutral-point-clamped converters [15]. Herein, a quality function is evaluated and optimized based on predictions from an analytical model of the system by selection of the most advantageous available switching vector. It is noted that so far very limited publications exist using the MPC strategy in VSI to reduce the DC-link capacitor current ripple. Therefore, without sacrificing the performance of fast AC current dynamic response, a flexible MPC method with the advantage of DC-link current ripple reduction is of interest in three-phase two-level VSIs.

To fill this gap, this paper proposes a finite-control-set model predictive control (FCS-MPC) method which works toward the reduction of the DC-link capacitor current ripple of three-phase three-wire VSIs. The proposed method is not only effective on the reduction of capacitor current stress, which enables size and cost minimization of this electric component, but it can also maintain the intrinsic MPC feature of fast AC current dynamic response. Since there are only eight feasible switching states in the two-level three-phase VSI, the proposed approach can be simply implemented in practice. The paper is divided as follows. Firstly, the analytical model of the three-phase two-level VSI is derived. Thereafter, the working principle of the proposed MPC strategy is illustrated. Finally a PLECS based simulation and experiments on a VSI hardware setup implementing the proposed MPC are used to verify its effectiveness on reducing DC capacitor current stress.

II. Modeling of the Three-phase Three-wire Two-level VSI

A three-phase three-wire two-level VSI circuit is shown in Fig. 1. The basic converter is composed of 6 active switches, two series-connected DC capacitors C_1 and C_2, and a Y-connected three-phase $R-L$ load. Note that in Fig. 1, i_a, i_b and i_c represent the output currents of the inverter, while v_a, v_b and v_c are

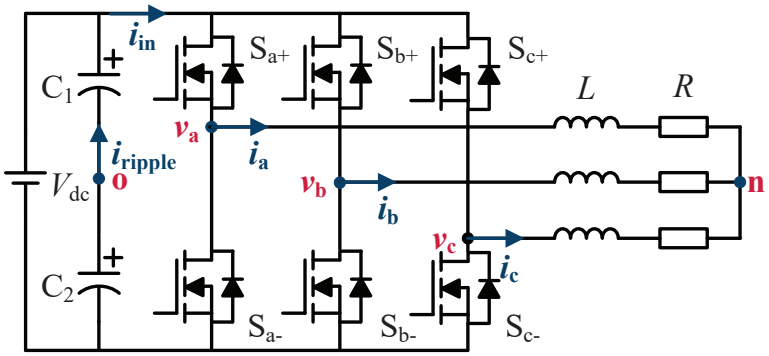


Fig. 1: Circuit schematic of the three-phase three-wire two-level VSI.

the converter terminal phase voltages; i_{in} is the inverter input current; i_{ripple} is the DC-link current whose RMS value is of paramount importance to the decide the size and the lifespan of the DC-link capacitor; L refers to the value of the AC inductor; and R is the value of the series resistor modeling the active power of the load. The switching states and the corresponding converter terminal voltages are summarized in Table I. Assuming that each capacitor voltage is equal to half of the DC-link voltage, then these three switching states ($x = a, b, c$) generate an output terminal voltage of $v_{xo} \in \{-V_{\text{dc}}/2, V_{\text{dc}}/2\}$, i.e. voltage of terminal $x = a, b, c$ with respect to the terminal o as shown in Fig. 1.

According to the current flow direction in Fig. 1, the output current dynamics can be represented in the α-β coordinates as given in the following:

$$\begin{cases} L\frac{\mathrm{d}i_\alpha}{\mathrm{d}t} = v_\alpha - Ri_\alpha \\ L\frac{\mathrm{d}i_\beta}{\mathrm{d}t} = v_\beta - Ri_\beta. \end{cases} \tag{1}$$

In order to be implemented in a digital controller, the model of the inverter must be defined in a discrete-time manner [13]. The derivative of the AC line currents and the capacitor voltages in the continuous-time form can be approximated based on the forward Euler approximation with the analog-to-digital conversion sampling period of T_s as:

$$\begin{cases} \frac{\mathrm{d}i_\alpha}{\mathrm{d}t} \approx \frac{i_\alpha(k+1)-i_\alpha(k)}{T_s} \\ \frac{\mathrm{d}i_\beta}{\mathrm{d}t} \approx \frac{i_\beta(k+1)-i_\beta(k)}{T_s}. \end{cases} \tag{2}$$

Accordingly, the expression (1) can be re-written in the discrete form as:

$$\begin{cases} i_\alpha(k+1) = \frac{L-RT_s}{L} i_\alpha(k) + \frac{T_s}{L} v_\alpha(k) \\ i_\beta(k+1) = \frac{L-RT_s}{L} i_\beta(k) + \frac{T_s}{L} v_\beta(k). \end{cases} \tag{3}$$

III. Working Principle of The Proposed FCS-MPC Method

A. FCS-MPC

The feedback current control based on the FCS-MPC technique is known for utilizing only a finite number of possible switching states that can be generated by the power converter during the optimization routines. This method can predict well the behavior of the modeled system variables and specific performance indexes for each analyzed switching state [12]. Herein, the reasoning is that each current $i_{\alpha,\beta}$ prediction is evaluated with respect to its references $i^*_{\alpha,\beta}$ in a cost function, and the switching state S_a, S_b, and S_c, that generates the minimum deviation (or error) value is selected to be applied in the next sampling period.

The block diagram of this control strategy for the three-phase three-wire two-level VSI is shown in Fig. 2. The main control objective is the regulation of the AC line currents in the α-β coordinates, i.e. $i_{\alpha,\beta}$. The

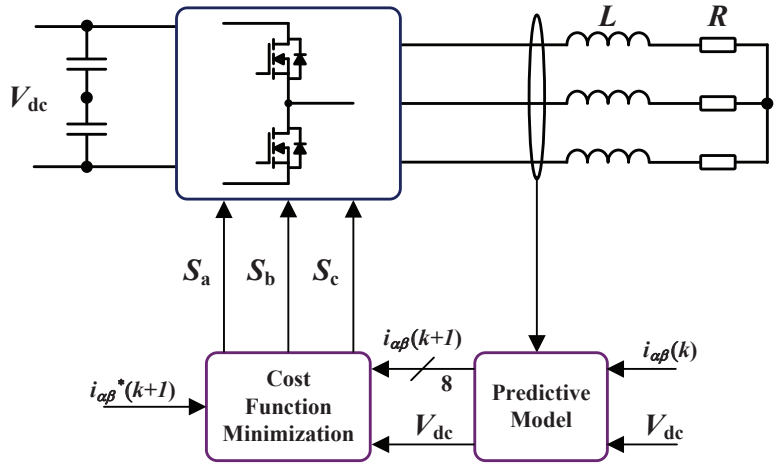


Fig. 2: Block diagram of a conventional FCS-MPC.

FCS-MPC method uses the discrete-models of the system developed in Section II, i.e. the AC currents analytical models, and all the 8 possible switching states to predict the future behavior of the controlled variables. The defined cost function G objective is to minimize the quadratic error between the predicted load currents $i_{\alpha\beta}(k+1)$ and their references $i^*_{\alpha\beta}(k+1)$, as represented:

$$G = |i^*_\alpha(k+1) - i_\alpha(k+1)|^2 + |i^*_\beta(k+1) - i_\beta(k+1)|^2 \tag{4}$$

The implementation steps of traditional FCS-MPC algorithm for two-level three-phase VSIs are summarized as follows [13]:

1. Measure the load currents at the kth sampling period.
2. Predict the load currents for the next (k+1)th sampling instant for all the possible switching states based on the discrete time model.
3. Evaluate the proper cost function based on the control objectives.
4. Apply the designed cost function for all the feasible switching states and select the switching state minimizing the cost function.
5. Apply the new switching state with minimum value of cost function.

B. Analysis of DC-link Current

The inverter input current i_{in} can be expressed as function of the switching state S_x and phase output current i_x as expressed in (5), which means the i_{in} is the sum of all three-phase currents through the switches. $S_x = 1$ means the switch is turned ON, while $S_x = 0$ defines that the switch is turned OFF. As shown in Fig. 1, the DC-link current ripple i_{ripple} can be derived in (6), where i_{avg} can be regarded as the average DC input current.

$$i_{\text{in}} = S_a i_a + S_b i_b + S_c i_c \tag{5}$$

$$i_{\text{ripple}} = i_{\text{in}} - i_{\text{avg}} \tag{6}$$

Taking space vector PWM (SVPWM) method as an example, the variation of inverter input current during a switching period is given in Fig. 3. The difference between the average and the instantaneous values is equal to the current flowing to the DC-link capacitors. A large fluctuation of i_{in} around its average value i_{avg} will generate a large current ripple i_{ripple} flowing into the capacitor. Therefore, one of the solutions to reduce the fluctuation of i_{in} during each switching period is to select the optimized vectors which minimizes i_{ripple}.

C. Delay Compensation

To compensate the unavoidable computation time delays in digital controllers, two steps of prediction are implemented. In practice, utilizing the values of $S_\alpha(k)$ and $S_\beta(k)$ calculated during the kth sampling

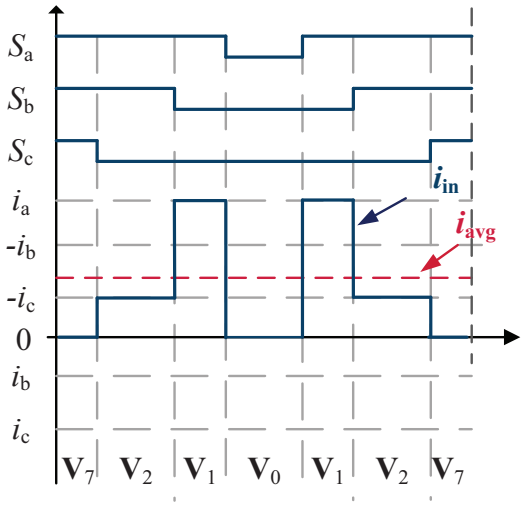


Fig. 3: Variation of inverter input current during a switching period for SVPWM.

interval and applied to the converter while computing their new values, the first prediction step just updates $i_\alpha(k)$ and $i_\beta(k)$ using the previously calculated converter state in (3). This update does not represent an extension in the prediction horizon, the cost function is not calculated, and the predictive optimization problem is not solved at the time instant $k+1$. Thus, the proposed FCS-MPC control can be considered as having an one-step prediction horizon. Once the currents have been updated, the current predictions in (7) are calculated for any possible converter state.

$$\begin{cases} i_\alpha(k+2) = \frac{L-RT_s}{L} i_\alpha(k+1) + \frac{T_s}{L} v_\alpha(k) \\ i_\beta(k+2) = \frac{L-RT_s}{L} i_\beta(k+1) + \frac{T_s}{L} v_\beta(k) \end{cases} \tag{7}$$

D. DC-link Current Prediction

Based on (5), the prediction horizon of the instantaneous DC-link inverter current $i_{\text{in}}(k+2)$ for the FCS-MPC method with the defined switching state $S_\alpha(k+1)$ and $S_\beta(k+1)$ is given by:

$$i_{in}(k+2) = 1.5 \times [S_\alpha(k+1) i_\alpha(k+2) + S_\beta(k+1) i_\beta(k+2)] \tag{8}$$

The current $i_{\text{avg}}(k+2)$ flowing from the DC source side can be regarded as a constant within a switching period. This variable can be derived according to the law of conservation of energy as:

$$i_{\text{avg}}(k+2) = \frac{1.5 \times [R i_\alpha^2(k+2) + R i_\beta^2(k+2)]}{V_{\text{dc}}} \tag{9}$$

E. Cost Function Design

In the proposed method, there are two important objectives that need to be fulfilled by the FCS-MPC controller. The first is the output current reference tracking to achieve the desired sinusoidal shape and magnitude of this variable. The second function is the minimization of the DC-link capacitor current ripple to be ideally as close as possible to i_{avg}. The lower i_{in} is, smaller will be the DC capacitor losses due to the consequent lower RMS value and harmonic amplitudes of the current flowing through it. Therefore, the FCS-MPC cost function can be defined as:

$$G = |i_\alpha(k+2) - i_\alpha^*(k+2)|^2 + \left| i_\beta(k+2) - i_\beta^*(k+2) \right|^2 + \lambda \left| i_{\text{in}}(k+2) - i_{\text{avg}}(k+2) \right|^2 \tag{10}$$

where $i_\alpha^*(k+2)$ and $i_\beta^*(k+2)$ are the current reference in $\alpha-\beta$ frame, and λ represents the weighting factor. The proposed cost function can deliver the sinusoidal output current while maintaining reduced

DC-link current ripple provided that λ is properly selected.

The overall block diagram of the proposed DC current reduction method is shown in Fig. 4.

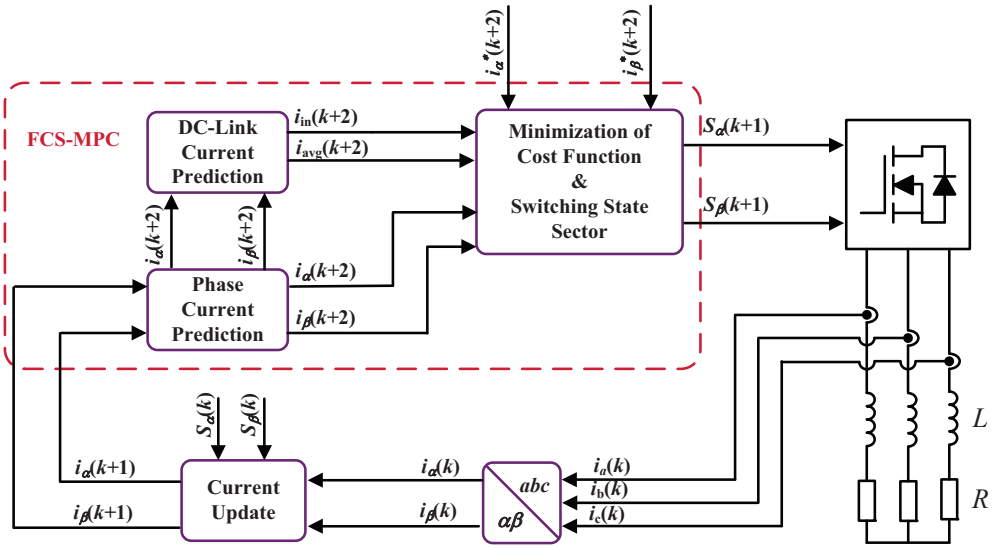


Fig. 4: Block diagram of the proposed FCS-MPC

IV. Simulation and Experimental Results

The verification of the proposed DC-link capacitor current reduction method is presented in both, a circuit simulation environment and with the use of a VSI experimental hardware setup by comparing the obtained results with the traditional FCS-MPC[13]. Simulations have been carried out in PLECS software and the control platform used in the experimental part is the Texas Instruments DSP TMS320F28335. In both simulation and experiments, the DC-link voltage is set as $V_{dc} = 200$V, the inductor L is chosen to be 4.3 mH; the sampling frequency T_s is selected as 20 kHz; λ is set as 0.3.

A. Simulation results

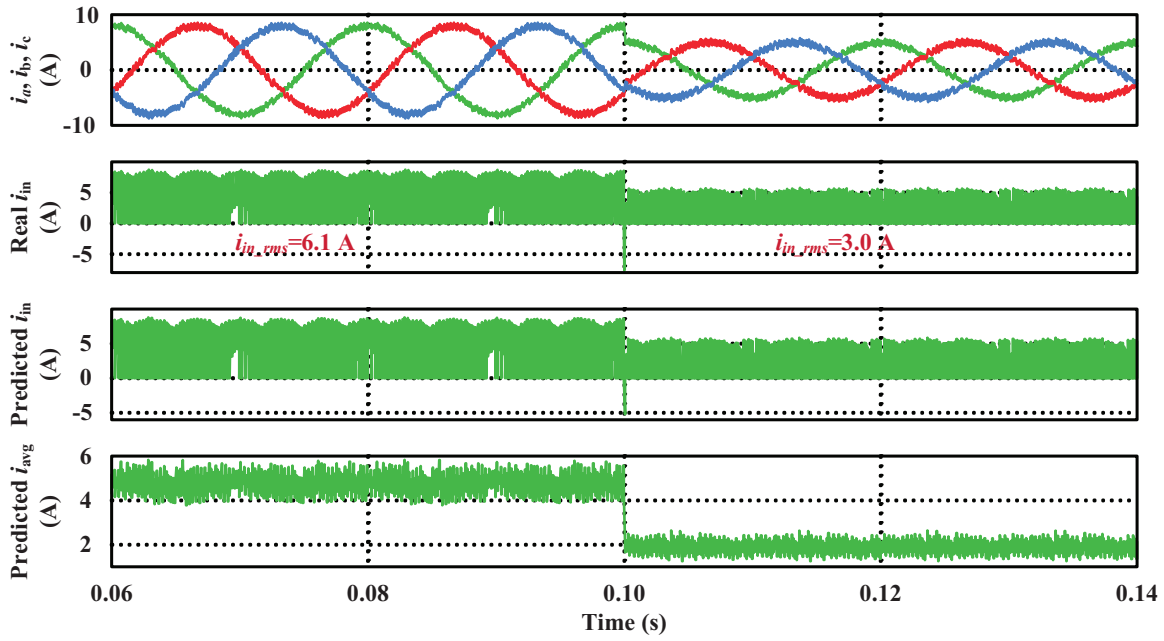
Fig. 5 shows the simulation results for the traditional and the proposed DC-link current ripple reduced FCS-MPC methods when the output current stepped down from 8A to 5A. It can be seen that the predicted i_{in} matches well the real i_{in}. Additionally, the current RMS value across the DC capacitors of the VSI implementing the proposed FCS-MPC is lower than that of the one using the traditional method. Since the i_{avg} and output currents are the same in both methods, the one with lower i_{in} will lead to reduced i_{ripple} and consequent less losses across the DC capacitors.

B. Experimental results

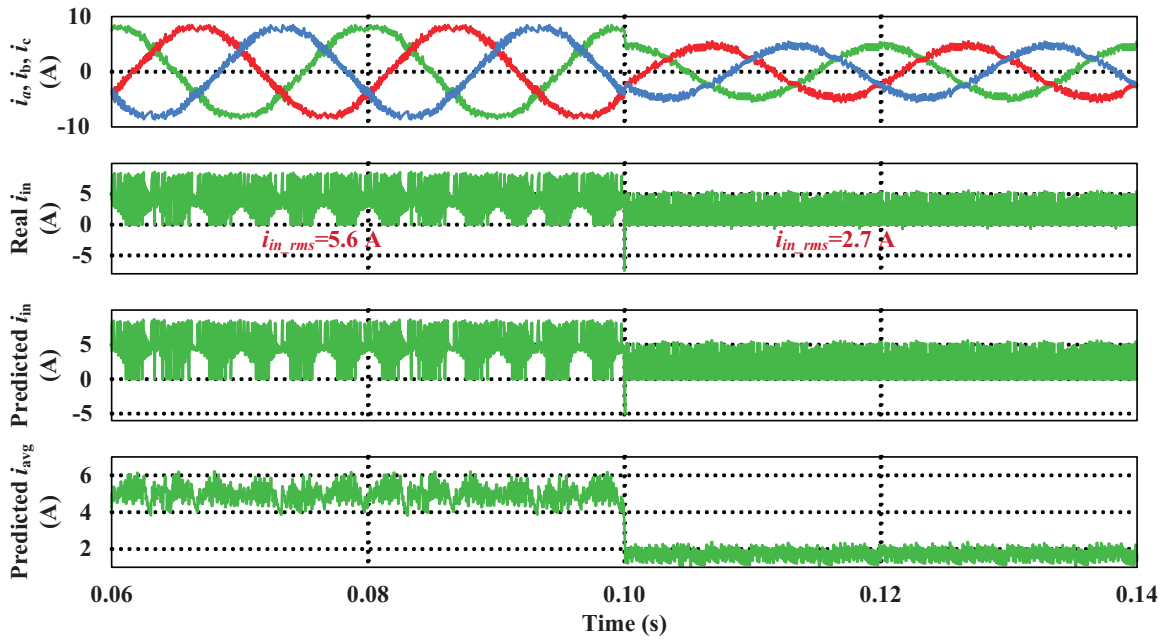
Fig. 6 shows the experimental results of the VSI implementing the traditional FCS-MPC and of the one using the proposed DC-link current ripple reduced FCS-MPC methods when the amplitude of the output current is set to 8A. The tested RMS value of i_{in} for the traditional FCS-MPC is 2.70A, while that for the proposed FCS-MPC is reduced to 2.13A, a considerable reduction of 21% is achieved. It is noted that due to the bandwidth limit of the current probe, high-frequency components into the i_{in} are not collected into the oscilloscope resulting in the difference of i_{in} between the experiment and simulation.

V. Conclusion

A FCS-MPC method with DC-link capacitor current ripple reduction has been studied for the two-level three-phase voltage source inverter. The basic discrete time model of a VSI and the model of the DC-link current have been analyzed. The control objective with reduced DC-link current ripple can be achieved with proper weight factor in the cost function of the FCS-MPC, while the typical logic for the fast



(a)



(b)

Fig. 5: Simulation results (a) traditional FCS-MPC, and (b) proposed reduced DC-link current stress FCS-MPC.

tracking of the sinusoidal output current is kept unaltered. Compared with the classic FCS-MPC, the proposed method can effectively reduce the DC-link current ripple while keeping the typical outstanding dynamic performance of the output current. Both, circuit simulation and laboratory experimental results have verified the theoretical analysis and the superiority of the proposed MPC approach.

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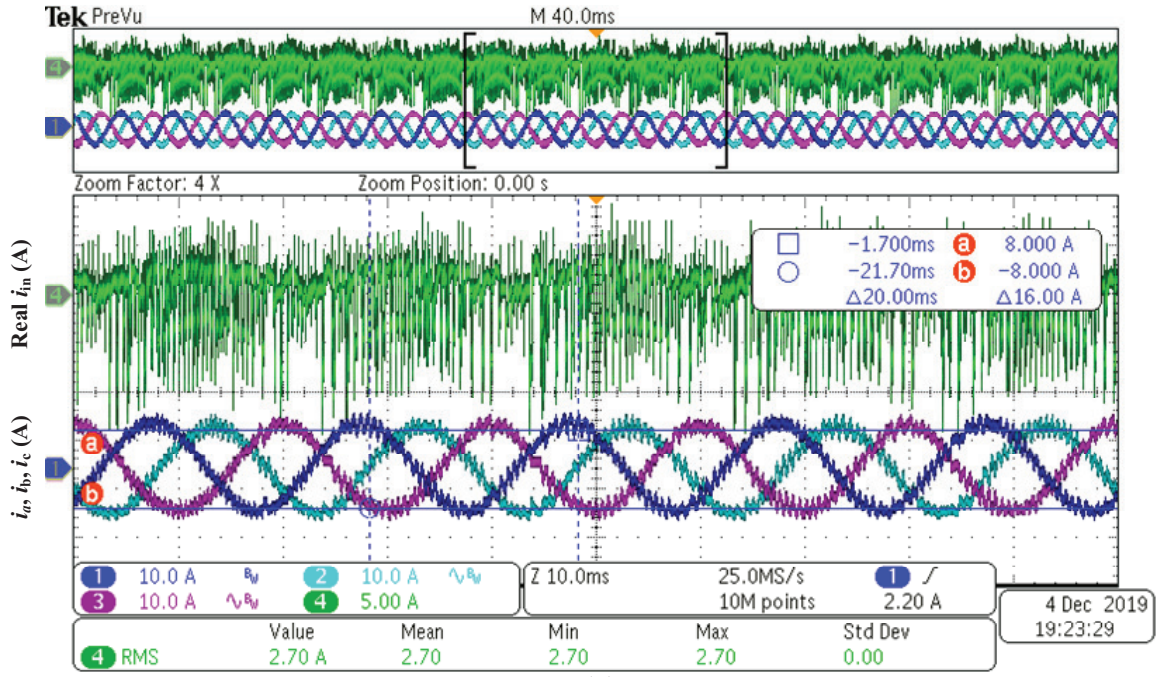

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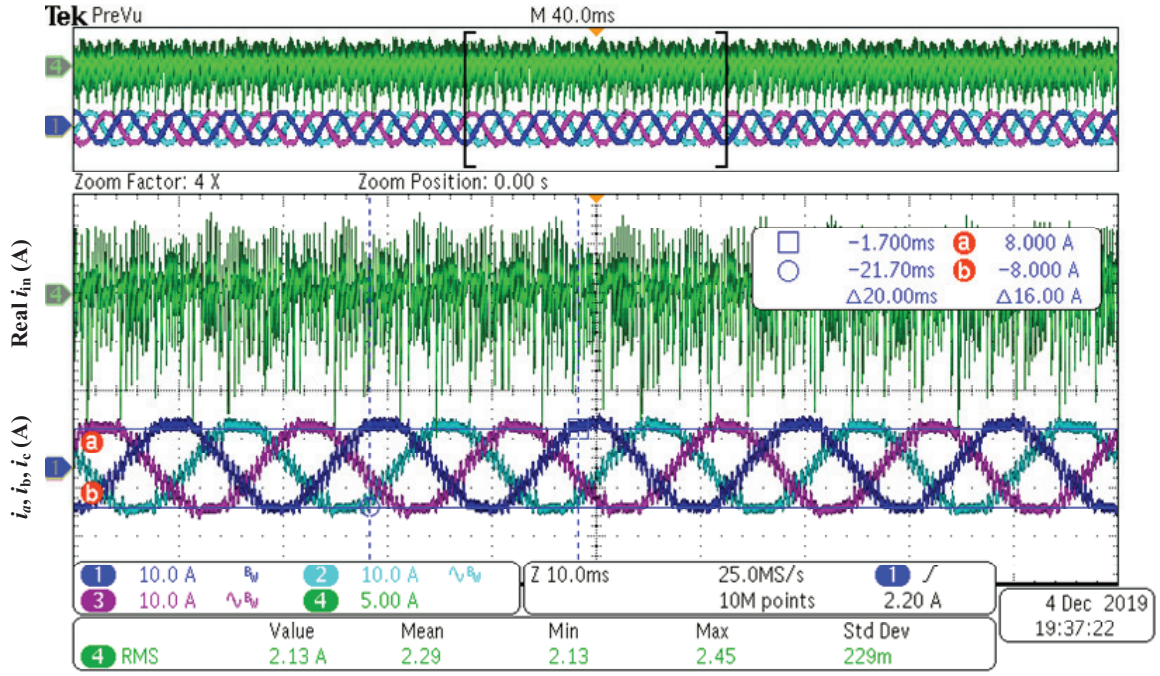

(b)

Fig. 6: Experimental results (a) traditional FCS-MPC, and (b) proposed reduced DC-link current stress FCS-MPC

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