End-of-life assessment of silicon IGBT and silicon-carbide MOSFET

using the power cycling test

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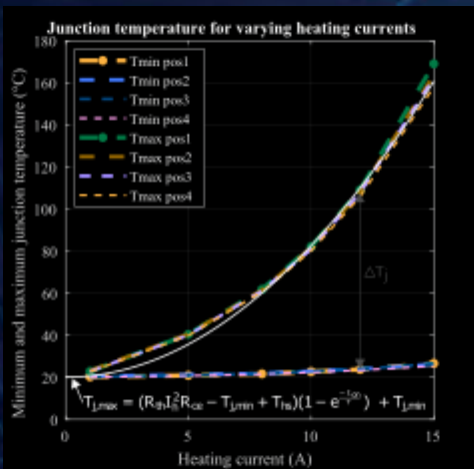

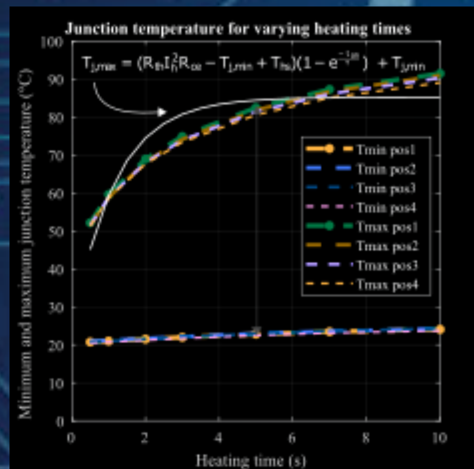

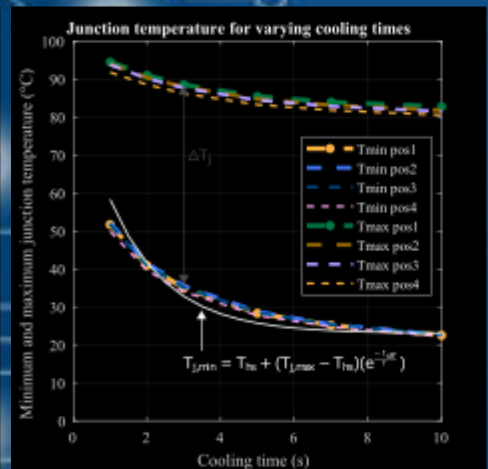

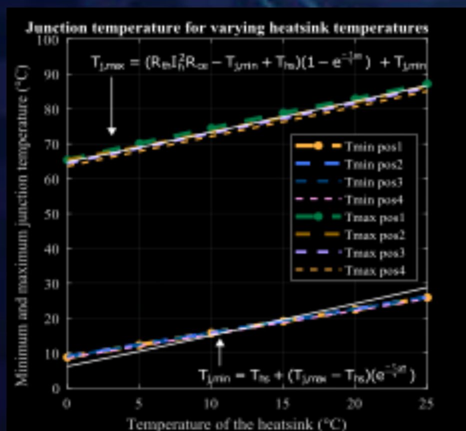

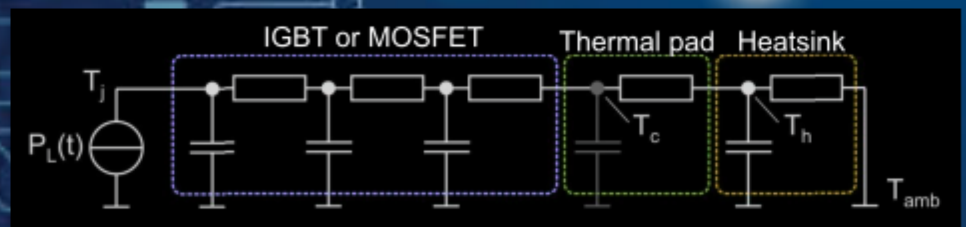

Heating: $T_j(t) = (R_{th} I_h^2 R_{ce} - T_j(t_0) + T_{amb})(1 - e^{\frac{-(t-t_0)}{\tau}}) + T_j(t_0)$

Cooling: $T_j(t) = T_{amb} + (T_j(t_0) - T_{amb})e^{\frac{-(t-t_0)}{\tau}}$

$$T_{j,min} = T_{hs} + (T_{j,max} - T_{hs})(e^{\frac{-t_{off}}{\tau}})$$

$$T_{j,max} = (R_{th} I_h^2 R_{ce} - T_{j,min} + T_{hs})(1 - e^{\frac{-t_{on}}{\tau}}) + T_{j,min}$$

$$\Delta T_j = (R_{th} I_h^2 R_{ce} - T_{j,min} + T_{hs})(1 - e^{\frac{-t_{on}}{\tau}})$$

TU Delft

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using the power cycling test

by

Margo Molenaar

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Preface

This thesis is the final part of my now complete education as an Electrical Power Engineer at the technical university of Delft. Since I started my bachelor's in 2018, I have increased my knowledge way more than I expected and I am definitely not done learning more. Looking back, I experienced the first year as the most difficult when I had to figure out how to fit all lectures, practicums, and self-study sessions into one week and still have enough time to cook and sleep. This thesis presents the work I accomplished during the last eight months. Not everything went as smoothly as planned but I was very satisfied when the measurements succeeded. I want to thank my supervisors Faezeh Kardan Halvaei and Aditya Shekhar for their support and for making time to help me out. I also want to thank the lab technicians Mladen Gagić, Bart Roodenburg, Harrie Olsthoorn, and Joris Koeners for all their help and knowledge. Furthermore, I want to thank Pavol Bauer and Willem Dirk van Driel to take the time to be part of my thesis committee. In addition, I want to thank my family for all their love and for motivating me to continue.

Margo Molenaar
Delft, June 2023

Summary

The reliability of power semiconductor devices is an important feature when designing converter, since the semiconductors are prone to failure and a weak link in the system [1]–[3]. Power semiconductor devices are susceptible to thermo-mechanical stresses, and should be investigated to make reliable semiconductors [2]. The power losses inside the device resulting in thermal cycling and expanding and contracting the layers of the semiconductors with different rates, are the cause of the thermo-mechanical stresses [1], [4]. Thermo-mechanical fatigues are the most frequently encountered forms of failure in power devices, e.g. bond wire lift-off, solder cracks, and reconstruction of chip materialization [2], [5]–[7]. In this thesis, the end-of-life assessment of the silicon IGBT and silicon-carbide MOSFET are investigated. Specifically the power cycling test can replicate the thermo-mechanical stresses and wear out the device in a couple of weeks [8], [9]. Multiple short power cycling tests are executed to find the relationship between the selected parameters and resulting thermal cycle. Furthermore, the thermal response measurements are used to study the thermal behaviour of the semiconductor devices and thermal fatigues. In addition, the thermal model for the test system is arrived, making it possible to create a testbed for the power cycling test for different thermal cycles. Lastly, the end-of-life assessment is executed for 23 days on eight silicon IGBTs.

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Nomenclature

Abbreviations

Abbreviation	Definition
IGBT	Insulated-Gate Bipolar Transistor
MOSFET	Metal-Oxide- Semiconductor Field-effect Transistor
BJT	Bipolar Junction Transistor
Si	Silicon
SiC	Silicon-Carbide
CTE	Coeficient of Thermal Expansion
DCB	Direct Copper Bonding
Pos	Position
TRM	Thermal Response Measurement
PCT	Power Cycling Test

Symbols

Symbol	Definition	Unit
$T_{\text{j,max}}$	Maximum junction temperature	[°C]
$T_{\text{j,min}}$	Minimum junction temperature	[°C]
ΔT_{j}	Junction temperature swing	[°C]
t_{on}	Heating time	[s]
t_{off}	Cooling time	[s]
I_{h}	Heating current	[A]
I_{s}	Sensing current	[A]
T_{hs}	Temperature of the heatsink	[°C]
V_{ge}	Gate-emitter voltage	[V]
V_{ce}	Collector-emitter voltage	[V]
V_{gs}	Gate-source voltage	[V]
V_{ds}	Drain-source voltage	[V]
V_{d}	Voltage drop over the diode of the IGBT	[V]
τ	Thermal time constant	[s]
R_{th}	Thermal resistance	[K/W]
C_{th}	Thermal capacitance	[Ws/K]
$R_{\text{ds,on}}$	Electric on-resistance between the drain and source of the MOSFET	[Ω]
$R_{\text{ce,on}}$	Electric on-resistance between the drain and source of the MOSFET	[Ω]
$P_{\text{L,c}}$	Conduction power losses	[W]
$P_{\text{L,sw}}$	Switching power losses	[W]

1 Introduction

Semiconductor devices are essential building blocks in power electronic systems and therefore crucial in our technological society. Semiconductor devices can be controlled to conduct current and are therefore used for switching applications, amplification, and energy conversion. The most commonly used semiconductor devices are the metal-oxide-semiconductor field-effect transistor (MOSFET) and insulated-gate bipolar transistor (IGBT), made from silicon doped with boron and phosphorous [10]. The drive for innovation, e.g. increasing the voltage range and efficiency, has led to the creation of the silicon-carbide MOSFET [11]. Silicon-carbide devices can handle higher operating temperatures, higher voltages, and higher switching frequencies and have lower conduction and switching losses than Si devices [4]. SiC MOSFETs have a breakdown voltage up to 3.3 kV and still have a low on-resistance, fast recovery time, and fast switching, whereas a Si MOSFET has a maximum voltage of 900 V in practice [11], [12].

Another important feature of semiconductor devices is their reliability, since failures can have severe consequences in e.g. the automotive and aerospace industry [3]. The semiconductor devices are particularly prone to failure in power converters or machines and are considered a weak link in the system reliability [1], [2]. In most cases, it is not profitable to install new semiconductors, and the whole system is replaced, leading to more e-waste.

During the operation of power converters, the generation of power losses results in the occurrence of thermal cycles characterized by repeated heating and cooling. These thermal cycles are primarily caused by variations in the load and switching actions. Power semiconductors, which are composed of multiple layers with different coefficients of thermal expansion (CTE), are susceptible to the effects of these temperature cycles [13], [14]. It is crucial to consider these thermal effects and the associated thermo-mechanical stresses in the design and operation of power converters to ensure their reliable performance and longevity. Thermo-mechanical fatigues are the most frequently encountered forms of failure in power devices [5]. The thermo-mechanical fatigues that can arise from these thermal cycles are bond-wire cracks, bond-wire liftoff, solder fatigues in the baseplate or chip, and the reconstruction of chip metallization [1], [2], [4], [6], [7]. These phenomena can lead to the deterioration and potential failure of the power devices over time. The most common failures due to thermo-mechanical stresses are bond-wire cracks and bond-wire liftoffs [4], [7].

Due to the time-consuming nature of collecting field data for the reliability evaluation of power devices, end-of-life assessments are frequently employed. These tests, involving power cycling and thermal cycling, aim to replicate the thermal stress effects that power devices undergo when in use [1], [4]. Evaluating the devices' reliability and determining end-of-life under more condensed timeframes is feasible by putting them through accelerated aging tests. During the thermal cycling test, the device is heated and cooled by for example a heatsink where the device will follow the thermal cycle of the heatsink [4], [10]. In addition, power cycling tests include periodically applying and removing power to the devices, resulting in active heating due to the power losses [4], [10]. During the power cycling test, the heatsink has a fixed temperature and is used to cool down the device. The thermal cycles

can be executed faster in the power cycling test, since only the device itself needs to be heated. Both tests will replicate the thermal stresses the devices experience in real-world situations and are useful tools to evaluate the device's reliability under various thermo-mechanical stresses [1]. Through these end-of-life assessments, valuable insights can be gained regarding the reliability of power devices, their main failure mechanism, and expected lifetimes under cyclic thermal loading [15]. This information is essential for designing robust and reliable power electronic systems, as it allows for early identification of potential failure mechanisms and optimizing device lifetimes [1].

Based on the literature study and the discussion with my supervisors, the following research objective are set:

- **Understand the electrical characteristics and thermal behavior of power semiconductor devices.**
- **Increase the knowledge about the end-of-life assessment of power semiconductor devices by performing the power cycling test.**
- **Derive the empirical thermal model of the semiconductor devices.**

The research question is therefore as follows:

How to perform an end-of-life assessment for silicon IGBTs and silicon-carbide MOSFETs?

Before answering this question, I will first divide it into smaller tasks and subquestions.

1. **What is the empirical thermal model of the semiconductor devices with the practical setup?**
    - Key focus:
        - Understand the power semiconductor device thermal behavior.
        - Employ a robust practical thermal model for the system.
    - Challenges:
        - The experimental setup has its own characteristics, so to accurately capture the unique characteristics of the practical setup, it is imperative to construct a thermal model that represents the entire system.
        - The used heatsink is predesigned by the university and doesn't have a datasheet.
        - The thermal characteristics of the semiconductors can vary from the datasheet since the datasheet is based on the optimal conditions.
2. **What is the influence of the selected parameters for the power cycling test on the thermal cycle?**
    - Key focus:
        - Perform different power cycling tests based on varying the dependent parameters.
        - Find out the impact of the dependent parameters on the thermal cycle.
        - Achieve the desired thermal cycle in the power cycling test based on the free parameters.
    - Challenges:
        - Power cycling tests have different parameters including the heating current, heating time, cooling time, heatsink temperature, and gate voltage which can affect different aspects of the thermal cycle including the maximum junction temperature, the minimum junction temperature, and the fluctuation of the junction temperature.

3. **How can we minimize the duration of the end-of-life assessment?**
    - Key focus:
        - Minimizing the heating and cooling time based on the impact of the thermal cycle.
        - Reduce the thermal time constant of the system.
    - Challenges:
        - In the end-of-life assessment, the semiconductor device needs to be heated and cooled down for around 200 000 cycles or more, which can take up to weeks to complete. Therefore, it is important to improve the setup and settings to reduce the testing time.
        - The thermal time constant determines how fast the system can be heated and cooled. The thermal time constant of the semiconductor devices is fixed, but the thermal interface material and connection can be improved.

The outline of the thesis report will be as follows. First, the relevant findings during the literature study are summarized in chapter 2. Secondly, the practical setup that is used throughout the thesis is explained in chapter 3. In the same chapter, the thermal response measurement, power cycling test, and electrical behavior analysis are discussed. Next, in chapter 4, the thermal equations are calculated for the system. Furthermore, based on the thermal response measurement, the cumulative structure function is derived and used to determine the Cauer thermal model, time constant spectrum and find the different layers of the semiconductor. Subsequently, in chapter 5, the parameters that will influence the thermal cycle and lifetime are investigated and the thermal and electric properties of the system are calculated. Moreover, in chapter 6, the end-of-life assessment is executed for the silicon IGBT. Lastly, the thesis report finished with a conclusion and future recommendation in chapter 7.

2
Literature study

This chapter contains the necessary knowledge obtained from the literature study relevant to understanding this master thesis. I will first discuss the power semiconductor devices, namely the MOSFET and IGBT and the relevance of using silicon-carbide to make them. Secondly, Moreover, the thermal behaviour is discussed. Subsequently, a closer look is given at the reliability, lifetime studies, and power cycling test of the IGBT and MOSFET in more detail. Finally, I will discuss the thermal failure mechanisms of the semiconductors.

2.1. Power semiconductor devices

Power semiconductor devices are essential building blocks in various electronic applications, e.g. power converters. When designing power converters, the important design specifications are typically low costs and high efficiency, referring to low power losses, and high power density. Also, considerations need to be taken for the thermal parameters, like device losses, cooling, and maximal operating temperature [10].

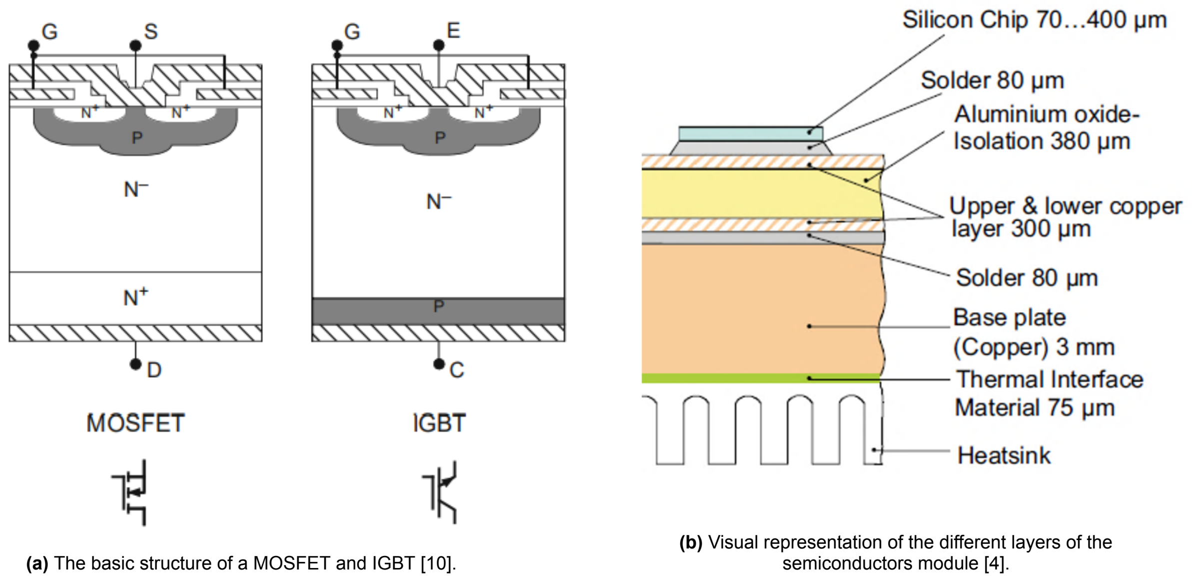
Semiconductors consist of two types of layers; n-type layers, where the silicon is doped with phosphorous, creating additional electrons, and p-type layers, where the silicon is doped with boron, creating additional holes [4], [10], [12]. Connecting the n- and p-type layers with different doping concentrations create semiconductor devices that can be controlled when to conduct electricity. The most common semiconductors used as switching devices are the MOSFET (metal–oxide–semiconductor field-effect transistor) and IGBT (insulated-gate bipolar transistor) [4]. Their basic structure is shown in Figure 2.1a. The difference is the replacement of the N^+-layer with the P-layer at the bottom, creating an extra bipolar junction transistor (BJT) [4], [10]. The semiconductors consist of an accumulation of different layers, as shown in Figure 2.1b [2]. At the top, the chip is soldered onto the copper layer. Between the copper layers is the isolation layer. The lower copper layer is soldered onto the baseplate and at the bottom of the semiconductor, there is a thermal interface layer and heatsink.

2.1.1. MOSFET

The MOSFET is a majority-carrier device that only uses electrons to conduct current. In order words, they have no excess minority carriers that must be moved and can therefore turn on and off faster than bipolar devices [4], [12]. By making the drift region (N^--layer) of the MOSFET wider, the voltage capability will increase, but so will the on-resistance [12]. Hence, there is a design trade-off between increasing the voltage capabilities and decreasing the conduction power losses. In practice, the maximum voltage of a silicon MOSFET is below 900 V [11]. The switching speed of the MOSFETs depends on the capacitance of the stray and depletion layers [12].

2.1.2. IGBT

The IGBT is a bipolar device, where electrons and holes are both used as charge carriers to conduct the current [4], [11]. The IGBT turns on when the gate-emitter and collector-emitter paths are positively biased and holes are injected from the P-layer at the bottom into the drift region [4], [12]. Therefore,



(a) The basic structure of a MOSFET and IGBT [10].

(b) Visual representation of the different layers of the semiconductors module [4].

Figure 2.1: The layout of semiconductor devices.

simultaneously increasing the carrier concentration and decreasing the resistance, and decreasing the forward voltage [4], [12]. This process is called conductivity modulation and makes the on-resistance of the IGBT much smaller than the on-resistance of the MOSFET [4], [12]. Therefore, the length of the drift region can be increased to achieve the desired voltage capability. Currently, available IGBTs are rated for voltages up to 6.5 kV, which is much higher than the rating for a Si MOSFET [11]. However, during turn-off the minority carriers must be dissipated from the drift area or recombined, resulting in larger turn-off times and increased switching losses compared to the MOSFET [4].

2.1.3. Power losses

During the operation of the semiconductor devices various power losses occur. These power losses is the source of the heating of the devices and the thermo-mechanical stresses. For designing semiconductor devices, power losses should be minimized in order to increase longevity and efficiency.

The conduction losses $P_{\text{L,c}}$ of the MOSFET are calculated as $P_{\text{L,c}} = I^2 \cdot R_{\text{ds}}$ where I is the current flowing through the device, and R_{ds} is the resistance between the drain-source. R_{ds} is the summation of the 5 parasitic resistances inside the MOSFET as shown in Figure 2.2. The gate-to-source bias voltage will affect the channel resistance and accumulation layer resistance [12]. Furthermore, the doping and dimensions of the regions will affect the on-state resistance [12].

The conduction losses of the IGBT are calculated as $P_{\text{L,c}} = I^2 \cdot R_{\text{ce}} + I \cdot V_{\text{d}}$, where I is the current flowing through the device, R_{ce} is the resistance between the collector-emitter which is very small because of the conductivity modulation and V_{d} is the voltage drop over the diode, which is typically around 0.8 V [16].

The power losses during the on and off switching of the IGBT and MOSFET can be calculated by adding the energy needed for turning on and off given in the datasheet and multiplying this with the switching frequency, $P_{\text{L,sw}} = (E_{\text{on}} + E_{\text{off}}) \cdot f_{\text{sw}}$ [16].

In power converter topologies, zero voltage switching or zero current switching can be applied to reduce the switching losses. Furthermore, by adding snubber circuits, the switching losses of the semiconductor device can be moved to the snubber circuit, reducing the heat and increasing the lifetime of the semiconductor device.

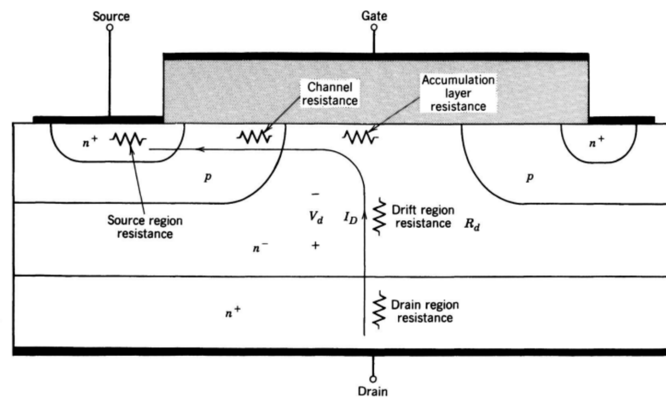


Figure 2.2: Cross sectional structure of the MOSFET and the components of the on-state resistance [12].

2.1.4. Silicon-carbide power devices

The next generation of power devices is made from Silicon-Carbide (SiC) to improve the device properties. SiC material has a wider bandgap of 3.26 eV compared to the bandgap of Si of 1.12 eV [17]. The higher bandgap will result in a device that can handle higher temperatures, higher voltages, and higher frequencies. The advantages of SiC devices over Si devices are [4]:

- Lower conduction and switching losses, therefore more efficient
- Higher blocking voltages
- Higher possible power densities
- Higher permissible operating temperatures
- Shorter switching times and higher switching frequencies

Especially fast majority-carrier devices, such as the Schottky barrier diodes and MOSFETs benefit from the use of carbon since their performances are limited by the applied voltages and conduction losses. SiC MOSFETs can handle up to 3.3 kV while keeping a low on-resistance, fast recovery time, and fast switching [11]. M. Nawaz and K. Ilves conducted research about the SiC MOSFET and concluded that the on-resistance is 4 to 8 mΩ for 1.2 to 1.7 kV power modules, the current rating is 120 to 300 A and the short circuit survivability time is 3 to 4 μs [18]

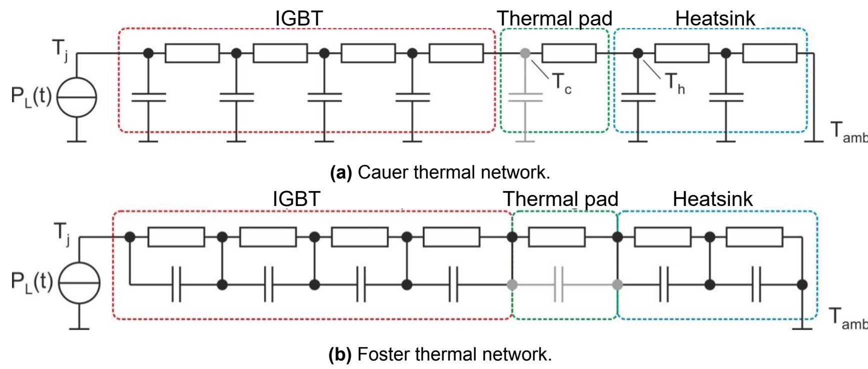
The coefficient of thermal expansion of SiC devices is $4.0 \cdot 10^{-6}$ °C^{-1}, which is slightly higher compared to $3.5 \cdot 10^{-6}$ °C^{-1} for Si [4], [19]. SiC devices have 2.4 times higher Young's modulus, 410 GPa compared to 169 GPa for Si devices [19], [20]. For semiconductors with the same geometry and thermal cycle, SiC semiconductors will experience larger thermo-mechanical strains inside the device, possibly reducing the lifetime [9], [21].

2.2. Thermal behaviour of semiconductor devices

The thermal properties and behavior of the semiconductors are needed when designing a thermo-electrical system, e.g. a battery charger, in order to postpone thermal failures. Many models exist to calculate the dynamic heat dissipation and heat transfer throughout the system [22]. The most used models are the Foster and Cauer thermal models shown in Figure 2.3 [23]. Most semiconductor manufacturers give the Cauer or Foster model in their datasheets [24], [25]. Furthermore, the time constant spectrum, calculated from the Foster model, can be used to solve transient and pulse heat-resistant problems [26].

2.3. Reliability of semiconductor devices

Semiconductor devices, such as the IGBT and MOSFET, are the most vulnerable component in power converters and are considered a weak link in the system reliability [1], [2]. Reliability is the ability of a system or component to perform its required functions under stated conditions for a specified period of



(a) Cauer thermal network.

(b) Foster thermal network.

Figure 2.3: The Cauer and Foster thermal network models.

time [27]. A failure in the semiconductor can have severe consequences in power electronic applications in e.g. the automotive and aerospace industry [3]. During the operation of power converters, the generation of power losses results in the occurrence of thermal cycles characterized by repeated heating and cooling [2]. Thermo-mechanical fatigues are the most frequently encountered forms of failure in power devices [5]. It is crucial to consider the thermal effects and the associated thermo-mechanical stresses in the design and operation of power converters to ensure their reliable performance and longevity. When a region of the semiconductor breaks, the surrounding regions can still continue to function, and therefore the device is not immediately completely malfunctioning. The component will, however, be less efficient, and consequently, the voltage and temperature will rise. This will also lead to more thermal stresses and accelerate the degradation process. In most cases, it is not profitable to install new semiconductors and the whole system is replaced, resulting in more e-waste.

In order to compare the IGBTs and MOSFETs, criteria are set for defining the end-of-life. The IGBT and MOSFET have declared broken if any of the following criteria are exceeded with respect to their initial (healthy) conditions [2]:

- The collector-emitter saturation voltage increases by 5 % or the drain-source voltage increases by 5 %.
- The thermal resistance increases by 20 %.
- The gate current increases by 20 %.

2.3.1. Accelerated aging test

To evaluate the reliability and end-of-life of the semiconductor devices without collecting data over a time period of years, accelerated aging tests have been developed. These tests aim to replicate the thermo-mechanical stresses present during the operation in the field [1]. The thermal cycles are accelerated, but the thermo-mechanical stresses are the same. Therefore, the amount of thermal cycles until the semiconductor devices break is the same as in practical applications [1], [2], [15].

The commonly used accelerated aging tests are the thermal cycling test and the power cycling test. During the thermal cycling test, the heatsink is heated and cooled repeatedly [4], [10]. The devices will follow the thermal cycle of the heatsink. In contrast, power cycling tests include periodically applying and removing power to the devices, resulting in active heating due to the power losses [4], [10]. During the power cycling test, the heatsink has a fixed temperature and is used to cool down the device. The thermal cycles can be executed faster in the power cycling test, since only the device itself needs to be heated. Nevertheless, the power cycling test needs a power source that can apply large currents and the longevity must be higher than the tested semiconductors.

Power cycling parameters

The thermal stresses are determined by the CTE difference and temperature variation. Therefore, the temperature cycle in the power cycling test will directly influence the number of cycles. Since bond wire failures are the most common type of failures [7], the junction temperature swing is the most important parameter influencing the lifetime. However, the median junction temperature and

case temperature variation are important as well. The LESIT model shows the relation between the junction temperature swing and median junction temperature to the number of cycles to failure [28]. The junction temperature swing is determined by the power losses, so the heating current and electric resistance and wire diameter will influence the lifetime. Experiments by Reinhold Bayerer et al. show that both the heating current and the heating time will influence the number of cycles [29]. I expect that the thermal time constant, i.e. the thermal resistance and thermal capacitance, play a role in the lifetime, since those thermal parameters affect the junction temperature.

Control strategies

There are 4 strategies to execute the power cycling test. The most basic one is to use fixed turn-on and turn-off times corresponding to the desired temperatures ΔT_{j}, $T_{\mathrm{j,max}}$ and $T_{\mathrm{j,min}}$. When using this control strategy, the degradation effects will increase the ΔT_{j} and shorten the lifetime [10]. This corresponds to the real-life applications. The second control strategy is to vary the turn-on and turn-off times depending on the measured case or heatsink temperature. This strategy will eliminate the influence of the cooling conditions and possible fluctuations. Furthermore, also the influence of changes in the thermal resistance between the case to heat sink will be eliminated if the case temperature is used as a reference [10]. The third control strategy is to maintain a constant power loss by varying the applied current or gate voltage The heating time will be fixed, and the energy losses are constant. This strategy reacts to degradation and stretches the lifetime of the IGBT [10]. The fourth control strategy is to maintain a constant temperature swing ΔT_{j}. Depending on the measured junction temperature, either the turn-on and turn-off times vary or the current or gate voltage varies [10]. This strategy is not influenced by the degradation effects and will result in a higher lifetime [10].

Lifetime studies

Z. Sarkany et al. executed the power cycling test on IGBT modules [8]. They tested different control modes, namely the constant heating current, constant heating power and constant temperature swing. In all cases, the heating current was around 68 A to reach a temperature swing of $105°$C. The module for constant heating current failed at 46 500 cycles after the stepwise rise of the voltage referring to bond wire degradation. The others IGBT modules continues until 65 000 cycles when the tests were stopped.

G. Zeng et al. executed the power cycling test on IGBT chips [30]. Not only did they test with different control strategies, but also different ways to obtain the constant power and constant temperature swing. In their test, the temperature swing was $87°$C and their medium temperature was $103°$C. The longest lifetime, namely 202 thousand cycles, was reached by adjusting t_{on} to keep a constant ΔT_{j}. The shortest lifetime of 115 thousand cycles was reached by keeping a constant heating current and not compensating for any degradation. All devices failed because of degradation of the chip solder, and the resulting thermal resistance from junction to heatsink was increased by 20 %.

N. Baker and F.Iannuzzo performed the power cycling test on MOSFETs and used the auxiliary source terminal to measure the voltage across the die and bond wires separately [9] [31]. The bond wire resistance increases from 3.3 mΩ to 3.9 mΩ and lifted up at 75 and 150 thousand cycles.

R. Schmidt and U. Scheuermann executed power cycling test with different bond wire geometries and solder layers [7]. By using small heating and cooling times, 1.2 s and 3.2 s respectively, they were able to increase the junction temperature by $70°$C and the case temperature by $20°$C resulting in only bond wire heel cracks and liftoff. Bond wires with a large aspect ratio, i.e. a larger loop radius, had the most amount of cycles to failure, namely 234 thousand cycles for a soldered and 647 thousand cycles for a sintered connection, while bond wires with a lower aspect ratio failed at 79 thousand cycles for both soldered and sintered connection. In this paper, all samples failed due to bond wire heel cracking. By using larger heating and cooling times, 13.6 s and 10.3 s respectively, their test resulted in a junction temperature swing of $110°$C and case temperature swing of $45°$C. Bond wires with a low aspect ratio, both soldered and sintered, as well as soldered bond wires with a high aspect ratio failed due to bond wire failures around 40 thousand cycles, while the sintered bond wire with a high aspect ratio failed at 54 thousand cycles due to chip solder degradation [7].

Finally, M. Nawaz and K. Ilves researched the SiC MOSFET and concluded that the on-resistance

is 4 to 8 mΩ for 1.2 to 1.7 kV power modules, the current rating is 120 to 300 A and the short circuit survivability time is 3 to 4 μs [18].

2.4. Failure mechanisms in semiconductors

There are many reasons why semiconductors can fail or break. There can be random failures like unexpected events that will exceed the maximum voltage or current ratings of the device. Furthermore, there are also many wear-out mechanisms that can cause the semiconductor to fail in the long run. This can be thermal stresses, mechanical vibrations, and humidity. In this thesis, the focus lies on investigating thermo-mechanical stresses.

During operation, the semiconductors are periodically turned on and off. When the device is conducting power, there are losses that will heat up the device. The device will cool down again when it's turned off. In most cases, a heatsink is connected, to cool down the device. Each material, and therefore each layer, has a different coefficient of thermal expansion (CTE), which is the fractional increase of length per unit rise in temperature [14]. The CTE of commonly used materials in IGBTs are given in Table 2.1. The periodic heating and cooling down of the device will expand and contract the layers resulting in shear stresses, because of the difference in CTE and the fixed constraints between layers [14].

Table 2.1: The coefficient of thermal expansion for different materials [4], [32]–[34].

Material	**CTE** (10^{-6} °C^{-1})
Si chip	3.5
SiC chip	4.0
AlN - DCB	8.2
Al_2O_3 - DCB	10.7
AlSiC base plate	7
Cu base plate	17
Al bond wire	23
SAC305 solder (SnAgCu)	23.5
PbSn solder	19

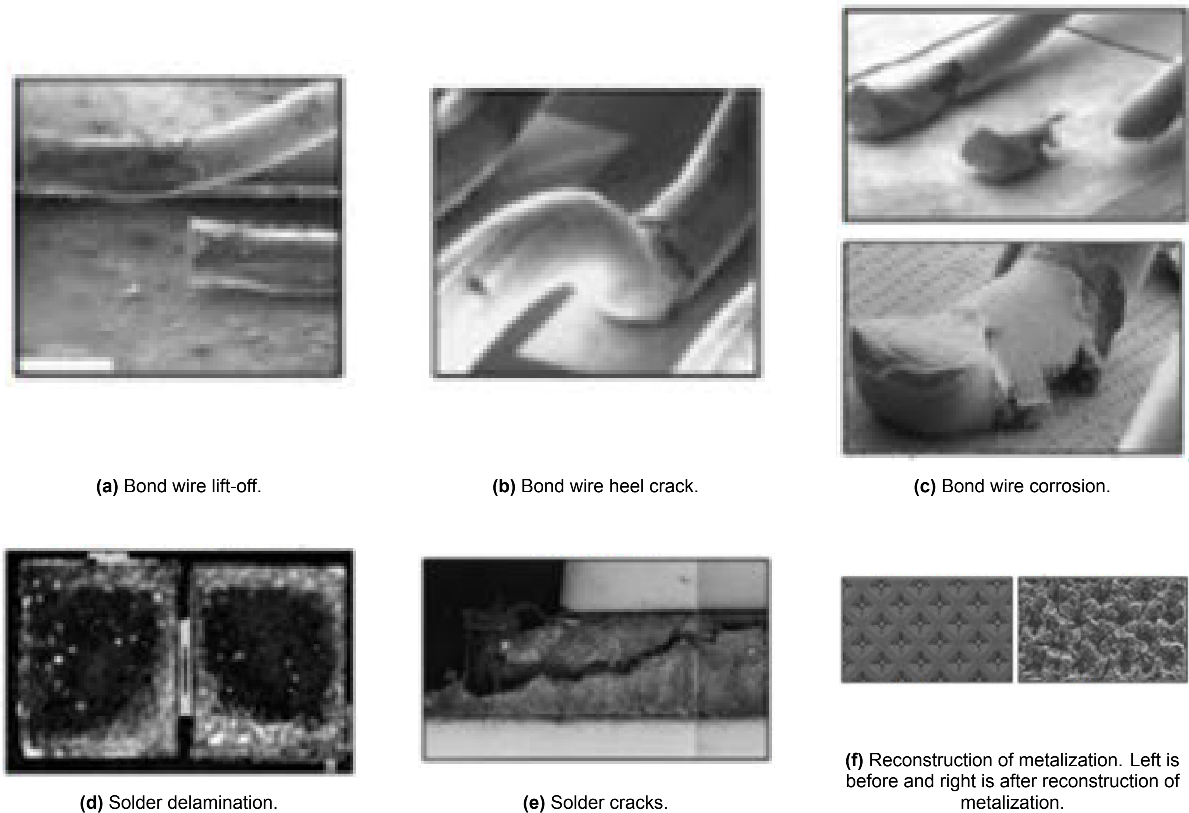
After a number of cycles, also known as the lifetime, the material is worn-out and the semiconductor fails. Further investigation can show which layers are broken. In the IGBTs and MOSFETs, thermal stress can result in bond wire cracks, bond wire lift-off, solder fatigue in the baseplate or the chip, and reconstruction of the chip metallization [2]. Examples of those thermal failures are shown in Figure 2.4.

The bond wire and chip will heat up the most since in these parts, the power losses are created. From there, the heat is transferred through the other layers. The most shear stresses appear when the difference in CTE of adjacent layers and temperature variation is large. Therefore, the strongest thermal stresses are between the bond wire and chip and between the solder layer and chip. It is expected that bond wire liftoff and solder fatigues are the most common thermal failures. The thermal stresses can be reduced by using materials with matching CTE, e.g. the PbSn solder will break later than the SAC305 solder.

2.4.1. Bond wire lift off or cracks

Thermal stresses between the bond wires and chip connection will eventually break the connection between the aluminum grains inside the bond wire and result in a crack [1]. An example of a crack is shown in Figure 2.5. When the stresses continue, the crack grows until the whole wire is disconnected or lifted. Usually, the crack starts at the bending edge, a.k.a. the heel and toe of the foot, and grows to the center [1]. The bond wire will lift off when the crack has reached the center of the connection [1]. Bond wire lift-off can also be the result of surpassing the current capability or burnouts due to cosmic rays [2].

After the bond wire has been lifted, the current is shifted to nearby wires, which leads to a non-homogenous current distribution on the IGBT chip [1]. This results in a higher local current and larger



(a) Bond wire lift-off. **(b)** Bond wire heel crack. **(c)** Bond wire corrosion.

(d) Solder delamination. **(e)** Solder cracks. **(f)** Reconstruction of metalization. Left is before and right is after reconstruction of metalization.

Figure 2.4: Examples of thermal failures in semiconductor devices [2].

thermal stresses on the other bond wires. The lifting of other bond wires is accelerated. Bond wire degradation can be observed as abrupt increases of the collector-emitter voltage of the IGBT or drain-source voltage of the MOSFET [2].

Bond wire lifting usually occurs before thermal fatigue of solder joints and is therefore considered the dominant failure mechanic caused by power cycles [1]. Furthermore, literature shows that the bond wire degradation is strongly dependent on the junction temperature swing [2].

By connecting the bond wires, the crystalline structure is impaired. Therefore, the main weak point of the bond wire connections are the areas above the ultrasonic bonds [4]. Wire alloys and bonding processes have been optimized to double the bond wire lifetime [4]. S. Ramminger et al. present the relation between the bond wire loop geometry and the mechanical stresses in the lateral direction, resulting in heel crack failures [6]. Furthermore, by using bond wires with double sides pressure contacts, the bond wire failures can be reduced [4], [7].

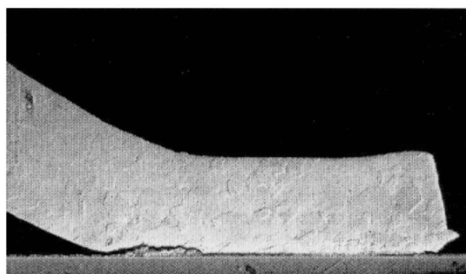


Figure 2.5: Cross-sectional view of a crack between the bond wire and chip [1].

2.4.2. Solder fatigue on the baseplate or chip

The solder layers have a large surface area. Consequently, their temperature rises quickly, while they don't have much space to expand [4]. Solder fatigues lead to an increase in the thermal resistance [4]. When the thermal resistance is increased, the device will heat up even more and the failure mechanisms are accelerated. The collector-emitter voltage of the IGBT or drain-source voltage of the MOSFET and maximal junction temperature will increase gradually, indicating the solder fatigues [2]. Figure 2.4d and Figure 2.4e show what the solder delamination and solder cracks look like. Solder fatigues will usually start at the corners and edges, but for larger chips, the center can also be damaged sooner since there the temperature deviation is the largest [4].

In some cases, the baseplate and corresponding solder layer can be removed, which will prevent device failure due to fatigue in the baseplate solder [4]. Furthermore, by using AlN substrates instead of Al_2O_3 substrates, the solder fatigues are reduced, since the difference in thermal expansion coefficients with silicon or silicon-carbide is decreased [4].

2.4.3. Reconstruction of chip metallization

When the temperature exceeds the homologous temperature, plastic deformation takes place [2], as shown in the example of Figure 2.4f. The site loses strength and the growth of microcracks is accelerated [2]. The creep mechanisms that lead to plastic deformation and reconstruction are diffusion, grain boundary sliding, and dislocation and are most severe under elevated junction temperatures [2].

Reconstruction of chip metallization leads to an increase in the sheet resistance and therefore increases the collector-emitter voltage of the IGBT or drain-source voltage of the MOSFET [1], [2]. As a result of the reconstruction and increase in voltage, the power losses and junction temperature are increased. This will accelerate the bond wire degradation and metallization degradation [2], [4]. Severe reconstruction can also lead to disconnection of IGBT cells and decrease the conducting area and increase the current densities [1].

3

Practical setup

During my research, I carried out two important tests, namely the thermal response measurement (TRM) and the power cycling test (PCT). Both tests and their practical setup will be explained in this chapter. In addition, the selection of the devices under test is made. Moreover, calibration and the electrical characteristics analysis is executed and discussed.

3.1. Thermal response measurement

In the TRM, a current will flow through the semiconductor device and the device will heat up because of the power losses inside the device. After the set heating time is passed, the heating current will switch off. The devices are connected to a large heatsink and the device will cool down when the heating current is switched off. During the TRM, the temperature is measured during the cooling phase, giving valuable information about its thermal response. Furthermore, the results from the TRM are used to construct the Cauer thermal network and time constant spectrum with the T3Ster Master software from Simcenter [35].

3.2. Power cycling test

The power cycling test is a valuable method to determine the lifetime of semiconductor devices. During the power cycling test, the current is repeatedly flowing through the device. During the on state, the device is actively heated up due to the power losses in the device [10]. During the off-state, the device is cooled down by the heatsink at a steady temperature. The device will heat up and cool down, as indicated in Figure 3.1, and the layers of the device will repeatedly expand and contract [4]. Each layer has a different coefficient of thermal expansion (CTE) and as a consequence, thermo-mechanical stresses are created between adjacent layers [13]. Even when the process of heating and cooling is accelerated, the thermo-mechanical stresses are the same and the test will give realistic information about the lifetime in the tested thermal cycle [1], [2].

Power cycling test with short pulses of a few seconds will heat up and stress the bond wires, die attach layer, and solder layers, and are therefore used to investigate the appearance of bond wire cracks and lift off, solder fatigues in the die attach, and reconstruction of chip metallization [2], [8]. Power cycling tests with longer pulses of a few minutes will heat up and stress the entire module. This can be used to investigate the reliability of the DBC attach, ceramic insulation, and package [2], [8]. In my research, I will execute the short power cycling test, since the bond wire and solder layer are the weakest part of the semiconductor devices.

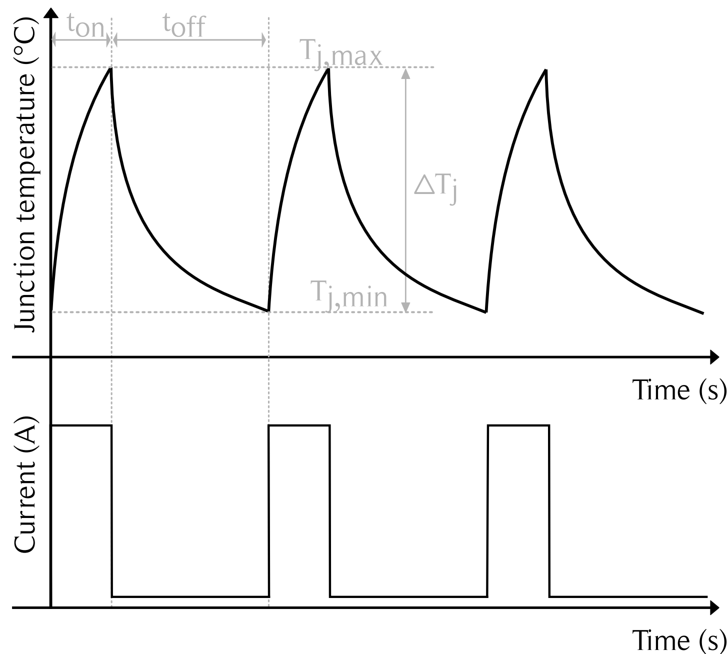


Figure 3.1: Illustrative representation of junction temperature swings created by the pulsating current flowing through the device.

3.3. Devices selection

By simply looking at the webshop of Digi-Key, there are more than 40 000 MOSFETs and IGBTs to choose from. In the next part, the relevant transistor properties are discussed in order to reduce the amount and find suitable devices for the power cycling test.

Manufacturer

Firstly, the manufacturer is important. In order to compare devices and declare possible differences, it is important that the manufacturing process and conditions of the devices are similar. Also, the information in the datasheets has certain criteria that are different per manufacturer. In order to study the datasheets, it is helpful if the same company makes the datasheets.

Price

For this research, we need to break quite some devices for a reliable conclusion. And so it is important to consider the cost of the devices as well.

Voltage rating

To make this research more relevant, it makes sense to choose voltage ranges applicable to the industry. For example, the automotive sector uses often semiconductor devices of 600 and 1200 V [36].

Current rating

The current capability of the device should be large enough to achieve high temperatures during power cycling. At the same time, a very large current rating results often in a larger surface area, to reduce the on resistance and power losses. In this case, more power is extracted from the power cycler to heat up the device. For high current ratings, the devices might be larger and more expensive. Therefore, it will be beneficial to choose a low current rating that can still achieve the desired temperature swing.

Thermal time constant

The measurements should be executed in a quasi-steady state. After a first-order step response, it will take 5τ seconds for the system to reach 99% of the steady state value [37]. So for a small thermal time constant, the steady state is reached faster and the power cycles can be made shorter. τ can be reduced by reducing the thermal capacitance and thermal resistance. So devices with low thermal capacitance and thermal resistance are beneficial.

On-resistance

The internal on-resistance between the drain and source is an important feature of the MOSFETs. The resistance is proportional to the power losses and temperature rise of the device. Although in general a low resistance is popular, for the power cycling test a higher resistance is desired because the high temperatures can be reached faster and with less power drawn from the power cycler. Furthermore, low-resistance devices are often more expensive than those with a higher resistance.

3.3.1. Conclusion

A silicon IGBT with suitable properties was already available in the lab, namely the IKP06N60T [38]. Hence, this device will be used in the experiments. In order to execute a reliable comparison, the properties of the chosen MOSFETs should be in the same range as the IGBTs.

The IGBT is made by Infineon, a trustworthy company, which documents their devices extensively. So it makes sense to choose MOSFETs made by Infineon as well. For the package, the PG-TO247-3 is chosen since it can be easily mounted to the heatsink and power cycler. SiC MOSFETs with the package PG-TO22-3 were not available. The IKP06N60T IGBT has a voltage range up to 600 V. The closest possibility for the silicon-carbide MOSFETs is 650 V.

Applying the above-mentioned decisions to the available silicon-carbide MOSFETs in DigiKey, only eight 650 V MOSFETs remained in stock. The datasheets of those eight MOSFETs are studied and compared based on their on-resistance, thermal resistance, current rating, and price. In the end, the IMW65R107 is chosen since its current rating is the closest to the IGBT, and is the cheapest. All the relevant properties of the IGBT and MOSFET used in the experiments are summarized in Table 3.1.

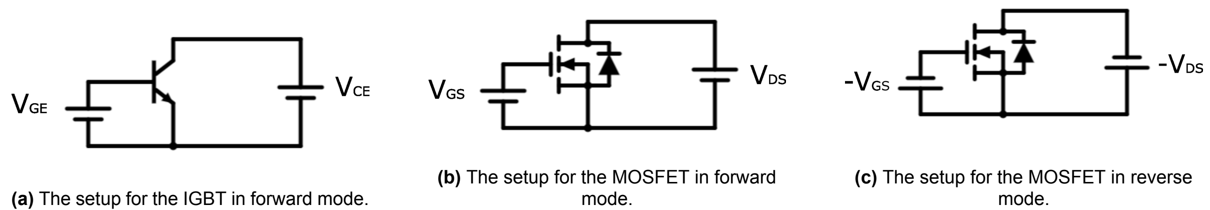
Table 3.1: Summary of the relevant properties of the selected devices for the experiment [38] [39].

Model	Si IGBT IKP06N60T	SiC MOSFET IMW65R107M1H
Package	PG-TO220-3	PG-TO247-3
Voltage rating (V) (collector-emittor or drain-source)	600	650
Continuous DC current (A) at T_{c} = 25 $°C$	12	20
Peak current (A) at T_{c} = 25$°C$	18	48
T_{j} ($°C$)	-40 to 175	-55 to 150
$R_{\text{th (j-c)}}$ (K/W)	1.7	1.6
$R_{\text{ds,on}} (m\Omega)$	-	107
Price (€)	1.85	11.25

3.4. Electrical characteristics analysis

The electrical characteristics analysis is used to study the electrical behavior of the silicon IGBT and silicon-carbide MOSFET. For this test, the IGBT or MOSFET is connected to two power supplies; one power supply will deliver the gate voltage and attract electrons to the channel, and one power supply will be used as a current source to make current flow between the collector and emitter or drain and source. Schematic representations of these setups are presented in Figure 3.2. In the thermal response measurement and power cycling test of the MOSFET, we have to choose if we want to heat up the MOSFET with the channel losses or the body diode, i.e. by apply or a positive or negative heating current [40]. Both setups will be investigated.

During the tests, the voltage and currents of both the power supplies are measured. The results of the electrical characteristics analysis for the IGBT in forward mode and the MOSFET in forward mode and reverse mode are shown in Table A.1. $V_{\text{GE,GS}}$ and $I_{\text{CE,DS}}$ are set at various values in this experiment, and the limits for $I_{\text{GE,GS}}$ and $V_{\text{CE,DS}}$ are set to 0.5 A and 5 V, respectively. During the experiments, only small $I_{\text{CE,DS}}$ currents are applied for a short period of time since the devices are not connected to a heatsink, and overheating of the devices has to be prevented. For applying negative voltages to the semiconductors, the output cables of the power supply are switched. The IGBT needs a large gate



(a) The setup for the IGBT in forward mode.

(b) The setup for the MOSFET in forward mode.

(c) The setup for the MOSFET in reverse mode.

Figure 3.2: Schematic representation of the setup for the electrical characteristics analysis.

voltage (of at least 6 V) to attract charge carriers to the channel and operate in saturation mode. It was found that the MOSFET needs a large gate voltage (of at least 8 V) before it turns on due to built-in protection. This prevents the MOSFET from operating in the saturation region. Increasing the gate voltage will increase the conductance of the channel and therefore decrease the drain-source voltage and decrease the power losses. When increasing the collector-emitter or drain-source current, the voltage over the device increases as well. The reverse mode of the MOSFET has a higher voltage drop, since it is the body diode that is conducting, and consequently larger power losses than the forward mode of the MOSFET. In all cases, the leakage current was smaller than 0.01 μA.

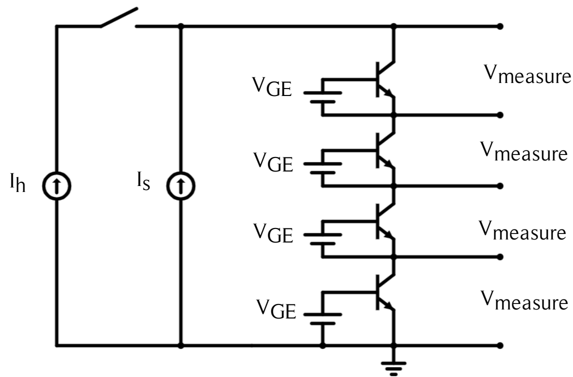
3.5. Set-up thermal response measurement and power cycling test

The electronic circuit is based on the test setups found in literature and expanded to four devices in series [8], [15]. The electric circuit of the IGBT test is shown in Figure 3.3a. I_{h} indicates the pulsating current that will heat up the device. I_{s} is a small bias current that flows continuously through the IGBT to keep the IGBT in forward-biased mode, such that the voltage drop can be measured to determine the junction temperature. V_{GE} is the gate-emitter voltage and V_{measure} is the collector-emitter voltage drop, which is measured for each device.

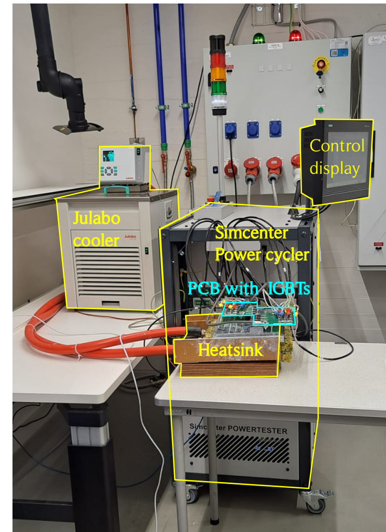
The setup of the experiments is shown in Figure 3.3b. First off, the *Simcenter power cycler* is used to provide the gate voltage and heating power to heat up the semiconductors and is also used to measure the voltage drop between the collector and emitter or drain and source. Secondly, the *Julabo cooler* is used to control the temperature of the *heatsink* and together are used to cool down the semiconductors. A predesigned PCB is used to electrically connect the semiconductors to the *Simcenter power cycler* by screwing the cables to the PCB and soldering the semiconductors onto the PCB. The semiconductors can be fixed onto the heatsink with screws. Between the MOSFETs and the heatsink another layer should be added to provide electric isolation. Between the IGBTs and heatsink a similar layer is added, to provide an equal test situation and to fill the air gaps.In the first weeks of the experiments, a thermal paste was used. However, the thermal paste varied in thickness and as a result, the thermal response and thermal resistance varied between the four samples. By using thermal pads and a torque screwdriver, the problem was solved. Another benefit was that the thermal pads are less messy to work with.

In most applications, the IGBTs operate in the saturation region, such that the forward voltage is low and the power losses are small. The gate voltage will be adjusted to reach the saturation mode. During the cooling phase, the voltage over the diode is used to calculate the junction temperatures. During the heating phase, the on-voltage is measured and the electrical resistance of the channel is calculated.

The direction of the diode of the MOSFET is reversed in comparison to the diode of the IGBT, i.e. from source to drain. Therefore, a negative sensing current is needed to measure the voltage over the diode and calculate the junction temperatures during the cooling phase. There are two possible methods to heat up the MOSFET; we can apply a positive heating current through the MOSFET channel and measure the on-voltage, or we can apply a negative heating current through the body diode and measure the voltage over the diode [40]. When heating the MOSFET in forward mode, the threshold voltage of the SiC MOSFET can be unstable and will influence the measurements of the on-voltage and thermal resistance [3], [9]. Furthermore, the voltage over the four samples in series required to achieve enough heating power using this method, is higher than the voltage the *power cycling machine*



(a) Schematic representation of the test setup.



(b) Picture of the setup between the semiconductors, heatsink, Julabo cooler and Simcenter power cycler.

Figure 3.3: The power cycling setup.

can provide. Therefore, the body diode is used to heat up the whole MOSFET, also because it has the larger losses at a specific current and therefore the required heating current is lower. However, when the gate-to-source voltage would be 0 V, and the voltage drop over the body diode increased, the channel of the MOSFET will start to partially conduct. By applying a negative gate voltage, the channel is kept closed and the effect of the threshold voltage shift is eliminated [3]. Therefore, in the setup, the positive side of the power source is connected to the source, and the negative side to the drain. This is in contrast to the IGBT and the standard connection of the MOSFET.

3.6. Device calibration

The junction temperature swing can not directly be measured accurately, so the voltage drop between the collector and emitter of the IGBT or the voltage drop between the drain and source of the MOSFET is used, since these voltages are sensitive to temperature changes. During the calibration, the exact relationship between the junction temperature and the collector-emitter voltage drop is established.

During the calibration, the heatsink itself is heated and can easily be measured with a Pt-100 thermal resistor. At the set temperature point, the heatsink is stabilized with fluctuations smaller than 0.01 °C. By waiting for at least five minutes, the layers of the semiconductor device will reach the same temperature as the heatsink and the voltage drop can be measured until a stabilized value is found. Repeating this process for different temperature points will determine the relationship between the junction temperature and the measured voltage drop. Based on the obtained data, a linear relation is established. Every time the devices are mounted on the setup, the calibration procedure will be repeated.

The calibration was executed at heatsink and junction temperatures of $20, 35, 50, 65$ and 80 °C. The bias current will be set to 100 mA such that it is large enough to measure the voltage drop accurately and the increase in temperature can be neglected. The gate voltage is set to 15 V for the IGBT and -2.8 V for the MOSFET.

At 20 °C the measured collector-emitter voltage for the IGBT in saturation mode was 0.71 V and for the MOSFET in body diode mode the drain-source voltage was -2.69 V. The voltage fluctuations are less than 4 mV. Based on the voltage measurements at the different temperatures, a linear curve is matched with the slope as K-factor and an offset at V = 0 V. The voltage equation can then be rewritten to a junction temperature equation. Table 3.2 shows the values for the first four IGBTs and four MOSFETs. The graph obtained during the calibration of the IGBTs and MOSFETs is shown in Figure 3.4.

Table 3.2: The K-factor, offset of the voltage and temperature equation obtained during the calibration.

Sample	K-factor (mV/°C)	Offset (V)	Temperature equation (°C)
IGBT ch1.1	-3.721	0.789	$212.1 - 267.8 \cdot V$
IGBT ch1.2	-3.354	0.778	$232.0 - 298.2 \cdot V$
IGBT ch1.3	-3.761	0.790	$209.9 - 265.9 \cdot V$
IGBT ch1.4	-3.720	0.790	$212.2 - 268.8 \cdot V$
MOSFET ch2.1	2.796	-2.748	$982.6 + 357.6 \cdot V$
MOSFET ch2.2	2.791	-2.737	$980.7 + 358.3 \cdot V$
MOSFET ch2.3	2.817	-2.743	$973.9 + 355.0 \cdot V$
MOSFET ch2.4	2.830	-2.745	$970.0 + 353.3 \cdot V$

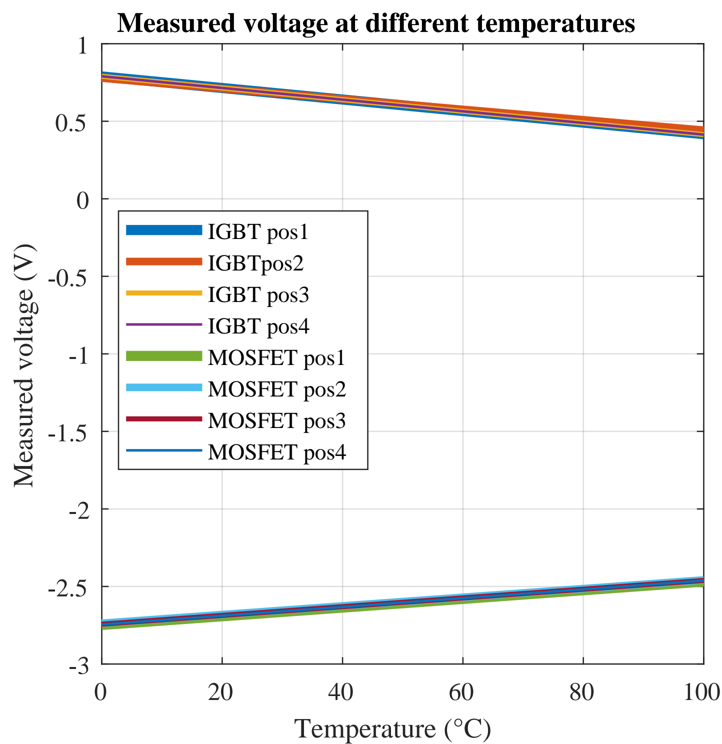
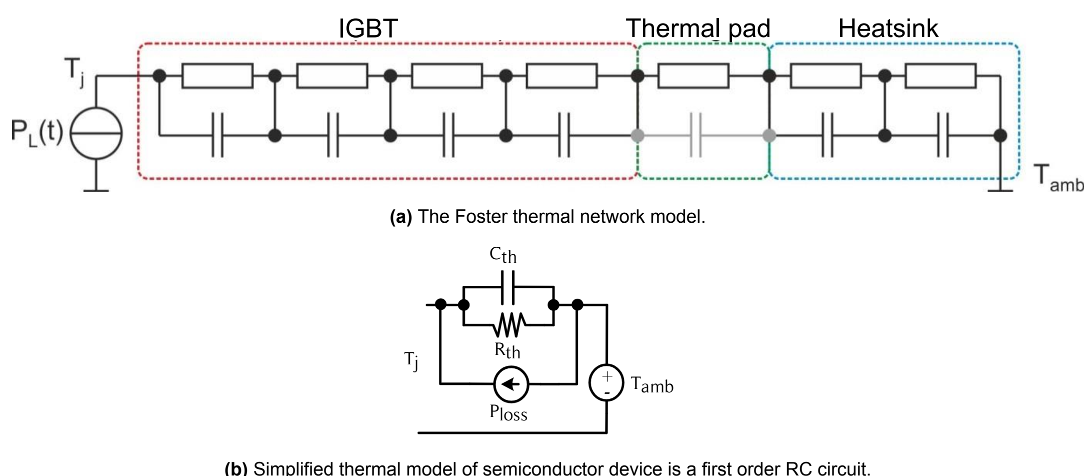


Figure 3.4: The results of the measured voltage during the calibration and the linear interpolation.

4 Thermal model of semiconductor device

Semiconductor devices are made of layers with different thermal behavior. In the Foster model shown in 4.1a, each layer is represented by a thermal resistance and thermal capacitance to model the thermal behavior. Additionally, the thermal pad and heatsink will influence the heat transfer and thermal behavior of the system. In order to process the results of the power cycling test, we first need to study the thermal behavior of the samples and test setup. In this chapter, we will first derive the thermal equations for a first-order system. Subsequently, the thermal response measurements are executed for the silicon IGBT with serial number IKP06N60T and the silicon-carbide MOSFET with serial number IMW65R107M1H. The results for different heating currents are discussed. The thermal response measurements are also used to calculate the cumulative structure function, Cauer thermal model, and time constant spectrum. Lastly, the thermal response measurement is executed for different thermal interface materials and heatsink temperatures, in order to identify the different layers in the cumulative structure function.



(a) The Foster thermal network model.

(b) Simplified thermal model of semiconductor device is a first order RC circuit.

Figure 4.1: Equivalent thermal circuits of the semiconductor devices and test setup. .

4.1. Thermal equations

The Foster thermal network model of the system can be simplified to a first-order RC circuit as shown in Fig. 4.1b. For this first-order RC circuit, the thermal equation is given in (4.1) [41]. By taking the Laplace transform of (4.1) and rewriting this equation, we can solve for $T_{\text{j}}(s)$ as shown in (4.2). Converting back to the time domain and substituting $P_{\text{loss}} = I_{\text{h}}^2 \cdot R_{\text{ce}}$ and $R_{\text{th}}C_{\text{th}} = \tau$, we find the expression shown in (4.3).

$$T_j(t) - T_{amb} = P_{loss} \cdot Z_{th} \tag{4.1}$$

$$T_j(s) - T_{amb} = \frac{P_{loss}}{s} \cdot \frac{R_{th} \cdot \frac{1}{sC_{th}}}{R_{th} + \frac{1}{sC_{th}}} = \frac{P_{loss}}{s} \cdot R_{th} \cdot \frac{\frac{1}{R_{th}C_{th}}}{s + \frac{1}{R_{th}C_{th}}} \tag{4.2}$$

$$T_j(t) - T_{amb} = I_h^2 \cdot R_{ce} \cdot R_{th} \cdot (1 - e^{\frac{-t}{\tau}}) \tag{4.3}$$

Lastly, the heating equation of (4.4) is derived when taking care of the boundary conditions that $T_j(t = \infty) = T_{amb} + I_h^2 R_{ce} R_{th}$ and $T_j(t = 0) = T_j(t_0)$. For the cooling equation, (4.5), the boundary conditions are $T_j(t = \infty) = T_{amb}$ and $T_j(t = 0) = T_j(t_0)$.

$$\text{Heating: } T_j(t) = (R_{th} I_h^2 R_{ce} - T_j(t_0) + T_{amb})(1 - e^{\frac{-(t-t_0)}{\tau}}) + T_j(t_0) \tag{4.4}$$

$$\text{Cooling: } T_j(t) = T_{amb} + (T_j(t_0) - T_{amb}) e^{\frac{-(t-t_0)}{\tau}} \tag{4.5}$$

The thermo-mechanical stresses are strongly related to the thermal cycles. The thermal cycles are represented by the minimum junction temperature $T_{j,min}$, maximum junction temperature $T_{j,max}$ and the junction temperature swing $\Delta T_j = T_{j,max} - T_{j,min}$. Equation (4.4) and (4.5) can now be rewritten to (4.6), (4.7) and (4.8).

$$T_{j,min} = T_{hs} + (T_{j,max} - T_{hs})(e^{\frac{-t_{off}}{\tau}}) \tag{4.6}$$

$$T_{j,max} = (R_{th} I_h^2 R_{ce} - T_{j,min} + T_{hs})(1 - e^{\frac{-t_{on}}{\tau}}) + T_{j,min} \tag{4.7}$$

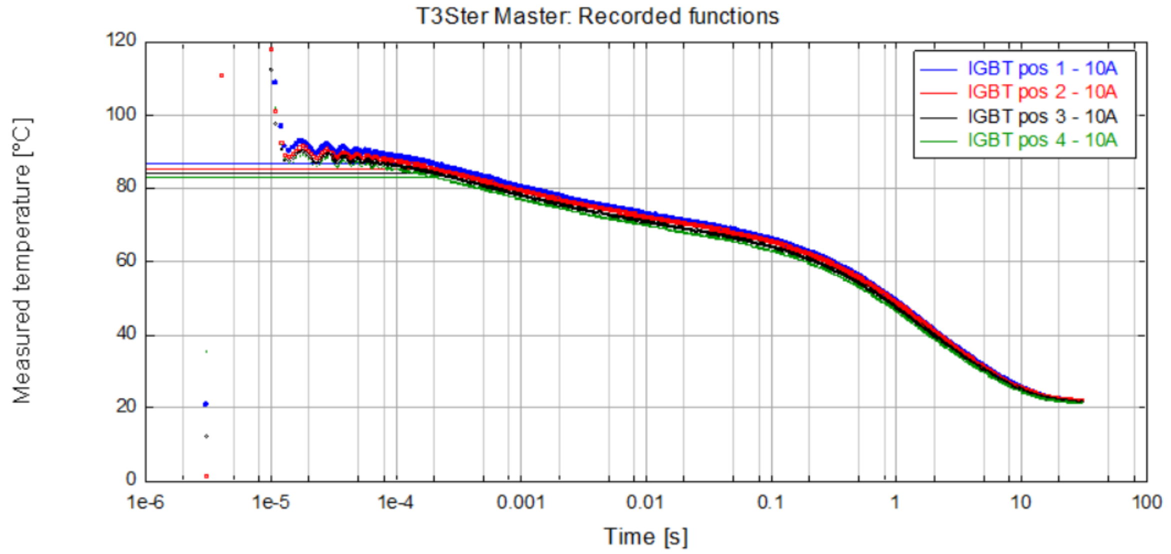
$$\Delta T_j = (R_{th} I_h^2 R_{ce} - T_{j,min} + T_{hs})(1 - e^{\frac{-t_{on}}{\tau}}) \tag{4.8}$$

Herein, $T_j(t)$ is the junction temperature at time t. $T_j(t_0)$ is the junction temperature at time t_0. T_{hs} is the temperature of the heatsink, which can be controlled to implement passive thermal cycles on the test samples. T_{amb} is the ambient temperature, which in this setup is the same as the heatsink temperature. I_h is the heating current. R_{ce} is the electrical resistance between the collector and the emitter. τ is the thermal time constant of the system and is equal to $R_{th} \cdot C_{th}$ where R_{th} is the thermal resistance from junction to ambient and C_{th} is the thermal capacitance from junction to ambient.

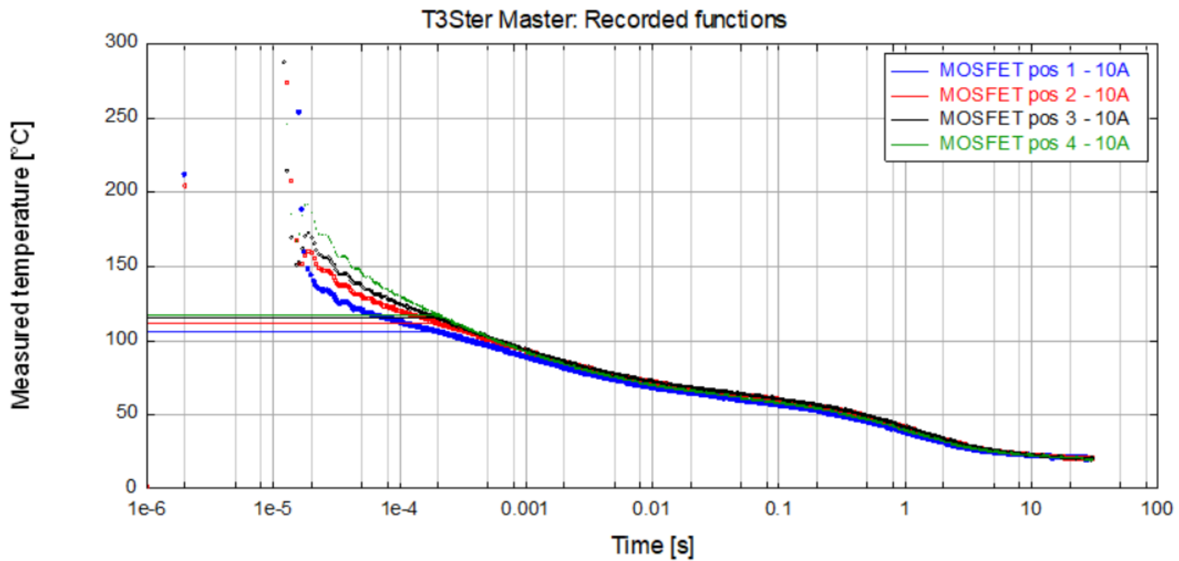
4.2. Thermal response measurement

The first test results I want to discuss are the thermal response measurements of the IGBT and MOSFET and their corresponding cumulative structure functions. In this test, the heating current I_h is set at 10 A, the heating time t_{on} is set to 10 seconds, the cooling time t_{off} is set to 30 seconds, and the heatsink temperature T_{hs} is set to $20\ ^\circ$C.

Figure 4.2a presents the results of the thermal response measurement of the IGBT. The results of the MOSFETs are presented in Figure 4.2b. The graphs show the junction temperature during the cooling phase. The thermal response measurement for the different positions are almost identical, they all have the same shape but the start temperature can vary a little. For the IGBT, in position 1 is $4\ ^\circ$C warmer than in position 4. For the MOSFET, position 4 has the highest start temperature and is $10\ ^\circ$C warmer than position 1. However, position 4 also cools down faster, and after 10 s the temperature of positions 1 and 4 are both $22\ ^\circ$C.



(a) The thermal response measurement for the four IGBTs.



(b) The thermal response measurement for the four MOSFETs.

Figure 4.2: The thermal response measurement for the IGBTs and MOSFETs. During the test, $I_{\text{h}} = 10\text{A}$ $t_{\text{on}} = 10\text{s}$, $t_{\text{off}} = 30\text{s}$ and $T_{\text{hs}} = 20°\text{C}$

The cumulative structure function is a graphical representation of the Cauer thermal network, where each new layer will change the slope of the graph [42]–[44]. The structure function is calculated from the thermal response measurement of Figure 4.2a. These measurements show faulty values before 10μs and some oscillation between 10 to 100 μs. The noise will likely be present during the whole experiment but due to the logarithmic scale only be visible at the first few μs. The period of the oscillation is 10 μs and has therefore a frequency of 100 kHz.

For the transient correction of the measurement, the minimum seek method is used, where the measured points before the start boundary are replaced by the value of the value at the start boundary. The start boundary is placed at 200 μs for both the IGBT and MOSFET. The stop boundary could also be moved but this did not influence the calculation of the cumulative structure function. The stop boundary was set at 10 s.

The cumulative structure functions corresponding to the previous thermal response measurement are

presented in Figure 4.3 for the four IGBTs and Figure 4.4 for the four MOSFETs. Since the thermal response measurements of the samples have the same shape, the cumulative structure functions are also almost identical. Only the temperature of the four IGBTs varied by $4°$C, which results that the thermal resistance from the junction to the ambient of position 1 being 0.11 K/W higher than position 4. The thermal resistance of the four MOSFETs varies more than the IGBTs. The thermal resistance from junction to ambient of MOSFET position 4 is 0.28 K/W higher than position 1.

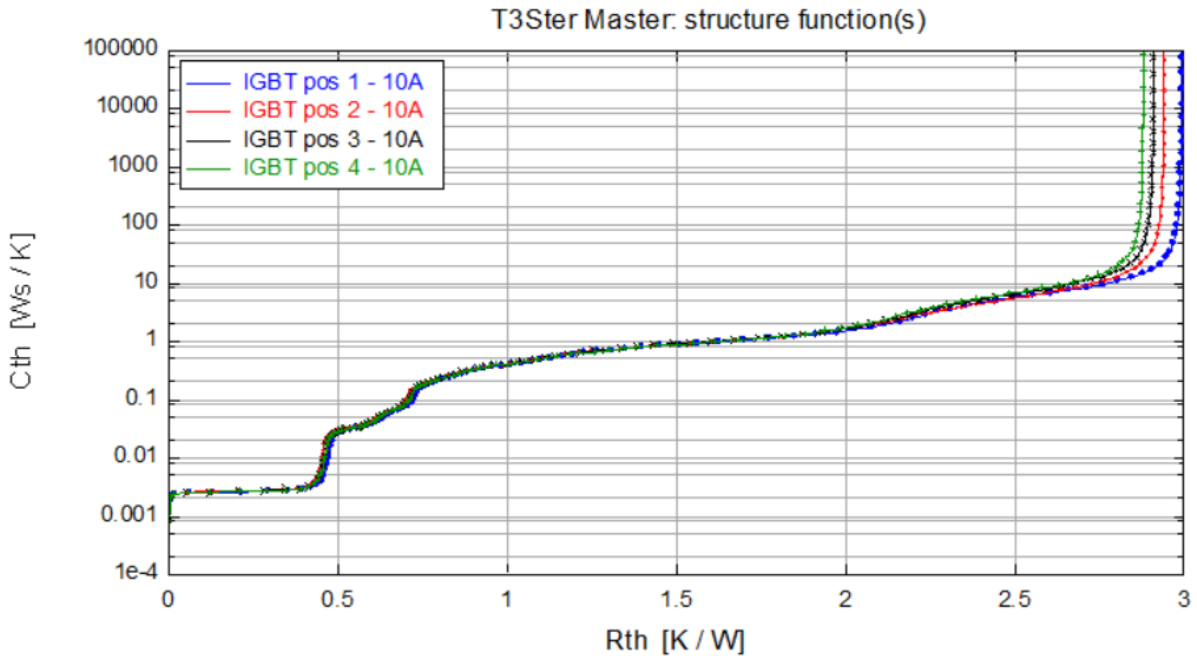


Figure 4.3: The cumulative structure function for the four IGBTs.

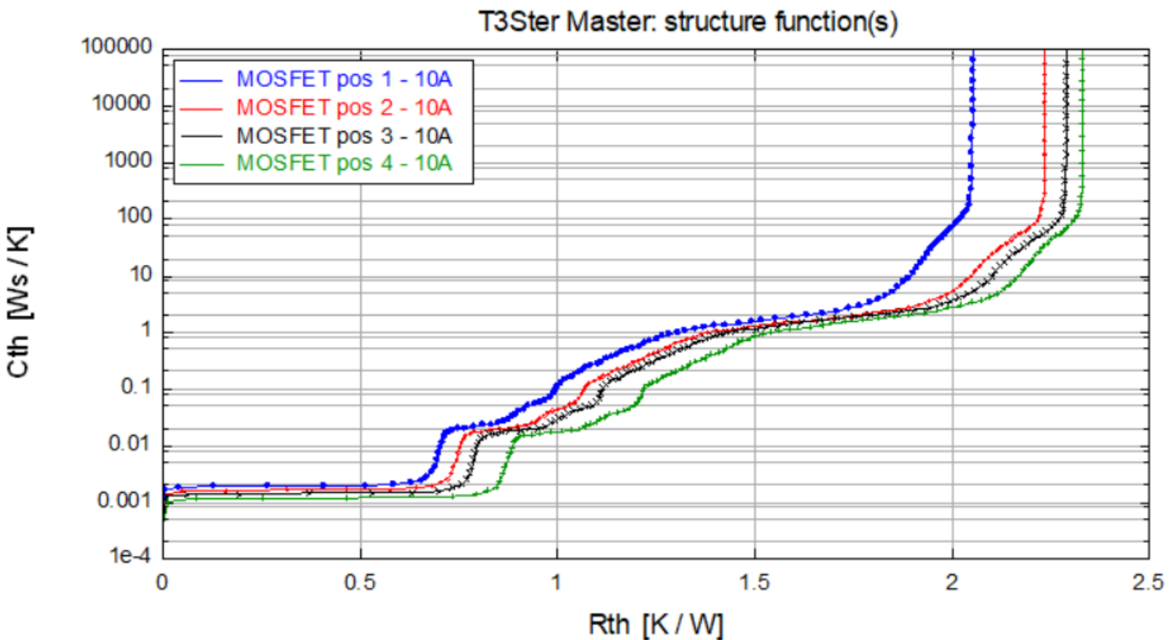
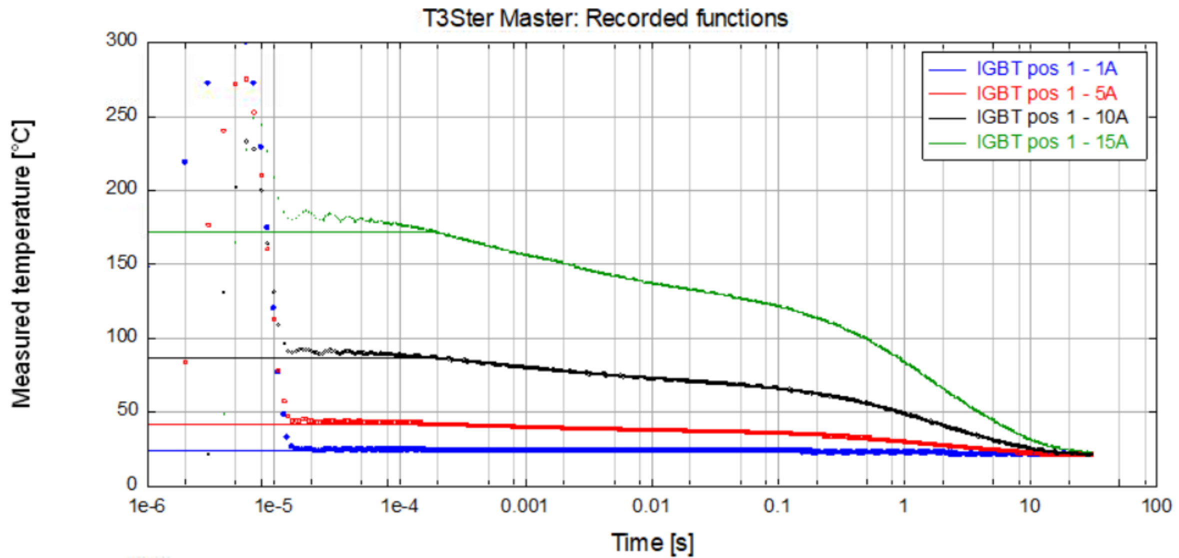


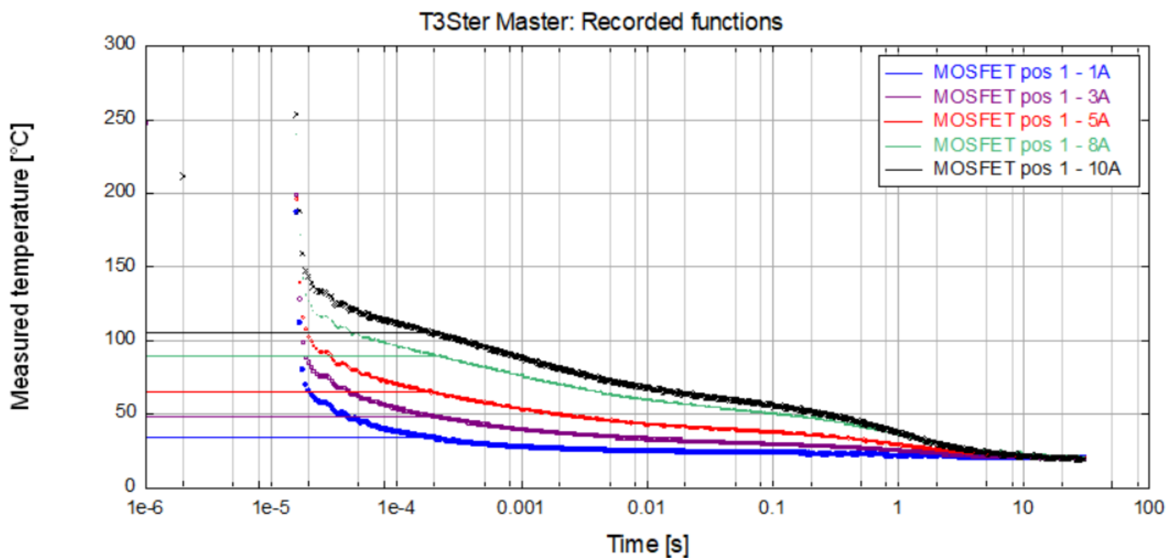
Figure 4.4: The cumulative structure function for the four MOSFETs.

4.2.1. Varying heating current

In the next test, the thermal response measurement is repeated for different heating currents. The other parameters are kept the same, so the heating time t_{on} is set to 10 seconds, the cooling time t_{off} is set to 30 seconds, and the heatsink temperature T_{hs} is set to $20\ ^\circ$C. The results are presented in Figure 4.5 for the first position of the IGBT and MOSFET. The graphs for the other positions are given in Appedix B, as well as their corresponding structure functions and time constant spectrum. The variation of the heating current will affect the structure function, especially for the MOSFET. The measurements with the lowest heating current have the highest thermal resistance from junction to ambient. When the heating current is low, the thermal transient is low and the effect of the electrical transient might dominate the behavior.



(a) The thermal response measurement of the IGBT in position 1.



(b) The thermal response measurement of the MOSFET in position 1.

Figure 4.5: The thermal response measurement for different heating currents. $t_{\text{on}} = 10$ s, $t_{\text{off}} = 30$ s and $T_{\text{hs}} = 20°$C

The graphs show that the higher the heating current, the higher the junction temperature, which matches the expectations from the equations. For the same current, the IGBT is heated up more than the MOS-

FET. This makes sense since the conduction losses for the IGBT are higher because of the diode and also the thermal resistance of the IGBT is 0.1 K/W higher according to the datasheets. The MOSFETs are cooled down to $22°$C in 10 seconds while the IGBTs need 25 seconds to reach $22°$C and the green curve only reached $23°$C in 30 seconds.

4.3. Cumulative structure function

For the comparison of the cumulative structure function of the IGBT and MOSFET, the results of the thermal response measurement with a heating current of 10 A are used. Figure 4.6 presents the cumulative structure function of the IGBT and MOSFET in one figure. When looking closely at the graphs, we can see some similarities in the shape of the graphs. Both graphs make almost the same five steps. The biggest difference is the width of each step, corresponding to the thermal resistance of that layer. The total thermal resistance from junction to ambient is indicated by the end of the graph. For the IGBT the junction to ambient thermal resistance is 2.99 K/W, while for the MOSFET this is 2.05 K/W. A higher thermal resistance means that the device is heated up more, which was also observed during the thermal response measurement. Both values of the thermal resistance are much higher than the values for the junction to case thermal resistance from the datasheet, namely 1.7 K/W for the IGBT and 1.6 K/W for the MOSFET [38], [39]. Notice that the datasheet only gives the thermal resistance from the junction to the case and that the thermal resistance from the thermal pad and heatsink should be added. The package of the MOSFET has a metal background that makes it easier to transfer heat, while the IGBT has a fully plastic package corresponding to the higher thermal resistance.

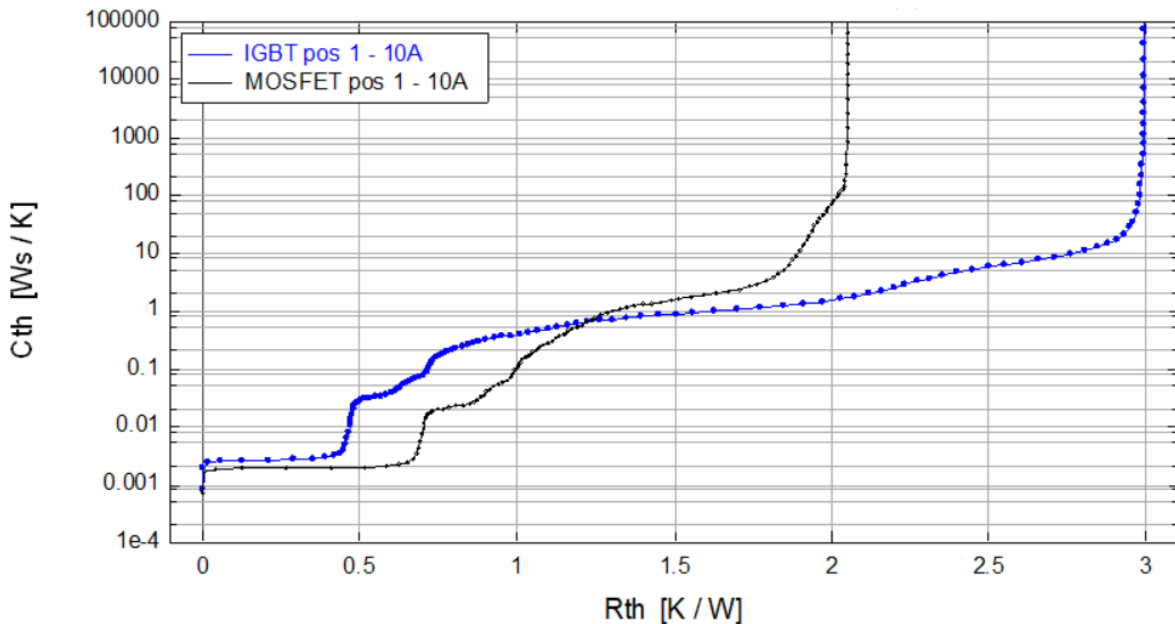


Figure 4.6: The cumulative structure function of the IGBT and MOSFET in position 1 with the heating current of 10 A.

4.4. Cauer model

Since the structure function is the sum of all the thermal resistance and thermal capacitance, we can use it to determine the values of the Cauer thermal network in Figure 4.7. At each time the graph changes its slope, a new layer is starting [42]. The graphs for the IGBT and MOSFET have five steps, consequently, I expect that there are five layers. The width and height of each step are measured to obtain the thermal resistance and thermal capacitance, respectively. Furthermore, the thermal time constant is calculated by multiplying the two values. Table 4.1 summarizes the finding for one IGBT and one MOSFET based on the structure function of Figure 4.6. In total, the IGBT has the largest thermal resistance but for the first and second layers, the thermal resistance of the MOSFET is larger. Since the heatsink is actively cooled and has a fixed temperature, the thermal capacitance will approach infinity.

There is also an effect of this visible on the fourth and fifth layers since their thermal capacitance is higher than expected from the datasheet. This also resulted in a very large thermal time constant.

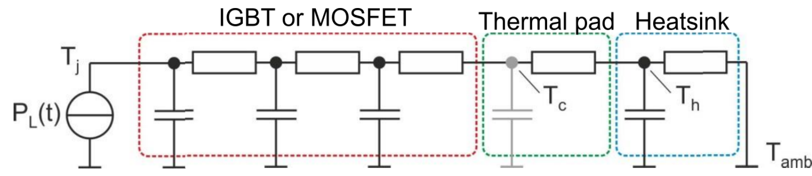


Figure 4.7: Cauer thermal network.

Table 4.1: The values of the thermal resistance and thermal capacitance of the Cauer network.

Layer	IGBT			MOSFET		
	R_{th} (K/W)	C_{th} (Ws/K)	τ (s)	R_{th} (K/W)	C_{th} (Ws/K)	τ (s)
1	0.481	0.0289	0.0139	0.7008	0.0188	0.0132
2	0.1297	0.0331	0.0043	0.1743	0.0274	0.0048
3	0.1339	0.1945	0.0260	0.122	0.1083	0.0132
4	1.163	1.134	1.3188	0.652	1.877	1.2238
5	1.084	19.14	20.748	0.3975	139.9	55.610
Total	2.9916	20.53	22.111	2.0466	141.9	56.87

4.5. Time constant spectrum

Each element in the RC Cauer thermal network has a corresponding time constant. The discrete values of the time constant and thermal resistance are substituted in the time constant spectrum [26], [45]. The T3Ster Master software from Simcenter [35] calculates the time constant spectrum and the results based on the thermal response measurements of position 1 with a heating current of 10 A are shown in Figure 4.8. The x-coordinates show the values of the time constants and on the y-axis is the corresponding thermal resistance value [26]. In appendix section B.3 the time constant spectrums of the other positions for the experiment with a heating current of 10 A are given as well as the time constant spectrum for position 1 for different heating currents.

Both the IGBT and MOSFET show five peaks, corresponding to the five steps/layers we observed in the cumulative structure function. The x coordinates of the peaks are not identical for the IGBT and MOSFET, indicating the difference in their time constant. The last peak of the IGBT is way higher than the peak of the MOSFET, meaning that there the thermal resistance of that layer is much larger. In the first layer, the thermal resistance of the MOSFET is larger than that of the IGBT. The values of the time constant and thermal resistance are read from the graph and presented in Table 4.2.

Table 4.2: The values of the time constant and time constant intensity for the IGBT and MOSFET.

IGBT		MOSFET	
Time constant (ms)	Time constant intensity (K/W)	Time constant (ms)	Time constant intensity (K/W)
1.14	1.08	1.17	1.34
7.79	0.22	6.30	0.30
89.8	0.14	47.3	0.12
994	0.98	1270	0.83
5630	3.30	7090	0.76

4.6. Layer identification

We can already see from the structure function that the steps have different thermal resistances. The insulation layer and thermal paste will have a larger thermal resistance and are therefore shown as a wider region. The heatsink is actively cooled and the thermal capacitance will approach infinity. In order

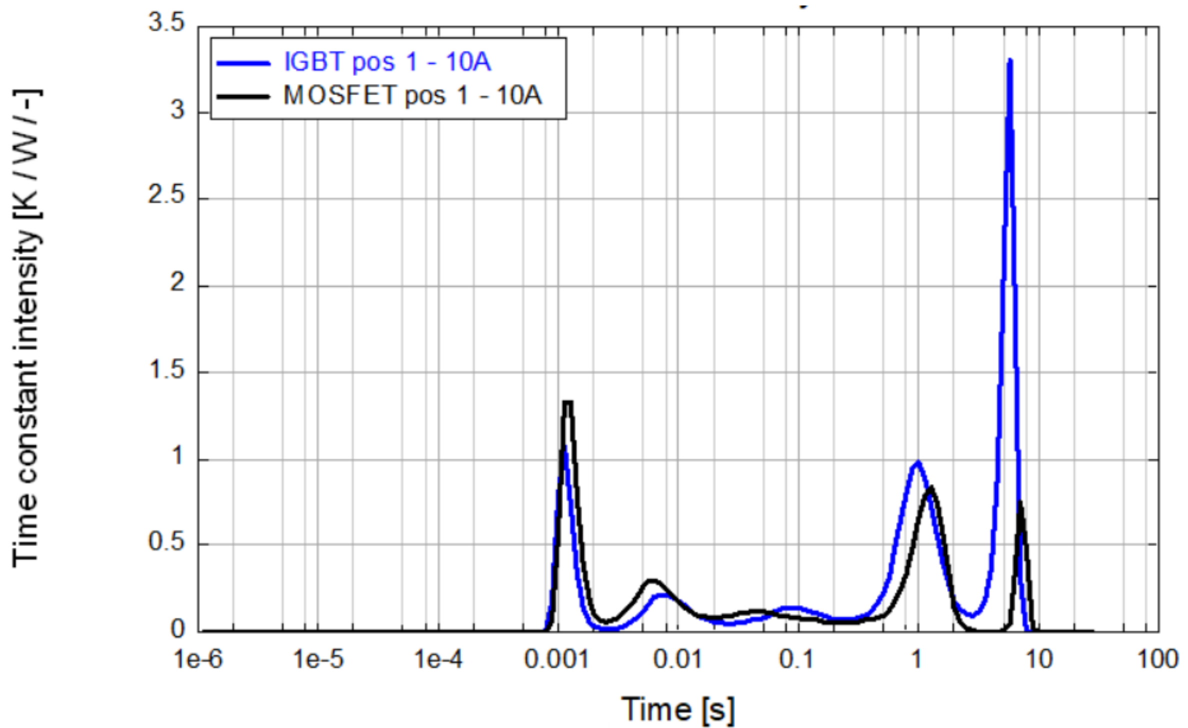


Figure 4.8: The time constant spectrum of the IGBT and MOSFET in position 1 based on the thermal response measurements with a heating current of 10 A.

to require more information about the layers, thermal response measurements in different situations are executed and their structure functions are compared.

4.6.1. Thermal interface material

Two tests are executed, one with thermal paste and one without thermal paste in order to find out where the last layer of the semiconductor and the layer of the thermal interface are. During the test, the heating current was 1 A, the heating time was 25 s and the cooling time was 30 s. Between the tests, the IGBTs need to be removed from the heatsink to apply the thermal paste and the system needs to be calibrated again. Figure 4.9 shows the thermal response and cumulative structure function of the experiments with and without thermal paste between the IGBTs and heatsink. The structure function shows clearly that the thermal path overlaps until 1.5 K/W and then splits up. Therefore, at 1.5 K/W, the IGBT package ends and the thermal interface layer and heatsink will start. As expected, the thermal paste will reduce the thermal resistance from case to ambient by 0.8 K/W. I should note that during the setup of this experiment, the torque wrench was not yet used and this could influence the measurements. The thickness of the thermal paste is dependent on the force applied to the IGBTs and therefore the thermal resistance of the thermal paste can vary.

4.6.2. Heatsink

The goal of the following experiments is to determine where the layer of the heatsink is. The heatsink is the last layer so it should correspond to the last part of the cumulative structure function.

In the first experiment the flow rate and pressure of the Julabo cooler are varied. In stage 1, the pump pressure is 0.4 bar, the suction pump is 0.2 bar and the flow rate is 22 l/min. In stage 4, the pump pressure is 0.7 bar, the suction pump is 0.4 bar and the flow rate is 26 l/min. For the experiment, the heating current is 15 A, the heating time 10 s, cooling time 30 s and the heatsink temperature is $5°$C. The results of the thermal response measurements and the calculation of the cumulative structure function are shown in Figure 4.10. The results are almost identical and little difference could come from inaccuracies in the measurements. Since the heatsink temperature is stable during the experiments, the flow rate and pressure have no effect on the results.

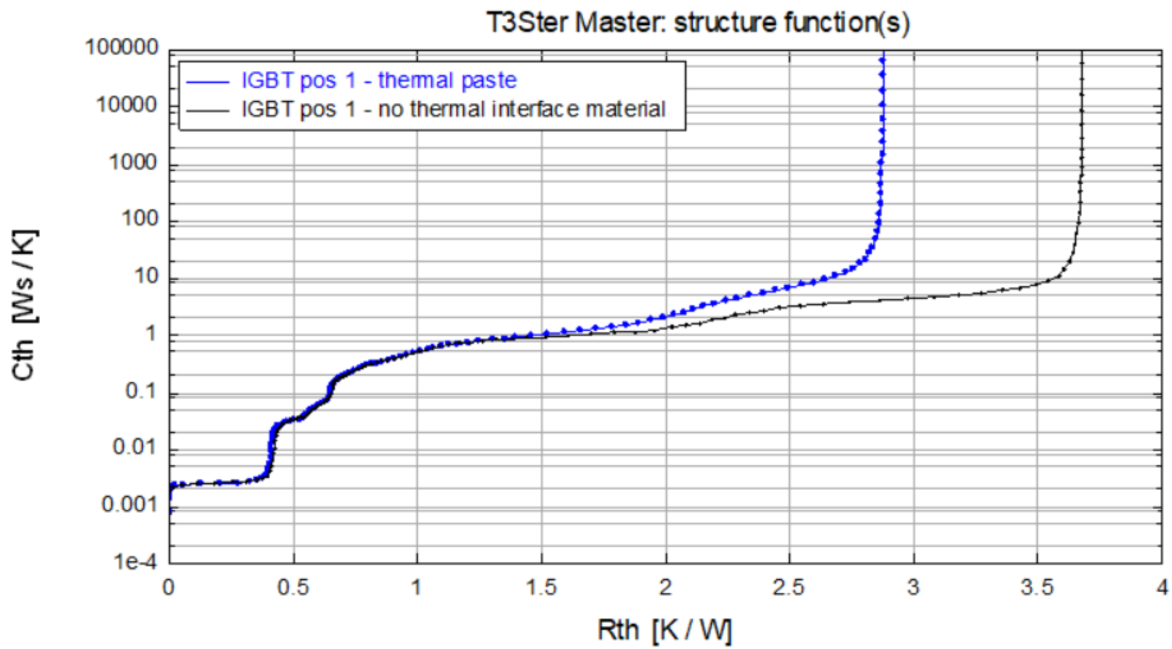


Figure 4.9: The cumulative structure function with and without a thermal paste layer. $I_{\text{h}} = 1$ A $t_{\text{on}} = 25$ s, $t_{\text{off}} = 30$ s and and $T_{\text{hs}} = 20°$C

In the following experiment the temperature of the heatsink itself is varied from 20 °C to 60 °C. During the test, the heating current was 10 A, the heating time 5 s and the cooling time 60 s. Both the thermal response and the structure function for position 1 of the IGBT are shown in Figure 4.11. The thermal response measurement is shifted towards higher temperatures but still has the same shape. Therefore, the structure functions are nearly identical in the two situations. The small differences could come from measurement inaccuracies. Nevertheless, the last part of the graph is shifted to the right, meaning that the thermal resistance of the last layer is increased by 0.1 K/W. The other four samples show the same shift. The assumption is made that around 2.4 K/W the layer corresponding to the heatsink starts.

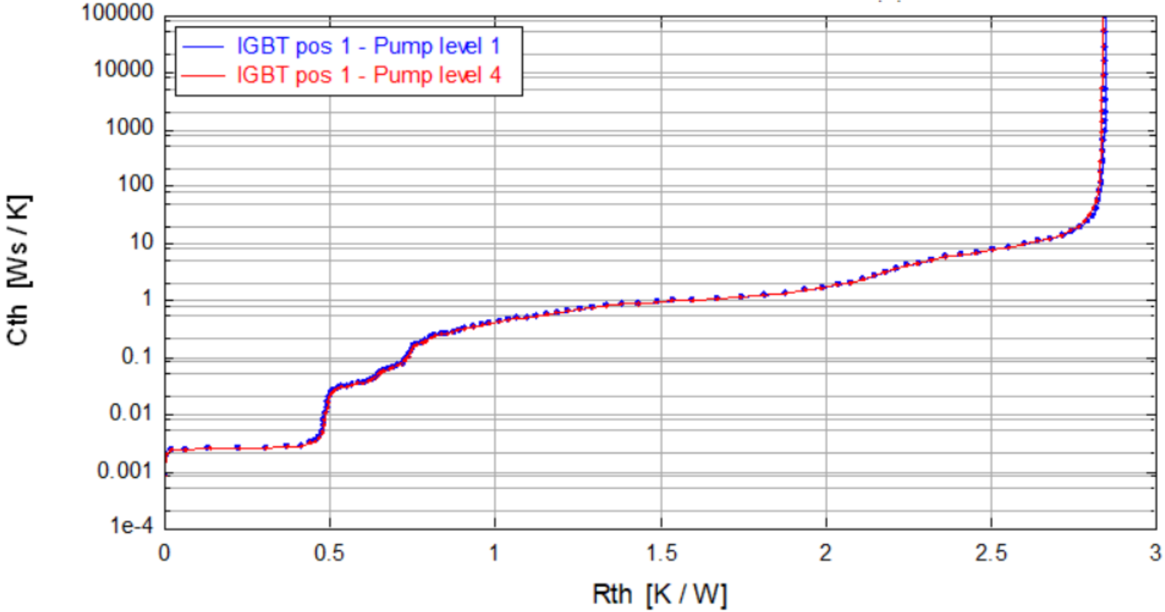


Figure 4.10: The cumulative structure function for different pomp pressures of the Julabo cooler. $I_{\text{h}} = 15$ A $t_{\text{on}} = 10$ s, $t_{\text{off}} = 30$ s and and $T_{\text{hs}} = 20°$C.

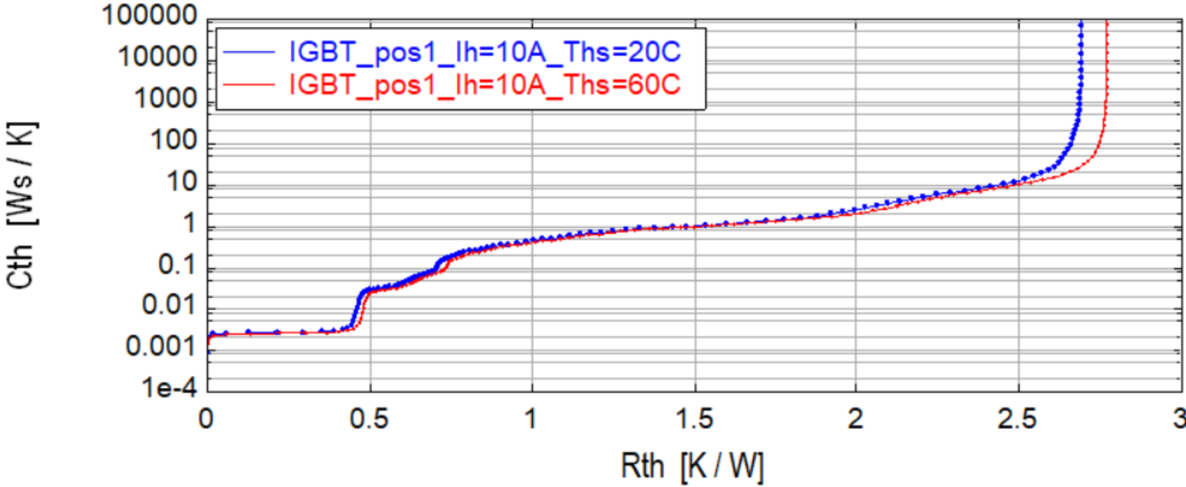


Figure 4.11: The cumulative structure function for different heatsink temperatures. $I_{\text{h}} = 10$ A $t_{\text{on}} = 5$ s and $t_{\text{off}} = 60$ s.

5
Power cycling test

The power cycling test will be used to execute the end-of-life assessment. In this chapter, the influence of the parameters, on the thermal cycle is investigated. Based on the results, the thermal resistance and thermal time constant are determined. Furthermore, the power cycling test is executed for multiple hours until one of the samples breaks. The experiments address points for attention for the maximum heating current and minimum heatsink temperature.

5.1. Parameter dependence

In the power cycling test, we have four parameters that can be selected to achieve the desired temperature cycle. Those are the heating current I_{h}, heating time t_{on}, cooling time t_{off}, and heatsink temperature T_{hs}. Based on the derived thermal model, it is expected that increasing the heating current and heating time will increase the $T_{\text{j,max}}$. Moreover, we expect that increasing the cooling time or decreasing the heatsink temperature will decrease $T_{\text{j,min}}$. The thermal resistance and capacitance are inherent to the IGBTs and can not be changed.

The relation between the selected parameters and the resulting temperature cycle will be studied by repeatedly performing the power cycling test. During the test, the gate-emitter voltage is set to 15 V and the bias current is set to 100 mA. During the measurement, the values of the collector-emitter voltage and corresponding $T_{\text{j,max}}$ and $T_{\text{j,min}}$ are determined. On average, the electrical resistance between the collector and emitter is calculated to be 235 mΩ, but this value depends slightly on the temperature.

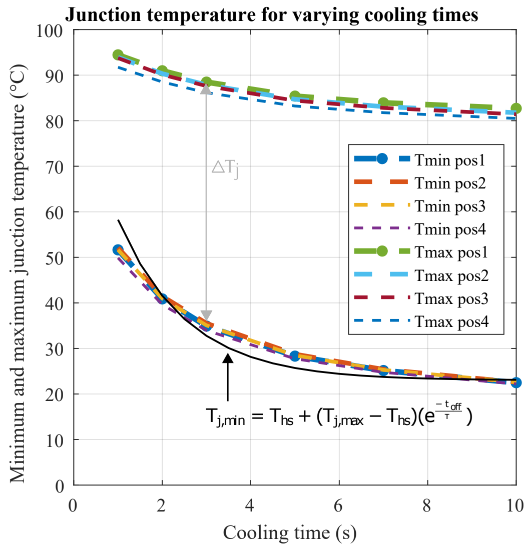
Furthermore, the thermal model is verified and the missing values of the thermal time constant and thermal resistance are determined with the curve fitting tool of MATLAB. The heating equation (4.4) has two unknowns, namely the time constant and the thermal resistance, and results in multiple combinations to the curve fitting, and it's difficult to decide which is practically realistic. Therefore, it makes sense to start with investigating the cooling equation (4.5) since it has only one unknown, namely the time constant. Secondly, the found time constant can be used as a starting point in the curve fitting of the heating equation (4.4) to obtain the thermal resistance. Lastly, the thermal capacitance is calculated according to $C_{\text{th}} = \frac{\tau}{R_{\text{th}}}$.

5.1.1. Cooling time

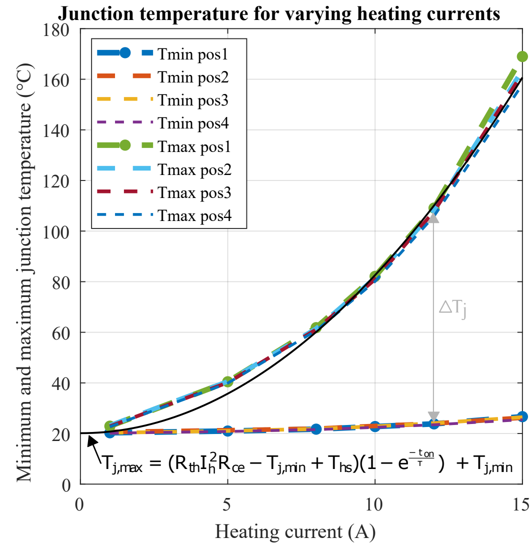
The cooling time only appears in the equation for $T_{\text{j,min}}$ but since $T_{\text{j,max}}$ is strongly dependent on $T_{\text{j,min}}$, both will change by varying the cooling time. The experimental results are shown in Figure 5.1a. For small t_{off}, $T_{\text{j,min}}$ is much larger than the heatsink temperature. Longer t_{off} will lead to a $T_{\text{j,min}}$ close to the heatsink temperature. $T_{\text{j,max}}$ is less impacted by the change of t_{off} but still varies by $12°$C. ΔT is therefore increasing for increasing t_{off} until its maximum is reached.

By fitting the measurement results of Figure 5.1a and (4.6) using the MATLAB curve fitting tool, we can determine the time constant. The results per sample are shown in Table 5.1. The thermal time constant is around 1.6 s. The R^2 and root-mean-square error (RMSE) values indicate the quality of the

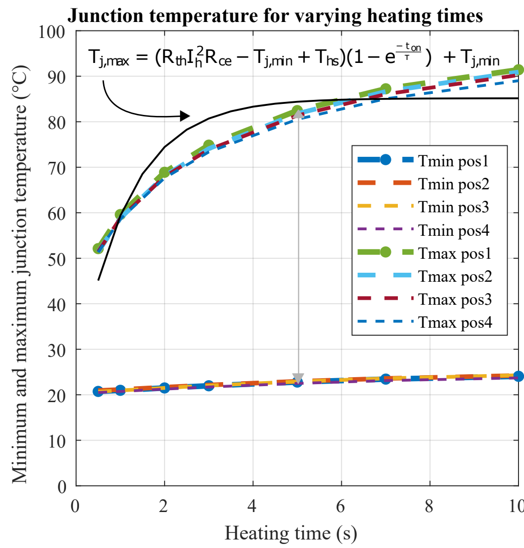
fitted curve. The equation after the curve fitting is also plotted in Figure 5.1a as a black line.



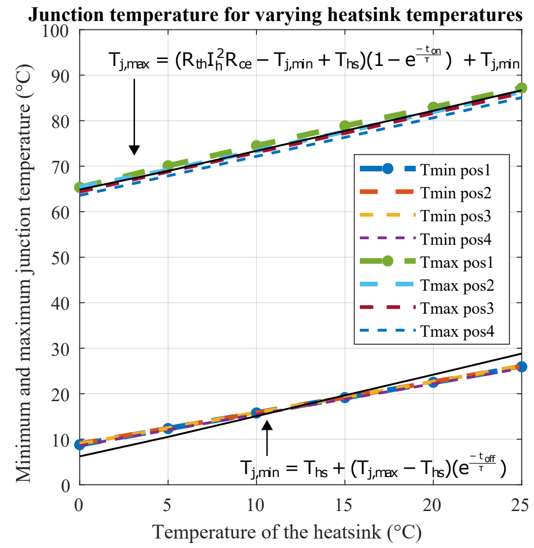
(a) The relation between the cooling time and minimum and maximum junction temperature. During the experiment $I_h = 10$ A, $t_{on} = 5$ s and $T_{hs} = 20^0$C.



(b) The relation between the heating current and minimum and maximum junction temperature. During the experiment $t_{on} = 5$ s, $t_{off} = 10$ s and $T_{hs} = 20°$C.



(c) The relation between the heating time and minimum and maximum junction temperature. During the experiment $I_h = 10$ A, $t_{off} = 10$ s and $T_{hs} = 20°$C.



(d) The relation between the heatsink temperature and minimum and maximum junction temperature. During the experiment $I_h = 10$ A, $t_{on} = 5$ s and $t_{off} = 10$ s.

Figure 5.1: Measurement results of the power cycling test for varying parameters.

Table 5.1: Results for applying the curve fitting on experimental results of Figure 5.1a where the cooling time is varying.

	Pos 1	**Pos 2**	**Pos 3**	**Pos 4**
τ	1.558	1.622	1.586	1.512
R^2	0.7677	0.7642	0.7623	0.7643
RMSE	5.293	5.393	5.33	5.053

5.1.2. Heating current

The power losses inside the device will act as a heating source and can be adjusted by selecting the heating current. The relation between the selected heating current, $T_{j,max}$ and $T_{j,min}$ is presented in

Figure 5.1b. The selection of the heating current has a large impact on $T_{\text{j,max}}$ and increases quadratically, as expected from (4.7). The effect on $T_{\text{j,min}}$ is minimal, in this configuration only $6°$C increase is observed, resulting from the increase in $T_{\text{j,max}}$.

By matching the measured results to equation (4.7), the thermal resistance and capacitance values are found and presented in Table 5.2. Additionally, the R^2 and RMSE values of the fitted curve are presented in this table. The determined values for the thermal resistance and capacitance are higher than those from the datasheet of the IGBT namely $R_{\text{th}} = 1.67$ K/W and $C_{\text{th}} = 0.164$ Ws/K [38]. This might be due to the optimistic values in the datasheet or due to the addition of the thermal pad and heatsink. Since the R^2 value is almost 1, the theoretical expectation from (4.7) represents the measurement results well. The analytic equation, shown in black in Figure 5.1b, starts a little lower than the measurement results and overlaps when applying higher currents.

Table 5.2: Results for applying the curve fitting on experimental results of Figure 5.1b where the heating currents is varying.

	Pos 1	**Pos 2**	**Pos 3**	**Pos 4**
τ **(s)**	2.000	1.756	1.600	1.600
$R_{\text{ce}}(\Omega)$	0.2371	0.218	0.2327	0.2239
R_{th} **(K/W)**	2.965	3.066	2.808	2.846
C_{th} **(Ws/K)**	0.6745	0.5727	0.5698	0.5622
R^2	0.9958	0.9966	0.9971	0.9972
RMSE (K)	4.390	3.803	3.497	3.342

5.1.3. Heating time

In this experiment, the relation between the heating time and junction temperature is tested. The resulting graphs are presented in Figure 5.1c. Increasing t_{on} will increase $T_{\text{j,max}}$ but eventually approaches a maximum. The selection of t_{on} will have a range of $40°$C on $T_{\text{j,max}}$ and $4°$C on $T_{\text{j,min}}$ in this setup.

Matching (4.7) with the measurements resulting in the time constant, thermal resistance, and thermal capacitance as indicated in Table 5.3. Also, the electrical resistance for the best fitting is given, which varies slightly per sample. The found values for the time constant are lower than in the experiments before, and therefore the thermal capacitance is lower as well. The values of the thermal resistance are in the same range as the experiment with the varying heating current. The analytic equation has a larger slope and reaches its asymptote sooner than the measured results.

Table 5.3: Results for applying the curve fitting on experimental results of Figure 5.1c where the heating time is varying.

	Pos 1	**Pos 2**	**Pos 3**	**Pos 4**
τ **(s)**	1.138	1.184	1.148	1.103
$R_{\text{ce}}(\Omega)$	0.2243	0.2304	0.2348	0.2175
R_{th} **(K/W)**	2.909	2.816	2.734	2.898
C_{th} **(Ws/K)**	0.3946	0.4205	0.4199	0.3806
R^2	0.8555	0.8607	0.8560	0.8540
RMSE (K)	6.754	6.670	6.653	6.503

5.1.4. Heatsink temperature

The selection of the heatsink temperature is used to move both $T_{\text{j,min}}$ and $T_{\text{j,max}}$ equally. By fixing the parameter in (4.6) and (4.7), the relation between $T_{\text{j,min}}$ and T_{hs} becomes linear, similar to the relation between $T_{\text{j,min}}$ and T_{hs}. Nevertheless, the slopes are not the same and ΔT_{j} is slightly increasing as T_{hs} increases.

The results of the experiments with varying heatsink temperatures are shown in Figure 5.1d. The x-axis shows the setting of the heatsink temperature, but the practical temperature can vary from the settings. When the semiconductor devices are heating up, the heatsink area under and next to the device will heat up as well. The temperature sensor of the heatsink is placed lower in the aluminum and

will not sense the local temperature fluctuations, the heat should first spread towards the sensor. The air temperature in the room can also have a slight influence on the actual temperature of the heatsink. When fitting equation (4.7) against the measurements results of $T_{\text{j,max}}$, the time constant, electric resistance, thermal resistance and thermal capacitance are found as shown in Table 5.4. The values are simular to the values obtained in the previous experiments. Moreover, the measurement results for $T_{\text{j,min}}$ can be plotted against equation (4.6). The resulting curve fitting parameters are presented in Table 5.5. The curve fitting was improved by measuring the local heatsink temperature next to the IGBT with another temperature sensor instead of using the selected heatsink temperature. Even so, the values of the thermal time constant are doubled compared to previous experiments, which should not be possible since it is the same setup. We expect that the measured heatsink temperature does not correlate to the actual heatsink temperature at the attachment of the devices, and therefore the obtained value of the thermal time constant is inaccurate in this curve fitting.

Table 5.4: The values obtained by curve fitting the experimental results of Figure 5.1d, where the heatsink temperture is varying to the cooling equation (4.7)

	Pos 1	**Pos 2**	**Pos 3**	**Pos 4**
τ **(s)**	1.505	1.500	2.000	1.548
$R_{\text{ce}}\,(\Omega)$	0.2219	0.2200	0.2265	0.2166
R_{th} **(K/W)**	2.885	2.871	2.771	2.854
C_{th} **(Ws/K)**	0.5217	0.5225	0.5734	0.5424
R^2	0.9591	0.9629	0.9736	0.9696
RMSE (K)	1.646	1.963	1.698	1.806

Table 5.5: The values obtained by curve fitting the experimental results of Figure 5.1d where the heatsink temperture is varying to the cooling equation (4.6).

	Pos 1	**Pos 2**	**Pos 3**	**Pos 4**
τ	3.584	3.640	3.652	3.529
R^2	0.893	0.891	0.893	0.889
RMSE	2.091	2.100	2.089	2.117

5.2. Discussion

Each test was used to calculate the thermal time constant and if possible also the electrical resistance, the thermal resistance, and the thermal capacitance. Throughout the tests, the obtained values are not identical, but their average gives a rough estimate of the values. For this system, $\tau = 1.6$ s, $R_{\text{th}} = 2.9$ K/W, $C_{\text{th}} = 0.5$ Ws/K and $R_{\text{ce}} = 220$ mΩ. During each test, the R^2 and RMSE values are good and verify the thermal model. Using the thermal model, a power cycling testbed with the desired temperature swing can be made.

The duration of several power cycling tests can take multiple days to even weeks. Therefore, it is important to consider the cycle time, i.e. $t_{\text{on}} + t_{\text{off}}$ and keep is as low as possible, while obtaining the desired temperature swing. Both the heating current and the heating time can be used to increase $T_{\text{j,max}}$, so it is beneficial to use the heating currents as a free variable over the heating time. Furthermore, the heatsink temperature can be chosen over the cooling time to select $T_{\text{j,min}}$ while keeping the cycle time low.

5.3. Experiment A

In this section, the power cycling test is executed until one of the samples will break. The measured temperature is compared to the expected values from the thermal model. In this experiment, the same samples are used as in previous experiments and the test setup was not changed. Therefore the used samples experienced stressed before the start of this test and the test will not give a relevant lifetime. The goal of the test is to investigate how the power cycling test can be used as an end-of-life

assessment and how to arrive at a testbed for the desired temperature cycle. The test took around 8 hours until one of the test limits was exceeded.

5.3.1. Testbed for experiment A

In this experiment, the desired temperature cycle would be from 25 to 150 °C, such that we stay under the maximum junction temperature of 175 °C. The heatsink temperature was set at 5 °C, such that it is low enough to keep the cooling time small and at the same time the oil in the Julabo cooler has some margin and will not reach negative temperatures. Equation (4.6) can be rewritten to find the cooling time. The calculation is given in (5.1) and results that the cooling time of the experiment being set at 3 s. The heating time is set at 1 s, making sure the semiconductor junction has enough time to heat up. The heating current was set at 20 A, based on the calculations given in (5.2) where (4.7) was rewritten. Based on these settings, the expected junction temperature cycle should be from 27 to 134 °C.

$$t_{\text{off}} = -\tau \cdot \ln \frac{T_{\text{j,min}} - T_{\text{hs}}}{T_{\text{j,max}} - T_{\text{hs}}} = -1.6 \cdot \ln \frac{25 - 5}{150 - 5} = 3.17 \text{ s} \tag{5.1}$$

$$I_{\text{h}} = \sqrt{\frac{\frac{T_{\text{j,max}} - T_{\text{j,min}}}{1 - e^{-\frac{t_{\text{on}}}{\tau}}} + T_{\text{j,min}} - T_{\text{hs}}}{R_{\text{th}} \cdot R_{\text{ce}}}} = \sqrt{\frac{\frac{150-25}{1-e^{-\frac{1}{1.6}}} + 25 - 5}{2.9 \cdot 0.22}} = 21.3 \text{ A} \tag{5.2}$$

Furthermore, the thermal response measurement is executed with a heating current of 20 A, a delay of 30 s, a heating time of 5 s and a cooling time of 60 s. Also, the gate current is measured.

The power cycling test should automatically stop when one of the following limits is exceeded. The limits are established by taking the average value of cycles 31 to 80.

- Min $|V_{\text{on}}| = 95\% = 3.30$ V
- Max $|V_{\text{on}}| = 105\% = 3.65$ V
- Max $\Delta T_{\text{j,}} = 110\% = 116.2$ °C
- Max $T_{\text{j,max}} = 110\% = 150.2$ °C
- Min $\Delta P = 95\% = 66.35$ W
- Min $I_{\text{cycle}} = 95\% = 19.0$ A
- Max $R_{\text{ce}} = 105\% = 181.6$ mΩ

5.3.2. Results of experiment A

The minimum and maximum junction temperature for each cycle are presented in Figure 5.2 and the median values are represented in columns 2 and 3 of Table 5.6. The minimum and maximum junction temperatures are around the expected values of 27 and 134 °C. The junction temperatures of sample 2 are a little higher. Investigation showed that the power losses of position 2 are 1.5 W higher than the other positions.

Table 5.6: The measurement results of the minimum and maximum junction of experiment A where $I_{\text{h}} = 20$ A, $t_{\text{on}} = 1$ s, $t_{\text{off}} = 3$ s and $T_{\text{hs}} = 5$ °C.

	Median values at start		After thermal response measurement		At faulty cycle 5865	
	$T_{\text{j,min}}$(°C)	$T_{\text{j,max}}$(°C)	$T_{\text{j,min}}$(°C)	$T_{\text{j,max}}$(°C)	$T_{\text{j,min}}$(°C)	$T_{\text{j,max}}$(°C)
Sample 1	28.5	134.7	21.2	127.8	-10.0	27.0
Sample 2	34.6	141.7	25.2	126.4	313.4	-3378.0
Sample 3	27.6	130.7	21.0	125.5	3.8	269.7
Sample 4	29.0	133.0	21.7	125.5	3.3	320.6

Before the thermal response measurements, the power cycling is paused and after a set delay of 30 seconds, the thermal response measurement is executed. The cooling phase of the thermal response measurement is 60 seconds, giving the device enough time to cool down. Therefore, in the power

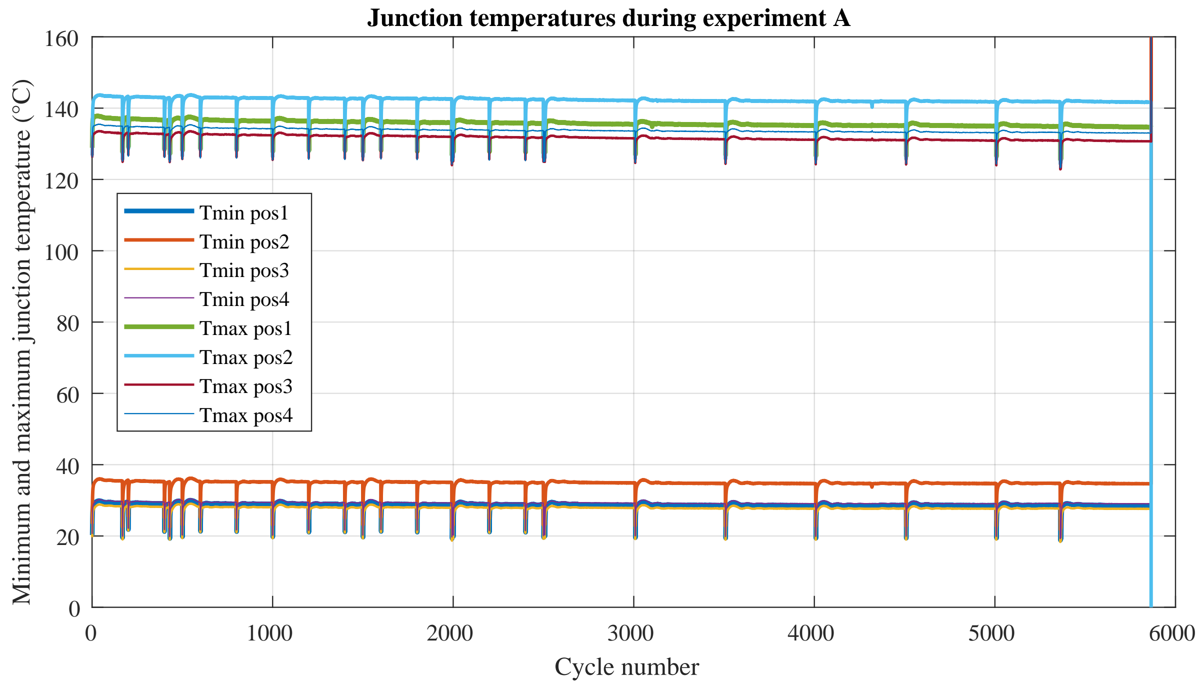
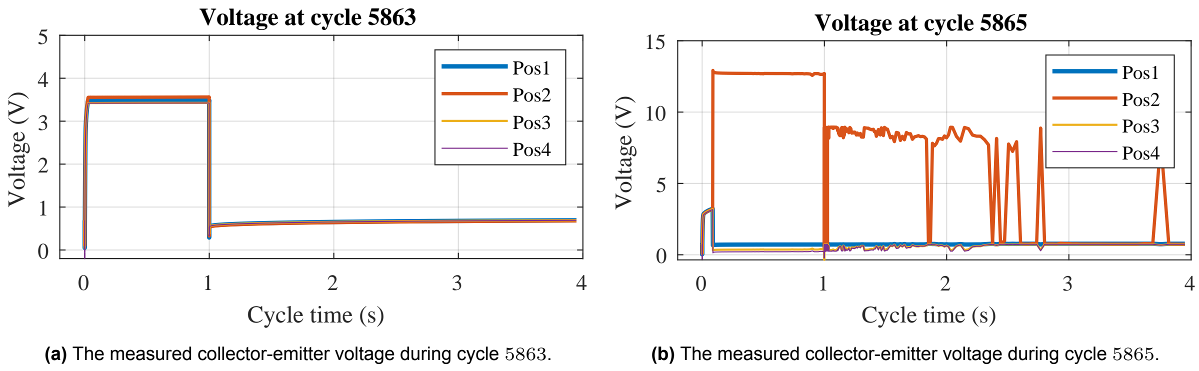


Figure 5.2: The minimum and maximum junction temperature during experiment A where $I_{\text{h}} = 20$ A, $t_{\text{on}} = 1$ s, $t_{\text{off}} = 3$ s and $T_{\text{hs}} = 5°$ C. During the thermal response measurements, the junction temperature of the device is decreased more than during the power cycling test, which creates spikes in the graph. At cycle 5865, the values of the measured voltage and corresponding junction temperature exceeds the limits, indicating a fault is happening.

cycling test, the minimum and maximum junction temperatures after the thermal response measurement are jumped down. The values right after the thermal response measurement of cycle 1000 are given in columns 4 and 5 of Table 5.6. The minimum junction temperatures are decreased by 6 to 9 $°$C and the maximum junction temperatures are decreased by 5 to 15 $°$C. At the start of the experiment and after the thermal response measurement, the minimum and maximum junction temperatures are increasing for 20 cycles, and have a little overshoot before the oil inside the heatsink is adjusted and reach the median temperature. This process can be observed by zooming in as done in Figure C.6 in the appendix.

At cycle 5865, the minimum and maximum junction temperature values jump to impossible values as given in column 6 and 7 of Table 5.6, and the test is stopped. The junction temperatures are calculated based on the measured voltage during that cycle. The measured voltages up to cycle 5863 are identical and presented in Figure 5.3a. However, at cycle 5865, presented in Figure 5.3b, the voltage of position 2 is unstable and also affects the measurement of the other samples. This will result in the extreme junction temperatures observed in cycle 5865.

After this test, the samples are connected to the electrical characteristics analysis. Samples 1, 3, and 4 are working correctly, but sample 2 has a varying gate-emitter voltage of 9.7 to 12 V and a gate current of 0.5 A (which was the maximum setting in the power supply). The collector-emitter current could still flow, and the collector-emitter voltage follows the change of the current. The electrical resistance between the collector and emitter is 243 kΩ while the electrical resistance between the gate and emitter is 657 Ω, which is too low. During the power cycling test, the gate leakage current was below 1 nA, as can be seen in Figure 5.4.
The different structure functions executed during the experiment are studied to see if there is a fault in the thermal layers. As can be observed in appendix section C.4, no changes are found in the structure functions and the corresponding thermal resistance per layer. Furthermore, as shown in Figure C.2 and Figure C.3 in appendix C the electrical resistance and on-voltage are slightly increasing but less than the 5% to call it a failure. During the thermal response measurement, the heating time is larger than during the power cycling test, and therefore the maximum junction temperature is increased. The mea-



(a) The measured collector-emitter voltage during cycle 5863.

(b) The measured collector-emitter voltage during cycle 5865.

Figure 5.3: The measured collector-emitter voltage during cycles 5863 and 5865 of experiment A where $I_h = 20$ A, $t_{on} = 1$ s, $t_{off} = 3$ s and $T_{hs} = 5°$ C.

sured junction temperatures during the thermal response measurement of cycle 5864 are presented in Figure C.7. Position 2 has the highest maximum junction temperature of 169 °C during the thermal response measurement. This is close to the maximum allowed junction temperature. Furthermore, the heating current is higher than the allowed limit and might be the reason for the failure.

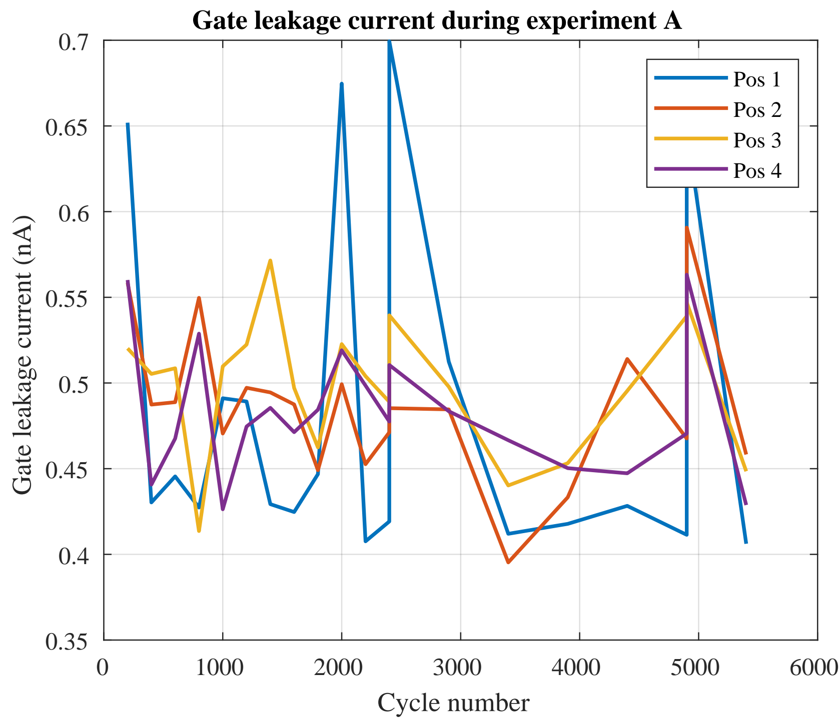


Figure 5.4: The gate leakage current during experiment A.

5.4. Experiment B

The broken sample in experiment A was replaced and calibrated. The same settings as in experiment A were set, however during this experiment the humidity was higher. When selecting the heatsink temperature at 5 °C, condense was forming on the heatsink and IGBTs. Even so, the test was continued. The measurements are different than expected and the devices broke down after 13 cycles. The measurement results are presented in appendix D.

6

Semiconductor end-of-life assessment

The goal of the end-of-life assessment is to find the lifetime of the semiconductor devices. In this experiment, eight IGBTs are connected, four in series connected to channel 1 and four in series connected to channel 2. It would have been better to test four IGBTs and four MOSFETs simultaneously, but the power cycling machine doesn't support this option.

This experiment, named experiment C, is split up into two runs of 116 714 and 184 250 cycles. The same devices are used, and the setup didn't change. Therefore the test results can be combined, but the results are discussed separately to make it more comprehensive.

After 300 964 cycles, the devices didn't show any aging due to the thermo-mechanical stresses. The expected lifespan of the IGBT for a temperature variation of $80\ ^\circ$C would be 160 000 cycles [46]. The tested IGBTs have exceeded this lifespan.

To avoid problems with the moister, the heatsink temperature was set at $16\ ^\circ$C, a little higher than the dewpoint of approximately $14\ ^\circ$C. The heating current is set to 12 A since this is the maximum continuous DC current according to the datasheet. The heating time is again set at 1 s and the cooling time is 3 s. This resulted in a temperature cycle from 25 to $103\ ^\circ$C for the samples in channel 1 and a temperature cycle from 30 to $115\ ^\circ$C for the samples in channel 2. The difference in junction temperatures is the result of the junction to ambient thermal resistance of the samples, varying from 3.6 to $4.1\ ^\circ$C/W. This is higher than the previously assumed value in the thermal model, which could be caused by the mounting of the devices. Furthermore, the measured electrical resistance is around 20 mΩ lower than assumed in the thermal model.

The stop criteria for the power cycling test are set by taking the average value over cycle 31 to 80 resulting in:

Parameter	Limit in percentage	Limit of experiment C1	Limit of experiment C2
Min V_{on}	95 %	2.29 V	2.26 V
Max V_{on}	105 %	2.53 V	2.50 V
Max ΔT_{j}	110 %	$87.3\ ^\circ$C	$95.2\ ^\circ$C
Max $T_{\text{j,max}}$	110 %	$124\ ^\circ$C	$125\ ^\circ$C
Min I_{cycle}	95 %	11.4 A	11.4 A
Max R_{on}	120 %	239 mΩ	236 mΩ

6.1. Results of experiment C1

The thermal response measurement is executed every 2500 cycles with a heating current of 10 A, heating time of 5 s, cooling time of 60 s, and delay of 30 s. After 81 750 cycles, the thermal response measurement is repeated every 200 cycles. In addition, the gate current is measured every 2500 cycles.

The minimum and maximum junction temperatures of the eight samples are presented in Figure 6.1. The spikes in the junction temperature are the result of the thermal response measurement since the device is cooled down more than during the power cycling test. The junction temperatures at the start of the experiment and at the end of this power cycling test are summarized in Table 6.1. Also, the value of the power, on-voltage, and electrical resistance are given in this table.

The power cycling was stopped at cycle 81 520 because the limit for max V_{on} was reached. The abrupt jump of the voltage occurred within one cycle. I expect that the power cycling machine initiated its safety procedure and stops the measurement since the maximum ambient temperature of the machine is 30 °C. During this day the room temperature was 28 °C and might exceed the 30 °C closer to the test setup. After decreasing the room temperature, the test was continued. The ventilation in the room was improved by keeping the door open to prevent this problem in the future.

Table 6.1: The measured valued at the start and end of experiment C1.

	$T_{\text{j,max}}$ (°C) at the start	$T_{\text{j,max}}$ (°C) at the end	Increase or decrease	$T_{\text{j,min}}$ (°C) at the start	$T_{\text{j,min}}$ (°C) at the end	Increase or decrease
Pos 1.1	107.6	107.6	0.0%	25.8	26.0	0.6%
Pos 1.2	102.8	103.0	0.3%	25.1	25.4	1.2%
Pos 1.3	103.2	103.6	0.4%	24.9	25.3	1.7%
Pos 1.4	103.6	104.1	0.6%	24.4	25.0	2.2%
Pos 2.1	115.3	118.0	2.3%	29.6	29.3	-0.7%
Pos 2.2	118.9	120.8	1.6%	32.4	31.0	-4.3%
Pos 2.3	111.3	113.2	1.7%	29.8	29.0	-2.5%
Pos 2.4	114.4	116.9	2.2%	29.4	28.9	-1.7%
	ΔT_{j} (°C) at the start	ΔT_{j} (°C) at the end	Increase or decrease	P (W) at the start	P (W) at the end	Increase or decrease
Pos 1.1	81.7	81.8	0.1%	197.7	198.0	0.2%
Pos 1.2	77.7	77.8	0.1%	194.2	194.6	0.2%
Pos 1.3	78.3	78.4	0.2%	195.9	196.5	0.3%
Pos 1.4	79.2	79.3	0.2%	196.1	196.8	0.3%
Pos 2.1	85.7	88.9	3.7%	199.2	199.1	-0.1%
Pos 2.2	86.6	90.1	4.0%	198.5	199.6	-0.1%
Pos 2.3	81.5	84.4	3.5%	198.5	198.2	-0.1%
Pos 2.4	85.0	88.2	3.8%	198.3	198.1	-0.1%
	V_{on} (V) at the start	V_{on} (V) at the end	Increase or decrease	R_{ce} (mΩ) at the start	R_{ce} (mΩ) at the end	Increase or decrease
Pos 1.1	2.39	2.40	0.2%	197.7	198.0	0.1%
Pos 1.2	2.35	2.35	0.2%	194.2	194.6	0.1%
Pos 1.3	2.37	2.38	0.3%	195.9	196.5	0.2%
Pos 1.4	2.37	2.38	0.3%	196.1	196.8	0.2%
Pos 2.1	2.41	2.41	-0.1%	199.2	199.1	3.7%
Pos 2.2	2.41	2.41	-0.1%	199.8	199.6	4.0%
Pos 2.3	2.40	2.40	-0.1%	198.5	198.2	3.5%
Pos 2.4	2.40	2.41	-0.1%	198.3	198.1	3.8%

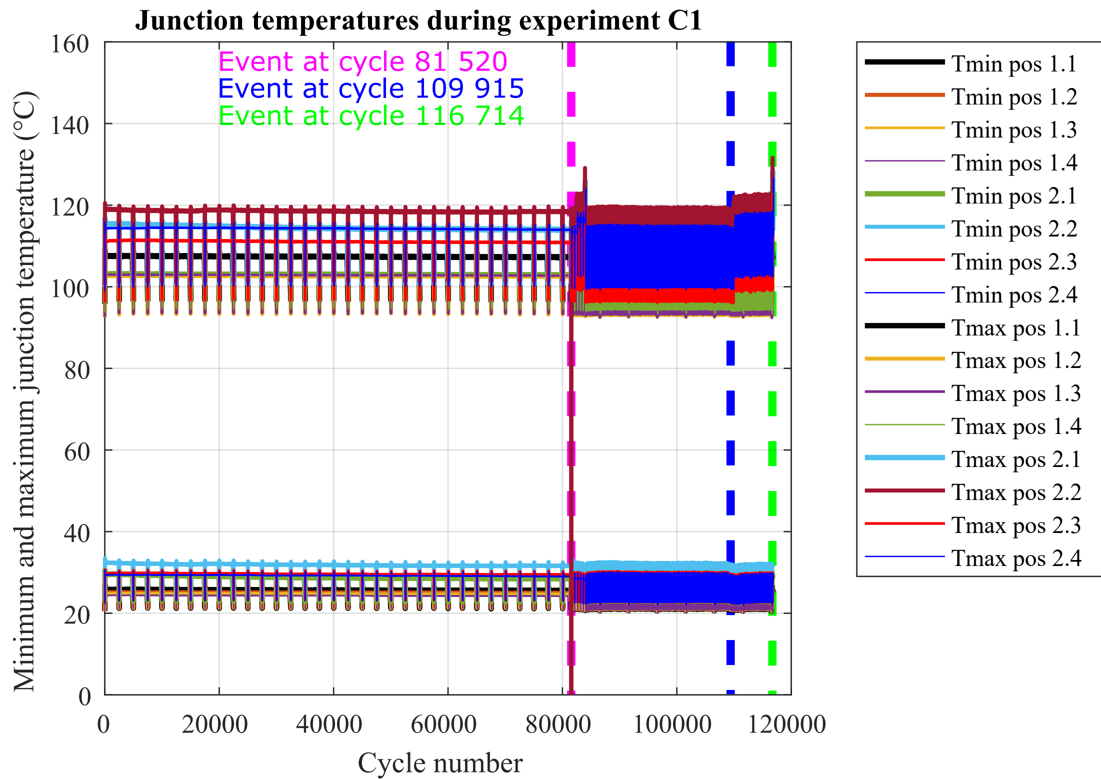


Figure 6.1: Measurement results of the power cycling test of experiment C1. The spikes in the junction temperature are the result of the thermal response measurement. The thermal response measurement is executed every 2500 cycles until cycle 81520 and after that, the thermal response measurement is executed every 200 cycles.

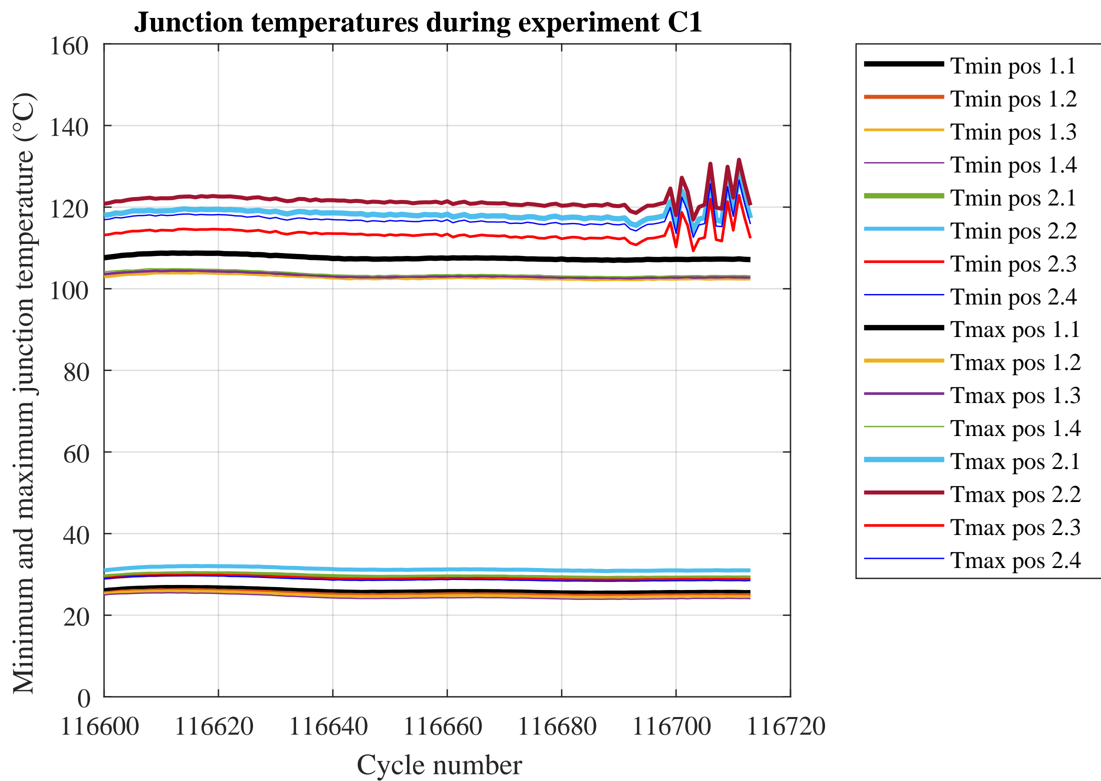


Figure 6.2: The minimum and maximum junction temperature during the last 100 cycles of experiment C1.

The maximum junction temperatures of position 2.1, 2.2, 2.3, and 2.4 around cycle 81 600 decrease by $1\ °C$ and increases by $4\ °C$ around cycle 81 750. After the test is manually restarted, the maximum junction temperature is decreased by $3\ °C$, so back to their original values. Around cycle 110 000, the maximum junction temperatures of position 2.1, 2.2, 2.3, and 2.4 are increases by $2\ °C$.

Furthermore, the test was stopped at 116 714 cycles. A closer look at the maximum junction temperature right before the stop is given in Figure 6.2. The maximum junction temperature during the last 20 cycles was changing by $4\ °C$, since the measured voltage was unstable. This can be observed in appendix section E.1. In the same section, the other parameters at the end of this experiment are presented. V_{on} and V_{cold} didn't have unstable behavior, and no change was observed in the measured voltage between cycle 116691 and 116714.

6.2. Results of experiment C2

After the power cycling test was stopped at cycle 116 714, the electrical characteristics analysis was executed and all eight IGBTs worked as expected. Since the devices were not removed from the heatsink or PCB, the experiment will be continued. However, the amount of cycles is reset and should be added to the 116 714 cycles during part one.

The minimum and maximum junction temperature of the eight samples are presented in Figure 6.3. During this experiment, the thermal response measurement is executed every 200 cycles. Due to the temperature variation after the thermal response measurement, the graphs are less readable when focusing on all the cycles. The values at the start and at the end of the power cycling test are summarized in Table 6.2 as well as their percentile increase or decrease. Moreover, the values for the junction temperature deviation, power, on-voltage, and electric resistance of the eight samples at the start and end are also presented in this table. The minimum junction temperature of positions 2.1, 2.2, 2.3, and 2.4 have a large decrease of 28% but this is not one of the set stop limits. The percentile increase per sample of V_{on} is the same as the increase of R_{CE} even before rounding the values.

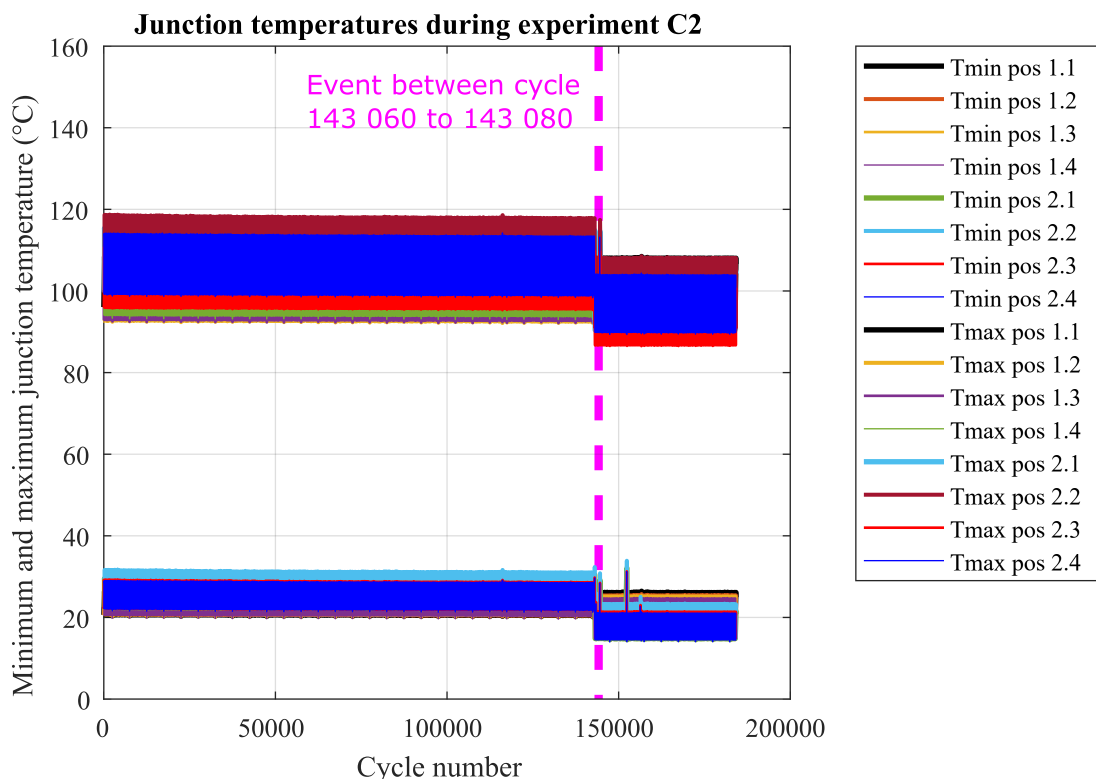


Figure 6.3: Minimum and Maximum junction temperature of the power cycling test of experiment C2.

Table 6.2: The measured valued at the start and finish of experiment C2.

	$T_{\text{j,max}}$ (°C) at the start	$T_{\text{j,max}}$ (°C) at the end	Increase or decrease	$T_{\text{j,min}}$ (°C) at the start	$T_{\text{j,min}}$ (°C) at the end	Increase or decrease
Pos 1.1	107.0	106.6	-0.4%	25.2	24.9	-1.1%
Pos 1.2	102.2	101.8	-0.8%	24.6	24.3	-1.1%
Pos 1.3	102.6	102.2	-0.4%	24.4	24.0	-1.4%
Pos 1.4	103.0	102.4	-0.6%	23.8	23.5	-1.4%
Pos 2.1	114.2	104.0	-8.9%	28.6	20.7	-27.9%
Pos 2.2	117.4	106.8	-9.0%	30.2	22.3	-27.2%
Pos 2.3	109.3	99.4	-9.1%	28.2	20.4	-27.8%
Pos 2.4	112.7	102.4	-9.1%	27.8	20.0	-28.3%
	ΔT_{j} (°C) at the start	ΔT_{j} (°C) at the end	Increase or decrease	P (W) at the start	P (W) at the end	Increase or decrease
Pos 1.1	81.8	81.7	-0.1%	28.9	28.9	0.0%
Pos 1.2	77.7	77.6	-0.1%	28.4	28.4	0.0%
Pos 1.3	78.3	78.2	-0.1%	28.7	28.7	0.0%
Pos 1.4	79.2	79.2	-0.1%	28.7	28.7	0.0%
Pos 2.1	85.7	83.4	-2.6%	29.1	29.1	0.0%
Pos 2.2	86.7	84.5	-2.6%	29.2	29.2	0.0%
Pos 2.3	81.1	79.0	-2.6%	29.0	29.0	0.0%
Pos 2.4	84.8	82.5	-2.7%	28.9	28.9	0.0%
	V_{on} (V) at the start	V_{on} (V) at the end	Increase or decrease	R_{ce} (mΩ) at the start	R_{ce} (mΩ) at the end	Increase or decrease
Pos 1.1	2.40	2.40	0.1%	198.0	198.1	0.1%
Pos 1.2	2.35	2.35	0.1%	194.4	194.6	0.1%
Pos 1.3	2.37	2.38	0.1%	196.3	196.4	0.1%
Pos 1.4	2.38	2.38	0.1%	196.4	196.5	0.1%
Pos 2.1	2.41	2.41	0.2%	199.0	199.4	0.2%
Pos 2.2	2.42	2.42	0.2%	199.6	200.0	0.2%
Pos 2.3	2.40	2.40	0.1%	198.2	198.4	0.1%
Pos 2.4	2.40	2.40	0.2%	198.0	198.3	0.2%

Between cycle 143 060 to 143 080 the minimum and maximum junction temperatures of position 2.1, 2.2, 2.3, and 2.4 goes down. Figure 6.4 shows the minimum and maximum junction temperature during this decrease. All samples in channel two make the same jump down, up, and down again, while channel one is unaffected. The minimum junction temperature is decreased by 7 °C and the maximum junction temperature is decreased by 9 °C. The junction temperature deviation itself did only decrease 2 °C. The cycle voltage before and after the jump are compared, but no difference is observed that could lead to the jump in junction temperatures. The progress of the cycle voltage is presented in appendix section E.3. The behavior of the heating current, power, on-voltage and electrical resistance around the jump can be observed in appendix section E.4. In the same section, the graphs focused on the start and end can also be found.

From the thermal response measurement, the structure functions are calculated. The cumulative structure functions are presented in Figure 6.6 After cycle 143 000, the structure functions of the four samples in channel 2 are slightly lifted to the left. The shift occurs around 3 °C/W, indicating that the thermal resistance of the heatsink is changed. The degradation plot made at $C_{\text{th}} = 10000$ Ws/°C is shown in Figure 6.5. The values of the thermal resistance in this plot are the junction to ambient thermal resistance. The thermal resistances of position 2.1, 2.2, 2.3, and 2.4 decreases abruptly by 0.1 °C/W at cycle 143 000. The degradation plots for the other layers are presented in appendix section E.5.

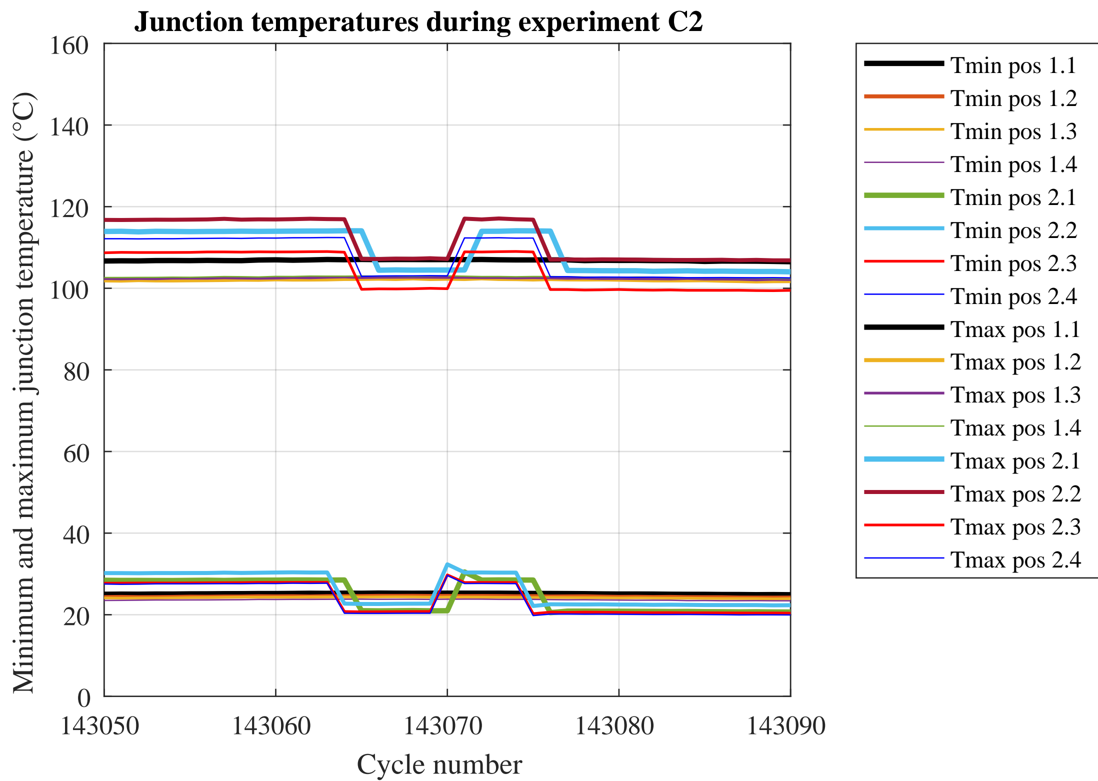


Figure 6.4: The maximum junction temperature between cycle 143050 and 143090 of experiment C2.

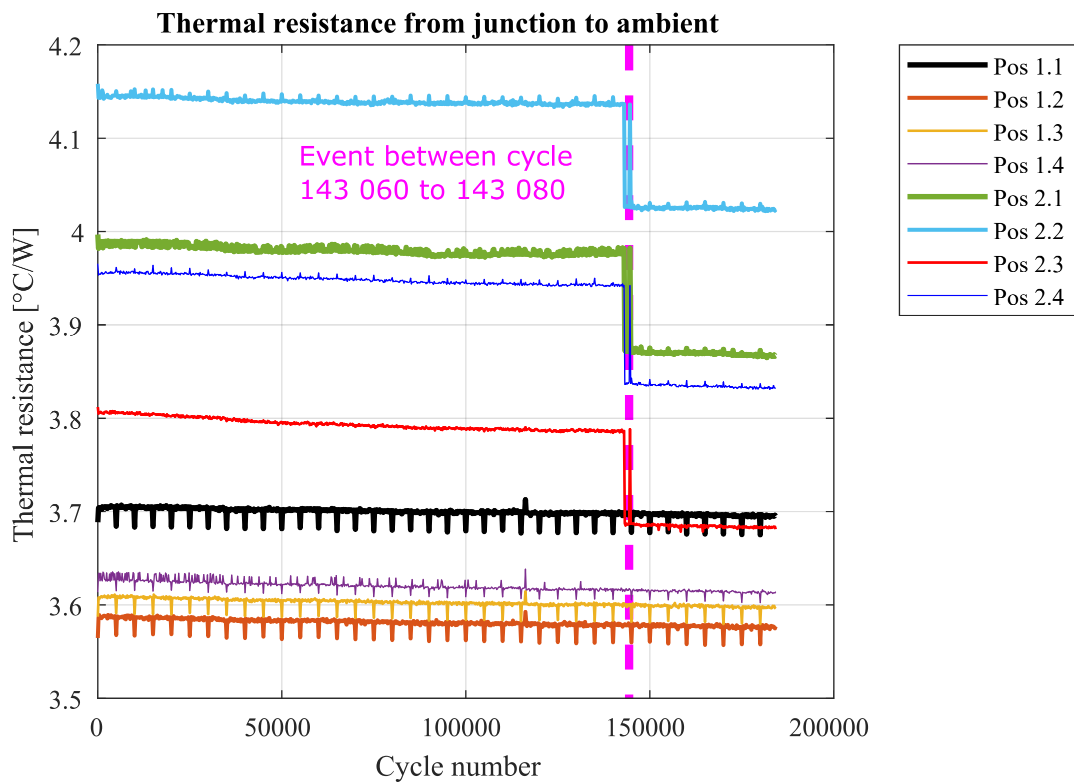


Figure 6.5: The process of the thermal resistance from junction to ambient.

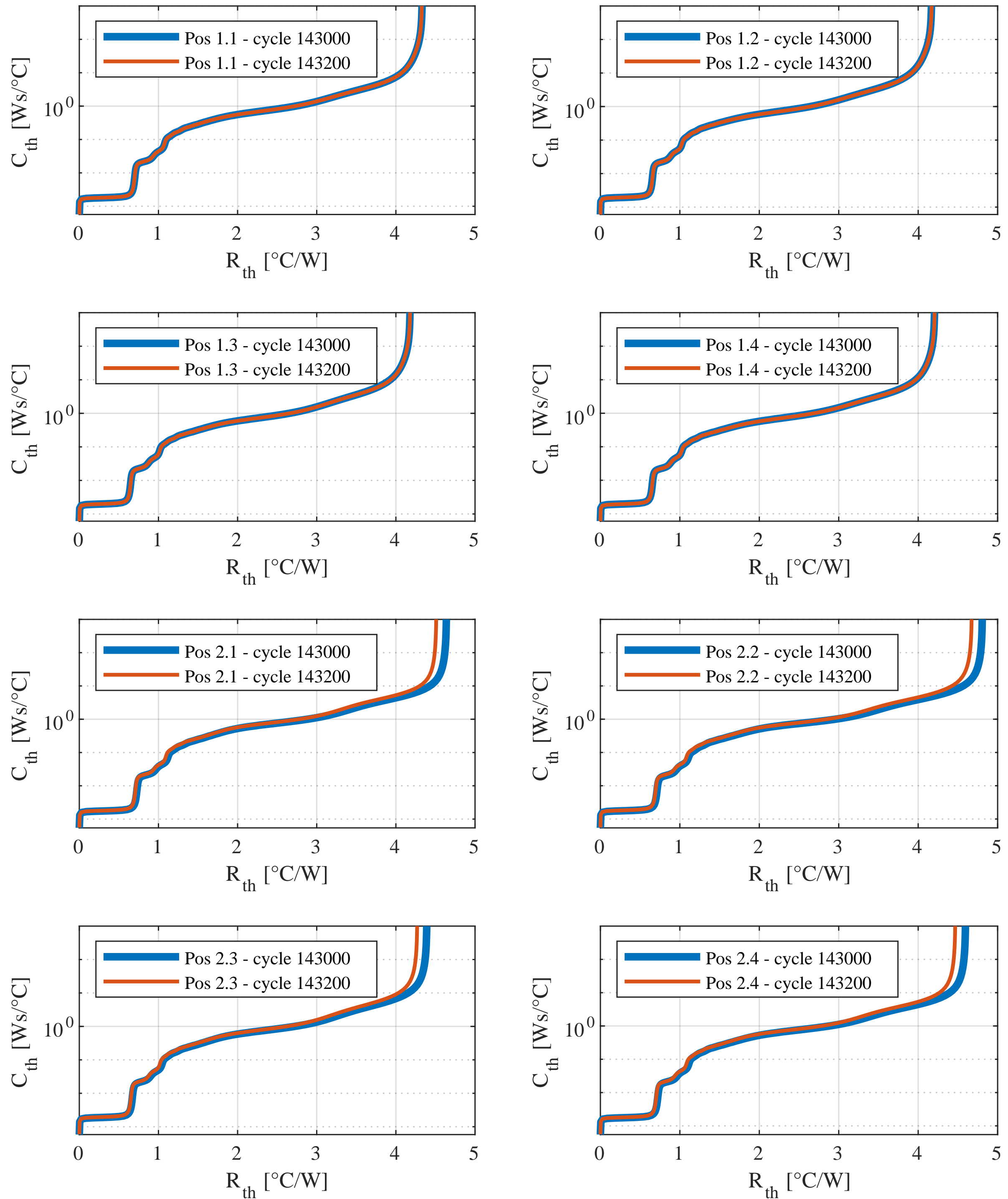


Figure 6.6: The cumulative structure functions based on the thermal response measurement of experiment C2. The structure functions up to cycle 143 000 are identical. After that the structure function of the four samples in channel 2 shifts at the heatsink layer (after $3\ ^\circ$C)/W.

6.3. Discussion

During the last cycles of experiment C1, the values of V_{hot} and therefore $T_{\text{j,max}}$ of the four samples of channel 2 are changing. Nevertheless, the on-voltage, power losses didn't change during this event. Moreover, the electrical characteristic analysis looks good, and after the test is restarted in experiment

C2 the maximum junction temperatures are stable.

During the event at cycle 81 520 of experiment C1, the test was abruptly stopped. The ambient temperature during that time was very high and close to the limit the power cycling machine can handle, which is most likely the cause of the event. After the test is continued, the measurement results are as expected.

Furthermore, the maximum junction temperatures of the samples of channel 2 are slightly increasing and decreasing during experiment C1. However, the change is small and can be considered random variations and not the cause of any failures. Mostly the thermal resistances for channel 2 are unstable.

In addition, the measured maximum junction temperatures between cycles 116 691 and 116 714 are varying. Since the variations are temporary, the devices didn't fail.

Moreover, during the event at cycle 143 060 of experiment C2, the four samples of channel 2 experienced a decrease in the minimum and maximum junction temperature. During this event, the electrical characteristics are the same but the thermal resistance of the heatsink is suddenly decreased. The change is not specific to one sample but common to all samples of channel 2. Therefore we can conclude that the devices didn't have any thermal degradation. In the case of thermal fatigues, the thermal resistances and maximum junction temperatures would increase which is not the case in this experiment. Since the decrease of the thermal resistance did not occur in the samples of channel 1, the julabo cooler could not be the cause of the change.

So in conclusion, the samples don't show any sign of degradation after 300 964 cycles. Therefore we have found a device and operating conditions with an infinite lifetime. However, it could be possible that the test doesn't replicate the thermo-mechanical stresses correctly. For example, the heating time can be set longer, to heat up the layers inside the device more.

7 Conclusion and future work

7.1. Conclusion

During this thesis, I learned a lot about the electrical and thermal behavior of the silicon IGBT and silicon-carbide MOSFET. The thesis started with a literature study about power semiconductor devices and the potential of silicon-carbide semiconductors. Furthermore, much knowledge was gained about reliability, end-of-life studies, and failure mechanisms. Next, a practical setup for the thermal response measurements, power cycling test, and the devices under test are selected. Moreover, the electrical characteristics are analyzed. In the following months, the thermal behavior was investigated by deriving the thermal equations of the system. Also, by executing the thermal response measurement for the IGBT and MOSFET, the cumulative structure function, the Cauer model, and the time constant spectrum are derived, and the effect of various heating currents, thermal interface material, and heatsink properties are studied. Moreover, the power cycling test was executed for varying cooling times, heating times, heating currents, and heatsink temperatures, and the results are used to predict the thermal resistance, thermal capacitance, and electrical resistance of the system and to verify the thermal equations. This leads to a thermal model that can be used to set up the power cycling test for different temperature cycles and loading conditions. Lastly, the end-of-life assessment for the IGBTs is executed for eight IGBTs. After 300 thousand cycles, the devices didn't show any degradation

At the start of this thesis, the following research questions are defined. They have been answered throughout the thesis.

7.1.1. What is the empirical thermal model of the semiconductor devices and the practical setup?

Firstly, the thermal behavior of the silicon IGBTs and silicon-carbide MOSFETs in the test setup is investigated with the different thermal response measurements. The values of the thermal resistance and thermal capacitance of the Cauer thermal model are thereafter found using the thermal response measurement and corresponding cumulative structure function.

Moreover, the thermal equations for the junction temperature during heating and cooling are derived and used to determine the minimum and maximum junction temperature during the power cycling test. In addition, the values for the thermal time constant, thermal resistance, thermal capacitance, and electrical resistance are determined based on results from the power cycling test for different heating currents, heating times, cooling times, and heatsink temperatures. For this system, $\tau = 1.6$ s, $R_{\text{th}} = 2.9$ K/W, $C_{\text{th}} = 0.5$ Ws/K and $R_{\text{ce}} = 220$ mΩ. Furthermore, the curve fitting of the thermal equations and the results have good R^2 and RMSE values to validate the thermal equations. The thermal equations can be used as a model for the power cycling test under different loading conditions and thermal cycles.

$$\text{Heating: } T_j(t) = (R_{th} I_h^2 R_{ce} - T_j(t_0) + T_{amb})(1 - e^{\frac{-(t-t_0)}{\tau}}) + T_j(t_0) \tag{7.1}$$

$$\text{Cooling: } T_j(t) = T_{amb} + (T_j(t_0) - T_{amb}) e^{\frac{-(t-t_0)}{\tau}} \tag{7.2}$$

$$T_{j,min} = T_{hs} + (T_{j,max} - T_{hs})(e^{\frac{-t_{off}}{\tau}}) \tag{7.3}$$

$$T_{j,max} = (R_{th} I_h^2 R_{ce} - T_{j,min} + T_{hs})(1 - e^{\frac{-t_{on}}{\tau}}) + T_{j,min} \tag{7.4}$$

(7.5)

7.1.2. What is the influence of the selected parameters for the power cycling test on the thermal cycle?

Multiple short power cycling tests are performed with varied parameter settings. The resulting minimum and maximum junction temperatures are investigated to find the relation between the chosen parameters and the thermal cycle, as presented in Figure 5.1 The increase in cooling time can decrease the minimum junction temperature greatly but will reach an asymptote around the ambient temperature. The increase of the heating current will increase the maximum junction temperature and the junction temperature swing exponentially and increases very fast while the change in minimum junction temperature is small. Increasing the heating time will also increase the maximum junction temperature and junction temperature swing, but will eventually reach a maximum. The effect of the heating time on the minimum junction temperature is small. The increase in heatsink temperature will increase the minimum and maximum junction temperature linearly, and also the junction temperature swing is slightly increased. All four parameters can be chosen to achieve the desired thermal cycle. The values of the parameters for different thermal cycles can be calculated from the thermal equations.

7.1.3. How can we minimize the duration of the end-of-life assessment?

Firstly, the number of cycles until failure can be reduced by increasing the temperature variations during the test, e.g. increasing the power losses. However, this will only give information about the worst-case scenario and is not a helpful approach when executing the end-of-life test for practical applications with a fixed thermal cycle.

Another option to accelerate the end-of-life assessment is to minimize the time of each thermal cycle by reducing the heating and cooling times. Since the power cycling test has multiple parameters to select the thermal cycle, we can fix the heating and cooling times at a low value and change the heating current and heatsink temperature to obtain the desired thermal cycle. Nevertheless, the heating and cooling period must be large enough to expand and contract the relevant layers. Furthermore, careful consideration must be taken with respect to the humidity in the air and possible condensing on the heatsink. In addition, the chosen current should not exceed the rated current of the device under test.

Lastly, the value of the thermal time constant of the system will affect the thermal behavior during the heating and cooling phases. Decreasing the value of the thermal time constant will speed up the heating and cooling process, so the cooling and heating times can be decreased to reach the same thermal cycle. The thermal time constant of the IGBTs and MOSFETs are fixed properties and have a large impact on the thermal time constant of the whole system. The thermal time constant of the system was slightly reduced by replacing the thermal paste with a thermal pad with a small thermal resistance.

7.1.4. How to perform an end-of-life assessment for silicon IGBTs and silicon-carbide MOSFETs?

The power cycling test can be used to execute the end-of-life assessment. Eight samples can be tested simultaneously in the prescribed setup. The IGBTs are used in saturation mode and during the cooling phase the measured voltage over the diode is used to calculate the junction temperature. The MOSFET is connected in body diode mode, i.e. a negative current and voltage are applied. The body diode of the MOSFETs is used to heat up the device and measure the voltage to calculate the junction temperatures.

Depending on the relation between the chosen parameters to the thermal cycle, the thermal model

can be used to select the desired parameters. Care should be taken to the trade-offs between cycling time and heating and cooling times. Also, the heatsink temperature has a minimum temperature to prevent moisture.

The power cycling test for eight IGBTs was executed. In the first experiment, the temperature cycle is from $30\ °C$ to $135\ °C$ and the devices broke after 5865 cycles. In the second experiment, the temperature cycle is from $25\ °C$ to $105\ °C$ and the devices continued functioning after 300 965 cycles.

7.2. Future work

After finishing this thesis, I have some recommendations to investigate in future work. To start, the power cycling test should be executed on more samples to get more data and be able to draw more reliable conclusions about the expected number of cycles to failure. Next, the test should be repeated for different thermal cycles and loading conditions. This makes it possible to create lifetime curves and estimate the number of cycles to failure for multiple thermal cycles and loading conditions. Furthermore, the influence of the median temperature on the number of cycles can be investigated and included in the lifetime curves.

The effects of the power cycling parameters on the thermal cycle of the MOSFET can be examined by executing short power cycling tests and changing one of the parameters. In a similar way to the IGBT, the thermal time constant, thermal resistance, thermal capacitance, and electrical resistance of the MOSFET can be found. The end-of-life assessment of the silicon-carbide MOSFET should be carried out, and the lifetime curve can be made when finishing the end-of-life assessment for many samples and thermal cycles. The reliability of silicon IGBTs and silicon-carbide MOSFETs can be compared based on their lifetime curves. Also, different IGBTs and MOSFETs types should be tested to be able to obtain a general conclusion.

Furthermore, the cause of the failures of the IGBTs and MOSFETs should be investigated. Which layer or layers broke down, and how can this be delayed in practice? The cumulative structure function can be used to find the thermal failures in each layer. In addition, the chosen heating and cooling times in the end-of-life assessment might influence which layer will break first. This might also be thoroughly investigated.

In addition, the power cycling test can be improved by expanding the setup to 16 devices. Moreover, the possibility of using a variable gate voltage should be investigated to create the thermal cycles. The gate voltages can also be set to different values per device and might cancel out the influence of the difference in power loss or thermal resistance per device. Lastly, the electric noise in the setup should be investigated and reduced.

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Power and Thermal Cycling Testbed for End of Life Assessment of Semiconductor Devices

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***Abstract*—The reliability of semiconductor power devices can be studied by performing a thermal and power cycling test. In order to create the desired temperature cycles, there are four free variables to select during the power cycling test, namely the heating current, heating time, cooling time, and heatsink temperature. In this paper, the relation between the selected variables and the minimum and maximum junction temperature is extensively tested for the silicon IGBT with serienumber IKP06N60T. Furthermore, the thermal model is discussed and verified and a rough estimate of the electrical resistance, thermal time constant, thermal resistance, and thermal capacitance are calculated.**

***Index Terms*—Power cycling test, Reliability, Thermal model, Silicon IGBT, Silicon-Carbide MOSFET, Thermal device characteristics, Lifetime testbed**

I. INTRODUCTION

Semiconductor devices are essential building blocks in power electronic systems and therefore crucial in our technological society. The most commonly used semiconductor devices are the metal-oxide-semiconductor field-effect transistor (MOSFET) and insulated-gate bipolar transistor (IGBT) made from silicon doped with boron and phosphorous [1]. The drive for innovation, like increasing the voltage range and efficiency, has led to the creation of the silicon-carbide MOSFET [2]. The bandgap is increased from 1.12 eV for silicon (Si) to 3.26 eV for silicon-carbide (SiC) [3]. SiC devices have a 2.4 times higher Young's modulus, 410 GPa compared to 169 GPa for Si devices [4]. The coefficient of thermal expansion of SiC devices is $4.0 \cdot 10^{-6}$ °C^{-1}, which is slightly higher compared to $3.5 \cdot 10^{-6}$ °C^{-1} for Si [4], [5].

SiC devices can handle higher operating temperatures, higher voltages, and higher switching frequencies and have lower conduction and switching losses than Si devices [5]. SiC MOSFETs have breakdown voltages up to 3.3 kV and still have a low on-resistance, fast recovery time, and fast switching, while the Si MOSFET has in practice a maximum voltage of 900 V [2], [6].

Another important feature of devices is their reliability, since failures can have severe consequences in e.g. the automotive and aerospace industry [7]. The semiconductor devices are particularly prone to failure in power converters and machines and are considered a weak link in the system reliability [8], [9]. In most cases, it is not profitable to install new semiconductors and the whole system is replaced leading to more e-waste.

During the operation of power converters, the generation of power losses results in the occurrence of thermal cycles characterized by repeated heating and cooling. These thermal cycles are primarily caused by variations in the load, switching actions, and environmental conditions. Power semiconductors, which are composed of multiple layers with different coefficients of thermal expansion (CTE), are susceptible to the effects of these temperature cycles [10], [11]. It is crucial to consider these thermal effects and the associated thermo-mechanical stresses in the design and operation of power converters to ensure their reliable performance and longevity. Investigations have shown that thermal stresses account for 55% of all stressors [12]–[16]. Therefore, thermo-mechanical fatigues are the most frequently encountered forms of failure in power devices [17]. For semiconductors with the same geometry, SiC semiconductors will experience larger thermo-mechanical strains inside the device, possibly reducing the lifetime [18]

The thermo-mechanical fatigues that can arise from these thermal cycles are bond-wire cracks, bond-wire liftoff, solder fatigues in the baseplate or chip, and the reconstruction of chip metallization [5], [8], [9], [19], [20]. These phenomena can lead to the deterioration and potential failure of the power devices over time. The most common failure due to thermal-mechanical stresses are bond-wire cracks and bond-wire liftoff because they experience the largest thermal-mechanical stresses since the CTE of the chip ($4{\cdot}10^{-6}$ $°C^{-1}$) and aluminum wire ($23{\cdot}10^{-6}$ $°C^{-1}$) differ the most [5], [20], [21].

Due to the time-consuming nature of collecting field data for the reliability evaluation of power devices, accelerated aging tests are frequently employed. These tests, involving power cycling and thermal cycling, aim to replicate the thermal stress effects that power devices undergo when in use [5], [8]. Evaluating the devices' reliability and determining end-of-life under more condensed timeframes is feasible by putting them through accelerated aging tests.

Thermal cycling tests include heating up and cooling down the devices with an external heating source. In contrast, power cycling tests include periodically applying and removing power to the devices, resulting in active heating due to the power losses. Both tests will replicate the thermal stresses the devices experience in real-world situations and are useful tools to evaluate the device's reliability under various thermal-

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mechanical stresses [1], [5], [8], [22].

Through these accelerated aging experiments, valuable insights can be gained regarding the reliability of power devices, their main failure mechanism, and expected lifetimes under cyclic thermal loading. This information is essential for designing robust and reliable power electronic systems, as it allows for early identification of potential failure mechanisms and optimizing device lifetimes.

In this paper, the thermal and power cycling tests, used to asses the reliability of the semiconductor power devices, are discussed in Section II. Subsequently, section III explains the thermal model applicable to the semiconductor devices in order to determine the settings of the power cycling test and make the testbed. In section IV, multiple tests are carried out to see the relation between the parameters and the maximum and minimum junction temperature and verify the thermal model. Furthermore, the thermal characteristics of the device, namely the thermal time constant, thermal resistance and thermal capacitance as well as the electrical resistance are determined based on the measurement results. Finally, the conclusion is given in Section V.

II. Methodology

The thermal and power cycling tests are valuable methods to impose thermal-mechanical stresses and determine the semiconductor device's lifetime [5], [8]. During the thermal cycling test, the heatsink is heated and cooled repeatedly. The devices will follow the thermal cycle of the heatsink. During the power cycling test, the pulsating current flowing through the device will heat up the device. During this test, the heatsink has a fixed temperature and is used to cool down the device. The thermal cycles can be executed faster in the power cycling test since only the device itself needs to be heated. Fig. 1 represents the junction temperature cycles obtained during the power cycling test. The other layers of the semiconductor device also experience thermal cycles and since each layer has a different coefficient of thermal expansion (CTE), thermo-mechanical stresses are created between adjacent layers.

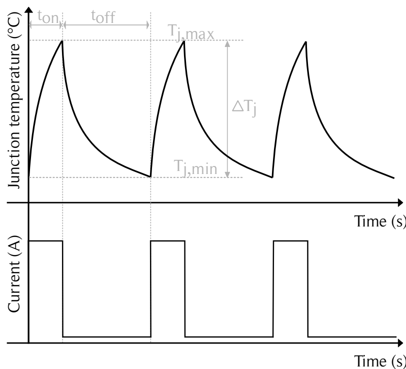

Fig. 1: Illustrative representation of junction temperature cycles created by the pulsating current flowing through the device.

The semiconductor devices are thermally connected to both the heatsink and the power cycling machine. The devices can be fixed onto the heatsink with screws and a thermal pad is added in between to fill the air gaps and provide electric isolation. The cables from the power cycling are screwed onto a pre-designed PCB and the devices are soldered onto this PCB. The setup can be seen in Fig. 2.

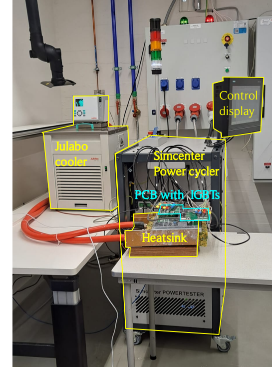

Fig. 2: Picture of the setup between the IGBTs, heatsink, cooling and power cycling machine.

In the following experiments, four 600V silicon IGBTs are connected in series to the setup. The chosen IGBTs for this experiment are the IKP06N60T from Infineon and are designed for junction temperatures up to 175°C and a peak current of 18A [23]. Fig. 3 shows a schematic representation of the test setup.

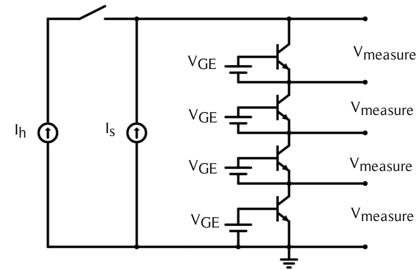

Fig. 3: Schematic representation of the test setup for channel 1 with 4 IGBTs.

Herein, I_h indicates the pulsating current that will heat up the device. I_s is a small bias current of 100 mA that flows continuously through the IGBT to keep the IGBT in forward-biased mode, such that the voltage drop can be measured to determine the junction temperature. V_{GE} is the gate-emitter voltage and $V_{measure}$ is the collector-emitter voltage drop which is used to calculate the junction temperature. The junction temperature cycles can not immediately be measured with the desired accuracy, so the voltage between the collector and emitter of the IGBT is used since the forward voltage is dependent on temperature. During the calibration, the exact relationship between the junction temperature and the collector-emitter voltage drop is established. For example, the measured

relationship during calibration for sample 1 is given in (1) and rewritten to (2).

$$V_{\text{ce}} = -3.721 \cdot 10^-3 \cdot T_{\text{j}} + 0.789 \quad (1)$$

$$T_{\text{j}} = 212.1 - 267.8 \cdot V_{\text{ce}} \quad (2)$$

III. Thermal model

The thermal model of the device can be simplified to a first-order RC circuit as shown in Fig. 4.

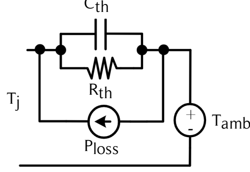

Fig. 4: Simplified thermal model of semiconductor device is a first order RC circuit.

For this first-order RC circuit, the thermal equation is given in (3). By taking the Laplace transformation of (3) and rewriting, we can solve the equation for $T_{\text{j}}(s)$ shown in (4). Converting back to the time domain and substituting $P_{\text{loss}} = I_{\text{h}}^2 \cdot R_{\text{ce}}$ and $R_{\text{th}}C_{\text{th}} = \tau$, we find the expression shown in (5).

$$T_{\text{j}}(t) - T_{\text{amb}} = P_{\text{loss}} \cdot Z_{\text{th}} \quad (3)$$

$$T_{\text{j}}(s) - T_{\text{amb}} = \frac{P_{\text{loss}}}{s} \cdot \frac{R_{\text{th}} \cdot \frac{1}{sC_{\text{th}}}}{R_{\text{th}} + \frac{1}{sC_{\text{th}}}} = \frac{P_{\text{loss}}}{s} \cdot R_{\text{th}} \cdot \frac{\frac{1}{R_{\text{th}}C_{\text{th}}}}{s + \frac{1}{R_{\text{th}}C_{\text{th}}}} \quad (4)$$

$$T_{\text{j}}(t) - T_{\text{amb}} = I_{\text{h}}^2 \cdot R_{\text{ce}} \cdot R_{\text{th}} \cdot (1 - e^{\frac{-t}{\tau}}) \quad (5)$$

Lastly, the heating equation of (6) is derived when taking care of the boundary conditions that $T_{\text{j}}(t = \inf) = T_{\text{amb}} + I_{\text{h}}^2 R_{\text{ce}} R_{\text{th}}$ and $T_{\text{j}}(t = 0) = T_{\text{j}}(t_0)$. For the cooling equation of (7), the boundary conditions are $T_{\text{j}}(t = \inf) = T_{\text{amb}}$ and $T_{\text{j}}(t = 0) = T_{\text{j}}(t_0)$.

Heating:

$$T_{\text{j}}(t) = (R_{\text{th}} I_{\text{h}}^2 R_{\text{ce}} - T_{\text{j}}(t_0) + T_{\text{amb}})(1 - e^{\frac{-(t-t_0)}{\tau}}) + T_{\text{j}}(t_0) \quad (6)$$

Cooling:

$$T_{\text{j}}(t) = T_{\text{amb}} + (T_{\text{j}}(t_0) - T_{\text{amb}}) e^{\frac{-(t-t_0)}{\tau}} \quad (7)$$

The thermal-mechanical stresses are strongly related to the thermal cycles. The thermal cycles are represented by the minimum junction temperature $T_{\text{j,min}}$, maximum junction temperature $T_{\text{j,max}}$ and the junction temperature swing $\Delta T_{\text{j}} = T_{\text{j,max}} - T_{\text{j,min}}$. Equation (6) and (7) are rewritten to (8), (9) and (10).

Parameters:

$$T_{\text{j,min}} = T_{\text{hs}} + (T_{\text{j,max}} - T_{\text{hs}})(e^{\frac{-t_{\text{off}}}{\tau}}) \quad (8)$$

$$T_{\text{j,max}} = (R_{\text{th}} I_{\text{h}}^2 R_{\text{ce}} - T_{\text{j,min}} + T_{\text{hs}})(1 - e^{\frac{-t_{\text{on}}}{\tau}}) + T_{\text{j,min}} \quad (9)$$

$$\Delta T_{\text{j}} = (R_{\text{th}} I_{\text{h}}^2 R_{\text{ce}} - T_{\text{j,min}} + T_{\text{hs}})(1 - e^{\frac{-t_{\text{on}}}{\tau}}) \quad (10)$$

Herein, $T_{\text{j}}(t)$ is the junction temperature at time t. $T_{\text{j}}(t_0)$ is the junction temperature at time t_0. T_{hs} is the temperature of the heatsink and can be controlled to implement passive thermal cycles on the test samples. T_{amb} is the ambient temperature, which in this setup is the same as the heatsink temperature. I_{h} is the heating current. R_{ce} is the electrical resistance between the collector and the emitter. τ is the thermal time constant of the system and equal to $R_t h \cdot C_t h$. R_{th} is the thermal resistance from junction to ambient. C_{th} is the thermal capacitance from junction to ambient.

IV. Influence of selected parameters

In the power cycling test, we have four parameters that can be selected to achieve the desired temperature cycle. Those are the heating current I_{h}, heating time t_{on}, cooling time t_{off}, and heatsink temperature T_{hs}. Based on the derived thermal model, it is expected that increasing the heating current and heating time will increase the $T_{\text{j,max}}$ and increasing the cooling time or decreasing the heatsink temperature will decrease $T_{\text{j,min}}$. The thermal resistance and capacitance are inherent to the IGBTs and can not be changed.

The relation between the selected parameters and the resulting temperature cycle will be studied by repeatedly performing the power cycling test. During the test the gate-emitter voltage is set to 15V and the bias current is set to 100 mA. During the measurement the values of the collector-emitter voltage and corresponding $T_{\text{j,max}}$ and $T_{\text{j,min}}$ are determined. On average, the electrical resistance between the collector and emitter is calculated to be 235 mΩ but depends slightly on the temperature.

Furthermore, the thermal model is verified and the missing values of the thermal time constant and thermal resistance are determined with the curve fitting tool of MATLAB. The heating equation (6) has two unknowns, namely the time constant and the thermal resistance, and results in multiple combinations to the curve fitting and it's difficult to decide which is practically realistic. Therefore it makes sense to start with investigating the cooling equation (7) since it has only one unknown, namely the time constant. Secondly, the found time constant can be used as a starting point in the curve fitting of the heating equation (6) to obtain the thermal resistance. Lastly, the thermal capacitance is calculated according to $C_{\text{th}} = \frac{\tau}{R_{\text{th}}}$.

A. *Cooling time*

The cooling time only appears in the equation for $T_{\text{j,min}}$ but since $T_{\text{j,max}}$ is strongly dependent on $T_{\text{j,min}}$, both will change

by varying the cooling time. The experimental results are shown in Fig. 5. For small t_{off}, $T_{\text{j,min}}$ is way higher than the heatsink temperature. Longer t_{off} will lead to a $T_{\text{j,min}}$ close to the heatsink temperature. $T_{\text{j,max}}$ is less impacted by the change of t_{off} but still varies by 12°C. ΔT is therefore increasing for increasing t_{off} until it's maximum is reached.

By fitting the measurement results of Fig. 5 and (8) using the MATLAB curve fitting tool, we can determine the time constant. The results per sample are shown in Table I. The thermal time constant is around 1.6s. The R^2 and root mean square error (RMSE) values indicate the quality of the fitted curve. The equation after the curve fitting is also plotted in Fig. 5 as a black line.

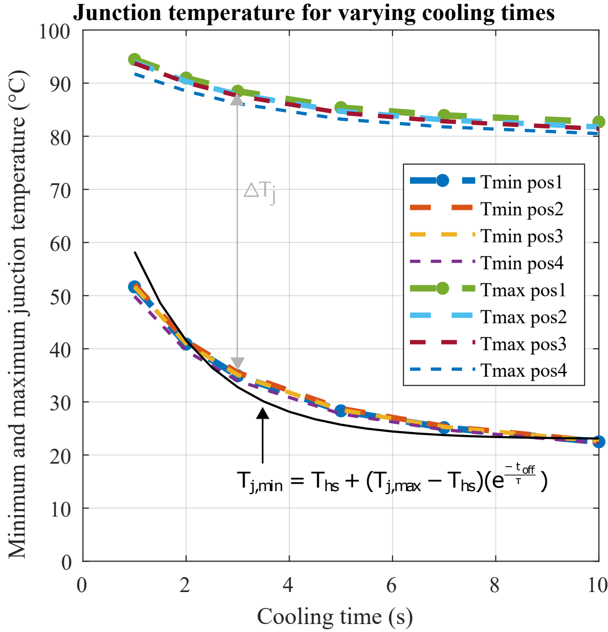

Fig. 5: The relation between the cooling time and minimum and maximum junction temperature. During the experiment $I_{\text{h}} = 10$A, $t_{\text{on}} = 5$s and $T_{\text{hs}} = 20^0$C.

TABLE I: Results for applying the curve fitting on experimental results of Fig. 5 where the cooling time is varying.

	Pos 1	Pos 2	Pos 3	Pos 4
τ	1.558	1.622	1.586	1.512
R^2	0.7677	0.7642	0.7623	0.7643
RMSE	5.293	5.393	5.33	5.053

B. Heating current

The power losses inside the device will act as a heating source and can be adjusted by selecting the heating current. The relation between the selected heating current, $T_{\text{j,max}}$ and $T_{\text{j,min}}$ is presented in Fig. 6. The selection of the heating current has a large impact on $T_{\text{j,max}}$ and is quadratically increasing as expected from (9). The effect on $T_{\text{j,min}}$ is minimal, in this configuration only 6°C increase is observed, arriving from the increase in $T_{\text{j,max}}$.

By using the curve fitting on the measured results and making use of (9), the thermal resistance and capacitance values are found and presented in Table II. Additionally, the R^2 and RMSE values of the fitted curve are presented in this table. The determined values for the thermal resistance and capacitance are higher than those from the datasheet of the IGBT namely $R_{\text{th}} = 1.67$ K/W and $C_{\text{th}} = 0.164$ Ws/K [23]. This might be because the values from the datasheet are optimistic or due to the addition of the thermal pad and heatsink. Since the R^2 value is almost 1, the theoretical expectation from (9) represents the measurement results well. The analytic equation, shown in black in Fig. 6, starts a little lower than the measurement results and overlaps when applying higher currents.

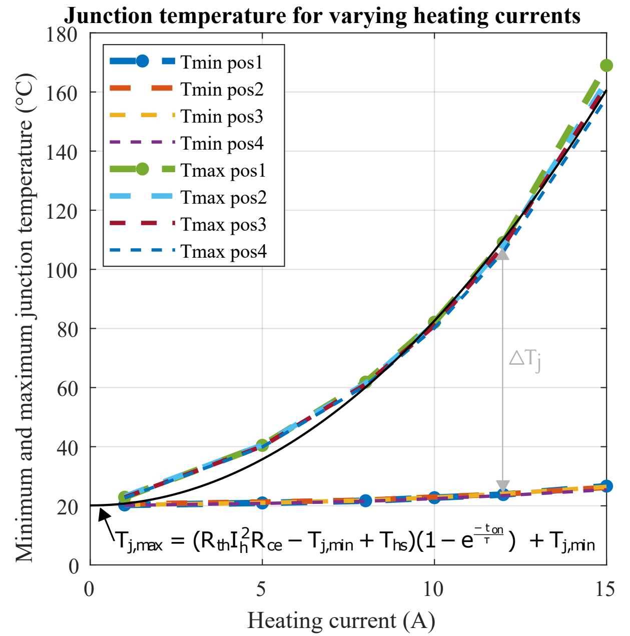

Fig. 6: The relation between the heating current and minimum and maximum junction temperature. During the experiment $t_{\text{on}} = 5$s, $t_{\text{off}} = 10$s and $T_{\text{hs}} = 20$°C.

TABLE II: Results for applying the curve fitting on experimental results of Fig. 6 where the heating currents is varying.

	Pos 1	Pos 2	Pos 3	Pos 4
τ (s)	2.000	1,756	1,600	1.600
R_{ce} (Ω)	0.2371	0.218	0.2327	0.2239
R_{th} (K/W)	2.965	3.066	2.808	2.846
C_{th} (Ws/K)	0.6745	0.5727	0.5698	0.5622
R^2	0.9958	0.9966	0.9971	0.9972
RMSE (K)	4.390	3.803	3.497	3.342

C. Heating time

In this experiment, the relation between the heating time and junction temperature is tested and the results are shown in Fig. 7. Increasing t_{on} will increase $T_{\text{j,max}}$ but eventually will

reach a maximum. The selection of t_{on} will have a range of 40°C on $T_{j,max}$ and 4°C on $T_{j,min}$ in this setup.

Matching (9) with the measurements, resulted in the time constant, thermal resistance and thermal capacitance as indicated in Table III. Also the electrical resistance for the best fitting is given, which varies slightly per sample. The found values for the time constant are lower than in the experiments before and therefore the thermal capacitance is also lower. The values of the thermal resistance are in the same range as the experiment with the varying heating current. The analytic equation has a larger slope and reaches it's asymptote sooner than the measured results.

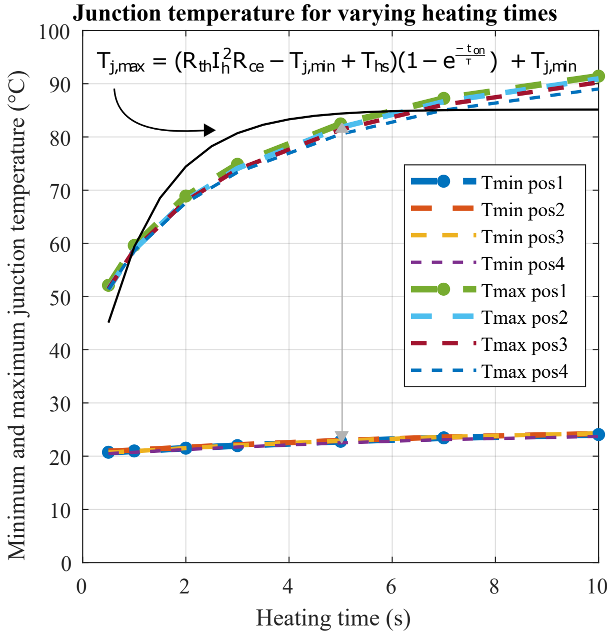

Fig. 7: The relation between the heating time and minimum and maximum junction temperature. During the experiment $I_h = 10$A, $t_{off} = 10$s and $T_{hs} = 20$°C.

TABLE III: Results for applying the curve fitting on experimental results of Fig. 7 where the heating time is varying.

	Pos 1	Pos 2	Pos 3	Pos 4
τ (s)	1.138	1,184	1,148	1.103
R_{ce} (Ω)	0.2243	0.2304	0.2348	0.2175
R_{th} (K/W)	2.909	2.816	2.734	2.898
C_{th} (Ws/K)	0.3946	0.4205	0.4199	0.3806
R^2	0.8555	0.8607	0.8560	0.8540
RMSE (K)	6.754	6.670	6.653	6.503

D. Heatsink temperature

The selection of the heatsink temperature is used to move both $T_{j,min}$ and $T_{j,max}$ in an even manner. By fixing the parameter in (8) and (9), the relation between $T_{j,min}$ and T_{hs} becomes linear similar to the relation between $T_{j,min}$ and T_{hs}. Nevertheless, the slopes are not the same and ΔT_j is slightly increasing as T_{hs} increases.

The results of the experiments with varying heatsink temperatures are shown in Fig. 8. The x-axis shows the setting of the heatsink temperature, but the exact temperature can vary. When the semiconductor devices are heating up, the heatsink area under and next to the device will heat up as well. The temperature sensor of the heatsink is placed lower in the aluminum and will not sense the local temperature fluctuations, the heat should first spread towards the sensor. The air temperature in the room can also have a slight influence on the actual temperature of the heatsink.

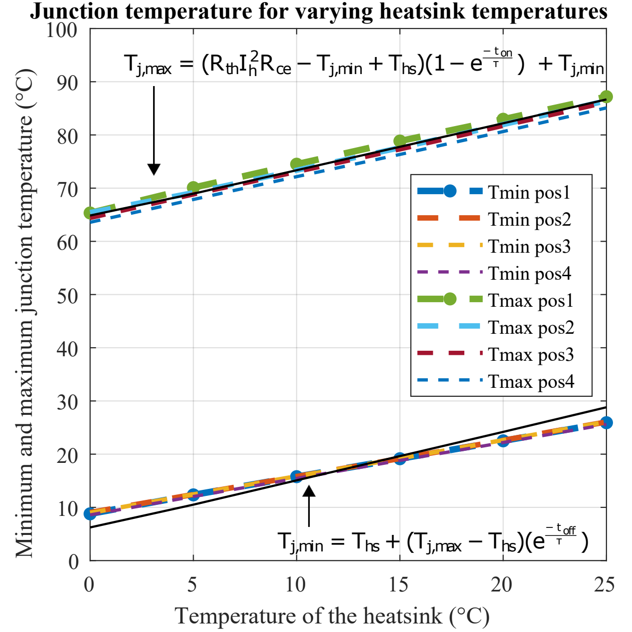

Fig. 8: The relation between the heatsink temperature and minimum and maximum junction temperature. During the experiment $I_h = 10$A, $t_{on} = 5$s and $t_{off} = 10$s.

When fitting equation (9) against the measurements results of $T_{j,max}$, the time constant, electric resistance, thermal resistance and thermal capacitance are found as shown in Table IV. The values are simular to the values obtained in the previous experiments. The measurement results for $T_{j,min}$ can also be plotted against equation (8). The resulting curve fitting parameters are presented in Table V. The curve fitting was improved by measuring the local heatsink temperature next to the IGBT with another temperature sensor instead of using the selected heatsink temperature. Even so, the values of the thermal time constant are doubled compared to previous experiments, which should not be possible since it is the same setup. We expect that the measured heatsink temperature does not correlate to the actual heatsink temperature at the attachment to the devices and therefore the obtained value of the thermal time constant is inaccurate in this curve fitting.

V. Conclusion

The reliability of semiconductor devices is an important research topic. In this paper, the accelerated power cycling

TABLE IV: The values obtained by curve fitting the experimental results of Fig. 8, where the heatsink temperture is varying to the cooling equation (9)

	Pos 1	**Pos 2**	**Pos 3**	**Pos 4**
τ **(s)**	1.505	1.500	2.000	1.548
$R_{ce}(\Omega)$	0.2219	0.2200	0.2265	0.2166
R_{th} **(K/W)**	2.885	2.871	2.771	2.854
C_{th} **(Ws/K)**	0.5217	0.5225	0.5734	0.5424
R^2	0.9591	0.9629	0.9736	0.9696
RMSE (K)	1.646	1.963	1.698	1.806

TABLE V: The values obtained by curve fitting the experimental results of Fig. 8 where the heatsink temperture is varying to the cooling equation (8).

	Pos 1	**Pos 2**	**Pos 3**	**Pos 4**
τ	3.584	3.640	3.652	3.529
R^2	0.893	0.891	0.893	0.889
RMSE	2.091	2.100	2.089	2.117

test is explained as well as the thermal model of the devices. Furthermore, the relation between the settings of the cooling time, heating current, heating time, and heatsink temperature are extensively tested against the resulting minimum and maximum junction temperature. During each test, the R^2 and RMSE values are good and verify the thermal model. The duration of several power cycling tests can take multiple days to even weeks. Therefore it is important to consider the cycle time, i.e. $t_{\text{on}} + t_{\text{off}}$, and keep it as low as possible while obtaining the desired temperature cycle. It is beneficial to use the heating currents as a free variable over the heating time to obtain the desired $T_{\text{j,max}}$ and keep the cycle time small. The heatsink temperature can be chosen over the cooling time to obtain $T_{\text{j,min}}$.

Furthermore, each test was used to calculate the thermal time constant and if possible also the electrical resistance, the thermal resistance, and the thermal capacitance. Throughout the tests, the obtained values are not identical but their average gives a rough estimate of the values. For this system, $\tau = 1.6$s, $R_{\text{th}} = 2.9$ K/W, $C_{\text{th}} = 0.5$ Ws/K and $R_{\text{ce}} = 220$ mΩ. Using the thermal model, a power cycling testbed with the desired temperature swing can be made.

The obtained thermal model and parameters make it possible to find a suitable power cycling testbed for different heating cycles and loading conditions. This will improve future reliability studies on silicon and silicon-carbide semiconductor power devices.

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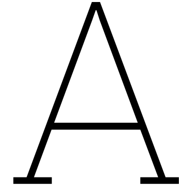


Electrical characteristics analysis

This section shows the measured values during the electrical characteristics analysis. In the test, one power supply is connected between the collector and emitter or drain and source of the IGBT or MOSFET, and the other power supply is connected between the gate and emitter or source. In order to supply negative voltages, the cables are reversed. The measured voltages and currents are summarized in the table below.

Table A.1: The results of the electrical characteristics analysis.

	$V_{\text{GE,GS}}$ (V)	$I_{\text{GE,GS}}$ (A)	$I_{\text{CE,DS}}$ (A)	$V_{\text{CE,DS}}$ (V)
IGBT	5	0	0	5.0
	7	0	1	1.2
	7	0	1.7	5.0
	10	0	1	0.9
	10	0	2	1.2
	10	0	3	1.3
	15	0	1	0.9
	15	0	2	1.1
	15	0	3	1.3
	15	0	4	1.5
MOSFET forward mode	5	0	0	5
	5	0	0.2	10
	10	0	1	0.5
	10	0	2	1.2
	10	0	3	1.8
	15	0	1	0.2
	15	0	2	0.4
	15	0	3	0.6
	15	0	4	0.8
	15	0	5	1.0
MOSFET body diode	0	0	-0.5	-2.4
	0	0	-1	-2.7
	0	0	-2	-2.9
	-2	0	-0.5	-2.8
	-2	0	-1	-3.0
	-2	0	-1.5	-3.2
	-2	0	-2	-3.3
	-2.8	0	-0.5	-3.0
	-2.8	0	-1	-3.1
	-2.8	0	-1.5	-3.3
	-2.8	0	-2	-3.4

B
Thermal response measurement

The thermal response measurement is executed for different heating currents. During the test, the heating time t_{on} is set to 10 seconds, the cooling time t_{off} is set to 30 seconds, and the heatsink temperature T_{hs} is set to 20 degrees Celcius. The results for the 4 IGBTs are presented in Figure B.1, B.2, B.3 and B.4 and the results for the 4 MOSFETs are presented in Figure B.5, B.6, B.7 and B.8. The corresponding cumulative structure functions are presented in Figure B.9, B.10, B.11, B.12, B.13, B.14, B.15 and B.16. The time constant spectrum of the different samples of the IGBT and MOSFET are given in Figure B.17 and B.19. The time constant spectrum for different heating currents is given in Figure B.18 and B.20.

B.1. Thermal response measurement

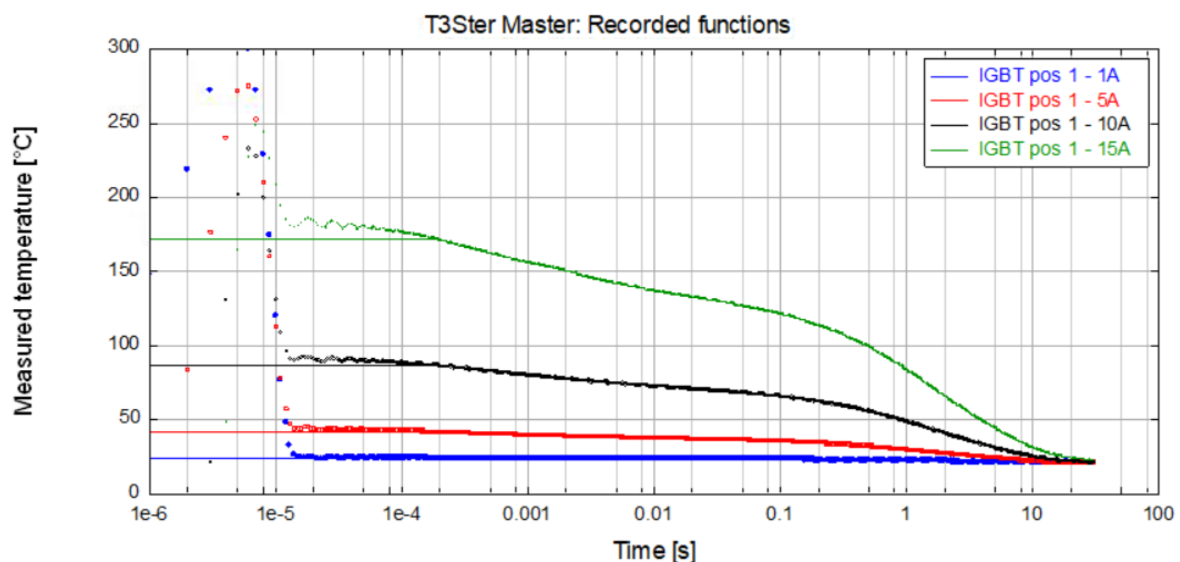


Figure B.1: The thermal response measurement for different heating currents for IGBT position 1.

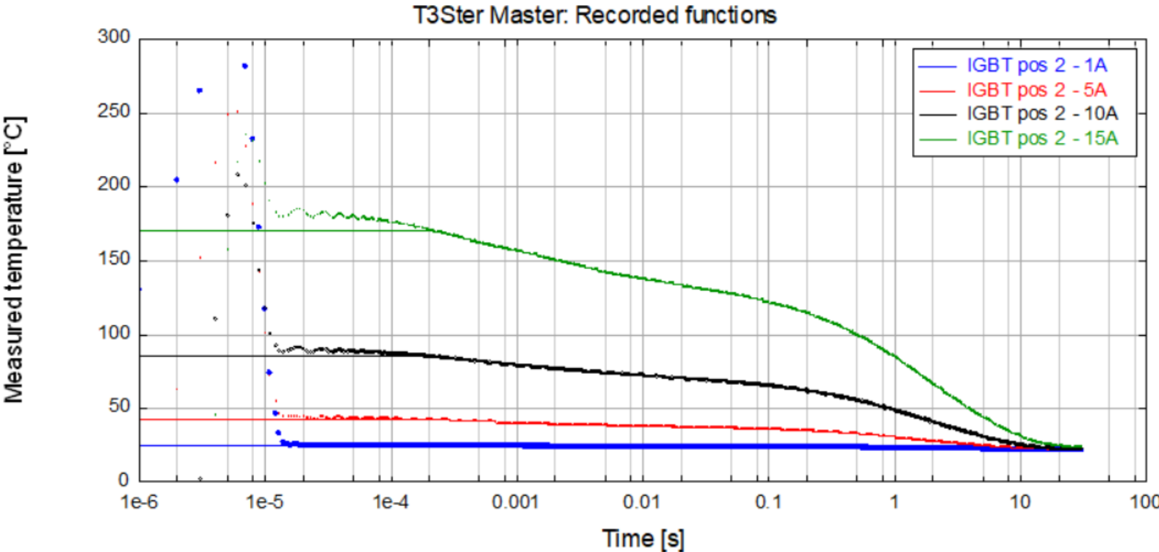


Figure B.2: The thermal response measurement for different heating currents for IGBT position 2.

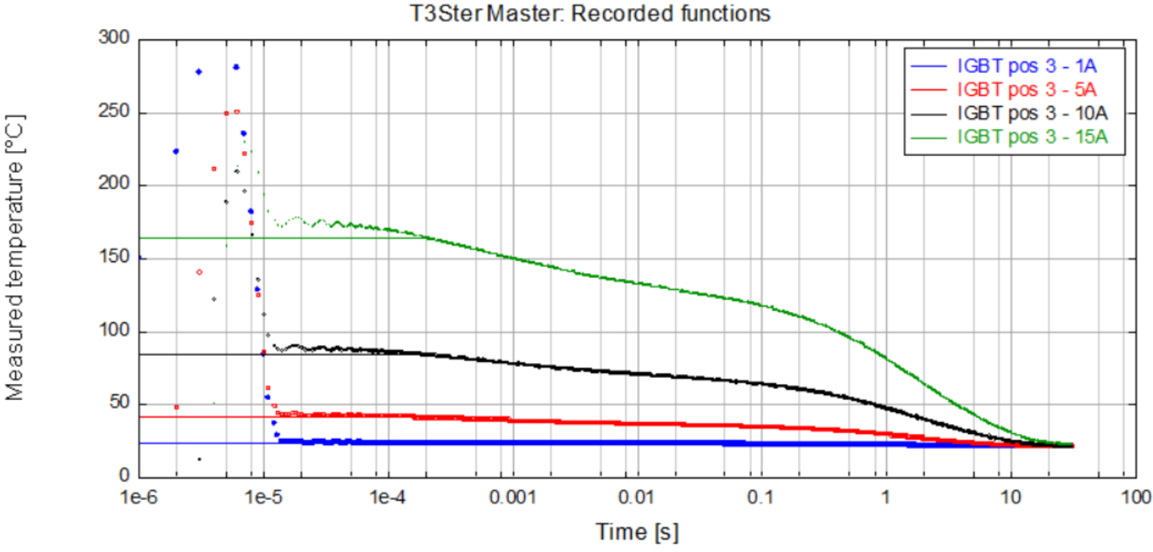


Figure B.3: The thermal response measurement for different heating currents for IGBT position 3.

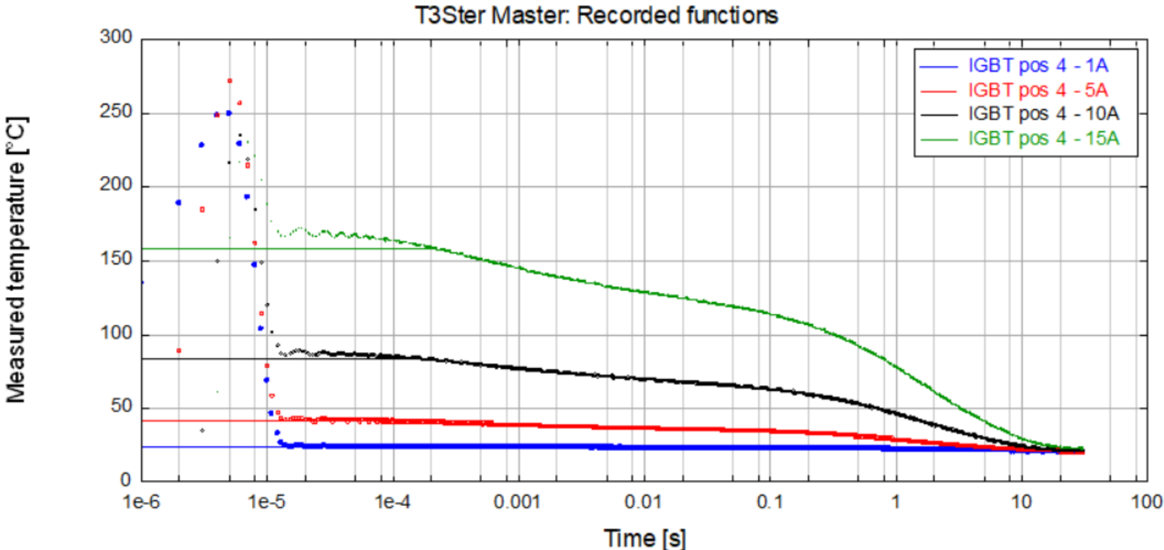


Figure B.4: The thermal response measurement for different heating currents for IGBT position 4.

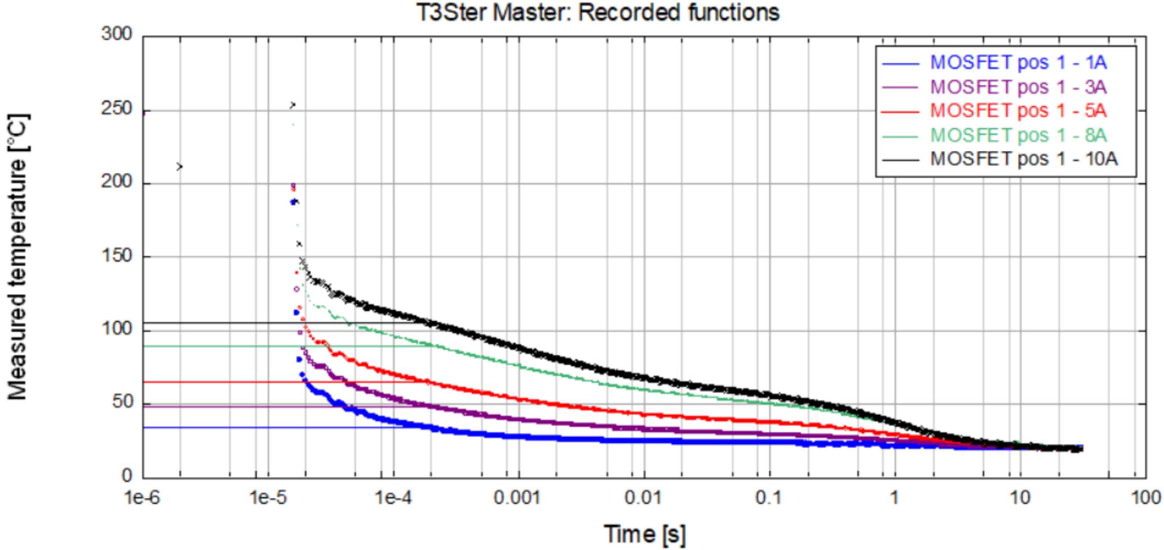


Figure B.5: The thermal response measurement for different heating currents for MOSFET position 1.

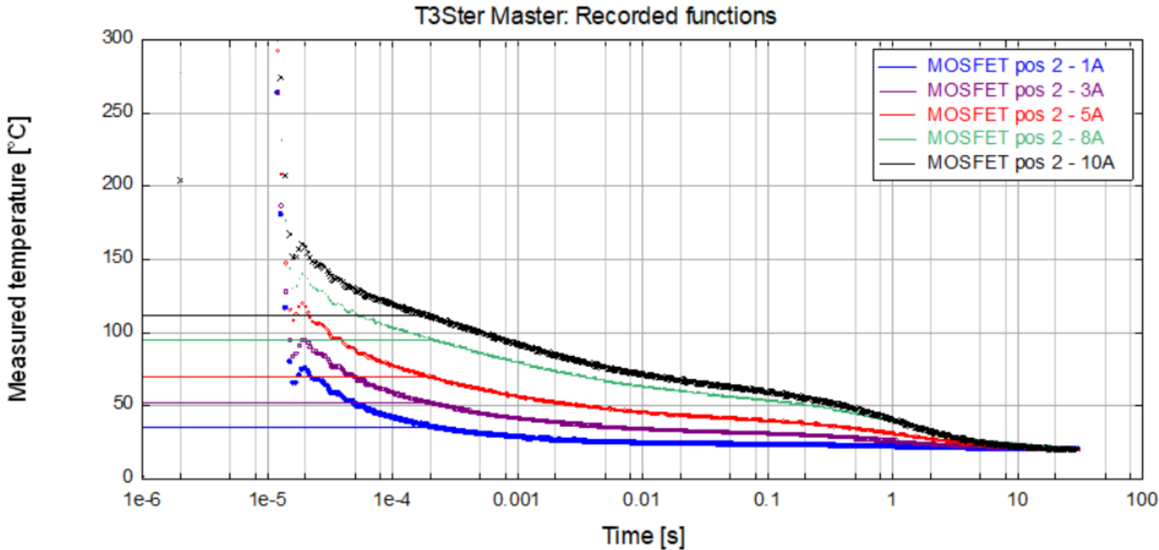


Figure B.6: The thermal response measurement for different heating currents for MOSFET position 2.

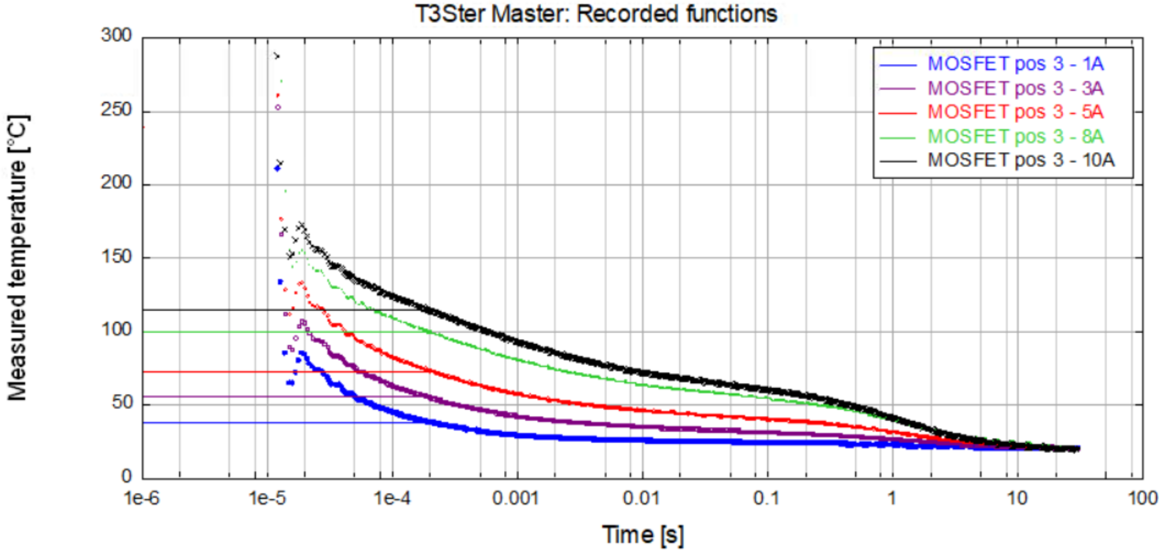


Figure B.7: The thermal response measurement for different heating currents for MOSFET position 3.

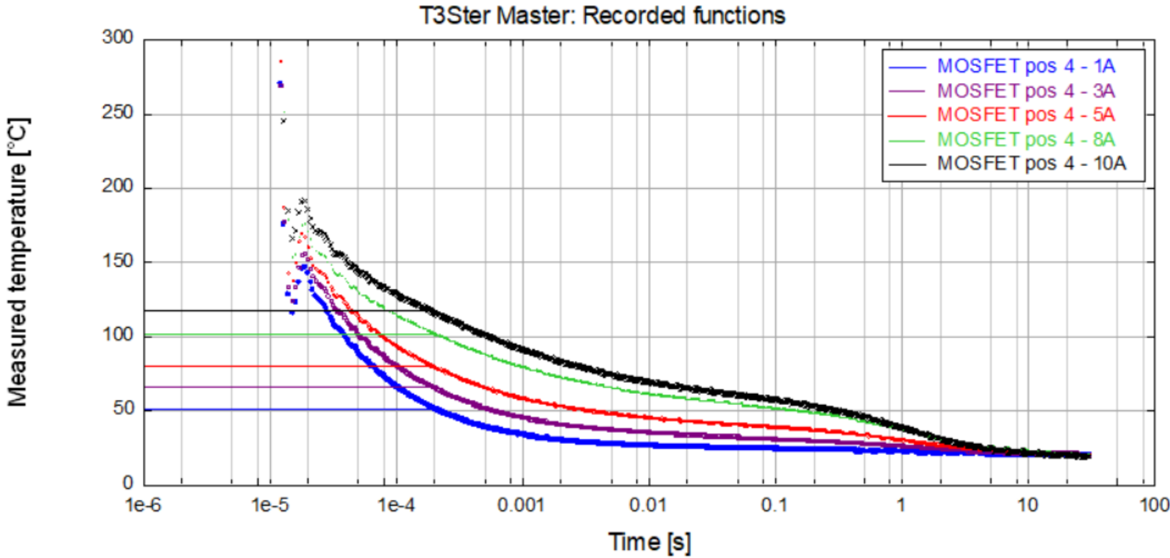


Figure B.8: The thermal response measurement for different heating currents for MOSFET position 4.

B.2. Cumulative structure function

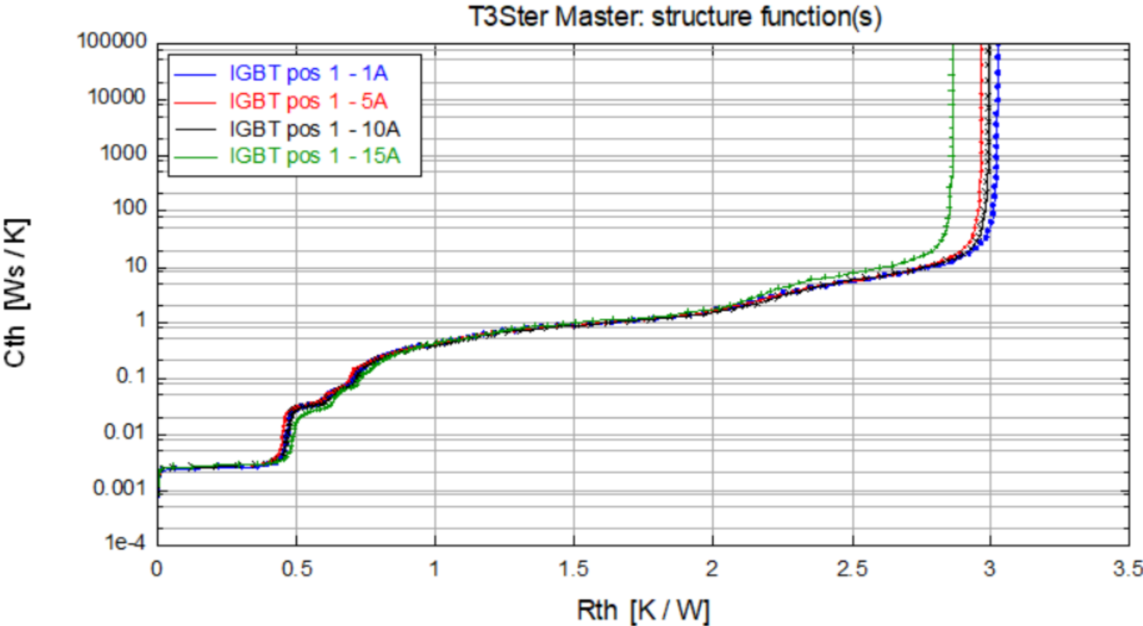


Figure B.9: The cumulative structure function for different currents for IGBT position 1.

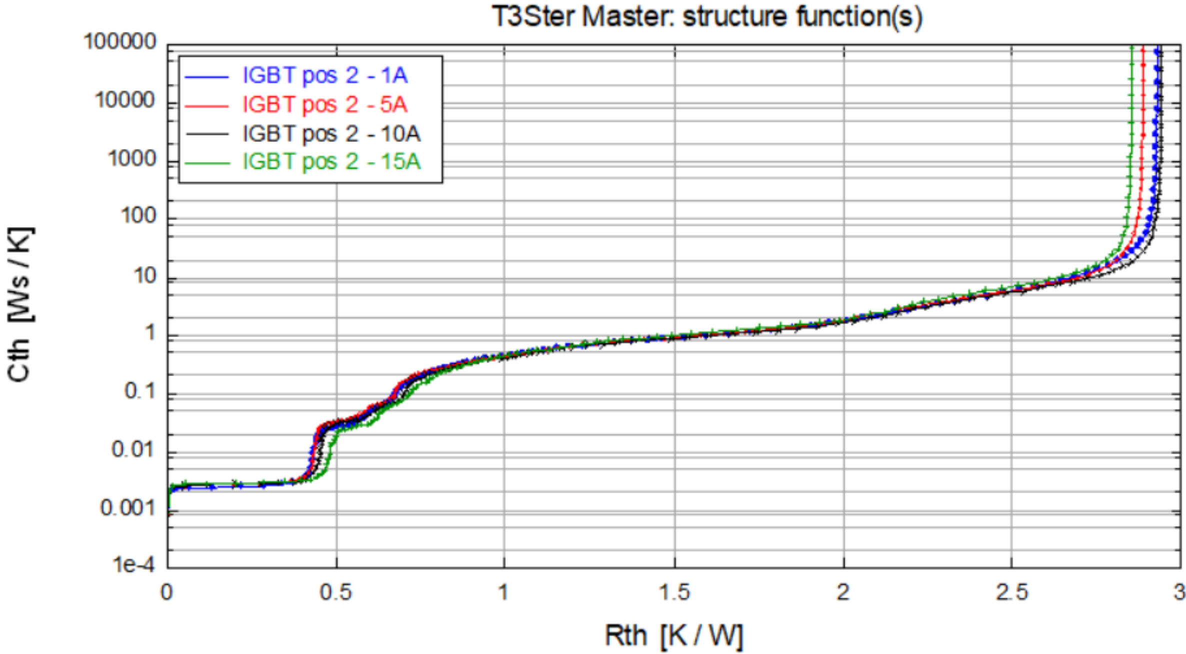


Figure B.10: The cumulative structure function for different currents for IGBT position 2.

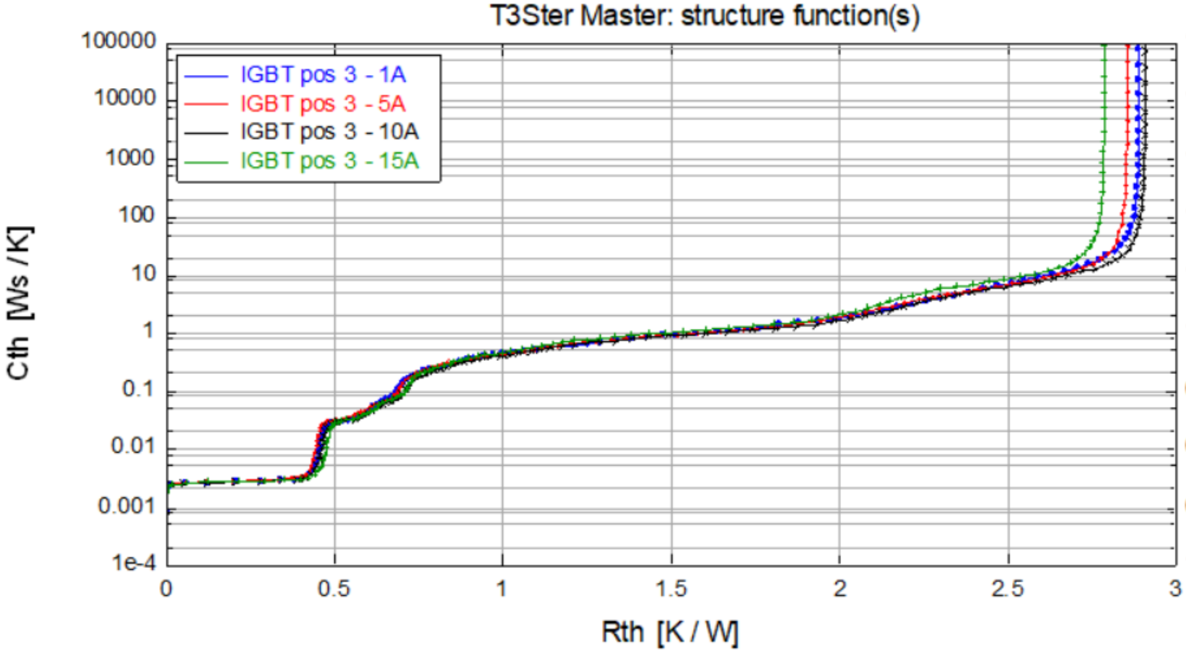


Figure B.11: The cumulative structure function for different currents for IGBT position 3.

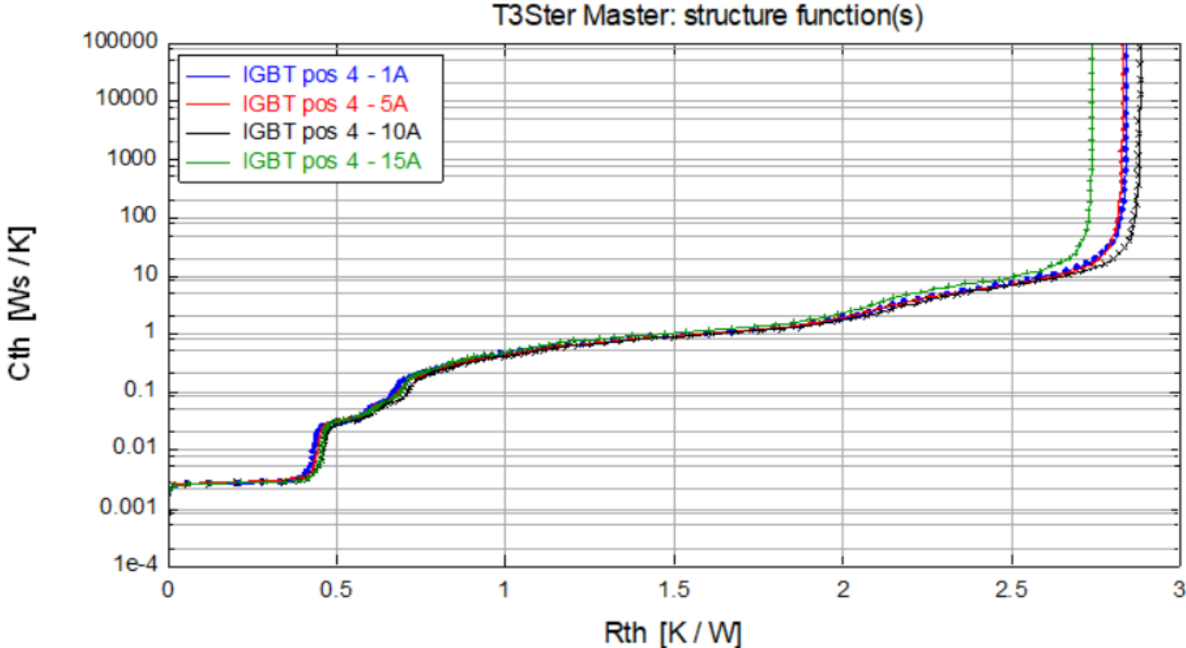


Figure B.12: The cumulative structure function for different currents for IGBT position 4.

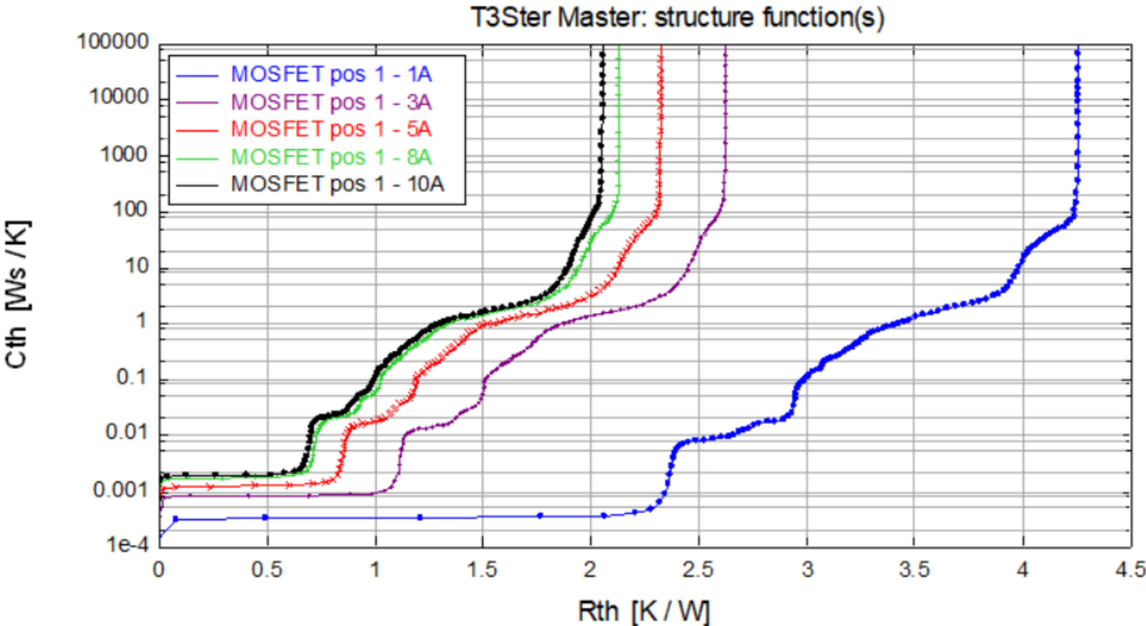


Figure B.13: The cumulative structure function for different currents for MOSFET position 1.

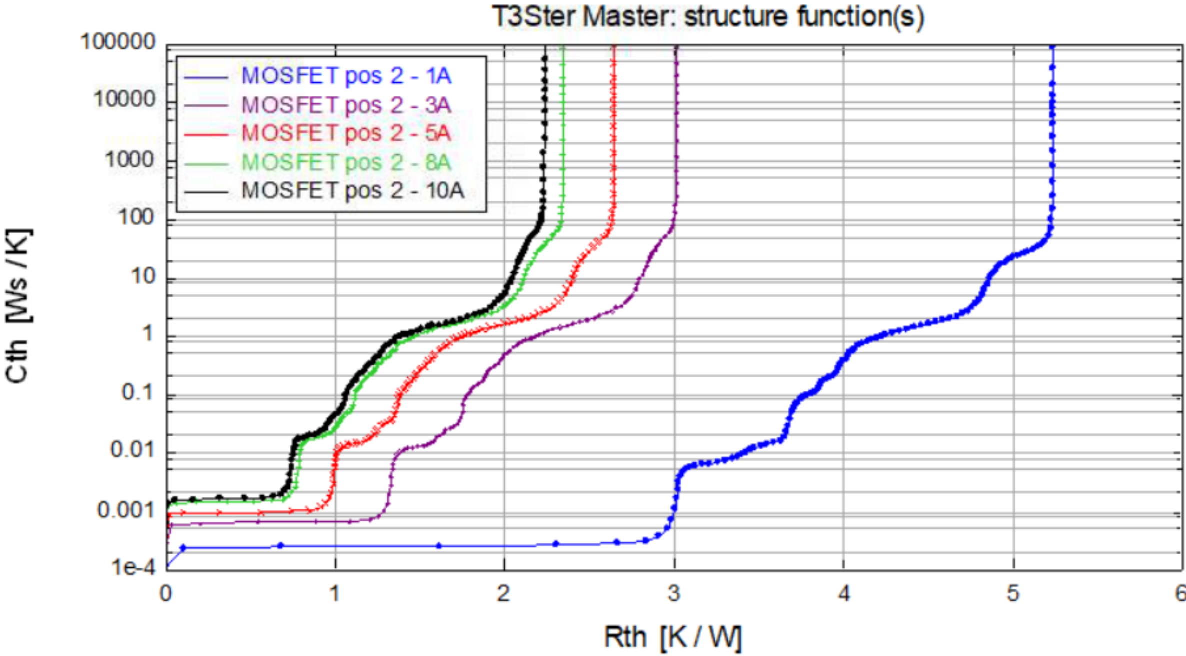


Figure B.14: The cumulative structure function for different currents for MOSFET position 2.

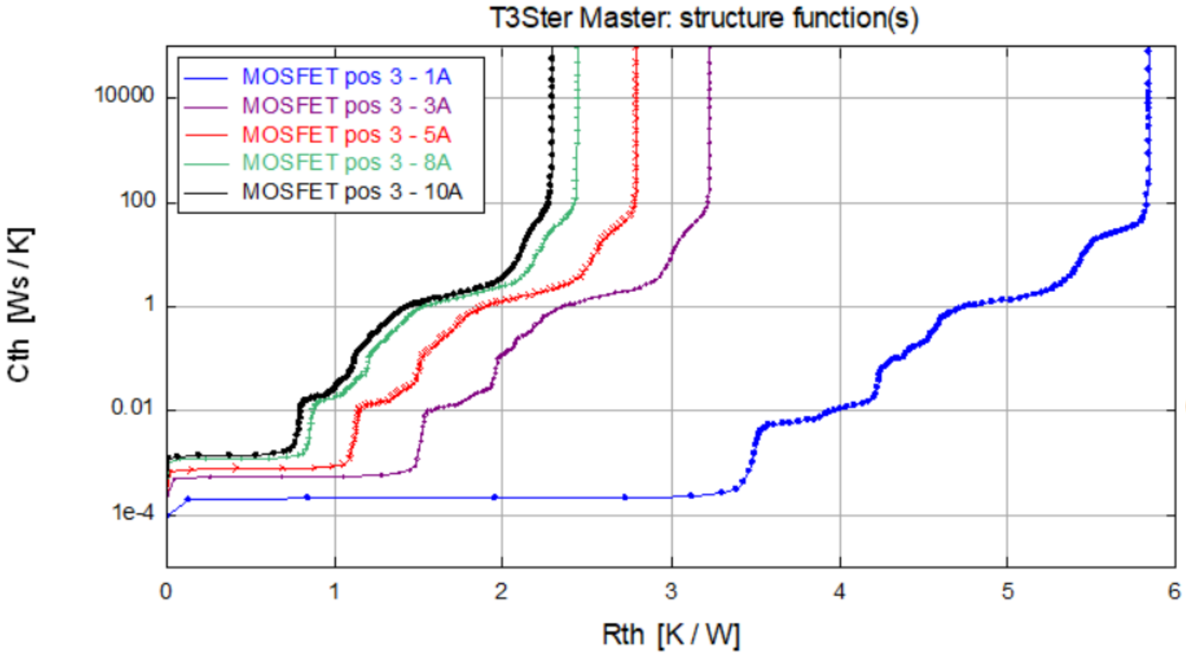


Figure B.15: The cumulative structure function for different currents for MOSFET position 3.

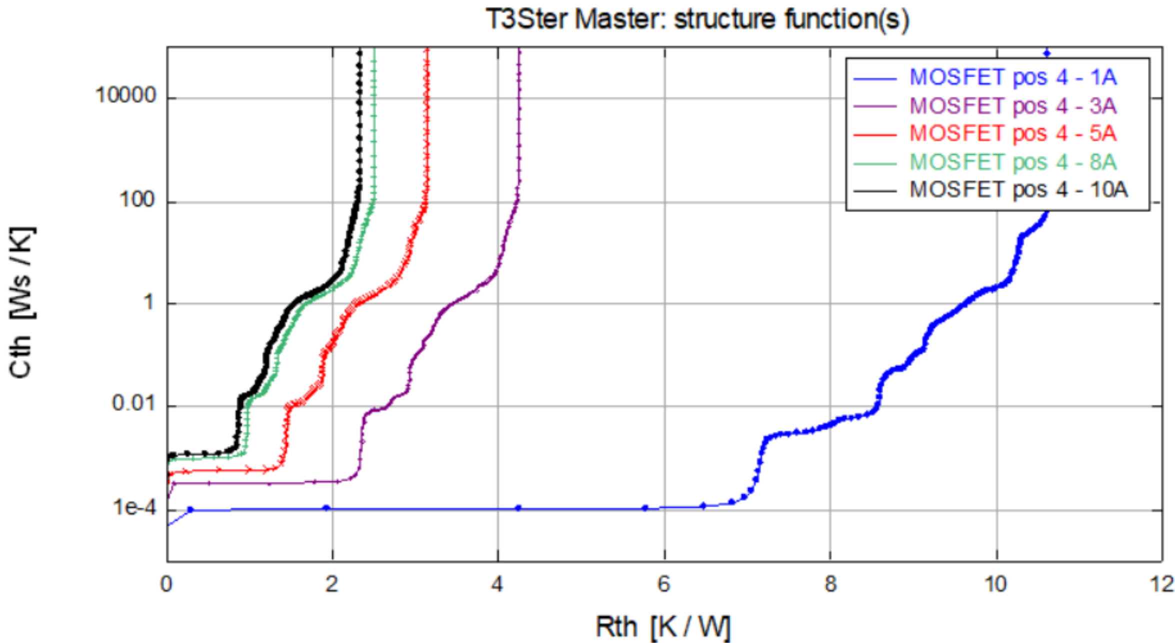


Figure B.16: The cumulative structure function for different currents for MOSFET position 4.

B.3. Time constant spectrum

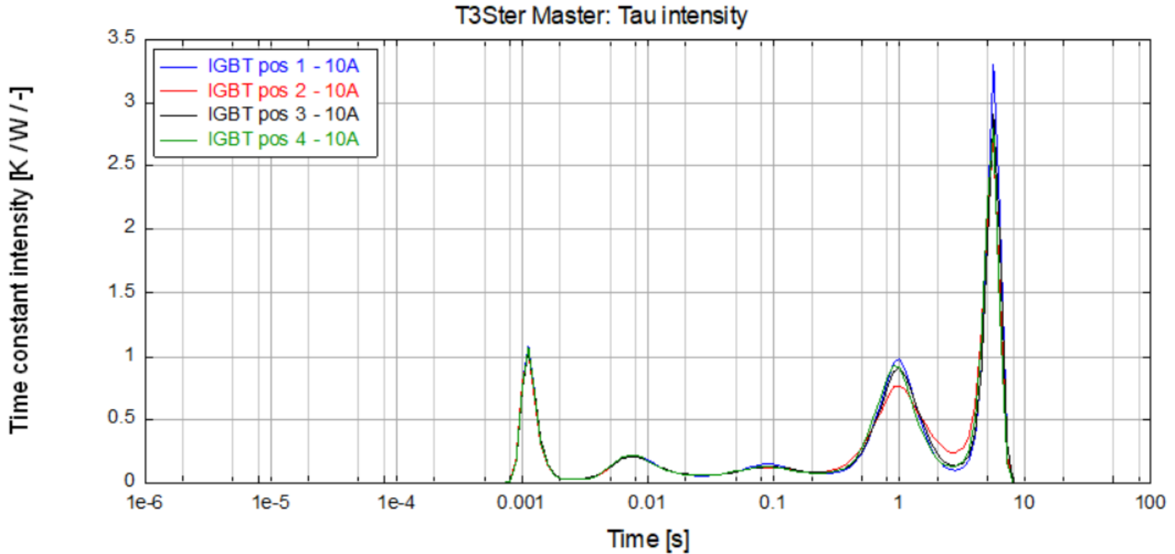


Figure B.17: The time constant spectrum of the 4 IGBTs.

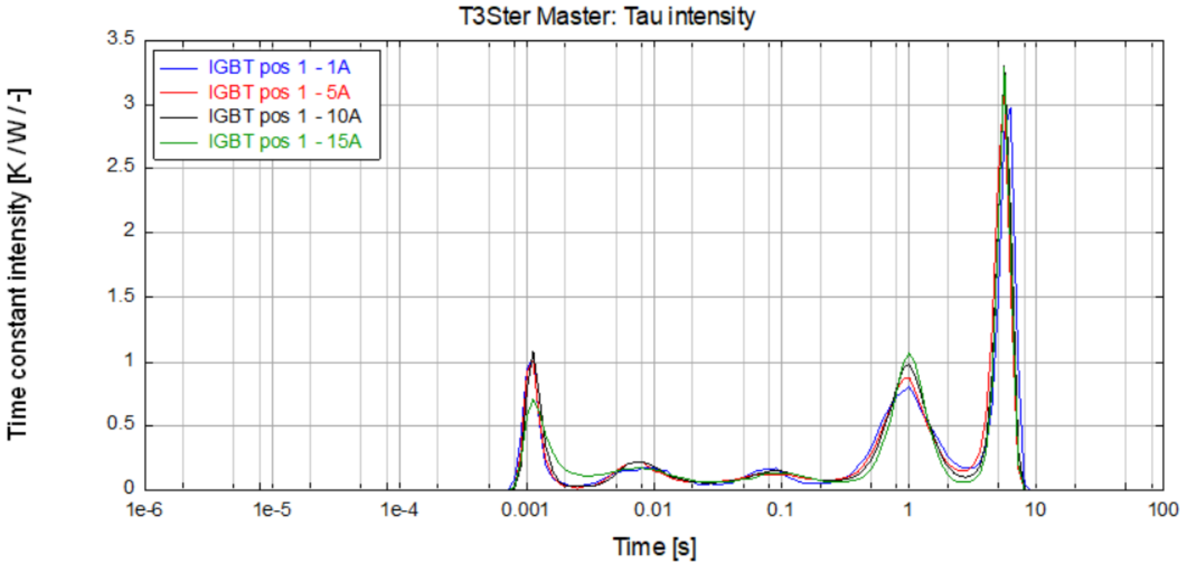


Figure B.18: The time constant spectrum for the IGBT at different heating currents.

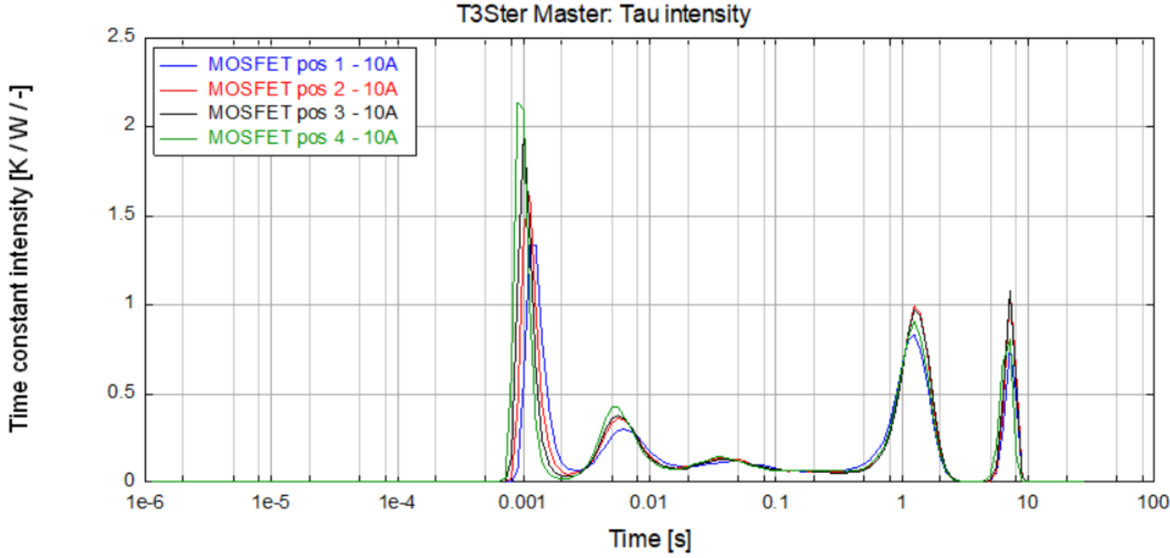


Figure B.19: The time constant spectrum of the 4 MOSFETs.

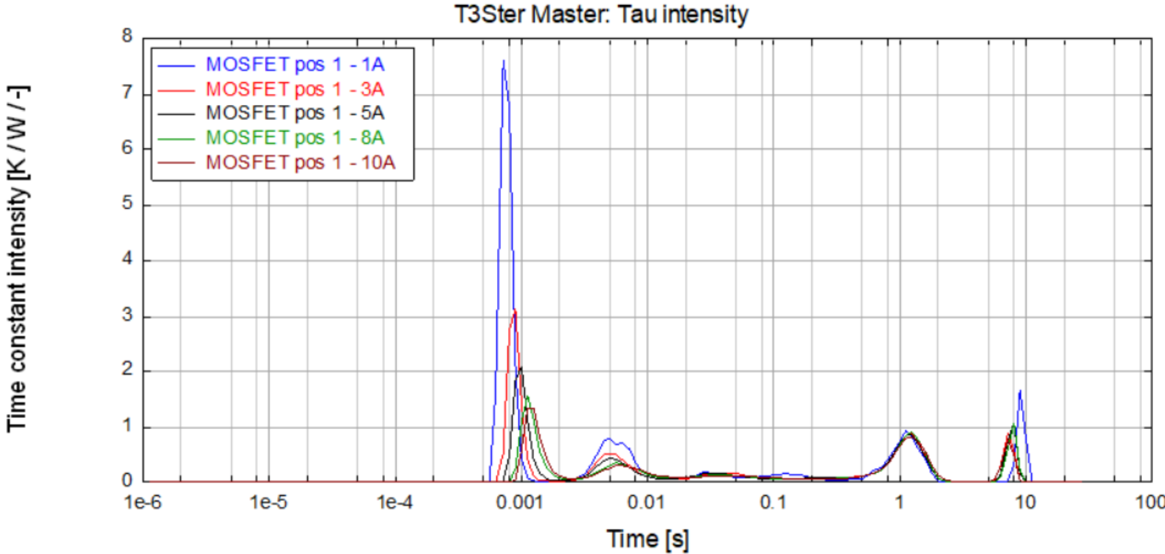


Figure B.20: The time constant spectrum of the MOSFET at different heating currents.

C
Experiment A

This chapter shows the measurement results of the power cycling test of experiment A. The heating current, electric resistance, and voltages are presented. Furthermore, the minimum and maximum junction temperatures are shown focussed on the effect of the thermal response measurement. In addition, the results for the thermal response measurements are presented as well as the cumulative structure functions os the samples.

C.1. Experiment A: I_{h} and R_{ce}

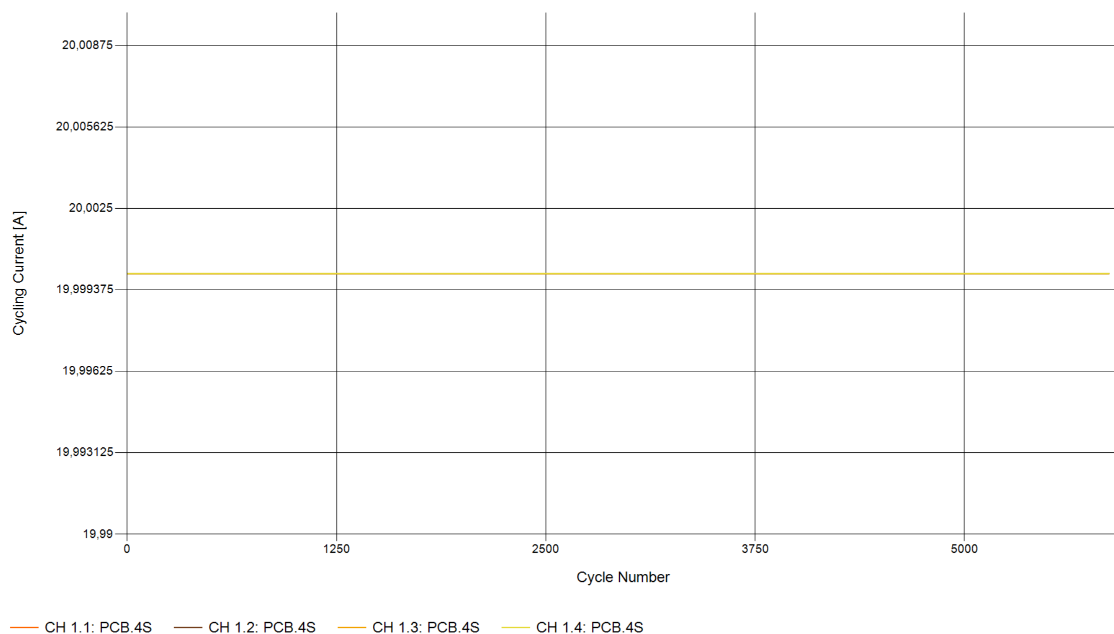


Figure C.1: The collector-emitter current per cycle during experiment A.

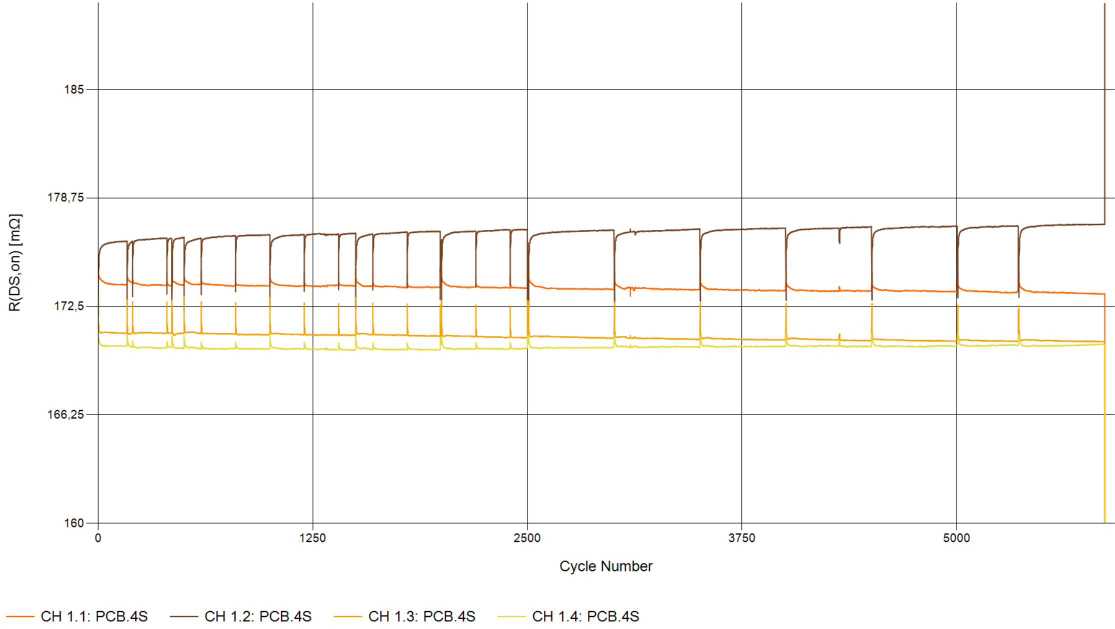


Figure C.2: The electric resistance between the collector and emitter during experiment A.

C.2. Experiment A: V_{on}, V_{hot} and V_{cold}

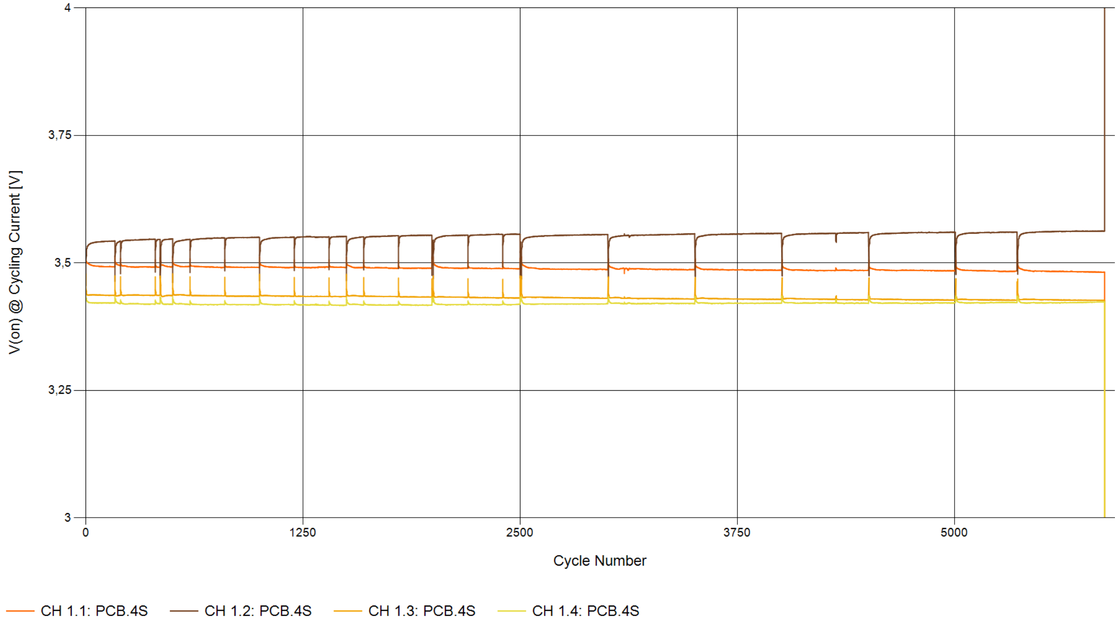


Figure C.3: The on voltages per cycle during experiment A.

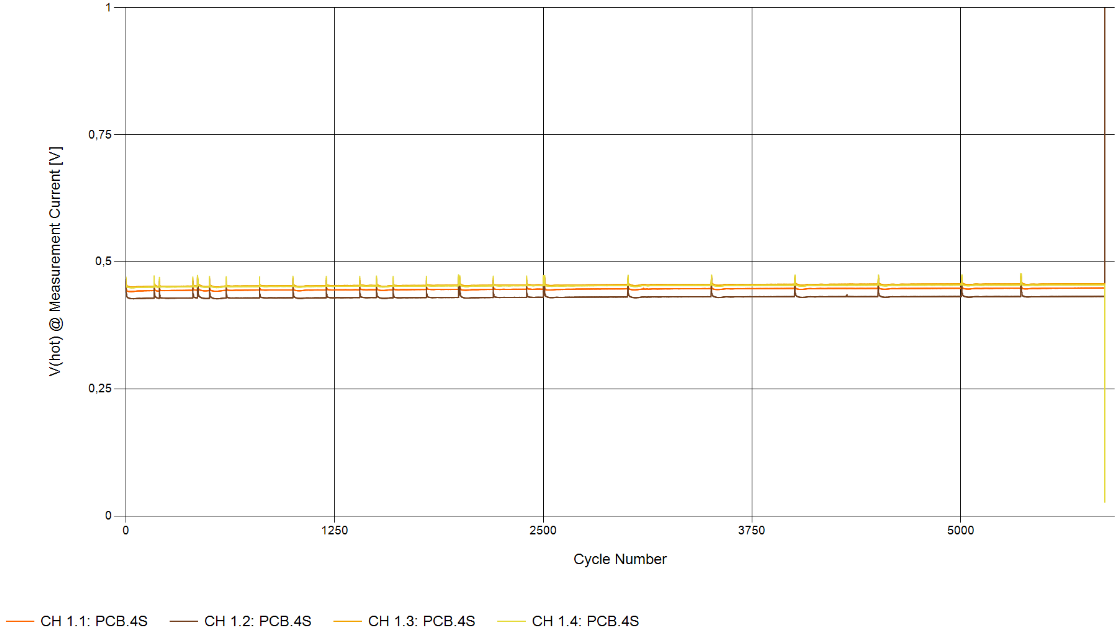


Figure C.4: The voltages used to calculate the maximum junction temperatures per cycle during experiment A.

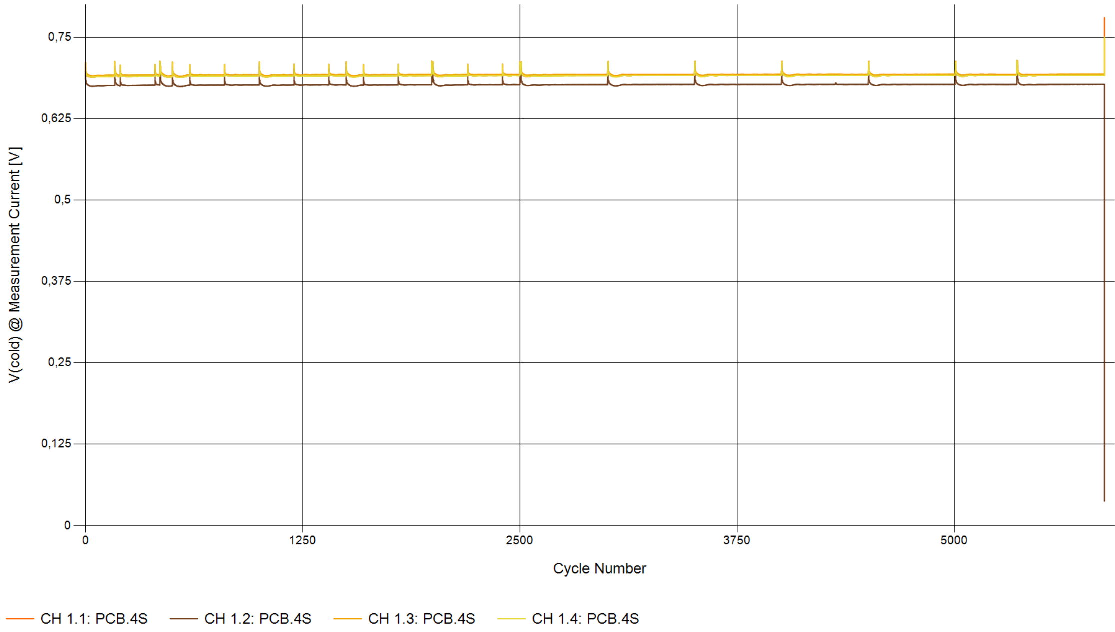
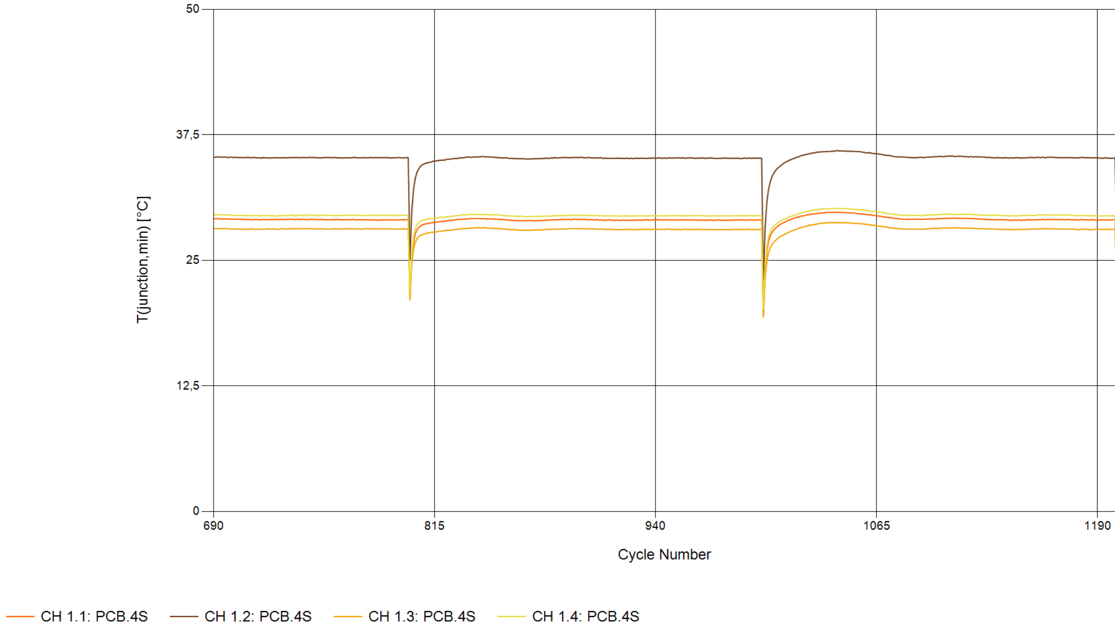
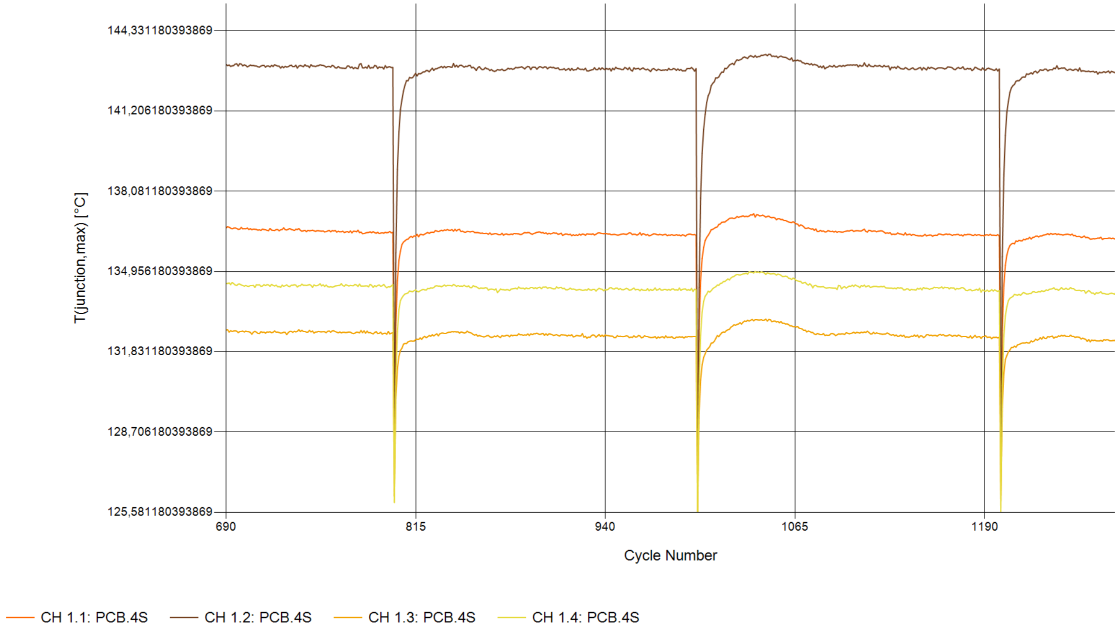


Figure C.5: The voltages used to calculate the minimum junction temperatures per cycle during experiment A.

C.3. Experiment A: minimum and maximum junction temperatures zoomed in to see the effect of the thermal response measurement



(a) The minimum junction temperature.



(b) The maximum junction temperature.

Figure C.6: The minimum and maximum junction temperature during experiment A where $I_h = 20$ A, $t_{on} = 1$ s, $t_{off} = 3$ s and $T_{hs} = 5°$ C. The graphs are zoomed in to see the effect of the thermal response measurement.

C.4. Experiment A: The thermal response measurement and structure functions of samples 1, 2, 3, and 4

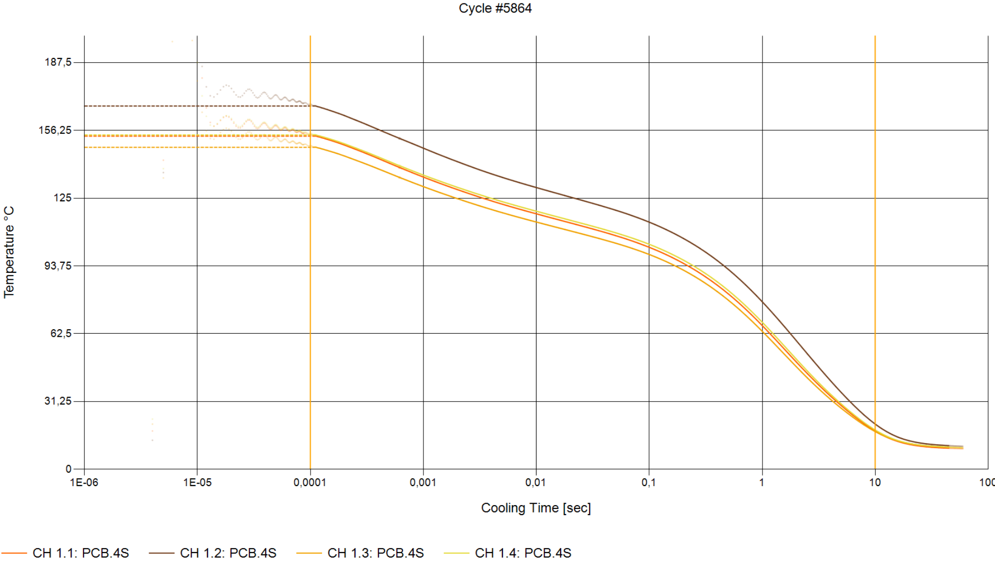


Figure C.7: The junction temperature during the thermal response measurement of cycle 5864 of experiment A.

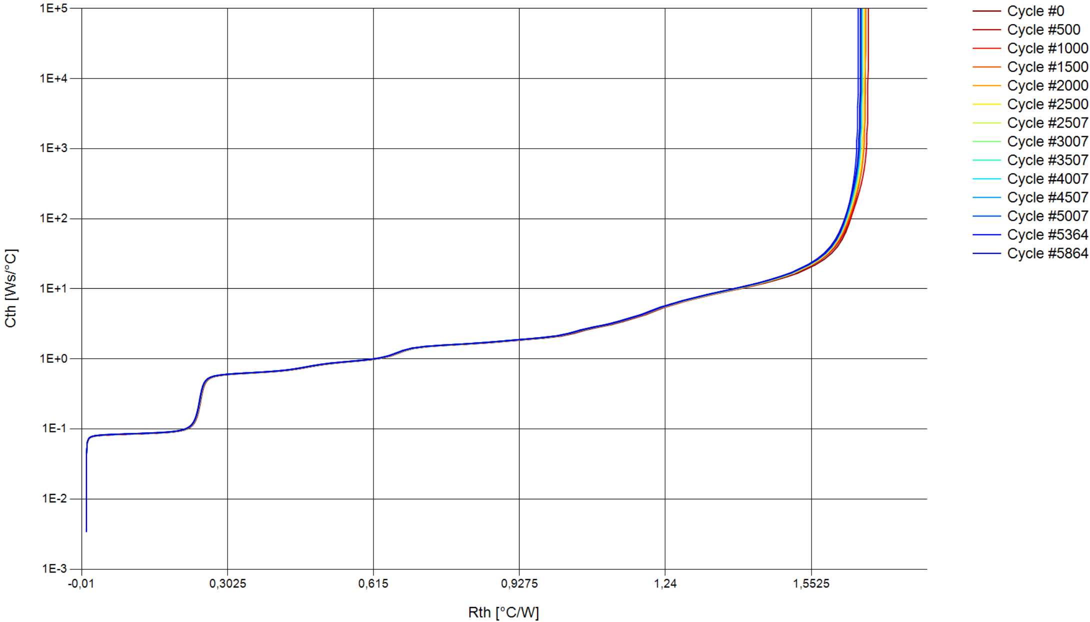


Figure C.8: The structure functions of sample 1 during experiment A.

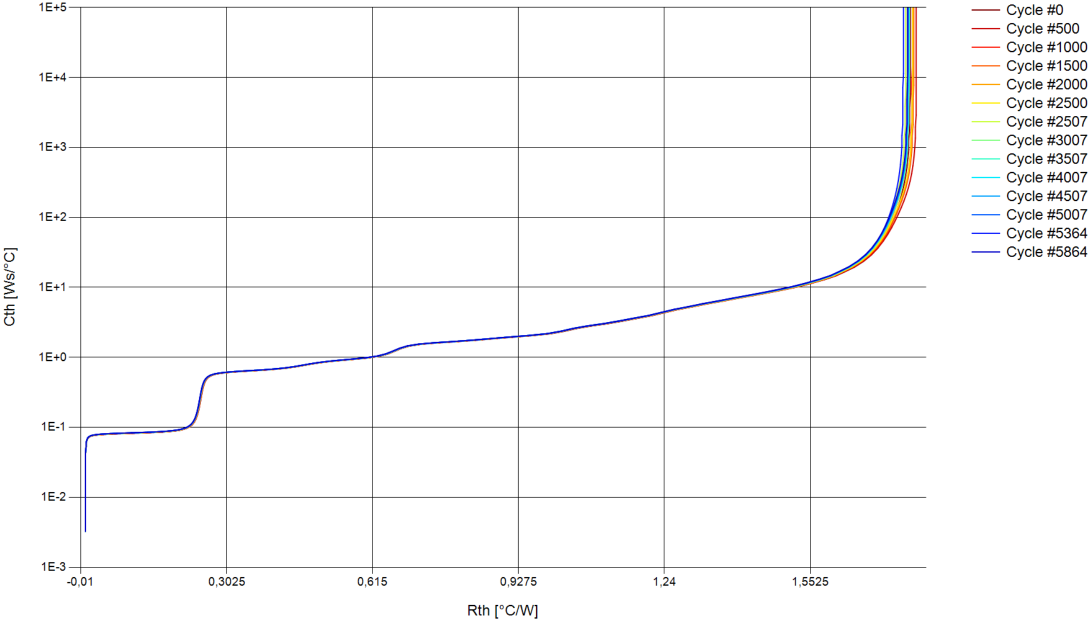


Figure C.9: The structure functions of sample 2 during experiment A.

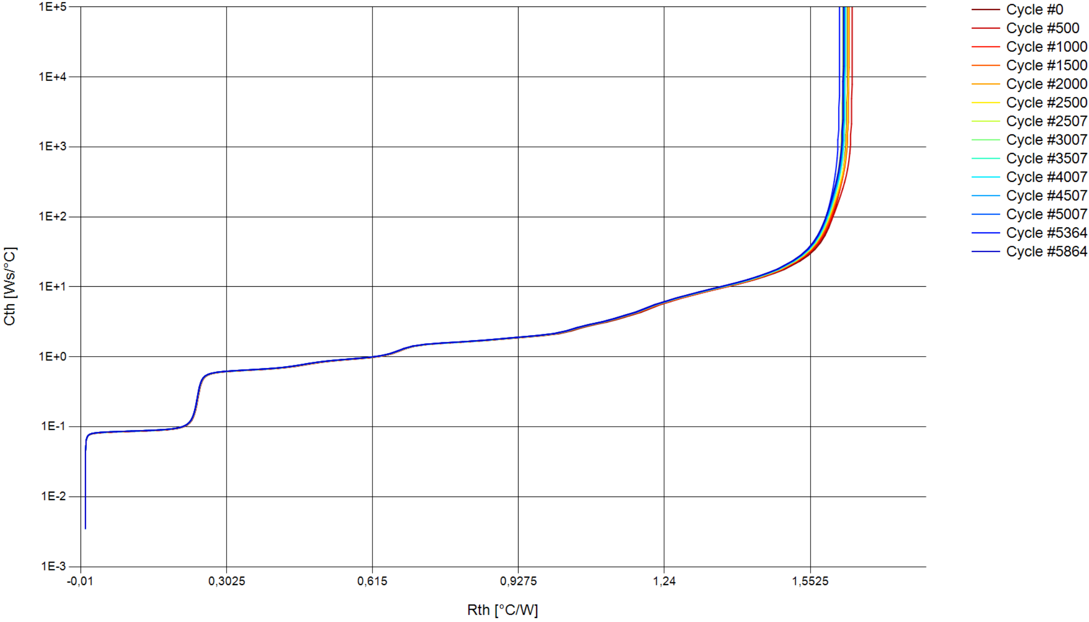


Figure C.10: The structure functions of sample 3 during experiment A.

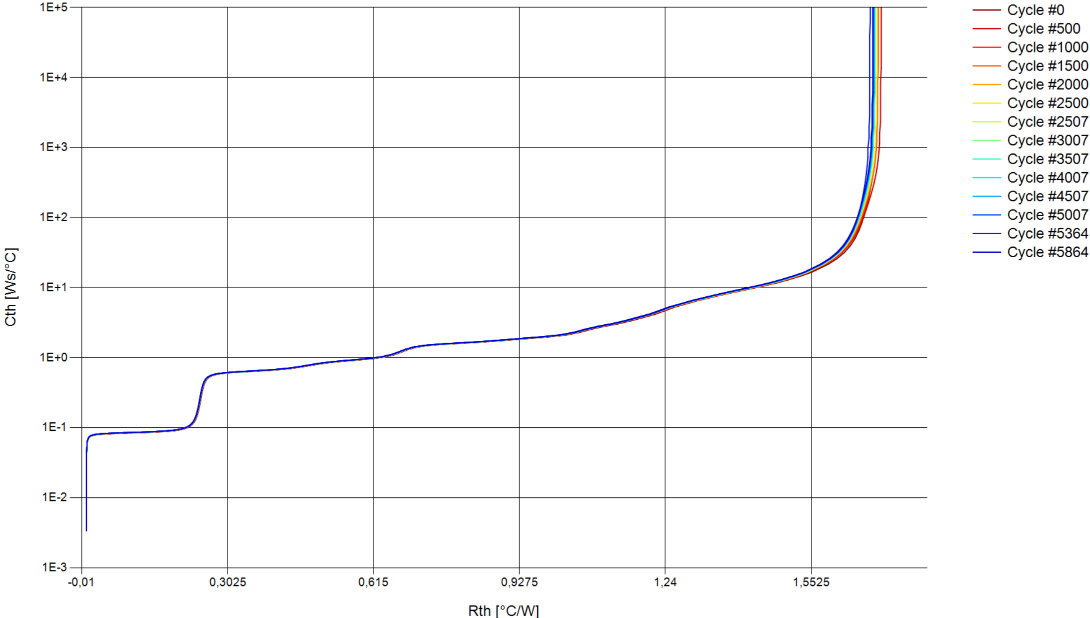


Figure C.11: The structure functions of sample 4 during experiment A.

D

Experiment B

This chapter presents the results of the power cycling test of the 13 cycles of experiment B. First, the voltage during cycles 1 and 11 are given followed by the on-voltage, hot-voltage, cold-voltage, current, power, and electric resistance throughout the experiment. Moreover, the minimum and maximum junction temperatures and temperature deviation is given.

D.1. Experiment B: Electric parameters

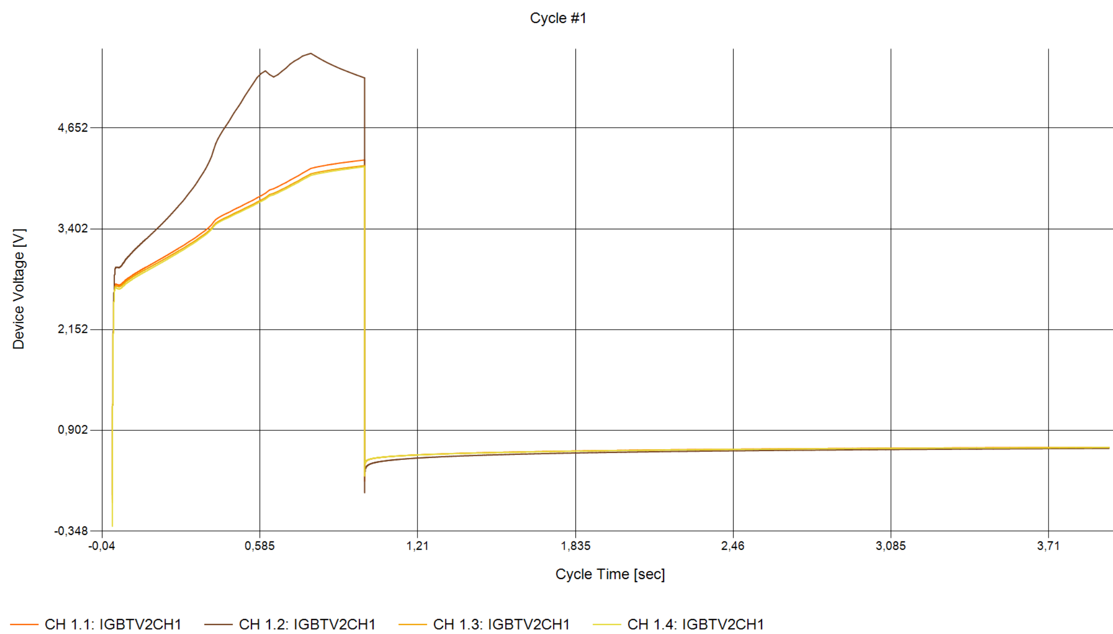


Figure D.1: The measured voltage during cycle 1 of experiment B.

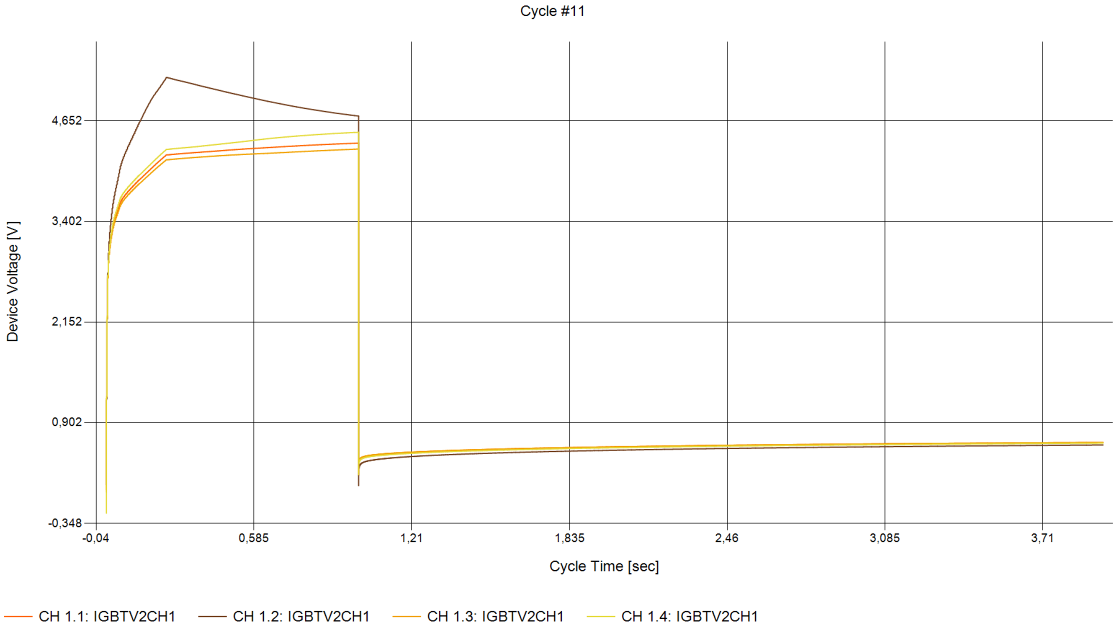


Figure D.2: The measured voltage during cycle 11 of experiment B.

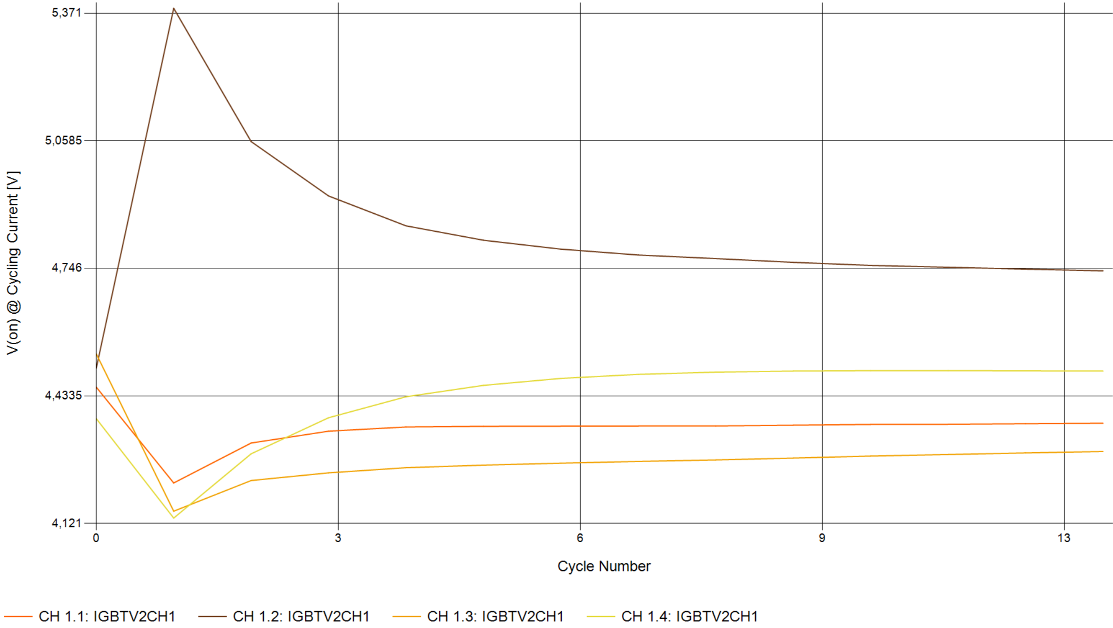


Figure D.3: The on voltages per cycle during experiment B.

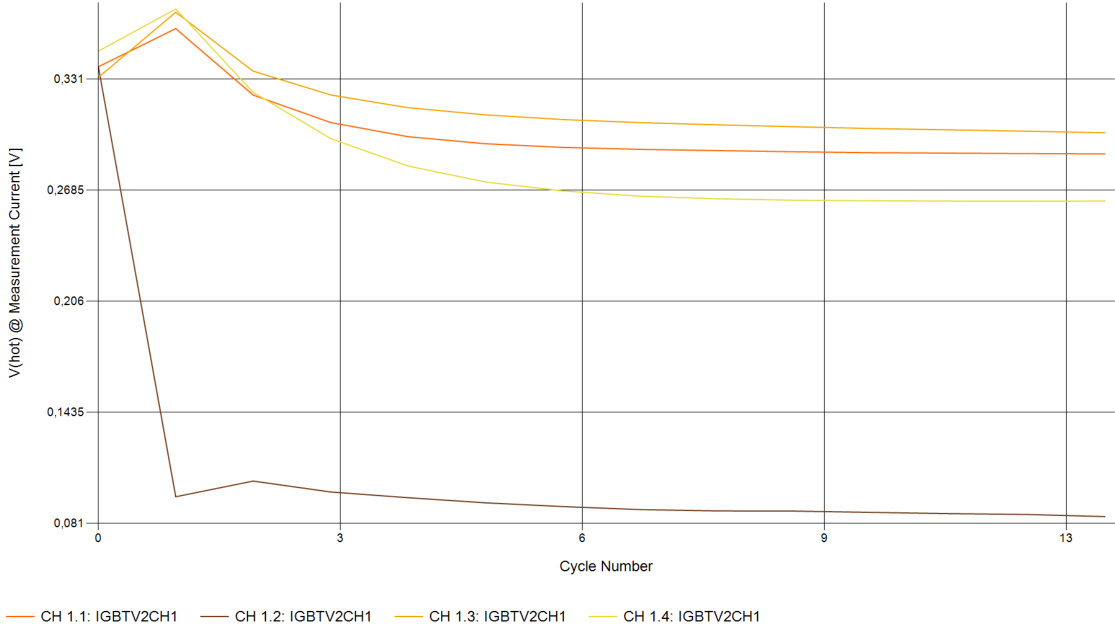


Figure D.4: The voltages used to calculate the maximum junction temperatures per cycle during experiment B.

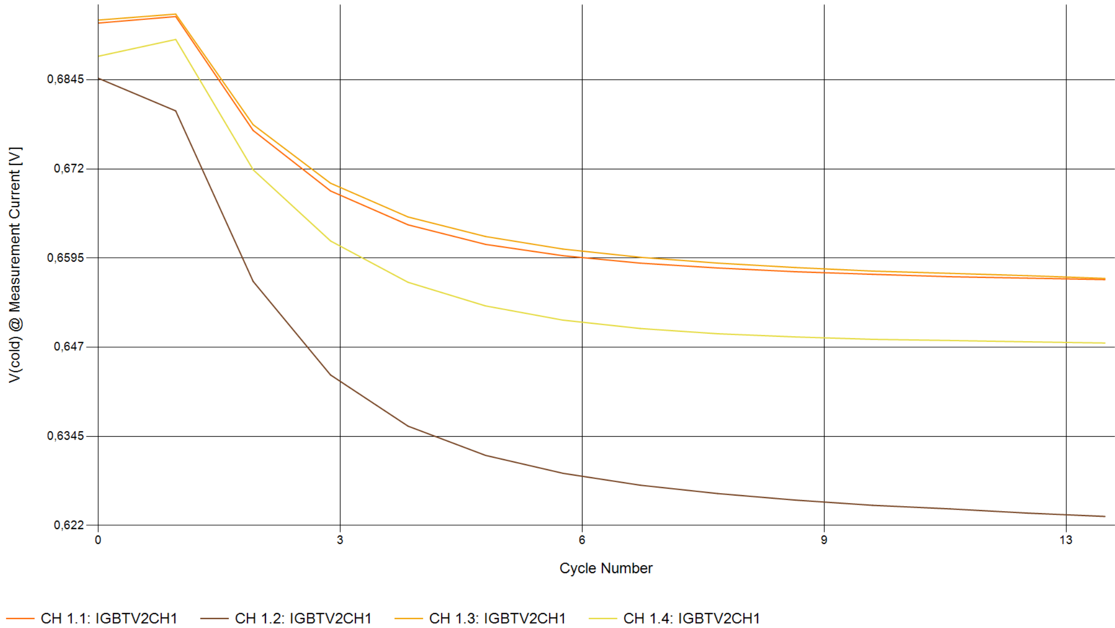


Figure D.5: The voltages used to calculate the minimum junction temperatures per cycle during experiment B.

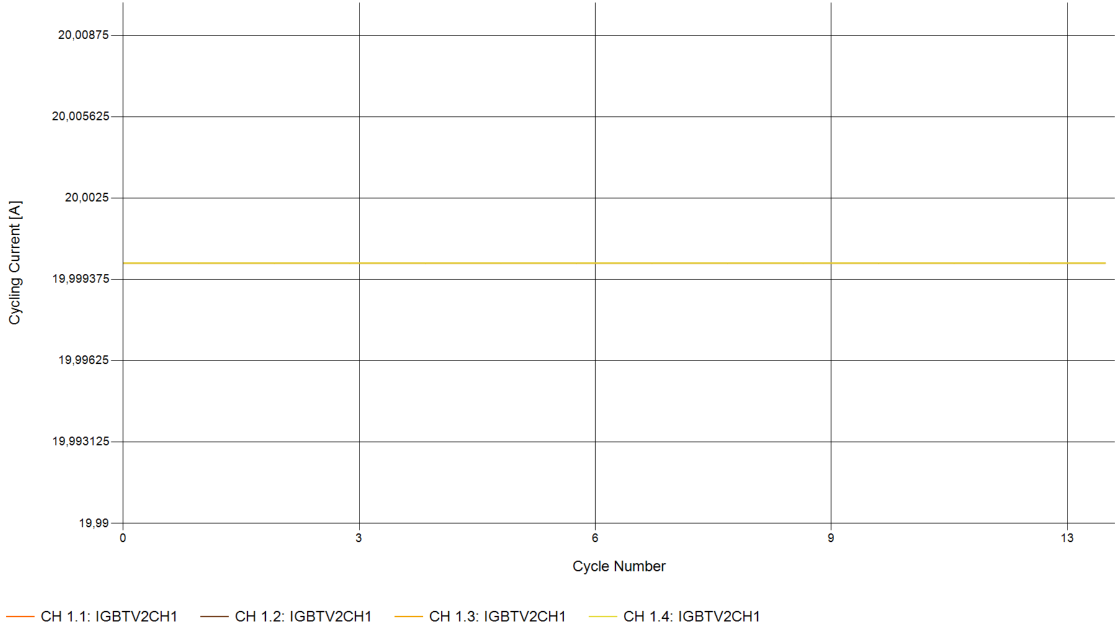


Figure D.6: The heating current during experiment B.

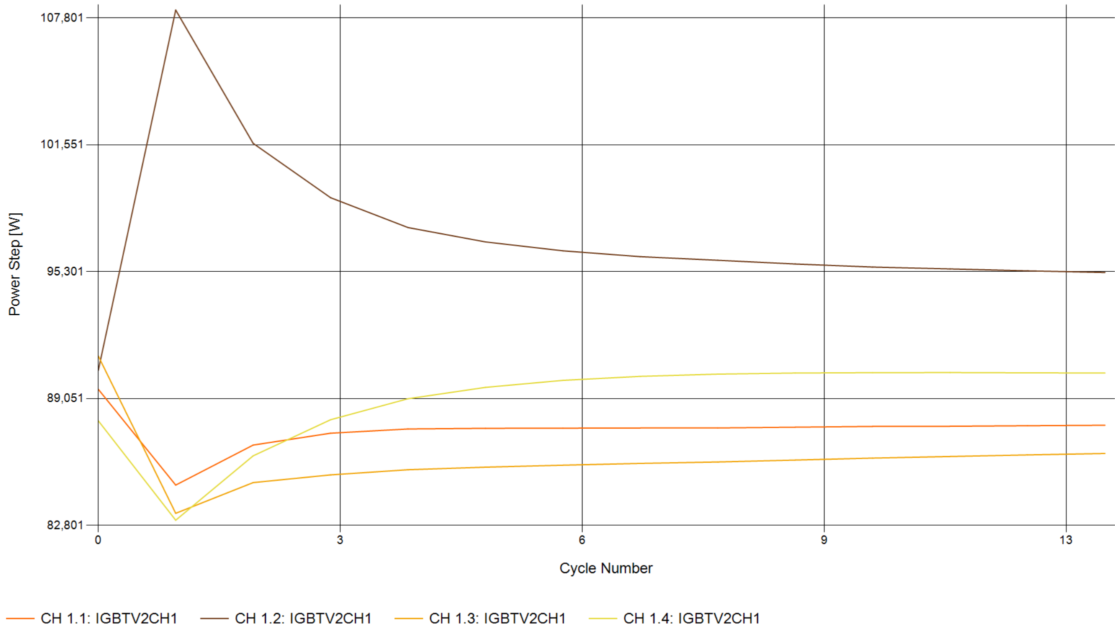


Figure D.7: The power losses during experiment B.

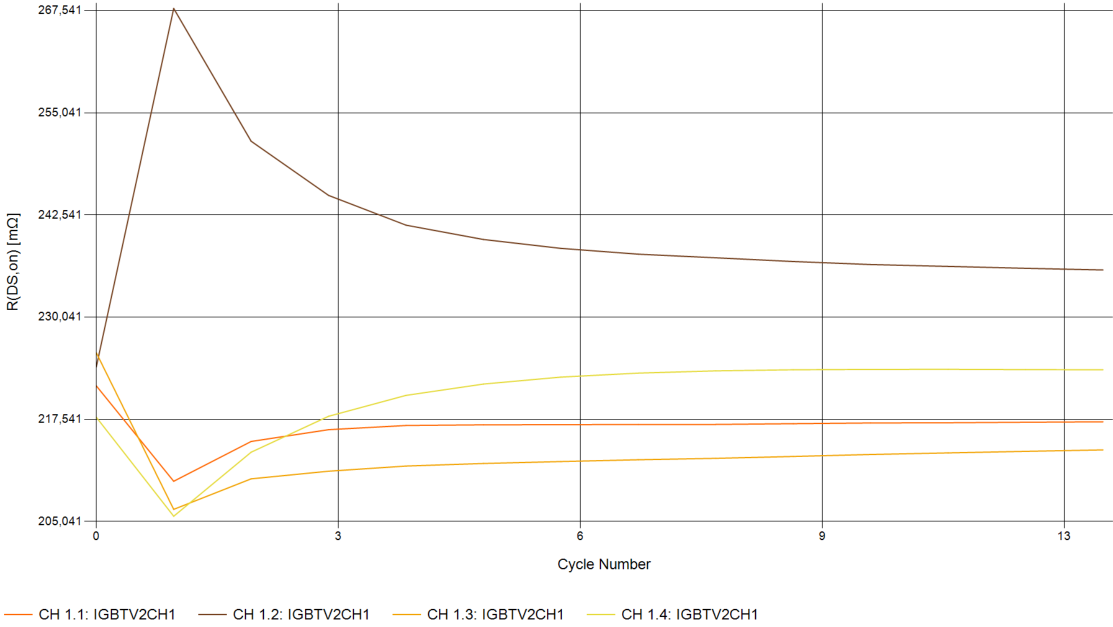


Figure D.8: The electric resistance during experiment B.

D.2. Experiment B: Thermal parameters

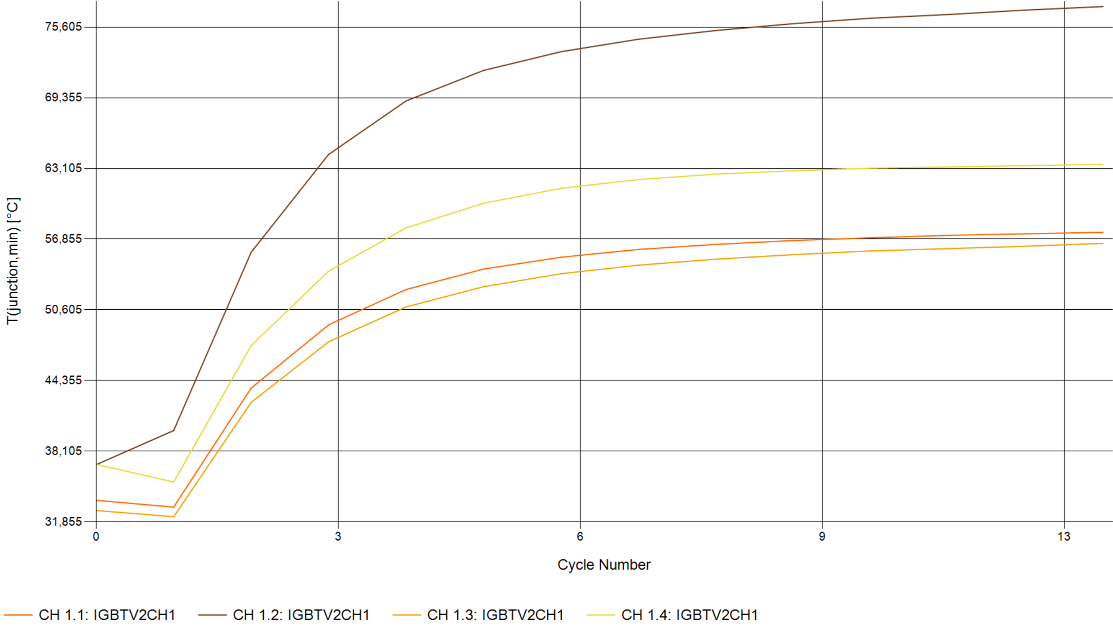


Figure D.9: The minimum junction temperature during experiment B.

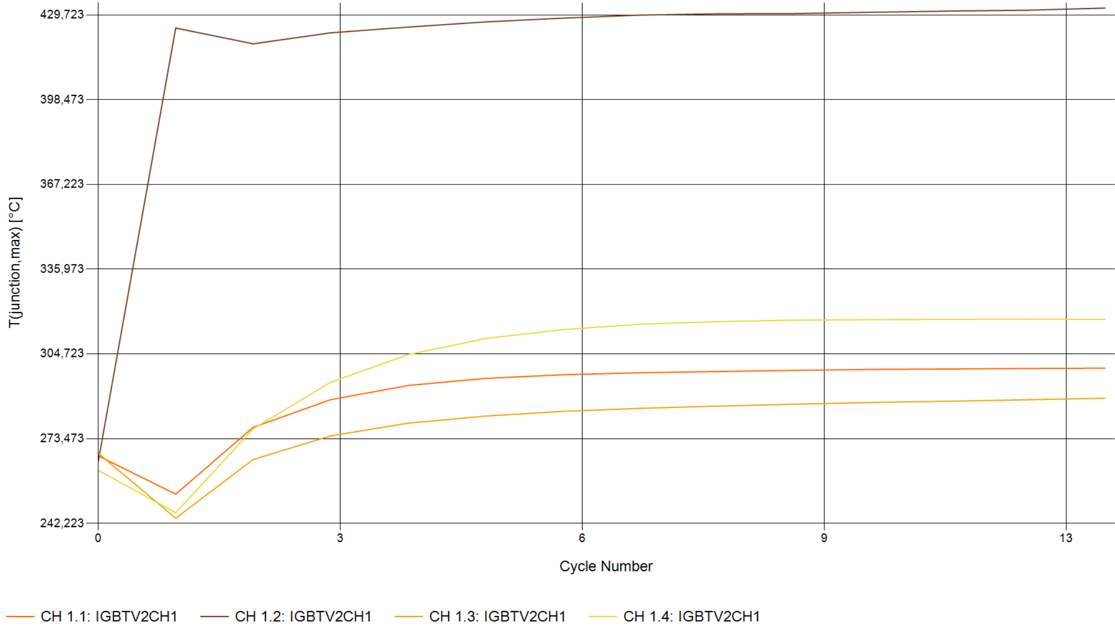


Figure D.10: The maximum junction temperature during experiment B.

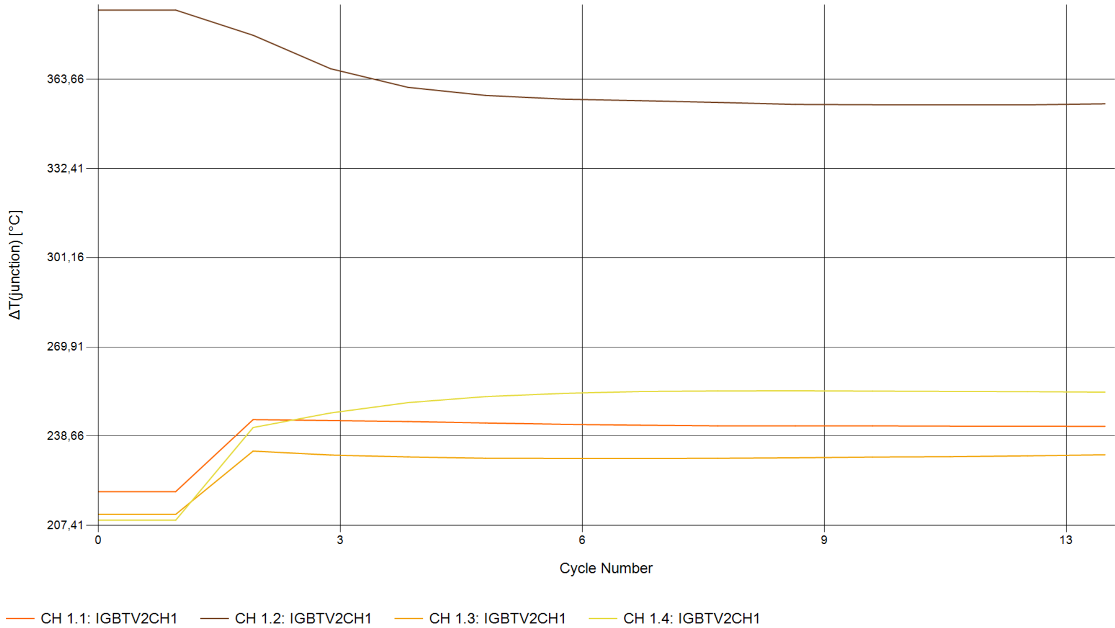


Figure D.11: The junction temperature deviation during experiment B.

E

Experiment C

This chapter contains the graphs for the power cycling test of experiment C.

E.1. Experiment C1: Parameters at the end of the experiment.

In this section, the current, voltage, and electric resistance are presented during the last cycles of experiment C1.

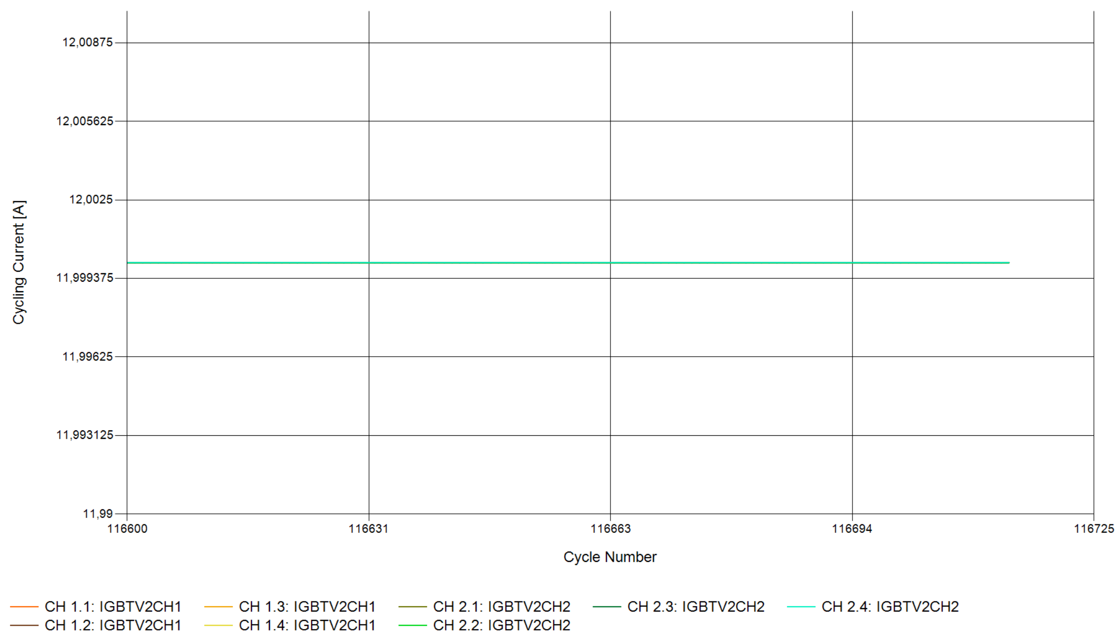


Figure E.1: The heating current at the last 100 cycles.

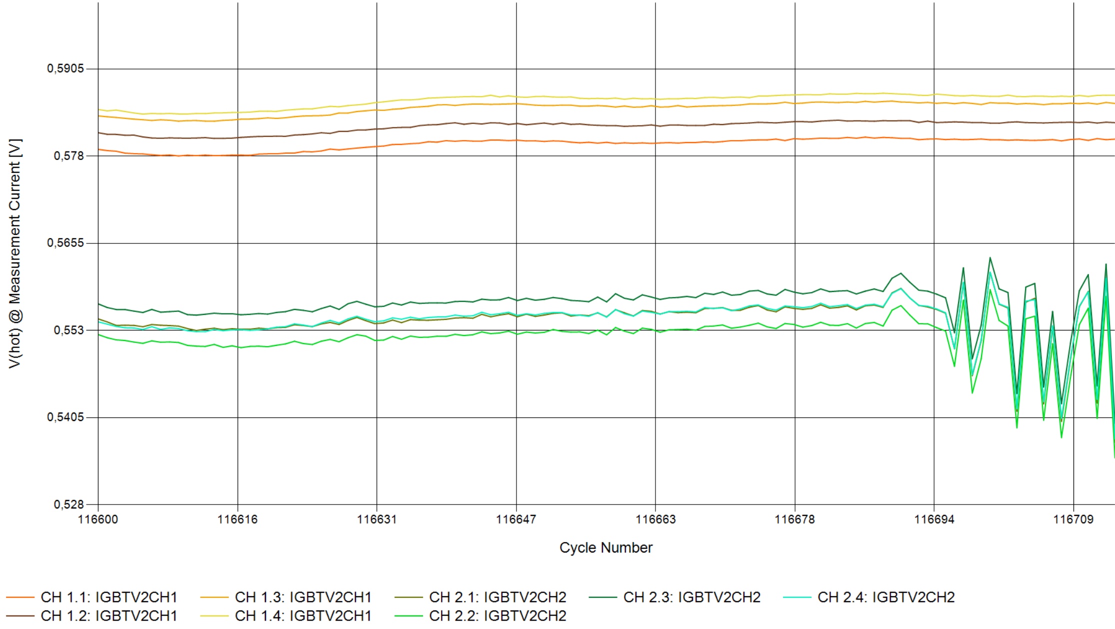


Figure E.2: The measured voltage to calculate the maximum junction temperature at the last 100 cycles.

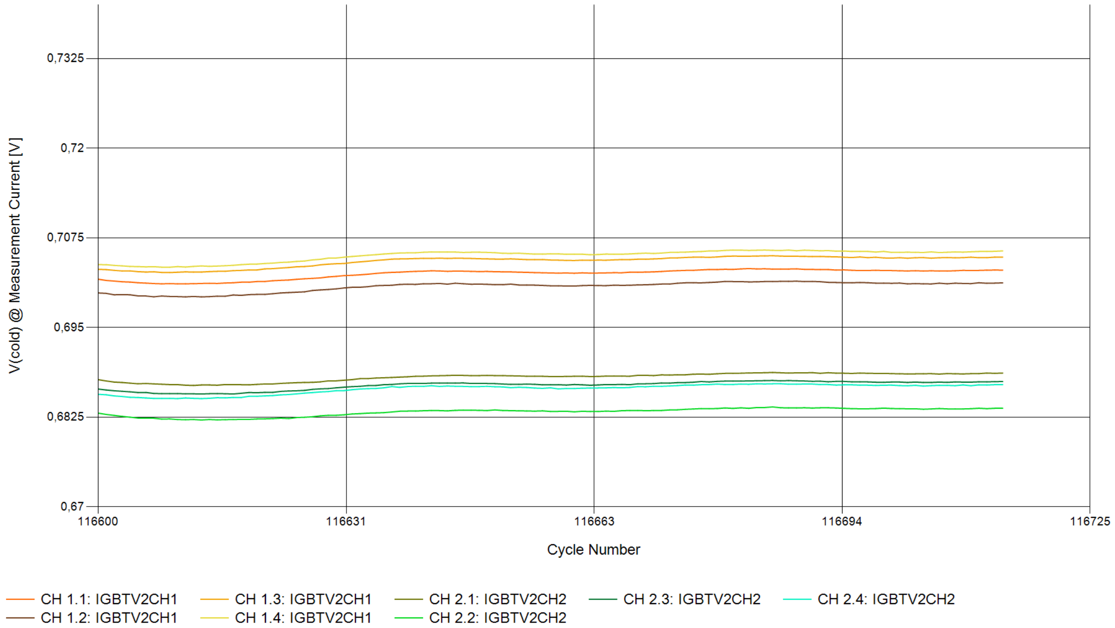


Figure E.3: The measured voltage to calculate the minimum junction temperature at the last 100 cycles.

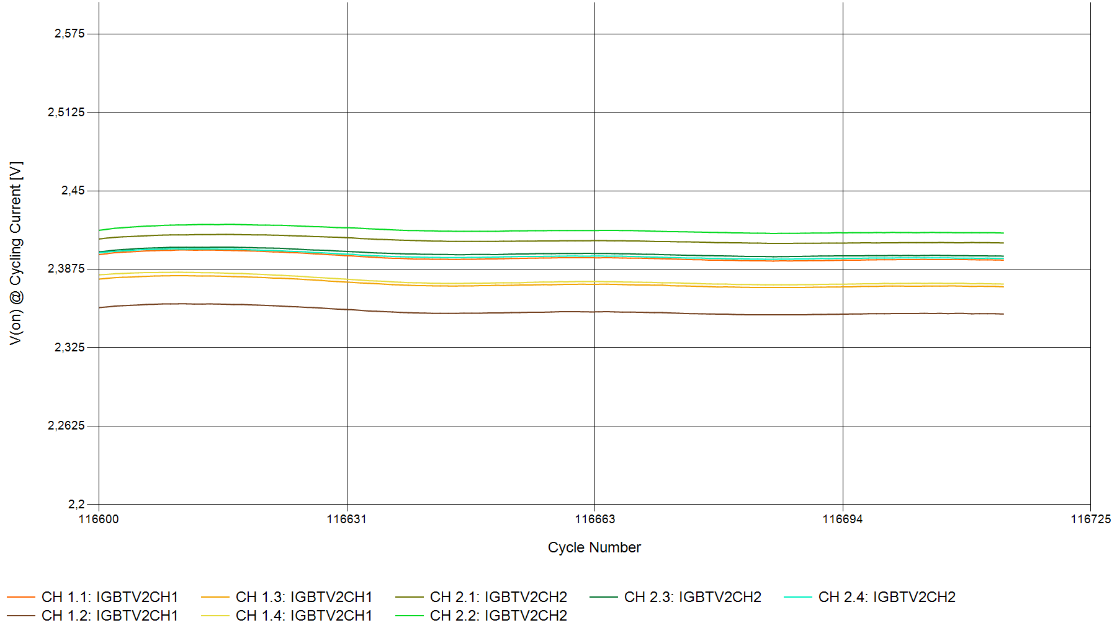


Figure E.4: The on-voltage during the last 100 cycles.

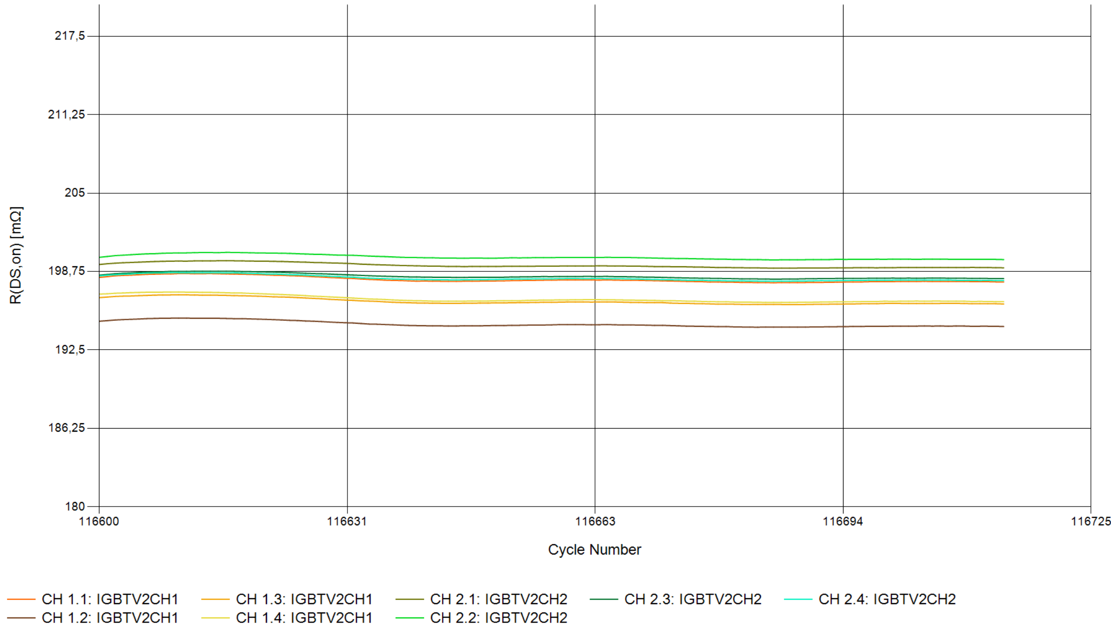


Figure E.5: The electric resistance during the last 100 cycles.

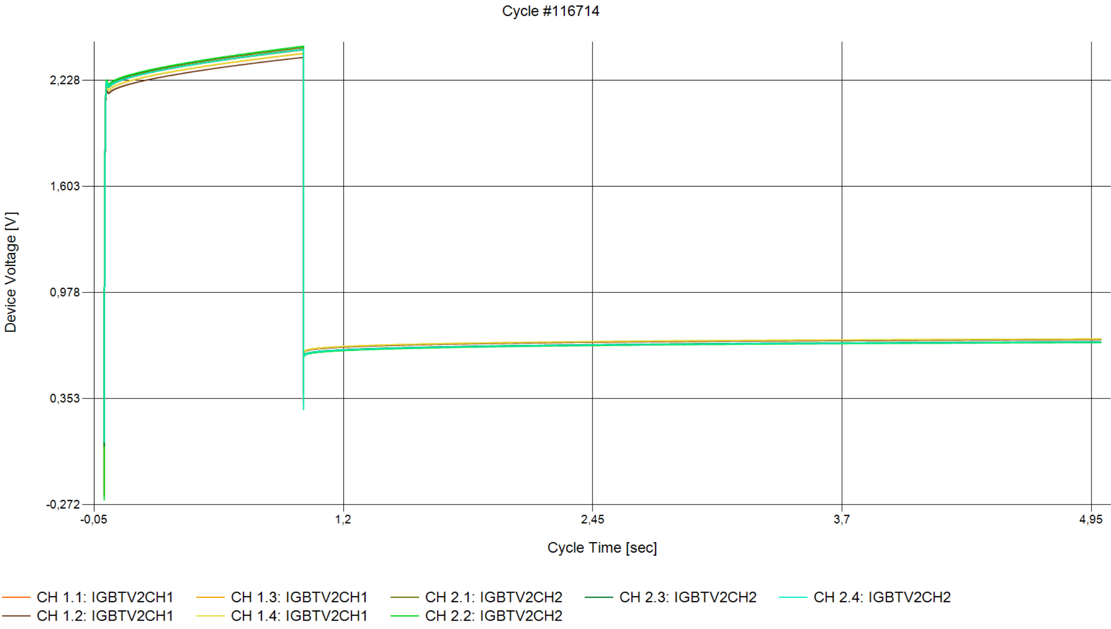


Figure E.6: The measured voltage during cycle 116714 of experiment C1.

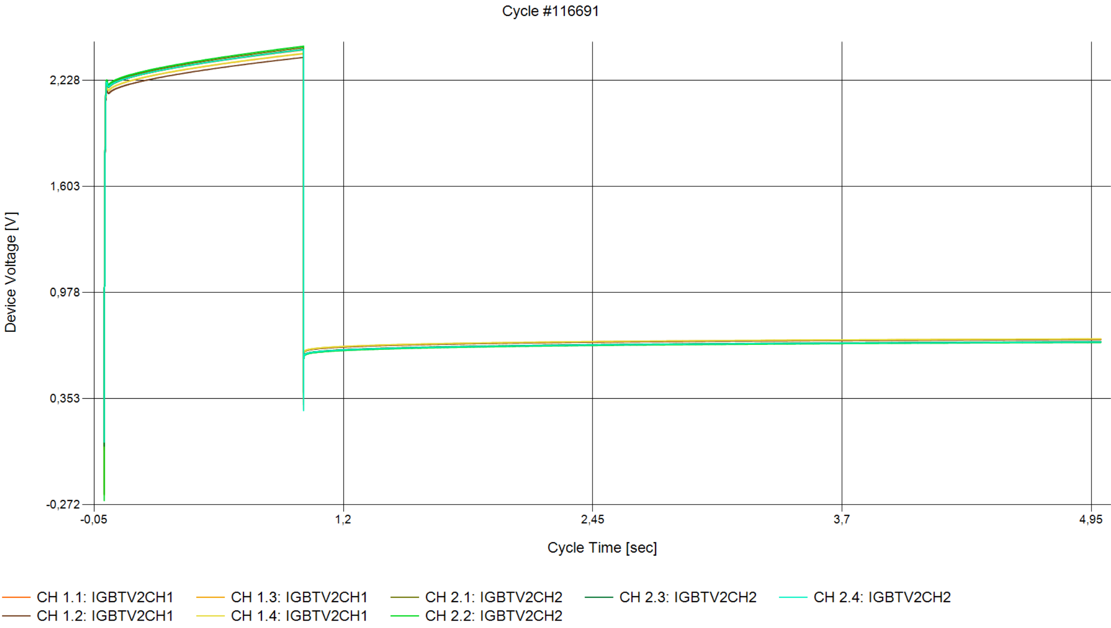


Figure E.7: The measured voltage during cycle 116691 of experiment C1.

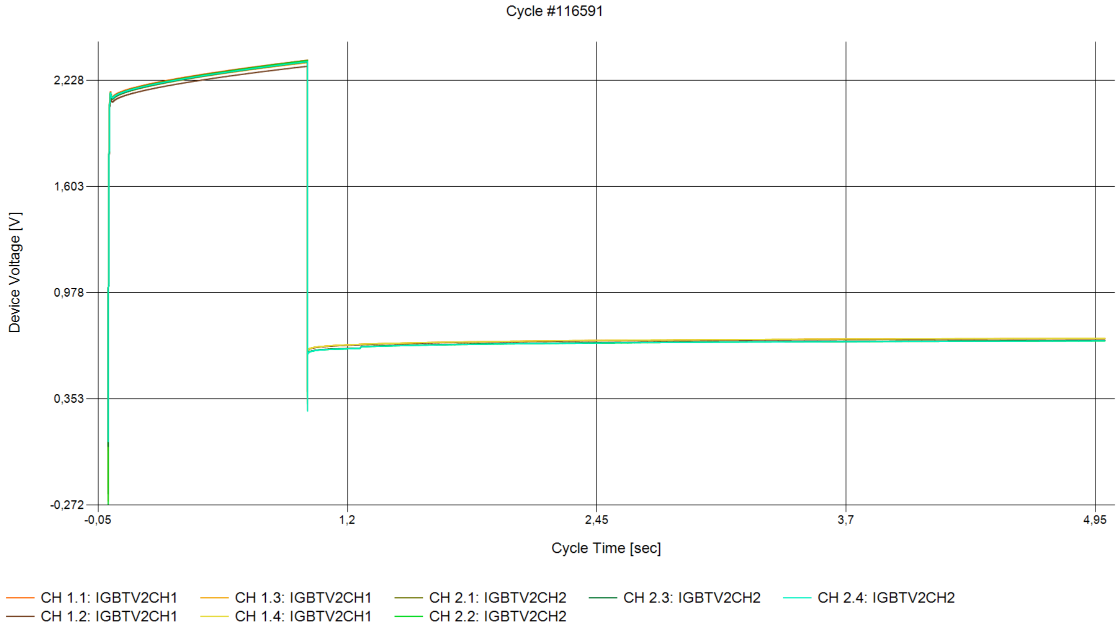


Figure E.8: The measured voltage during cycle 116591 of experiment C1.

E.2. Experiment C1: cumulative structure function and degradation.

In the following figures, the cumulative structure functions of the eight positions are given and the degradation plots at different C_{th} are found.

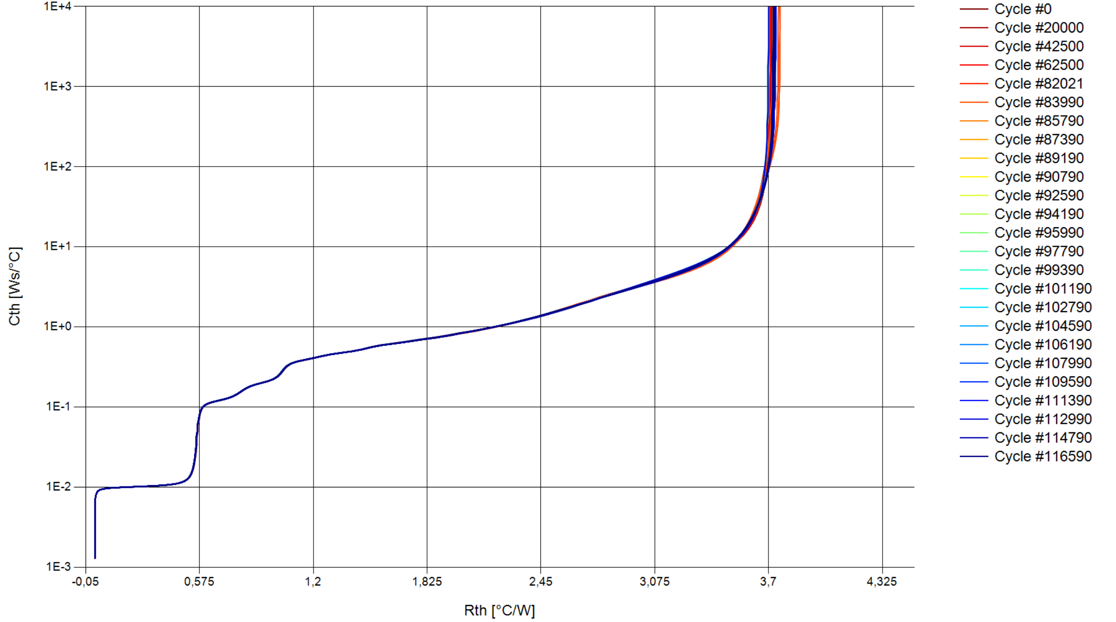


Figure E.9: The cumulative structure function of position 1.1 of experiment C1.

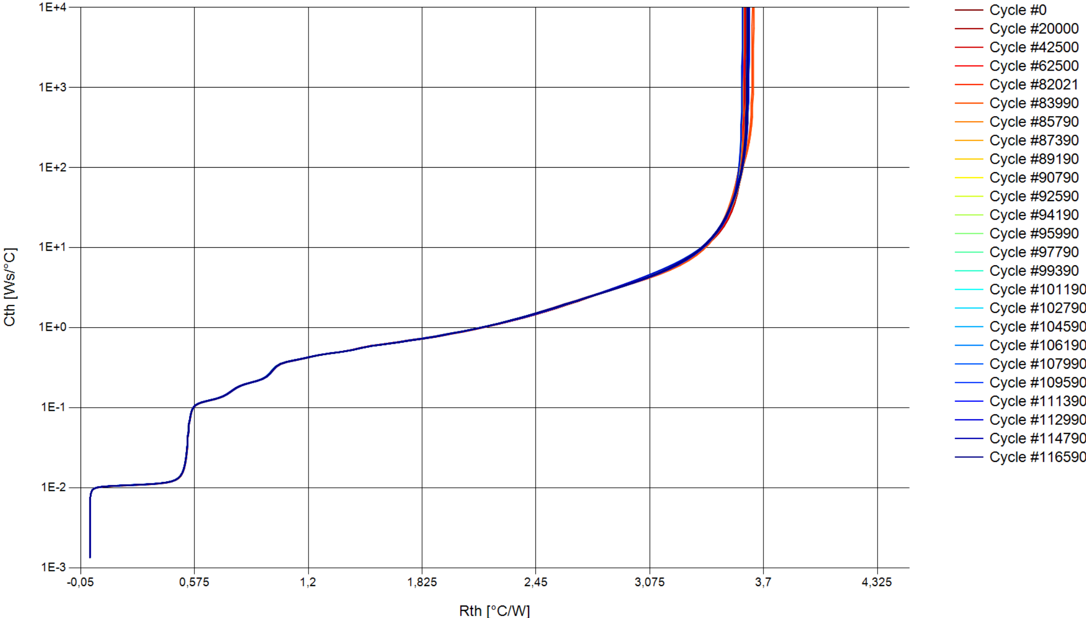


Figure E.10: The cumulative structure function of position 1.2 of experiment C1.

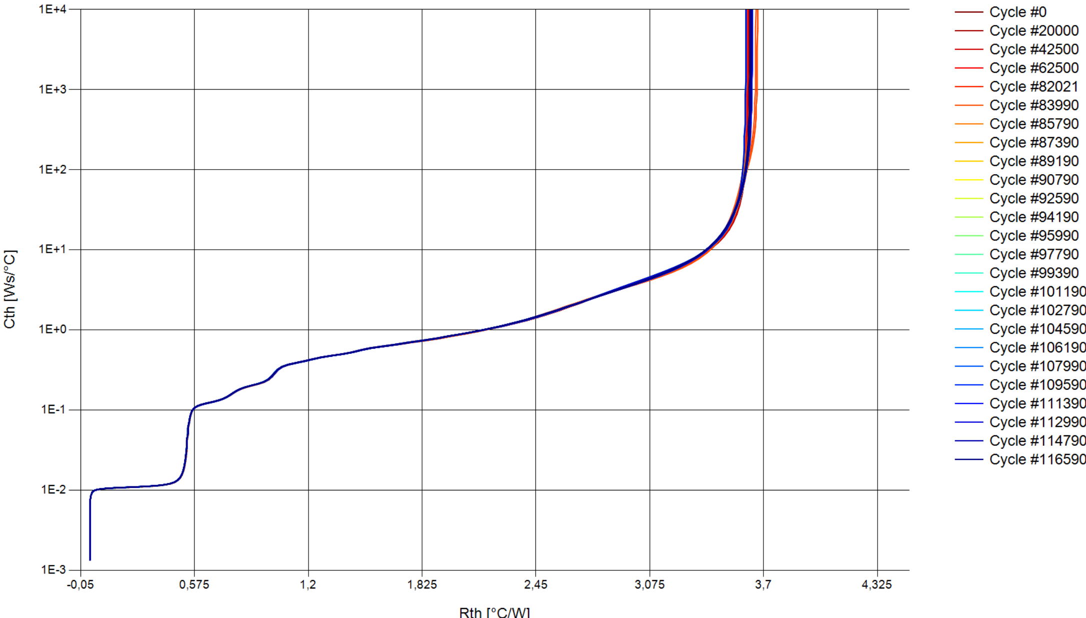


Figure E.11: The cumulative structure function of position 1.3 of experiment C1.

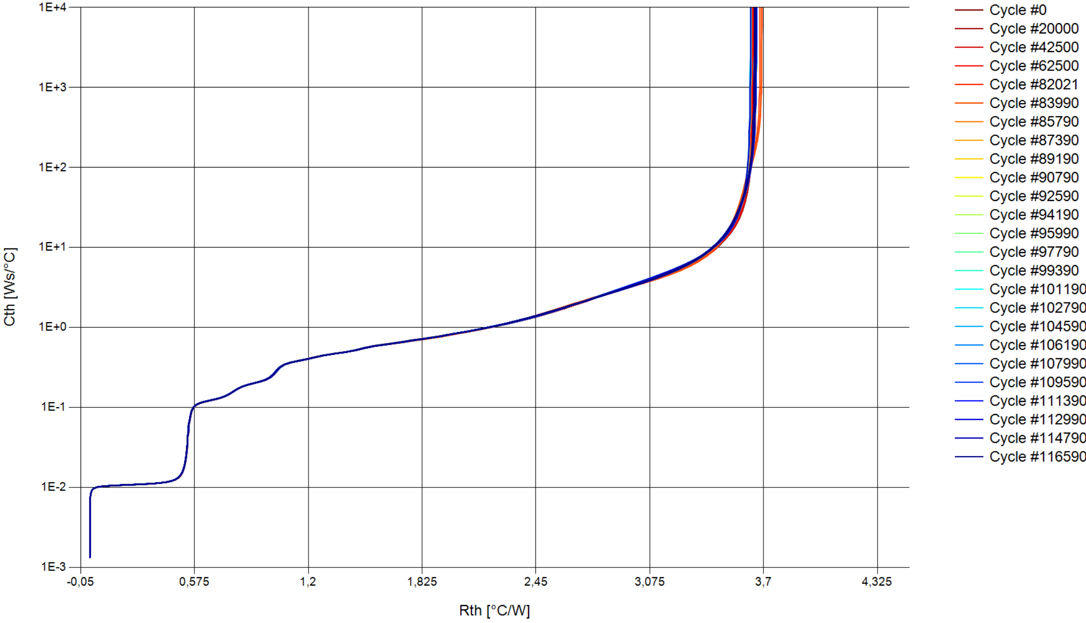


Figure E.12: The cumulative structure function of position 1.4 of experiment C1.

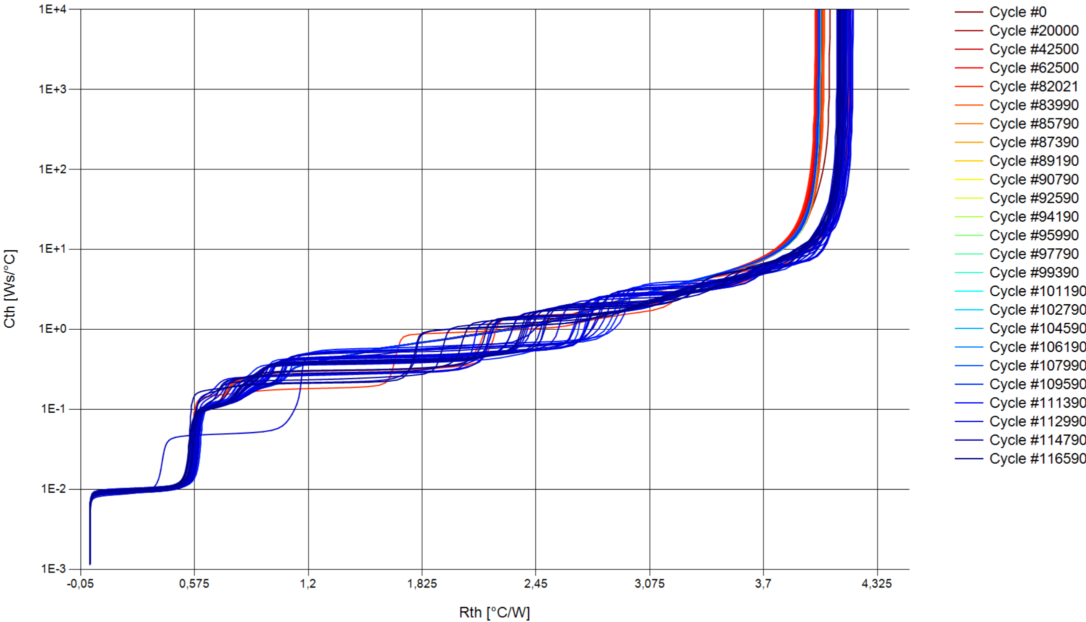


Figure E.13: The cumulative structure function of position 2.1 of experiment C1.

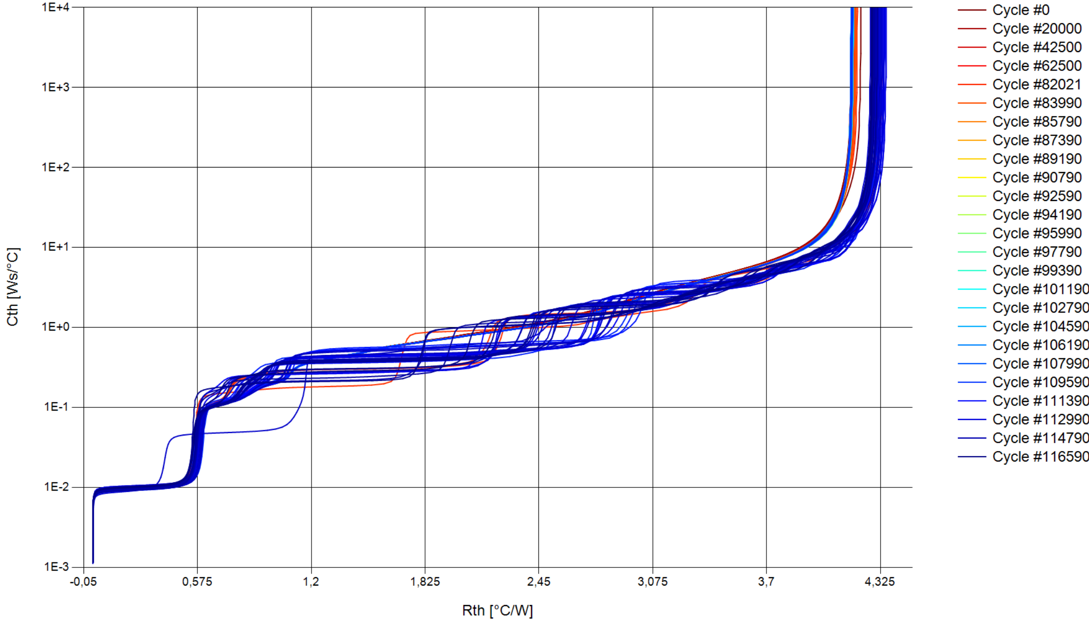


Figure E.14: The cumulative structure function of position 2.2 of experiment C1.

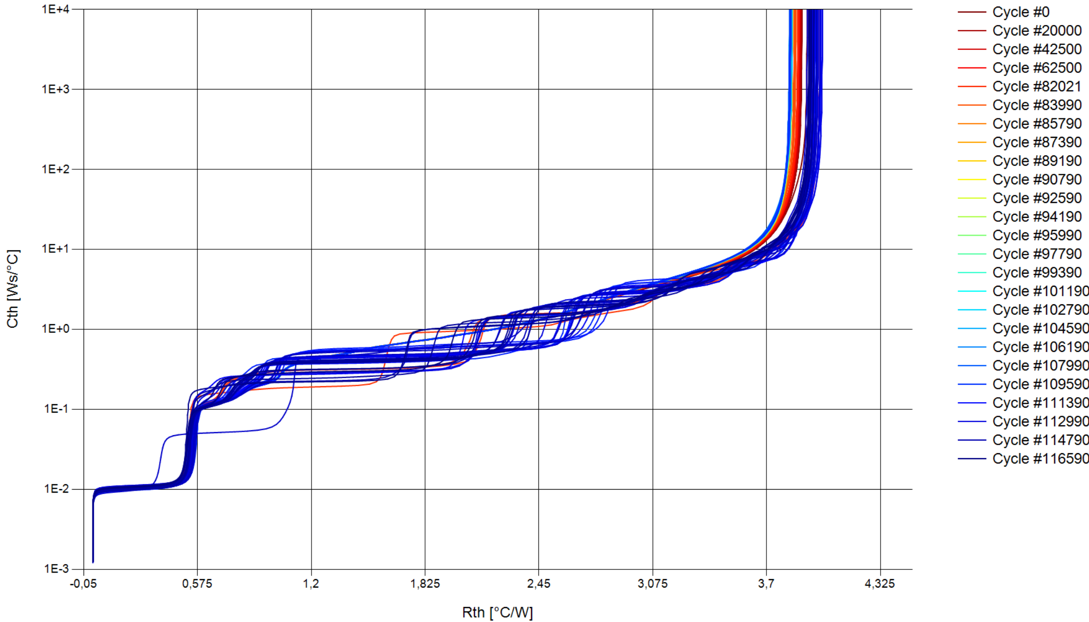


Figure E.15: The cumulative structure function of position 2.3 of experiment C1.

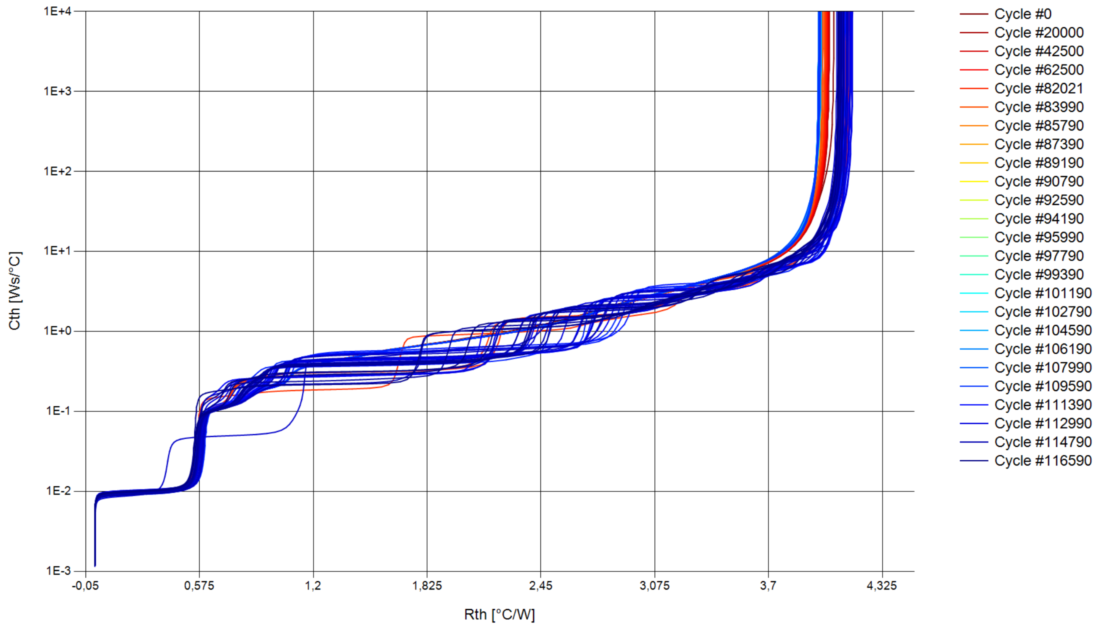


Figure E.16: The cumulative structure function of position 2.4 of experiment C1.

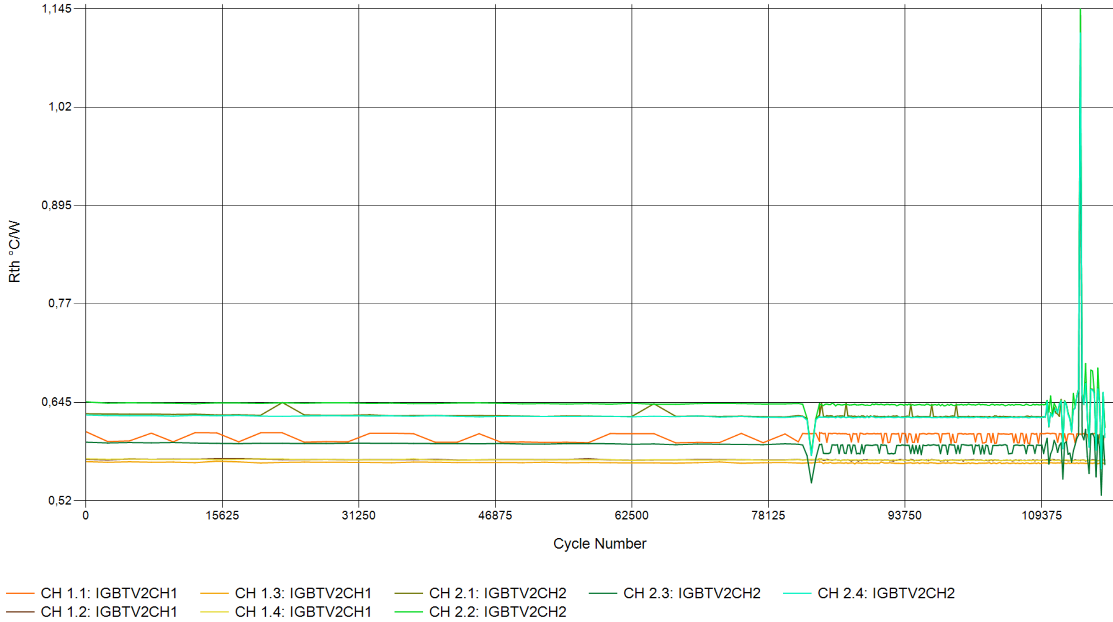


Figure E.17: The thermal resistance value at $C_{\text{th}} = 0.1$ Ws/°C during experiment C1.

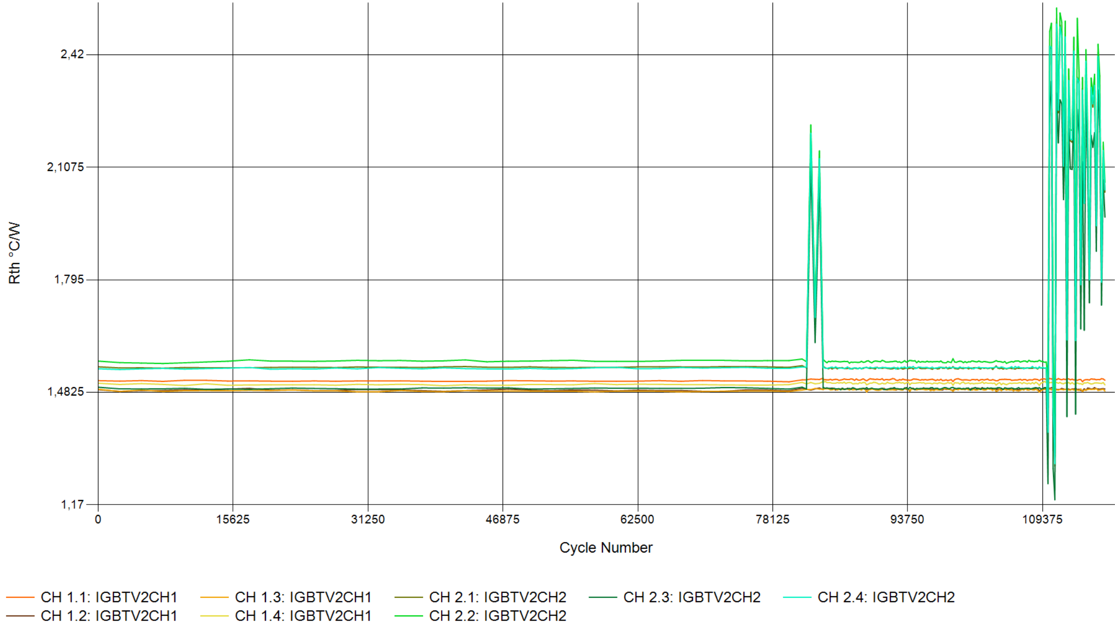


Figure E.18: The thermal resistance value at $C_{\text{th}} = 0.5$ Ws/°C during experiment C1.

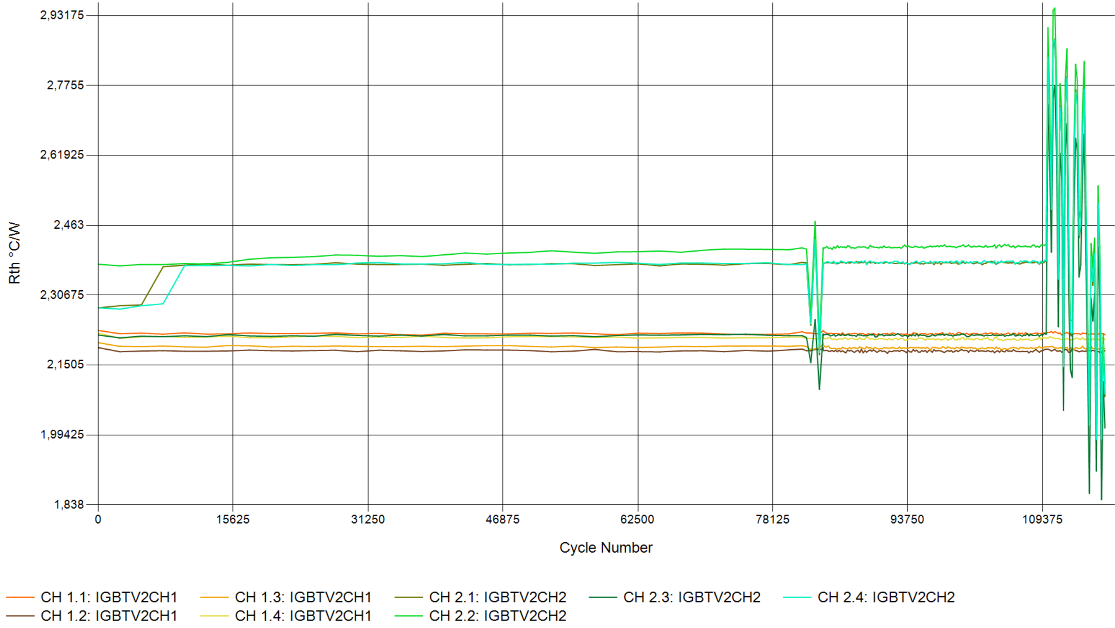


Figure E.19: The thermal resistance value at $C_{\text{th}} = 1$ Ws/°C during experiment C1.

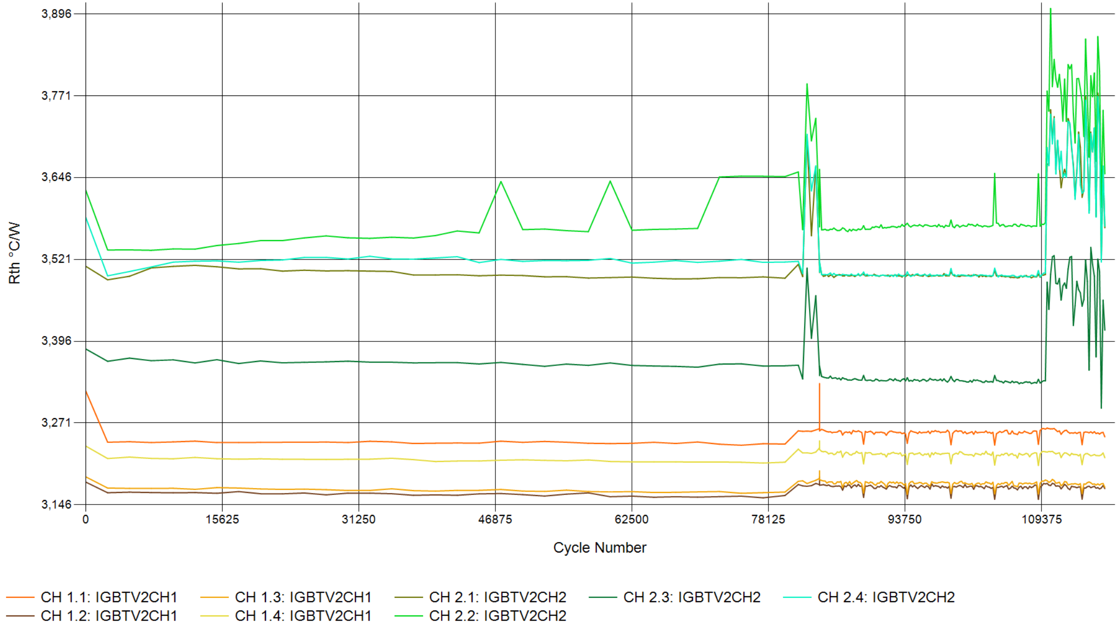


Figure E.20: The thermal resistance value at $C_{\text{th}} = 5$ Ws/°C during experiment C1.

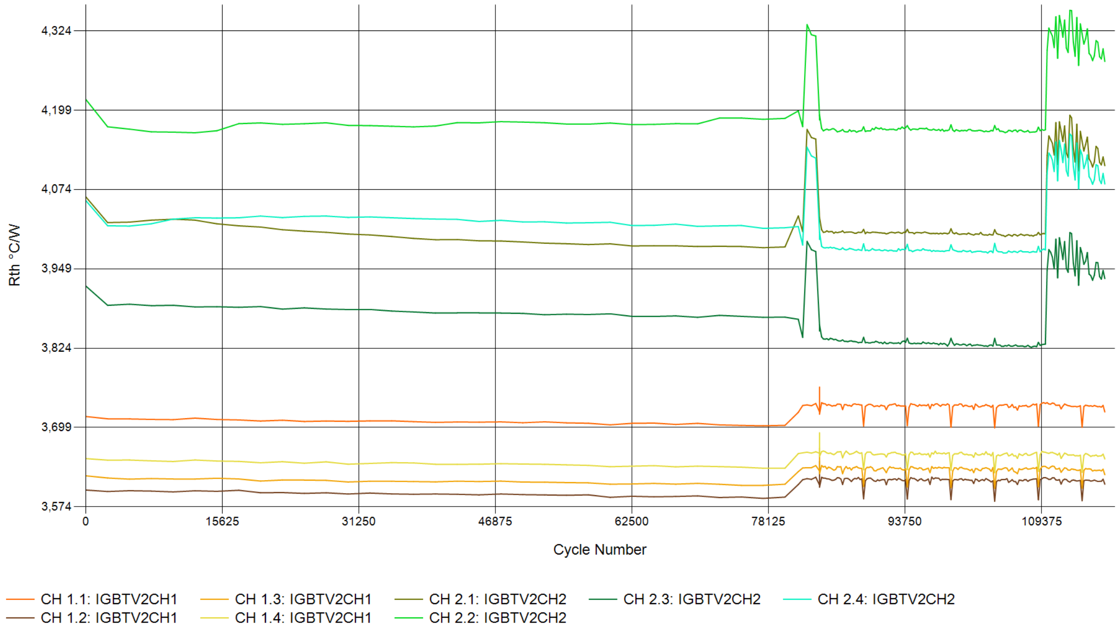


Figure E.21: The thermal resistance value at $C_{\text{th}} = 1000$ Ws/°C during experiment C1.

E.3. Experiment C2: The procession of the voltage

In the following figures, the measured voltage for multiple cycles during the power cycling of experiment C2 are given.

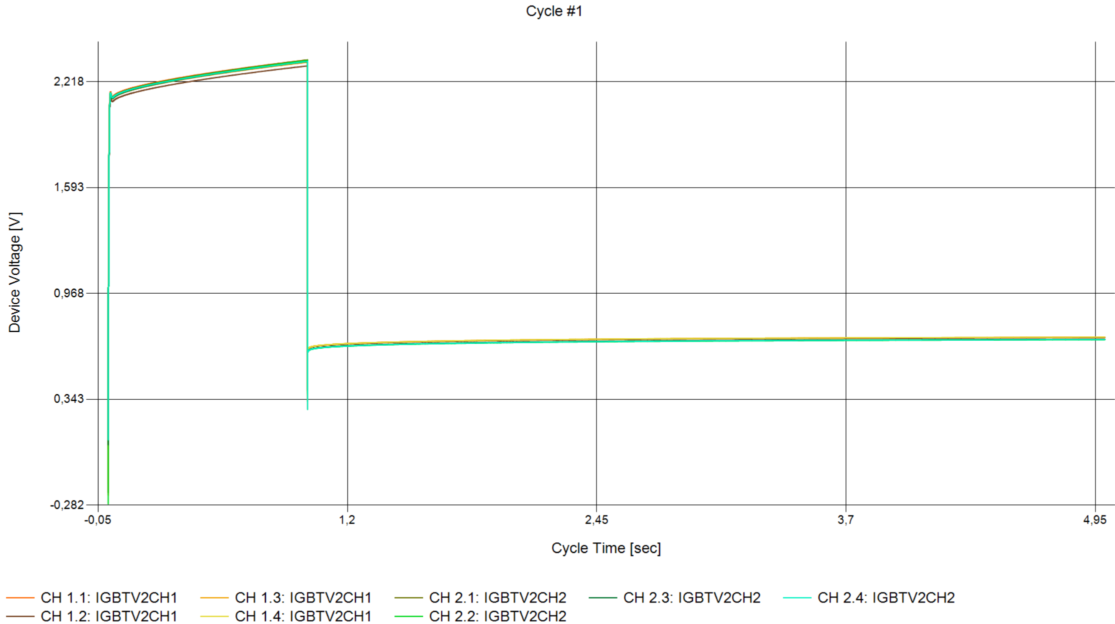


Figure E.22: The measured voltage during cycle 1 of the power cycling experiment C2.

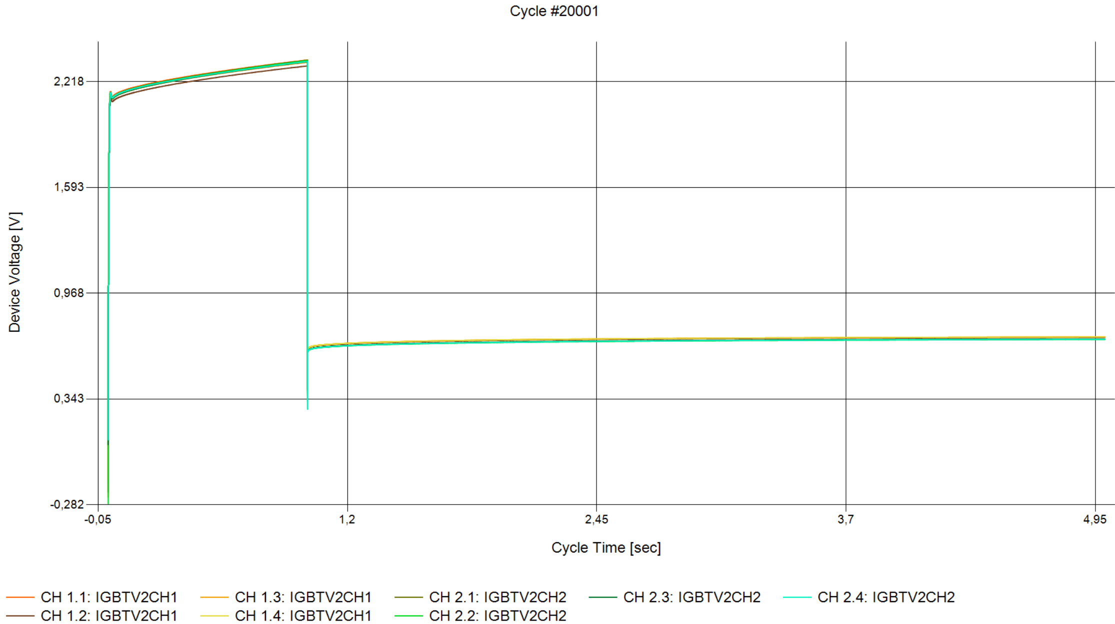


Figure E.23: The measured voltage during cycle 20001 of the power cycling experiment C2.

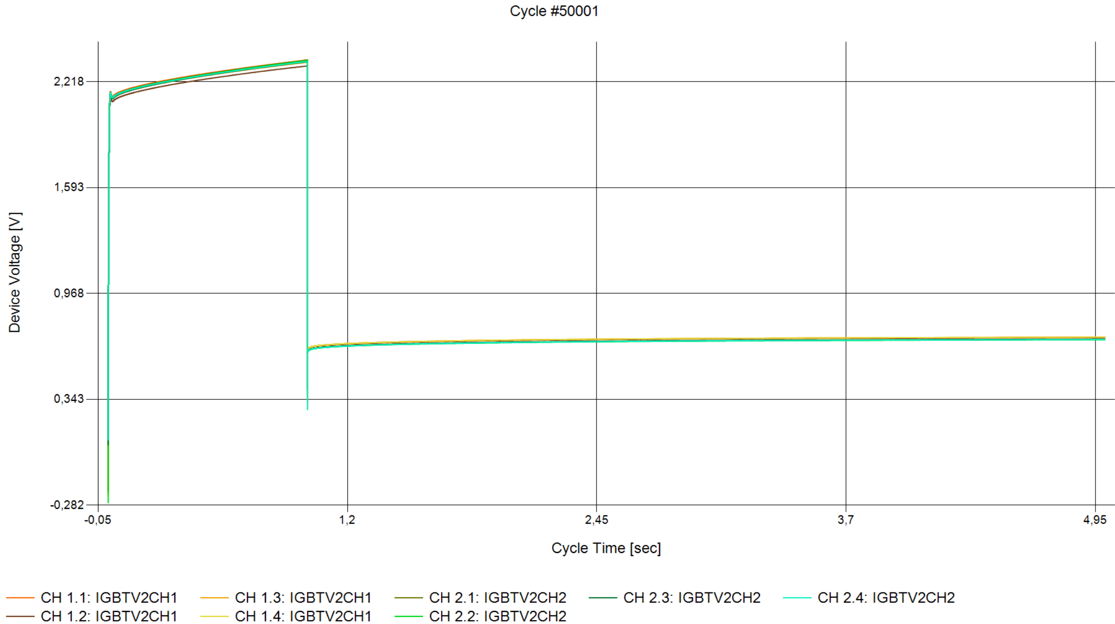


Figure E.24: The measured voltage during cycle 50001 of the power cycling experiment C2.

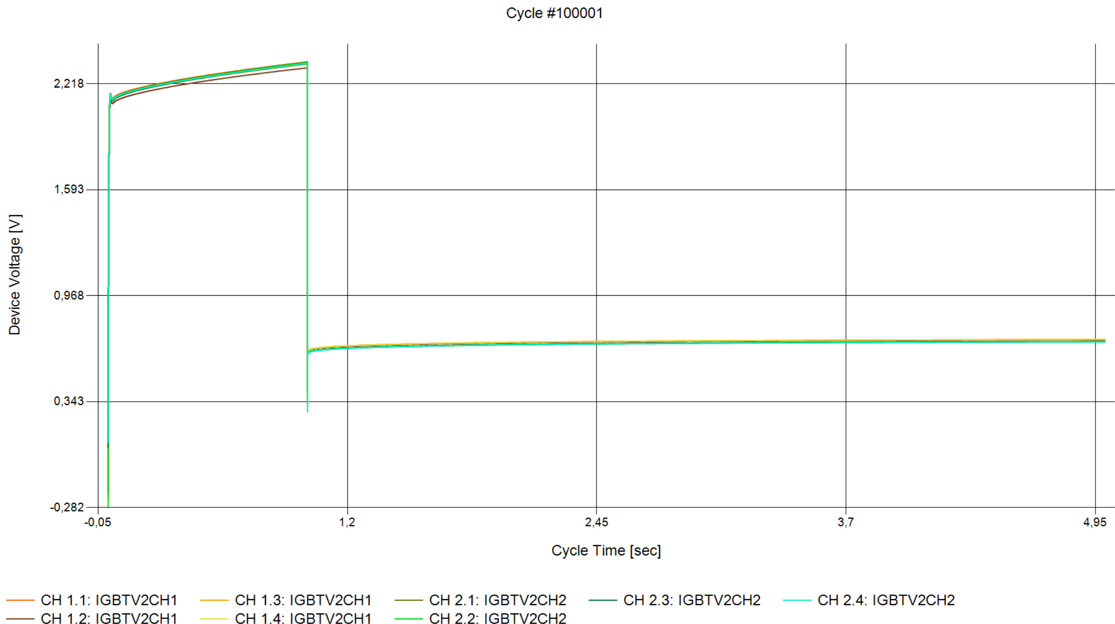


Figure E.25: The measured voltage during cycle 100001 of the power cycling experiment C2.

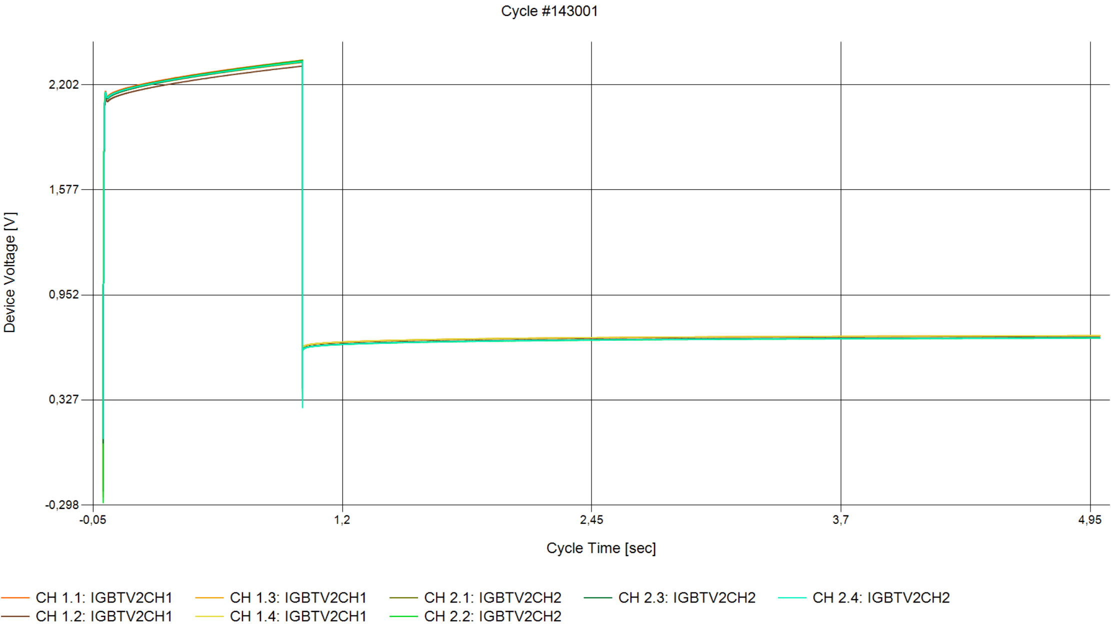


Figure E.26: The measured voltage during cycle 143001 of the power cycling experiment C2.

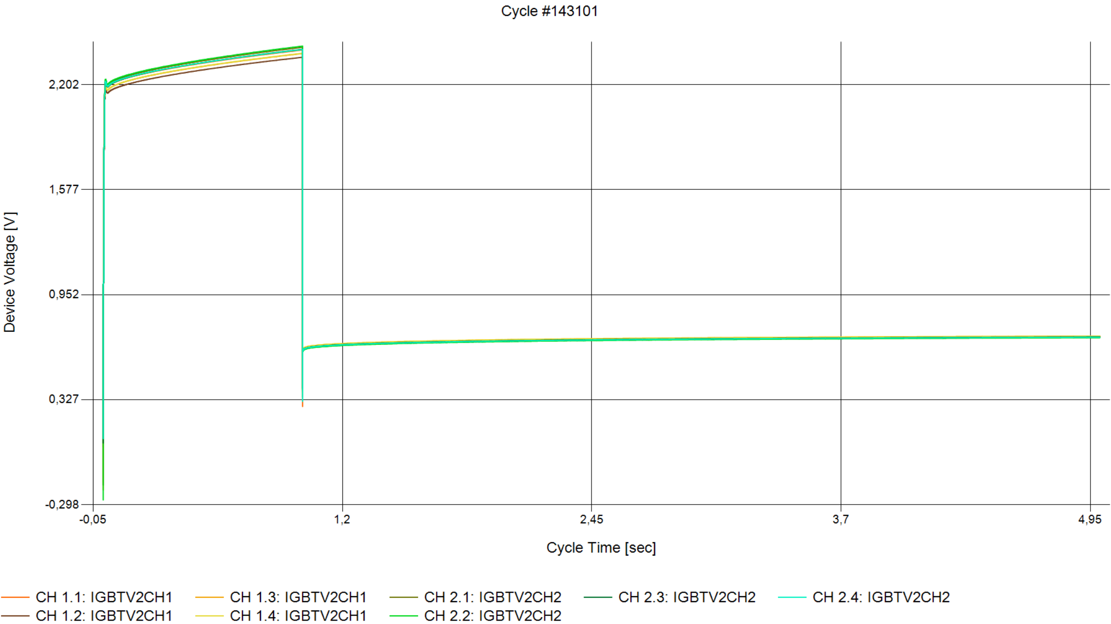


Figure E.27: The measured voltage during cycle 143101 of the power cycling experiment C2.

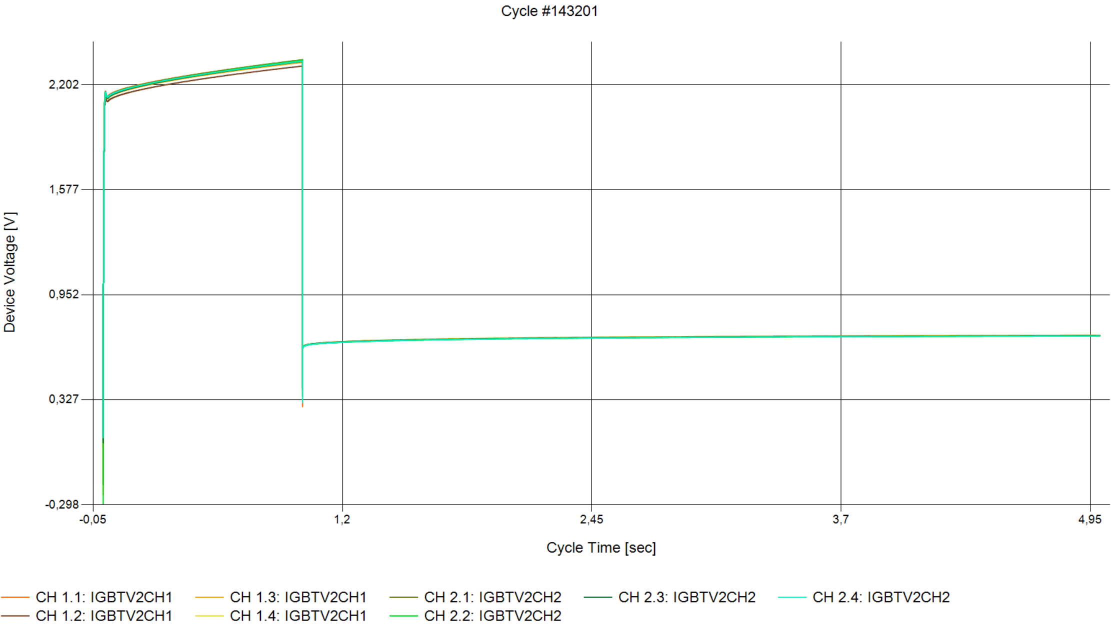


Figure E.28: The measured voltage during cycle 143201 of the power cycling experiment C2.

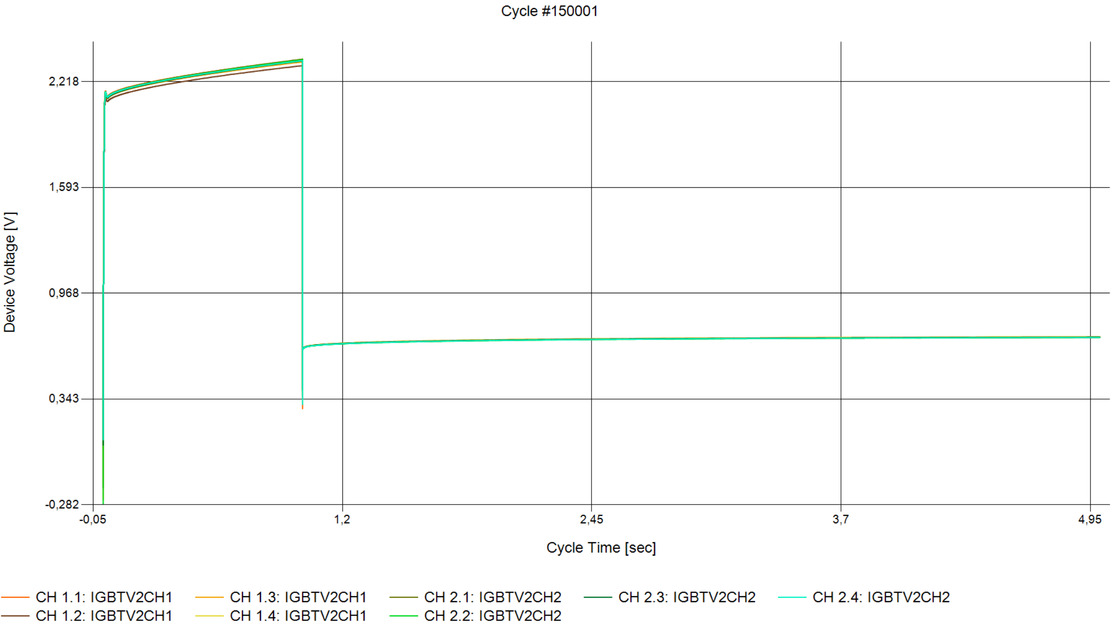


Figure E.29: The measured voltage during cycle 150001 of the power cycling experiment C2.

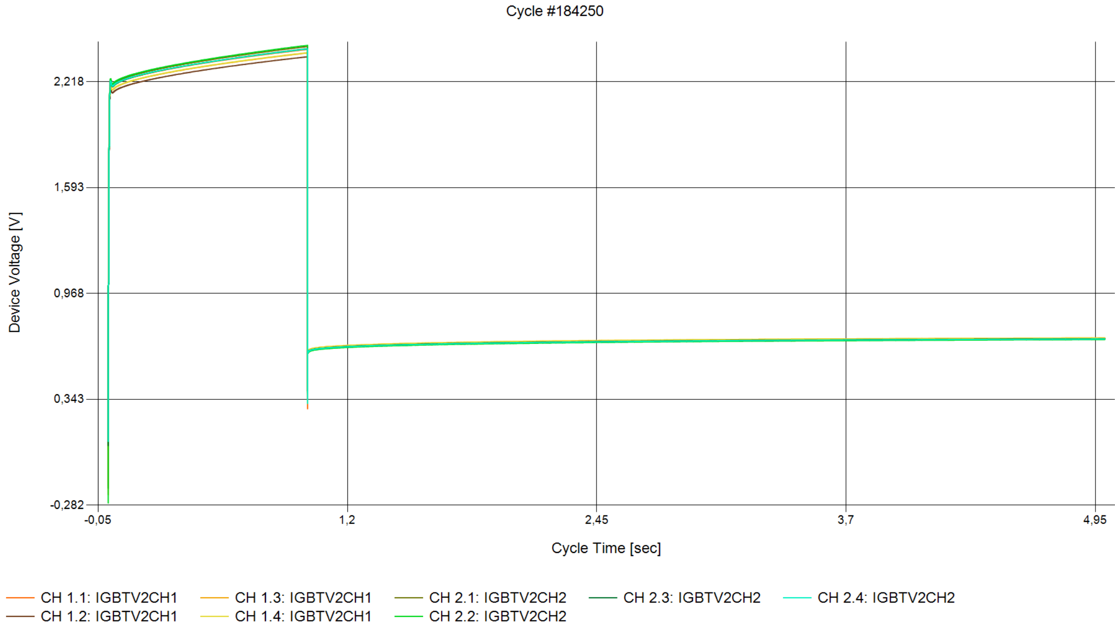


Figure E.30: The measured voltage during cycle 184250 of the power cycling experiment C2.

E.4. Experiment C2: ΔT_j, I, R_{CE}, V_{on}

This section contains the junction temperature deviation, heating current, electric resistance, and on-voltage of the power cycling test of experiment C2.

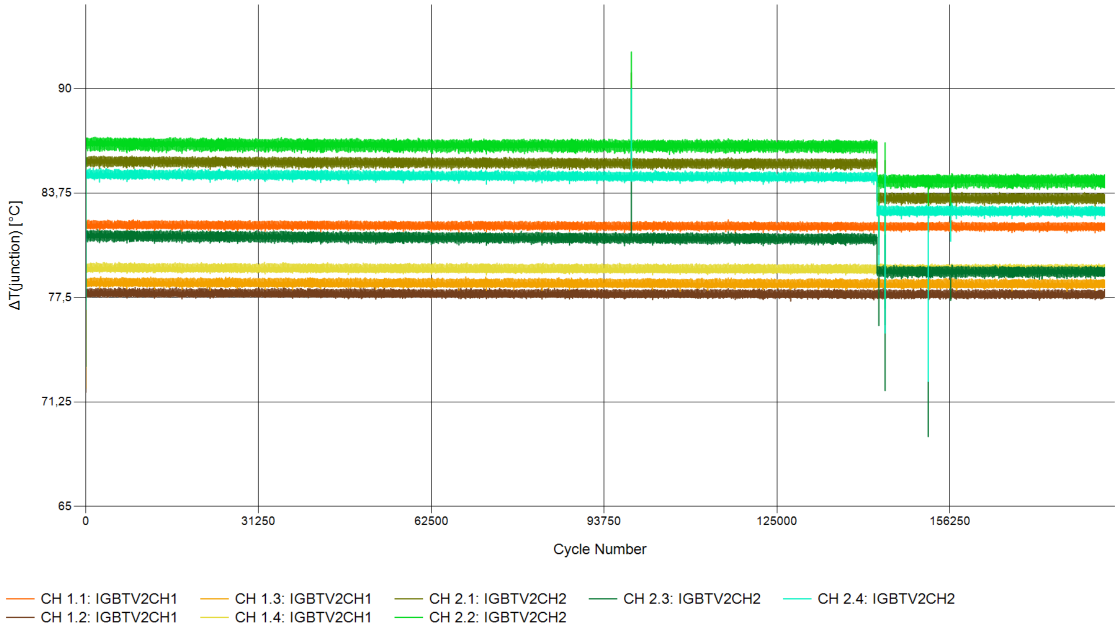


Figure E.31: The junction temperature deviation during the power cycling experiment C2.

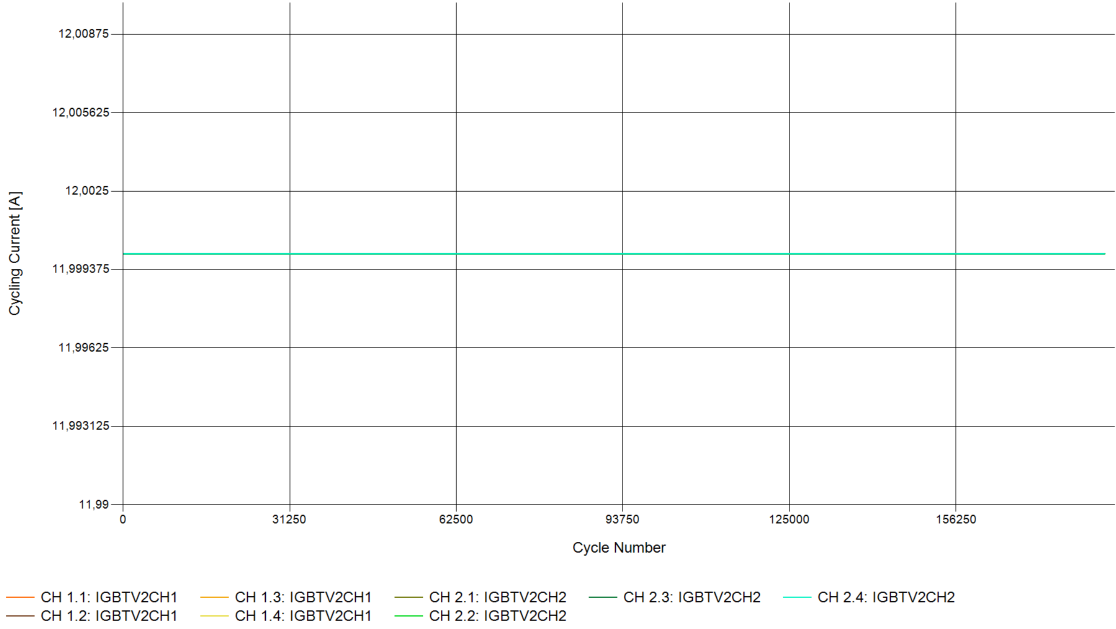


Figure E.32: The heating current during the power cycling experiment C2.

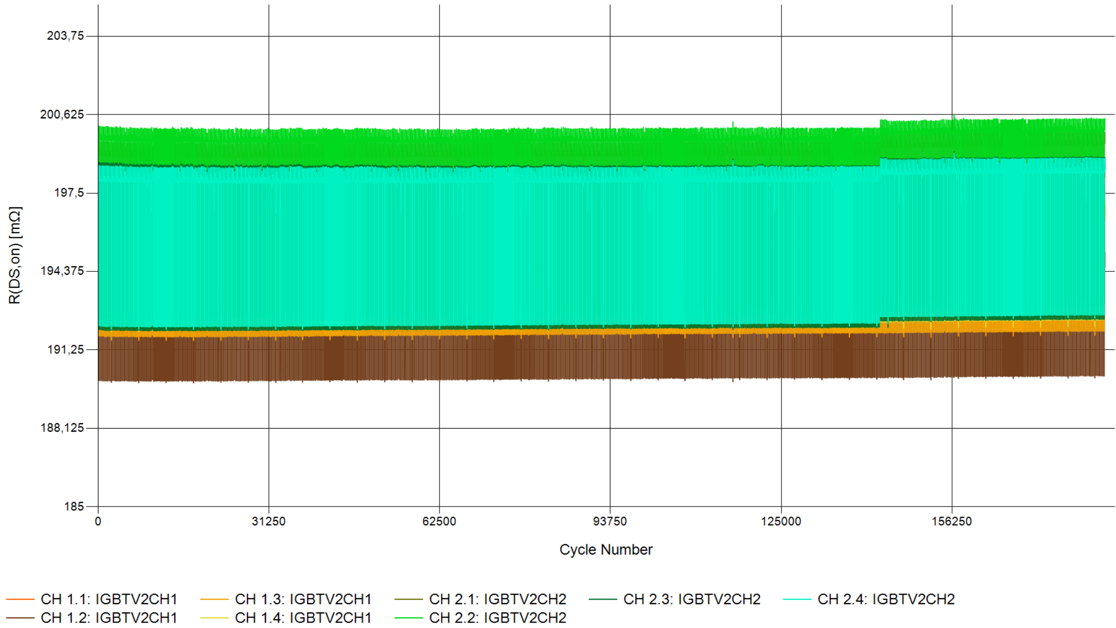


Figure E.33: The electrical resistance between the collector and emitter during the power cycling experiment C2.

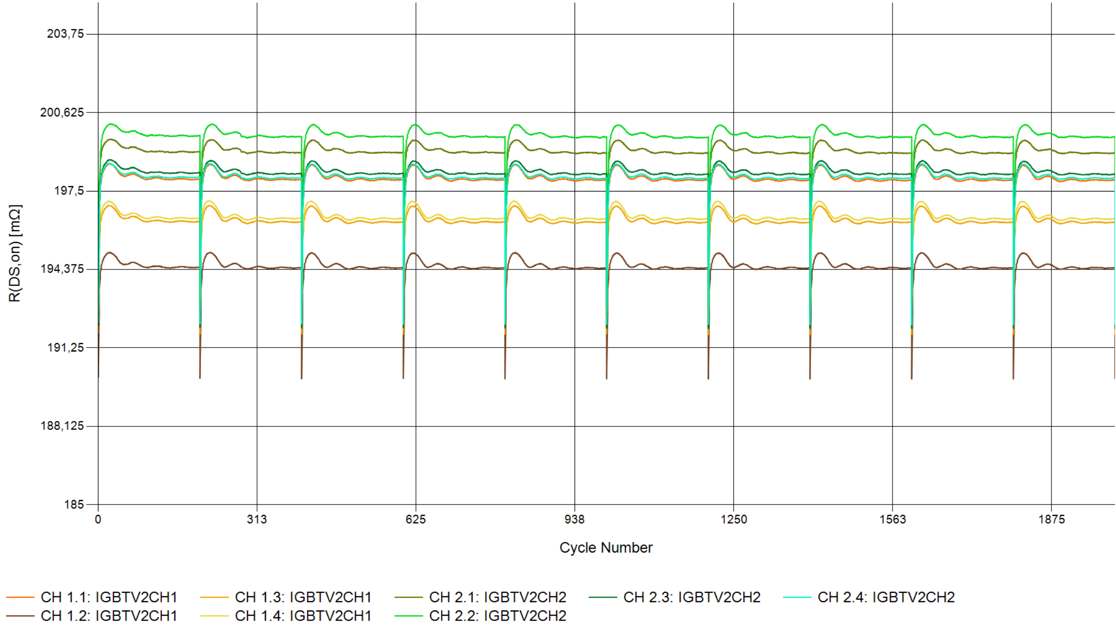


Figure E.34: The electrical resistance between the collector and emitter during the first 2000 cycles of experiment C2.

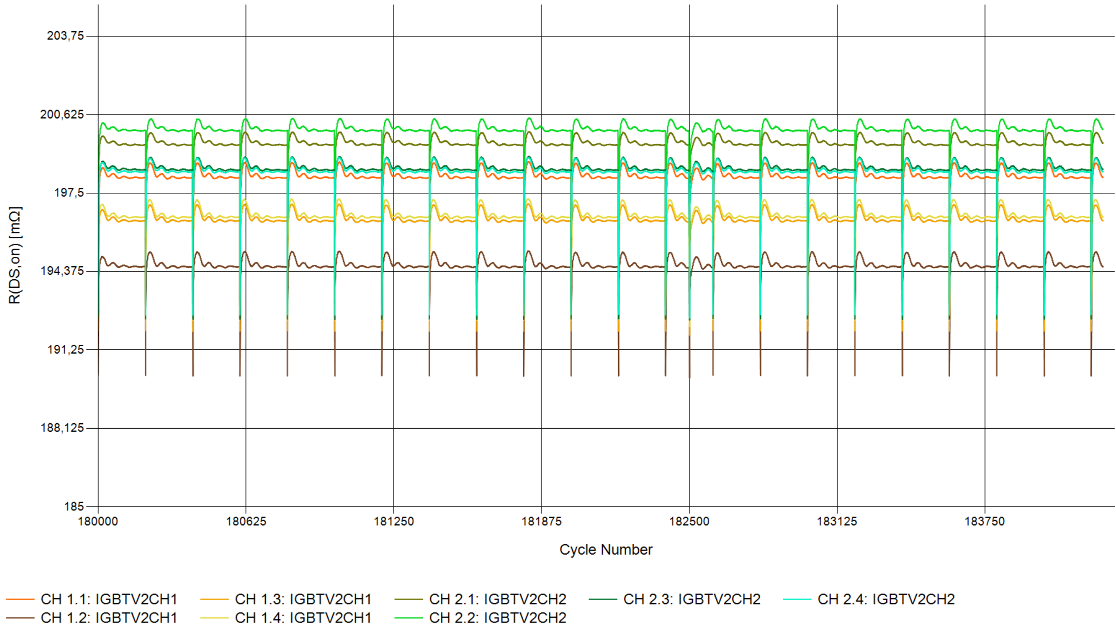


Figure E.35: The electrical resistance between the collector and emitter during the last 4000 cycles of experiment C2.

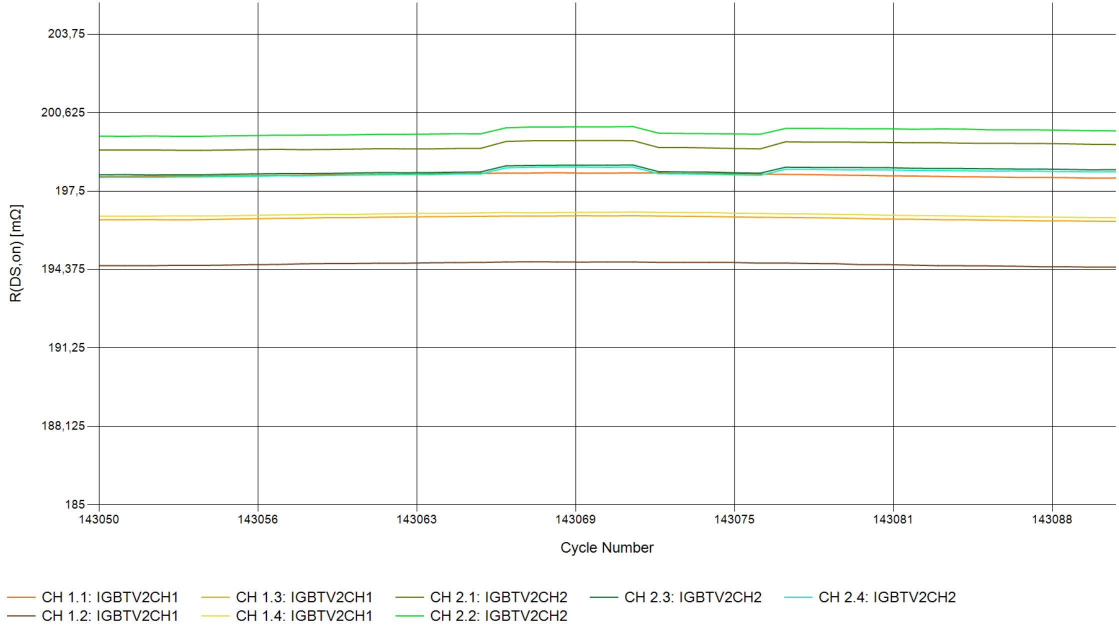


Figure E.36: The electrical resistance between the collector and emitter around the junction temperature jump of cycle 143070 of experiment C2.

E.5. Experiment C2: degradation plots

In the following figures, the degradation plots at different C_{th} are found.

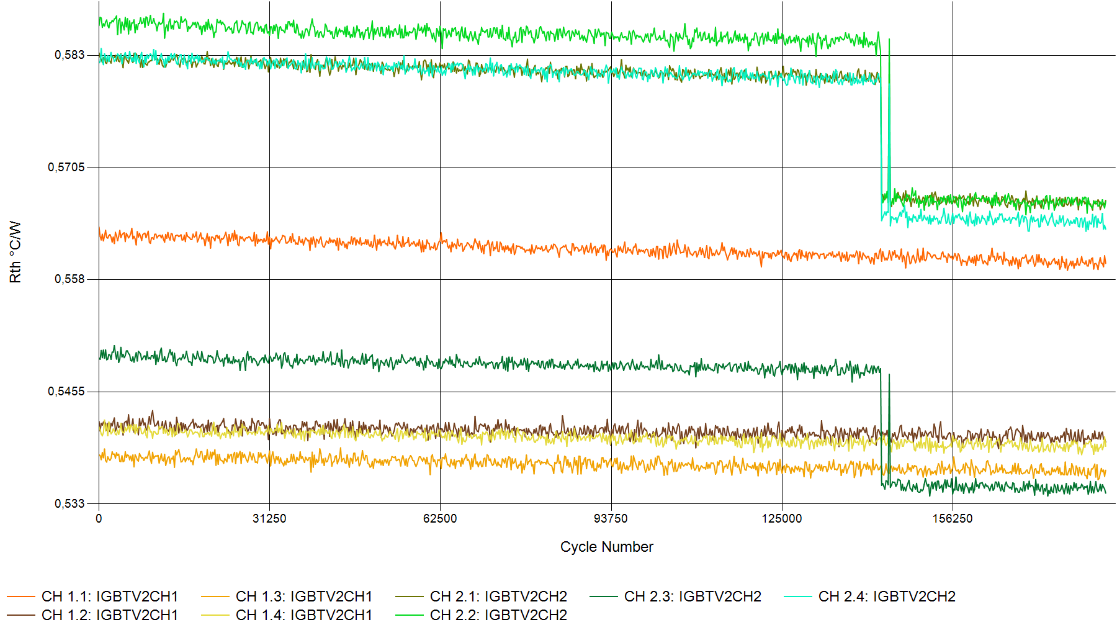


Figure E.37: The thermal resistance value at $C_{\text{th}} = 0.05$ °C/W during experiment C2.

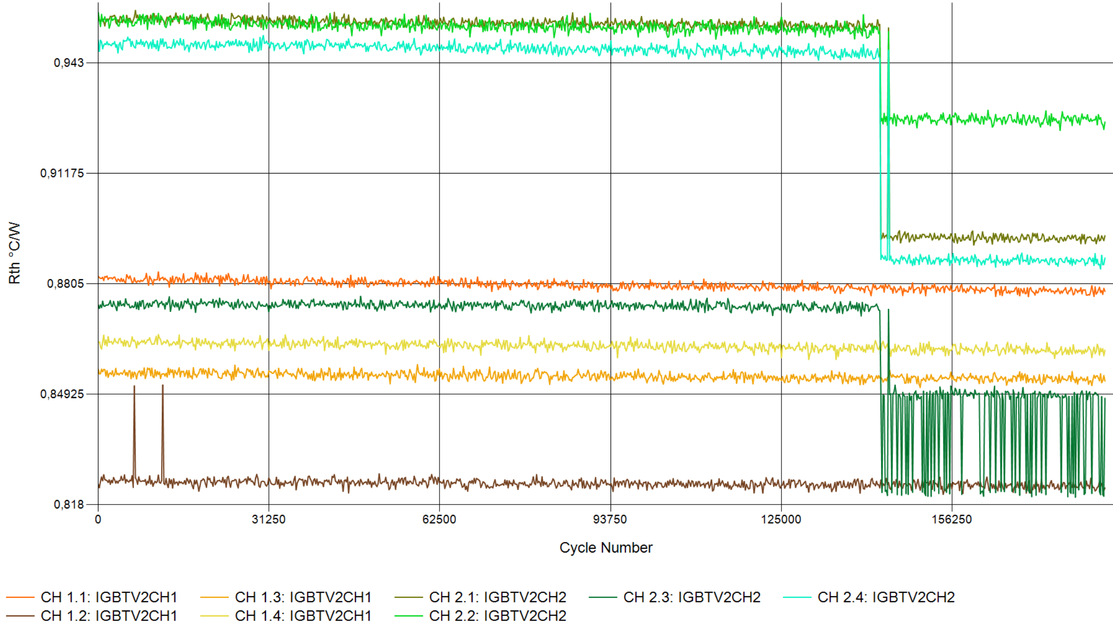


Figure E.38: The thermal resistance value at $C_{\text{th}} = 0.2$ °C/W during experiment C2.

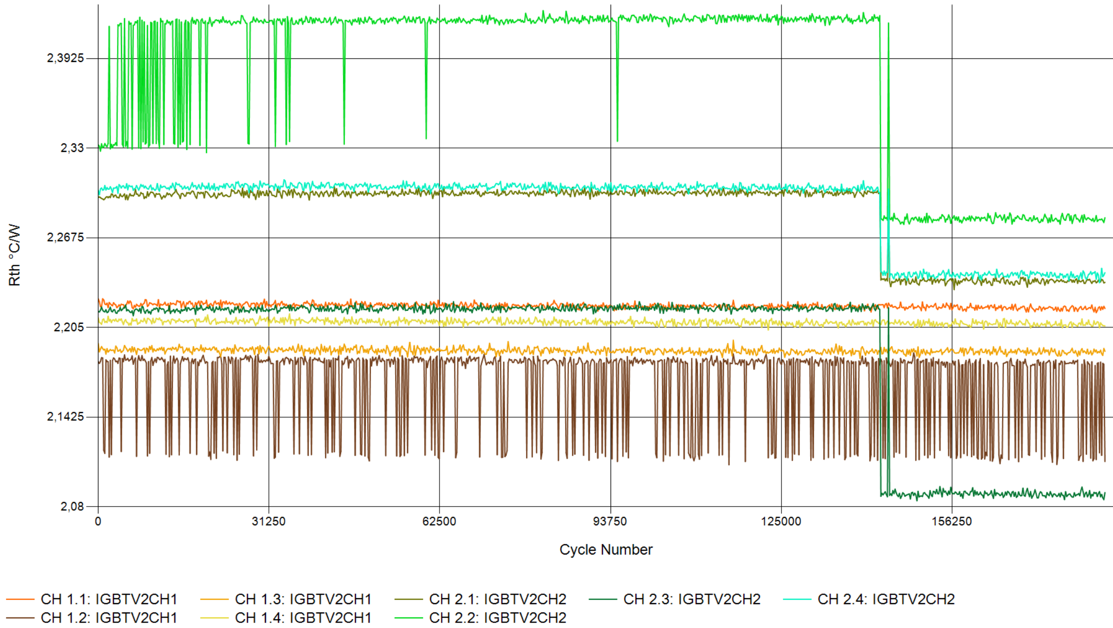


Figure E.39: The thermal resistance value at $C_{\text{th}} = 1$ °C/W during experiment C2.

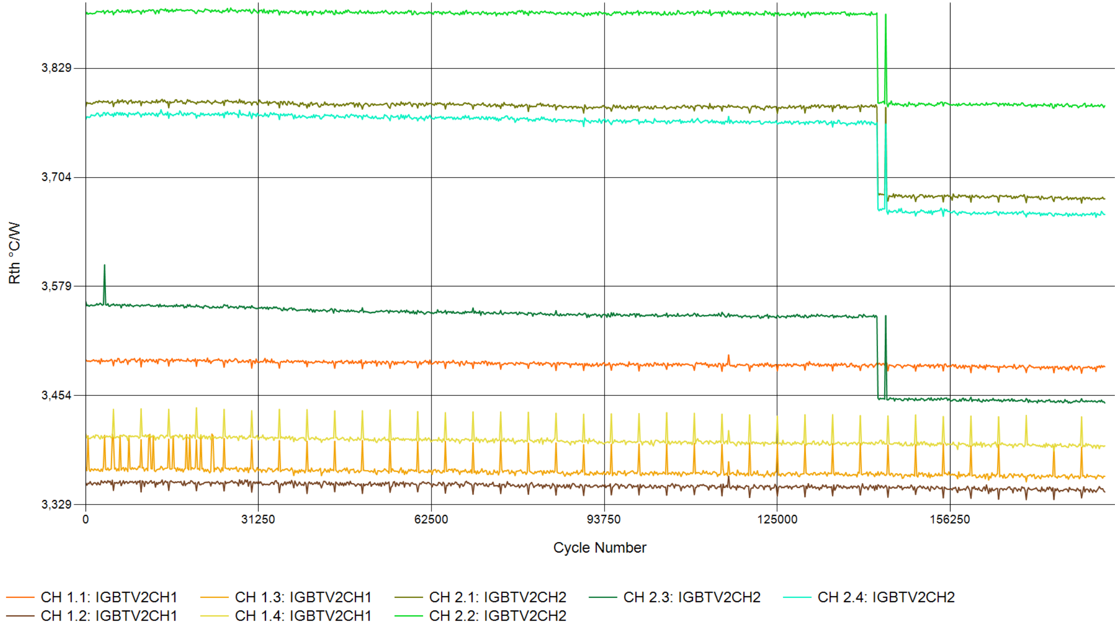


Figure E.40: The thermal resistance value at $C_{\text{th}} = 10$ °C/W during experiment C2.