Synergy between quantum computing and semiconductor technology

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Synergy between quantum computing and semiconductor technology

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ABSTRACT

As part of the National Agenda for Quantum Technology, QuTech (TU Delft and TNO) has agreed to make quantum technology accessible to society and industry via its full-stack prototype: Quantum Inspire. This system includes two different types of programmable quantum chips: circuits made from superconducting materials (transmons), and circuits made from silicon-based materials that localize and control single-electron spins (spin qubits). Silicon-based spin qubits are a natural match to the semiconductor manufacturing community, and several industrial fabrication facilities are already producing spin-qubit chips. Here, we discuss our latest results in spin-qubit technology and highlight where the semiconducting community has opportunities to drive the field forward. Specifically, developments in the following areas would enable fabrication of more powerful spin-qubit based quantum computing devices: circuit design rules implementing cryogenic device physics models, high-fidelity gate patterning of low resistance or superconducting metals, gate-oxide defect mitigation in relevant materials, silicon-germanium heterostructure optimization, and accurate magnetic field generation from on-chip micromagnets.

Keywords: Quantum Computing, Device Manufacturing, Spin Qubit in Silicon

1. INTRODUCTION

The theory of quantum mechanics was developed in the early 20th century to explain microscopic-scale observations that were not compatible with existing established theories at that time, e.g. observations on black body radiation and the photoelectric effect. The understanding and application of quantum mechanics to electronic devices led to the development of lasers and transistors. Later, the ability to very locally and precisely control quantum mechanical principles, such as quantum tunneling, superposition and entanglement, enabled the development of devices for quantum sensing, quantum communication and quantum computing. Technologies leveraging the latest developments in quantum mechanics have therefore led to new and more powerful electronic devices.

The power of quantum computing lies in the unique quantum physical resources of superposition and the entanglement of quantum bits, which allow certain classes of computations to be performed much faster than conventional computers. Grover, for example, showed that quantum search algorithms have a quadratic speedup compared to classical algorithms. Shor's quantum algorithms for factoring, which is based on the quantum Fourier transform, is exponentially faster than known classical algorithms[1,2]. Quantum algorithms that can factor prime numbers exponentially faster could crack currently used public-key encryption methods (e.g. RSA) when applied on a future fully functioning quantum computer. The parallelization of calculations allows for linear time algorithms to be created for the most challenging computational problems, such as simulations of molecules, search algorithms, and a number of optimization problems. Once we have scalable quantum computer designs, an increase of the number of functional qubits will result in dramatically increasing computing power, thus matching the exponential increase in the computational complexity of these problems with the numbers of components. The minimum number of qubits needed to achieve this quantum advantage is, however, many times larger than current state-of-the art.

A general-purpose quantum processor is expected to have societal impact in the fields of energy, health, and security[1,2]. Such general-purpose, fault tolerant, quantum computers will require several developments in the fields of algorithms, error correction schemes, control hardware, and materials development because quantum states used for computation are inherently fragile and susceptible to deterioration from the environment around them. In the shorter term, however, there

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are many developments in hybrid technologies that combine the strengths of classical supercomputers and state-of-the-art, but error-prone, quantum computing devices. These are the so called Noisy Intermediate-Scale Quantum (NISQ) devices and the corresponding NISQ algorithms and applications are also in need of development[3,4,5]. Minimizing the error rates in quantum processors will make them more useful for NISQ algorithms and will also help lower the challenges faced to reach fault tolerance.

Physical realizations of quantum bits span a wide range of material systems including: superconducting circuits[6], silicon-based quantum dots[4], diamond vacancies[7,8], trapped ions[9], photonics[10], and many others. Superconducting circuits are currently the most advanced technology in terms of the number of qubits involved in a computation. Silicon-based quantum dot qubits are currently much smaller in physical size and, hence, are imagined to be scalable to much larger qubit arrays within reasonable chip sizes for PCB integration and dilution refrigerator operation. Spin qubits also have another advantage in that their material and integration-scheme similarity to transistor devices makes them a natural match to the semiconductor manufacturing community, which is capable of producing chips with billions of transistors.

Currently, quantum computing stacks are being developed by various companies and institutes in the world such as Intel, IBM, Google, Honeywell, and QuTech. QuTech, a collaboration between Delft University of Technology (TU Delft) and the Netherlands Organisation for Applied Scientific Research (TNO), has a mission to develop scalable prototypes of quantum computers and an inherently safe quantum internet. As part of the National Agenda for Quantum Technology, QuTech has agreed to make quantum technology accessible to society and industry via its full-stack prototype: Quantum Inspire[11]. This system leverages two different types of programmable quantum chips: devices made from transmons and devices made from spin qubits.

In the following we will describe the recent developments of silicon-based spin-qubit processors for Quantum Inspire and describe how the semiconductor manufacturing community can help advance the state-of-the-art for these devices.

2. SILICON-BASED SPIN-QUBIT PROCESSORS

2.1 Spin qubit chips used in Quantum Inspire

Quantum algorithms that run on spin-qubit devices are enabled by the ability to localize single electrons (or holes) within a host semiconductor and to control the individual spin state and its interaction with spins from neighboring electrons (or holes). The spin state of the single electron can be used as a quantum bit (or qubit), and the controlled interactions between spin states of neighboring electrons can be used to entangle qubits. Multi-electron spin states can also be used as qubits but here we limit ourselves to single-electron qubits. This level of single-electron control is possible once the spin qubit devices are cooled in a dilution refrigerator below a few kelvin. The first spin-qubit device that was publicly available worldwide through the Quantum Inspire cloud platform was QuTech's Spin-2 device. This chip was fabricated in a method similar to previous work[4,11-14]. Figure 1a shows a top-down scanning electron micrograph (SEM) of a similar device prior to the deposition of the top aluminum gate and a cobalt micromagnet (see Figure 1b). The blue and red spots on Figure 1a represent regions under which two quantum dots can be formed; the aluminum metal electrodes used to control the electrons below them will be referred to as quantum dot gates (similar to the gate of a transistor). When the appropriate voltages are applied to all the metal gates in the vicinity, a single electron can be stabilized under each of the two quantum dot gates of the device.

The location of these single electrons is further depicted in the schematic cross section of the device shown in Figure 1b; the region to the right of the vertical cut represents the region on Figure 1a indicated by a dashed line. The electrons trapped within the red and blue dots are located in a thin (4-10 nm) strained silicon quantum well situated between two latticed-matched, relaxed $Si_{70}Ge_{30}$ alloy layers. The conduction band of the strained Si layer is about 100-200 meV lower in energy relative to that of the relaxed $Si_{70}Ge_{30}$ layers[11,15], and this leads to confinement of the electron to about 40-60 nm below the quantum dot gates, which are depicted as yellow lines with positive, +, voltages on them. This semiconductor heterostructure substrate is grown epitaxially with concern for minimizing both oxygen impurities and atomic interdiffusion between the layers. The electrons are therefore confined in all three dimensions: they are defined in the lateral dimension by the metal gates, and in the vertical direction by the quantum well. An estimation of the spatial variation of the potential energy responsible for confining the electrons is sketched by the black line. The potential energy barrier between the quantum dots, and therefore the coupling strength between the two electrons, can be

nominally turned off by tuning the voltage on the aluminum top gate (Figure 1b, right; not shown in Figure 1a) to a sufficiently negative value. It is often desired to quickly reduce this potential energy barrier, e.g., in order to perform a 2-qubit interaction, and this can be done by applying voltage pulses on certain gates near the quantum dot gates. A cobalt micromagnet (Figure 1b, right; not shown in Figure 1a) is here used to create two magnetic field gradients along two different spatial dimensions. This is described in more detail below. The left side of Figure 1b shows the ohmic contact region that is needed to inject electrons into the strained Si layer. Electrons, supplied from a bond pad at the edge of the device, arrive via the aluminum gate on the left. They travel through a platinum contact (red) and into a degenerately doped region of the semiconductor (green), which stays conductive even at cryogenic temperatures. When a positive voltage is applied on a second metal gate (yellow, labelled with a "+" sign), then electrons from the degenerately doped region can flow into the conduction band of the thin strained silicon quantum well (darker blue) creating a two-dimensional electron gas (2DEG) under that gate. This gate can therefore bring electrons to the heart of the device, which may be microns away from the implanted region. Because the implant region may contain defects associated with its fabrication, it is desired to have them some distance away from the quantum activity.

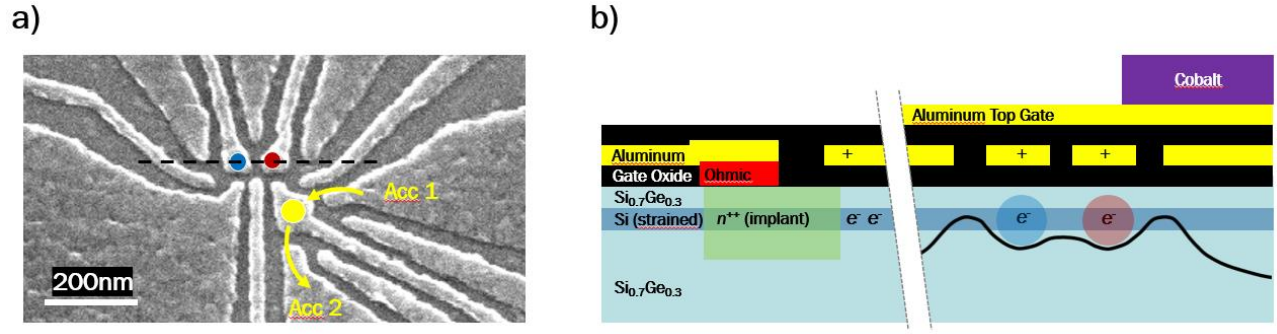

Figure 1. Top-down scanning electron micrograph a) and a cross-sectional schematic b) of QuTech's Spin-2 Device.

The presence or absence of electrons under the gates can be sensed by a single-electron-transistor (SET), which is shown in Figure 1a (yellow). The SET consists of three parts: source and drain electron gas reservoirs, formed below Acc 1 and Acc 2 gates, and a SET island, formed under the central gate of the SET (yellow dot). A voltage difference is applied across the source and drain reservoirs so that, only when the electrochemical potential of the SET island lies in the bias window of the source and drain electrochemical potentials, a current will flow as depicted by the yellow arrows. This property makes the SET current strongly dependent on its electrostatic environment, and a measurable change in current can be observed for single-electron changes in occupation of the red and blue quantum dots. This sensitivity of the SET allows the quantum dots to be controllably filled with single electrons. The SET can also be used to readout the spin state of the single electrons quantum dots using either an Elzerman[16] or Pauli-Spin Blockade[4] method. Further details on the performance of the Spin-2 QPU can be found on the Quantum Inspire webpage[14].

The TNO fabrication team at QuTech is currently developing new Spin-6 QPU devices similar to those already published[4]. A top-down false-color SEM of a 6-qubit chip is shown Figure 2a. Figures 2b and 2c show two different schematic cross-sectional images of the device when cut along the two different axes represented by the dashed lines in Figure 2a. The six single-electron qubits are situated below the 6 yellow-colored "plunger" gates, and the potential energy barrier between any set of two neighboring electrons can be independently controlled by the voltage on the corresponding blue-colored "barrier" gate situated between them. Figure 4c shows that the electron is confined in the other lateral dimension by the presence of the screening and drive gates. The spatial extent of the electron wavefunction is rather small due to the fine critical dimensions (~50 nm x 100 nm) of the plunger and barrier gates. Electrons can be supplied from the ohmic contacts to the plunger quantum dots by way of the red-colored metal gates; the red gate is tuned to a potential to accumulate a reservoir of electron charges, and then the outer-most blue barrier gates must be tuned to a voltage to allow tunneling from that reservoir into the plunger quantum dot. In this device, the reservoir under the red gates can also be operated as an SET; and there is one SET on either side of the six-dot array for measurement of the various electrons as described above.

Control of an individual electron spin is achieved by electric dipole spin resonance (EDSR), which is a manipulation of the electron with the electric field of the drive gate in the magnetic field gradient generated by the micromagnet. As indicated in Figure 2c, the single electron, which is confined within the strained-silicon layer, experiences a local

magnetic field gradient in the direction along the blue arrow (labeled "Drive Gradient"). When gigahertz (GHz) electromagnetic radiation is applied to the drive gate, the electric field oscillates the mean position of the electron quickly along the axis of the blue arrow, and the electron experiences a time-varying magnetic field. When the correct frequency of GHz electromagnetic radiation is applied as a pulse with the correct time duration, the electron spin can be flipped (or set to any orientation). In order to achieve addressability among the 6 different single-electron qubits of the device, the micromagnets also need to supply a magnetic field gradient along the axis of the dot array (schematically represented in Figure 2b and labeled "Qubit Frequency Gradient"). This gradient ensures that each electron has a different resonant drive frequency and can therefore be controled independently. This, together with short entangling pulses applied to the barrier gates between two neighboring electrons, supplies a universal set of control operations as needed for running quantum computing algorithms.

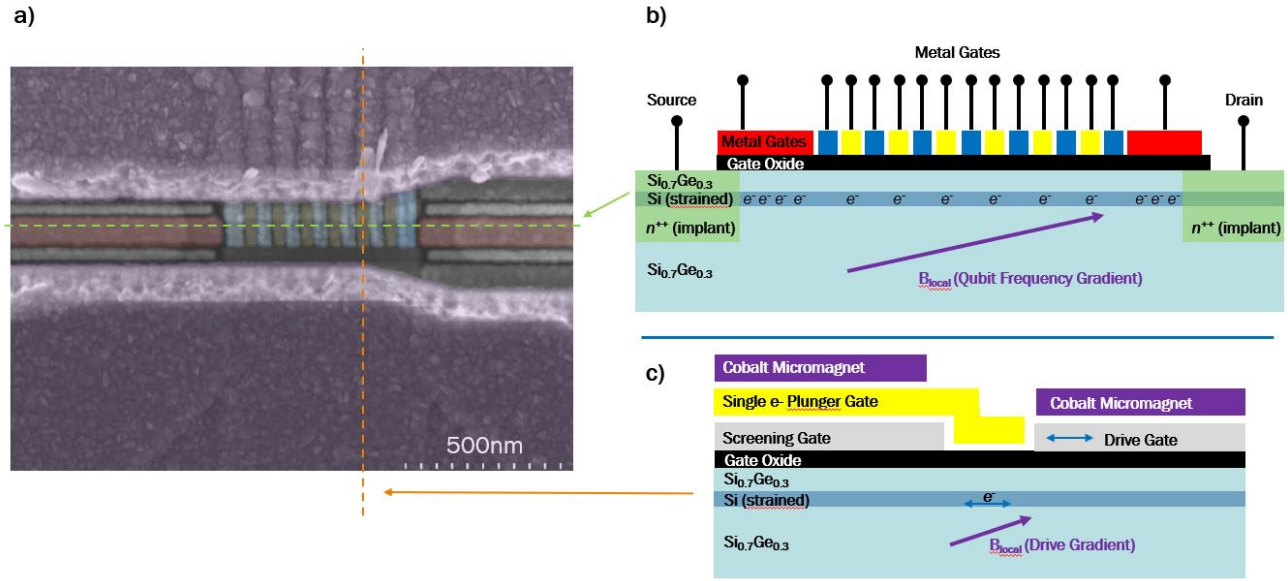

Figure 2. Top-down false-color scanning electron micrograph a) and cross-sectional schematic views b) and c) of QuTech's Spin-6 device.

Figures 1 and 2 together describe the functionning principles of spin qubit chips fabricated with a silicon quantum well where single electrons can be localized and controled. A new exciting technology at QuTech uses the localization of holes within a similar thin quantum well of strained germanium.[17]. A recent demonstration of this technology generated a non-trivial four-qubit state with hole spin qubits in a 2x2 array. These germanium-based qubits do not require micromagnets, the quantum operations can be performed all electrically, and controllable qubit couplings are achieved along both directions of the array. This particular circuit is therefore rather compact and shows promise of achieving scalable designs with tight qubit packing.

2.2 Industrial spin qubit chip fabrication

As can be seen in Figures 1 and 2, spin-qubit devices look at some level like multi-gate transistors, where single electrons (supplied by implanted source and drain regions) are localized under plunger gates, the occupancy and interactions are controlled by gate voltages, and the spin state of the electron can be controlled by radio-frequency pulses. Accordingly, many advanced semiconductor fabrication facilities, such as Intel[18,19], CEA Leti together with CNRS[20], and IMEC[21] are fabricating and optimizing spin qubit devices within their industrial factories. QuTech researchers have recently measured spin-qubit devices fabricated in Intel's 300mm CMOS fabrication facility[18]. These devices were fabricated using standard optical lithographic and pitch division techniques to achieve 30 nm gates spaced roughly 50 nm apart. Intel has fabricated both fin-based Si-MOS[18] and epitaxially grown quantum-well[19] devices. These are all impressive demonstrations for the future scalability of spin qubit devices within CMOS-based high-volume manufacturing settings, and the outlook for these industries is very encouraging. A few challenges that these factories face, however, are the inflexibility to test new materials quickly given the strict contamination requirements, the cost and

long lead times associated with optical mask design changes, the constraints imposed by design rules and acceptable processing flows, and (sometimes) the inability to test devices at intermediate stages of device fabrication. These can make circuit design modifications, process choices, and material exploration costly and slow.

2.3 QuTech's spin qubit chip fabrication

The QuTech fabrication facility provides a complementary, but not CMOS-compatible, approach. Here, QuTech's advantage lies in the ability to rapidly screen new materials, systematically assess how the material properties evolve throughout the fabrication process, and quickly evaluate new circuit designs for the establishment of quantum-based design rules. We believe that QuTech is therefore a powerful scale-up partner for industry by providing complementary advantages. Chips fabricated at QuTech use electron-beam patterning and metal lift-off techniques to achieve gate patterning at similar critical dimensions as industrial factories, e.g., gates width of order 40-50 nm[4,19]. While this lift-off patterning method is not CMOS compatible, new layouts of chips with multiple layers of metallization can be fabricated and measured usually within a few weeks. This rate of information is beneficial particularly because there are no clear design rules already widely recognized for the behavior of low-temperature 2DEGs.

Another advantage of the QuTech fabrication methods is that we routinely evaluate the device material quality at various stages during the fabrication process via a series of test-structures that can methodically evaluate process-induced material changes. This may not be possible in larger facilities, where testable devices may require the full fabrication flow in order to be fully connectorized for testing. This can make it more challenging to evaluate the impact of a single particular step in a long, often hundreds-of-step, process flow. Figure 3 shows QuTech's process and measurement flow, which was developed to evaluate the properties of the chip at different stages of the fabrication process. The first step in the process, Figure 3a, is the growth of the isotopically purified silicon and germanium heterostructure stack at the 4" wafer level. These stacks can be immediately quantified by high resolution transmission-electron-microscopy (TEM) and atom-probe tomography for structural and chemical analysis[22,23]. The next step, Figure 3b, involves an optical-lithography patterning loop at the 4" wafer level to generate multiple die; some die contain Hall bars and other test structures (Figure 3b1), and others contain markers, implants, and ohmic contacts for subsequent nano-fabrication of the quantum devices. The wafer is then diced to remove some Hall-bar-containing die for immediate cryogenic measurement to assess the substrate quality under the minimum number of processing steps. Other die are stored or processed further using nano-fabrication techniques (Figure 3c). A variety of nano fabricated devices (Figure 3c1-c3) can be made. Simple structures with only a single layer of metallization can be used to test new gate materials, the performance of the quantum well at small dimensions (Figure 3c2), and the defectivity of various gate oxides (Figure 3c2). Structures with multiple metal interconnect layers, such as the quantum devices themselves (Figure 3c) and other test structures (Figure 3c2-3), can also be fabricated. Such multi-layer test structures can be used to evaluate back-end interconnect health (dielectric constant, leakage, and breakdown risk), process-induced changes to gate oxide defects, low-temperature turn-on voltage values, and physics necessary to generate 2DEG-related circuit design rules. The Hall bars from the optical-lithography fabrication step can also be monitored after any additional processing and compared with the results from initial fabrication. The fully fabricated quantum chips can be cooled to milliKelvin temperatures for the most relevant (but also most-time consuming) testing; the best chips move on to dilution fridges dedicated either for Quantum Inspire application or scientific studies by our TU Delft colleagues. The results from any of these various devices are fed back into the fabrication process and/or circuit designs for rapid modifications. This process flow not only allows rapid chip design development but also enables to methodically study material/process interactions, both of which are expected to become more complicated as quantum chips scale to larger qubit numbers.

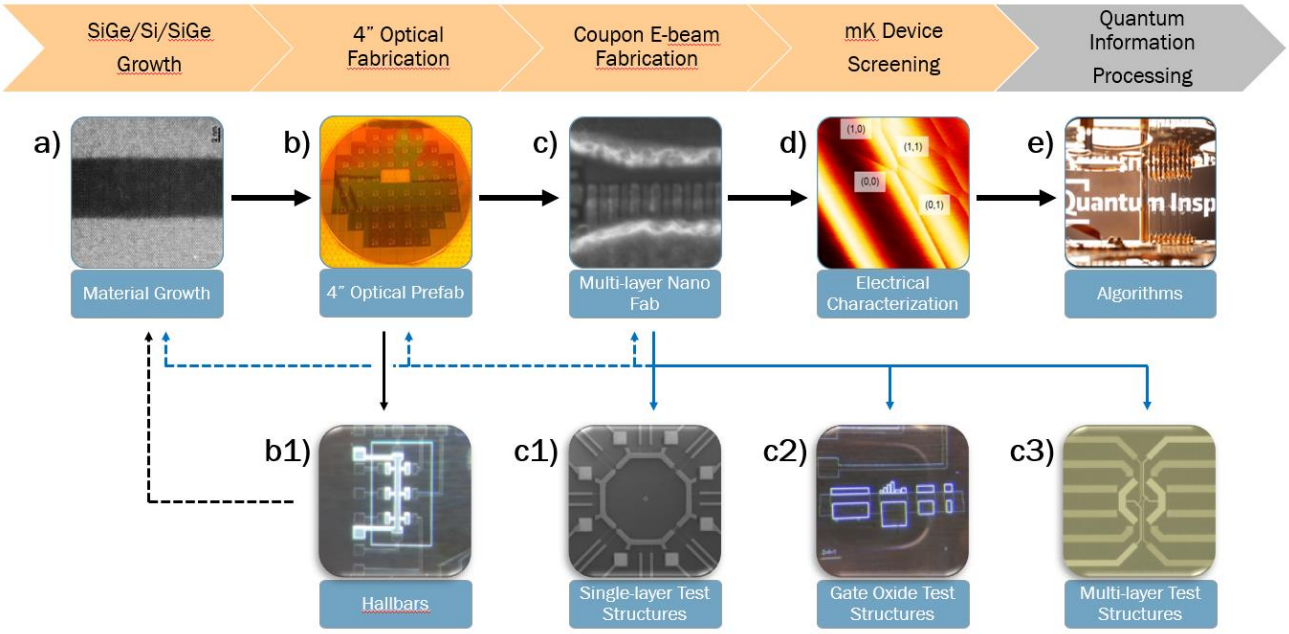

Figure 3. A process flow used at QuTech to evaluate new chip designs and materials used in the fabrication of spin qubit chips.

3. FROM LAB TO FAB: HOW THE SEMICON INDUSTRY CAN HELP

As quantum computing chips scale to ever increasing qubit numbers, the complexity of the circuit design and the level of perfection required from each of the materials will grow and become more challenging to integrate together into successful devices. As each of these areas become more complex, specialists with highly technical knowledge will become all the more critical, as well as integrators (system engineers), to bring all the pieces together seamlessly. Here, we share our perspective on where regions of unique expertise will be needed to drive the development of spin qubit circuits to the next level. These are shown schematically in Figure 4, and will be described in more detail in the following sections. We feel that these are work areas are where the semiconductor industry is uniquely poised to facilitate rapid development in quantum chip performance.

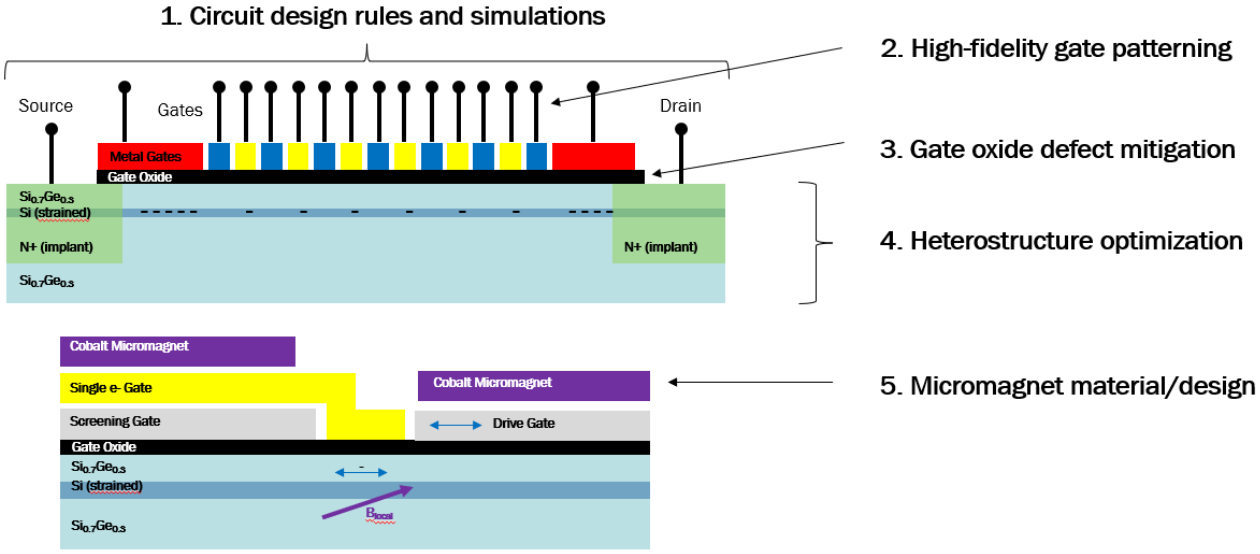

Figure 4. A schematic representation of a spin qubit chip highlighting material and technological areas where the expertise of the semiconductor industry can help improve device performance.

3.1 Circuit design rules and simulations

Circuit design rules are used to ensure that layout changes implemented in next-generation devices don't incur deleterious performance effects. Process design kits add another layer of complexity by incorporating constraints from the physical fabrication processes of factory-specific sites. The 300-mm industries listed above implement all of these tools in the fabrication of conventional electronic devices. While many of the fundamentals behind these tools will provide useful direction for spin qubit fabrication, it's not obvious that all those design rules will apply to spin qubit chips operating at cryogenic temperatures. Operation at mK temperature will certainly change some critical parameters, such as semiconductor device modeling physics[24], while other material and circuit differences, such as dielectric properties (e.g., capacitance, leakage and breakdown), metal line resistance, and signal propagation, are not well documented at these temperatures. Modeling and data on carrier populations and current flow within the 2DEG structures are also not well reported. While much work has been done on how to understand the device physics of peripheral CMOS structures, such as amplifiers, analog-to-digital converters, digital-to-analog converter, and other components, at cryogenic temperatures[24], we have seen far fewer reports on the device physics of free carriers in the qubit chip itself outside of the SET and qubit regions. Here, we are specifically referring to current transport and electric field distributions in the accumulated reservoirs and regions closer to the ohmics. Understanding this aspect of device physics at cryogenic temperatures is important because some quantum chips show current flow in unwanted regions of the device, and these currents can complicate measurements of the intended quantum activity. Then, once the device physics of interconnect material properties at cryogenic temperatures is also well understood, a combination of DC and RF modeling of the spin qubit chips can be undertaken. Data can be taken to confirm and update models, and together a more relevant set of design rules and process design kits can be built.

Interconnect fanout and multiplexing of qubits in a scalable way (analogous to the exponent of Rent's Rule) will become more complex as semiconductor quantum devices grow in qubit count[25]. There have been multiple papers working through scalable designs as thought experiments given realistic spin qubit parameters constraints[26-28]. These works are impressive in their device simulations and attention to detail of quantum mechanical behavior of the chips, but there are areas where a more concerted effort in generating data supporting the scaling plan is needed. QuTech colleagues at Delft are, for example, testing qubit sub-lattices[17] of the larger crossbar array proposed by Li[26]. These researchers are also working on methods to make quantum dots sufficiently similar in electrical properties to be addressed in a multiplexing scheme. Demonstration of the fabrication of superconducting lines at the relevant pitch (vide infra) that can carry the currents needed to effectively drive a spin qubit via ESR still needs to be demonstrated. In short, interesting ideas for scalable qubit design have been proposed based upon best-effort modeling, but relevant materials data are still needed as

inputs to properly generate process-design kits needed for scaling. There are thus opportunities to generate data-based 3D electromagnetic modeling software for semiconductor carrier physics at cryogenic temperatures, generation of cryogenic models for the interconnect fanout, co-design of qubit array geometries for RF and DC qubit control, and understanding methods to reduce heat dissipation in quantum chips and peripheral electronics. When done effectively, these pieces can be put together into a data-based process to effectively compare scalable designs for quantum computing chips.

3.2 High-fidelity gate patterning

Clearly, a high level of pattern fidelity is required for the metallic gates as they define the lateral extent of the potential wells that confine the single charge-carrier spins (qubits). 300 mm factories with extreme UV patterning and/or pitch division techniques have demonstrated high-fidelity patterning of ultra-fine pitch metal lines of healthy line resistances[19]. The natural progression of the microelectronics industry toward ever smaller gate pitch to values of 50 nm and below is therefore synergistic with the needs of the quantum community, where spin qubit researchers want to test smaller-sized qubits positioned closer together. More rapid and less costly ways to generate optical masks for fine-pitch patterning would also be desired. The time and cost to make design changes is quite high, so efforts to make mask design changes more economical are appreciated. This desire is not unique to the field of quantum computing and is already being driven by the semiconductor industry.

One challenge with quantum chip operation is thermal dissipation. This is generally assumed to be due to the metal line resistance (and also to the resistance associated with carriers in the quantum well). The impact of heating from on-chip resistance is only expected to grow as circuit sizes continue to get larger. Demonstrations of fine-pitch metal lines with low-resistance or superconducting metal materials is therefore of interest. Many spin qubit devices, like those described above, also require an external magnetic field in the range of 0.5 to 2 T, so low resistance, or superconducting, metal lines in the presence of these magnetic field conditions are also desired.

Methods for customizable patterning at fine pitches with minimal dielectric impact is also desired. Electron-beam patterning is known to induce defects in SiO_2-based dielectric materials[29]. Thus, studies detailing the trade-offs between resolution and dielectric material damage as a function of resist material, dose, excitation energy, and dielectric material would be particularly illuminating.

3.3 Gate oxide defect mitigation

Since the early days of MOSFET transistors it was realized that gate oxide defects need to be sufficiently low in density for healthy device operation[30]. Several textbook chapters[31-32] and at least several hundred journal articles have been published on the topic of gate oxide defect characterization and mitigation. The thermally grown Si/SiO_2/Metal and, more recently, the Si/SiO_x/High-k/Metal systems have been well characterized by a large number of methods. Figure 5a shows a 2D chemical representation of the various types of defects understood to be present at the thermally grown Si/SiO_2/Metal interface. Briefly, D_{IT} refers to dangling bond atomic orbitals on silicon or germanium atoms at the interface of the semiconductor that can accept and release charge under mild operating voltages at room temperature. Fixed charge, Q_f, refers to the empty atomic orbitals on silicon atoms in the oxide transistion region between the semiconductor surface and lower-defect-density SiO_2 bulk. Oxide trapped charge, ρ_{OT}, is understood to be due to missing O atoms in the SiO_2 matrix, which are often formed as a result of damage from various forms of radiation[29]. Mobile charges, ρ_M, such as Na^+ or K^+ can be introduced due to poor handling or contaminated quartz chambers used for the thermal oxide growth. More recently, there have been reports that proton, H^+, can be an important mobile charge species[33]. This schematic representation indeed oversimplies the more complex chemical nature of the defects, which have been more rigorously identified chemically through the power of EPR-related techniques[34]. For the thermally grown Si/SiO_2/Metal system, the level of defects have reached extremely low levels through a variety of process controls and defect-mitigating techniques. By proper cleaning of the quartz furnace and control of the oxidation process (e.g., injection of chlorine-containing species, using dry O_2, and tuning the post oxidation conditions and ramp down) the number of mobile charges, fixed charges and oxide trapped charges can be dramatically reduced. Application of a forming gas anneal (e.g., 5-10% H_2 in N_2 for several tens of minutes at 300-500 °C) can reduce D_{IT} nearly 3 orders of magnitude, such that there are only a few defects per million surface atoms. The thermally grown Si/SiO_2/Metal system therefore represents one of the cleanest gate oxide systems reported to date. This provides sufficient motivation for the

use of SiMOS based spin qubit devices. One complication, however, is that the efficacy of forming gas anneal can depend on the metal, the processing steps performed on the wafer, and the crystallographic face of silicon at the oxide interface. The best gate-oxide dielectrics can be harmed by uncontrolled downstream processing[29]. Despite it being one of the best gate oxides for transistor based devices, the use of SiMOS systems for spin qubits still seems to show a relatively high influence of defectivity (as evidenced by the presence of spurious dots[19]). There are only a few reports[19] quantifying defect densities for SiMOS-based quantum devices, and even the best fully-fabricated test devices show defect levels 10-100 times larger than the best MOSCAP samples. It is an open question whether SiMOS-based quantum devices could be further improved through better quantification and monitoring of defects as a function of processing conditions.

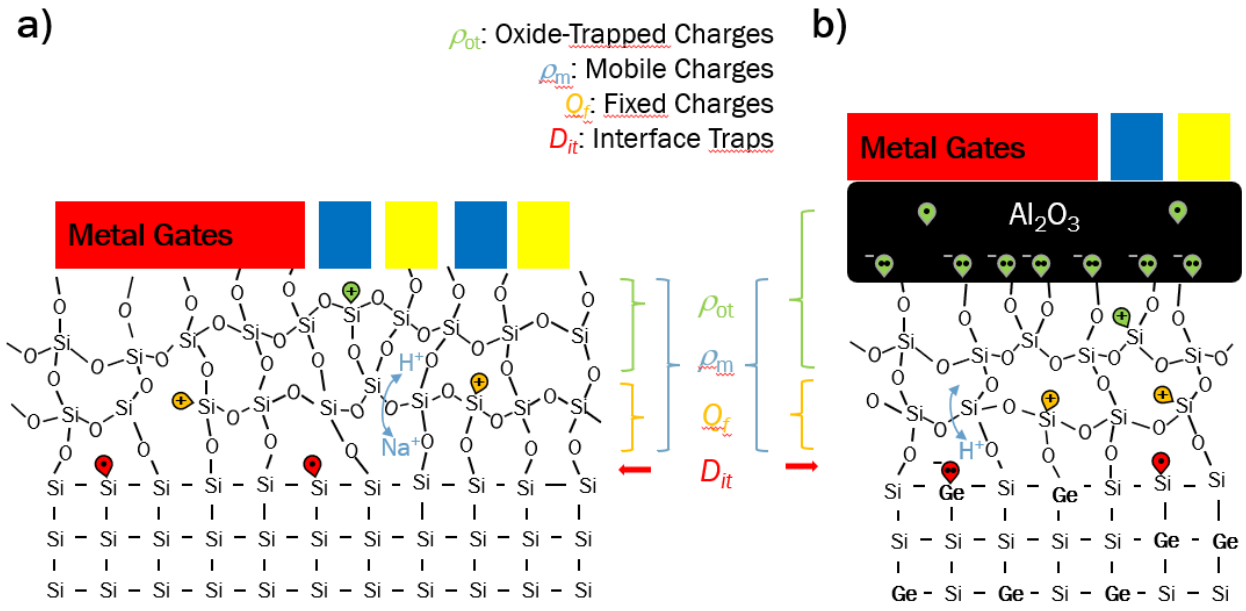

Figure 5. A schematic of the various chemical defects that could exist within different gate oxide materials used in spin qubit devices.

While SiMOS-based quantum devices are perhaps most closely resembling transistors of previous generations, there is new excitement within the quantum computing field for devices containing a strained-silicon buried quantum well within a $Si_{70}Ge_{30}$ alloy, as described in section 2.1 above. In these devices, the electrons reside in the quantum well several tens of nanometers below the defective gate oxide interface. This provides a benefit only in so far as the interface defect density is the same or better (or at least not much worse) than the SiMOS devices. A typical gate stack for these devices include a process-induced surface oxidization layer followed by atomic layer deposition (ALD) of a dielectric material, such as Al_2O_3, for the gate oxide. While there is still a lot of room for careful interface science to identify the gate oxide defects on integrated devices, a schematic of the possible gate oxide defects present on these types of devices is shown in Figure 5b. When the silicon germanium heterostack is grown, there is often a capping layer of strained silicon deposited at the top of the wafer. This layer can be as thin as a few monolayers to several nanometers thick. The layer is intended to be as thin as possible, and ideally almost fully consumed into SiO_2 throughout the integration process so that there is no surface conduction channel in parallel with the quantum well. If a few atomic layers of the silicon cap still exist upon completion of the device fabrication, then the schematic of Figure 5a may be a reasonable representation of the types of surface defects; the strain in the cap layer may however lead to different defect densities than that of a typical, unstrained, MOS device. If the silicon cap is fully consumed by oxidation, and the $Si_{70}Ge_{30}$ layer begins to oxidize, then the presence of germanium-based dangling bonds is also reasonable (Figure 5b). EPR studies have demonstrated that Ge dangling bonds can be measured at the surface of oxidized SiGe alloys[35]. The presence of Ge within the oxide is, however, not often seen. The addition of the atomic-layer deposition (ALD) of Al_2O_3 on top of SiO_2 is known to form a

layer of negative charge[36] that can be reduced by UV irradiation. For spin qubits operating with single electrons in strained silicon quantum wells, this layer of negative charge helps to prevent electron accumulation in regions outside of where there are intented. Figure 9, thus, shows the many charge defects that can exist in gate oxides.

Proper quantification of the defect densities is normally done electrically with capacitance-voltage and conductance-voltage data and/or EPR techniques. Peaks in conductance can often be equated to D_{IT} under certain conditions, hysteretic behavior to ρ_M, and the position of the flatband voltage to Q_f and ρ_{OT}, the latter two of which can be further segmented by a thickness depedences of the gate oxide[31]. Accurate extraction of the flat-band voltage requires capacitance-voltage data clean enough to be fit to state-of-the-art semiconductor physics models. For some systems, D_{IT} and semiconductor bulk defects are simply too high for such analysis to work at room temperature, but measurement at temperatures down to 100 K can result in far cleaner data[37]. This means that proper quantitative analysis of the various defect densities can only be extracted using low-temperature probe stations, where there are not many turn-key automated systems available for researchers. Low-temperature electrical characterization is also critical for the evaluation of dielectric leakage and breakdown statistics of dielectrics to enable proper circuit design rules. Leakage measurements, which are often reported at room temperature, are generally dominated by thermally activated mechanisms, and the estimation of the more relevant temperature-independent tunneling mechanism for leakage can only be assessed via a temperature study[32].

Similar to the decades of work on the Si/SiO_2/Metal-gate and Si/High-k/Metal-gate structures, there is an opportunity for the semiconducting manufacturing community to participate in the characterization and subsequent mitigation of the defects specific to the materials systems and processing conditions used in the fabrication of quantum devices. Automated metrology that can routinely test material properties as a function of temperature is needed in order to understand how the various defects, typically characterized between 50 and 300 K, behave at temperatures below 1 K. Once the defects densities can be fully characterized and independently tuned, their contribution to charge noise and device drift can be evaluated at ultra-low temperatures. Understanding the precise chemical contributors to charge noise and device drift and reducing their influence on qubits would be a huge success for the quantum computing community.

3.4 Heterostructure optimization

As the spin qubits are confined to thin quantum wells of strained silicon (or strained germanium) situated between two layers of silicon-germanium alloy (as shown in Figures 1b, 2b-c, and 3a), the atomic perfection of these materials and their interfaces is paramount. Thankfully, high-quality CVD reactors are available such that fairly clean structures can be reliably fabricated under the right processing conditions. Mobility measurements[38] suggest that defects at the gate-oxide interface are still the dominant mechanism for carrier scattering at low densities. But, high-fidelity single electron control at the quantum level requires proper band structure engineering; high valley splitting between the otherwise degenerate conduction band minima is, for example, assumed to require very sharp interfaces between the silicon-germanium alloy and the strained-silicon layer[39-40]. Achieving sharp defect-free interfaces is an interplay between needing a sufficiently high temperature to get rapid growth (with minimum oxygen, carbon, and other various defects incorporated into the crystal) and a low-enough temperature to minimize surface roughening or interdiffusion of Ge into the Si quantum well. Clean tools with ultra-low base pressures and new Si and Ge precursors that lower the temperature of highly pure material growth could enable the continued perfection of these materials scale[22,41].

Because the electron spin can interact with the atomic spins of nearby nuclei, there has been a recent push to move toward using isotopically purified silicon and germanium precursors in the growth of the semiconductor epitaxial layers[42,43]. The development of new precursors chemically designed to enhance growth rates of isotopically pure semiconductors will help the development of these materials for quantum computing. After the structure is grown, the methods for bulk purity and interface analysis only keep getting more powerful. Raman spectroscopy, and X-ray diffraction (XRD) studies with reciprocal space mapping (RSM) can be used to identify stress in the quantum well. Secondary ion mass spectroscopy (SIMS) can detect very low levels of oxygen, carbon, and other defects in the materials. Transmission electron microscopy (TEM) analysis is yielding increasingly higher atomic resolution images and chemical analysis, and recent atom-probe tomography can deliver impressive 3D maps of atomic positions[22,23].

3.5 Micromagnet material and design

As described in section 2.1, the micromagnet structure on top of the spin qubit device is essential for fast qubit operation[4], and to provide magnetic field gradients along both the qubit array (for unique qubit addressability) and perpendicular to the array (for fast single-electron spin control). The ferromagnetic micromagnet, thus, needs to create very precise magnetic field gradients along two axes of the device chip. It was shown that a thorough study into the desired effect of, and the subsequent configuration and design of, the micromagnets should be done before micromagnet fabrication[4]. Accurate magnetic field simulation and calculations, calibrated by experimental data, are therefore needed to assess the device-dependent sensitivity factors associated with micromagnet shape, placement misalignment, and the impacts on driving gradient, decoherence gradient, and qubit frequency bandwidth. The magnetic properties of a patterned micromagnet are determined partly by a) the bulk and surface magnetic properties, b) the micromagnet size and shape, and c) sufficient control of fabrication-related defects. The most important of these are the last two.

The magnetic thin films should have low stress, to enable stable film deposition up to a few 100 nm in thickness, and well controlled magnetic properties. Conventional BH loop tools, tools based upon superconducting quantum interference devices (SQUIDs), and high-resolution x-ray diffraction (HR XRD) tools can be used to measure the magnetic properties and structure of thin films. The benefit of SQUIDs is that the magnetization properties can be measured at low temperatures, conditions that are more relevant to device operation. Conventional material chemical analysis tools like x-ray photoelectron spectroscopy (XPS) can be used understand the oxidation state of the magnet surface after deposition and fabrication processing. But, the extent to which the surface oxide (which often has its own magnetic properties) plays on the resulting magnetic field profile is still an open question. Another critical bulk property is film stress. Deposition of magnet films of desired thickness near 200 nm has led to unreliable amounts of film stress run-to-run that pose a risk to device yield. Given that micromagnet deposition is one of the last steps in the fabrication of devices, a low yield during magnet deposition results in a lot of wasted fabrication effort. Figure 6 shows the partial delamination of a micromagnet as a result of excessive film stress. Further development and improvements in deposition techniques to achieve reliable adhesion layers and magnetic films properties are therefore needed.

Even with a reliable thin-film deposition method, patterning of the magnets into small structures capable of creating the necessary magnetic field gradients at the location of the single electrons is another challenge. One aspect of the challenge is the size and shape dependence of the resulting magnetic field orientation. Larger aspect ratios in the dimensions of the magnet are more likely to result in magnetic fields aligning to the long axis, but larger structures can form multiple domains of uncontrolled magnetic field orientation. In order to generate the relatively high magnetic field gradients needed, a given micromagnet may need to be larger than what can be accommodated by a single magnetic domain. A second challenge is the fabrication of a given micromagnet design. From a nanofabrication perspective, we need to understand the impact of micromagnet alignment relative to the device below it, topography of magnet (note from Figure 2a that the magnets rest on top of the patterned gates), line-edge roughness, and deposition-related defects such as larger grains, particles, and contamination during lift-off. Methods to characterize the magnetic properties of patterned structures, such as for example vibrating-sample magnetometers[44], scanning probe microscopy (AFM, MFM)[45], Kerr microscope, and others, are therefore critical in understanding how micromagnet design and fabrication impact the magnetic fields they generate.

Magnet simulation software is used to guide initial micromagnet design, and therefore improvements in these types tools with respect to capturing the nuance described above is critical. Such data-based modeling software could help quantify fabrication tolerances and explore pathways to extend the tolerance range. The important outcome of such analysis would be a range of recommended parameters for optimal micromagnet design without over simplistic assumptions on materials and fabrication realities. Tools of this nature will be critical for evaluating the scalability of different magnetic materials and designs for larger linear arrays and/or grids of future spin qubit chips.

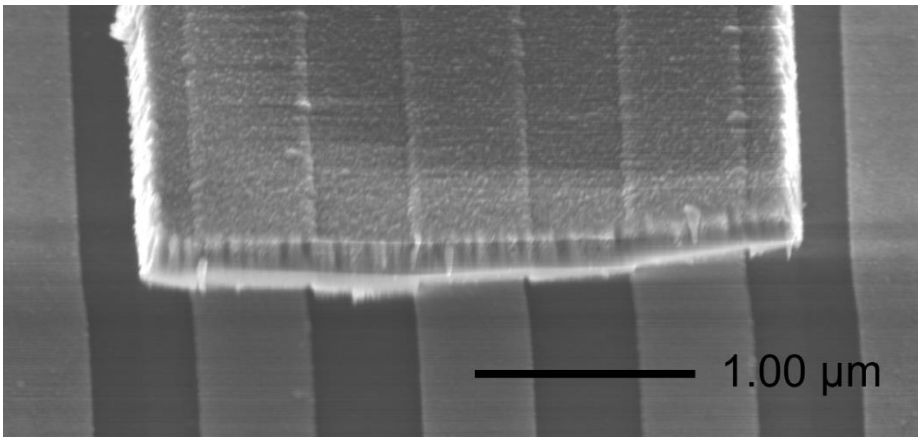

Figure 6. SEM image of a cobalt micromagnet on top of Ti/Pd gates of a quantum dot device.

4. FROM FAB TO PRODUCT: QUANTUM INSPIRE

Many of the breakthroughs involving developments in epitaxial materials, spin qubit device design, control schemes and algorithms have come from academic groups around the world. At TNO, it is our goal to bring this new technology from the realm of fundamental studies to applied research and product development. For this reason, we developed Quantum Inspire (QI), QuTech's cloud platform for quantum computation[46]. The full-stack QI system, currently containing a QuTech-fabricated spin qubit processor with cloud-based public access, comprises of several layers including quantum hardware, classical control electronics, and a software front-end with a cloud-accessible web-interface. Full-stack systems are essential for understanding and developing the quantum computing paradigm. By careful analysis of the individual system layers and their interdependencies it is possible to identify gaps and required next steps in innovation roadmaps and supply chains. Offering QI to the public provides another method to understand user needs and stimulate the growth of the exciting field. The QI platform is developed with a high degree of modularity. It is clear that the semiconductor industry can play a key role in the development of quantum computing technology.

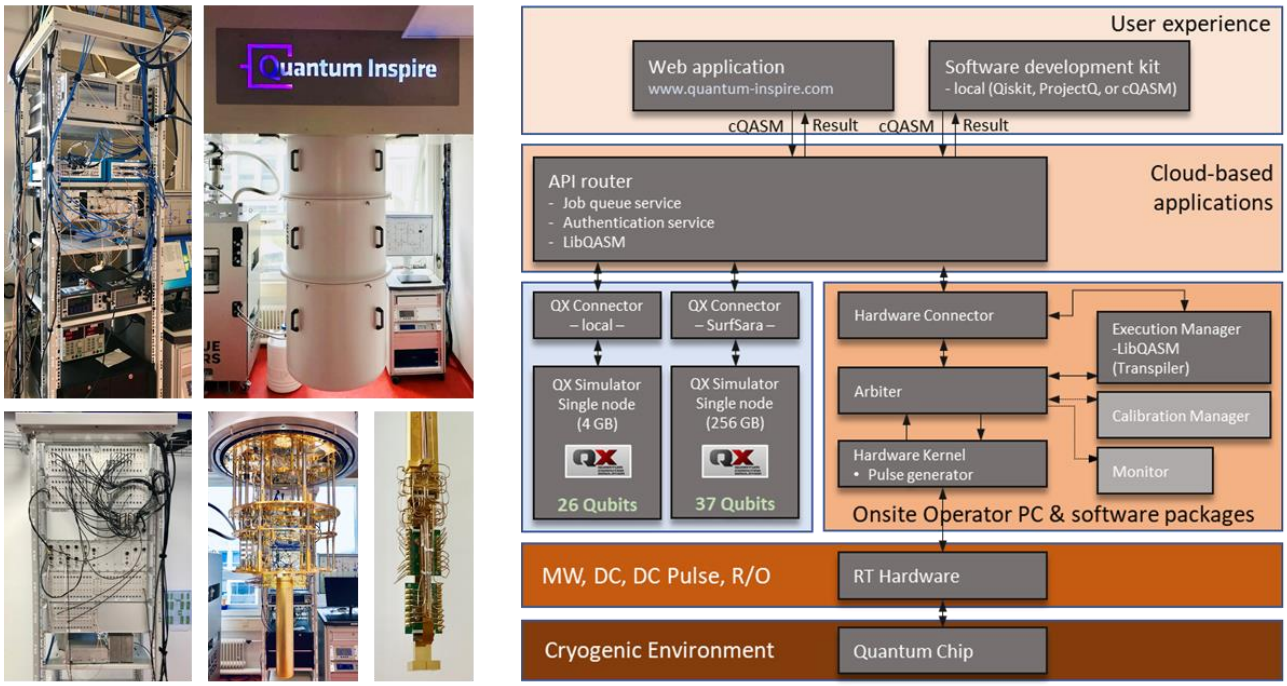

Figure 7. Quantum Inspire's full stack cloud quantum computing system, hardware stack for Spin qubits (left) and system architecture (right).

5. SUMMARY AND OUTLOOK

Quantum technology is now steadily maturing towards a novel discipline where full-stack systems considerations are essential for future development, research and engineering. QuTech (TU Delft and TNO) has agreed to make quantum technology for computing accessible to society and industry via its full-stack prototype Quantum Inspire, which leverages two different types of programmable quantum chips: circuits made from superconducting materials (transmons), and circuits made from silicon-based materials that localize and control single-electron spins (spin qubits). Silicon-based spin qubits are a natural match to the semiconductor manufacturing community. Here, we have discussed the latest results in spin-qubit technology and we have highlighted where the semiconductor community has opportunities to drive the field forward.

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