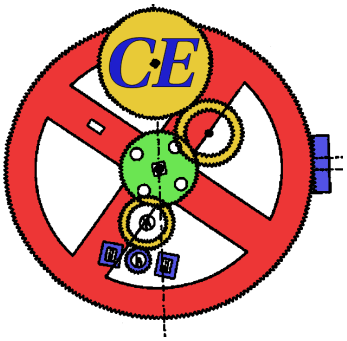

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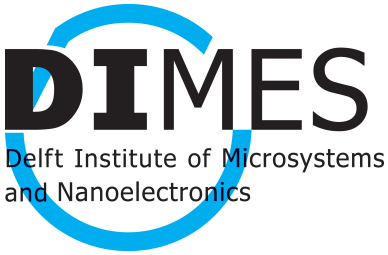
2009

MSc THESIS

A Flexible Electronic Paper with Integrated Display Driver using Single Grain TFT Technology

Wei Man Chim



CE-MS-2009-01

Abstract

DIMES and the department Computer Engineering from the University of Technology Delft are developing an Electronic Paper Display. This display will have a paper-like appearance (paper-white, wide view angle), and it can retain its display contents even after power down. The E-paper Display will have its own display driver integrated in the display itself. In the future it will be possible to integrate with the E-Paper Display, large and complex digital circuits or even microcontrollers with their peripherals.
We are using the Single Grain TFT (SG-TFT) Technology developed at DIMES for the integrated electronics. Using this technology we are able to create high performance transistors out of amorphous silicon film. With these TFTs, a Display Driver is build that will control the QR-LPD E-Paper material from Bridgestone. This E-Paper material has an ultra fast pixel response, which makes it possible to use this E-Paper to view animations.
This E-Paper Display will showcase some of the possibilities that the SG-TFT Technology has to offer: 1) Mixed signals, both analog and digital circuits are present in this display; 2) High voltage SG-TFTs (70V) to control the QR-LPD E-Paper material; 3) Flexible Electronics, the possibility to fabricate on plastic substrate and make a fully flexible E-Paper Display, including the integrated electronics.

A Flexible Electronic Paper with Integrated Display Driver using Single Grain TFT Technology

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THESIS

submitted in partial fulfillment of the
requirements for the degree of

MASTER OF SCIENCE

in

COMPUTER ENGINEERING

by

Wei Man Chim
born in Amsterdam, The Netherlands

Computer Engineering
Department of Electrical Engineering
Faculty of Electrical Engineering, Mathematics and Computer Science
Delft University of Technology

A Flexible Electronic Paper with Integrated Display Driver using Single Grain TFT Technology

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Laboratory : Computer Engineering
Codenumber : CE-MS-2009-01

Committee Members :

Advisor:	Dr. Ir. A. van Genderen, CE, TU Delft
Advisor:	Dr. R. Ishihara, ECTM, TU Delft
Chairperson:	Dr. K.L.M. Bertels , CE, TU Delft
Member:	Dr. J.S.S.M. Wong, CE, TU Delft

I would like to dedicate this thesis to my parents, may they rest in peace. Much love goes out to my brother Steven, for taking care of us in the absence of our parents.

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Acknowledgements

First of all, I would like to thank my supervisor Arjan van Genderen for guiding me through my Master Thesis. I want to thank him for taking the time to give me useful advice all along this project and for proofreading my paper and this thesis.

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I also want to express my gratitude to Alessandro Baiano, for his time and efforts put in the measurements of digital test circuits, the frustrations and the joyful moments. And of course I would like to express my thanks to Nitz Saputra, for the fruitful discussions on the analog electronics.

As for the Super E-Paper Bachelor group, Michel Verhulst, Rico van Dongen, Sander Geursen, Daniel Petrarca and Vladimir Shirokov, I had a great time being the technical assistant. Thank you all for that wonderful barbecue, price money well spend in my opinion.

Last, but not least, I would like to give my special thanks to Stephan Wong and Koen Bertels for being part of my graduation committee.

Wei Man Chim
Delft, The Netherlands
January 27, 2009

1 Introduction

Since the first transistor was turned on that historic day, December 23rd 1947, the researchers of Bell Laboratories would not have any idea what role the transistor will play after this historic event. After the point-contact transistor, many types of transistors were invented. Among these are Bipolar, JFET, MOSFET, TFT etc. The work described in this thesis is based on the new Single Grain Thin-Film Transistor (SG-TFT) made with μ-Czochralski process, a special type of high performance TFT. An Electronic Paper display with integrated Display Drivers will be build using the SG-TFTs to show the possibilities with this technology.

This introduction chapter is organized as follows: Section 1.1 presents the motivation behind the presented work. Subsequently, project goals are identified in Section 1.2. Section 1.3 lists the persons involved with the development of the E-Paper Display. Section 1.4 concludes this introduction chapter with an overview of this thesis' organization.

1.1 Motivation

After the introduction of the transistor, electronic devices rapidly became part of the lives for most people all over the world. Nowadays, it is for them unimaginable to picture a world, without the ease and comforts these electronic devices offer them. The possibilities seem endless with electronics, and with the SG-TFT technology even flexible electronics are possible.

With the use of μ-Czochralski Single Grain Thin-Film Transistor Technology [32], it is possible to fabricate TFTs at relative low-temperatures (<350°) with near SOI performances [27]. These SG-TFTs can be used for building analog, RF and digital circuits. With this technology it is possible to fabricate these circuits on flexible substrate for flexible electronics and it is possible to stack these SG-TFT circuits on top of each other for 3D integration of ICs [10]. Until now, only analog and RF [11] circuits are build and tested using these SG-TFTs. Digital circuits are not realized yet with this technology.

We want to build a flexible Electronic Paper (E-Paper) Display with the μ-Czochralski SG-TFT technology. E-Paper is a display type that has a paper-like appearance (paper white, wide view angle) and can retain an image without power. The Display Driver will control a Quick-Response Liquid Power Display (QR-LPD) [17] as E-Paper material. A mockup of our E-Paper Display prototype can be seen in Figure 1.1. Although this is a mockup, the integrated Display Drivers can be seen on the edges. With this E-Paper Display we want to showcase the possibilities and versatility of the SG-TFT technology. The E-Paper Display Driver will be made solely using the SG transistors. Both analog and digital circuits are required for the Display Driver. A large part of the analog circuit needs to be designed for high voltages up to 70V, this is

required by the E-Paper material and a specially designed high voltage SG-TFT is used. For digital circuits, an automated design flow using a Standard Cell Library is essential for designing more complex digital circuits. Using this Standard Cell Library it is possible to design big and more complex devices like processors. It starts with a hardware description in HDL (Hardware Description Language), that then gets translated in logic gates based on the SG-TFT Standard Cell Library [36].

The versatility of the SG Technology showcased by the E-Paper Display is listed here:

- Mixed Signal: both Analog and Digital Circuits
- Standard Cell Library for Digital Circuits
- High Voltage SG-TFT (up to 70V)
- Flexible Electronics

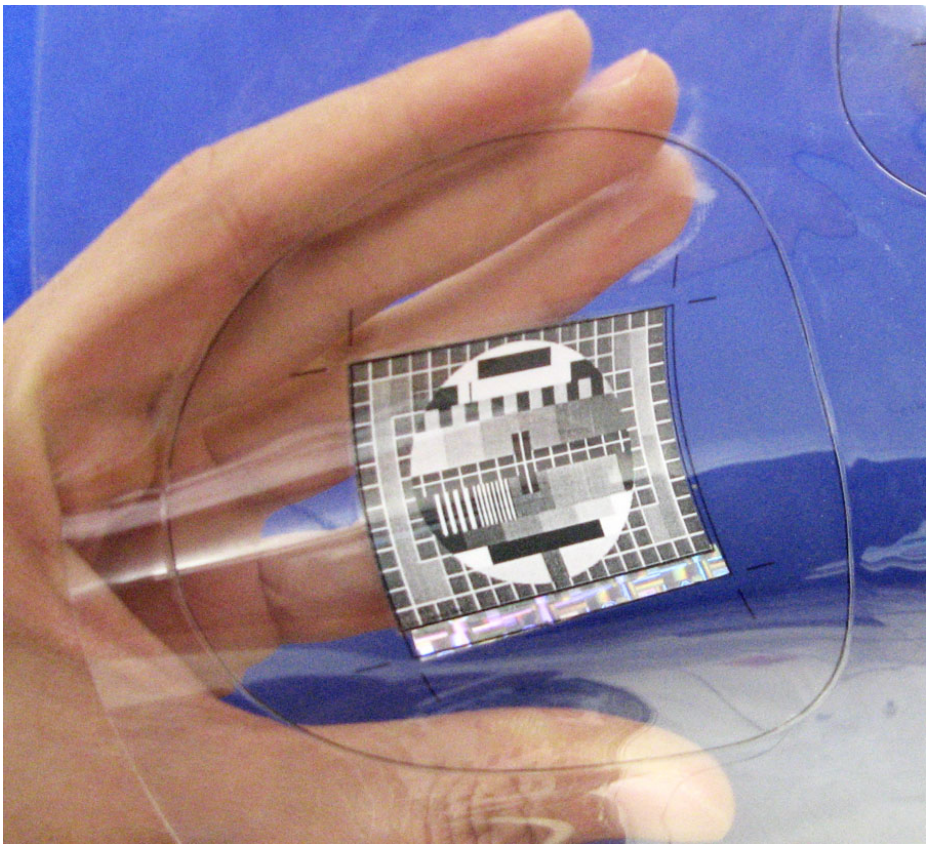

Figure 1.1: A mockup of how the E-Paper Display will look like.

1.2 Project Goals

At the start of this project the main project goal was clear, to build an E-Paper Display with integrated Display Drivers using the Single Grain Transistors. To reach this goal, the project can be divided in the following different stages:

1. First do the research and define what is needed and required by the QR-LPD E-Paper material. Using this information, define a organization for the Display Driver while keeping in mind that the implementation is done using the SG-TFT technology.

2. Second, investigate how the functional blocks of the organization can be implemented. Make clear distinction between the different implementation domains: digital - analog, low voltage - high voltage. And implement these functional blocks.

3. Since we want to make a real E-Paper Display, the implemented functional blocks need to be realized in silicon. Requiring a layout stage, to place and route the different components.

4. Make an E-Paper Display prototype.

5. Testing and measurements on the prototype to improve the SG Technology and future E-Paper Displays with integrated Display Drivers.

6. Next to the Display Driver, some simulation and development tools need to be made. For development of E-Paper applications without the E-Paper Display.

1.3 Project Organization

Since this E-Paper Display is made as a collaborative project, this thesis will also cover the work of others to give a complete view of the E-Paper Display development. The involvement of the persons directly related to the E-Paper Display development are listed as follows:

Person	-	Responsible for
R. Ishihara	:	E-Paper project leader
A. van Genderen	:	SG Standard Cell Library
A. Baiano	:	SG-TFT pixel cell and High Voltage SG-TFT
N. Saputra	:	Analog Circuit Design
W.M. Chim	:	Analog and Digital Circuits

1.4 Thesis Organization

The thesis is organized as follows. The E-Paper Display that is being developed here is based on two technologies. The Single Grain TFT Technology developed at DIMES for the integrated electronics and the QR-LPD E-Paper material from Bridgestone. The technology inner workings and operational principles are explained in Chapter 2. Based on constraints and requirements of the two technologies, the E-Paper Display driving concepts are made, and presented in Chapter 3. Keeping in mind what the constraints and properties are of the QR-LPD E-Paper material, and how it is possible to construct a feasible E-Paper Display using the SG-TFT technology. From these driving concepts, a functional block diagram is made of the complete E-Paper Display. The implementations of the functional blocks in the block diagram are presented in Chapter 4 together with the E-Paper simulator for development of E-Paper applications. Chapter 5 is a discussion about the process of design and implementation regarding to the digital parts of the Display Driver. These digital components follow the automated design flow: Starting of as VHDL files (a hardware description language); They get synthesized and mapped on to logic gates of the Single Grain Standard Cell Library; The Netlist of gates then get placed and routed for a chip layout. A test chip is made with various test circuits, the digital test circuits are described in Chapter 6, together with the test results of these circuits. In Chapter 7 the current state of development is presented and what still is needed to be done. Together with the future design considerations when designing digital circuits with the SG technology and a practical example of how the E-Paper can be used. Finally, this thesis is summarized in Chapter 8 and concluded in Chapter 9.

2 The Technologies

The E-Paper Display that we are developing at the TU Delft is based on two technologies. The first is the μ-Czochralski Single Grain Thin-Film Transistor technology. This is used for the integrated electronics. The second is the Quick-Response Liquid Powder Display technology developed by Bridgestone, the E-Paper material for our E-Paper Display.

This chapter is organized in two sections, explaining the SG-TFT Technology (Section 2.1) and the QR-LPD E-Paper material (Section 2.2). The subsections of Section 2.1 will cover the following points: The SG-TFT process steps (Subsection 2.1.1), performance of SG-TFTs (Subsection 2.1.2) and the Standard Cell Library based on the SG-TFT technology for designing logic using EDA tools (Subsection 2.1.3). For Section 2.2 we have the following two subsections: The Liquid-Powder with its properties explained (Subsection 2.2.1) and the structure of the QR-LPD cells forming the E-Paper pixels (Subsection 2.2.2).

2.1 μ-Czochralski Single Grain Thin-Film Transistor

Transistors can be made out of different materials. Looking only at silicon transistors, it is possible to make them out amorphous silicon (a-Si), poly-crystalline silicon (p-Si) and single-crystalline silicon (c-Si) [13]. The difference is in the way how the silicon atoms are organized and are characterized by size of the ordered regions within the material. An ordered region is where the silicon atoms have regular geometric arrangement or periodicity. a-Si lacks such ordered regions, while p-Si have ordered regions, but vary in size and orientation with respect to one other. These ordered regions are called grains and separated from each other by grain boundaries. c-Si has a regular geometric periodicity throughout the entire material, all with the same grain (single grain). The c-Si electrical properties are superior compared to a-Si and p-Si, since c-Si lacks the grain boundaries that degrade the electrical characteristics, making it a suitable material for high performance transistors.

The Thin-Film Transistor (TFT) is a type of MOS transistor where the active semiconductor material (silicon) is deposited as a thin-film over a supporting substrate. The substrate can be a large panel, for example glass, for making large LCD screens. Since the silicon is deposited, the type of silicon is limited to a-Si or p-Si type. In contrast, regular type MOS transistors are made from c-Si wafers. These wafers are grown from a single seed (by Czochralski process for example), and have regular geometric periodicity throughout the entire wafer.

The μ-Czochralski Single Grain Thin-Film Transistor (SG-TFT) technology is a method to produce high performance transistors out of amorphous silicon by Excimer-laser crystallization. These SG-TFTs out perform the a-Si and p-Si TFTs, and yet the electrical performance is comparable to c-Si transistors [12]. SG-TFT technology has

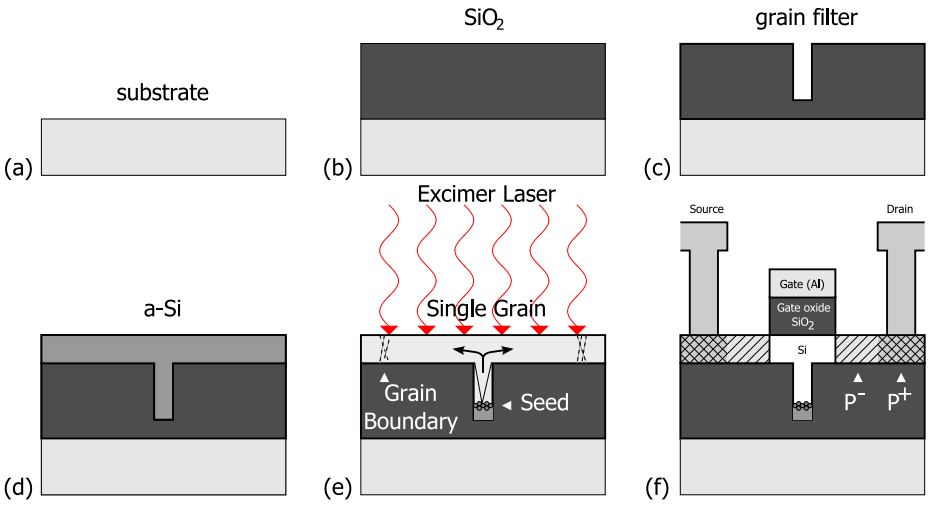

Figure 2.1: The SG-TFT process: From the applied SiO_2 (b) on top of the substrate (a), a grain filter (c) is made. The a-Si (d) deposited and melted by an Excimer laser where a Single Grain is formed (e). On this Single Grain a PMOS Thin-Film Transistor is made (f).

the advantage of high performance SG transistors that can be manufactured on a panel substrate, for example glass or plastic, with the possibility to use these transistors in analog, digital and RF circuits.

2.1.1 SG TFT Process Steps

The first steps for making SG-TFTs is depicted in Figure 2.1. It starts with the creation of so called *single grains*, small islands of single grain silicon for making reliable TFTs on it. The process of making one *single grain* is illustrated in Figure 2.1. We start of with a substrate, were SiO_2 is deposited on top. Small cavities are patterned in the SiO_2, these cavities are called the *grain filters*. A layer of a-Si is deposited on top, covering everything and filling up the cavities. An Excimer laser is used to crystallize the silicon: the laser partially melts the a-Si, the bottom of the cavities stays unmelted and forms the seed for the crystallization of the upper silicon. The *grain filter* ensures that the crystallization is grown from a single grain. The result can be seen in Figure 2.3, where the *single grains* form a grid and the *grain filters* can be found in the middle of each square shaped *single grain*. Inside these grains, source and drains are made by implanting with phosphorus and boron for NMOS SG-TFT and PMOS SG-TFT respectively. Ideally, these islands are of a single grain. Although planar defects are present inside the *single grain*, it has been reported that these defects are less active than random grain boundaries [19] [20]. These planar defects often grown out the grain filter radially [28] and can be seen in Figure 2.3. It is possible to place the transistor channel parallel to these planar defects so that the current flow does not cross these defects, resulting in a higher mobility for better transistors. In Figure 2.3, the transistor placed in position X has the highest field effect mobility.

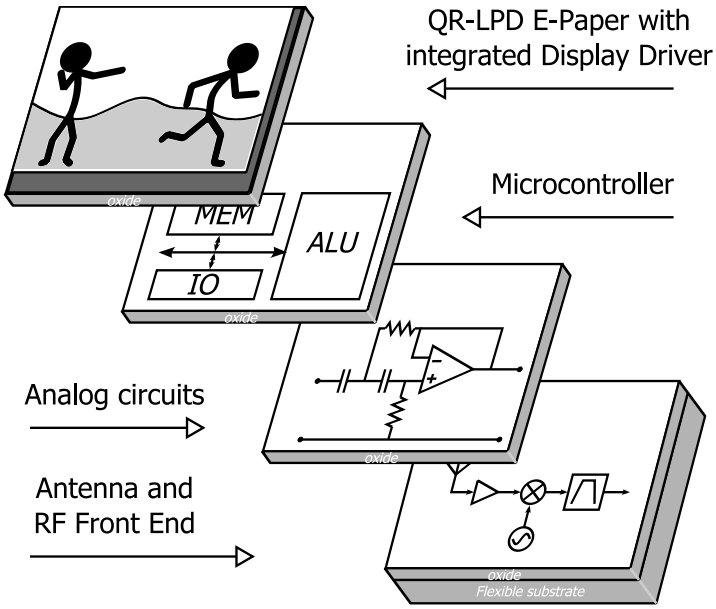

Figure 2.2: 3D circuits integration concept.

All the fabrication steps can be done at relatively low temperatures (<350°). This makes it possible to fabricate SG-TFT on cost-effective plastic substrate for flexible electronics. In our case a flexible display with integrated display drivers. Another advantage of this technology is that it is possible to stack SG-TFTs on top of each other. A concept of this can be seen in Figure 2.2, each layer is used for a different purpose; display, digital, analog and RF electronics.

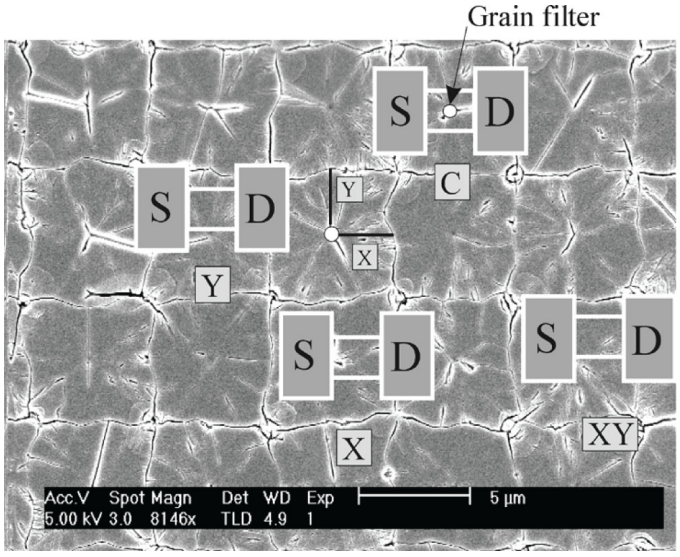

Figure 2.3: SEM image of a grid of grains formed by the μ-Czochralski process. Different TFT channel orientation with respect to the grain filter with positions X, Y, XY, C.

2.1.2 SG Thin-Film Transistor performance

The SG Thin-Film Transistor have better electrical characteristics compared to the a-Si and p-Si transistors. Near SOI* performance have been reported [27], with high field effect mobility (μ_{FE}) of average 600 cm^2/Vs and 270 cm^2/Vs for n-channel and p-channel respectively. In Table 2.1 the performance parameters the mobility (μ_{FE}), subthreshold swing (V/dec), threshold voltage (V) and off-current (A) are seen for both NMOS and PMOS SG-TFTs [12].

Field Effect Mobility
One of the most important parameters to characterize TFTs is the Field Effect Mobility (μ_{FE}). The mobility relates the carrier (electron or hole) velocity to the electric field (expressed in μ_{FE}).

Subthreshold Swing
The subthreshold swing slope factor S describes the quality of the turn-on characteristics. The slope factor S defines the amount of gate voltage needed to change to drain current by a factor of 10 (expressed in V/dec). For digital applications, an ideal switch-like behavior is desired. An ideal transistor has a S parameter of 60 mV/dec.

Threshold Voltage
The gate-source voltage at wich conduction appears in the channel is called the threshold voltages. A low threshold voltage is desired, so that the TFT operational regime is within a reasonal voltage range.

Off-Current
The off-current is the minimum current in the transfer characteristics of the TFT. It is the current that still is present when the TFT is off.

Table 2.1: SG-TFT Performance Parameters.

SG-TFT Device	**Mobility μ_{FE} (cm^2/Vs)**	**Sub-threshold Swing (V/dec)**	**Threshold voltage (V)**	**I_{off}(A)**
NMOS	600	0.2	0.5	$1.3 \cdot 10^{-13}$
PMOS	270	0.13	-2.3	$1 \cdot 10^{-14}$

2.1.3 Standard Cell Library for Digital Logic

It is possible to design digital circuits manually, connecting transistors in CMOS pairs to make digital circuits. When the circuits gets larger, the manual labor grows dramatically, and mistakes are easily made. To make the SG-TFT technology useful for future large

*Silicon On Insulator technology, used to reduce parasitic device capacitance and thereby improve transistor performance.

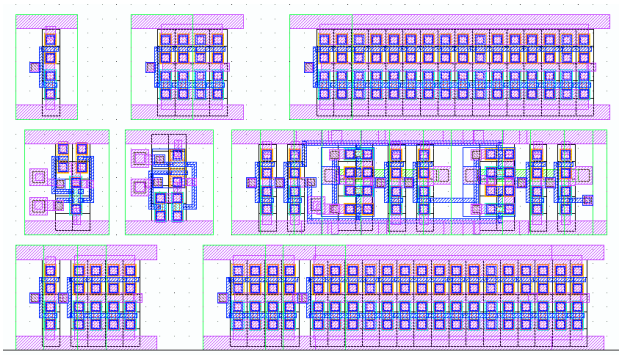

Figure 2.4: Layout of cells in the Standard Cell Library. Starting from top left: inv, inv4, inv16, nand2, nor2, dff, buf4 and buf16.

scale digital circuits, an automated design design flow is needed. A SG Standard Cell Library is made based on previous work [36], this library consists of a number of standard logic cells. With this Standard Cell Library it is possible to map digital circuits on to the logic cells based on SG-TFTs using EDA tools.

Table 2.2: The Standard Cells Library.

Type of cell	**Cell name**	**Cell description**
Inverters	inv inv4 inv16	Inverters with different sizes 1, 4 and 16.
NAND Gate	nand2	Two ports NAND Gate
NOR Gate	nor2	Two ports NOR Gate
Flip-Flop	dff	D Type Flip-Flop
Buffers	buf4 buf16	Buffer with sizes 4 and 16.

The library currently consists only of a few standard cells. This is because the SG-TFT technology is still under development, and adjustments to improvements the technology are expected in the future. This means that the standard cells will need to be modified as well, and by limiting the number of standard cells, the amount of work needed to update the library is reduced. Once the technology is matured enough, a more complete library can be made with more standards cells, for a better and optimized logic mapping. The currently library consists of inverters, NAND gate, NOR gate, flip-flop and buffers. The complete list of cells can be seen in Table 2.2.

2.1.4 High Voltage Transistors

The E-Paper material requires a high driving voltage of 70V (see next Section 2.2). This high voltage will cause breakdown and destroy the normal SG-TFTs. Compared to a normal transistor, the specifically designed high voltage transitor has a thicker gate oxide and a change in doping profile(see Figure 2.5). By introducing lighter doped regions, the peak electric field in the space charge region is reduced and the breakdown and hot electron effects are minimized. Besides the obvious additional process steps, LDD devices have another disadvantage, the increase in drain resistance. However, the result is a transistor with LDD profile will show significant performance improvement under high voltages. In the cross section it can be seen that the source terminal is also in a lightly doped region. This does not improve transistor performance, but reduces fabrication complexity.

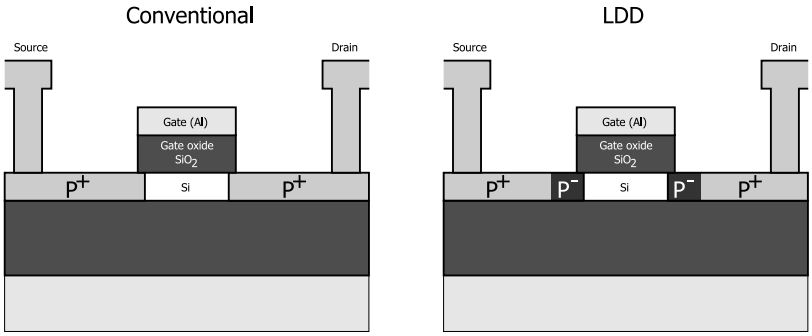

Figure 2.5: Left: The Conventional structure; Right: The Lightly Doped Drain (LDD) structure;

Because the low voltage and high voltage transistors are made with the same process some design considerations had to be made. It is possible to make gate-oxides with two different thicknesses in the same process (30nm and 300nm for low voltage and high voltage respectively). In order to reduce cost and manufacturing complexity, all the transistors are LDD type TFTs, even though this is not beneficial for the low voltage transistors.

2.2 Quick-Response Liquid Powder Display

With the introduction of the personal computer in office environment, some people believed that the PC will make paper redundant for routine tasks such as record-keeping and bookkeeping, creating a paperless office, the office of the future. Contrary to this paperless office vision, the introduction of the computer has led to an increase of paper usage. Due to the preference of many people who prefer reading e-mails and documents off paper rather than reading off the computer screen. With sufficient lighting, the strain on the eyes is minimal when reading off paper, while reading off the computer screens can get uncomfortable for extended periods of time.

An ideal Electronic Paper (E-Paper) display has a paper-like appearance with all the advantages of paper, when reading off of it. The Japanese company Bridgestone

Figure 2.6: A QR-LPD Display.

has developed a new *Electric Liquid-Powder* suitable for making E-Paper Displays, the QR-LPD (Quick-Response Liquid Powder Display). The Liquid-Power is a high-fluidity material, a combination of powder and liquid properties and is highly sensitive to electric fields. QR-LPD has a paper like appearance and has shown excellent image stability, quick response, high resolution, clear threshold characteristics and low power consumption [39]. And with the simple display structure a cost effective display can be made, making QR-LPD and ideal technology for electronic paper displays.

The Subsection 2.2.1 will describe the properties of the Liquid-Powder and what forces the particles are subjected to, and in Subsection 2.2.2 the structure of the QR-LPD is explained.

2.2.1 The Liquid-Powder

The new developed material by Bridgestone behaves like a liquid despite its powder form. Two types of powders were developed: a white colored powder with a negative charge, and a black colored powder with a positive charge. The two powders are attracted to each and make a gray mass. The Liquid-Powder is moved when subjected to an electric field, white particles are attracted to the positive electrode and black particles are drawn to the negative electrode.

The forces that work on these particles are summed up in Figure 2.7, with the two different colored and different charged powders. The charge is intrinsic to the particle itself, and does not require external friction to obtain this charge. The attractive force F_a is the force that attracts the positive and negative particles. This attractive force F_a consists of the Coulomb force F_q and the Van der Waals force F_v. At the surface of the electrode, the attractive force is similar but with an additional force: The image charge force, due to the polarization of the electrode by the charged particle. These attractive and repulsive forces between particles and electrodes make the QR-LPD bistable, and are able to retain an image on the display without power. When a voltage potential is put across the electrodes, the electric field E acts as a repulsive force to the pair of oppositely charged particles. The pair of particles will separate when the electric field force F_E is strong enough to overcome the attractive force F_a. The particles then travels

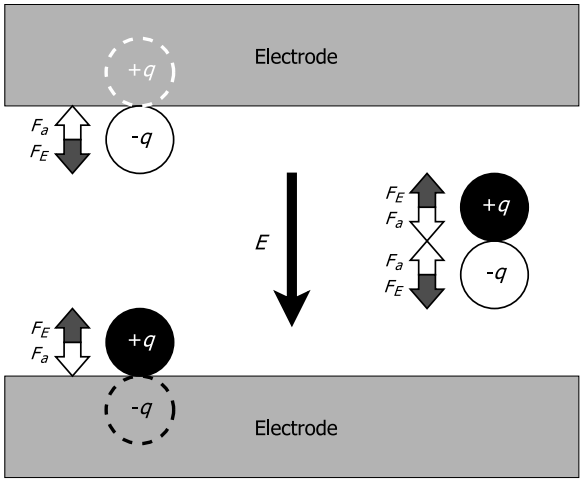

Figure 2.7: The forces that work upon the Liquid-Powder particles.

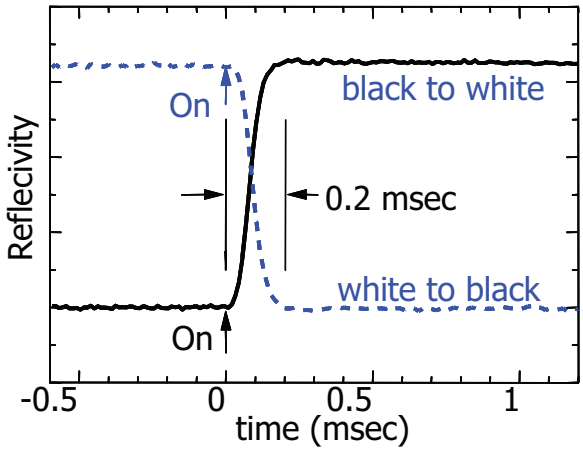

Figure 2.8: Graph showing the pixel reponse time of both white and black Liquid-Powder.

to the electrode of opposite charge with respect to the charge of the particle it self. The same principle holds for separating particles from electrode. The attractive force is represented by $F_a = F_q + F_v = k\ q^2/r^2 + F_v$. The electric field force is given by $F_E = qE$, where q is the charge of the particle. When particles travel from one electrode to the opposide one, the particls accelerate to high speeds. It has been reported that the particle transfer speed was over 11.11m/sec (∼40km/hour) [39]. This high speed transfer results in a fast pixel response of about 0.2 ms for both white tot black and black to white pixel transistion seen in Figure 2.8.

The bistable nature of the Liquid-Powder particles is observed in the hysteresis plot in Figure 2.9. The threshold voltage can be seen very clearly. Depending on the current state of the particles, the applied voltage can move the particles to a new state. The QR-LPD requires a relative high driving voltage of 70V, the threshold voltage to overcome the attractive force is about 35V. The voltage potentials between 35V and 70V is interesting

for gray-scale levels, it does not make any sense to have full control over 0V to 70V since everything below the threshold level will not have any effects on the Liquid-Powder.

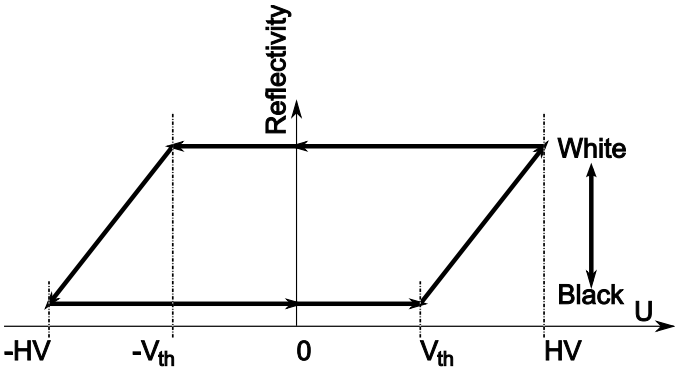

Figure 2.9: Hysteresis plot, reflectivity versus applied voltage. (HV stands for High Voltage and V_{th} for the Threshold Voltage.)

2.2.2 QR-LPD Structure

The structure of the QR-LPD is shown in Figure 2.10. In a single cell there are the two types of powders (negatively charged white powder and positively charged black powder) and plain air to fill the remaining space of the cell. Two electrodes on top and bottom generate an electric field. With this electric field the Liquid-Powder can be controlled. When applying a negative voltage over a cell, the top electrode will attract the black particles and the top of the cell will turn black. And when a positive voltage is applied to a cell, the white particles will move to the top electrode making the cell top white. The powder particles can move fast through the air within the cell, resulting in an ultra fast pixel response time of 0.2ms. With this simple cell structure a roll-to-roll manufacturing process is possible [24] for efficiently making inexpensive flexible QR-LPD.

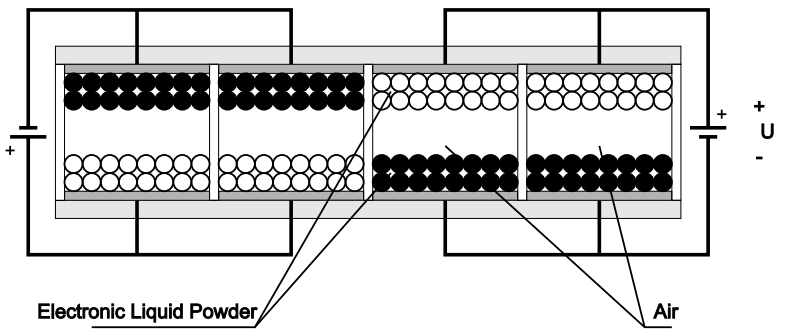

Figure 2.10: Simple structure of the QR-LPD display here showing four pixels cells.

2.3 Summary

Two technologies were discussed in this chapter, the μ-Czochralski Single Grain Thin-Film Transistor (SG-TFT) technology and the Quick-Response Liquid Powder Display (QR-LPD). By combining these two technologies, we want to make a Flexible E-Paper Display.

The SG-TFT technology is used to make high performance transistors out of a-Si (amorphous silicon) by Excimer-laser crystallization. The electrical performance of these SG-TFTs are comparable to single-crystal transistors. These TFTs can be used for analog, RF and digital circuits. All the fabrication steps can done at relatively low temperatures (<350°). This makes the SG-TFT Technology suitable for electronics on glass substrate or cost effective plastic substrate for flexible electronics. It is even possible to stack TFTs on top of each other, for making 3D chips. High electrical performances have been reported, with field effect mobility (μ_{FE}) of average 600 cm^2/Vs and 270 cm^2/Vs for n-channel and p-channel respectively. For digital circuits, a small Standard Cell Library is made with a few logic gates, buffers and a flip-flop. This library is used to design digital circuits according to an automated design flow. High voltage TFTs are also designed, capable of surviving voltages of up 70V. These transistors are needed to control the E-Paper material.

The QR-LPD developed by Bridgestone has a paper-white appearance with high contrast and high reflectivity, suited to be used for E-Paper Displays. The QR-LPD uses a new developed Liquid-Powder. This powder is electrical sensitive and combines the properties of both powder and liquid. The QR-LPD Display is build up out of cells that contains of a black and white Liquid-Powder mixture. These powders are of opposite charge, negatively charged white powder and positively charged black powder. By applying an electric field the Liquid-Powder can be controlled. The powder particles can move fast through the air within the cell, resulting in an ultra fast pixel response time of 0.2 ms. The QR-LPD requires a relative high driving voltage of 70V with a clear threshold voltage of 35V. The bistable nature of the Liquid-Powder makes the QR-LPD retain its image after writing and even when there is no power at all.

3 The Electronic Paper Display

Before designing anything, it is important to know what to design for, what the constraints and requirements are. This chapter will discuss the ways to control the E-Paper material given the constraints and properties of QR-LPD and knowing the limits of the technology. After this, some requirements or goals can be defined for the prototype display.

This chapter is organized as follows: In Section 3.1 the driving scheme is discussed for addressing the individual pixels in an efficient way. In Section 3.2 writing and erasing the E-Paper are discussed. How the SG-TFT electronics is connected to the QR-LPD material can be found in Section 3.3. The chosen specifications for interfacing the E-Paper display can be found in Section 3.4. Knowing how the QR-LPD material is controlled, some design goals are setup. The specifications can be found in Section 3.5.

3.1 Display Driving Scheme

The most straight forward way to control a plane of pixels is to control each pixel individually. This is of course not an efficient way to work, considering that each pixel will need its own set of separate wires. One way to control the pixels is to organize them in a matrix. Pixels can then be controlled at the borders of the plane and addressed by row and column lines. This is the most common way to address a display [9]. The number of wires required for a matrix organized display is now reduced to the sum of the number of rows and columns. This basic principle of controlling matrix organized display is depicted in Figure 3.1. A small matrix screen of 4 by 3 pixels is controlled by seven lines, four for the columns and three for the rows. The crossing of a column line with a row line will control the pixel on that position. Instead of writing each pixel one by one, it is faster and more practical to write a whole row at once. This is also seen in Figure 3.1 for a small 4×3 screen, first the pixel data is put on the column lines. Next is to select a row, when a row is activated, the pixel data will be transferred to the pixels on the activated row. The result is that one row of pixels is written with the corresponding pixel data. For writing the whole display, these steps are repeated for the remaining rows.

3.1.1 Passive or Active Matrix?

There are two common ways two address the pixels. Both methods can be used for the QR-LPD display. They are called Passive Matrix addressing and Active Matrix addressing. The situation depicted in Figure 3.1 can be considered to be passive matrix addressing. This is when the row and column lanes are directly used to control the pixels. In our display, the crossing of these lines will generate the required electrical field

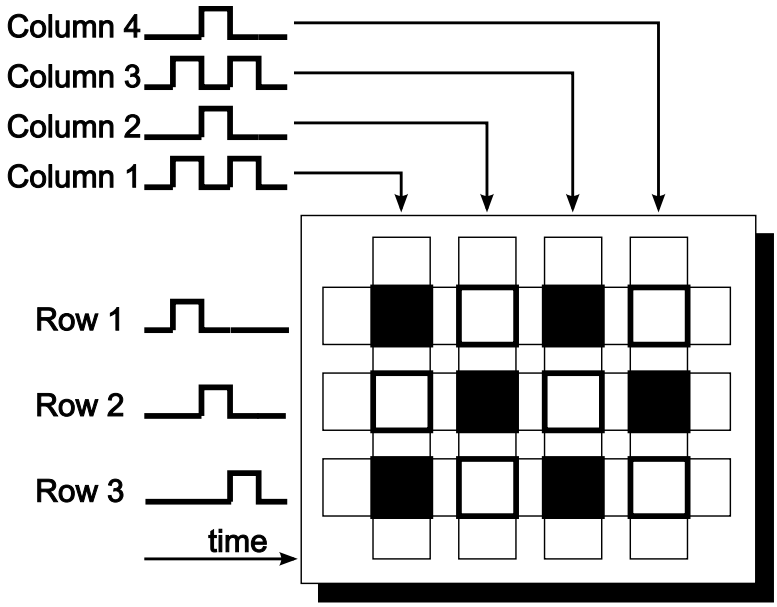

Figure 3.1: Basic driving matrix scheme.

for the Liquid-Powder to change state. An active matrix addressed display works with transistors as switches for each pixel. Usually the rows of the display are connected to the transistor gates, and the columns wires are connected to the drains of the corresponding transistors. Each transistor is than controlling its own pixel. This structure can be seen in Figure 3.2 with the transistor connected to its pixel. When writing a line, a single row is activated. The transistors on that row will pass the voltage from columns to the pixels, writing a line. The rest of the pixels stay unchanged, because the transistors of those lines are not activated. The structure seen in Figure 3.2 is commonly found in the literature. The schematics also show the pixel modeled as an capacitor, and storage capacitor. In Chapter 4 Section 4.3.1 the final design of the Active Matrix schematic is explained.

The major advantage of Passive Matrix addressing its simplicity. Only horizontal and vertical wires are needed, stretching across the whole screen. A drawback of passive matrix addressing is the crosstalk among wires. This is more problematic for other types of displays than compared to QR-LPD, because the Liquid-Powder has a high and clear threshold voltage. QR-LPD is suitable for Passive Matrix addressing. A Passive Matrix addressed QR-LPD will most likely have three voltage levels or more, for example HV (70V) MV (35V) and GND (0V). The middle voltage level MV is needed, so that pixels can stay unchanged when they should not be written or erased. Ensuring that only the pixels on the activated row can have a potential difference higher than the threshold voltage (>35V), the other pixels not on the activated row may have voltages anywhere between 0V to 35V. Anything that is below the threshold level will not effect the pixels, and this is desired since we want to write only one row. Passive Matrix addressing with two voltage levels is not sufficient, pixels on the rows that are not activated can still be influenced by the pixel data on the column lines.

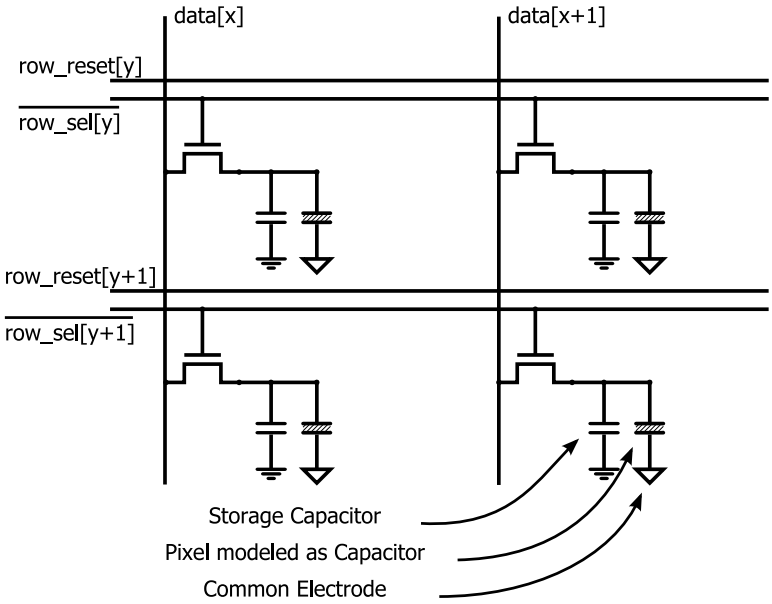

Figure 3.2: Basic Active Matrix schematic for four pixels.

Active Matrix addressing is not affected by cross talk. When writing a line, the transistors on that row ensure that the pixels are activated so that the column voltage will only go to these pixels. The other lines stay inactive, leaving the remaining display unchanged. Adding a storage capacitor per pixels, makes it more robust and less prone to noise. It is also possible to write an image faster compared to passive matrix addressing, it is not needed to wait the 0.2 ms per line for pixels to change state (see Figure 2.8 for the pixel response time). Therefore an higher frame rate is possible with Active Matrix addressing.

For our display we have decided to use the Active Matrix addressing, with the advantages of robustness and speed. The basic Active Matrix schematic of Figure 3.2 is modified: for each pixel a PMOS transistor is placed, activating the pixel when writing. This can be seen in a schematic shown in Figure 4.8 of Section 4. A NMOS transistor is also found in the schematics, this is for erasing the pixel. Write and Erased are explained in the upcoming section, Section 3.2.

3.2 Write and Erase

Writing and erasing pixels for the QR-LPD is done by applying an electric field. Depending on the current state of the pixel (e.g. black or white), an applied potential difference greater than threshold voltage will cause the Liquid-Powder to move and change the pixel state (to white or black for example).

There are two ways to change the polarity (see Figure 3.3). The first is by changing only one terminal with the second terminal grounded. This means that the terminal than needs to switch between positive and negative voltage, and in our case +70V and -70V. The second option is to change both terminals, eliminating the need of negative

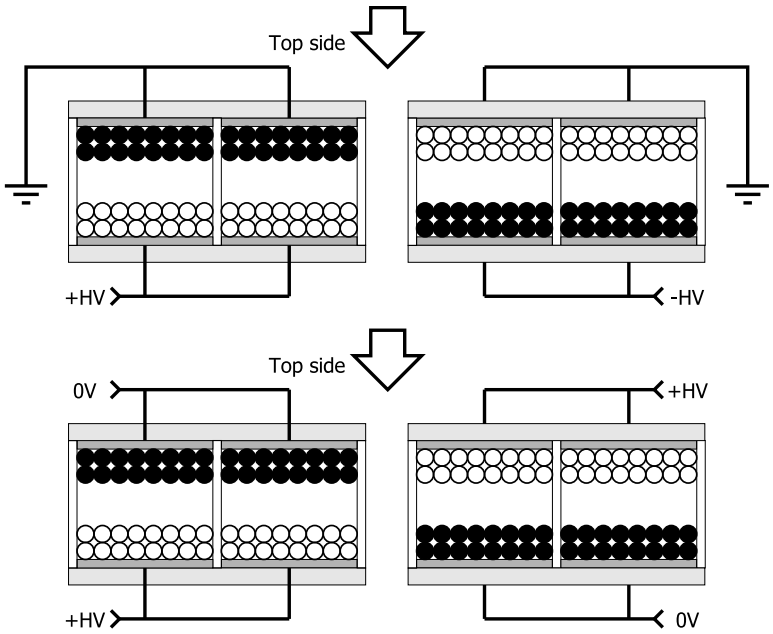

Figure 3.3: Top- One terminal drive: pixel electrode need both positive and negative voltages, the common electrode is grounded; Bottom- two terminal drive: only positive voltages needed for pixel electrode and common electrode.

voltages.

We have decided to go for the second option and control the potentials of the two terminals instead of dealing with negative voltages. The second option is more save, the voltage swing is at most 70V comparing to the 140V of the first option. By adding an additional transistor we can erase the pixel very easily. More on this can be read in section regarding the Active Matrix Backplane, Section 4.3.1.

3.2.1 Erase before Write

The QR-LPD can hold an image even when there is no power, this is due to the bi-stability properties of the Liquid-Powder. For most applications it is required to erase the screen before writing. You can compare this when using a black board for lectures. After the board is filled up, the professor needs to clean the board before continuing the lecture. A board that is overwritten multiple times without cleaning is useless for the students to take notes off. This also holds for the E-Paper Display. Although there are situations thinkable where it is not needed to erase before writing, but generally speaking, this is not the case.

We can define two use cases for our E-Paper: Picture mode and Movie mode. The first use case is when it is not required to update the images frequently. It can be used for displaying images (electronic photo frame), slide shows, e-book readers etc etc. The QR-LPD materials has ultra fast pixel response of 0.2 ms. We can use this property to display moving pictures with the E-Paper Display, hence Movie mode.

For the first use case, Picture mode, erase before writing is straight forward. Before

writing or updating a displayed image, the whole screen needs to be erased. This does not work well for Movie mode, when the frames (images) need to be updated multiple times per second. The display time of the first line will be longer than the display time of the last line. It is better to erase it line by line instead of the whole frame at once. This guarantees that all the lines get an equal amount of display time.

3.3 Structure of this E-Paper Display

The QR-LPD E-Paper material can be seen as polymer sheet with cells filled with black and white Liquid-Powder. The idea is to glue the E-Paper sheet on top of the Active Matrix Backplane to form an E-Paper Display. This can be seen in Figure 3.4 as a cross section of a single pixel. On the top of the E-Paper material, we have a common electrode. An ITO plane, both electrical conductive and optical transparent, called V_{common}. On the other side, at the bottom of each pixel, we have the other electrode connected to the source of the transistor corresponding to that pixel. With these two electrodes, it is now possible to apply a voltage across the QR-LPD cells, to generate an electric field to move the Liquid-Powder particles.

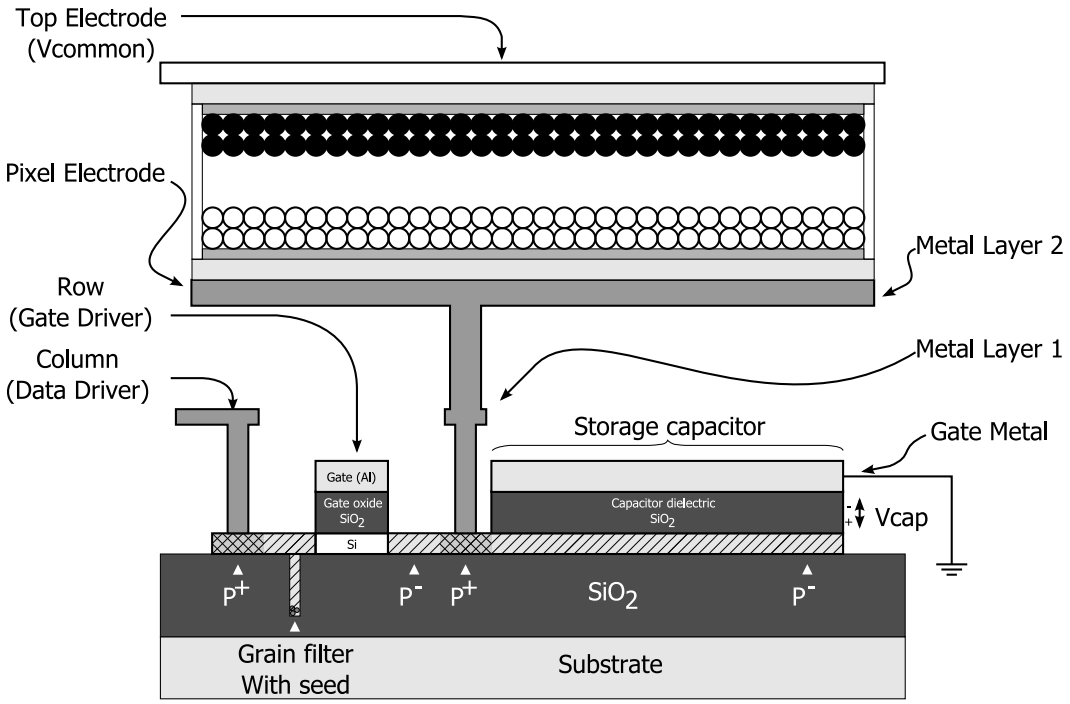

Figure 3.4: Cross section of a pixel with a SG PMOS transistor.

3.4 Display Interface Signals

A display is useless without a proper defined communication interface. The communication interface for our E-Paper Display is based on the VGA monitor signals [3]. This

is an easy way to format the data for the display requiring only two synchronization control signals: *hsync* and *vsync*. In Figure 3.5 the wave forms can be seen that are based on the VGA monitor signals. The horizontal synchronization signal *hsync* (Top of Figure 3.5) synchronizes the incoming data, denoting the start of a row and the validity of the data when *hsync* is high. A low signal is given between two consecutive rows, this is called the horizontal sync pulse. For frame synchronization, we have the vertical synchronization signal *vsync* (Bottom of Figure 3.5). Similar to *hsync*, *vsync* marks the start of the frame, and the validity of the rows when *vsync* is high. A low signals is also given between two consecutive frames, this is called the vertical sync pulse. The VGA monitor signals has so called *back porch* and *front porch* parts in the sync signals, this is where the data is invalid even though the synchronization signal is high. The *back porch* and *front porch* are not defined in the E-Paper Display interface nor it can be found in Figure 3.5. The length of the horizontal and vertical sync pulse is not fixed. The Display Driver should be capable of handling sync pulses of at least one clock cycle for *hsync* and one line for *vsync*. For a 320×240 E-Paper screen, the signal timing specifications for the Display Driver can be found in Table 3.1.

Table 3.1: E-Paper Signal Timing Specifications.

Row Timing	
Pixel Data	320 clock cycles
hsync pulse width	> 1 clock cycle
Total row time	*hsync* pulse + 320 clock cycles
Frame Timing	
Lines	240 lines
vsync pulse width	> 1 line
Total frame time	*vsync* pulse + 240 lines

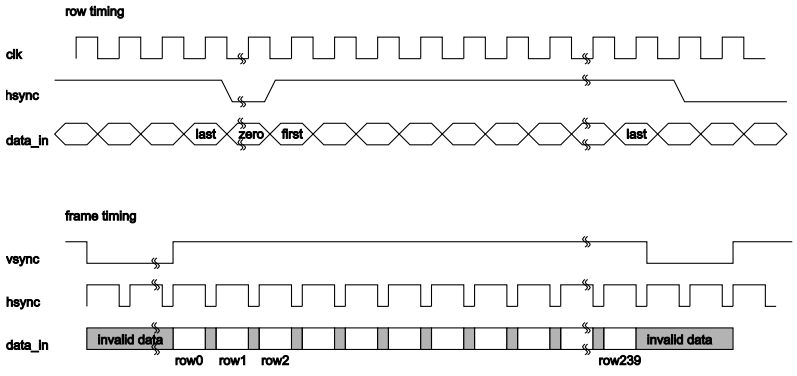

Figure 3.5: top: Horizontal timing for a single row; bottom: Vertical timing for whole frame.

3.5 Specifications of our E-Paper Display

Knowing the different aspects of the technologies we want to use and having a general idea of how an QR-LPD display can be constructed, we can compile a list of design goals for the prototype QR-LPD E-Paper Display with the integrated SG-TFT Display Drivers. The specifications are summed up in Table 3.2.

We want to design a monochrome E-Paper Display with the screen format of 320×240 pixels (QVGA). Each pixel will have 64 gray-scale levels (6bits) and will be 150×150μm big (about 170 pixels per inch). The viewable screen size will be 4.80×3.60cm, a screen diagonal of 6.0cm (about 2.3inch). Our aim is to reach 25 frames per second, making it possible to view animations fluently. With the given number of pixels and the desired number of frames, we can determine the minimal operating speed. The number of pixels per frame multiplied with the frames per second results in minimal clock of 1.92 MHz. Why minimal clock? Because the sync pulses are not taken in to account. We can say that the system clock frequency will be at least 2 MHz.

For moving the Liquid-Powder particles, a high voltage of about 70V is required. To design all the electronics for 70V is not practical, the high voltage SG-TFTs are not as suited as the normal SG-TFTs for logic circuitry. It is better to design the digital part of the display driver using low voltage gates, and use high voltage electronics to drive the pixels. So there is a separation in driving electronics, low voltage and high voltage.

Table 3.2: Desired E-Paper Specifications.

Display Specifications	
Pixel pitch	150 μm
Pixels Per Inch	170 ppi
Screen format	320×240 QVGA
Screen size	4.80×3.60 cm
Screen diagonal	6.0 cm or 2.3 inch
Gray-scale levels	64 levels 6 bits
Frame rate	25 fps
Clock frequency	2 MHz
Logic voltage	5V
Driving voltage	70V

3.6 Conclusions

This chapter discussed a way to control the E-Paper material given the constraints and properties of QR-LPD and knowing the limits of the SG-TFT technology. The concepts presented in this chapter form the bases for the implementation of the Display components.

Although QR-LPD is suited to be controlled with a Passive Matrix, an Active Matrix addressing is chosen. The Display Driver together with the Active Matrix Backplane will be made using the SG-TFT technology. With the advantage that the display will be less prone to noise and the possibility to write faster, compared to Passive Matrix, for higher frame rates. By controlling the E-Paper with the SG-TFT technology, it will be a nice demo platform to showcase the possibilities with this technology. The possibilities with a bistable screen requires extra care for writing and erasing. Two use cases are defined, for viewing still images: Picture Mode; and for viewing animation and videos: Movie Mode. An Erase before Write scheme is defined for the Movie Mode, to make sure that pixels are cleared and erased before rewriting them. The structure of the E-Paper Display is seen in Figure 3.4. The QR-LPD material will be glued on top of the Active Matrix Backplane. The Display Interface is based on the VGA timing signals, but not compatible. The interface is synchronized with two synchronization signals, horizontal *hsync* and vertical *vsync* similar to VGA. The Display Interface Timing Specifications are given in Table 3.1. And finally, the desired E-Paper Specifications are defined in Table 3.2.

Implementation of the Electronics

4

In the previous chapter, Chapter 3, we have seen how QR-LPD can be used to construct an E-Paper Display. With this as a starting point, we will further develop the basic concepts in to a feasible E-Paper implementation. Because the Liquid-Powder requires a high driving voltage, we have split the Display Driver in to two domains, the low voltage for digital circuits and high voltage for driving the QR-LPD.

This chapter will cover how the integrated Display Driver is organized, in Section 4.1. Since the Display Driver works with two voltage domains, there is a section devoted to the low voltage components (Section 4.2) and a section devoted to high voltage components (Section 4.3). The following low voltage components will be covered: The Display Driver (Subsection 4.2.1) with subcomponents Gate Driver, Data Driver and Timing Control; Pattern Generator for running a build in test (Subsection 4.2.2); Ring Oscillator (Subsection 4.2.3); Buffers (Subsection 4.2.4). Section 4.3 will discuss the following high voltage components: Active Matrix (Subsection 4.3.1); High Voltage Level Shifters (Subsection 4.3.2); Digital to Analog Converters (Subsection 4.3.3);. Two types of simulators are presented in Section 4.4, for testing, verification and development purposes.

4.1 Display Organization

The design for the Display Driver is pretty straight forward. First we have the Active Matrix Backplane. This matrix has horizontal and vertical lines (wires) for the rows and columns. For controlling the rows and columns we have the Gate Driver and Data Driver respectively. Both drivers operate at low voltage. For interfacing the low voltage Gate Driver with the display rows, a High Voltage Level Shifter is used. And for interfacing the low voltage Data Driver with the display columns, a Digital to Analog converter is used. How these components are organized can also be seen in the block diagram of Figure 4.1. It can also be seen that the Timing Control is controlling the Gate Driver and the Data Driver. The Timing Control will control those drivers accordingly, using the horizontal and vertical synchronization control signals. All these blocks form the electronics for driving the QR-LPD E-Paper.

In the block diagram we can see other blocks in dashed lines. We can expect such components in the future, integrated together with the components of the Display Driver. This could lead to smart flexible E-Paper devices for example.

For testing the display, we have designed a test pattern generator. Although this is not illustrated as a block, it would be placed where the dashed components are. The idea is to integrate this component together with the Display Driver for a build in self test. Just to confirm that everything is working accordingly and that we have a test pattern on the display.

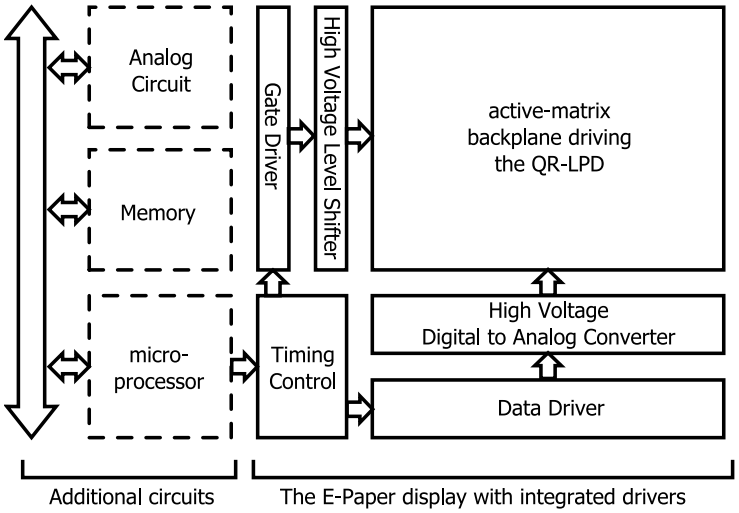

Figure 4.1: A block diagram of the E-Paper Display with integrated drivers and additional circuits.

4.2 Low Voltage Components

This section is devoted to the low voltage components of the E-Paper Display. These components are all digital circuits and designed with the SG Standard Cell Library in mind (see Chapter 5 for more details on the process). The SG Standard Cell Library includes the following gates: inverters (inv; inv4; inv16), two port NAND (nand2), two port NOR (nor2), D type Flip-Flop (dff) and buffers (buf4; buf16). With these basic gates it is possible to implement all kinds of digital circuits.

In the upcoming subsections we will discuss the implementation of the following components in more detail: The Display Driver (Subsection 4.2.1) with subcomponents Gate Driver, Data Driver and Timing Control; Pattern Generator for a build in test (Subsection 4.2.2); Ring Oscillator (Subsection 4.2.3); Buffers (Subsection 4.2.4).

4.2.1 Display Driver

The Display Driver is the grouping of the subcomponents Gate Driver, Data Driver and Timing Control. Together they form the low voltage components involved in controlling the QR-LPD E-Paper.

It can be considered that the Gate Driver and the Data Driver are the muscles and the Timing Control is the brains. Both of the drivers are build up structurally, reducing the drivers to Unit drivers, responsible for driving one row or one column. Gate Unit and Data Unit are then copied and linked 240 and 320 times respectively to form the complete Gate Driver and Data Driver.

To work more efficiently, the time spend on shifting incoming image data is overlapped with the write time of a row, resulting in a small two stage pipeline is. For example, we write a picture on to the E-Paper Display. The data of the first row is send to the display and is then stored and buffered. Once all the pixel data of the first row is received, the

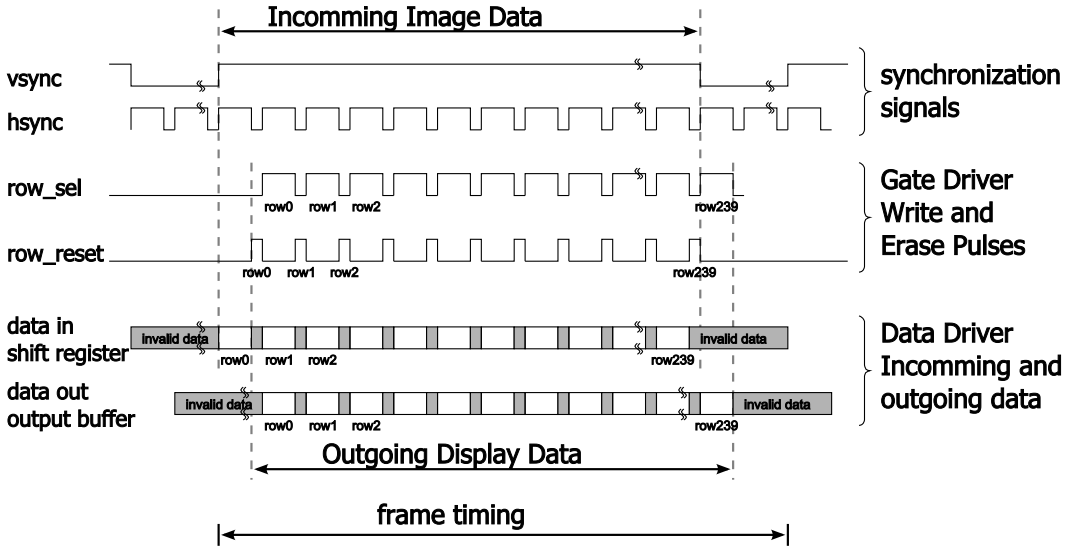

Figure 4.2: Movie Mode frame timing where the incoming image data is buffered before sending to the display. At the same time the upcoming row is erased before it gets written.

first row will be written on the display. During this write time of the first row, we can start storing and buffering the pixel data of the second row. This can be seen back in Figure 4.2, where the outgoing display data is delayed compared with the incoming image data. The write time and erase time are both seen in this figure as pulses of signal *row_sel* and signal *row_reset* respectively. This is deducted from the *hsync*, a logic 1 for the write time and a logic 0 for the erase time. It can be seen that Erase before Write is applied here, *row0* is erased before writting. We can see that the erase pulse is shorter compared to the write pulse, this is completely depending the *hsync* pulse time. It is possible to widen the erase pulse by widening the *hsync* pulse.

4.2.1.1 Gate Driver

The main task of a Gate Driver is to activate a single row of interest, and that row will be written. The selection of a row is implemented with a serial to parallel shift register that is 240 bits long (we call this the *write vector*). The serial output is fed back to the input for continues writing. A logic 1 travels through the shift registers, while the other the other bits are zeros. The result is that we have maximum one line active out of the total 240 lines. The Gate Driver activates one line after the other, scanning the whole frame.

Apart from writing, we also need to erase. Since there are two use cases, Movie mode and Picture mode, two erase modes are implemented. We have implemented a *Programmable Erase Vector* for the Movie mode, programmable to have more flexibility for the correct erase time. It now is possible to decide how many lines before the *write vector* we want to start erasing lines, and how many lines we want to erase at the same time. Erasing lines multiple times, has the advantage to keep the erase time short.

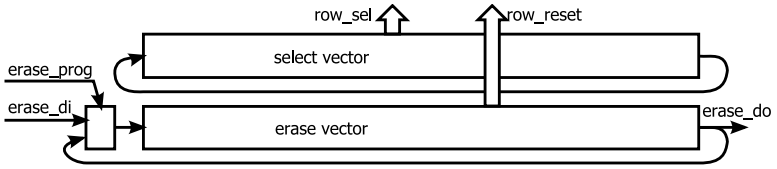

Figure 4.3: Block diagram of the Gate Driver.

The combined erase time of the multiple erases ensures that the row is erased enough and erased properly before writing. Similar to the *write vector*, the *erase vector* is implemented with a shift register. Instead of directly feeding back the serial out of the shift register, we add an option to choose to reprogram the *erase vector* with an external input. By default the *erase vector* erases the upcomming row before this gets written.

For the Picture mode, it is easier to erase the whole display prior to writing the picture. Because we have included a dedicated reset NMOS transistor for every pixel, erasing the whole frame is quite easy. Simply by activate all the row erase lines, will clear the whole screen.

In Figure 4.3 the block diagram can be seen. It consists of two shift registers, *write vector* and *erase vector*. The *erase vector* can be reprogrammed, so that is possible customize the erase policy. Together with some control signals (for Resetting; Shift enable; Movie/Picture Mode Select; Output Enable;) the Gate Driver is complete.

4.2.1.2 Data Driver

The Data Driver takes care of the incoming image data, collects and forward the correct digital data to the DACs that are connected to the columns, so that the correct voltage levels are on those columns. The Data Driver is build out of a shift register, and a output register. The shift register is big a serial to parallel shift register, shifting data words of 6 bits each clock cycle. It is able to store 320 words, corresponding the same number of columns. Besides this shift register, an output register is also included. This enables the display to output the voltages on the columns and at the same time, shift in the data for the next line.

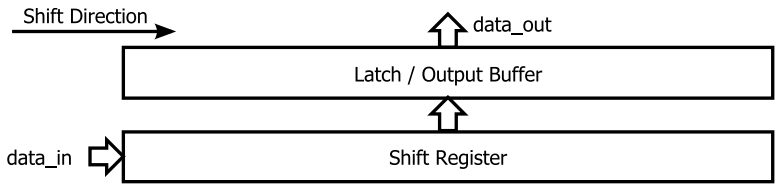

Figure 4.4: Block diagram of the Data Driver.

In Figure 4.4 we can see the block diagram of the Data Driver. Image data is shifted in, pixel per time, 6 bits per clock cycle. Once all pixels of a row are shifted in, it will be latched to the output buffer. Making it possible to write a row, and shift in the next row at the same time. Together with some control signals (for Resetting; Latch Enable; Output Enable;) the Data Driver is complete.

4.2.1.3 Timing Control

The Timing Control controls the Gate Driver and the Data Driver using the synchronization control signals, *hsync* and *vsync*. With these incoming synchronization control signals, the finite state machine tells the Gate Driver whether to write or erase, when to write or erase and when the Gate Driver should select the next line. The Timing Control also controls the Latch Enable and Output Enable of the Data Driver. Ensuring the values in the latch register are correct, and outputting these values at the correct moment.

The Timing Control also controls the electrode V_{common}. V_{common} is the common electrode seen in the Active Matrix schematic in Figure 4.8, it is the top electrode of Figure 4.9, an ITO plane on top of the QR-LPD E-Paper material that is both transparant and electric conductive. This common electrode is shared with all the other pixels. The applied voltage on a pixel is between the individual pixel electrode and V_{common}. Depending on whether it is needed to Write or Erase, the voltage on V_{common} will be 0V or 70V respectively (see Section 4.3.1 for details).

4.2.2 Pattern Generator

A (E-Paper) Display by itself is useless. It needs an image input in order for it to do something, to display something. This input can be anything, from movies to photos, from video games to live TV. Of course we can connect these input sources externally. We thought it might be good to have a test Pattern Generator implemented in the Display next to the Display Driver, so that the display can be tested and checked for correct operation by just looking at the displayed output.

We have decided to make a simple Pattern Generator. This Pattern Generator will give the correct horizontal and vertical synchronization signals, together with the 6 bits of data for filling up the display with a test pattern. The Pattern Generator is split up in two subcomponents, *patt_core* and *patt_mp*.

The synchronization control signals are generated in *patt_core*, using a horizontal and a vertical counter for correct timing. A *Variable Sync Time* is implemented in *patt_core*, a feature to vary the horizontal synchronization pulse, for a balanced erase time. The horizontal synchronization pulse is used for both writing (logic 1) and erasing (logic 0), The ratio of this can be adjusted using the *Variable Sync Time*. See Sections 4.2.1 for details on write and erase time.

The subcomponent *patt_mp* (mp stands for movie/picture, to test the two use cases) generates image data from the horizontal and vertical value of *patt_core*. With just using some XOR operations on these counters, we can make a checker board test pattern.

When developing applications for the E-Paper Display, designers can choose to make their own horizontal and vertical synchronization signals. Or reuse the subcomponent *patt_core* and use *patt_mp* as a template for their design.

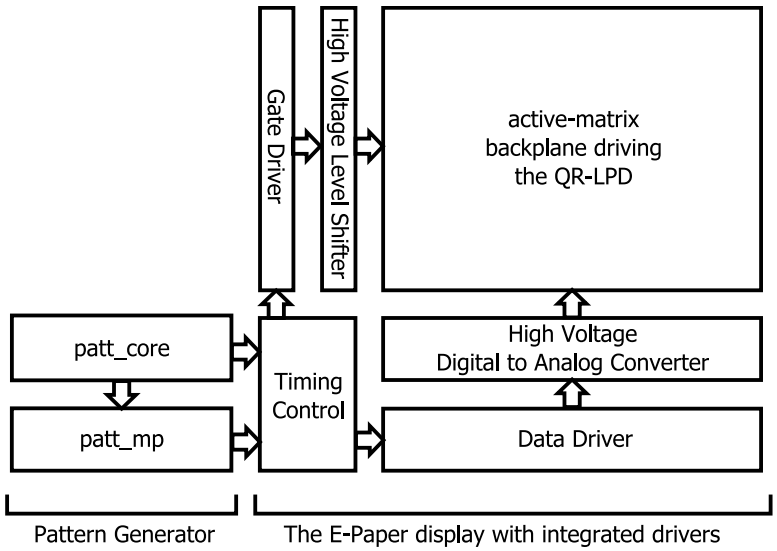

Figure 4.5: The Display Driver with an build in Pattern Generator.

4.2.3 Ring Oscillator

We will include a build in Ring Oscillator, mainly for testing purposes. The Ring Oscillator will not oscillate at a reliable frequency, so it is not a suitable clock source to be used as the main system clock. Although it might be interesting to connect this Ring Oscillator in a test setup with the Display Driver and the Pattern Generator, to test the display with a test pattern using only the on-chip components, fabricated with the SG TFT technology. In a real world setup, the system clock is most likey to be provided by the device that writes the display (e.g. microcontroller, FPGA).

The Ring Oscillator is ring of an odd number of inverters, connected to each other from output to the input of the next inverter. This is the defacto standard circuit for gate delay measurement, t_p. The oscillation period T is determined by the signal propagation time through the complete chain of inverters, or $T = 2 \times t_p \times N$ with N inverters in the chain. A full clock cycle consist of two signal transitions, low-to-high and high-to-low, resulting in the factor 2.

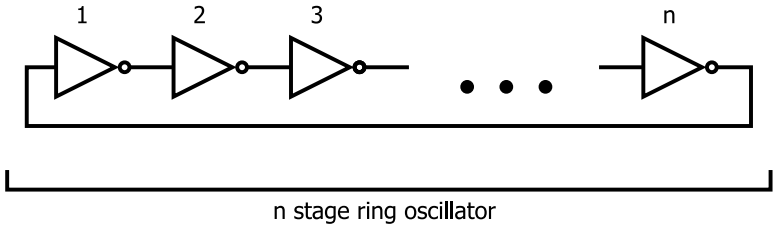

Figure 4.6: Circuits of a n-stage ring oscillator, where n is the odd number of stages.

4.2.4 Buffers

The control signals of the drivers have a large capacitive load. These signals are connected to all of the unit drivers and have a large number of gates connected to them. The normal approach is to use buffer trees to connect all those gates. This has the advantage that the load is balanced and the buffers can be placed distributed over the display. Although a balanced buffer tree is very important for high speed sub micron chips, we are not there (yet) with the SG-TFT technology. With operating frequency of 2MHz, the display can considered to be a low speed device, so the wire delays are neglected and not considered to be the speed bottleneck of the whole system.

Instead of making a balanced tree buffer, we opted for a proportionately sized buffer for those big control nets. From the synthesis we can report back the amount of load on each of those control lines, and dimension a buffer accordingly.

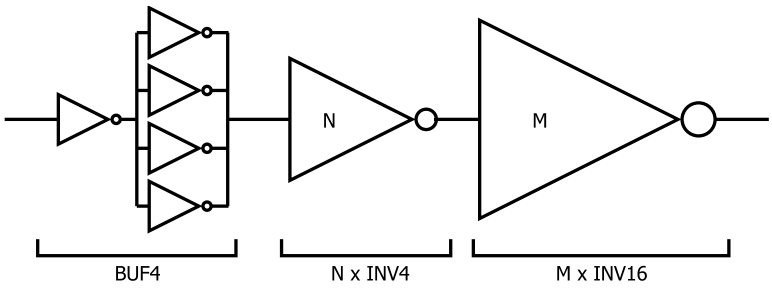

Figure 4.7: Generic 4 stage buffer, with parameters N and M for the number of parallel inverters.

A generic buffer component is designed in VHDL. This buffer is non inverting, resulting in a equal number of inverter stages. For simplicity, the total depth of inverters is kept to 4 stages. The generic buffer looks as follows: buf4 (inv, 4×inv); m×inv4; n×inv16; Where the m and n are the generic parameters for sizing the buffer. When using the generic component, it must be taken to account not to violate the fan-in and fan-out between the stages while fulfilling output load requirements.

4.3 High Voltage Components

In order to move the Liquid-Powder particles, high voltages up to 70V are needed. So it is not possible with the low voltage (5V) digital circuits to directly control the pixels. Special high voltage transistors are developed to operate at these high voltages without breakdown. These SG high voltage TFTs will drive the Liquid-Powder particles and form the interface for the QR-LPD E-Paper material. Special interface components are needed to make it possible to control the display in low voltage digital domain.

The next subsections will discuss the high voltage parts of the E-Paper Display. First the Active Matrix Backplane (Subsection 4.3.1) and then the two components that form the interface between the low voltage domain and the high voltage domain: the High Voltage Level Shifter (Subsection 4.3.2) and the Digital to Analog Converter (Subsection 4.3.3).

4.3.1 Active Matrix Backplane

QR-LPD is suited to be driven by the passive matrix method. For this E-Paper display it is more interesting to drive the QR-LPD by the Active Matrix Backplane made from SG-TFT, to showcase the possibilities that the SG technology can offer. A small 2x2 Active Matrix Backplane circuit is illustrated in Figure 4.8. As seen in this illustration, each pixel has two transistors and one storage capacitor.

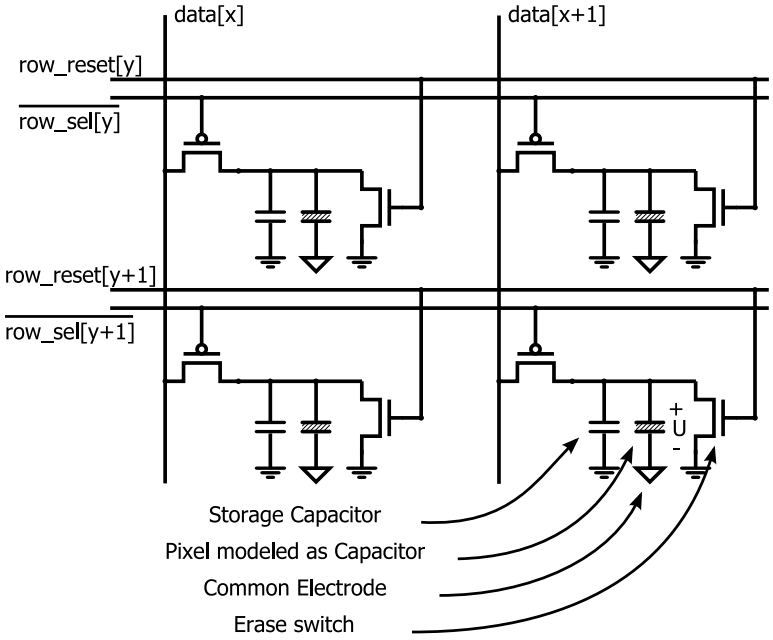

Figure 4.8: Active Matrix schematic for four pixels.

Writing is done by activating a row with *row_sel*, and the voltage on *data* is transfered through the PMOS to the pixel and storage capacitor. The voltage range of *data* is 35V to 70V, voltages below the threshold voltage of 35V are useless and not interesting. The PMOS is perfect for transferring the *data* voltage (even the maximum voltage of 70V) to the pixel, the PMOS stays *on* until the capacitive load is charged till the *data* voltage (The gate source voltage will always be bigger than the threshold voltage $V_{GS} > V_{th}$). This is not the case when using a NMOS here, the NMOS will switch *off* before fully charging the load. The NMOS TFT is better suited for resetting the pixel, pulling the pixel electrode to ground, and discharging the storage capacitor.

Notice that the pixel is modeled as a capacitor, in Figure 4.9 we can see the origin of this. A pixel consist of QR-LPD particles between two electrodes, the first one is the pixel electrode connected to the PMOS SG-TFT, second one is the top common electrode V_{common} share with all the other pixels. The two electrodes with the QR-LPD material in between has the electrical characteristics similar to a capacitance, hence the pixel is modeled as such. V_{common} is the ITO plane on top of the QR-LPD, and is both transparant and electric conductive.

For writing, the *data* voltage (35V-70V) passes through the PMOS to the pixel electrode. Only when V_{common} is at 0V, the potential difference between the two electrode

will between 35V and 70V. When V_{common} is not 0V, but instead 70V, the potential difference on the QR-LPD will in the range of -35V en 0V. This is below the threshold voltage, not enough to change the pixel.

For erasing, we will use the NMOS TFT inside the pixel. V_{common} is put to 70V, and the pixel electrode is 0V when the NMOS transistor is switched on. The potential difference of -70V over the QR-LPD will erase or reset the pixel, resulting in a white pixel.

The storage capacitor makes the whole display more robust against noise. With this capacitor it is possible to write faster than the pixels response time. Changing QR-LPD pixels, from black to white or vice versa, takes 0.2 msec (see Figure 2.8). In a passive matrix addressed QR-LPD display, it means that writing each line must take at least 0.2 msec for the Liquid-Powder particles to settle down. In the active matrix display it is possible to quickly charge up the storage capacitor (< 0.2 msec), and continue with the following lines, while the storage capacitor ensures the voltage over the pixel stays for the Liquid-Powder particles to settle (> 0.2 msec).

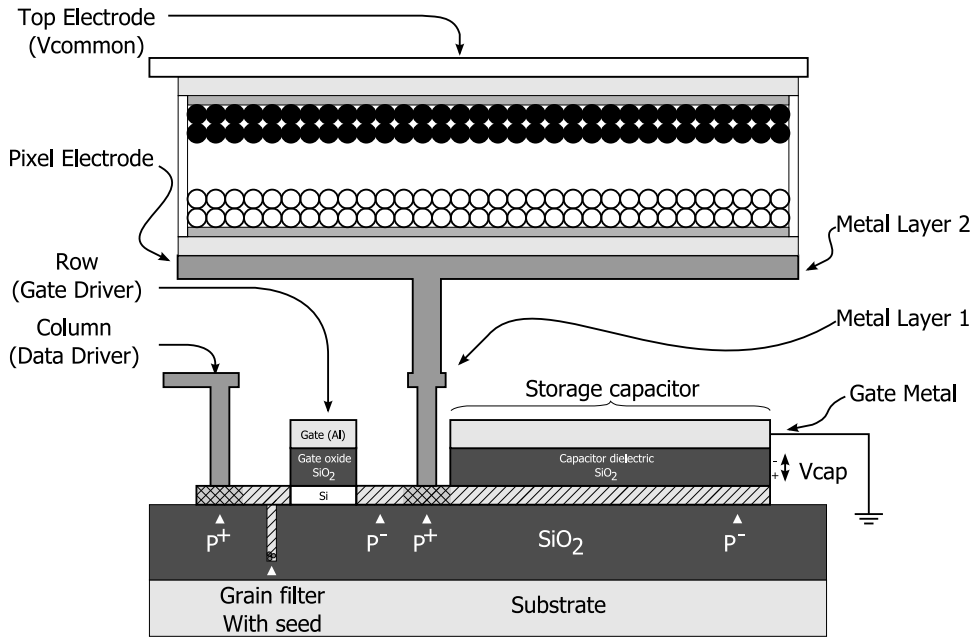

Figure 4.9: Cross section of a pixel with a SG PMOS transistor.

In Figure 4.9 a cross section of a single pixel can be seen. The E-Paper Display is manufactured on a substrate, this can be a silicon wafer, glass or plastic. On this substrate the electronics are made with the SG TFT technology. In the cross section, a high voltage SG PMOS transistor can be seen, connected to the storage capacitor and the pixel electrode. The storage capacitor is made from two conductive planes with SiO_2 as dielectric in between. The pixel electrode in found on the very top of the electronics. On top of this the QR-LPD is glued, with cells filled with black and white Liquid-Powder. The optical transparant and conductive ITO plane on top of the QR-LPD forms the common second electrode for all the pixels.

4.3.2 High Voltage Level Shifter

The low voltage Gate Driver controls the high voltage SG-TFTs of the Active Matrix Backplane. High voltage level shifters are needed for the low voltage logic to interface the high voltage matrix properly. In Figure 4.10 the level shifter circuit is seen. Four high voltage transistors are used to convert the incoming low voltage logic levels to high voltage logic levels, two PMOS and two NMOS. These transistors are LDMOS type transistors with an extra thick gate oxide, these are designed to endure and survive the high voltages. The Gate Driver has two types of signals, for writing and erasing. Each row will have two level shifter circuits accordingly. The Level Shifter expects a low voltage differential input signal A, and converts it in to a high voltage differential output signal Y.

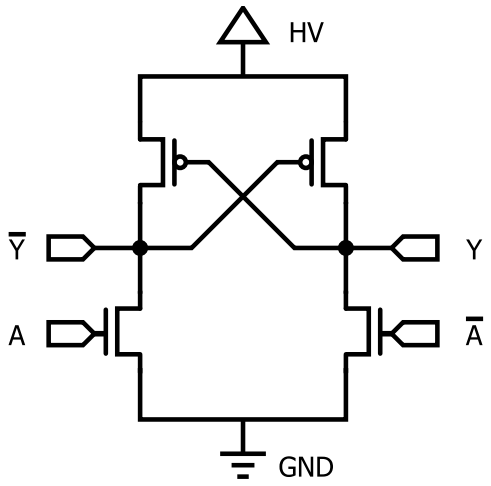

Figure 4.10: Level shifter circuit. Input A, ouput Y

4.3.3 Digital to Analog Converter

The column lines of the display are also known as data lines, since they carry the data information that will be written on to the display. The Data Driver hold this information in digital form, so a high voltage DAC (Digital to Analog Converter) is needed to interface the Data Driver with the data lines of the Active Matrix. This high voltage DAC will convert the low voltage digital data to a high voltage analog signals. With 320 column lines on the display, 320 voltages need to be generated at the same time, this is done with 320 individual DACs

The pixel reflectivity (black-grey-white) is a function of a potential difference over the Liquid-Powder between the two electrodes. The relation between the reflectivity and the potential difference is not a linear function. This can be seen in the hysteresis plot in Figure 2.9. Writing pixels is only possible with voltages over the threshold voltage of 35V. So the DACs are designed to ouput voltages in the range of 35V and 70V.

A current driven DAC architecture is chosen. The simplified schematic of the DAC is shown in Figure 4.11. In this architecture the current sources and switches can be built

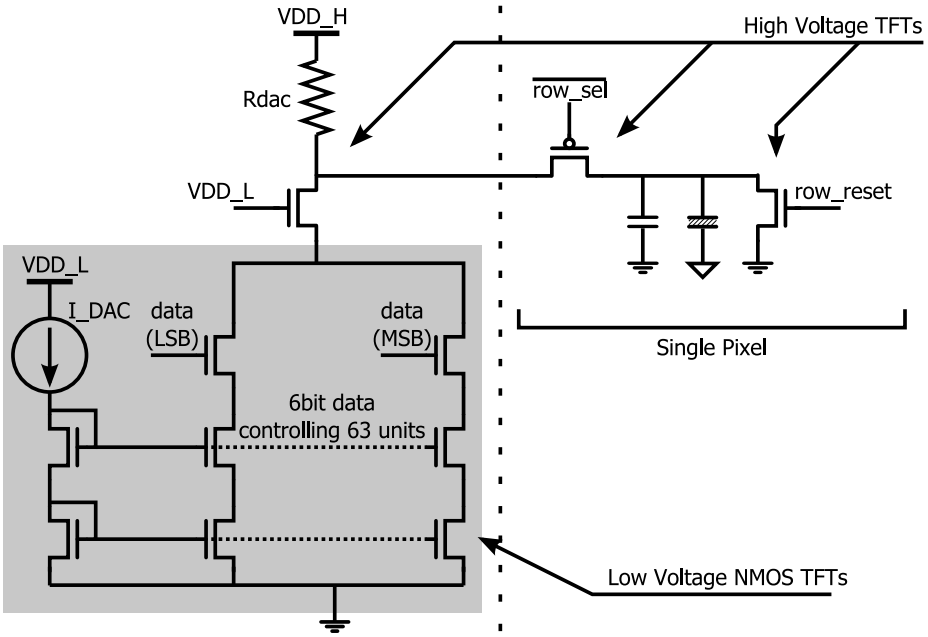

Figure 4.11: Schematic of the current driven DAC (left) connected to a single pixel circuit (right). The pixel is modeled as a capacitor, and connected to a common electrode V_{common}.

using the low voltage, small and fast NMOS SG-TFT. The current drives a resistive load which generate the output voltage. Between the resistive load R_{DAC} and the current sources, one high voltage NMOS TFT is used to protect the current DAC network from breakdown due to a large voltage swing. The cascode current sources are employed to minimize the current variation and the cascode also reduces feed through effect due to the switching of the switches. The major advantage of this architecture is the use of low voltage SG-TFTs for the current sources and switches, only one high voltage transistor is needed. This means that that we can control the DAC directly with the low voltage Data Driver. DAC architectures that use the high voltages TFTs as switches are not practical. Additional level shifters need to be inserted between the Data Driver and DAC, resulting in many high voltage transistors and a slow DAC.

The unity current generator is mirrored by 63 DAC unit cells. These unit cells are binary weight controlled with 6 bits digital data. The Most Significant Bit (MSB), controlling 32 units and the Least Significant Bit (LSB) controls only one DAC unit cell. The DACs supply the voltages on the column lines. Writing a line is done when two conditions are met. First the Gate Driver needs to select and activate one line of interest. Second, the common electrode V_{common} needs to be set to 0V, so that the potential difference on the pixels of the selected row are between 35V and 70V, making it possible to write a line. The mapping of the data values to analog signals can be seen in Table 4.1. With data input values ranging from 0 to 63 corresponding to the output voltages 70V to 35V. The resulting pixel reflectance is only valid when V_{common} is 0V and when the the pixel is erased (reset to white) prior to writing.

Table 4.1: The range of the Digital to Analog Converter.

Data Value		Output Voltage	Pixel Reflectance
0	000 000	70V	Black/Write
1	000 001	69.4V	•
•	•	•	•
•	•	•	•
•	•	•	•
62	111 110	35.6V	•
63	111 111	35V	White/No change

4.4 E-Paper Simulator

Simulators can be useful for a number of different reasons. We have build two types of display simulators for testing, verification and development purposes. The software display simulator and the hardware display simulator.

For testing and verifying the different display driver development stages, a software display simulator was made in Tcl/Tk for Modelsim. This script based display simulator interprets the (low voltage) digital signals from the two drivers and translates them into a 64-scale gray image. Different use case modes, write and erase are supported in this simulator. The simulator works by looking at he V_{common} signal. The logic level 0 (corresponding to 0V on the common electrode) indicates a write. And the logic level 1 (corresponding to 70V on the common electrode) indicates a erase. So depending on

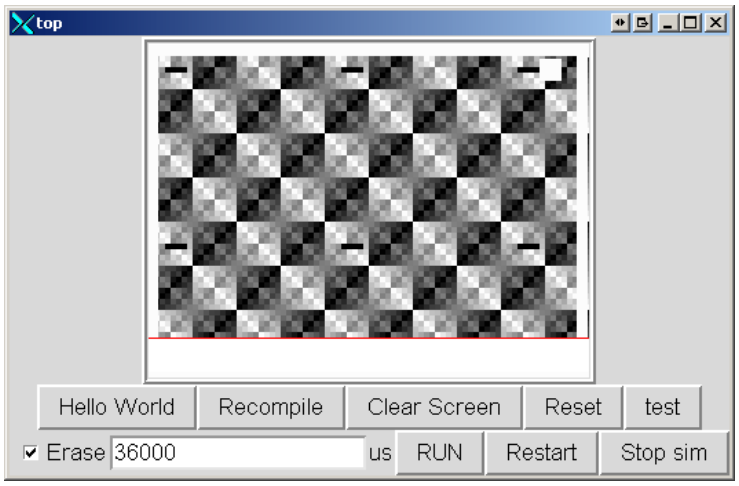

Figure 4.12: The Modelsim E-Paper simulator written in Tcl/Tk. The line that is being erased is shown in red.

the signal V_{common}, the simulator will write or erase the row(s) that the Gate Drivers activates. It is possible to erase multiple rows by programming the Erase Vector, and this is supported by the simulator. The hysteresis curve of the Liquid-Powder is not implemented in this software simulator, meaning that it is possible to overwrite a darker gray shade with a lighter one without erasing. With real QR-LPD this is NOT possible, the darker gray shade will become more dark due to the repetitive writing. The software simulator is quite slow, it takes about one minute to simulate a whole frame.

For practical development of application that want to display useful information using the real E-Paper Display, a hardware simulator is build. This hardware simulator is designed and tested on an FPGA, and can act like the E-Paper Display in the Movie mode. The simulator displays the image on a standard computer screen, and is capable of simulating the Movie mode in real time or up to 2.5 times faster. Useful for development of games or video players, without the slow simulation time of the software simulator. The subcomponent *patt_mp* described in Subsection 4.2.2 can be used as a template for the design. The hardware simulator is very basic, it is possible to support Picture mode by expanding the simulator with a frame buffer. With a frame buffer it is even possible to implement the hysteresis curve of the Liquid-Powder, making it a full E-Paper Display simulator.

A photo of the hardware simulator can be seen in Figure 4.13. The computer screen is connected to the FPGA board. The FPGA controls the screen at a screen resolution of 640×480 at 60Hz. Because our E-Paper is a fourth of this screen resolution (320×240), only the upper left corner is valid for the simulators results. In the simulation seen in the photograph, a bouncing box application is seen, running on the same FPGA. The white ball, bounces around within the box and can also bounce at the black obstacles placed within the box.

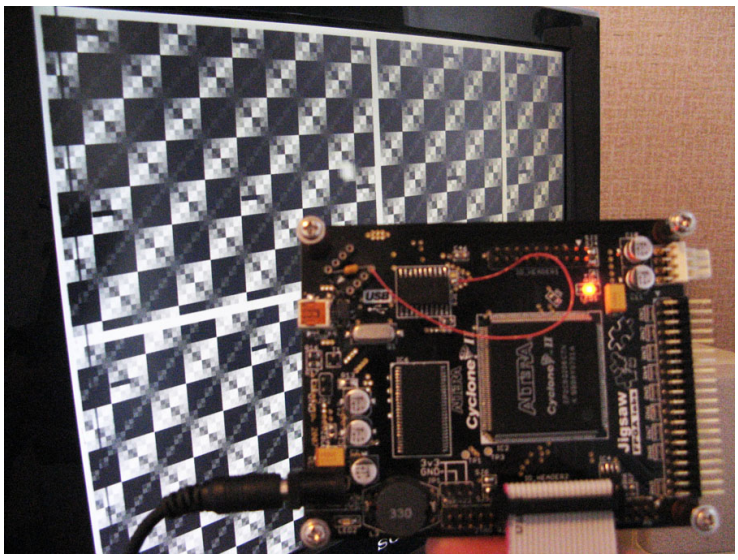

Figure 4.13: The hardware E-Paper simulator running on FPGA. The content is put on a standard computer screen.

4.5 Conclusions

This chapter discussed the different aspects that had to do with the implementation of the E-Paper Display Driver. First a Display Organization block diagram is made, seen in Figure 4.1. In this diagram, all of the components of the Display Driver can be found. A distinction is made between Low Voltage and High Voltage components.

Low Voltage Components
The Low Voltage components are all digital components designed with the automated design flow, using the SG Standard Cell Library. The digital components implemented are Display Driver, and two components that are more related to testing: Pattern Generator and Ring Oscillator. The Display Driver consist out of the following subcomponents: Gate Driver (controls the rows), Data Driver (collects the incoming data to put on the columns) and the Timing Control (insures the right synchronization of the components in Display Driver). Gate Driver and Data Driver are divided into Unit Drivers, responsable for only a single row or column respectively. This will reduce the work later on, when doing the layout of these components. Pattern Generator is not part of the Display Driver, but instead it can act like a build in self test. Pattern Generator is capable of generating display signals suited for the Display Driver. A test pattern is included to verify the Displays basic functionality. A Ring Oscillator is also implemented. Although a Ring Oscillator is not a reliable clock source to be used as a system clock, for a test setting it is possible to connect this Ring Oscillator together with the Pattern Generator and the rest of the Display for an even more complete build in self test.

Two features have been implemented, the *Programmable Erase Vector* and the *Variable Sync Time*. With these features it is possible to determine the correct settings for proper use of the Movie Mode with the Erase before Write scheme. The subcomponent Gate Driver has the *Programmable Erase Vector*. By default the Erase Vector erases the upcoming row before this row gets rewritten. By reprogramming this, it is possible to erase a different row than the one that is set by default, it is even possible to erase multiple rows at the same time. Row lines will be erased multiple times, which makes it possible to shorten the erase time. The combined erase time of multiple erases ensures that the row is erased properly before writing. Another way to influence the erase time is by changing the horizontal synchronization signal *hsync*. The Display Driver uses the *hsync* for the write (logic 1) and erase (logic 0) time. By changing the time when *hsync* is 0, we can change the corresponding erase time. The Pattern Generator is equipped with a feature allowing it to change the *hsync* pulse width, the so called *Variable Sync Time*.

High Voltage Components
The High Voltage components are high voltage analog circuits made with the special designed high voltage SG-TFT. The Active Matrix Backplane forms the electrical interface with the Liquid-Powder particles, see Figure 4.9 for the pixel cross section. It defines the pixels in the QR-LPD material. Each pixel consists of a PMOS TFT, a NMOS TFT, a storage capacitor and the pixel electrode for the interface with the E-Paper. The backplane is organized as a matrix, with horizontal row wires en vertical column

wires running across the whole screen. The PMOS TFT acts as a switch, when turned on, it will transfers the voltage on the column wire to the storage capacitor and pixel electrode. A PMOS TFT is well suited for this job, since it is capable to fully charge the storage capacitor. The NMOS TFT takes care of erasing the pixel. The storage capacitor can stably hold the voltage over the QR-LPD for at least 0.2 ms, so the Liquid-Powder particles can move and change the reflectance of the pixel.

Two High Voltage components are connected to the Active Matrix Backplane. These components form the interface with the Low Voltage digital components and the high voltage Active Matrix Backplane. The Gate Driver is connected to the backplane via High Voltage Level Shifters. A single level shifter is made out of two PMOS and two NMOS high voltage SG-TFTs. Transforming low voltage 5V digital signals to high voltage 70V signals. The Data Driver is connected to the backplane via Digital to Analog Converters (DACs). A current driven DAC architecture is used, with this architecture the majority of the used transistors are low voltage type NMOS TFTs. So the current sources and switches are implemented with the low voltage TFTs and can be directly connected to the Data Driver. The DAC combines two functionalities in one device, interface between Low Voltage and High Voltage, and the conversion of digital signals to an analog output signal. The DAC is a 6 bits DAC, capable to output 64 different voltages in the range between 35V and 70V.

Simulators

Two E-Paper simulators were implemented, a software based simulator and a hardware based simulator. The simulators can be used for testing, verification and development purposes. The software simulator is script based, written in Tcl/Tk for Modelsim. The two use case modes, Picture and Movie mode, together with write and erase can be simulated with this simulator. The hardware simulator is designed and implemented on FPGA. The FPGA is connected to a standard computer screen to display the same content that should appear on the real E-Paper Display. When developing applications for the E-Paper is possible to connect this with the FPGA or design it in the FPGA. The advantage with the hardware simulator is the real time performance, useful for development of games and movie players for the E-Paper Display.

The Process of Design and Implementation

5

This chapter discusses the process of the design and implementation during the development of the E-Paper Display Driver, this includes design approaches, some design considerations and the different implementation stages. The implementation stages are Writing functional HDL code, Synthesis and Layout. Although it may seem that these stages are decoupled, this is not the case. The implementation is an iterative process, where it sometimes is needed to go back to improve the design.

Starting off with the Design Exploration (Section 5.1) a concept design is realized. A Structured Design (Section 5.2) approach is taken for writing the functional hardware description (VHDL). Synthesis and Layout are described in Section 5.3 and Section 5.4 respectively. These two sections also describe some of the functionalities associated with the EDA tools. Three examples are used to explain different techniques and strategies used during synthesis and layout. These are found in the Subsection 5.3.1 about Synthesis on the Pattern Generator and the Subsections 5.4.1 and 5.4.2 about the layout of components Data Unit and Comparator respectively. Throughout the different implementation stages, verification by simulation is needed and described in Section 5.5. Section 5.6 discusses the Timing Analysis.

5.1 Design Exploration

After the necessary literature study on the two technologies, a display driving concept was made. Most information on driving flat panel displays are related to LCD screens, the basics of addressing the screen as a matrix can be applied to our E-Paper Display as well. The basic concept is explained earlier (Subsection 3.1), with the Gate Driver driving the rows, and the Data Driver driving the columns. An initial design is made in VHDL, with basic features for these components. To verify the design at this point, a display simulator was made in Modelsim using the scripting language Tcl/Tk. An image on the simulator display means that the basic functions of Gate Driver and Data Driver work, thus the initial implementation of the concept of driving a screen is verified.

With the concept verified, the real work of implementing a proper Display Driver can begin. Starting off with the initial draft as bases, expanding the design into a feasible working E-Paper Display Driver with all the necessary features.

We use the following EDA tools and define the following implementation stages: *Modelsim* for writing and testing the digital components; *Synopsys* for synthesizing the designed digital components and generating a netlist; *Cadence* for placing and routing the components to get a chip layout for the display. Although these stages may suggest that they are independent and decoupled, this was not the case during design and implementation. It was more of an iterative process, jumping back and forward between the stages, each time improving the design.

5.2 Structured Design

The digital components of the Display Driver are designed in the hardware description language VHDL. Using Modelsim for simulations, the VHDL hardware components can be tested in software for correct operation.

The initial designs for the different components were implemented as behavioral VHDL designs. After realizing that both Gate and Data Driver have regular structures, the behavioral description needed to be changed to a structural description. With the structural design, we reduce the Gate Driver in to a Gate Unit for a single row and then use 240 copies of these units to make a whole Gate Driver. The layout stage will benefit from this structure, since it only needs to layout the Gate Unit, and just use copies for the rest. The same goes for the Data Driver, a Data Unit is created and 320 copies of this make up the Data Driver.

If the behavioral design is used, we will not benefit the regular structure of the drivers. Doing the layout of this would literally be impossible. All the gates would be clustered together, without any form of hierarchy. Resulting in a clump of gates, with unnecessary long wires, and a highly inefficient layout.

5.3 Synthesis

When the VHDL designs show promising results in Modelsim, we can move to the next step, the synthesis. The synthesizer Synopsys will map the VHDL component description onto logic gates defined in the SG-TFT Standard Cell Library. It is good to know how to write synthesizable VHDL code for Synopsys to be useful. For example, asynchronous resets of registers are not synthesizable in the SG technology, all registers must have a synchronous reset. Synthesis script files were used to record the different synthesis steps and to automate the synthesis. These script files are written in the script language Tcl.

The synthesis is an important stage, with the synthesizer the designer still has a lot of control and influence on the design. By constraining the design, it is possible to optimize the design for speed, power or area. This is a choice that the designer has to make, and decide what criteria is the most important one. With the display driver, the requirements are not that strict. This is due to the relative slow operating frequency and the fact that the timing parameters are based on assumptions and are not empirical timing parameters. For example, it is difficult to optimize the design for speed, when the synthesizer relies on these assumed timing parameters. It is possible to end up with a design that does not work at all. So it decided not to do any timing optimizations until the correct timing parameters are known.

Besides speed and area optimizations, the synthesizer can also be used for adding or removing structure in the design. It is possible to group cells into subdesigns and the reverse, un-group subdesigns. Un-grouping of subdesigns is useful when a subdesign is fractionally utilized, having unconnected pins and useless logic cells. The synthesizer can resolve these and optimize and remove unused pins and cells. Grouping cells in to a subdesign can make the layout easier. It is even possible to structure the design according to the label inside the VHDL code. The usefulness these functions are best explained with an example.

5.3.1 Synthesis of Pattern Generator

The pattern generator consists of two counters, four comparisons, a small state machine and some glue logic. Of the four compares, three are compares with constants. These compares do not need full functional comparators since they only compare with constants and optimizations are possible. So these comparators were ungrouped and optimized. The remaining comparator is a full functional comparator, needed for the variable sync-time. The two counters, the horizontal pixel count (count to 320+sync) and vertical line count (count to 240+sync), are both 9 bit counters. For the vertical counter, 8 bits was sufficient, but both counters are intentionally kept the same. This way extra work is avoided at the layout stage. Only one counter has to be placed and routed instead of two. The pattern generator now consists of three subdesigns (two adders, one comparator) and a lot of gates for the state machine, the other three comparisons and glue logic. The loose gates were grouped together in a new subdesign, this to maintain some structure in the pattern generator and to make it easier when routing the component. The result can be seen in Figure 5.1. The structural description is taken and additional re-structuring was done as described. A clean schematic is seen with only four subdesign blocks, the two adders, one comparator and one subdesign that holds the state machine, the other three comparisons and some glue logic.

When comparing the structured approach with the synthesis of the behavioural description, and synthesize this without any re-structuring in mind, it will result in a chaotic schematic seen in Figure 5.2. With some effort, the comparator can be found on the left and the two adders are on the center right.

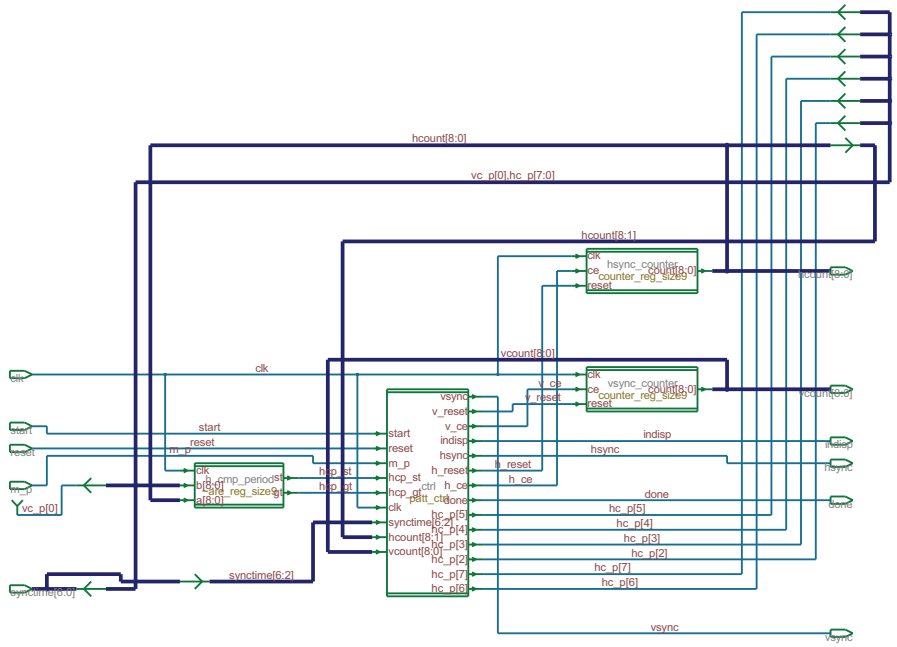

Figure 5.1: Structural synthesis of the pattern generator core after re-structuring in the synthesis tool.

It can be seen that with the synthesizer, it is still possible to add or remove structure from your design. The techniques shown here intended to lighten the work at the layout stage. By reusing components, less layout work is needed. By dividing a big design in to smaller subdesigns, it will be easier to layout the complete design in smaller steps.

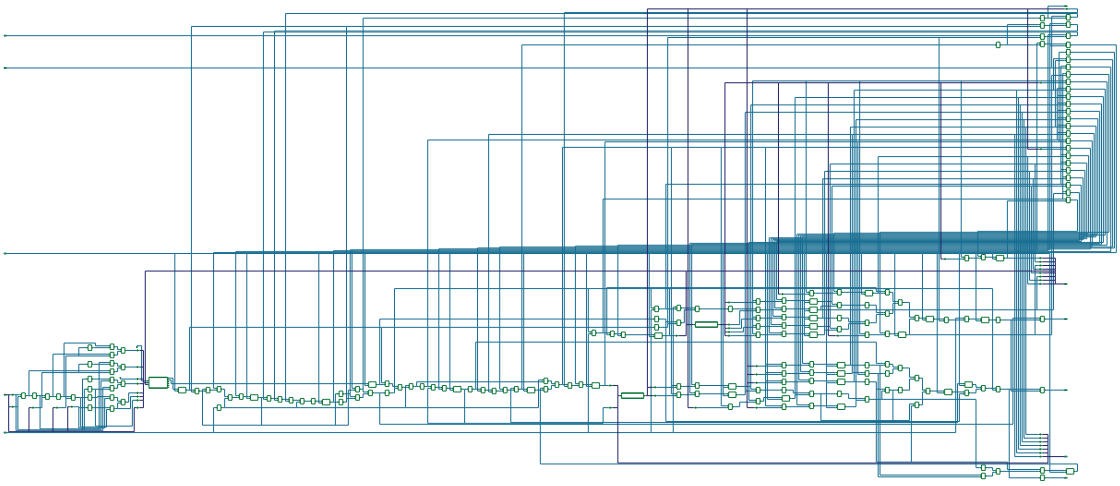

Figure 5.2: Behavioural synthesis of the pattern generator core.

5.4 Layout

With all the netlist files verified and working according to the simulations, the layout can be made. The layout of designs and subdesigns is done in two steps: Place and Route. During this stage it is important to keep in mind the number of metal layers. The E-Paper Display will only use two metal layers for the wiring. This means that extra space has to be reserved between the cells for routing the wires that connect to the cells.

First the cells of the design are placed and then connected according to the netlist by routing wires. For both place and route, it is possible to let the computer do this in an automated fashion, but this may result in a sub-optimal solution. Especially when the design has a regular structure, the layout tool may fail to exploit this regularity.

In the E-Paper Display driver some components are manually placed to obtain a better layout. Components that have regularity are for example counters, looking at a larger scale, Gate Driver and Data Driver are regular because they are structural designed in such a way to expose their regularity. These component benefit from manual placement to fully utilise their regular structure. After the manual placement, the rest is routed by computer. An optimized placement results in a smaller design, since less space has to be reserved for routing the wires because most of the wires are kept local and short.

5.4.1 Layout of Data Unit

The Gate Driver and Data Drivers are build out of 240 Gate Unit components and 320 Data Unit components respectively. Making the layout for the Gate Unit and Data Unit is far more easier than making the layout for the whole Driver without any hierarchical structure. A Unit component consists of a handful of logic gates compared to the whole Driver. The size of the Unit components is restricted by the pixel size of 150μm(for a straight forward connection with the Active Matrix). A Unit subcomponent wider than the pixel size will result in bigger drivers compared to the display or alternative Unit placement strategies.

We will use the Data Unit as layout example. Data Unit consists of two register parts: a shift register and an output register. Both registers are 6 bits wide, consistent with the number of bits needed for the 64 gray-scale levels. In the schematic seen in Figure 5.3, a fairly regular structure can be observed. The larger, wider blocks are the D-flip flops. The left ones are for the shift registers with the feedback logic at the bottom, this is needed because the flip flop does not have an enable signal and the values are fed back to retain the value. The registers on the right side are the output buffers, holding the pixel values when writing. What clearly can be seen in the schematic is that the gates are organized in rows of 6. The gates corresponding to the same bit are found on the same row.

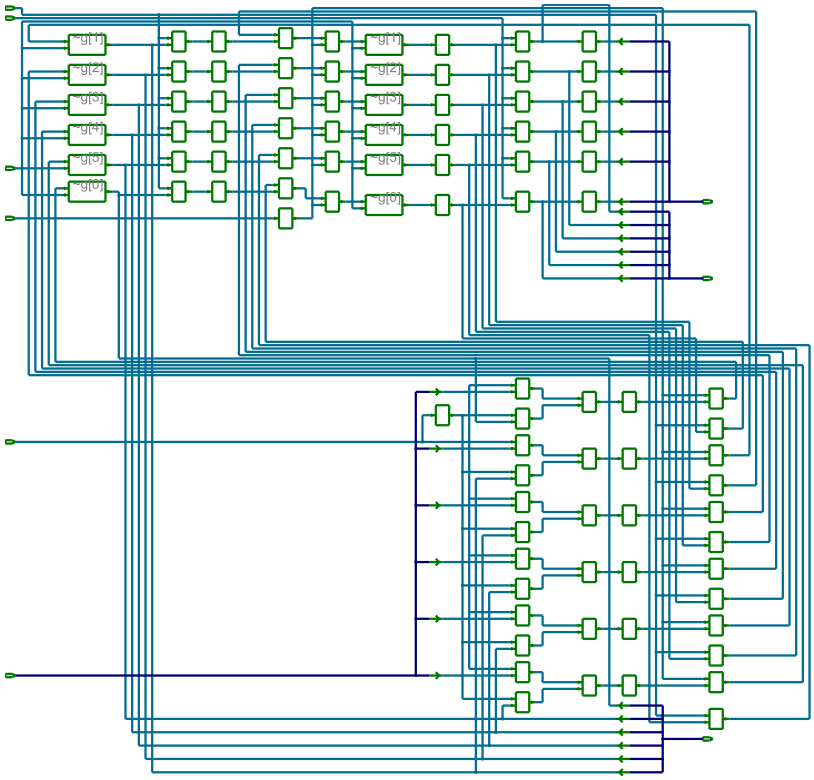

Figure 5.3: The regular structure found in the schematics of the Data Unit.

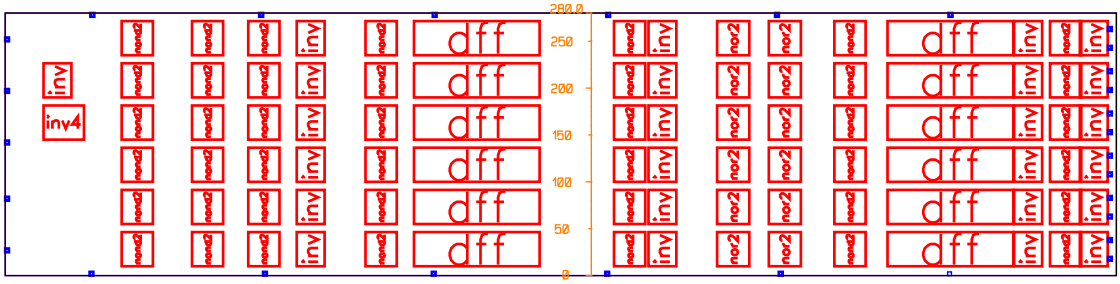

Figure 5.4: The regular structured placement of the Data Unit.

To exploit this parallelism, a manual-place automatic-route approach is taken. In the layout tool Cadence the gates are manually ordered and structured. With the schematics as reference the gates are ordered, in a similar fashion, in six rows with gates corresponding to the same bit on the same row. The result can be seen in Figure 5.4, the Data Unit is $280\mu m$ wide. On the right side, the data out pins can be seen that lead to the Digital to Analog Converter. The complementary signals can also be found, resulting in twelve pins. On the left side the control signals are located, clock, reset, latch enable, output enable etc. The Data Unit is also part of the big shift register of the Data Driver. 6 bit data is forwarded to the subsequent Data Unit, data enters via the bottom six pins and gets shifted via the top six pins to the next Data Unit.

The height of the standard cell is fixed to $37\mu m$. With the restriction of $150\mu m$ for the Data Unit (same restriction holds for Gate Unit), it can be concluded that this layout is almost two times too big. At most it is possible to fit in three rows of gates. With several iteration steps, by trail and error, it was found that a configuration with two rows works. This means that the requirements are met and it is still possible to successfully route the gates. The Data Unit is now at least three times longer, and the width is now smaller than required: $140\mu m$. This is to reserved space for additional wires that are required later on. In Figure 5.5 we can see a piece of the Data Driver. Three Data Units are shown here with a combined height of $3 \times 150\mu m = 450\mu m$. Inside a single Data Unit it can be clearly seen that the gates are organized in two rows instead of the six row configuration previously seen. Figure 5.4 and Figure 5.5 are not shown in scale, although both configurations consist out of six rows of gates, they are not of the same height $280\mu m$ versus $450\mu m$. The two row configuration has more space between the two rows for the wires.

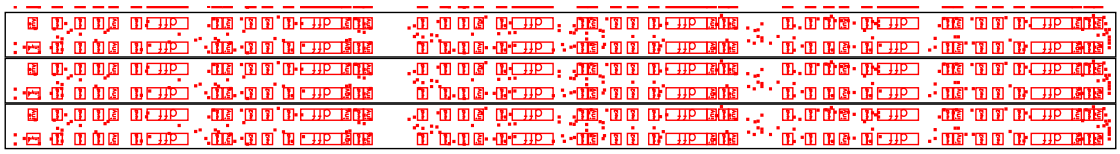

Figure 5.5: A portion of the Data Driver, three the Data Units are seen here.

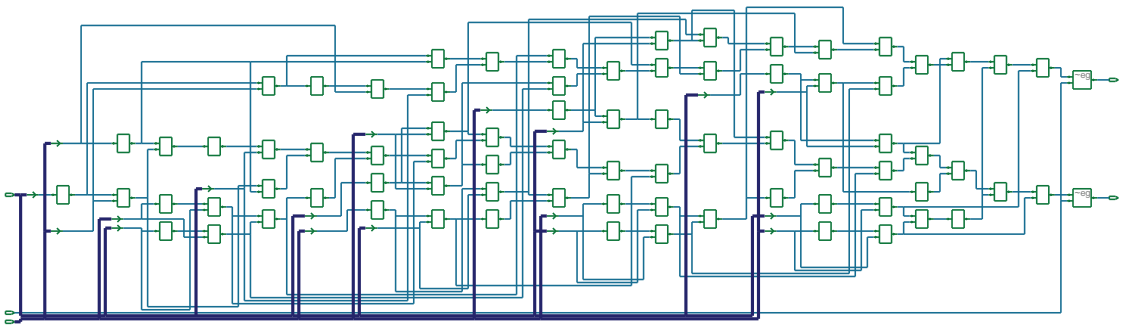

Figure 5.6: The irregular structure of the 9 bit comparator.

5.4.2 Layout of Comparator

One example of a schematic that seems to have an irregular structure at first hand is the comparator, seen in Figure 5.6. Although it most likely that the comparator function has some kind of structure or regularity, this was not easily observed in the schematic view. The manual place automatic route approach is taken again, but this time the schematic view did not provide an straight forward layout plan for the gate placement. Instead a different place strategy was used. This comparator compares two 9 bits numbers (a and b) and has two output signals (*greater than* and *smaller than*). What can be observed from the schematics is that all (or nearly all) of the signals go from left to right, inputs on the left, and the two outputs on the right. The same pin orientation is used for the layout. On the left side the a and b bits are woven together, grouping pins according to their bit significance. Knowing that the signal flow direction is from left to right, the gates can be placed accordingly. Starting at the a and b input pins, and than manually look for the cells that are directly connected to these pins. This was done by placing a clear overhead sheet on top of the computer monitor and mark the gates with a white board marker. First look for the logic gates that are directly connected to the input signals, number them according to their bit significance on the overhead sheet with the white board marker. Then move and place to logic cells next to the corresponding input pins, so the wires will stay local and short. The result can be seen in Figure 5.7, with 9 bits inputs there are 9 rows of gates. After placing the first column of gates that are directly connected to the inputs, the subsequent gates were marked and placed, giving structure to the comparator. With each mark and place step, there are fewer gates per column. With fewer gates, there is more space in the vertical direction. At this point the gates were just placed in a grid like orientation, reserving enough space in between for the wires. Once the placement is done, we can route the design. The amount of space between the cells can be adjusted easily. Enough space needs to be reserved for routing the wires, but too much will lead to an inefficient layout. In Figure 5.7, we can see that the gates on the left are tighter packed than on the right. The logic gates on the left are connected using short local wires, while the connections on the right are longer, because these cells were placed in left over space of vertical direction.

An automatic placement approach was also taken, to compare it with the manual results. The placement area was restricted to the same dimensions as the manual layout.

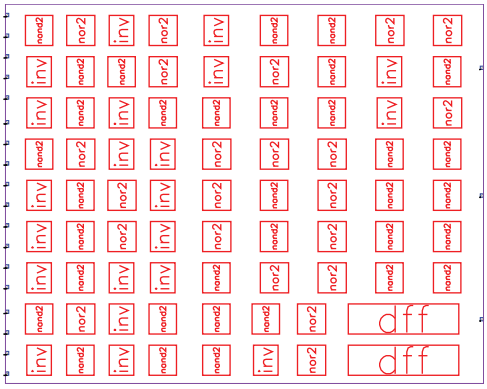

Figure 5.7: The result of manual placing the 9 bit comparator.

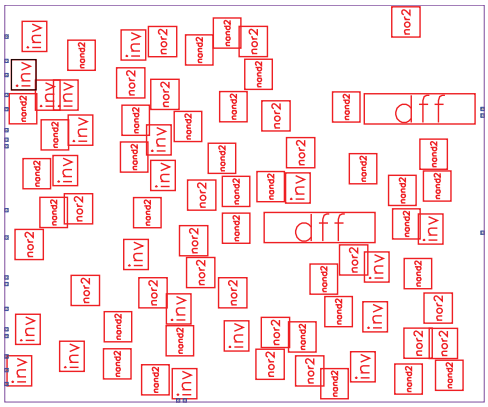

Figure 5.8: The result of auto placing the 9 bit comparator, but unable to route.

The results can be seen in Figure 5.8. After two attempt with the auto-placer and auto-router, it was unable to place and route the comparator inside this restricted space.

Although at first hand the comparator did not seem to have any structure, it does have a clear signal flow without any feedback loops. This property was exploited with manual placement. The auto-place and route was unable to get the same results (successful place and route in the same area). This does not mean that auto-place and route is useless, for state machines and control flow structures, were no parallelism is found, the auto-place and route can get decent results in less time than with manual-place strategies.

5.5 Verification

Throughout out the design process, there are certain milestones where it is good to have some confirmation that the work up till now is still correct. Extensive simulations were done to check the correct and functional operation of the digital logic components. Finally a LVS check is run to confirm if the layout is still corresponding to the schematics and a DRC checker checks if the layout violates any of the DRC rules.

5.5.1 Simulation

In the early stages of design a display simulator was written in Tcl/Tk script. This virtual display was to confirm the basics of the two drivers in a visual way instead of extracting the information out of the wave diagrams.

After finding out that the behavioral descriptions of the drivers are not sufficient (inefficient) for layout later on, structural designs were made based on the behavioral files. Although only the structural design files are used for synthesis, the behavioral files were kept. These behavioral files were maintained and updated with all the design changes for verification purposes. This approach has proven it self several times during the design process, looking for anomalies by just comparing the behavioral and the structural output signals.

After successful synthesizing the structural VHDL files, a netlist can be exported. The format chosen is Verilog, for an easier import in the layout tool Cadence. The netlist is verified for correct functioning in Modelsim. Before this is possible, the Standard Cell Library needs to be exported, because the netlist uses the components of the Standard Cell Library and the simulator needs them as well. In Synopsys we can export the library including some gate related timing information in a VITAL compliant format. VITAL (VHDL Initiative Towards ASIC Libraries) is a industry standard that can be summed up with the following quote:

> *Accelerate the development of sign-off quality ASIC macrocell simulation libraries written in VHDL by leveraging existing methodologies of model development.*

In other words, we can use this to simulate our netlist using the cells of the Standard Cell Library. Again, it was a good idea to run these simulations because two more design errors were found and fixed!

After running the netlist simulation with the Tcl/Tk display simulator, we can say with some confidence that the synthesized design works. Because we got a nice pattern as expected on the display simulator.

5.5.2 LVS

Another verification tool is the LVS check. LVS stands for Layout Versus Schematic. The tool extracts both layout and schematic down to transistor level and compares these to each other. The LVS can check for the mismatches in the netlist and highlight them in the schematics view or extracted layout view. The LVS is very strict when comparing the layout and schematics.

Many of the Display Driver components had to be re-routed, because they did not match the schematics according to LVS. Most of the components were missing some pins (power pins). They were left out because the routed did not connect wire at these pins, but did connect nets of components even if there were no pins. A wrong idea occurred that pins are not always necessary, it turns out that these pins are indeed needed by the LVS.

When the LVS check is successful, without any netlist miss matches, we can draw the conclusion that the layout is corresponding to the schematic.

5.5.3 DRC

A manufacturer has certain limitations for the process, this is normally indicated by the minimal size (gate width) that the manufacturer still is able to create using lithography. In our case, DIMES is able to do the SG-TFT process with a minimal width of 1.5 μm. Apart from the minimal size for the physical structures, there are also a minimal distances for these structures. For example the distance of two parallel wires must be big enough so that do not short circuit. All these manufacture, process and technology dependent information are defined as rules. The Design Rule Checker (DRC) can check if the layout violate these rules. If so it will give an error message and locate the mistake. Ignoring these error messages can lead to an incorrect layout due to short circuits of wires for example. More on this can be read in Chapter 6, where ignoring the DRC led to partially functional test circuits.

5.6 Timing Analysis

When designing digital circuits it is good to make sure that the design works for a given clock frequency. Making sure that there are no timing violations and that the critical signals have no negative slack.

Attempts have been made to do some timing analysis for the designed components. This led to various results depending on the constraints given to the Synthesizer. The Synthesizer bases the timing calculations on the parameters from the SG Standard Cell Library. Parameters for intrinsic rise, intrinsic fall, rise resistance, fall resistance etc.. These values are not determined yet for the SG Standard Cell Library. So we have assigned a unit value for the parameters of inv (inverter), and based on the physical structures of the rest of the gates these parameters are scaled accordingly.

Transistor level simulations of the Standard Cell Library gates have failed as well. We were unable to connect the current Verilog-A model of the SG transistors to the simulator in Cadence. Without these simulations we do not know what the transient behaviour is of our gates, leaving us with incorrect timing parameters.

Another thing that was unknown was the maximum frequency the SG Standard Cell Library can operate on. To investigate this, a test chip with a 51-stage ring oscillator is fabricated. With this ring oscillator we can measure the oscillation frequency and calculate back what the average inverter gate delay is. The gate delay is the clock period divided by two time and the total number of inverter stages. With this information the Standard Cell Library can be adjusted and the timing analysis results would make more sense.

In most designs, timing analysis is a mandatory task for the designer. But what do the results represent when the timing parameters are not correct? What are the dangers of over (or under) constraining the design? After many discussions we have decided that the timing analysis is not too crucial for our display driver. Our design for the Display Driver is fairly simple. There are no long chains of logic gates presents (without any flip-flops in between). Long chains of logic gates have the largest latency. This can lead to dangerous timing violations, when the output signal of such chain arrives too late and misses the clock edge of the next register. The Display Driver is simple because the

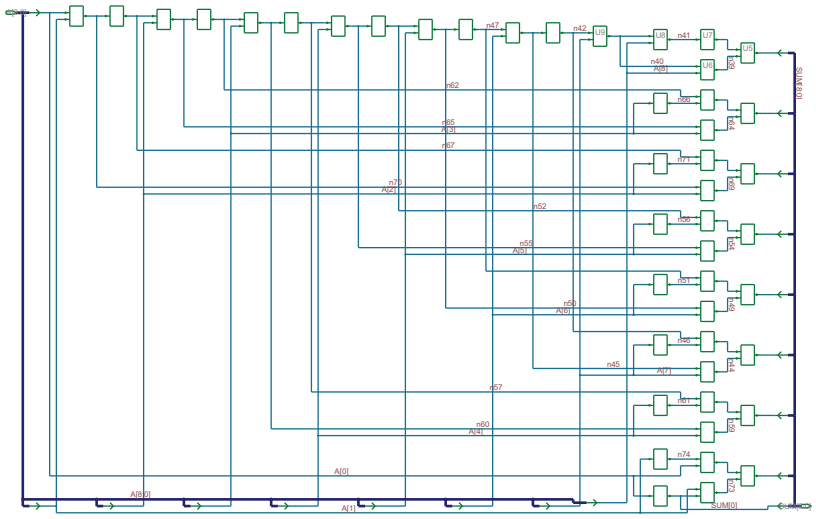

Figure 5.9: Schematics of the incrementer, used in the Pattern Generator.

Display Driver only moves data and does not need to do any calculations. In the worst case, we will have to operate on a lower clock frequency, and have to settle with a lower frame rate.

The Pattern Generator has more complex functionalities. This component needs to count and compare numbers. When looking at the incrementer generated by the synthesizer, in Figure 5.9, we can clearly see a long chain of logic gates. This is the carry propagate chain of 16 logic gates, and is the longest logic chain identified from the design. Theoretically, this chain will limit the maximum operating frequency of the Pattern Generator. The incrementer is part of the counter, the counter has registers to store the current count value and increments this per clock cycle. The total logic chain from register to register, is 18 logic gates. When we want to have a Pattern Generator, operating at 2 MHz, the worst case propagation delay through the chain cannot exceed the clock period of 0.5 μs. Actually this is not true, the setup time of the flip-flop also needs to be taken in to account. Let us assume 0.1 μs for the setup time, leaving 0.4 μs for the logic delay. This means that the average logic delay need to be 22 ns, for the Pattern Generator to operate at the desired 2 MHz.

5.7 Conclusions

This chapter described the process of the design and implementation during the development of the E-Paper Display Driver. The main focus was on the implementation of the digital circuits, following the automated design flow. Three distinct implementation stages were defined: writing functional HDL code, synthesis and layout. Although these stages were discussed in different sections it may seem that they are decoupled, this was certainly not the case during development. The implementation is an iterative process, where it sometimes is needed to go back to improve the design.

From the implementation of the digital components, the following points are highlighted:

- Structured HDL, dividing the Gate Driver and Data Driver is small unit drivers Gate Unit and Data Unit. The layout stage will benefit from this. By just making the layout of the unit drivers, the majority of the work for the layout of Gate Driver and Data Driver is already done then.
- At the synthesis stage, it is possible to manipulate the organization of the design. For example by grouping loose components in to a subdesign, or un-grouping a subdesign in to loose components. The result is to get a balance of the right logic optimizations without creating chaos and subdesigns that are approximately the same size and complexity for a simpler layout.
- At the layout stage a manual-place automatic-route approach is presented. Designs that have parallelism or regular structures may benefit from this approach. Automatic placement by computer may fail to exploit the regularity for a compact layout.
- Automatic placement is more useful for finite state machines and control flow structures, where regularity or structure is hard to identify in the schematics. Automatic placement will save the time and effort of the designer.

Verification
Throughout out the design process, there are certain milestones where the design is checked, tested and verified for its correct operation and to confirm that the work up till now is still correct. This was mainly done using logic simulations. After making the layout of the components, an LVS check and an DRC is done.

The Timing Analysis
The timing parameters of the Standard Cell Library still need to be determined by simulation and measurements. A 51 stage Ring Oscillator was build using the SG inverter. With this circuit the average logic gate delay can be determined. A calculation is made, based on the longest logic chain present in the counters of Pattern Generator. This chain consist of 18 logic gates. An average logic gate delay of 22 ns is required for the Pattern Generator to operate at 2 MHz. Expected is that the Display Driver will be able to operate at higher frequencies compared to the Pattern Generator, due to the simpler design. In the worst case, we will have to operate at a lower frequency.

6 Test Circuits

Several test circuits have been manufactured with the SG-TFT Technology. Among these test wafers, there are test circuits for the high voltage TFTs, low voltage digital logic, pixel array (5×5 Active Matrix Backplane) and others. In this chapter the digital test circuits are discussed together with the measurement results.

In Section 6.1 the digital test circuits are described. The digital test circuits are: Ring Oscillator (Subsection 6.1.2), 4 bits counter (Subsection 6.1.3) and a test circuits with Logic Cells of the Standard Cell Library (Subsection 6.1.4). The results of the measurements taken from these circuits are presented in Section 6.2. In Section 6.3 an explanation is given for the subpar results. The conclusions from the results are drawn in Section 6.4.

6.1 Digital Circuits

Instead of directly sending the E-Paper design to the manufacturer, it was decided to make a test chip first. On this chip several circuits and process techniques are tested. The results are then used to change and improve the E-Paper design. The test chip include test circuits for the high voltage TFTs, pixel array and other test circuits. Because there was spare space left on the chip, a last minute decision was made to include test circuits for low voltage digital logic. A selection of digital circuits was designed, these digital designs were then synthesized and the layout was made. The design of these circuits followed the automated design flow, and used the cells from the Standard Cell Library. The following digital circuits were made: Ring Oscillator, a 4 bits counter and a test circuits to test the Logic Cells of the Standard Cell Library. The test plan can be found in Appendix A, photos of the fabricated chip can be found in Appendix B.

6.1.1 Output Buffer

An output driver was designed, to drive the output signals with sufficent strength. A single logic gate is not strong enough to drive a large load with the enough speed. As a result, the load of a measuring probe could influence the oscillation of the ring oscillator. By using an output buffer to strengthen the output signal, it is then possible to measure the ring oscillation without the probe influencing the frequency too much. The same output driver is used for the other designs as well, making the output signal stronger for the measuring probe.

This output buffer was designed before the buffer cells were available in the Standard Cell Library. The output buffer is made using four inverter stages. An even number of inverter stages is needed to avoid an inverted output. The output buffer is configured with the following number of parallel inverters per stage: 2, 4, 16, 64. The delay of the

buffer is kept to a minimum by increasing the number of inverters per stage. Ensuring that each stage will have a load that is able to drive with enough speed. The fan-out 4 (FO4) delay metric [37] is used here. The delay of a logic gate with a fan-out of 4 (driving 4 other gates) is the same for stages 4, 16 and 64.

6.1.2 Ring Oscillator

A ring oscillator was designed to determine the inverter gate delay t_p. The ring consists of an odd number of inverters, connected to each other from output to the input of the next inverter. The oscillation period T is determined by the signal propagation time through the complete chain of inverters, or $T = 2 \times t_p \times N$ with N inverters in the chain. A full clock cycle consist of two signal transitions, low-to-high and high-to-low, resulting in the factor 2. A 51-stage ring oscillator was designed and connected to an output buffer. The output buffer is needed so that the measurement probe will not influence the oscillation. An output buffer with enough speed and strength will produce a full-swing oscillation signal. It might be possible that buffer is over dimensioned, and having 64 parallel inverters is too much. The intermediate signals of the buffer inverter stages are equipped with test pads. Allowing measurements to be done on the intermediate buffer signals, to determine the minimal number of parallel inverters needed for a proper oscillation signal.

6.1.3 4 bits Counter

To test the automated design flow, a 4 bits counter was designed. This designs starts off as behavior level VHDL, which then gets translated to the logic gates of the Standard Cell Library. From the resulting netlist a layout is made. A 4 bits counter as design is chosen, because it uses all the basic logic gates that the Standard Cell Library has to offer: inv, nand2, nor2 and dff. The four outputs corresponding to the 4 bits are all buffered using the output buffer.

6.1.4 Logic Cells

In case the previous test circuits fails, another test circuit is made. This test circuits only tests the loose logic gates of the Standard Cell Library. The logic gates inv, nand2, nor2 and dff are equipped with test pads for the inputs and each gate output has its own output buffer, seen in Figure 6.1.

6.2 Test Results

The first measurements on the digital test circuits were very disappointing. The Ring Oscillator had a very weak output signal, an peak-to-peak signal of 120 mV. At that time we could not conclude if this was the oscillation of the Ring Oscillator or whether it was noise. The first measurements of the inverter test circuits showed a non inverted behavior. This test circuit consist, of only an inverter, with an output driver connected to the output pin. By placing the needle of the probe on a output wire of the inverter, the output driver was by passed and a inverted behavior was observed. A conclusion

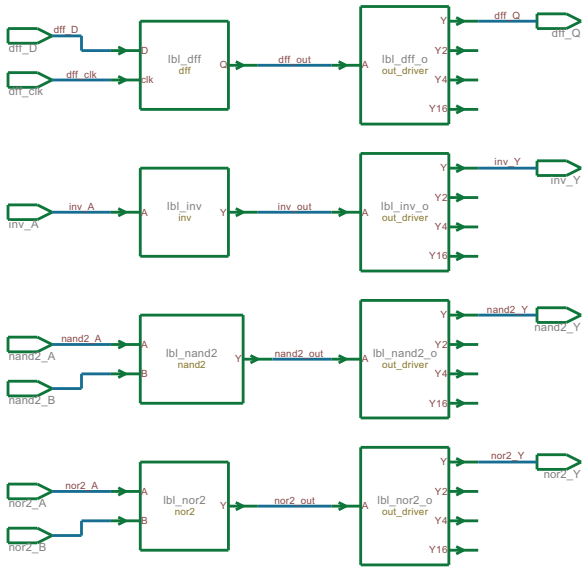

Figure 6.1: Logic gates from the Standard Cell Library, each with an output driver connected to its output.

was drawn that the output driver did not work properly (more on this can be read in Subsection 6.3).

The following subsections will present the measured results. The results of the Ring Oscillator can be found in Subsection 6.2.1 and the measurement results of the Logic gates are found in Subsection 6.2.1. Unfortunately we were unable to verify the correct operation of the 4 bits counter, more on this can be read in Subsection 6.2.3.

6.2.1 Ring Oscillator measurement results

The 51-stage Ring Oscillator is connected to an output driver. Only for the Ring Oscillator test circuit, the intermediate buffer stages are available as test pads. These are labeled as follows: Y2, Y4, Y16 and Y (the main output of the buffer). The number reflects the number of parallel inverters connected to the test pad. 2, 4, 16 and 64 parallel inverters are connected to the test pads Y2, Y4, Y16 and Y respectively as seen in Figure 6.2.

The first measurements were done with a 1:10 probe. On die 1, measurements were taken at the different output pins. These pins correspond to the intermediate buffer stages and the main output stage. The results are seen in Table 6.1. The Ring Oscillator is power by a 5V power supply. We can see that the signal are stronger at pins Y4 and Y16, when comparing to Y2. The output on Y16 and Y do not show significant difference, most likely due to a short circuit in the last stage. The oscillation stays around the same frequency range, this is expected since the supply voltage does not change.

The output Y2 and Y4 of die 2 at 5V were measured without probe and plotted in Figure 6.3. The wave form shape remains intact, the difference here is in the amplitude of the signal.

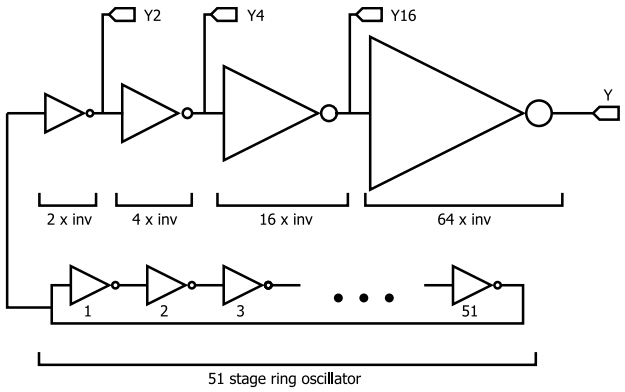

Figure 6.2: Schematic of the 51-stage Ring Oscillator with intermediate output buffer signals.

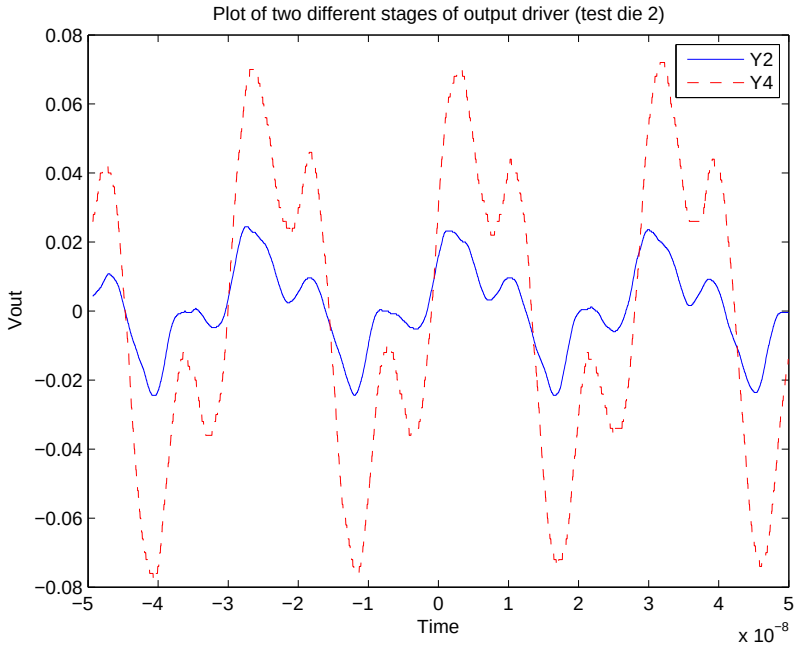

Figure 6.3: Die 2 at 5V, directly measured with an oscilloscope on output Y2 and Y4.

Table 6.1: Die 1 at 5V measured with a 1:10 probe on different output pins.

Output pin	**Frequency(MHz)**	**Pk-Pk(mV)**	**Gate Delay(ns)**
Y2	37.1	85	0.26
Y4	37.1	195	0.26
Y16	36.3	430	0.27
Y	36.0	420	0.27

Table 6.2: Ring Oscillator measurement results of 3 dies.

Die	Supply(V)	Frequency(MHz)	Pk-Pk(mV)	Gate Delay(ns)
die 2	5*	33.0	130	0.30
	7*	44.0	176	0.22
	10†	-	-	-
	9‡	53.9	240	0.18
die 3	5	35.0	208	0.28
	7*	46.5	230	0.21
	8*	51.3	410	0.19
	9†	-	-	-
	8*‡	50.5	528	0.19
die 4	5	32.2	120	0.30
	7	42.8	210	0.23
	8	47.2	250	0.21
	9	50.9	456	0.19
	10†	-	-	-

Measurements were taken from three different dies. We measured the oscillation frequency and peak-to-peak value of the output signal with different supply voltages. All output signals were measured directly from the Y2 pin, this time without a 1:10 probe. At output pin Y2, two parallel inverters are buffering the oscillation signal from the Ring Oscillator. The oscillation frequency is dependent on the applied supply voltage. When applying a supply voltage that is too high, the output signal collapses. This may be explained by transistor breakdown. After decreasing the supply voltage, the Ring Oscillator continued to work, but there was a difference observable. This can be seen in results of Table 6.2. The output wave form shape is different per die, and is also dependent on the applied voltage. Some of the entries in Table 6.2 are plotted in Figure 6.4. Different wave form shapes of two dies can be seen in this figure, the supply voltage has a clear influence on the shape here. This figure also includes the wave form shape before and after the overvoltage of the Ring Oscillator on die 3.

*The signal of these conditions can be found in Figure 6.4.

†At this supply voltage, the output voltage collapsed. This may indicate that breakdown had occurred in the transistors.

‡After the overvoltage, the ring oscillator still works but the results were different.

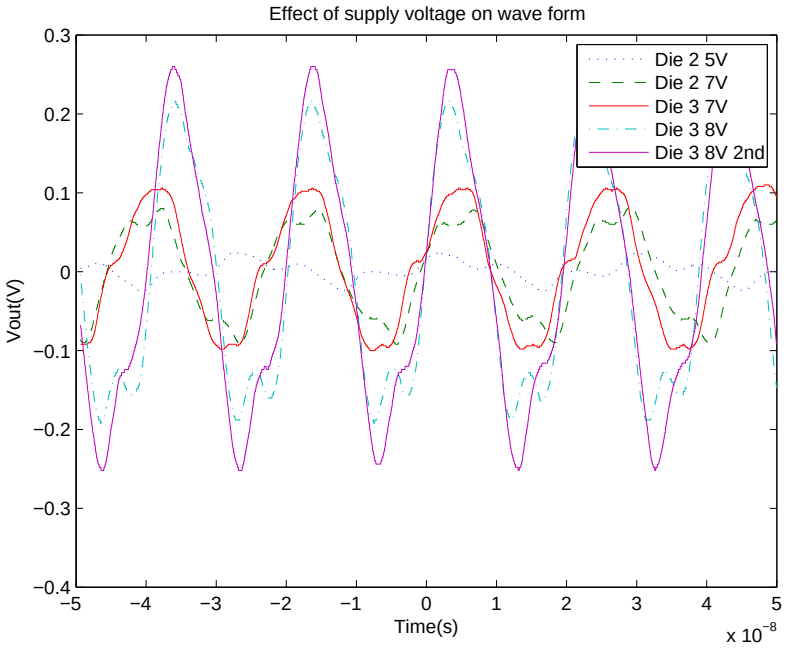

Figure 6.4: Different oscillation wave form shapes, dependent on applied voltage and differs from die to die. The effects before and after overvoltage is seen in the two plots of die 3 at 8V.

6.2.2 Logic Gate measurement results

The basic logic gates of the Standard Cell Library are tested individually. Due to a short circuit in the output driver (for details see Subsection 6.3), the output driver is bypassed. This was done by placing the measuring probe on the output wire of the logic gate. Voltage Transfer Characteristics (VTC) of the logic gates inv, nand2 and nor2 were obtained by DC measurement.

6.2.2.1 The Inverter

The simplest logic gate is the inverter. To determine the Voltage Transfer Characteristics of the inverter, the output voltage V_{out} is measured as function of the input voltage V_{in}. An example of an inverter VTC plot is seen in Figure 6.5. The switching threshold voltage V_M is found by the intersection of V_{out}=V_{in} with the VTC curve. The high and low nominal voltages, V_{OH} and V_{OL}, can be identified in the plot. Two more points of interest are found in this figure. These are V_{IH} and V_{IL}, they indicate the two points where the slope equals -1 of the VTC curve. With these parameters the high and low noise margin can be determined:

$$NM_L = V_{IL} - V_{OL}$$
$$NM_H = V_{OH} - V_{IH}$$

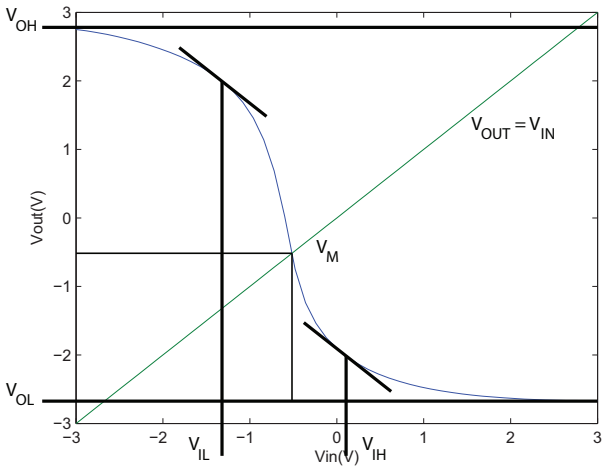

Figure 6.5: Inverter voltage transfer characteristic.

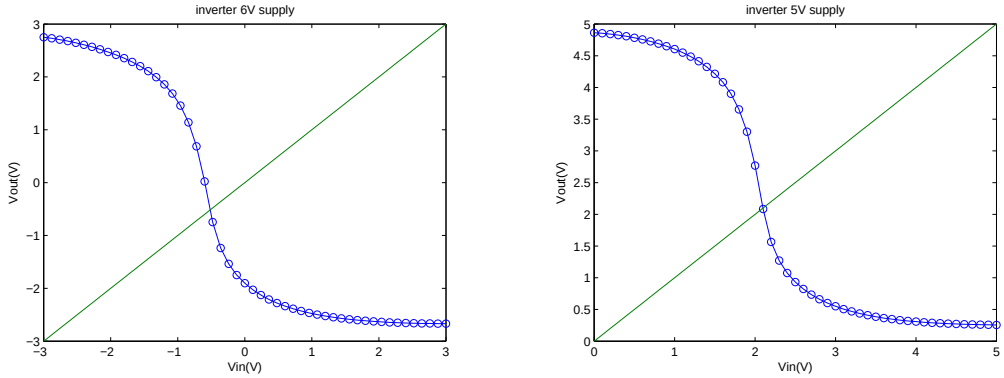

Figure 6.6: Voltage Transfer Characteristics of the inverter. On the left V_{dd}=3V and V_{ss}=-3V; On the right V_{dd}=5V and V_{ss}=0V.

Two measurements are plotted in Figure 6.6. On the left the applied voltages are: V_{dd}=3V and V_{ss}=-3V. And on the right: V_{dd}=5V and V_{ss}=0V. The measurements were taken from the same inverter. From the plot we can see that the negative voltage on V_{ss} does not effect the voltage transfer characteristics. The plots are similar, but there is a small difference due to the difference in voltage potential 6V versus 5V. We can determine the inverter parameters. The results are seen in Table 6.3. The switching threshold voltage V_M is a bit on the low side. This is most likely due to the difference in threshold voltage of the P-type and N-type channel. Ideally V_M should be in the middle of the supply voltage, 0V and 2.5V respectively for the two test cases. The result of a shifted V_M is seen back in the high and low noise margin. The noise margin low NM_L is smaller compared to the noise margin high NM_H.

Table 6.3: Inverter parameters with two different supply voltages. All values are in Volts (V)

Supply	$\mathbf{V}_M$	$\mathbf{V}_{OH}$	$\mathbf{V}_{OL}$	$\mathbf{V}_{IH}$	$\mathbf{V}_{IL}$)	$\mathbf{NM}_L$	$\mathbf{NM}_H$
3;-3	-0.5	2.8	-2.7	0.12	-1.4	1.3	2.68
5;0	2.1	4.9	0.2	2.6	1.35	1.15	2.3

6.2.2.2 Logic gates nand2 and nor2

The logic gates nand2 and nor2 are more complex than the inverter. These logic gates have two input pins. A VTC plot similar to the inverter can be obtained by changing only one of the pins. The measurements were taken with supply voltages of V_{dd}=3V and V_{ss}=-3V, the results are seen in Figure 6.7. For convenience the truth table of these logic gates can be found in Table 6.4. From the plot results we can conclude that these logic gates are functional and show a behavior that is consisted with their function.

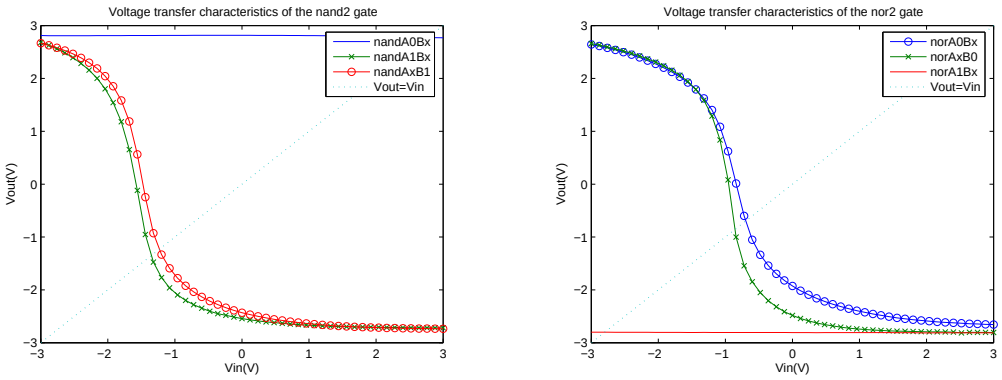

Figure 6.7: Voltage Transfer Characteristics of the nand2 and nor2 logic gate. The x indicates the pin that is being changed.

Table 6.4: Truth table for nand2 and nor2.

nand2			**nor2**		
A	B	Y	A	B	Y
0	0	1	0	0	1
0	1	1	0	1	0
1	0	1	1	0	0
1	1	0	1	1	0

From the plot in Figure 6.7 we can extract the different parameters for comparison, see Table 6.5. Again we can notice that the switching threshold voltage V_M is a bit on the low side. With the supply voltages V_{dd}=3V and V_{ss}=-3V, an ideal V_M should be 0V. The V_M of the tested nand2 is actually too low, the noise margin low NM_L is less than 0.5V, such a low noise margin makes the circuit more vulnerable to noise and less reliable. It might be caused by a bad device or a mismatched in the NMOS-PMOS TFT pair.

Table 6.5: Parameters for the logic gates inv, nand2 and nor2. All values are in Volts (V)

test case	$\mathbf{V}_M$	$\mathbf{V}_{OH}$	$\mathbf{V}_{OL}$	$\mathbf{V}_{IH}$	$\mathbf{V}_{IL}$	$\mathbf{NM}_L$	$\mathbf{NM}_H$
invAx	-0.5	2.8	-2.7	0.12	-1.4	1.3	2.68
nandA1Bx	-1.3	2.7	-2.8	-1.0	-2.3	0.5	3.7
nandAxB1	-1.2	2.7	-2.8	-0.8	-2.2	0.6	3.5
norA0Bx	-0.7	2.7	-2.7	-0.1	-1.6	1.1	2.8
norAxB0	-0.8	2.7	-2.8	-0.4	-1.6	1.2	3.1

6.2.2.3 D-Type Flip-Flop

The D-Type Flip-Flop (dff) cannot be tested using DC measurements. Instead two pulse generators were connected to the flip-flop, and the output was measured with an oscilloscope. From observations we saw that the Flip-Flop worked. The dff was able to latch the data on the rising edge of the clock pulse. Unfortunately the measuring data was not saved properly, so no plot can be shown of this measurement.

6.2.3 The 4 bits Counter results

The measurements on the 4 bit counter were not successful. Each pin of the 4 bits output can be seen as a clock divider. When measuring each of the 4 bits directly (without output buffer), the expected frequency dividing behavior was not observed. Sometimes the output signal had the same pulse width as the applied clock, this should never happen. Even on the least significant bit, bit 0, the minimal pulse width should correspond to a whole clock period. Effectively dividing the clock frequency in two. We can confirm the functionality of the reset pin, when a logic 1 was applied to this pin, the output signals stayed at the logic value 0.

Extensive tests are needed to pinpoint the exact reason for the failure of this digital circuit. At this time, there are a few reasons thinkable, that might cause this circuit not to work properly.

1. **Bad layout.** Similar to the output driver (see Section 6.3) the layout might not work due to DRC violations. Inspection on the layout file show that there are indeed DRC errors. But there was no DRC error found that can cause a short circuit, like in the case of the output driver.

2. **Probe influence.** It is possible that the load of the probe influences the circuit. Measurements were taken directly from the flip-flops. It is possible that the probe affects the output voltage of these flip-flops, forcing it into an undefined region. The subsequent gates misinterprets this logic value and the circuit will not function properly.

3. **Transistor failure.** Because the measurements were by bypassing the output driver, it takes some effort to place the test needle correctly, in contrast to probing a test pad. This was the reason that we only tested one die, it could be possible that this die had a faulty circuit.

The reasons given here are all related to the realisation of the circuit. So far we are assuming that the logic design is correct. The design files were double checked to make sure this was the case. Netlist simulation of the synthesized design, show that the circuit behaves as it should. According to the LVS (Layout Versus Schematic) check, the layout corresponds to the schematic of the netlist. But the layout still contains DRC violations.

6.3 Short Circuit

From the first set of measurements, suspicion grew that the output driver was not working accordingly. After looking at the layout file of the design, our suspicion was confirmed. Two wires of separate nets were placed too close to each other. The manufacturer cannot handle the clearance, and most likely, this resulted in a short circuit. In Figure 6.8 two DRC violations can be seen, the violation on the right is the short circuit in the output driver. The output wire on that inverter is routed too close to the input of the same inverter. This inverter is one of 64 inverters of the last buffer stage. The short circuit in this inverter make the last two stages of the buffer useless.

During the layout stage of the test circuits, the DRC violations were ignored. The reason was that the designs were full of wire DRC violations, and was caused by the auto router. In Figure 6.9 the DRC violations of the output driver are highlighted. When inspecting some of the violations, it was found that they all belong to the same type of violation. A clear example can be seen on the left of Figure 6.8. The wire that runs horizontally is too close to the square shaped via. Since the wire and the via are of the same net, this should not cause any trouble. They should be connected anyway. Most of the DRC violations are of this type. At that time a decision was made to ignore these DRC errors, since they seem harmless. This turned out to be disastrous for the output driver, the large number of *false* DRC violations overclouded the DRC violation that eventually led to a short circuit.

It is not responsable to ignore these DRC errors for future designs. A solution needs to be found to avoid the *false* DRC violations, so that they will not hide the DRC violations that will causes short circuits for example. An assumption was made that the auto router does not produce any routings where short circuits can occur. A solution might be by changing the DRC rules, so that checker will not give any *false* DRC violations. A better solution is to change the auto router. By including all of the DRC rules in to the routing rules. The idea is that the router will not route in such a way that it can violate the DRC rules.

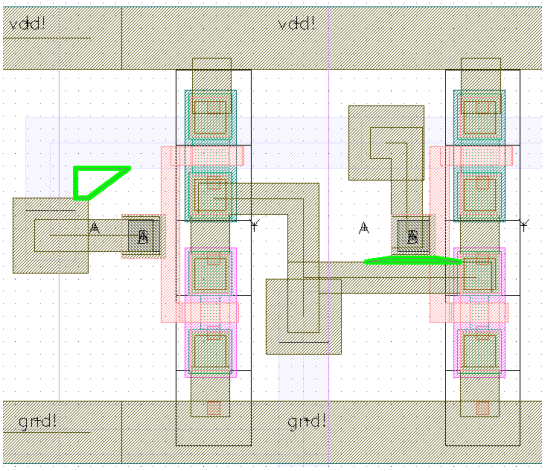

Figure 6.8: Left: 'false' DRC error. Right: DRC violation leading to a short of two different nets.

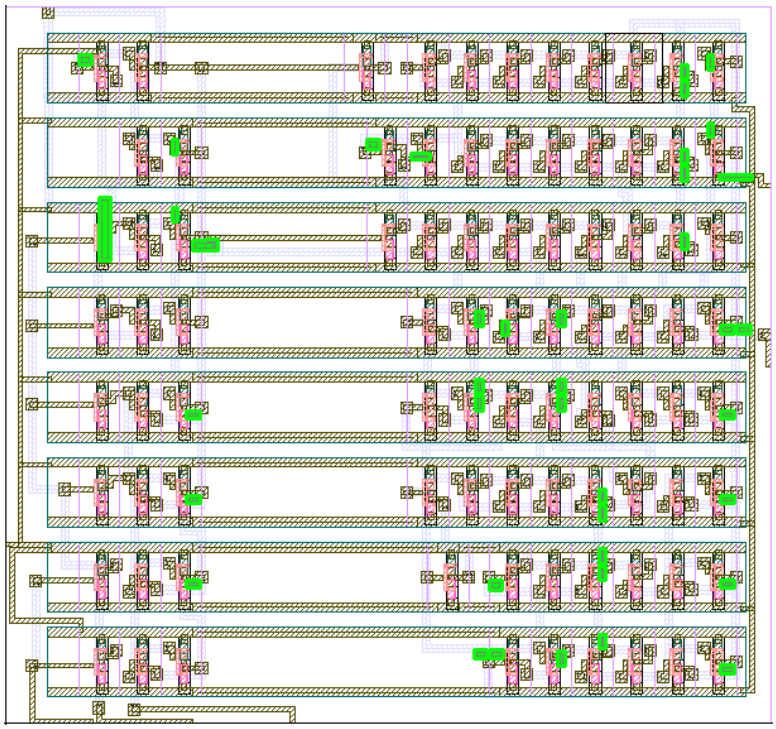

Figure 6.9: The layout of the output driver, the DRC violations are highlighted.

6.4 Conclusions

The digital test circuits that were designed in a short time frame of two days, were not completely successful. Despite this, we were still able to gather valuable information on the logic cells of the SG Standard Cell Library. Three test circuits were designed: The

Ring Oscillator, for determining the inverter propagation delay; The 4 bits Counter to verify the automated design flow; The Logic Gates from the Standard Cell Library, to test the logic gates individually.

The Ring Oscillator
The measurements on the Ring Oscillator were done using only the first stage of inverters pin Y2. The last two stages were not reliable due to a short circuit in the last stage. Measurements were taken from different dies and all of them show an oscillation frequency around same region, 30 MHz to 50 MHz, dependent on the die and supply voltage. Full swing output signal is expected with a fully operational output buffer. It is not clear if the current buffer configuration is strong enough to achieve the full swing. The inverter propagation delay is determined, from the measurements of the Ring Oscillator. The SG inverter has a propagation delay of 0.30 ns or less at 5V. Lower gate delay values of 0.19 ns was observed when increasing the supply voltage to 9V. It seems that we are able to reach our desired operating frequency of the E-Paper Display. An rough estimation was made that 22 ns or less is required as logic gate delay, in order to operate at a clock frequency of 2 MHz. The inverter gate delay is two orders of magnitude faster than the minimal requirement.

The Logic Cells
The basic logic gates of the Standard Cell Library are tested individually. The output driver was bypassed because of the short circuit. This was done by placing the measuring probe directly on output wire of the logic gate. Voltage Transfer Characteristics (VTC) of the logic gates inv, nand2 and nor2 were obtained by DC measurement. From the VTCs of the logic gates, the different parameters are extracted. What was clearly observed is that the switching threshold voltage V_M is a bit on the low side. This might be adjustable by changing the dimension of the PMOS and NMOS. The V_M of the tested nand2 gate is even lower than expected, it might be cause by process variations. Further testing is desired. From all the tested logic cells, we can conclude that they were behaving as expected.

The 4 bits Counter
The measurements on the 4 bits Counter did not show a fully operational circuit. More extensive testing is required to pinpoint the exact reason of this. At this time, there are three possible causes thinkable: Bad layout; The probe influences the circuit; Transistor Failure.

Overall, we were still able to collect valuable information on the digital test circuits, despite the short circuit in the layout of the output driver. Further tests are required to determine the quality of the process, by gathering enough data from different dies to extract the parameter variations of the SG-TFTs. The results of the DRC check cannot be ignored. The DRC rules or the router rules need to be changed to avoid short circuits in future designs.

7 Current State of Development

In this chapter the current state of the development of the E-Paper Display is discussed. In Subsection 7.1 the progress of the whole E-Paper project is described, some components are finished, other components need the results of the test circuits for completion. In Section 7.2 the bachelor project Super E-Paper is presented. Once the E-Paper prototype is finished it can be used as a part of Super E-Paper. And finally some suggestions are given for future designs with SG-TFTs, and what still needs to be done to complete the SG-TFT E-Paper Display.

7.1 Progress

At the time of writing this thesis, we do not have a finished working E-Paper yet, even though it is one of the goals for this thesis. At this moment, measurements are taken from the fabricated SG test wafers. In these wafers, there are test circuits for the high voltage TFTs, low voltage digital logic, pixel array and others. Several versions of these high voltage TFTs were made. With different LDD length, gate oxide thickness and oxide types. The different high voltage TFTs are measured for their characteristics and performances, this will determine the final high voltage TFT that will be used for the E-Paper Display.

The pixel array is a small 5×5 Active Matrix Backplane. The schematic looks similar to the one illustrated in Figure 3.2, with a small difference in the schematic. The NMOS transistor is coupled with a PMOS transistor to a pair, a so called transmission gate. Several of these small pixel arrays will be shipped off to Bridgestone in Japan. Bridgestone will then further process it, by gluing a small piece of QR-LPD material on top of the circuit.

From the measurements on the digital test circuits we can conclude that the logic gates of the Standard Cell Library are all functional. VTC plots are made from the DC measurements on these logic gates. The inverter propagation delay was determined by measuring the oscillation frequency of the Ring Oscillator circuits. The 4 bits counter that was designed using the automated design flow is not fully operational. Further tests are needed to pinpoint the exact cause.

All of the digital components are finished, they just have to be connected to each other to form the complete layout of the E-Paper Display. The high voltage component Active Matrix needs some adjustment depending on the measurements of the high voltage SG-TFTs. Once the high voltage SG-TFTs are finalized, the component Level Shifter can be made and the DAC can be finalized. The low voltage part of the DAC is already finished.

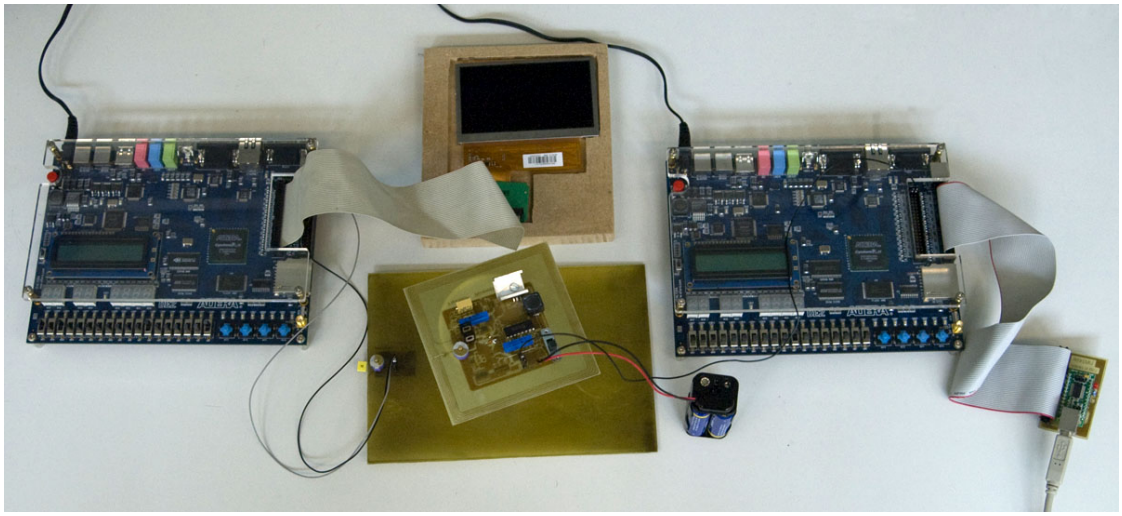

Figure 7.1: Super E-Paper prototype: image data is send from PC via USB to the right FPGA. It then gets transmitted in a wireless fashion to the second FPGA on the left, connected to a LCD screen instead of an E-Paper screen.

7.2 A Practical example Product: Super E-Paper

A group of Bachelor students were given the assignment to design and develop a product that will use this E-Paper. They noticed that the bus schedules and advertisement posters in the bus stops, take a lot of time and effort to change. To make this easier they came up with the product Super E-Paper. Super E-Paper will replace the traditional paper schedules and posters. Updating the content of the display will be done in wireless way, and because the E-Paper is bistable, the content will not change after the update. The bus stops will not have to be modified to accommodate Super E-Paper.

In Figure 7.1 a picture can be seen of the developed prototype. It consists of several key components. A computer is used to send the image information to the USB component. This is connected to the FPGA on the right, that then sends it to the transmitter. The transmitter modulates the information on a 13.56 MHz carrier. The receiver is the bigger circuit board under the transmitter seen the picture, and it is connected to the left FPGA board. This decodes the signal and extracts the valid image data, which then gets forwarded to the E-Paper. Unfortunately, no E-Paper was available at that time, so an alternative solution was used. The send image is displayed onto a LCD screen instead.

The students approached the bus company Connexxion to propose their product Super E-Paper. The company was very excited by the idea and wanted to know more about this product.The advantage of wireless updating the content of the Super E-Paper saves the company a lot of time and effort when changing the bus stop schedules. Also, Connexxion has a lot of remote bus stops, where power is not available. Super E-Paper retains the image without power. A very appealing feature for the bus company Connexxion.

7.3 Considerations for Future SG Designs and Future Work

In this section some pointers are given, for designers that want to design digital circuits in the SG Technology. This is based on the work and experience obtained from this thesis. To improve the digital circuit design for the Single Grain Technology, some points of improvement are listed here in this section.

When using the Standard Cell Library for digital designs, try to keep the design structural. This can be done by using labels in VHDL and by splitting the design into subcomponents. This will make the design easier to layout and the possibility to reuse of previously designed components. When making the layout for the design, do not ignore the DRC checker.

The Standard Cell Library might need some small changes.

- The gates of the SG-TFTs need to be extended. Lengthening the gate will improve the alignment tolerances and over exposure. Improving the process yield.
- Enlarge the P-select and N-select to improve the the alignment tolerances. With the same idea of improving the process yield.
- Make sure the *single grain*, that contains the transistor channel, is surrounded by other *single grains*. This will make a grid, and the *single grain* at the center will have a better crystal structure for the transistor channel.

To finalize the E-Paper prototype, a few things still need to be done. More measurements need to be done on the fabricated wafers. From these measurement we can extract the information needed for the high voltage TFTs for example. Some of the pixel array circuits are going to be shipped to Bridgestone. They will glue the QR-LPD on top of the array and measurements can be done with this E-Paper material. From these tests we can verify that the we can control the Liquid-Powder particles using the SG-TFTs.

The DRC rules and router rules will need a revision. By including the DRC rules in to the router rules, it will be possible to make the router produce wire routing that will not violate the DRC rules.

The Level Shift component still needs to be made and the DAC component needs to be finalized. These components are high voltage components and use the high voltage SG-TFTs. The work needed for these component is not much, the Level Shifter is a simple circuit and the most of the DAC design is finished already.

Once all the components are done, the complete layout can be made. Including the low voltage and the high voltage components. Some extra attention is needed for connecting the high voltage power wires to the high voltage components. The high voltage supply wires need to be routed through the reserved spaces in the Gate Driver and Data Driver.

8 Summary

The E-Paper Display is an combination of two new technologies. The technology details are described in Chapter 2. The SG-TFT technology is used to make high performance transistors out of a-Si (amorphous silicon) by Excimer-laser crystallization. The electrical performance of these SG-TFTs is comparable to single-crystal transistors. These TFTs can be used for analog, RF circuits and digital. All the fabrication steps can done at relatively low temperatures (<350°). This makes the SG-TFT Technology suitable for electronics on glass substrate or cost effective plastic substrate for flexible electronics. It is even possible to stack TFTs on top of each other, for making 3D chips.

The Quick-Response Liquid Powder Display (QR-LPD) is used as the E-Paper material. QR-LPD is developed by Bridgestone and has a paper-white appearance with high contrast and high reflectivity, suited for making E-Paper Displays. The QR-LPD uses a new developed Liquid-Powder. This powder is electrical sensitive and combines the properties of both powder and liquid. The powder particles can move fast through the air within the cell, resulting in an ultra fast pixel response time of 0.2 ms. The QR-LPD requires a relative high driving voltage of 70V with a clear threshold voltage of 35V. The bistable nature of the Liquid-Powder makes the QR-LPD retain its image after writing and even when there is no power at all.

Based on the constraints and properties of QR-LPD and knowing the limits of the SG-TFT technology, different ways to control the E-Paper material are possible. Chapter 3 discusses these different aspects and the E-Paper Display concepts are presented that form the basis for the implementation of the Display components. The display interface is specified, based on similar signals found in controlling VGA screens. Although they look similar, they are not compatible. The interface is synchronized with two synchronization signals, horizontal *hsync* and vertical *vsync* similar to VGA timing signals. The desired E-Paper specifications are presented. We want to design a monochrome E-Paper Display with a screen format of 320×240 pixels (QVGA). Each pixel will have 64 gray-scale levels (6 bits) and will be 150×150 μm big. The viewable screen size will be 4.80×3.60 cm. Our aim is to reach 25 frames per second, making it possible to view movies and animations fluently. This means that the display system clock frequency will be at least 2 MHz.

Chapter 4 discussed the different aspects that had to do with the implementation of the E-Paper Display Driver. First a Display Organization block diagram was made. In this diagram, all of the components of the Display Driver can be found. A distinction was made between Low Voltage and High Voltage components. The Low Voltage components are all digital components designed with the automated design flow, using the SG Standard Cell Library. The digital components implemented are Display Driver, and two components that are more related to testing: Pattern Generator and Ring Oscillator. The Display Driver subcomponents Gate Driver and Data Driver are divided into Unit Drivers, responsible for only a single row or column respectively. This will reduce

the work later on, when doing the layout of these components. Pattern Generator is not part of the Display Driver, but instead it can act like a build in self test. Pattern Generator is capable of generating display signals suited for the Display Driver. A test pattern is included to verify the Displays basic functionality. Two features have been implemented, the *Programmable Erase Vector* and the *Variable Sync Time*. With these features it is possible to determine the correct settings for proper use of the Movie Mode with the Erase before Write scheme.

The High Voltage components are high voltage analog circuits made with the special designed high voltage SG-TFT. The Active Matrix Backplane forms the electrical interface with the Liquid-Powder particles. Two High Voltage components are connected to the Active Matrix Backplane. These components form the interface with the Low Voltage digital components and the high voltage Active Matrix Backplane. The Gate Driver is connected to the backplane via High Voltage Level Shifters, transforming low voltage 5V digital signals to high voltage 70V signals. The Data Driver is connected to the backplane via Digital to Analog Converters (DACs). A current driven DAC architecture is used. With this architecture the DAC combines two functionalities in one device, interface between Low Voltage and High Voltage, and the conversion of digital signals to an analog out signal. The DAC is a 6 bits DAC, capable to output 64 voltages in the range between 35V and 70V.

Two E-Paper simulators were implemented, a software based simulator and a hardware based simulator. The simulators can be used for testing, verification and development purposes.

Chapter 5 described the process of the design and implementation during the development of the E-Paper Display Driver. The main focus was on the implementation of the digital circuits, following the automated design flow. Three distinct implementation stages were defined: writing functional HDL code, synthesis and layout. Although these stages were discussed in different sections it may seem that they are decoupled, this was certainly not the case during development. The implementation is an iterative process, where it sometimes is needed to go back to improve the design. Throughout these different stages, the design is continuously verified using simulations. At the layout stage, LVS and DRC checks are done to check if the layout still corresponds to the schematic and to check whether the layout meets the DRC rules.

Chapter 6 discussed the designed digital test circuits and the measured test results. Three test circuits were designed: The Ring Oscillator, for determining the inverter propagation delay; The 4 bits Counter to verifying the automated design flow; The Logic Gates from the Standard Cell Library, to test the logic gates individually. The SG inverter has a propagation delay of 0.30 ns or less at 5V. Two orders of magnitude faster than the estimated maximum gate delay of 22 ns, for the display to operate at a clock frequency of 2 MHz and achieve the desired 25 frames per second. From all the logic gates, a low switching threshold voltage V_M was observed while an V_M in the middle of the supply voltage is desired. DRC errors were ignored during the design of these test circuits, this has eventually led to a short circuit in the output driver. The results of the DRC check cannot be ignored for future designs. The DRC rules or the router rules need to be changed to avoid short circuits in future designs. By gathering enough data from future tests and measurements of different dies, we are able to determine the quality of

the manufacturing process.

At the time of writing this thesis, we do not have a finished working E-Paper yet, even though it is one of the goals for this thesis. At this moment measurements are still taken from the fabricated SG test wafers. A few of the test pixel arrays will be shipped off to Bridgestone. They will glue a piece of QR-LPD material on top and ship them back. With these pixel arrays we can test how well the high voltage SG-TFTs can control the Liquid- Powder particles. All of the digital components are finished. They just have to be connected to each other to form the complete layout of the E-Paper Display. The high voltage components await the results of measurements. Once the high voltage SG-TFTs are finalized, these components can be completed as well.

9 Conclusions

In this thesis we presented the design and development of our E-Paper Display prototype using the μ-Czochralski Single Grain TFT Technology for the integrated electronics. By controlling the E-Paper with the SG-TFT technology, it will be a nice demo platform to showcase the possibilities with this technology. High Voltage TFTs together with the rest of the Display Driver (both analog and digital), all made with the same process. The process steps can be done at relative low temperatures, which make it possible to fabricate the display on a plastic substrate for a complete flexible E-Paper Display. With the possibility to make 3-dimensional chips by stacking the SG-TFTs on top of each other, we can expect highly integrated circuits for mixed signals devices. The SG-TFT technology will offer promising applications in the near future, giving new dimension to high integration.

Main Contributions

The following contributions of this thesis can be assigned to the E-Paper project:

- An E-Paper Display Driver organization is presented, taking into account the requirements of the QR-LPD and given the constraints of the SG-TFT Technology.
- Following an automated design flow, the digital part of the Display Driver was implemented using the SG Standard Cell Library. The layout of most of the components is complete.
- Two E-Paper simulators were developed, for testing, verification and development purposes.
- Digital test circuits were designed and measured, resulting in valuable information on the logic cells of the SG Standard Cell Library. The inverter gate propagation delay was determined by measurements.

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Abbreviations

a-Si	-	amorphous-Silicon
buf	-	Buffer
c-Si	-	single-crystalline Silicon
CMOS	-	Complementary Metal-Oxide-Semiconductor
DAC	-	Digital to Analog Converter
dff	-	D-Type Flip-Flop
DRC	-	Design Rule Checker
E-Paper	-	Electronic Paper
EDA	-	Electronic Design Automation
FO4	-	Fan-Out 4
FPGA	-	Field-Programmable Gate Array
fps	-	frames per second
HDL	-	Hardware Description Language
inv	-	Inverter
ITO	-	Indium Tin Oxide
JFET	-	Junction gate Field-Effect Transistor
LDD	-	Lightly Doped Drain
LVS	-	Layout Versus Schematic
MOSFET	-	Metal-Oxide-Semiconductor Field-Effect Transistor
nand2	-	Two ports NAND gate
NMOS	-	N-type Metal-Oxide-Semiconductor
nor2	-	Two ports NOR gate
p-Si	-	poly-crystalline Silicon
PMOS	-	P-type Metal-Oxide-Semiconductor
QR-LPD	-	Quick Response Liquid Powder Display
QVGA	-	Quarter VGA
SG-TFT	-	Single Grain Thin Film Transistor
Tcl/Tk	-	Tool Command Language / GUI Toolkit
TFT	-	Thin-Film Transistor
USB	-	Universal Serial Bus
VGA	-	Video Graphics Array
VHDL	-	VHSIC Hardware Description Language
VTC	-	Voltage Transfer Characteristic

Test Plan for the SG-TFT Digital Circuits

A

There are three digital test circuits:

- ring_osc: 51-stage ring oscillator, with different output buffer strength.
- logic: 3 logic gates and 1 Flip-Flop
- count123: a four bit counter

If the individual tests of the circuits are successful, we can try to connect ring_osc to count123 directly and measure the results. We also can try different output buffer strength in this measurement.

Table A.1: Terminal pin names per test circuit.

ring_osc

out:	Y2
	Y4
	Y16
	Y
supply:	vdd!
	gnd!

logic

in:	nand2_A
	nand2_B
	nor2_A
	nor2_B
	inv_A
	dff_D
	dff_clk
out:	nand2_Y
	nor2_Y
	inv_Y
	dff_Q
supply:	vdd!
	gnd!

count123

in:	clk
	reset
out:	count_out[0]
	count_out[1]
	count_out[2]
	count_out[3]
supply:	vdd!
	gnd!

Minimal Measuring equipment requirements:

- At least 2 channel, 40MHz oscilloscope
- Some digital input stimuli, for at least two inputs at the same time
- Analog input stimuli, voltage between 0 and 5V
- Stabilized Power supply: at least 5V, best is a stabilized variable supply with minimal range of 0 to 10V

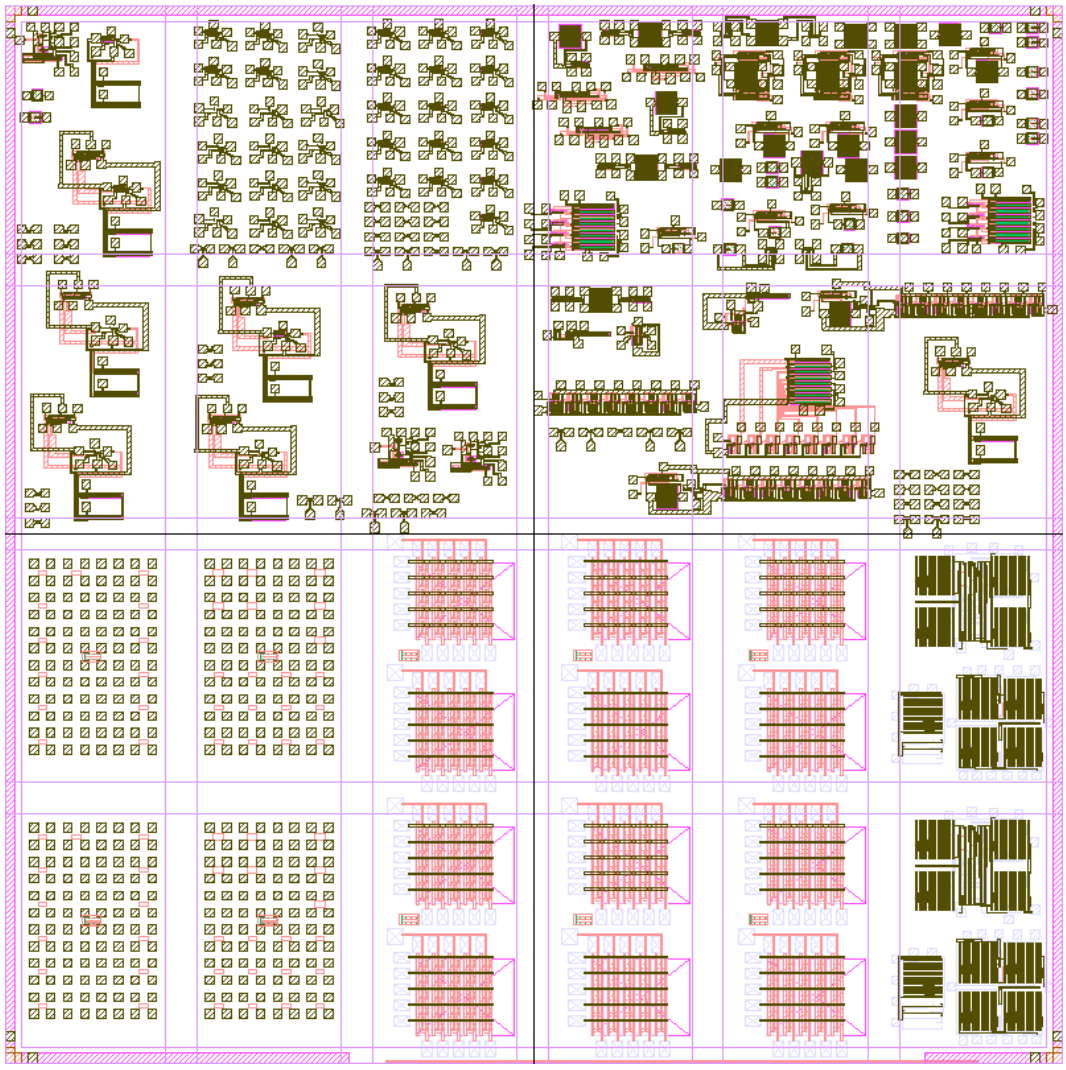

Figure A.1: Photograph of the complete die with different test circuits, the digital test circuits are located on the bottom right.

A.1 Test plan ring_osc

Measure the generated frequency at main output Y. Test the range of supply levels, for a rail-to-rail oscillation. Different output strength terminals are available as well. Y is the standard output buffer with 64 inverters in parallel. The Y2 with two, Y4 with four and Y16 with sixteen inverters in parallel.

Requirements for the outputs: At least one channel scope. The output frequency could be any anything, but my guess is that it would be slower than 16MHz, so the scope should be able to measure that. Sampling frequency of at least 40MHz to be on the save side

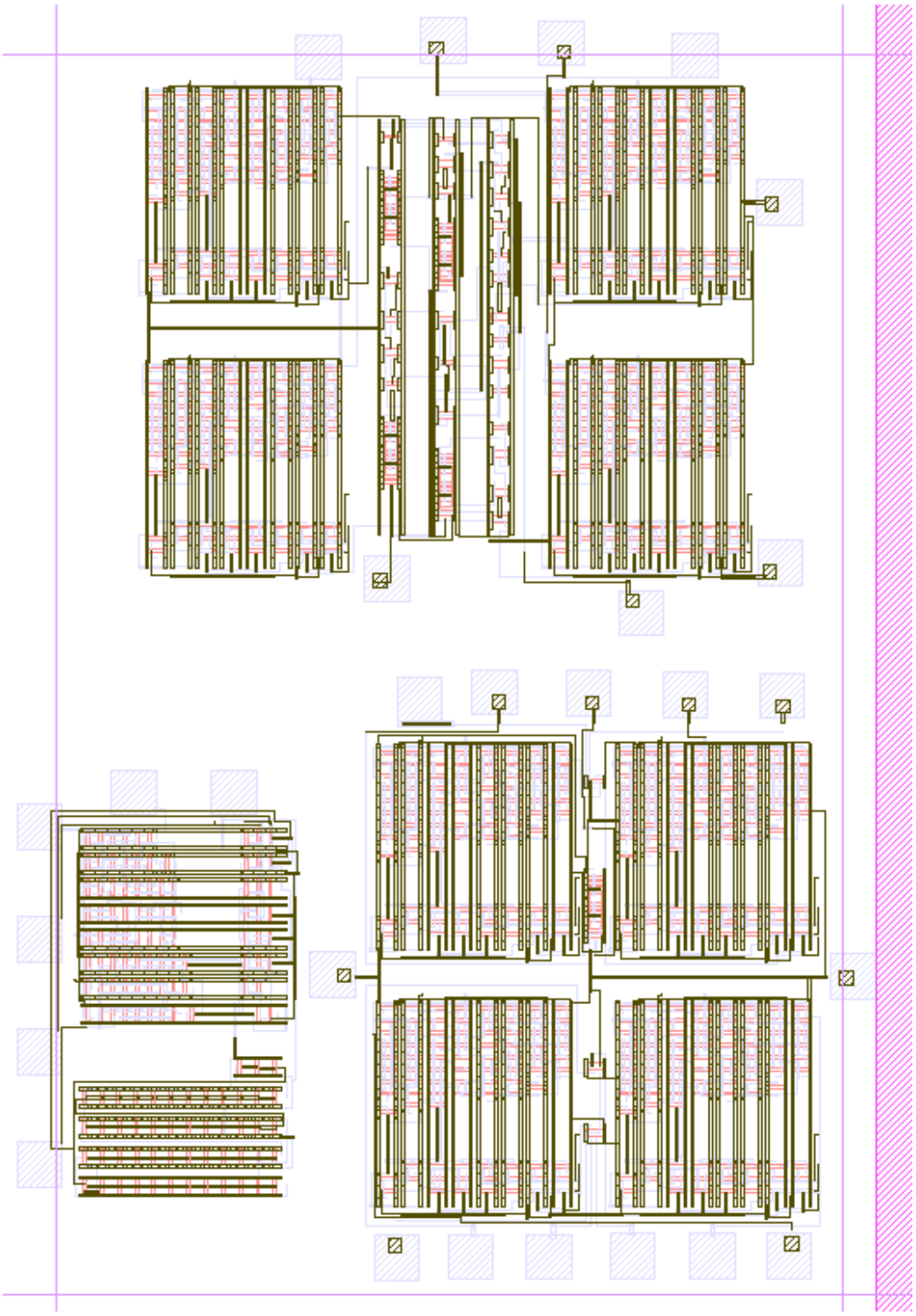

Figure A.2: A closeup photo of the three digital test circuits. Top: count123; Left: ring_osc; Right: logic;

A.2 Test plan logic

Different lose gates for verification: INV (inverter), NAND2, NOR2 and dff (D-type Flip-Flop).

Digital test: Two inputs, one output.

Analog test: Make a VTC (voltage-transfer characteristic) graph of the inverter. Input voltage ranging from 0 to at least 5V, and maybe more for further testing (I have no idea what the maximum supply voltage is). Measure the output voltage, and make a nice plot out of this.

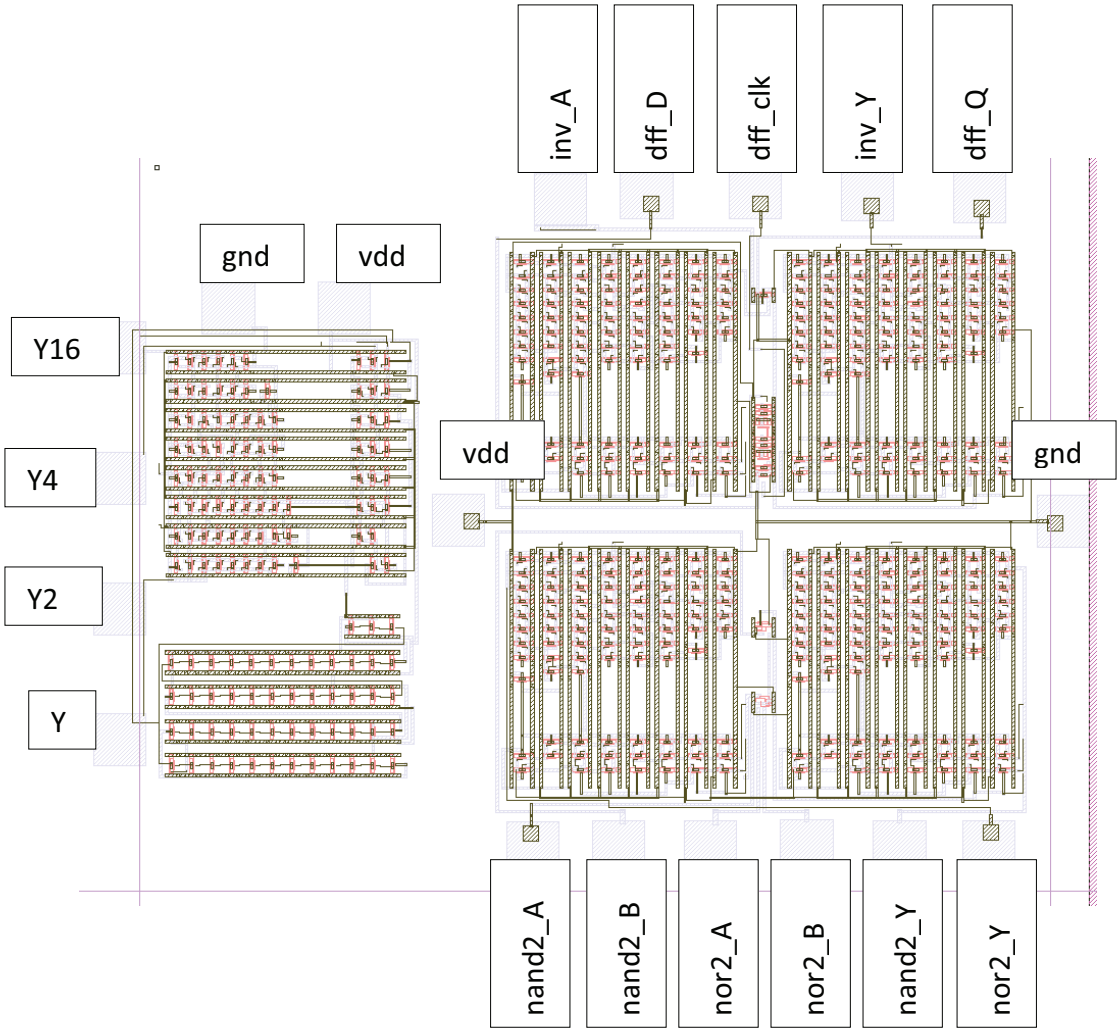

Figure A.3: The test pads with the correct labels. Left: ring_osc; Right: logic;

A.3 Test plan count123

Connect a clock source to pin clk and measure the output. Test if reset pin works.

Requirements for the clock source: *brute force* switching of low and high should be sufficient for testing. It is only a 4 bit counter so 16 different output patterns.

Requirements for the outputs: If possible a scope with 4 channels, but not necessary. Minimal requirements: two channel scope, one for input and one for output. The different output signals can be measured sequentially

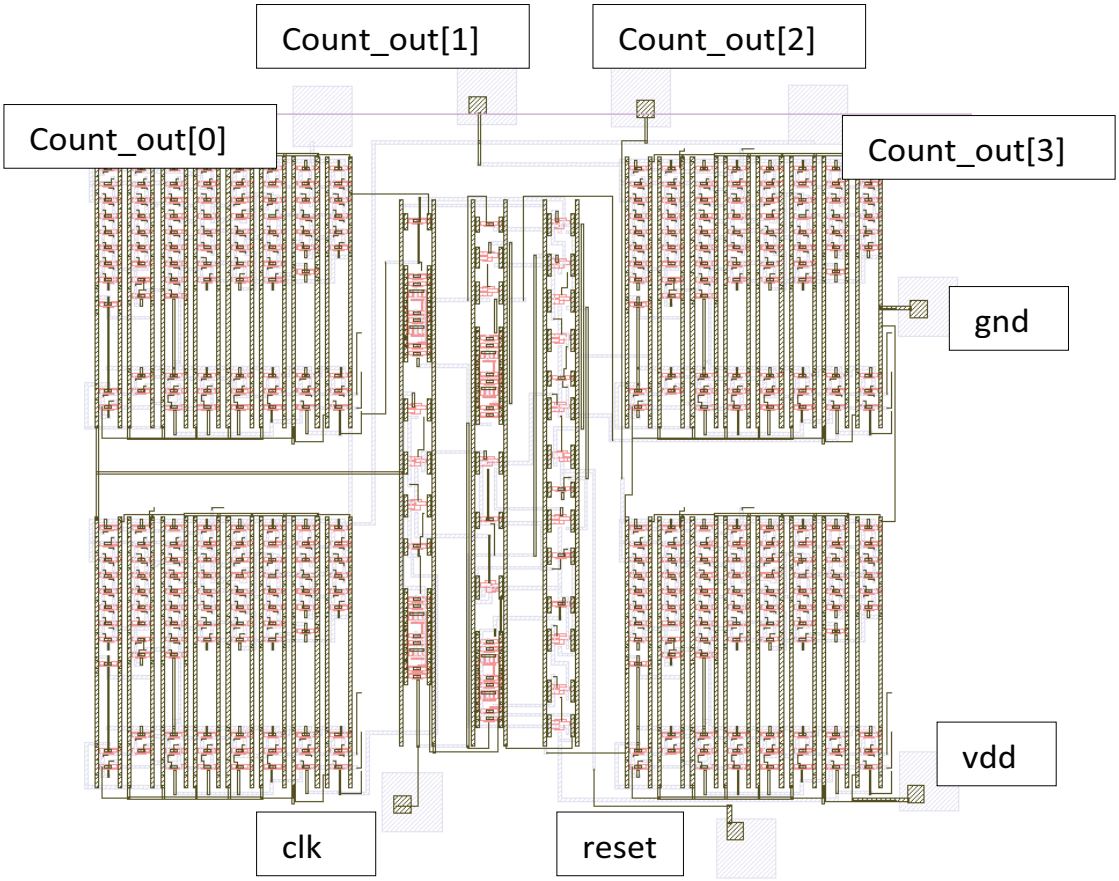

Figure A.4: Test circuit count123 with labeled test pads.

Die Photos of the SG-TFT Digital Circuits

B

B.1 Ring Oscillator

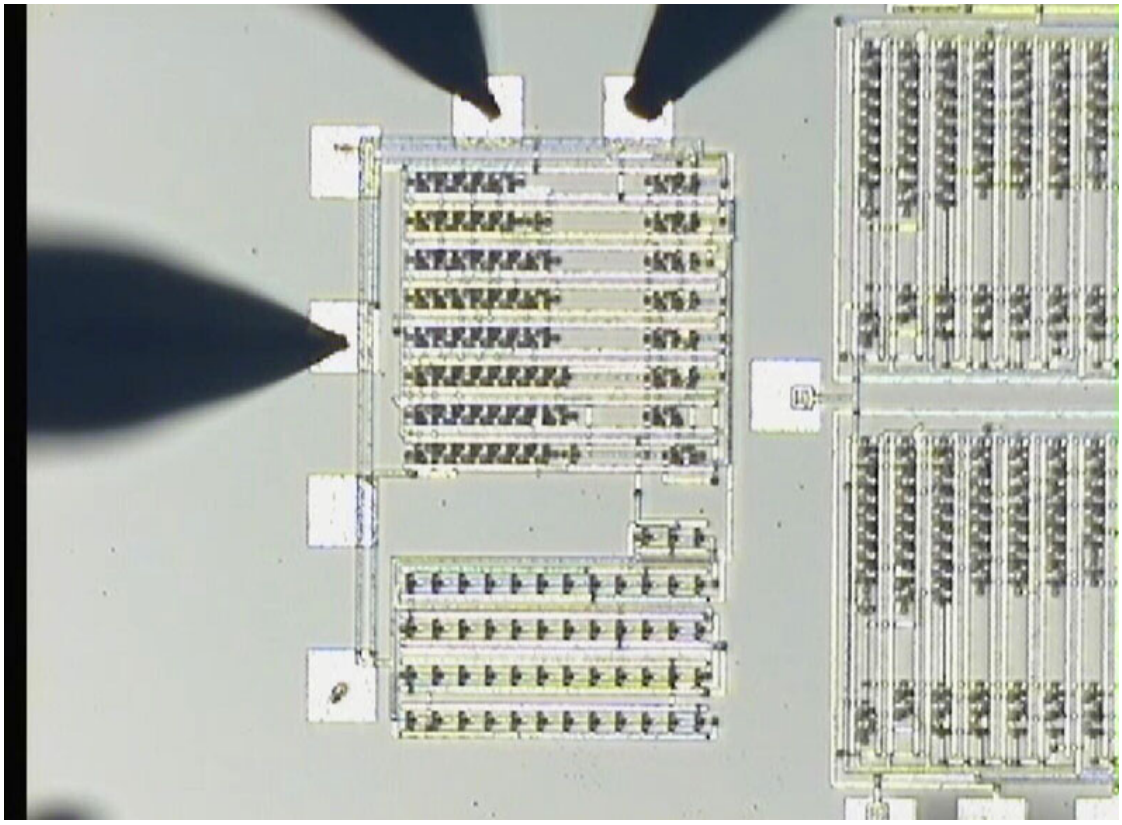

Figure B.1: The 51-stage Ring Oscillator is at the bottom. At the top the output driver can be seen, together with the test pad for the intermediate buffer stages.

B.2 Logic Gates

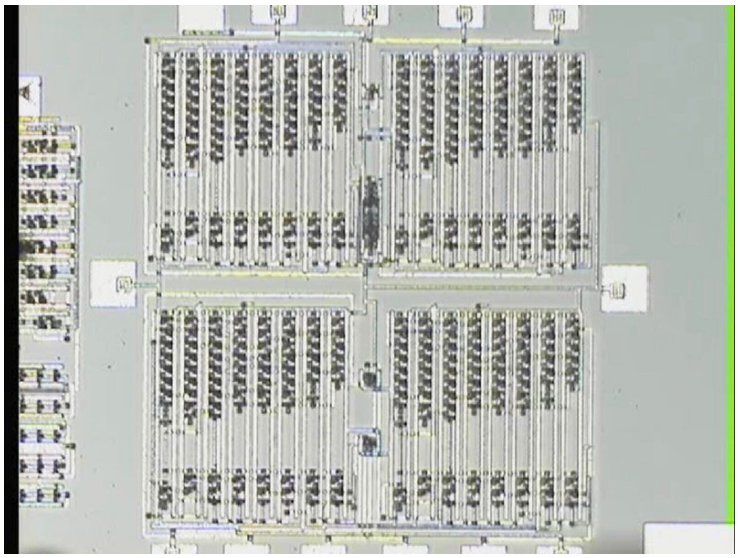

Figure B.2: The logic gates: inv, nand2, nor2 and dff are in located the middle, placed in a vertical orientation. Four output buffers are seen in each of the corners, these are connected to the output of each logic gate.

B.3 4 Bits Counter

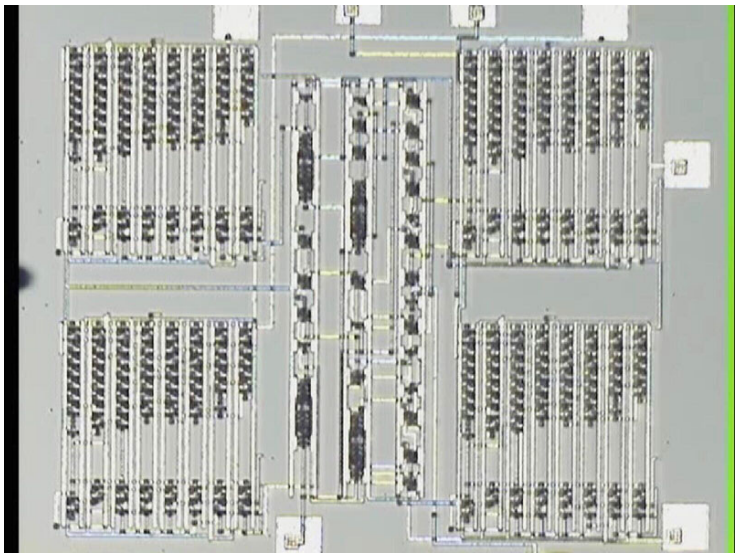

Figure B.3: The 4 bits counter is seen in the middle, each bit had an associated output driver.