Battery Management System

A Custom Design for Delft Hyperloop

EE3L11: Bachelor Graduation Project

Thijs Geschiere
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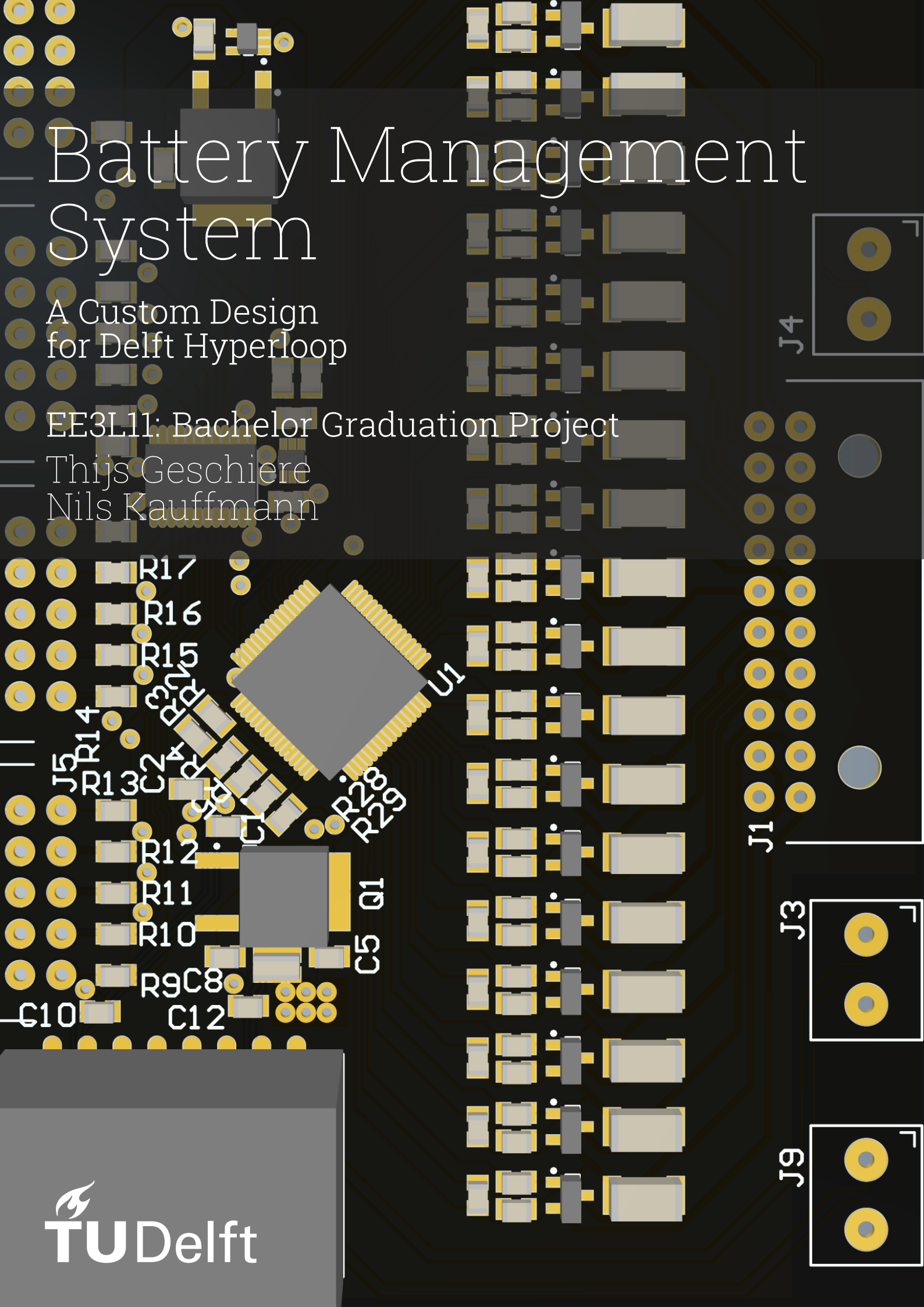

TU Delft

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A Custom Design for Delft Hyperloop

by

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Project Duration: October, 2024 - January, 2025

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TU Delft

Preface

This thesis is written in the context of the Bachelor Graduation Project of the Electrical Engineering curriculum. The project was commissioned by the Delft Hyperloop dream team with the goal of designing a battery management system (BMS), suitable to be implemented on their new pod design. Together with the power distribution department of Delft Hyperloop, requirements for the BMS were established and a prototype that complies with the requirements and the regulations of the European Hyperloop Week competition has been developed. We would like to express our gratitude to our daily supervisor, Daniel Bot, who despite his busy schedule, spent many hours every week guiding us in the project. Furthermore, we would like to thank our project supervisor, Chris Verhoeven, who allowed us to develop a prototype up to academic standards. Additionally, we would like to thank Lukasz Pakula for helping us calibrate the temperature sensors. Finally, we would like to thank Rok Štular, Sam Waterman and Dirk-Jan Kragt of the powertrain department for the fun and productive collaboration.

Thijs Geschiere
Nils Kauffmann
Delft, January 2025

Abstract

This report details the design and implementation of a custom battery management system, tailored to the needs of the Delft Hyperloop dream team. The goal of the custom battery management system is development time reduction for future Delft Hyperloop teams, modularity which allows prototyping with various battery sizes and compliance with the rules and regulations of the hyperloop competition. The core functionalities of the battery management system include safety cell monitoring, cell group balancing and communication. Cell group balancing entails the determination of the amount of charge present in a cell group and consequently, taking action which leads to all cell groups having an equal amount of charge, this ensures performance, longevity and safety of the battery pack.

The battery management system discussed in this report, consists of a prototype printed circuit board which can manage up to 18 battery cell groups. The prototype is centred around a battery stack monitor integrated circuit, which allows high voltage measurement, balancing control and isolated communication. The integrated circuit supports 18 cell inputs with as many cell balancing outputs. The cell balancing outputs drive PMOS transistors which allow excess energy in cell groups to be dissipated in special resistors. Furthermore, a multiplexer is present on the prototype, which allows sixteen cell temperature measurement inputs to the battery stack monitor integrated circuit. Finally, a shunt resistor is present on the prototype, allowing for an accurate current measurement. The prototype has been developed with modularity in mind, the circuit allows to be chained up with multiple circuits of the same type, allowing the management of potentially up to hundreds of battery cell groups.

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Acronyms

BMS Battery Management System. 1

EHW European Hyperloop Week. 1

FPGA Field Programmable Gate Array. 17

PoR Programme of Requirements. 12

RDT Remaining Discharge Time. 3

SoB State of Balance. 3
SoC State of Charge. 2
SoE State of Energy. 2
SoH State of Health. 2
SoP State of Power. 3
SoT State of Temperature. 3

1

Introduction

The Delft Hyperloop dream team consists of about 40 ambitious students, divided over eight departments, many of which working full-time to reach the common goal; Building a hyperloop pod which innovates on the previous team's design with the goal of accelerating the implementation of hyperloop technology and winning the European Hyperloop Week (EHW) competition. The pod is a sort of train engine which levitates using hybrid electromagnetic suspension modules, the pod propels itself using a linear motor based on the magnetic reluctance principle. The team has set ambitious goals for this year, focusing on significantly scaling up the pod compared to previous years. This scaling results in a much heavier pod, which requires a significantly more powerful levitation system and motor. Due to the increase in power requirements, a significantly larger high-voltage battery pack is required. The Delft Hyperloop team employs Lithium-Ion battery cells in their battery pack to power the pod. An integral part of a Lithium-Ion based battery pack is the presence of a Battery Management System (BMS) which ensures the safety, performance and longevity of the battery pack by measuring the states of the cells and taking according action.

The Delft Hyperloop team requests a custom BMS, because existing solutions are often over specified and every new team at the beginning of the year needs to spend months to configure the existing solution. A custom solution would accelerate development time and allow for early testing of subsystems which rely on the battery. In close collaboration with the powertrain department of the Delft Hyperloop team, a BMS has been developed, tailored to the requirements of the team and the battery pack.

2

State-of-the-Art Analysis

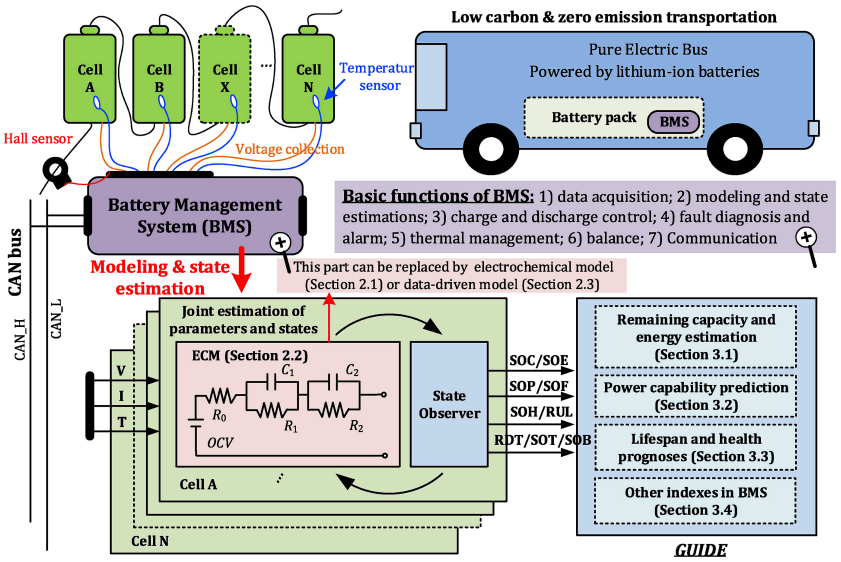

Figure 2.1: Functions of an Advanced Battery Management System [17].

Reference [17] shows that key features of a BMS include: cell data acquisition, battery modelling & battery state estimation, charge & discharge control, fault diagnosis & alarm, thermal management, balance control and communication. An overview of the battery management system functionality can be seen in Fig. 2.1.

2.1. Battery State Estimation

Battery state estimation entails using sensory measurements in order to estimate crucial battery states. Some examples of commonly estimated states include [17], [9]:

- State of Charge (SoC): An index related to the average concentration of lithium present in the positive and negative electrodes of the battery cells. It is commonly expressed as the ratio between the actual capacity and the maximum capacity of the cell.
- State of Health (SoH): A critical index for lifespan and health prognoses, defined as how much capacity the battery pack has compared to when the battery pack was new.
- State of Energy (SoE): A variable which expresses the remaining energy in the battery pack compared the nominal energy available.

- State of Power (SoP): The rate at which energy can be moved from the battery to the loads, commonly defined as the percentage of peak power relative to the rated power. Where the peak power is maximum continuous power available over a short amount of time.
- Remaining Discharge Time (RDT): An indication of the continuous operational time until the battery voltage reaches its lower threshold.
- State of Balance (SoB): A characterization of cell-to-cell battery charge consistency.
- State of Temperature (SoT): An indication of the internal cell temperature.

The SoC and the SoH shall be further elaborated on below as these are the most critical battery states which are relevant to the project

2.1.1. State of Charge

The SoC is one of the most important battery states for a BMS to estimate. It is a quantity which expresses the difference between the actual capacity of the cell and the discharged capacity. The quantity can be seen as a sort of 'fuel gauge', indicating the level of charge present in the cell. It is a critical parameter, used for balancing the cells and indicating the remaining capacity in the battery. The SoC facilitates balancing because it indicates the amount of charge present in each cell group, if certain groups have a higher SoC than other groups, a balancing circuit can be used to equalize the charge in all the present cell groups.

$$SOC\% = 100 \cdot \frac{Q_0 + Q}{Q_{max}} \tag{2.1}$$

Equation (2.1) shows a common calculation for the SoC, $Q_0\ (mAh)$ is the initial charge of the battery, $Q\ (mAh)$ is the quantity of charge delivered by or supplied to the battery. $Q_{max}\ (mAh)$ is the maximum quantity of charge that can be stored in the battery.

Many different techniques exist for estimating the SoC of a battery cell, literature [17] provides a review of modern state-of-charge estimation approaches which shall be summarized below.

Look-up Table Method The first and one of the most straightforward SoC estimation techniques is the look-up table method. In this method, the SoC is determined by a table which maps characteristic parameters (such as impedance spectroscopy, internal resistance, open circuit voltage, etc.) to corresponding SoC values. The advantage of this method is the simplicity, however, the disadvantage is that the battery is required to be rested for a long time in order to ensure the accuracy of the measured parameters [17]. By rested it is meant that no current should be drawn from the cell groups for a certain time period until the parameters have stabilized.

Coulomb Counting The SoC of a battery cell can be determined by taking a time integral of the current coming in or out of the cell, this technique is known as Coulomb counting and is the most straightforward SoC estimation technique, (2.2) shows a common Coulomb Counting calculation.

$$SOC(t) = SOC_0 - \frac{\eta}{Q_{rated}} \int_{t_0}^{t_0+\tau} I\,dt \ \cdot 100\% \tag{2.2}$$

Here, SOC_0 is the initial SoC which needs to be estimated with another technique, η is an efficiency factor which accounts for Ohmic losses in the battery pack. Q_{rated} (mAh) is the known capacity of the cell and I (A) is the current which flows through the battery. However, there are many shortcomings associated with this simple technique. First of all, sensor error will accumulate due to the open-loop calculation. Secondly, the SoC estimation will be negatively affected by effects such as aging and temperature variations. Lastly, the initial SoC must be estimated with the table-lookup method, which means that any initial error will run through the entire SoC calculation process. Due to these shortcomings, this technique is usually combined with other SoC determination techniques [17].

Filter-Based Techniques The filter-based methods can be roughly subdivided into two groups: the Gaussian process-based group and the probability-based group.

A common Gaussian process-based filter approach uses the Linear Kalman Filter (LKF), the LKF is widely used for battery state estimation. It is a recursive process that involves two steps [11]. First of all, predicting the system state and output. Secondly, updating the system state based on output error.

This approach can be extended towards non-linear systems as well. In that case an extended Kalman filter (EKF) must be used. This approach approximates the non-linear system at every step as a linear time-varying system. This LTV system is then used in the Kalman filter in order to estimate the state variables [11].

An extension to the EKF filter approach is the adaptive extended Kalman filter approach. In AEKF, the covariance of process and observation noise is adaptive. This makes AEKF avoid the divergence/bias of the estimation algorithm.

Another variant which expands upon the AEKF is the Sigma-Point Kalman filter, literature [16] has shown that this approach could obtain higher SoC estimation accuracy than approaches based on EKF. In Ref. [3] a SoC estimation method based on an electrochemical battery cell model was proposed, this method used an adaptive square root sigma point Kalman filter (ASRSPKF) and was shown to be 30 % more accurate compared to AEKF and with an 88% shorter convergence time.

The unscented Kalman Filter (UKF) is based on the standard KF and can be used to apply non-linear system equations to the KF under linear assumption. This method uses a technique called ”traceless transformation” to apply the non-linear equations to the KF.

An upgrade to the unscented Kalman filter exists, this upgrade is known as the Adaptive unscented Kalman filter (AUKF). This filter can automatically adjust the noise covariance in the SoC estimation, improving accuracy.

A Central Difference Kalman Filter (CDKF) assumes that the state variables of the cells obey Gaussian distribution. CDKF estimates their mean and covariance after any non-linear transformation. CDKF uses the Sterling interpolation formula to expand the non-linear model according to the central difference.

The Cubature Kalman Filter (CKF) approximates the mean value of the non-linear system state by using a series of volume points in combination with the third-order spherical radial volume criterion.

All the previously mentioned approaches were based on the Kalman Filter, however, a more popular approach in recent time to solve the generic filter is to use the particle filter (PF). The core idea of the particle filter is to generate a set of discrete sampling points in the state space according to the empirical distribution of the system state vector and subsequently adjust the position and state of particles according to the observed values. Finally, the optimal particle state is estimated by adjusting the particle sets. In similar fashion to the Kalman filter based approaches, many expansions and variants of the PF approach exist, each with varying levels of complexity and SoC estimation accuracy.

Observer-based methods A state observer can obtain the values of the cell state variables based on the measured external values of the system. Recently, observer based methods such as the Luenberger observer (LO), the sliding mode observer (SMO), the proportional-integral observer (PIO) and the H-infinity observer (HIO) have been used extensively for battery state estimation [17].

Data based methods Data based methods capable of estimating the SoC exist, these methods consider the battery as a black box and with the help of large amounts of measurable input and output data, internal battery dynamics can be learned. Common data based SoC estimation techniques are based on a neural networks, fuzzy logic, genetic algorithm, support vector machine and other machine learning approaches [17].

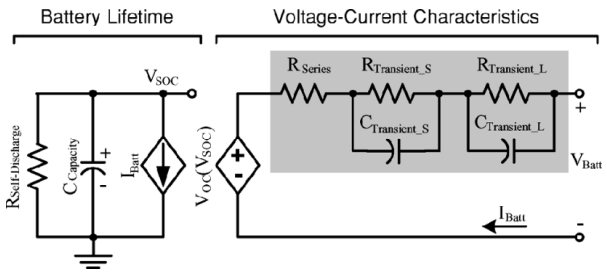

Figure 2.2: The equivalent Circuit Model of a Battery Cell Proposed in [5].

2.1.2. State of Health

The state of health (SoH) is a critical index for lifespan and health prognoses, it depicts the health status of a cell by calculating the ratio between the maximum available capacity of the cell and the capacity of a new cell according to (2.3).

$$SOH\% = 100 \cdot Q_{max}/Q_{max,new} \tag{2.3}$$

Estimation approaches can be divided into four groups: measurement & analysis approach, Bayesian-based estimation approach, empirical fitting approach and machine learning based approach [17].

2.2. Battery Models

Every cell type has its unique characteristics due to the chemical and physical properties of the cells. Even cells of the same type could inhibit different characteristics due to statistical variations in the production process or aging effects which vary from cell to cell. Some battery state estimation techniques rely on a model of the battery cell which accounts for the chemical and physical properties of the cell. For example, many of the filter based SoC estimation techniques mentioned in section 2.1 depend on a fitted equivalent circuit battery model. Other battery models exist, but these usually serve other purposes. Now, three different types of models used in the industry are presented.

2.2.1. Physics based model

Physics based models can achieve a high accuracy when it comes to simulating battery cell behaviour, however, these models are very complex and often need long simulation times. These models are more suited for battery designers to optimize battery compositions and to capture characteristics of the chemical reactions inside the battery [15]. Physics based models can, however, be used in certain SoC and SoH estimation techniques and in some cases, they can be used to study ageing effects of the battery cells [12].

2.2.2. Fitted (electric circuit based) model

A good electrical model of a battery cell is presented by Chen and Mora [5] and an example is given in [1]. This model consists of a SoC dependent voltage source, a series resistor and followed by two pairs of parallel RC circuits. The SoC is modelled by a capacitor with a resistor modelling self discharge and a dependent current source as a function of current in the ‘output’ side. The proposed model can be seen in figure 2.2

All the passive components in this model also exhibit SoC dependency but mostly near the end of a charging cycle, at which point they exhibit a exponential behaviour. The values also differ between charging and discharging. Also the temperature influences the value of these parameters. In [5] it is explained that some of these variables may be omitted in the model to simplify the extraction of these parameters.

The traditional way of estimating the circuit parameters is based on the HPPC test, this is an offline test which is able to accurately fit the battery characteristics to the model [6]. In this test, pulses of current are used to measure the transient response of the cell and from these experimental results the

resistance and time constants of the RC networks can be determined. However, this approach requires a static testing environment which is impractical in practical application.

2.2.3. Data Based Methods

Data based models can also be used to simulate cell behavior, similar to the data based SoC estimation approach, the battery is considered as a black box and with the help of training data and for example a neural network or any other machine learning algorithm, battery parameters can be estimated. This type of approach has good performance concerning nonlinear problems, however, they are easily influenced by training datasets and methods [17].

2.3. Cell Balancing

Due to statistical differences in the manufacturing process, storage and lifetime operating conditions of individual cells, the charge in each cell may differ after a charging or discharging cycle. This can cause an under-voltage in a specific cell in the case of discharging or an over-voltage on a relatively full cell when charging, thus causing a premature end of the (dis)charging cycle [18]. To remedy this issue the cells must be balanced (at the end of a charging cycle). This process can take the form of either active or passive balancing. In the active charge equalization scheme, energy is conserved as opposed to being dissipated in the passive scheme.

2.3.1. Active Balancing

Reference [4] shows four common active charge equalization techniques which are summarized in Table 2.1. Generally, active balancing techniques are more complex to implement, provide bulkier circuits and are more costly than passive balancing based circuits. Figure 2.3 shows an example design of an active charge equalization circuit based on the LT8584 flyback converter and the ADBMS1818 battery stack monitor integrated circuit. This topology is a variant of the *Distributed Cell-To-Cell* active

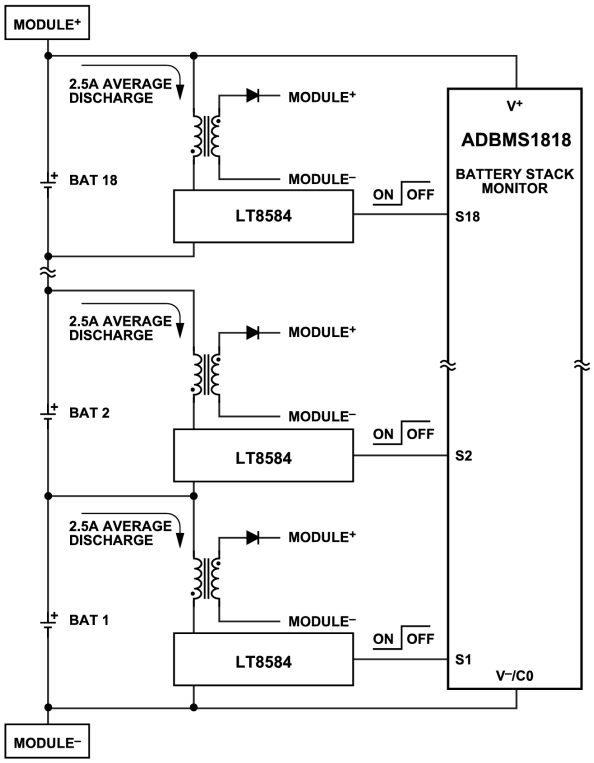

Figure 2.3: An Active Balancing Circuit Design Using Flyback Converters from the ADBMS1818 data sheet [2].

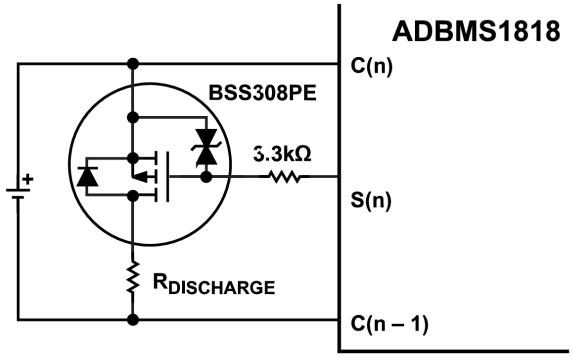

Figure 2.4: A passive Balancing Circuit Design from the ADBMS1818 data sheet [2]. It should be noted that this balancing circuit does not contain an analog RC anti-aliasing filter between the C(n) voltage sensing input and the drain of the MOSFET.

charge equalization technique. When a cell in the group is out of balance, the adjacent flyback converter will allow a current to flow from the top of the stack to the bottom of the stack, distributing the energy of the cell over all the other cells in the battery module.

2.3.2. Passive Balancing

The passive charge equalization scheme is the simplest to implement, but it is also the most inefficient and time consuming equalization scheme. Cells with excess charge are discharged through a resistor until the state of charge of every cell group has equalized.

In Figure 2.4 a passive balancing circuit element can be seen. The battery cell is the leftmost component, it is connected to a MOSFET and a discharge resistor, once the control signal labelled ”S(n)” is pulled low, the MOSFET will turn fully on and the excess energy from the battery cell will mostly be dissipated in the $R_{discharge}$ resistor.

Designers are free to choose a value for $R_{discharge}$, having to make a trade-off between fast balancing time and heat generation.

Table 2.1: Summary of Active Balancing Techniques [4].

Technique	Pros	Cons
Module-to-Cell	Relatively Simple	Switch Network
(Charge is transferred from a battery module to a single cell)	Good Efficiency	High Isolation Voltage of the DC/DC
	Fast	
Distributed Cell-to-Cell	Moderate Efficiency	Bulky
(Charge is transferred between adjacent cells)	Moderately Fast	Complex control
Shared Cell-to-Cell	High Efficiency	Switch Network
(Charge is transferred from cell A to an energy tank and then from the tank to cell B)	Fast	
Cell/Module Bypass	High balancing efficiency	High current switches
(A cell or module is disconnected from the current path)	Very fast and flexible	Complex implementation
		Decreased battery efficiency during normal operation

2.4. Problem Definition

Battery management systems have existed for as long as rechargeable battery powered applications have. A BMS facilitates safety, performance and longevity of rechargeable battery packs consisting of battery cells by taking measurements and taking action according to the input. Literature shows that battery management systems have existed for at least since the year 1990 [8]. Battery management systems in those days were built for specific industrial applications or for research purposes, users required significant economical resources to obtain a BMS.

However, since the 2000's, battery powered technology is more prevalent than ever. More and more consumers and companies have replaced greenhouse gas emitting combustion engine powered vehicles with Lithium-Ion based electric vehicles. Due to the relatively unstable nature of Lithium-Ion based cells, battery management is more crucial than ever. Large commercial companies with significant resources often develop custom battery management systems in-house, these battery management systems are tailored to the battery powered applications such as a certain production line of electric vehicles. Users with less resources and/or knowledge on how to develop a custom BMS are required to purchase a commercially available solutions.

These commercially available solutions are the reason why Delft Hyperloop has requested a custom BMS, they have proven to be over specified for the needs of the team, prolonging development time by months due to the significant configuration time needed. The team uses a battery pack comprised of Lithium-Ion cells, the commercially available BMS Mini 3 produced by the company EMUS was used to manage these cells. However, the commercial BMS had proven itself to be expensive and programming the BMS was a technical challenge, demanding hundreds of man hours due to the extensive accompanying user manual [7]. Relatively small users like the Delft Hyperloop company request BMS solutions which are: cheaper, less over specified than the commercially available solutions and more flexible for prototyping with various battery compositions. Therefore the problem to be solved is: design an affordable battery management system which is inherently modular and supports the management of various battery sizes with minimal reconfiguration effort.

2.5. Thesis Synopsis

The thesis explains the prototype implementation from start to finish in a logical order. First of all, the mandatory and trade off requirements which have been created together with the Delft Hyperloop team are presented. These requirements are listed in an order of importance where the first requirement is considered the most important and the last requirement the least. Generally, safety has been considered the prime factor for ordering the requirements, followed by essential requirements which must be satisfied in order for Delft Hyperloop to deem the product acceptable. The last requirements in the list are considered nice to have, but not essential in order to meet the desired functionality.

Following the requirements, the thesis elaborates on the design process and choice justification. The design process explains the procedure in which the requirements were translated into a functional prototype. It explains which requirements were considered first and the consequences of these requirements, then it explains the order in which the rest of the prototype was implemented.

The choice justification part, as one might guess, explains important design choices. Different options for certain implementations are weighed according to the requirements and other factors such as standardizations in the Delft Hyperloop dream team and consequently, the present solutions are presented. Some of these choices are for example: the choice for a battery stack monitor integrated circuit opposed to a fully discrete circuit, the choice for an NTC temperature measurement sensor, the choice to measure current with a shunt based resistor opposed to a hall effect sensor, the chosen balancing algorithm and the chosen type of master controller.

Subsequently, the thesis elaborates on the prototype implementation and validation results. This section provides a detailed elaboration on the prototype and shows certain accompanying results. The elaboration on the prototype follows the design process. The first choice was implementing a battery

stack monitor IC and a detailed explanation is given on the functionality of the IC. Then the communication between the (theoretical) additional slave boards fitted with the IC and the master board is described. Following the communication, the chapter touches on the implementation of the temperature sensors, then the cell balancing implementation, the current measurement and finally, the results.

After the prototype implementation and validation results, a section is dedicated to the discussion. This section mostly details on possible errors in the practical implementation and in the design methodology. The thesis closes with a conclusion and some recommendations for future work.

3

Programme of Requirements

The requested product by the Delft Hyperloop dream team is a custom battery management system, tailored to the needs of the team. The BMS should be able to balance battery cells, monitor temperature, communicate with the main system and be inherently modular.

In close collaboration with the department responsible for distributing power over the hyperloop pod, a list of requirements has been developed, tailored to the needs of the team and made to obey the rules and regulations necessary for participation in the European Hyperloop Week competition, the requirements are listed in Table 3.1.

Table 3.1: The Programme of Requirements for the BMS.

ID	Requirement for the Battery Management System	Requirement Type
BMS.TEMPERATURE.1	The BMS should measure the temperature of at least 25% of the cells present in the complete battery.	Mandatory
BMS.DISCONNECT.1	The BMS must disconnect the relays of the battery when any malfunction is detected	Mandatory
BMS.DISCONNECT.2	The BMS must disconnect the battery if any cell temperature measurement equals or exceeds 60 ° C, the allowed uncertainty was not specified by the team.	Mandatory
BMS.DISCONNECT.3	The BMS must be able to prevent cell over current during discharging by disconnecting the battery when any battery current measurement equals or exceeds 105 A, unless the situation of requirement BMS.PEAK.1 is in effect. The allowed uncertainty was not specified by the team.	Mandatory
BMS.DISCONNECT.4	The BMS must be able to prevent cell over current during battery charging by disconnecting the battery when any battery current measurement equals or exceeds 18 A, the allowed uncertainty was not specified by the team.	Mandatory
BMS.DISCONNECT.5	The BMS must be able to prevent cell over voltage by disconnecting the battery when any cell voltage measurement equals or exceeds 4.25 V with an uncertainty of 50 mV.	Mandatory
BMS.DISCONNECT.6	The BMS must be able to prevent cell under voltage by disconnecting the battery when any cell voltage measurement equals or is less than 2.50 V with an uncertainty of 50 mV.	Mandatory
BMS.SAFETY.1	The BMS must give a visual indication of its current mode of operation.	Mandatory
BMS.BALANCING.1	The BMS should be capable of balancing cells	Mandatory
BMS.MODULAR.1	The BMS must facilitate the expansion or removal of modules, allowing management of various battery sizes.	Mandatory
BMS.MODULAR.2	A single BMS module must allow for the management of 8 up to 18 cell groups.	Mandatory
BMS.COMMUNICATION.1	The BMS must be capable of full duplex digital communication to the rest of the hyperloop system.	Mandatory
BMS.COMMUNICATION.2	All collected measurements must be accessible from a communication interface where the measurements are updated at a minimum rate of 50 Hz.	Mandatory
BMS.PEAK.1	The BMS must facilitate a peak battery current of 240 A for a duration of up to 14 seconds after which the battery should be disconnected, unless the battery current returned to a value below or equal to 105 A. The allowed uncertainty was not specified by the team.	Mandatory
BMS.BALANCING.2	The BMS should be capable of balancing cells in an active manner, conserving more energy than in the passive scheme	Trade-off
BMS.STATE.1	The BMS should be capable of estimating the state of charge, the allowed accuracy was not specified by the team	Trade-off

4

Design Process

The Programme of Requirements (PoR) places a requirement on the modularity of the BMS to be designed. Each module should be able to manage 8 up to 18 cell groups. This means that multiple modules should be able to be connected together in order to facilitate the management of larger battery packs such as those present on the Hyperloop pod. For this reason it is beneficial to keep these repeating modules relatively simple and to move the more complex features such as the balancing algorithm to a master board. The repeating modules shall be referred to as slave boards and the board which controls the slave boards is called the master board, both shall be elaborated on below.

4.1. Slave Board

The role of the slave board is to perform relatively simple tasks which are repeated for every group of cells and cannot be centralized from the master board. The functions of the slave board and the design process shall be detailed on below.

In designing the BMS, the PoR was examined point per point, observing which requirements operate together so that they may be served or or harmed by a single choice to be made. An example that will come to mind is the OVP/UVP protection, which may both benefit from a single voltage measurement. Other requirements may impede one another such as the simultaneous need for frequent updating and for accuracy. In such a case a trade-off has to be made. The slave circuit is a reused circuit in the final use of the system, as such price considerations may weigh more than in the case of the master circuit, of which only one exists.

The first interest was in finding a solution for the requirement of up to 18 cell voltage measurements. This is not an trivial task to manage, given the relatively high voltages present at the cells. In this case, a requirement was placed on the range and accuracy of the measurement. The PoR and the EHW competition rules and regulations also impose requirements on the frequency of measurement. To suit these requirements more or less integrated solutions might bring a solution.

As part of these more integrated solutions ‘battery monitoring’ ICs were explored. These ICs offer in their most basic form voltage measurements of one or more cells. They may also include GPIO pins or communication lines fit for isolation by means of capacitors or transformers. One such IC is the ADBMS1818 by Analog Devices [2]. This IC combines all the mentioned features. Less integrated solutions would follow a intricate design process with care for the high voltages.

The second interest was in finding a temperature measurement solution fulfilling the requirements. As no strict constraints exist on the accuracy or resolution of the measurement, the primary concern was the number of channels to be measured. This being one quarter of all cells, in the case of last years battery at least 11. Multiple technologies were examined and compared, first of all for compliance with the requirements and secondly for factors such as: price, ease of implementation, standards in the Hyperloop team and availability.

Lastly, the method of current measurement was chosen. Because of the series connection of cell groups in the battery pack, only one measurement point is necessary to obtain the value of the battery current. Therefore, this burden could be placed on the master circuit. However, the authors have chosen to integrate this feature on the slave circuit, as this preserves the existing isolation between the master circuit and the battery. The method of measurement should be chosen on the basis of certain qualities that are beneficial to the protection and SoC estimation. As no requirements were set in terms of accuracy nor resolution, an acceptable solution was chosen. If future teams would find the solution unsatisfactory, it may simply be replaced as it is not related to other circuitry.

4.2. Master circuit

The role of the master circuit in the chosen architecture is to collect information from the slave circuits, to process this information and to order the slave circuits to act appropriately. Other tasks of the master are making or breaking the emergency relay line and reporting the measured data to other parts of the Hyperloop Pod. All these functions are most easily implemented on a main processor/controller as all required information from the slave circuits can be easily accessed from a single communication line.

Therefore, the primary task is to choose a controller that can function in this role and preferably, is straightforward to implement. The preference from the hyperloop team of reusing parts also weighs in the choice. The performance requirements of this controller to be chosen are dependent on the algorithms to be used, primarily in estimating the SoC.

5

Choice Justification

In this chapter, the previously described design process is executed, weighing the different available options to find the ones which best satisfy the requirements. This is done in the order presented above.

5.1. Voltage

In finding a solution for the voltage measurement both a more and less integrated solution were examined. A less integrated system would consist of separate multiplexers, ADCs and communication systems. In searching for suitable multiplexers and ADC's none were found that could satisfy. Most problematic are the relatively high voltages present, requiring a solution consisting of multiple stacked circuits. This of course adds complexity, which is opposed to the goals of this project. In looking for a more integrated solution battery monitoring ICs were then examined and found to be very complete in their features. A highly valuable function of some of these ICs is their ability to be 'daisy chained'. In this way one single line of communication is presented to the master circuit. The model introduced earlier, the ADBMS1818 also brings a total of 9 GPIO pins that can also be read out by the ADC. This IC was chosen for the project.

5.2. Temperature

Temperature measurement can be achieved by a few technologies as set out below, each with their own qualities and costs. The sensor types considered below are the RTD, NTC, the silicon sensor and the thermocouple [13].

The RTD (resistance temperature detectors) is a resistor made from a pure metal. The change in resistance is measured and the thermal coefficient of resistance is used to find the temperature change. These changes in resistance are quite small (0,39%/K for Platinum) and thus require some care and circuitry to properly measure. The accuracy provided is excellent, but the financial costs are the highest of the four categories.

The NTC (negative temperature coefficient) also called thermistor is a resistor made of a semiconducting material with an exponential temperature characteristic around the temperature of interest. This exponential response makes the sensor more sensitive near this temperature of interest. The temperature range covered by NTCs is generally smaller than that of RTDs. The accuracy is less than that of the RTD, tolerances exist in both the nominal value at a fixed temperature, and in the exponential behavior of the semiconductor.

COMPARISON BETWEEN THE DIFFERENT TYPES OF THERMAL SENSOR

Feature	PRTD	NTC-Thermistor	Silicon	Thermo-couple
Temp. range	H/M	M/L	L	H
Accuracy	H	L	M	H/M
Linearity	H	L	H/M	M
Sensitivity	M	H	H/M	L
Read-out circuit complexity	M	M	L [a]	H
CMOS compatibility	No	No	Yes	Yes [b]
Self-heating	Yes	Yes	Yes	No
Cost	H	L	L	M/H [c]

Abbreviations: L: Low; M: Medium; H: High
[a] From the user's point of view.
[b] But without being a standard type.
[c] It depends on the type of metal (base or noble) employed.

Figure 5.1: Technical comparison between the presented temperature sensors[13]. Only some of these features are of interest in this project.

The silicon temperature sensor is an integrated circuit in which two transistors wired as diodes are biased at different currents. This results in two different V_{be} temperature coefficients. The voltage difference is measured and in this way the temperature can be found. These ICs often have integrated output circuitry that converts this voltage difference to a single ended voltage with a certain offset. In this way reading the temperature only requires a voltage supply and a voltage measurement. These sensors may also include an integrated ADC, enabling digital readout.

Thermocouples consist of two wires of dissimilar metals with a junction at the end. The Seebeck effect causes a voltage difference to exist over these wires. When the open ends of the wires are connected to a circuit for measuring, at each of these connections a new junction is formed. When these two junctions are at the same temperature (due to physical proximity in the connector) these voltages cancel eachother out, and the resulting voltage is now only a function of the temperature difference between the further junction and the connection point. To obtain absolute temperature, a temperature measurement of the 'cold' junction (between the wires and the connector) must be taken by any of the previous methods.

All of this is presented in a tabular form in Figure 5.1. Self-heating is not important in the present application as the the temperature sensors are to be glued to the cells which have a great thermal mass and the cells are large compared to the sensors.

To weigh the benefits and the costs of each of these four solutions a weighing systems was devised to account for the present needs, consisting of these few qualities in which the options will be ranked from zero to three, multiplied by a factor in brackets. Accuracy is not one of these qualities in question as no requirements are fixed. Each of these solutions would suffice.[1] Ease of use is weighed doubly to express the scarcity of time that exists in a dream team such as Delft Hyperloop.

- Ease of use: the implementation of this sensor brings with it the least additional complexity (2)
- Price: the sensor and necessary circuitry bring with them little cost (1)
- Team standard: the DH team uses in type of sensors in other/previous parts (1)

From this comparison the NTC is found to be preferable.

[1] The temperature limit imposed by the EHW Rules and Regulations is some 20 degrees below the temperature limit which the cell can handle according to the datasheet.

Table 5.1: Comparison of temperature sensors weighed by the factors

	Ease of use	Price	Team standard	Sum
RTD	0	0	0	0
NTC	6	2	1	9
Silicon	4	3	0	7
Thermocouple	2	1	0	3

CATEGORY	SHUNT-BASED	HALL-BASED
Solution size	Similar	Similar
offset	Very low	Medium
Offset drift over temperature	Low	Medium
Accuracy	<0.5% after calibration	<2% after calibration
Noise	Very low	High
Bandwidth	Similar	Similar
Latency	Similar	Similar
Nonlinearity	Very low	High
Long-term stability	Very high	Medium
Cost	Similar	Similar
Vibration impact	Very low	Low
Power dissipation	Low	Very low
Customization	Flexible	Limited

Figure 5.2: Comparison table for current measurement[10]. As can be seen, the hall-based sensors only true benefit is low power consumption and isolation. In all other categories the shunt based sensor prevails.

5.3. Current measurement

In general two methods of current measurement are found. The first one being the use of a shunt resistor, the second one being the use of a hall effect sensor. The principal advantages of the latter is that no power is spent in a resistor measuring the current and the fact that the output is isolated from the signal to be measured. In most other factors the shunt is superior. A good overview can be seen in Figure 5.2 made by Texas Instruments[2]. Given that there is no need for power conservation nor isolation[3], the table should be convincing for the choice of a shunt resistor.

5.4. Balancing method

The two types of balancing, these being active or passive, each have advantages and disadvantages. The primary advantage of active balancing is the conservation of energy in the battery. In the present case this was not found to be of great importance. During the charging of the battery and therefore during the balancing, power is supplied by the grid, therefore the marginal energy loss associated with passive balancing was deemed acceptable.

The simplicity of passive balancing also played a role. The slave circuit is repeated multiple times in a complete battery. Any simplification of this part weighs stronger in the choice.

The worst case in balancing occurs when one single cell is at a lower SoC than the rest. In this case all of the full cells need to be discharged while the lower cell is charged. $N-1$ cells are discharged. With 18 cells and a 5% imbalance this comes out to $\frac{17}{18} \cdot 5\% = 4,7\%$ of the total capacity. But as charging is done from the grid, this loss is accepted.

[2]Who have business in both of these solutions.

[3]Earlier the burden of current measurement was placed on the slave circuit which is not isolated from the battery. In this way isolated current measurement would not be advantageous.

5.5. SoC estimation algorithm

SoC estimation algorithms relying on a complex model of the cell to be managed work only if this model is of good quality. As of now, it is not yet known what model of cells the Delft Hyperloop team will use. This and consideration of the complexity (and with it the chance of errors) of such an estimator informed the choice for the coulomb counting method.

At a later point this may in be changed in software if it is found to be unsatisfactory and a good model of the batteries is known.

5.6. Master controller

In choosing the controller to be used by the BMS master there exists a dilemma. This is the choice between a micro-controller and an Field Programmable Gate Array (FPGA) [14]. Both are found in literature and each have their own advantages. Speed can be gained by the use of an FPGA, while bringing increased complexity compared to micro-controllers.

With the choice of coulomb counting it is thought that the update rate is not limited by processing, but rather by time spent in measurement and communication. The final factor in this choice is that of the team standard. In the Delft Hyperloop team the use of STM32 micro-controllers is the standard, and encouraged for all parts of the pod. For these reasons the use of these STM32 micro-controllers was preferred over an FPGA.

6

Prototype Implementation and Validation Results

Following the decisions described above the authors commenced the design of a prototype. In the interest of time only the slave circuit was designed. Development boards for the STM32 were available and the master circuit was implemented on such a board.

A graphical representation of the practical implementation of the system designed is shown in Figure 6.1

6.1. Practical implementation

6.1.1. The ADBMS1818

The ADBMS1818 IC was chosen as the battery monitoring IC. This is a product very well suited to the present needs. The total measurement error in normal operation[1] is only $\pm 4mV$. The same error also applies for the 9 GPIO pins, each of which can be measured by the same ADCs[2]. This IC also exposes the internally generated reference voltage of the ADCs, allowing for ratiometric measurement when this voltage is applied to a divider. The internal structure is shown in Figure 6.2

A full list of features is presented below. Only part of these features are used in the prototype.

- 18 Voltage measurments
- 9 GPIO voltage measurements or outputs
- ISOSPI communication
- Internal self test of the MUX, ADC, digital filter
- Open wire detection
- Balancing outputs with PWM option[3]
- SPI/I2C communication on the GPIO pins[4]
- Pulse output on balancing pins

Cell voltages presented to the IC are to be filtered by a RC low-pass filter per the datasheet. A trade off can be made between settling time and anti-aliasing performance by choosing the values of this filter. A good trade off between the aforementioned affects resulted in the values of 100Ω and $10nF$. This resulted in a time constant of $1\mu s$. At one half of the ADC sampling frequency this filter has a -20dB transfer. This filter can also serve as EMI protection for the IC. Currently it is unknown in which

[1] In terms of conversion speed

[2] Three are present to speed up conversion and permit verification among the three.

[3] Settable in 2 seconds increments with a period of 30 seconds.

[4] As a sort of virtual communication port that is controlled by the master.

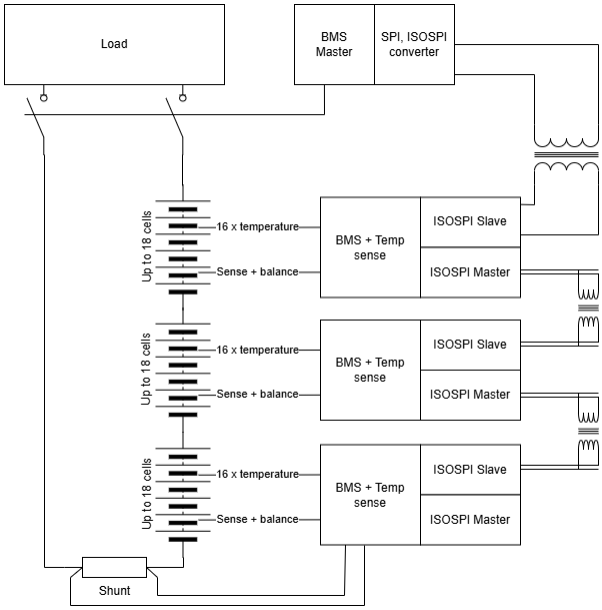

Figure 6.1: A diagram showing how the presented BMS slave circuit would be used in a practical battery. In this diagram three slave circuits are shown, but more can be present. As can be seen the shunt is connected to the slave managing the lowers group of battery cells. Note that only the master controls the disconnection relay.

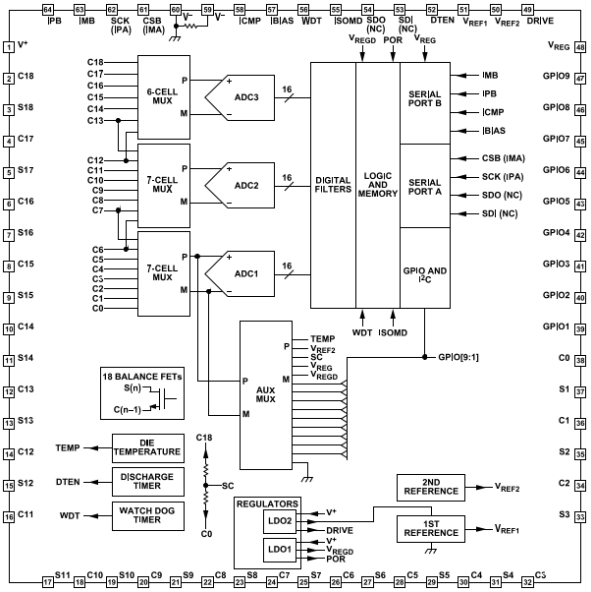

Figure 6.2: Block diagram of the ADBMS1818. Originally figure 52 in [2]

environment the BMS will operate, but if it is found that EMI is significant enough to be harmful to the IC, the RC values can be adjusted to resolve the effects.

The IC has two communication ports, A and B. Port A can be configured as either SPI or ISOSPI. The latter is a communication protocol developed by Linear Technology (now Analog devices) to permit SPI communications over longer wires, and be able to isolate the communication. Port A is configured as ISOSPI.

To permit balancing, the ADBMS1818 includes for each cell a MOSFET. In cases where the current to be balanced is small, these MOSFETs in combination with resistors can be sufficient for balancing. In the present case this would have caused intolerable heating of the IC. In these cases the internal MOSFETs act to turn on or off external MOSFETs, which will in combination with an external resistor dissipate the heat. For a graphical explaination please see Figure 2.4. In this figure the RC filter is not shown. It would be between the drain of the MOSFET and C(n).

Power to the IC is taken from the batteries being managed. The voltage of the top most cell in the eight to eighteen cell stack is fed to the collector of a NPN transistor. In the IC a $5,7V$ signal is generated and this is fed to the base of the transistor. In this way a $5V$ supply is generated for the ADBMS1818 and other components. The efficiency of this system is poor and gets worse with increasing voltage on the cells. There is in the present case no need for power saving, as a large safety margin exists on the capacity of the hyperloop pod battery, therefore, the marginal reduction in power use would not significantly affect the performance of the pod. Thermal dissipation is a concern and this had been taken care of. To dissipate the heat generated, it is conducted to the ground plane of the PCB. As none of the pads (and certainly not the large thermal pad) is at the potential of the ground plane, a Vishay ThermaWick® has been used to conduct the heat.

6.1.2. Communication

The communication between the slave boards and the master is done by way of ISOSPI. The signal uses differential pulses in a twisted pair. Positive and negative pulses communicate the information by their order. Positive followed by negative signals a high value, the inverse signalling a low value. Like in normal SPI, ISOSPI uses a *chip select* line that is active when it is low. Chip select signals are communicated by longer pulses. When one port on the ADBMS1818 receives data, it will automatically relay this information to the second port. This repeating of the received signal permits the daisy-chaining of multiple slave circuits. When the chip select is signaled to be deactivated, all the ICs latch the data that is present. In this way they act as a long shift register.

The ADBMS1818 has a limited acceptable common-mode voltage range on the transceivers that must be respected for correct operation. In the present prototype, both of the ports are isolated by a center-tapped transformer followed by a common-mode choke. The center tap of the transformer is bypassed by a capacitor to further reduce common-mode noise in the signals. This is of great importance, for the common-mode voltage present results directly from changing battery voltage. The signal originating from another slave circuit has a steady common-mode voltage that is equal to the voltage of the cells being managed per slave (that is of course rejected by the two transformers). But when due to peaks in current consumption, the battery voltage drops, the common-mode voltage follows without attenuation. At $1kHz$ cells typically used by Delft Hyperloop have an internal impedance of $24m\Omega$. If 18 cells are managed in series, this gives $432m\Omega$. At a typical discharge current of $10A$, this would result in a voltage drop of $4,32V$ which is too high for the receiver and thus requires filtering.

An attempt was made at measuring the realized CMRR (common-mode rejection ratio) with the measurement setup shown in Figure 6.3. This resulted in unusable data as the setup measured leakage from the signal source. At $100kHz$ the filtering is estimated to be at least 62dB. This value was found by imposing a 1Vrms common mode signal on the primary side of the transformer and measuring a voltage on the secondary. The voltage measurement was dominated by voltages picked up by the probes. The value that was finally accepted was $800\mu V$, but the uncertainty is high.

Despite the short duration of the ISOSPI pulses, the communication speed is rather limited. It is capped at $1Mb/s$ by the ADBMS1818. When using ISOSPI on the ADBMS1818 the amplitude of the pulses is a free design choice. Signals with higher amplitude are more resistant to noise, but of course con-

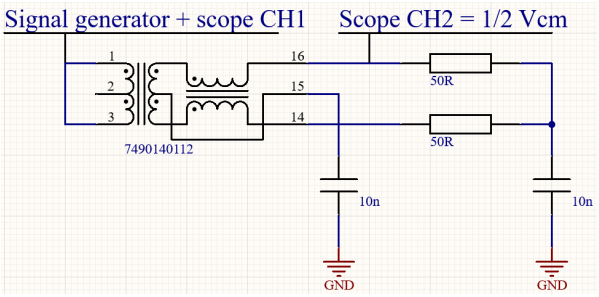

Figure 6.3: Measurement setup used to find CMRR. The signal generator is applied to the primary side of the transformer and measured with the first channel of an oscilloscope. The secondary side is measured with the second channel. The setup finally failed to produce usable data due to leakage of the generator signal into the second channel of the oscilloscope.

Table 6.1: Parameters of MF52B2

R_0	$10k\Omega \pm 1\%$
T_0	$298K$
β	$4150K \pm 1\%$

sume more power. In the present case power consumption is of little concern, and the reliability of the communication was given higher priority.

6.1.3. Temperature

The temperature measurement is performed by means of $10k\Omega$ NTC thermistors. The circuit used is a voltage divider with the NTC as one of the resistors. The other resistor is a $10k\Omega$ resistor. The voltage applied to the divider is the reference voltage from the ADBMS1818 buffered by an op-amp. In this way the ADC measurement measures the ratio of the resistors.

The voltage that results from this divider is given by Equation 6.1. By manipulating this equation R_{ntc} can be found, as shown by Equation 6.2. The NTC response to temperature is exponential. Within the temperature range of the specific thermistor used, it follows Equation 6.3. The three constants are R_0, T_0, β. The first two specify a certain resistance at a certain temperature. The β parameter defines the exponential behavior of the thermistor. By rewriting this equation the temperature can be found for a given resistance. This is shown in Equation 6.4

In the case of the chosen thermistor with parameters as shown in Table 6.1. At T_0 the $\pm 1\%$ tolerance in R_0 results in a measurement error of less than $0,3K$. At 50 the tolerance of β results in an error of $0,2K$.

$$V_o = V_{ref} \cdot \frac{R_{ntc}}{R_{ref} R_{ntc}} \tag{6.1}$$

$$R_{ntc} = V_o \cdot \frac{R_{ref}}{V_{ref} - V_{V_o}} \tag{6.2}$$

$$R_{ntc} = R_0 e^{\beta(\frac{1}{T} - \frac{1}{T_0})} \tag{6.3}$$

$$\frac{1}{T} = \frac{\log R_{ntc} - \log R_0}{\beta} + \frac{1}{T_0} \tag{6.4}$$

The 16 resistor dividers are all fed to a 16 way multiplexer. This multiplexer is controlled by four control wires from other GPIO pins of the ADBMS1818. As these GPIO outputs are of the open-collector type, pull-up resistors are included in the circuit. Given that the on-resistance of the multiplexer with a 5V

power supply voltage can be as high as $1k\Omega$ the settling time was thought to be of concern. This was unfounded, as the temperature measurement only occurs $500\mu s$ after switching. If ten times the RC time constant is allowed, the input capacitance would have to be $50nF$. The datasheet of the ADBMS1818 IC does not specify a value, but $50nF$ is thought to be implausible.

6.1.4. Balancing

Balancing is achieved in a passive way using a MOSFET and an external resistor per cell. The value of this resistor was chosen to permit a certain amount of discharge in a given time. The current needed is found using Equation 6.5. The resistor value can be found using the expected voltage at the moment of discharging: $R = V/I$.

$$I_{dis} = \frac{BalError(\%) \cdot Q_{total}(Ah)}{Time(hours)} \tag{6.5}$$

Initially balancing of 5% of the total capacity in 20 minutes was sought out. The BMS was designed for three cells of $3Ah$ connected in parallel, giving $9Ah$. This would require a current of $1350mA$. At a voltage of around $4V$ this would generate more than $5W$ of heat.

For the prototype this was not realistic. For testing of the prototype, single cells were used (and not three in parallel) and speed was not of the essence. A resistor of 20Ω was instead used, allowing for 5% discharge in 45 minutes and dissipating $0,8W$.

6.1.5. Current measurement

The value of the chosen shunt resistor is a function of the maximum current to be measured. This current is $240A$. A value of $100\mu\Omega$ was chosen as this would only result in $5,8W$ of heating of the shunt, alleviating the need for cooling.

The voltage present at the shunt resistor is $100\mu V/A$. Given the total measurement error of the ADBMS1818 ADC, this would result in a possible error of $\pm 40A$, and a resolution of $1A$, which are unacceptable. For this reason an amplifier was used. An instrumentation amplifier was used because as a result of the large currents, none of the two terminals of the shunt are at ground potential. Also of note is the fact that the common mode voltage of the two terminals is lower than the ground potential of the BMS slave.

A suitable instrumentation amplifier was chosen which could accomodate the negative common mode voltage. This amplifier is supplied with 5V. The 3V voltage reference originating from the ADBMS1818 is used as the offset voltage. The output of the amplifier being rail-to-rail, it allows for $-3V$ to $+2V$ output, the negative value occurring during discharge. With a maximum input voltage of $24mV$ at $240A$ ordinarily a gain of 100 would be too much. In this case however, charging will never be performed at these extreme currents, and a gain of 100 is possible.

A special source of measurement errors in such low voltage situations is that of the Seebeck effect. This effect generates small voltages in junctions of dissimilar metals, like in a thermocouple. In the present case this is limited due to the copper construction of the shunt used and the limited temperature difference due to the highly thermally conductive construction.

An inventory of all sources of error is shown in Table 6.2. As can be seen the offset is significant. But as the drift is limited, this can easily be corrected in the software. The gain error can also be calibrated.

6.2. Results

The slave board has been designed and a custom Printed Circuit Board (PCB) was ordered and assembled by the authors. Figure 6.4 shows a picture of this PCB with only the first four filter/balancing circuits soldered. The functions were then tested. Firstly the temperature measurement was evaluated, followed by the current measurement and the voltage measurement. The results of the SoC estimation and balancing are presented last.

Table 6.2: Inventory of current measurement errors. All values are the maximum specifications except where specified. $R = 100\mu\Omega$, $Gain = 100$

Source of error	Gain / Offset	Quantity	Effect
Shunt value	Gain	5%	5%
Amp. gain error	Gain	$0,3\%$	$0,3\%$
Amp. offset	Offset	$Gain \cdot 15\mu V$	$1,5mV \rightarrow 15A$
ADC error	Offset	$4mV$	$4mV/Gain \rightarrow 0,4A$
Shunt drift	Thermal	$20ppm/K$	$175ppm/K$
ADC gain drift	Thermal	$10ppm/K(typ)$	$10ppm/K(typ)$
Thermal EMF	Thermal	$1\mu V/K$	$1\mu V/K \rightarrow 10mA/K$
Amp gain drift	Thermal	$7ppm/K$	$7ppm/K$
Amps offset drift	Thermal	$80nV/K$	$80nV/K \rightarrow 0,8mA/K$
Total	Gain	$5,3\%$	
Total	Offset	$15,4A$	
Total	Thermal	$10,8mA/K + 192ppm/K$	

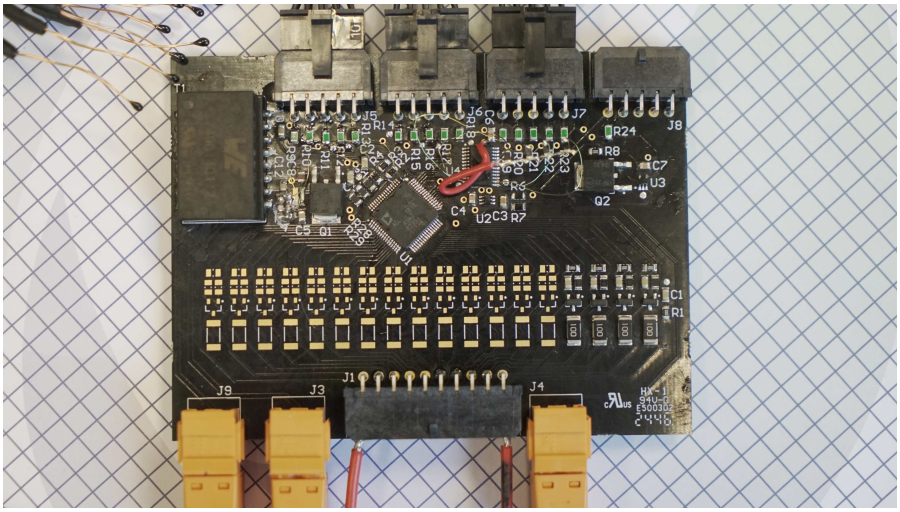

Figure 6.4: Partly assembled slave circuit PCB. The top row of connectors connect the thermistors. The left two connectors on the bottom are the A and B communication ports of the ADBMS1818. The large central connector at the bottom connects to the battery cells. The rightmost connector on the bottom connects to the shunt resistor, this is only fitted on one of the slave circuits. The black box at the top left of the PCB is the isolation transformer.

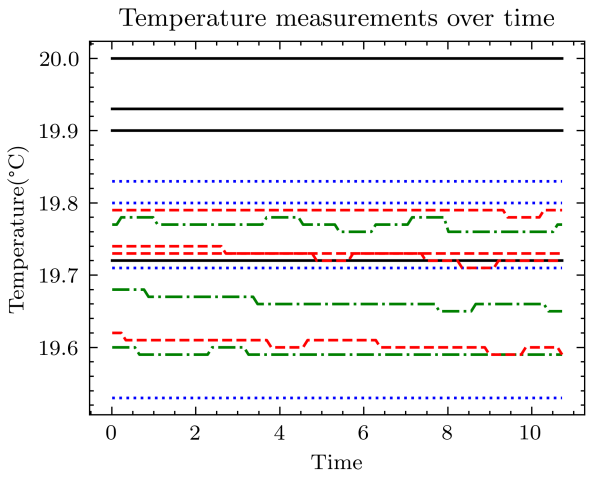

Figure 6.5: Measurement of 15 of the 16 temperature measurements. The last one is omitted for practical reasons. The thermistors are wrapped in paper to keep out air movements.

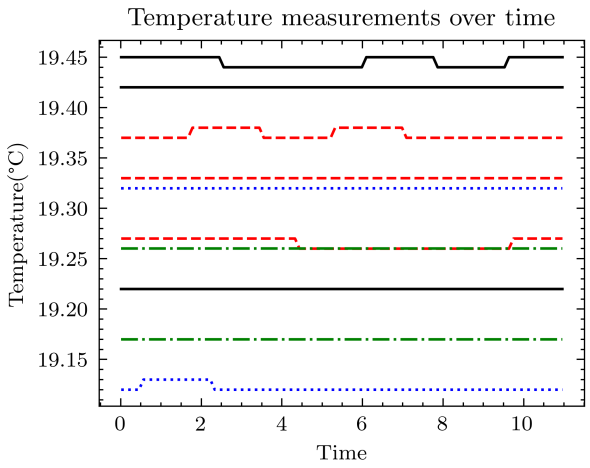

Figure 6.6: Verification of absolute temperature accuracy. The actual temperature was $19,46C$ with an uncertainty of maybe not more than $0,2K$. For this measurement all thermometers involved were placed in an aluminum block.

The temperature measurements are shown in Figure 6.5. It can be seen that the values are spread over $\pm 0,25C$. This is as expected from the tolerances of the thermistor used. It is most likely not a result of the resistor used in the divider, as for the prototype ones with a $0,1\%$ tolerance were used[5].

A verification of the absolute accuracy of the measurements was then made. The thermometer used as a reference was a $10k\Omega$ NTC but of a higher grade. This thermistor was calibrated by the Instrumentation group on the 15th story of EWI. Thanks from the authors go to Lukasz Pakula for the time he took in this calibration. The results of the first ten measurements are shown in Figure 6.6. The temperature measured by the reference thermometer was $19,46C$[6]. As can be seen the offset is between zero and $0,2K$. This is very acceptable.

The current measurement was then tested. Due to an ordering mistake, the amplifier used in the prototype has a gain of 50 instead of 100. This mostly affects the resolution, now being $20mA$ instead of $10mA$. As expected there was a significant offset that had to be accounted for. The gain error of the current measurement system was then determined by comparing the current measured of the shunt and the measurement of a multimeter believed to be accurate. The current measured by the shunt

[5] A 1% offset would influence the measurement by $0,22C$

[6] A four wire measurement of the thermistor was taken. All the thermometers involved were placed in an aluminum block with holes. Thermal grease was used for even better equalization.

Table 6.3: Verification of cell voltage measurements

Cell	Voltage, ADBMS	Voltage, DMM	Error
1	$3.9061V$	$3.9083V$	$-2,2mV$
2	$3.9088V$	$3.9101V$	$-1,3mV$
3	$3.8833V$	$3.8849V$	$-1,6mV$
4	$3.8995V$	$3.9013V$	$-1,8mV$

was $2,92A$, the multimeter indicated $2,8870A$, a difference of $1,1\%$. This is lower than the maximum expected error as calculated in Table 6.2. This gain error may of course also easily be corrected as a shunt resistor is linear.

Verification of the voltage measurement was performed on the four cells that were used in testing. The results are visible in Table 6.3. All measurement errors fall within $2,2mV$, lower than the specified $\pm 4mV$ as expected.

The SoC estimation based on coulomb counting was for the prototype computed on a laptop PC with measurement data being read over a serial communication from the master circuit. The estimation was tested by first fully charging the four cells used an setting $Q_0 = 0$. A resistor on a radiator was then used to discharge the four cells. The discharge was stopped when the first cell reached the cutoff of $2,5V$. The expected coulomb count for a 3Ah cell was $10800C$. A lower value was found. This has a combination of the following reasons: the ohmic efficiency of the cell is not 100%, the cells did not in reality have a capacity of 3Ah, one of the cells was less charged, the current measurement was off, the implementation of the integration was bad.

The balancing was for testing implemented with a simple threshold of $4,15V$. In this way the charging current, that at the end of the charging cycle is very low, can be bypassed fully. of course this algorithm prevents the charging of the cells to $4,2V$ but this is advisable according to the cell manufacturer.

7

Discussion

Following this work a few remarks are appropriate.

7.1. Errors in the practical implementation

In designing the prototype a few errors were made. Below these will be explained and their possible effect will be examined.

- Pull up resistors omitted on the PCB: the datasheet of the ADBMS1818 does not clearly indicate the fact that GPIO outputs are open-collector. Because of this they were omitted on the PCB. This error was remedied by using extremely fine varnished wire soldered directly between a resistor and the SMD package of the multiplexer. The negative effects of this modification are thought to be minimal. The same reasoning applies as to the settling time of the NTC readings.
- Bypass capacitors omitted on ADBMS1818 voltage reference pins: this error the authors can only blame on themselves. The remedy was again the use of extremely fine varnished wire. In this case hoverer is is thought to have caused excessive noise on the voltage reference potentials. This would be the result of increased series inductance and environmental voltages picked up.
- Ground plane present under transformer: the datasheet of the transformer advices against this. The presence of this ground plane probably negatively affects the filtering of the transformer.
- Various little mistakes: some connectors stick out of the PCB, mounting holes were forgotten and solder mask was not present between the pads of the ICs at great pain during soldering.

7.2. Errors of methodology

The project was wholly done in the D:DREAM hall building 23. While initially some testing with battery cells could be performed here at the desk, this was later prohibited. The fire protected battery room in this building was not yet finished and testing had to be halted. Some test that had been performed but for which no values had been recorded, could not be repeated. For example the SoC estimation algorithm.

8

Conclusion and Recommendation for Future Work

In conclusion, Delft Hyperloop requested an inherently modular battery management system which would support the current and future teams in prototyping with various battery sizes for their 'pod'. The present BMS fulfils the requirement of modularity as each slave board allows for the management of up to 18 battery cell groups and multiple slave boards can be connected together due to the daisy chain isolated SPI interface of the ADBMS1818 battery stack monitor IC. This would theoretically allow for the management of hundreds of cell groups.

Next to the modularity requirement, the present prototype fulfils all other mandatory requirements with a small footnote for two requirements which are delegated as minimal future work. There are 16 temperature sensor inputs per slave board which allow the master board to disconnect the battery from the pod if any cell temperature should be measured to be out of range. The slave boards facilitate over and under voltage protection as the ADBMS1818 IC is capable of measuring cell group voltages and communicating these to the master board over an isolated SPI interface. The BMS is also outfitted with a shunt resistor which allows for a measurement of the current through the battery pack, this measurement facilitates over current protection during (dis)charging. A cell balancing algorithm has been implemented on the master board and the master board allows full duplex communication with the rest of the pod as it is implemented on a STM32 micro controller with various digital interfaces.

For future work it is recommended to design a second iteration where the overseen component footprints are present on the PCB and where the current measurement amplifier has double the gain, which would allow a higher current measurement resolution. The second recommendation concerns the master board, it is presently implemented on an off the shelf STM32 Nucleo board as this is a team standard, however, a more custom and compact solution could be achieved by implementing a self designed micro controller board. Due to time constraints the BMS does not currently have requirement BMS.PEAK.1 implemented, this requirement concerns the allowance of a peak current above the protection limits for a short amount of time, however, due to the accessibility of all measurements and the flexible implementation of the algorithm on the master board, this is left as future work and should not be challenging to implement. The visual indication of the state (requirement BMS.SAFETY.1) has also not been implemented, but this is also easily implementable on the STM32 board by driving LED indication lights.

If future teams demand the requirement of having a more efficient system, a DC-DC converter can be used to power the IC instead of an emitter follower circuit, furthermore, an accurate state of charge estimation algorithm based on for example, a Kalmann filter or a non-linear observer should be implemented on the micro controller and the slave boards could also be outfitted with an active balancing circuit if even more efficiency is desired.

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A

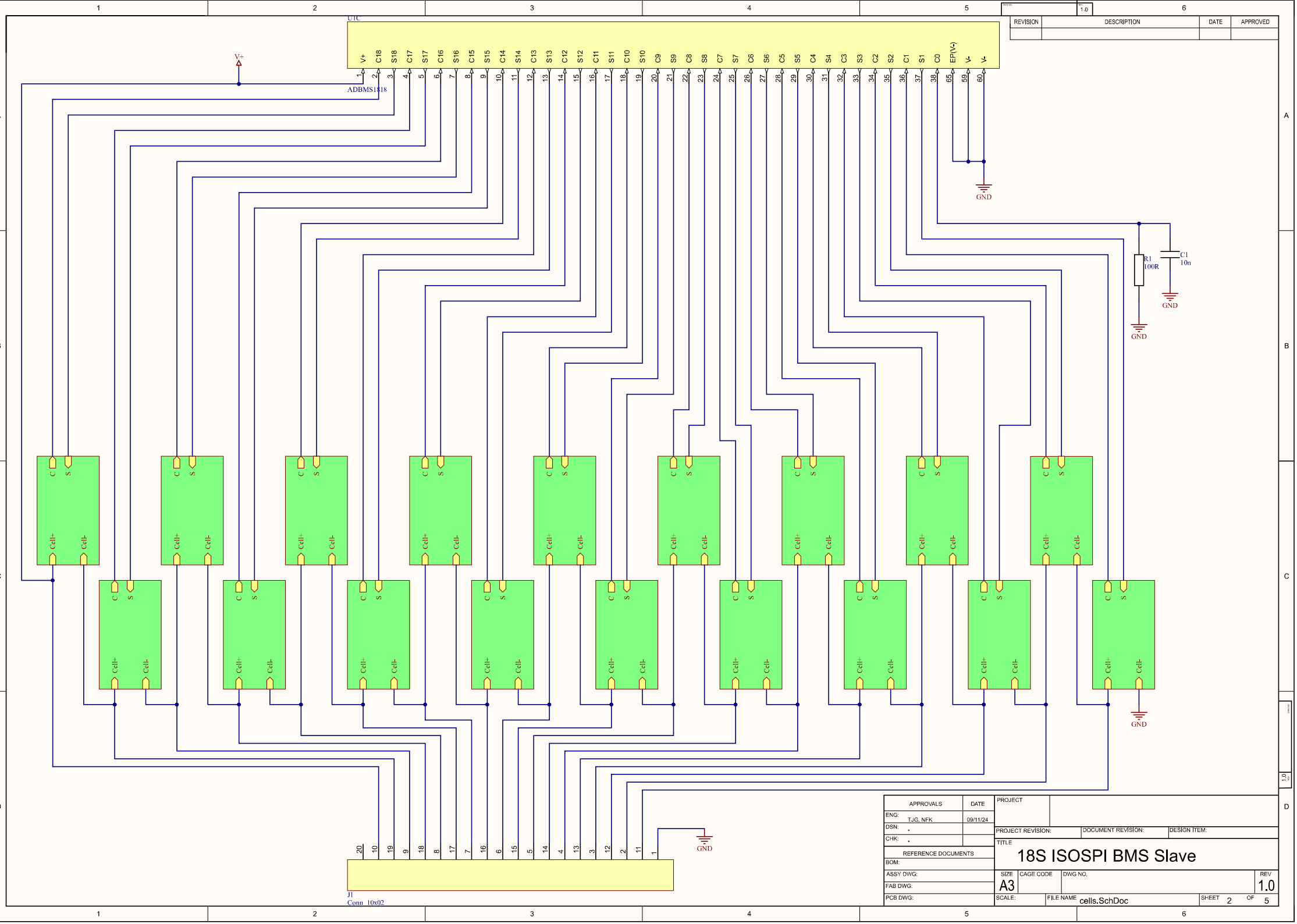
Prototype Electrical Schematic

This section includes a copy of the electrical schematic of the designed prototype. The first sheet shows the ADBMS1818 battery stack monitor on the left side (In the tilted orientation, as included in the document.) Connected to the IC are 18 repeating elements which are displayed as a green box. These repeating elements concern the balancing circuit, which can be seen on the second sheet. These 18 balancing circuits are connected to a connector on the right side, 18 battery cells will be connected to this connector.

On the second sheet, the balancing circuit can be seen. The bottom inputs represent the poles of a battery cell. These poles are connected to a MOSFET which is driven by the ADBMS1818 IC, if balancing is necessary,most of the excess energy from the battery cells will be dissipated in the resistor right of the MOSFET. On the top left an RC filter can be seen, this is an anti-aliasing filter for the voltage sensing input of the ADBMS1818 IC which can also be seen on the top left.

The third sheet shows the isolated SPI architecture. On the bottom left the ADBMS1818 IC can be seen with the communication ports only, There are two SPI channels labeled IMA, IPA, IMB and IPB, these four pins represent two differential signals which are isolated from the connector through the two isolation transformers which can be seen in the upper middle part of the sheet. The top part of the sheet shows the two connectors used for the isoSPI daisy chain communication and in the case of the bottom BMS slave, communication to the master board.

On the last page of the schematics a few different functions are implemented. In A1-2 the 5V power supply for the slave circuit is generated by Q1 used as a linear regulator. The drive signal for the base is generated in the ADBMS1818 and is around 5,7V. In A3-4 the internally generated reference voltage is buffered to be supplied to all 16 NTCs. The resistors in B1-C3 together with the NTCs connected to the connectors shown form the voltage divider used to measure the temperature. In B-C5 the inputs and the single output of the multiplexer used is shown. In A4-6 the amplifier for current measurement and a filter are shown. In B5-6 the GPIO outputs of the ADBMS1818 are connected to the contol lines of the multiplexer.



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PROJECT

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TITLE

18S ISOSPI BMS Slave

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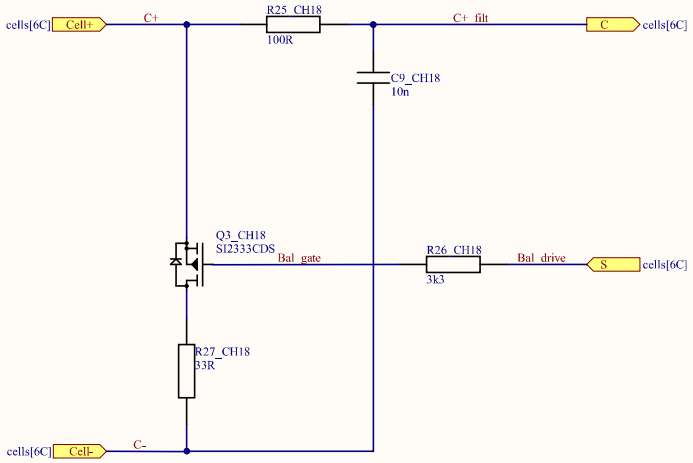

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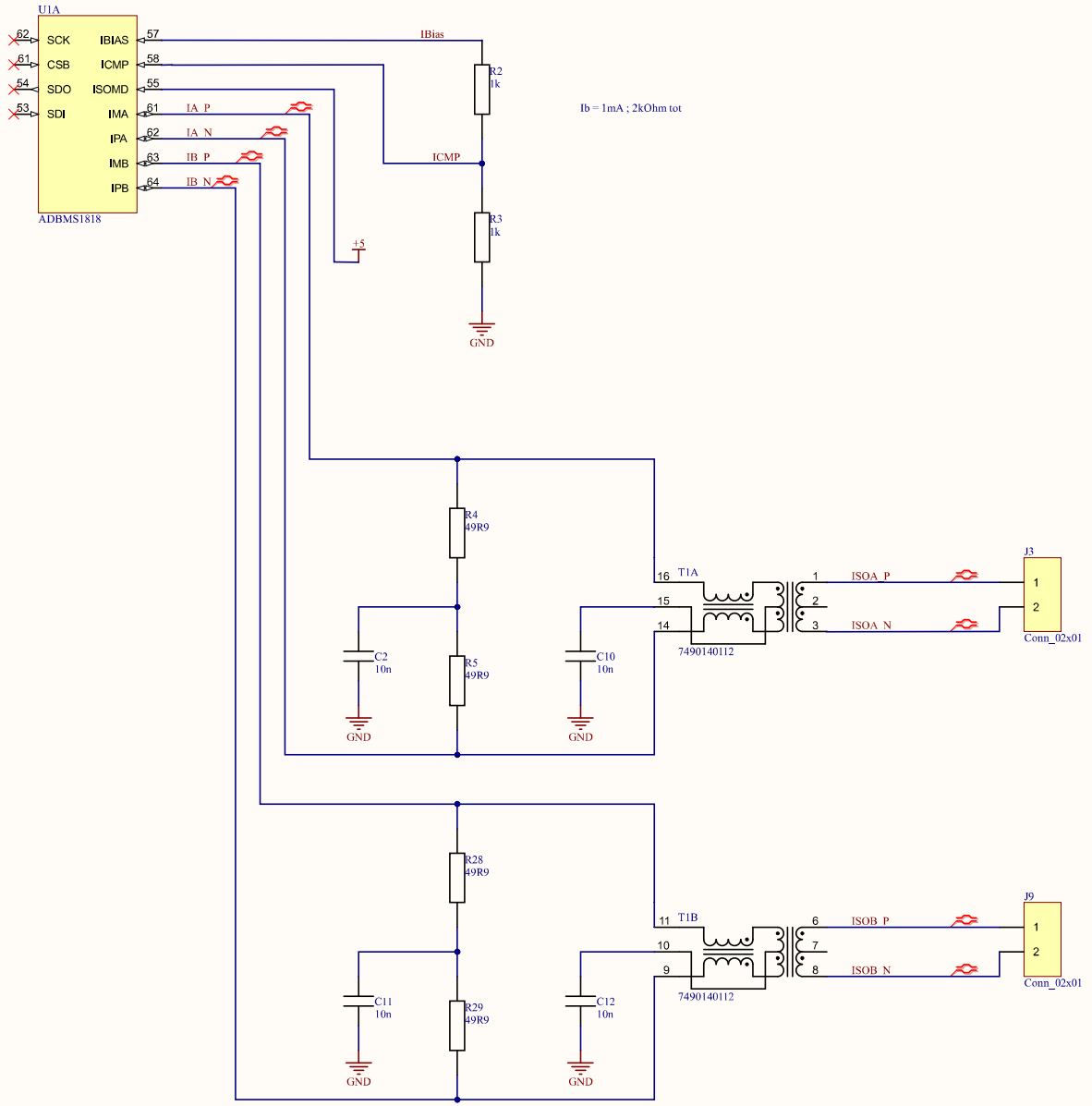

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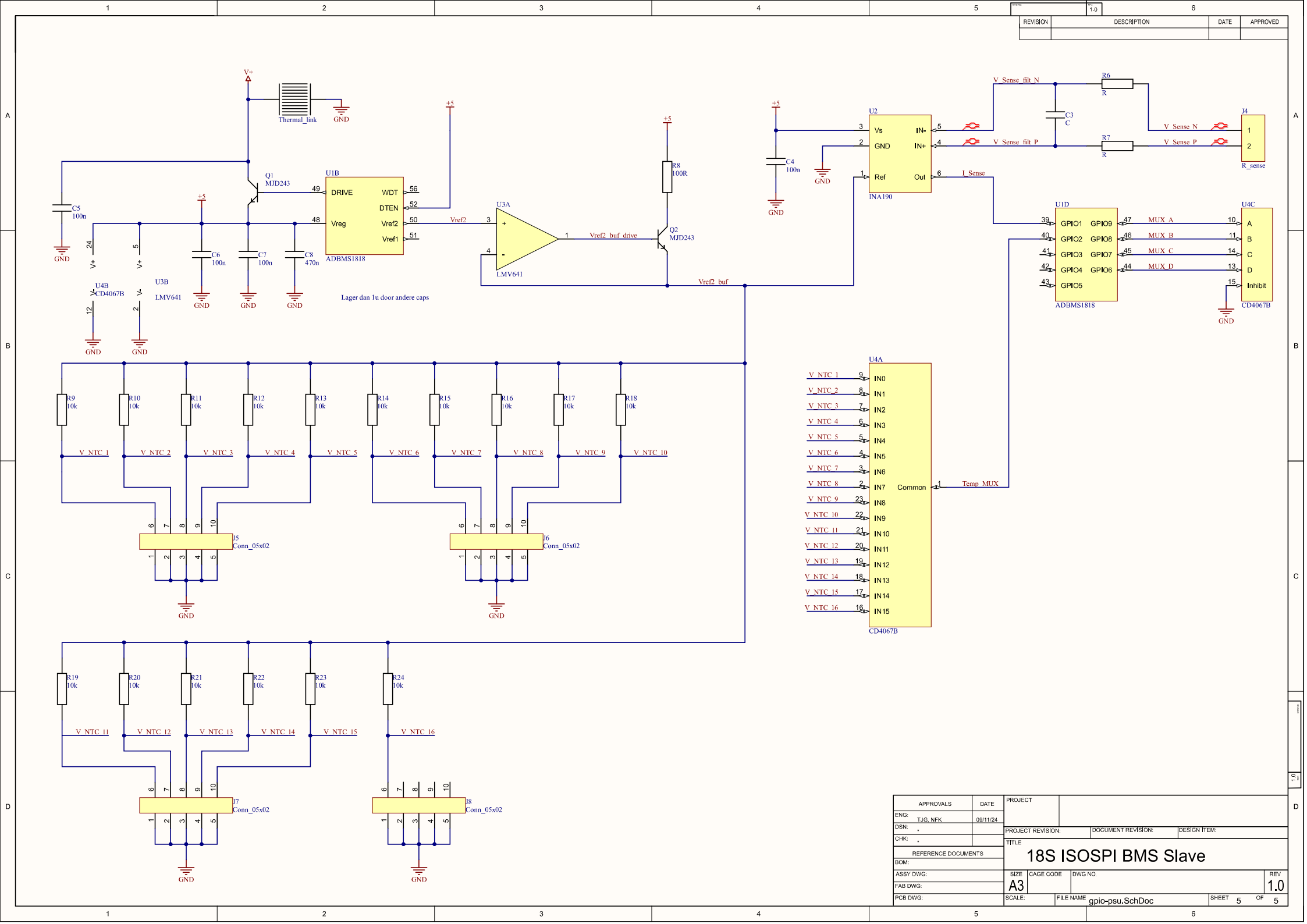
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