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A Crystal-Less Clock Generation Technique for Battery-Free Wireless Systems

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***Abstract*— The size of wireless systems is required to be reduced in many applications, such as ultra-low-power sensor nodes and wearable/implantable devices, where battery and crystal are the two main bottlenecks in system miniaturization. In recent years, battery-free radios based on wireless power transfer (WPT) have shown great potential in miniature wireless systems, while a reliable on-chip clock without a crystal remains a design challenge. Conventional methods utilized the RF WPT tone as the reference for clock generation, but the high RF frequency leads to high power consumption. In comparison, using a lower WPT frequency results in an antenna with a larger size. In this work, the 2^{nd}-order inter-modulation (IM2) component of the two RF WPT tones is extracted to lock an on-chip oscillator, providing a low-jitter PVT-robust clock. In this way, the wireless systems can benefit from: 1) The clock recovery circuits operate at a low IM2 frequency, reducing the power consumption. 2) The WPT can be set to a high RF frequency to minimize the antenna. Fabricated in 65 nm CMOS process, the proposed crystal-less clock generator takes a small area of 0.023 mm^2 in a wireless system chip. Measured results show −92 dBc/Hz@10 kHz phase noise and 6.8 μW power.**

***Index Terms*— Battery-free, clock generator, wireless power transfer (WPT), injection locking, inter-modulation.**

I. Introduction

THE proliferation of the internet of things (IoT) requires the wireless nodes to be miniaturized and battery-free in many applications. For example, a battery-free counter-counterfeit chip is minimized to 116 μm×116 μm without external components [1]. Especially for wireless implants, a small size takes an important role in alleviating surgical injury and mitigating infection [2], [3], such as a 0.125 mm^2 wireless neural sensor chip in [2] and a 0.009 mm^3 neural stimulator in [3]. To miniaturize the wireless systems, it is effective to eliminate the bulky components such as batteries and crystals. Nowadays, wireless power transfer (WPT) is widely used to minimize or eliminate the battery, while the crystal is still desired to provide a reference frequency for system clock or local oscillator (LO) of a wireless system.

For clock generation, most wireless systems utilize a crystal as the frequency reference, leading to bulky size and high power consumption [4]. With a size of 10s to 100s of mm^3, the crystal becomes the main bottleneck in the system miniaturization due to the low integration [5], [6]. Therefore, on-chip oscillators without a crystal are usually used to reduce the system size and power consumption [7], [8], [9]. However, the on-chip oscillators suffered from large jitters and PVT variations, leading to the expense of performance degradation or off-chip tuning.

In a battery-free wireless system, the wireless-powering tone can be utilized as a frequency reference. In this way, a stable clock signal can be generated without a crystal. For example, the clock recovery from a RF powering tone generated a synchronized clock for a wireless system [10], [11]. However, the clock recovery circuits dissipated high power consumption due to the high RF powering frequency, which is not applicable in a low-power wireless system, especially in a battery-free system. Therefore, efforts have been made to reduce the power consumption. For instance, two coil antennas were utilized for data telemetry and clock recovery, respectively, where the clock recovery frequency was set to be much lower than the RF frequency to reduce the power of clock generator [12]. Nevertheless, the two-antenna solution significantly enlarge the size of wireless systems, e.g., 0.5 cm^3 in [12].

In this paper, we propose a crystal-less clock generation technique realizing low power and miniature chip size for battery-free wireless systems. Instead of a single power-transfer tone in conventional battery-free systems, two RF tones are used for WPT. The proposed circuits extract the 2^{nd}-order intermodulation (IM2) component, to drive an injection-locked ring oscillator (ILRO), achieving a wide lock range against PVT variations. As a prototype, the

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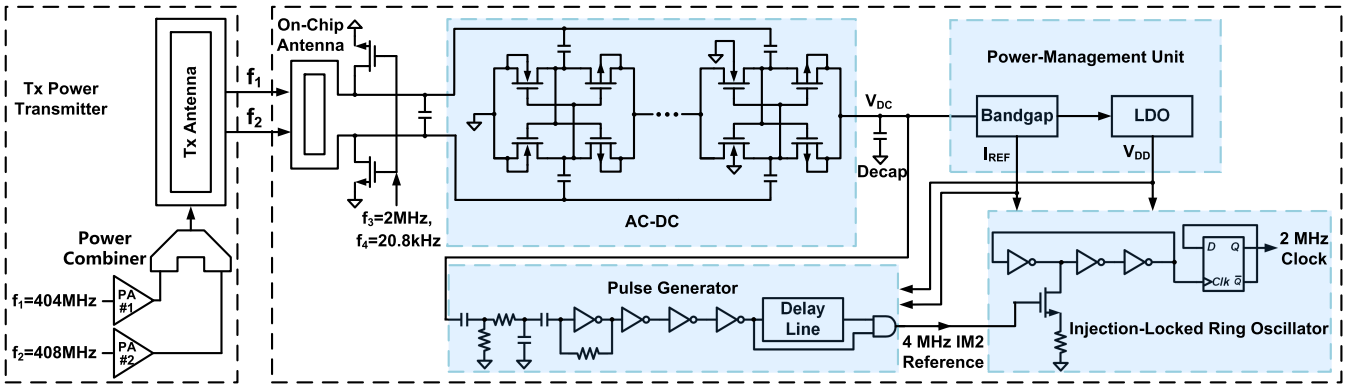


Fig. 1. Top architecture of proposed clock generation technique for battery-free wireless systems.

proposed clock generation technique is demonstrated in a fully-integrated battery-free neural-recording chip fabricated in 65 nm CMOS process. The neural-recording chip is battery-free, which is wirelessly powered by an external power transmitter. All the circuits are integrated inside the 2 mm×2 mm on-chip coil antenna. The neural-recording chip utilizes the crystal-less clock generation technique to provide a global clock for signal-acquisition unit and backscatter communication. The signal-acquisition unit includes an analog front-end (AFE) and an ADC to amplify and digitize neural signals, and both of the two blocks require clock signals. In addition, the communication block uses the clock to encode the digital neural data, which drives the backscatter switches. In this way, the prototype wireless system have benefited from: 1) The WPT tones is set to a 404 MHz high frequency to ensure a small antenna size, i.e., 2 mm×2 mm. 2) As the IM2 component can reach a much lower frequency than the RF powering tones, the power consumption of crystal-less clock generation is significantly reduced compared to conventional works.

The rest of this article is organized as follows. Section II presents the system architecture of the proposed clock generation circuit in a battery-free system. The circuit designs are detailed in Section III, and the measured results are summarized in Section IV. Finally, Section V concludes the paper.

II. System Architecture

The system architecture based on the proposed clock generation technique is shown in Fig. 1, including an off-chip power transmitter and a fully-integrated battery-free wireless chip. The power transmitter includes two RF signal generators, two power amplifiers (PAs), a power combiner, and a PCB coil antenna. The proposed crystal-less clock generation technique is implemented on the CMOS chip, which includes an on-chip rectenna (antenna & rectifier), a power-management unit, a pulse generator, and an ILRO.

In comparison to the two-antenna solution [12], our chip includes a single antenna to reduce the system volume, which harvests energy through wireless power transfer (WPT). Meanwhile, backscatter circuits are also implemented for data communication. To reduce the size of antenna, the WPT link operates at a high RF frequency (400 MHz frequency band), realizing an on-chip antenna with 2 mm×2 mm dimension. All the circuits locate inside the loop antenna, resulting in a 2 mm×2 mm die area.

Compared to the conventional RF-based clock recovery [11], we design a clock generator based on the IM2 component (f_{IM2}) of the two RF powering tones. The IM2 frequency f_{IM2} is much lower than the WPT frequencies, so the proposed clock generator consumes less power than the conventional RF-based clock recovery.

The operating principle and flow of proposed clock generation technique can be analyzed by equations. The powering tones $f_1 = 404$ MHz and $f_2 = 408$ MHz coming from two power amplifiers (PAs) is summed by a power combiner, and then emitted by a PCB coil antenna. Then, the two powering tones are harvested by the on-chip antenna and converted into a DC voltage (V_{DC}) by the subsequent rectifier. Afterwards, the rectified DC voltage V_{DC} is regulated by a power-management unit (PMU), which provides supply voltages V_{DD} and biasing currents I_{REF} to pulse generator and ILRO. The input signal of rectifier can be expressed by:

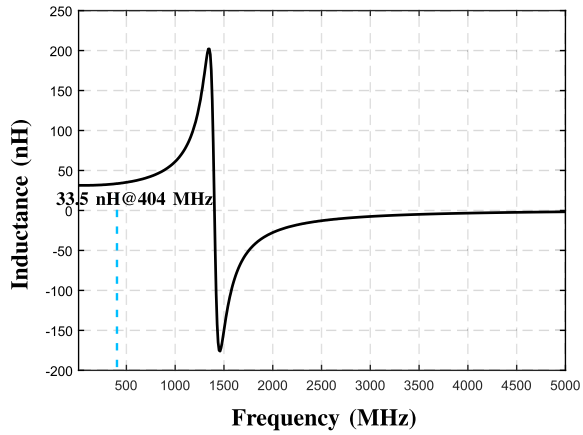
$$\mathrm{x(t)} = (\mathrm{A_1}\cos\omega_1\mathrm{t} + \mathrm{A_2}\cos\omega_2\mathrm{t})\mathrm{G_{ant}}(\omega), \tag{1}$$

where $A_1\cos\omega_1 t$ and $A_2\cos\omega_2 t$ are the two WPT tones, and $G_{ant}(\omega)$ is the link gain. Due to the nonlinearity of rectifier, there will be intermodulation components at the output:

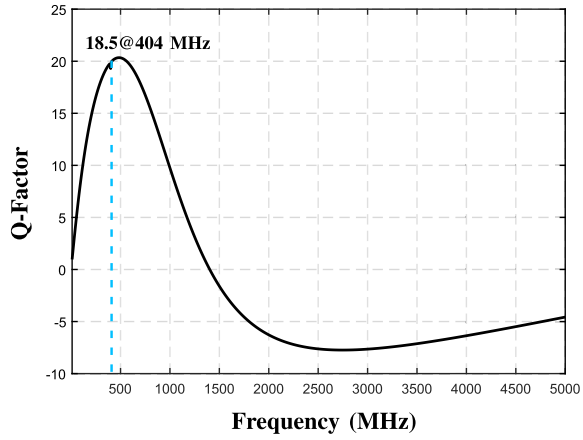
$$\begin{aligned}\mathrm{y(t)} \approx\ & \alpha_1((A_1\cos\omega_1 t + A_2\cos\omega_2 t)G_{ant}(\omega)) \\ & +\alpha_2((A_1\cos\omega_1 t + A_2\cos\omega_2 t)G_{ant}(\omega))^2 \\ & +\alpha_3((A_1\cos\omega_1 t + A_2\cos\omega_2 t)G_{ant}(\omega))^3,\end{aligned} \tag{2}$$

where the IM2 component $\alpha_2 G_{ant}(\omega)A_1A_2\cos(\omega_2-\omega_1)t$ is explored for clock generation. By setting gap between the two WPT frequencies, the IM2 tone locates at a lower frequency than the RF WPT tones but close to the f_{SYS}. As a result, the pulse generator and the ILRO realize the low-power clock for the chip system.

To realize a reliable clock for the wireless system, our clock generator includes a pulse generator and an ILRO. The pulse generator extracts the IM2 component ($f_2 - f_1$) and suppresses other undesired signals. To achieve a clean IM2 frequency, we apply an RC network to suppress the



(a)



(b)

Fig. 2. On-chip antenna: (a) Inductance and (b) Q-factor.

undesired frequency components. For instance, the rectifier output includes the WPT tones f_1 and f_2, as well as f_3 and f_4 induced by backscattering communication. Afterwards, the IM2 component is amplified and shaped into a pulse signal, which serves as an reference for the subsequent ILRO. The ILRO is designed to lock to the IM2 component, where the pulses with optimized width is injected into the ILRO to achieve the injection lock and provide a low-noise clock $f_{\mathrm{SYS}} = 2$ MHz.

III. Circuit Designs

The details of the circuit are presented in this section. Firstly, we introduce the designs of the coil antenna in the power transmitter and the on-chip rectenna in the CMOS chip. Secondly, the circuit of the pulse generator is described. Finally, we details the design of clock generator, and discussed how the lock range of ILRO is maximized against PVT variations.

A. On-Chip Rectenna

For the application of medical implant, the chip is designed with an on-chip antenna to minimize the system size. Fabricated in the 65 nm CMOS process, the RF WPT frequency is

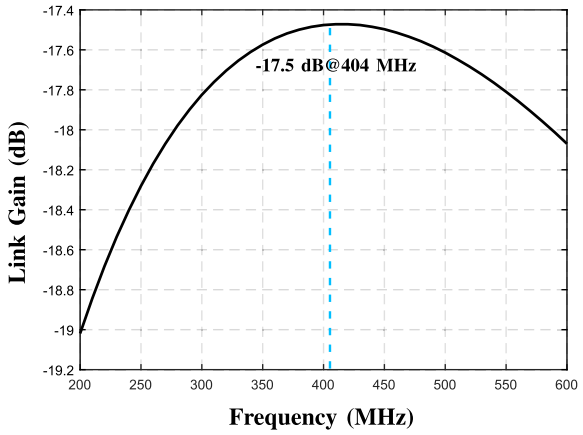
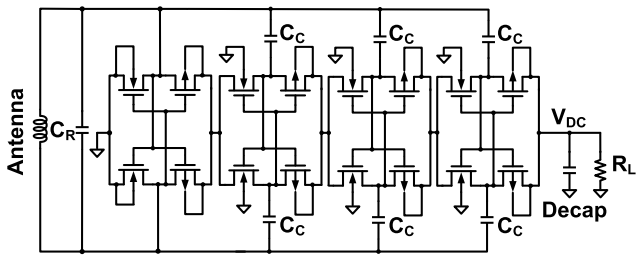
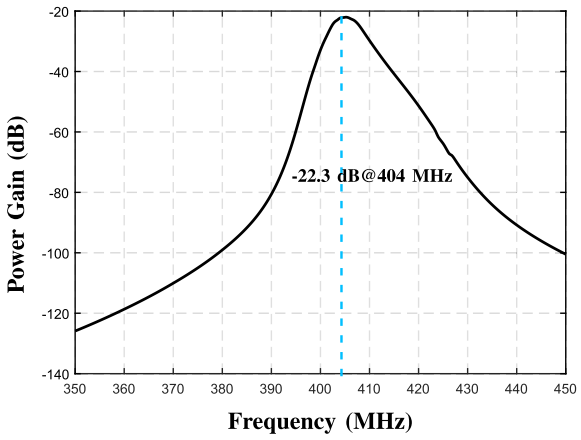


Fig. 3. Simulated link gain between transmitting and receiving antennas.



(a)



(b)

Fig. 4. Rectenna: (a) Circuit and (b) Simulated frequency response.

set to 404 MHz, resulting in an on-chip coil antenna with a dimension of 2 mm×2 mm. Fig. 2(a) shows the simulated inductance of the on-chip antenna versus the operating frequency, while Fig. 2(b) illustrates the simulated Q-factor, which is optimized at the 404 MHz frequency. It can be seen that the optimized on-chip antenna has an inductance of 33.5 nH and a Q-factor of 18.5. Afterwards, the transmitting (Tx) coil antenna is also optimized for maximal link gain, as shown in Fig. 3. At 404 MHz, the simulated link gain between the antenna pair is -17.5 dB at 1-cm range towards the ultra-small on-chip antenna.

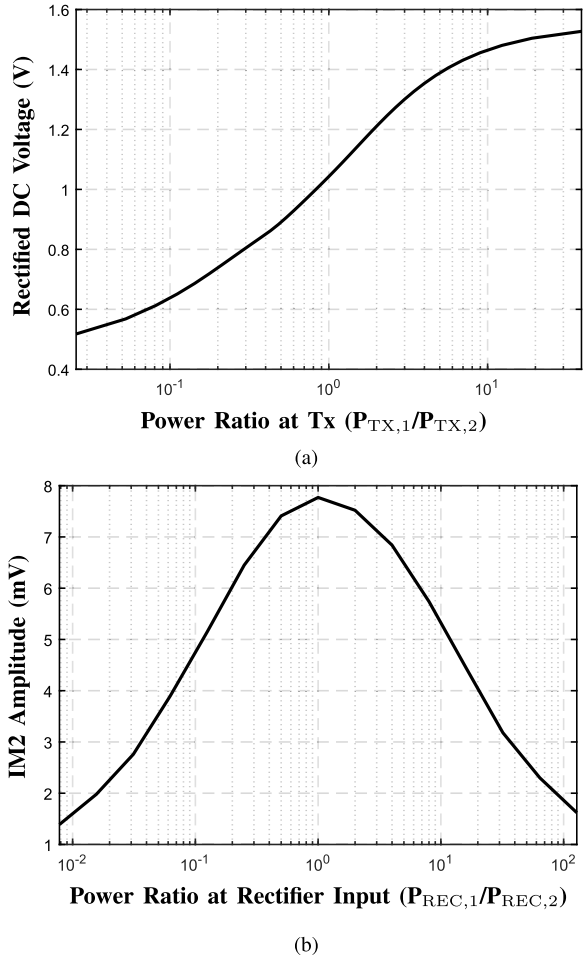


Fig. 5. (a) Harvested DC voltage vs. Tx power ratio ($P_{\mathrm{TX},1}/P_{\mathrm{TX},2}$). (b) Simulated IM2 amplitude vs. power ratio at rectifier input ($P_{\mathrm{REC},1}/P_{\mathrm{REC},2}$).

The AC-DC rectifier is co-designed with the antenna targeting at a high power gain. As illustrated in Fig. 4(a), the number of the differential-driving rectifier cells [13] is optimized to be four stage for maximal RF-to-DC power-transfer gain. The resonant capacitor C_{R} is designed to resonate with the antenna, and the coupling capacitors C_{C} are used for AC coupling. Fig. 4(b) illustrates the simulated frequency response of the rectenna. At WPT frequency f_1, the overall power gain is optimized and reaches -22.3 dB at 1-cm range.

Instead of the single-tone in conventional WPT systems, we adopt two WPT tones delivered from the transmitter to the CMOS chip. The gap between the two tones are set to be 4 MHz, i.e., $f_1 = 404$ MHz and $f_2 = 408$ MHz. Thus, the IM2 component ($f_2 - f_1 = 4$ MHz) of the two tones can be extracted to generate the clock signal for the system, reducing the power compared to the conventional RF-based clock recovery.

Compared to single-tone WPT, the rectified DC voltage and IM2 amplitude are related to the power ratio of the two tones. The total power of the two tones ($P_{\mathrm{TX},1}$ and $P_{\mathrm{TX},2}$) is fixed to 40 mW. Meanwhile, we increase $P_{\mathrm{TX},1}$ and decrease $P_{\mathrm{TX},2}$ to observe the rectified DC voltage and IM2 amplitude. Since the rectenna resonates at the frequency f_1, the power gain at f_1 is higher than f_2. As a result, the rectified DC voltage rises versus the increasing of power ratio $P_{\mathrm{TX},1}/P_{\mathrm{TX},2}$, as shown in Fig. 5(a).

In this work, the IM2 of the two WPT tones at the rectifier output is extracted for clock generation. Note that the AC-DC rectifier is a typical nonlinear module, so various frequency components are produced at the rectifier output. The two input tones of the rectifier can be represented by

$$V_1 = V_{m1} \cos 2\pi f_1 t, \tag{3}$$

$$V_2 = V_{m2} \cos 2\pi f_2 t. \tag{4}$$

Due to the 2^{nd}-order nonlinearity in the rectifier circuit, the $(V_1 + V_2)^2$ component appears at the output of the rectifier, resulting in an IM2 tone $f_2 - f_1$. The amplitude of IM2 component follows the relationship $V_{\mathrm{IM2}} \propto V_{\mathrm{m1}} \times V_{\mathrm{m2}}$.

The amplitude of IM2 component can be increased by optimizing the power ratio of two tones at the rectifier input. In the proposed design, the amplitude of IM2 component is critical since it directly determines the lock range, which reflects the ability to avoid PVT variations. The IM2 power versus power ratio of f_1 and f_2 at the rectifier input is simulated in Fig. 5, where the total power is kept to be 150 μW ($P_{\mathrm{REC},1} + P_{\mathrm{REC},2}$). We represent the power ratio of the two tones at rectifier input by a parameter $\alpha = P_{\mathrm{REC},1}/P_{\mathrm{REC},2}$, where $P_{\mathrm{REC},1}$ and $P_{\mathrm{REC},2}$ represent the power of f_1 and f_2 at the rectifier input, respectively. The simulation result shows that the IM2 tone reaches the peak when the two input tones of rectifier are with the same power, i.e., $P_{\mathrm{REC},1} = P_{\mathrm{REC},2}$.

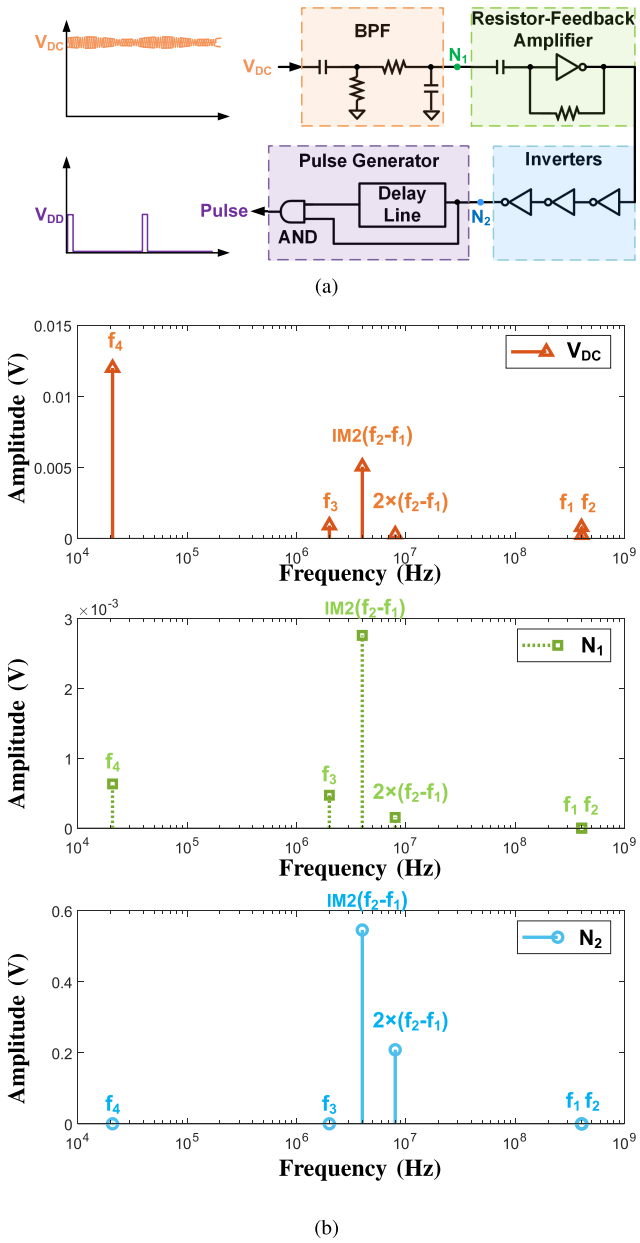
B. Pulse Generator

The pulse generator shapes the IM2 signal into optimized pulses for injection locking, and filters down other frequency components as well. At the output of AC-DC rectifier, there are various frequency components, while the injection locking only requires the IM2 signal $f_2 - f_1$. In addition to the wireless powering tones f_1 and f_2, there are other frequency signals introduced by backscattering communication, such as $f_3 = 2$ MHz and $f_4 = 20.83$ kHz shown in Fig. 1. The proposed clock generator is implemented in the neural-recording chip, and the neural data is encoded to drive the switches for backscatter communication. The backscatter signal includes two frequency components, where $f_3 = 2$ MHz is the frequency of the encoding carrier, and $f_4 = 20.83$ kHz is the sample rate of the signal-acquisition unit. At the rectifier output, there are several frequency components including

$$f = af_1 \pm bf_2 \pm cf_3 \pm df_4, \tag{5}$$

where the parameters a, b, c, and d are integers. In general, the high-order tones show low power, which can be neglected.

The base-frequency and 2^{nd}-order tones with relatively higher power should be taken into account, such as $f_2 - f_1$, $2\times(f_2 - f_1)$, f_3, f_4, f_1, f_2. Subsequent to the AC-DC rectifier, the pulse generator converts the weak IM2 signal into strong pulses to enhance the injection locking. As shown in Fig. 6(a), we adopt a bandpass RC filter to suppress undesired frequency tones in V_{DC}. As a result, the filter is designed to be with a center frequency of IM2 ($f_2 - f_1 = 4$ MHz) and a passband of



(a)

(b)

Fig. 6. IM2 pulse generator: (a) Circuit. (b) Signal spectrum in nodes V_{DC}, N_1, and N_2.

2.5 MHz−15 MHz. The frequency component $2\times(f_2-f_1)$ is the 4^{th} harmonic generated by the rectifier, which is -25 dB lower than the IM2 signal f_2-f_1 in V_{DC}. As a result, the component $2\times(f_2-f_1)$ shows little impact on the injection lock. Then, an inverter-based amplifier is used to enlarge the IM2 signal while a feedback resistor is used to set the DC operating point. Finally, the IM2 signal is further amplified into a full-scale square waveform by cascaded inverters.

The frequency response of the pulse generator is simulated in Fig. 6(b). The simulation only incorporates the dominated tones, while the weak tones are neglected. At the node V_{DC}, the magnitude of IM2 and other frequency components are shown in Fig. 6(b), top. At the node N_2, we can see that the IM2 tone dominates all the frequency components, indicating that

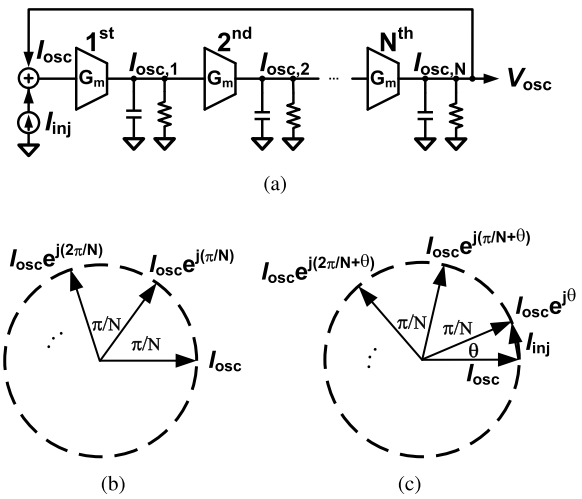


Fig. 7. Analysis of injection locking: (1) Circuit model. (b) Phasor diagram of free-running state. (c) Phasor diagram of injection-locked state.

the filter has effectively suppressed undesirable interference (Fig. 6(b), bottom).

To provide an optimized pulse signal for injection locking, it is necessary to convert the IM2 signal into narrow pulses. As analyzed in [14], narrow-pulse shaping of the injected signals can help to improve the noise performance of ILRO. In this design, the pulse generator adopts a delay line and an AND gate to convert the amplified square signals into pulses. The delay line employs three identical delay cells to provide a ns-level time delay, where each cell is composed by a current-starved inverter controlled by the bandgap reference I_{bias}, and two other inverters used to re-shape the delayed signals. Finally, the AND gate is used to provide a narrow pulse injected into the ring oscillator.

C. Injection-Locked Ring Oscillator

An ILRO is designed to be locked to the IM2 component of two wireless powering tones, which generates a stable clock signal while filtering out undesired tones. The two wireless frequencies f_1 and f_2 generates the IM2 component f_2-f_1, replacing a crystal to serve as the reference of ILRO. In this way, the IM2 frequency f_2-f_1 is much lower than the RF powering frequencies f_1 and f_2, so the clock generator consumes much lower power than the conventional RF based clock recovery circuits. A ring oscillator structure is adopted for a small die area and low power. The target of circuit optimization is to provide a reliable clock in a wide range of applications [14], [15], [16], [17], [18], [19], [20], [21]. In this section, the design considerations of ILRO circuit is discussed.

To generate a reliable clock immune to PVT variations, it's necessary to maximize the lock range. Given the free-running frequency ω_0 and the injected frequency ω_{inj}, the lock range can be defined as [22]:

$$\text{lock range} := \omega_{0,\max} - \omega_{0,\min}, \tag{6}$$

where $\omega_{0,\max}$ and $\omega_{0,\min}$ are the maximal and minimal free-running frequencies that can be locked to ω_{inj},

respectively. The symbol ":=" means "be defined as". In addition, the upper edge and the lower edge of the lock range is represented by $\omega_{0,\max}$ and $\omega_{0,\min}$, respectively. If the free-running frequency of ILRO exceeds the lock range, the oscillator will not be able to locked to the injected frequency, leading to injection pulling.

Conventional methods such as Alder's equations [22], [23], [24], [25] and phasor diagram [26], [27], [28], [29] analyzed the injection locking based on the injection current. Conventional injection locking methods result in limited lock range, where the injection current $i_{\text{inj}}(t)$ should be strong and the injection frequency w_{inj} is required to be close to the free-running frequency w_0.

A periodic current $i_{\text{inj}}(t)$ injects to the oscillator, and the frequency w_{inj} of the injection current is close to the free-running frequency w_0 of the ring oscillator. If there is a phase difference θ between I_{inj} and I_{osc}, the oscillating is shifted to a new frequency w_1, resulting in an additional current flowing into the oscillator. To satisfy the Barkhausen criteria [30], each stage should provide a phase shift of $-\pi/N$ to sustain the oscillation. As the periodic current I_{inj} is injected into a stage, an extra phase shift θ changes the oscillating period, resulting in injection locking to ω_{inj}. The lock range is inversely proportional to the stage number of ILRO for a given $I_{\text{inj}}/I_{\text{osc}}$. Likewise, the lock range is proportional to $I_{\text{inj}}/I_{\text{osc}}$ at a given stage number [29].

In this work, we design an ILRO with three-stage single-ended ring oscillator based on inverter cells. The circuit is shown in Fig. 8, where each stage contains a current-starved inverter for low power operating and two additional inverters for waveform shaping. At the output of the current-starved inverter, there is a capacitor that determines the delay time T_0 of each stage. The free-running frequency of the ring oscillator is expressed by

$$f_0 = \frac{1}{2NT_0}(N = 3), \tag{7}$$

The bias current and the capacitor are set to operate the ring oscillator around the 4 MHz target frequency. At a low power, the charging and discharging of the capacitors are relatively slow, resulting in a triangular wave at the output of the current-starved inverter. To improve the jitter performance, another two inverters in each stage shape the signal into a full-swing square wave. As the input, the voltage pulses coming from the pulse generator is converted into current pulses through the injection stage (including a NMOS transistor and a resistor). Acting as a degenerator, the source resistor R_S is used to control the gain of the injection stage, optimizing the lock range and noise performance.

We develop a time-domain model based on the theory in [31] for the injection locking process. In the ring oscillator, we analyze the time delay of each cell in different conditions. Three points in the ring oscillator are picked up, which are marked by N_1, N_2, and N_3 in Fig. 8. In free-running state, each stage in the oscillator has a delay of T_0, resulting in an oscillating frequency of $1/6T_0$. If the pulse signal is injected into N_2 through the injection transistor, then the delay from N_1 to N_2 will be periodically affected. Then, the injection

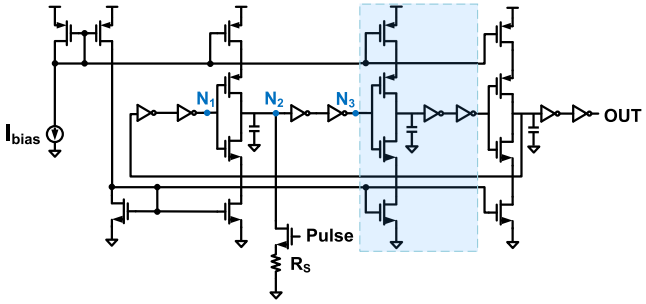


Fig. 8. ILRO circuit.

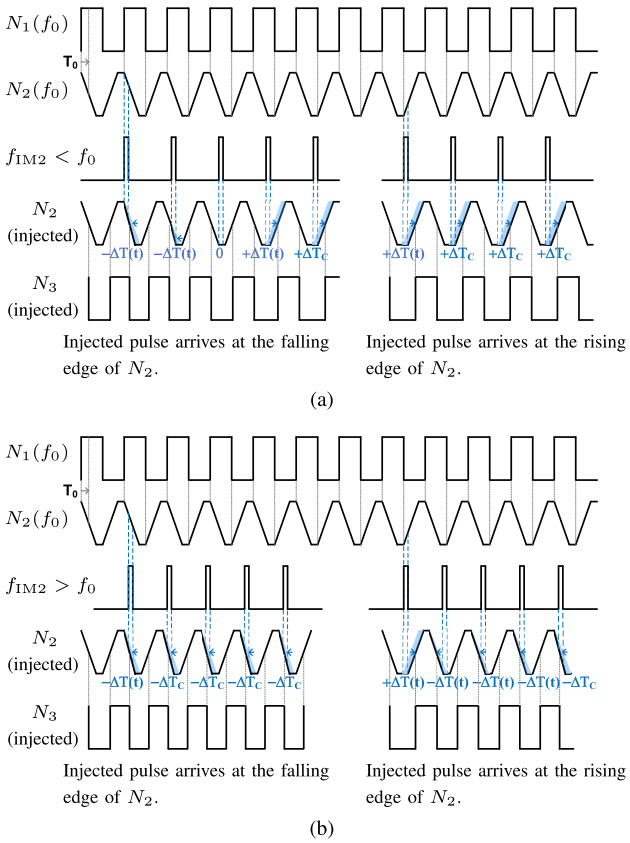


Fig. 9. Time-domain analysis at (a) a lower-frequency injected signal and (b) a higher-frequency injected signal.

current breaks the free-running state, and pushes the ring oscillator into a new steady state. Fig. 9(a) and Fig. 9(b) show the cases that the ring oscillator reacts to an injection current with a lower and higher frequency, respectively.

Firstly, we analyze the case that the injection frequency (f_{IM2}) is lower than the free-running frequency (f_0), as shown in Fig. 9(a). Generally, the injected pulse has a random phase difference with the signal of N_2. If the injected pulse arrives at the falling edge of the waveform at N_2, the falling of N_2 will be accelerated due to the injected pulse. Then, the signal of N_2 will be pushed towards the left side. We assume the falling time is shortened by $\Delta T(t)$, where $\Delta T(t)$ changes with the injection pulse. As the signal of N_2 is pushed towards left, the injected pulse will arrive at the rising edge of the N_2 signal after several periods. Then, if the injected pulse meet the

rising edge of the N_2 signal, the injected pulse will delay the rising of the N_2 by $\Delta T(t)$ towards right. This process is illustrated in Fig. 9(a), left. Apparently, if the injection pulse meets the rising edge of N_2 at the beginning, the waveform of N_2 will be directly shifted towards right, as shown in Fig. 9(a), right. Finally, the waveform at N_2 enters a steady state, i.e., injection-locked state, when the shifting time becomes a constant $\Delta T(t) = \Delta T_C$. During the locking process, the delay from N_1 to N_3 becomes $T_0 + \Delta T(t)$, depending on the frequency difference. $\Delta T(t)$ keeps changing till the oscillator is locked, then we have $\Delta T(t) = \Delta T_C$ and

$$6 \times T_0 + 2 \times \Delta T_C = T_{IM2}, \tag{8}$$

where T_{IM2} is the period of IM2 pulse signal. Note that the time drift ΔT_C depends on the frequency difference between the f_{IM2} and f_0.

From the analysis above, we can see that the oscillator can be locked within the lock range. In addition, the locking will happen no matter even there is a big initial phase difference between the injected pulse and the N_2 signal.

Secondly, the other injection locking case is shown in Fig. 9(b), where the injection frequency (f_{IM2}) is higher than the free-running frequency (f_0). If the injected pulse comes at the falling edge of N_2, the falling edge will be shifted by $\Delta T(t)$ towards left. After several cycles, the oscillator is locked and $\Delta T(t) = \Delta T_C$. If the injected pulse meets the rising edge of N_2, the oscillating waveform will be shifted until the injected pulse arrives at the falling edge. In this way, the injection locking will be completed as the time drift becomes a constant of $\Delta T(t) = \Delta T_C$. The delay from N_1 to N_3 is reduced to $T_0 - \Delta T(t)$, increasing the oscillating frequency. The period of the oscillator in locked state can be expressed by

$$6 \times T_0 - 2 \times \Delta T_C = T_{IM2}. \tag{9}$$

Based on the analysis, we can conclude that the injected pulse changes the oscillator frequency by delaying the rising of N_2 signal (when $f_{IM2} < f_0$) or accelerating the falling of N_2 signal (when $f_{IM2} > f_0$). When $f_{IM2} < f_0$, the time drift $+\Delta T_C$ can achieve a relatively large value as long as it is smaller than $1/f_0$. However, when $f_{IM2} > f_0$, the time drift $-\Delta T_C$ is limited since the falling time of N_2 is greater than 0, so we have the delay from N_1 to N_3

$$T_0 - \Delta T_C > 0. \tag{10}$$

Thus, the time drift has different limitations in these two situations, resulting in an asymmetrical lock range.

The source degenerator R_S of the injection transistor is optimized to improve the lock range. As shown in Fig. 8, the injection stage is a common-source stage with a degeneration resistor R_S, which converts the injection pulse into a periodic current signal. The source degeneration resistor improves the linearity of the injection stage, impacting the lock range. In this case, we adjust the value of R_S to observe the change of lock range of ILRO, as given in Fig. 10. Accompanying the increasing of R_S, the lock range is shortened since the gain of injection stage is reduced.

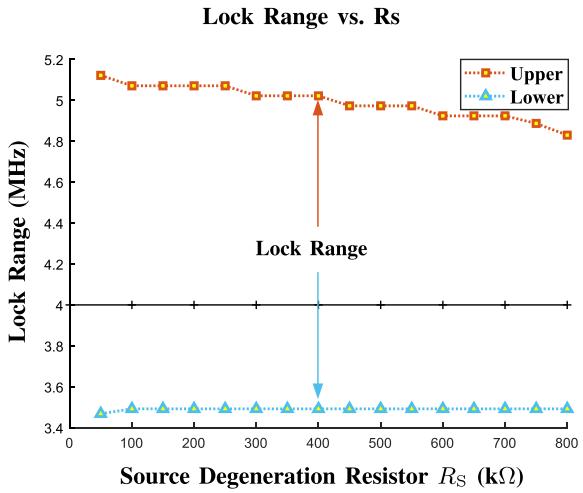


Fig. 10. Lock range vs. source degeneration resistor R_S.

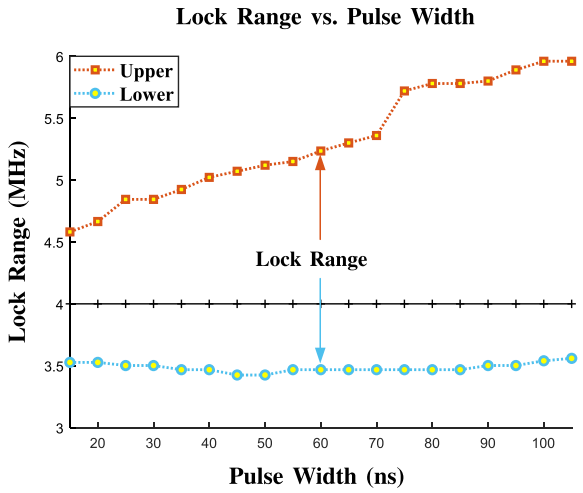


Fig. 11. Lock range vs. injected pulse width.

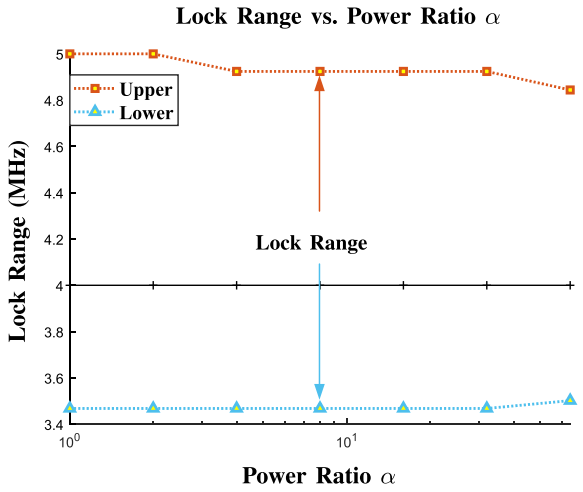
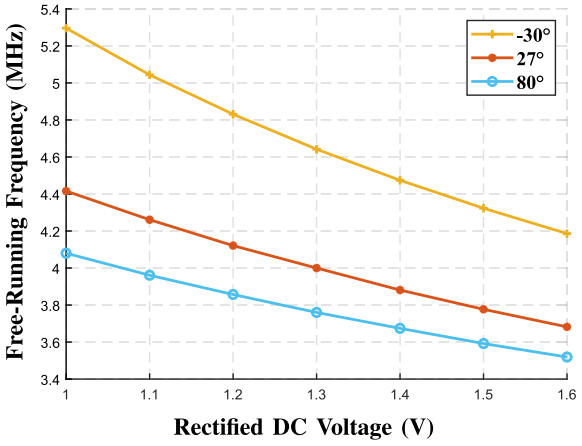
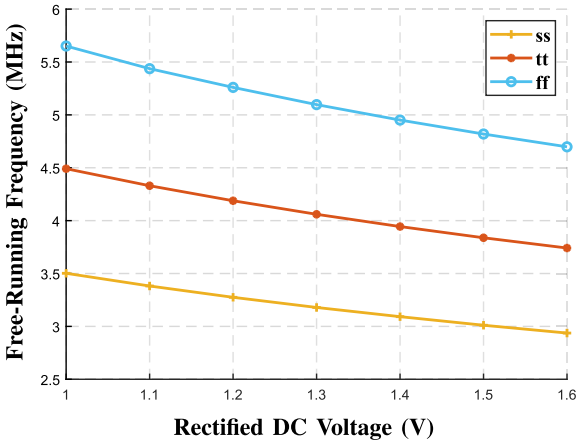


Fig. 12. Lock range vs. power ratio at rectifier input (α=$P_{REC,1}/P_{REC,2}$).

To further improve the lock range, the width of the injected pulse is also optimized in our design. The lock range versus pulse width is simulated in Fig. 11. As we analyzed before, the

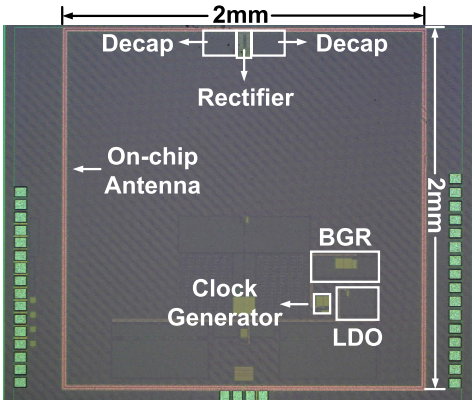


(a)

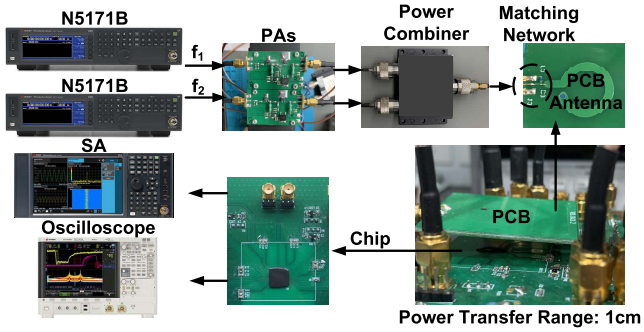


(b)

Fig. 13. Free-running frequency vs. rectified DC voltage at (a) -30 °C, 27 °C, 80 °C, and (b) corner 'ss', 'tt', 'ff'.



(a)



(b)

Fig. 14. (a) Die micrograph. (b) Measurement setup.

lock range is asymmetrical, i.e., the upper edge and lower edge of the lock range show different trends versus the increasing of the pulse width. According to the analysis in Fig. 9(a) and Fig. 9(b), a wider pulse can help a higher-frequency oscillator lock to the f_{IM2}, so the upper edge of lock range $\omega_{0,max}$ can be increased by enlarging the pulse width. For the lower edge, the frequency $\omega_{0,min}$ can be decreased slightly as the pulse width is enlarged, leading to a wider lock range. However, a too-wide injected pulse will damage the free-running waveform, leading to even worse lock range. Overall, the lowest edge of lock range can be achieved when the pulse width is close to T_0.

At the Tx side, we optimize the strength of two tones to enhance the clock performance. As analyzed in Section III-A, the amplitude of IM2 reaches the peak when the power of f_1 and f_2 at the rectifier input are the same. We assume the ratio of the two power as $\alpha = P_{\mathrm{REC},1}/P_{\mathrm{REC},2}$, where $P_{\mathrm{REC},1}$ and $P_{\mathrm{REC},2}$ corresponds to the power of frequency f_1 and f_2 at the rectifier input, respectively. Fig. 12 shows the lock range versus the ratio α. As α is increased, the upper edge of the lock range ($\omega_{0,\mathrm{max}}$) falls and the lower edge of the lock range ($\omega_{0,\mathrm{min}}$) rises, leading to a smaller lock range ($\omega_{0,max} - \omega_{0,min}$). The lock range is decreased because the IM2 amplitude is reduced by a higher power ratio α.

The simulated free-running frequency at different supply voltages V_{DC} and temperatures is shown in Fig. 13(a). From −30 °C to 80 °C, as the rectified DC voltage varies from 1 V to 1.6 V, f_0 ranges from 3.5 MHz to 5.3 MHz. The simulated free-running frequency at different supply voltages V_{DC} and corners is shown in Fig. 13(b). The rectifier output voltage changes in the range of 1 V−1.6 V at different Tx power. As the targeting rectified voltage is expected to be 1 V−1.6 V, there is some margin to compensate the process corners. With a 50 kΩ R_{S} and a 65-ns-pulse-width injected pulse, the lock range can cover all the frequency variations induced by temperature, process, and DC voltage. Meanwhile, the harmonics of the IM2 signal is excluded in the free-running frequency range to ensure the injection lock to fundamental frequency.

The neural-recording chip utilizes the crystal-less clock generation technique to provide a global clock for signal-acquisition unit and backscatter communication. Instead of a crystal oscillator, our clock generation technique utilizes the IM2 component of the WPT tones as the reference, and the temperature coefficient is determined by the external RF powering signal. Meanwhile, the lock range of our ILRO can cover temperature varies from −30 °C to 80 °C, ensuring a clock robust to temperature.

IV. Measurement Results

This chip is implemented in 65 nm CMOS process, and the die micrograph is shown in Fig. 14(a). The proposed clock

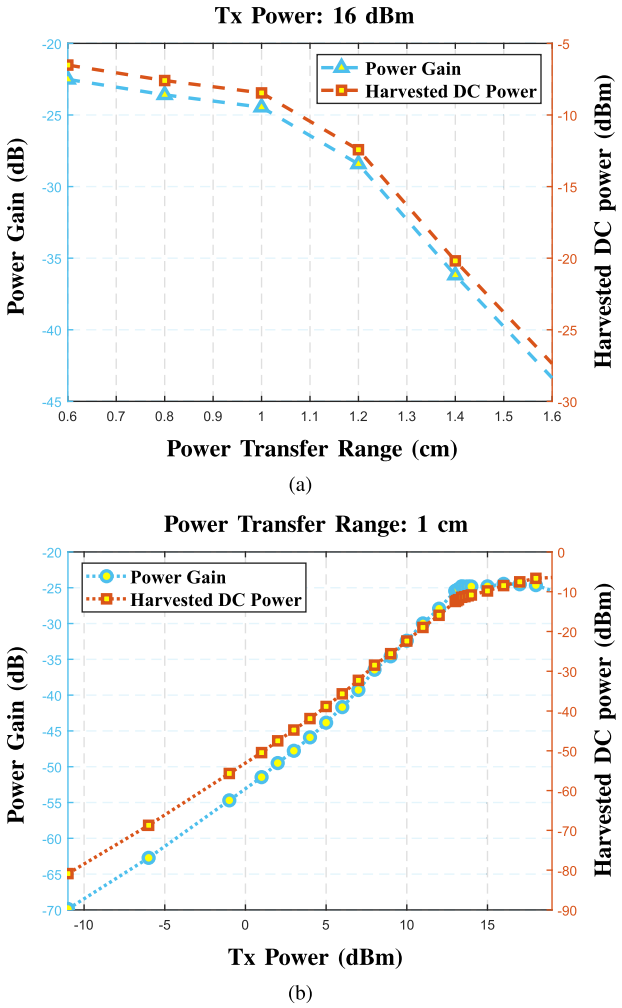


Fig. 15. (a) Power gain vs. power transfer range. (b) Power gain vs. Tx power.

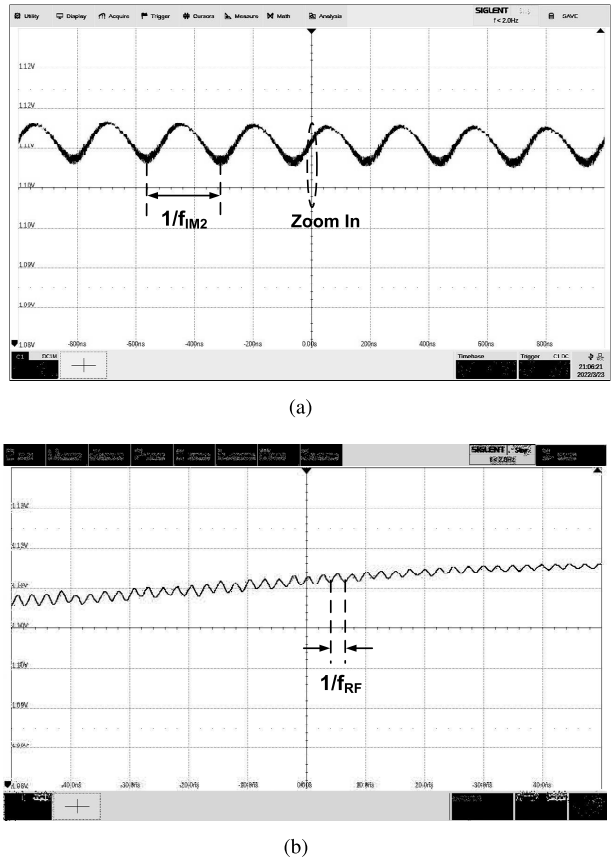


Fig. 16. (a) IM2 envelope at rectifier output. (b) Carrier frequency of RF powering tones.

generation technique is integrated into a 2 mm×2 mm chip for medical implants, where the clock generation circuits take an area of 0.023 mm^2. The rectifier takes a dimension of 144 μm×85 μm, while the pulse generator and ILRO occupy a chip dimension of 94 μm×116 μm. As the system incorporates an off-chip Tx power transmitter and a fully-integrated CMOS chip, the testing setup is demonstrated in Fig. 14(b). Two RF signal generators, two PAs, and a power combiner deliver two WPT tones f_1 and f_2 to a Tx antenna. Meanwhile, a probe station holds the miniature CMOS chip in place to receive the WPT tones. In this way, the IM2 signal and the output of clock generator can be measured by an oscilloscope and a spectrum analyzer (SA).

The WPT from the Tx power transmitter to the CMOS chip is measured at different ranges and Tx power. We utilize an RF signal generator and a PA to provide a 404 MHz tone with 16 dBm power, which is harvested by the CMOS chip. The harvested power and the power gain versus the power transfer range is measured in Fig. 15(a). It shows that the power gain is −24.5 dB at a typical powering range of 1 cm. In addition, the power gain versus Tx power is shown in Fig. 15(b), indicating that the maximum power gain is achieved at 16 dBm Tx power.

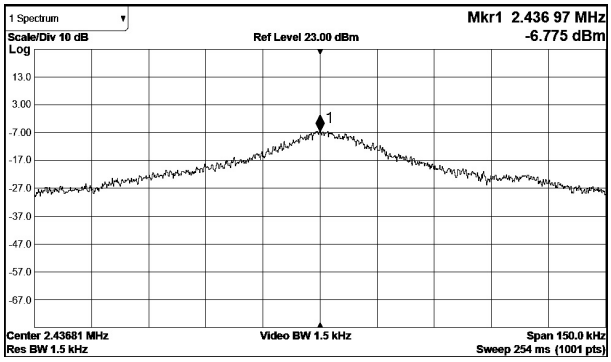
The waveform and magnitude of the IM2 signal is measured at the output of AC-DC rectifier. We apply two tones $f_1 =$ 404 MHz and $f_2 =$ 408 MHz to power the chip wirelessly. The rectifier output is monitored by an oscilloscope, as shown in Fig. 16(a). At the output of AC-DC rectifier, the signal envelope indicates the 4 MHz IM2 frequency. The waveform is zoomed in Fig. 16(b), where we can still see the carrier frequency of RF WPT tones. Since the on-chip rectenna is optimized at f_1, the residual RF signal in V_{DC} is mainly f_1 component. The V_{PP} of the residual RF signal is only a few mV, which can be suppressed by the subsequent circuits.

Finally, we measured the noise of both the ILRO and the injected pulse signal. In the free-running mode, the ring oscillator works at a frequency of 4.8 MHz, which is shifted away from the targeting 4 MHz due to the PVT variations. The clock frequency is obtained by a divided-by-2 divider, which is approximately 2.4 MHz, as shown in Fig. 17(a). With injection locking, the ring oscillator is pushed to the targeting frequency of 4 MHz, resulting in a 2 MHz stable clock, as shown in Fig. 17(b). Fig. 18 shows the phase noise traces of pulse signal (the output of pulse generator), free-running oscillator, and ILRO, respectively. Without the injection signal, the phase noise of free-running oscillator is −45 dBc/Hz@10 kHz. In comparison, the phase noise is reduced to −92 dBc/Hz@10 kHz by the injection locking. The crystal-less clock generator achieves a measured 10 ppm

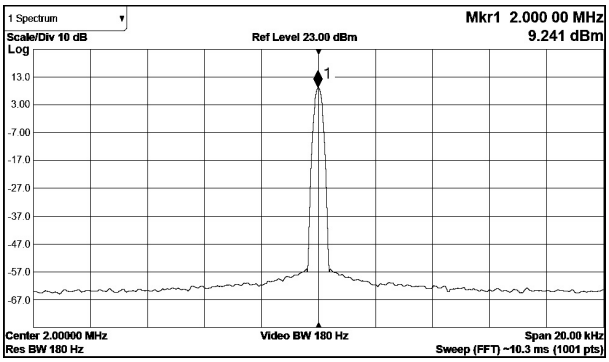
TABLE I
COMPARISON OF CLOCK GENERATORS IN BATTERY-FREE WIRELESS SYSTEMS

Clock Gen.	Process	Fully-Integrated	Crystal	Antenna Type / Size (mm^2)	Techniques	Jitter* (Freq.)	Power (μW)**
[6], 2013	130 nm	No	Yes	Off-Chip / N/A	Crystal + On-Chip Oscillator	N/A	N/A
[7], 2014	180 nm	No	No	Off-Chip / N/A	Free-Running Oscillator + Tuning	176 ps (800 kHz)	60 (9×)
[11], 2015	65 nm	Yes	No	On-Chip / 23.04	RF-Clock Recovery + Long Division	N/A	10.6 (1.5×)
[12], 2017	180 nm	No	No	Off-Chip / 143	Separate Antenna + Clock Recovery	N/A	N/A
[9], 2021	130 nm	Yes	No	On-Chip / 4.8	VCO + Tuning	N/A	20 (3×)
This Work	65 nm	Yes	No	On-chip / 4	IM2 Based Injection Locking	100 ps (2 MHz)	6.8 (1×)

*The jitter refers to simulated cycle jitter.
**The power consumption refers to the clock generator circuits.



(a)



(b)

Fig. 17. ILRO output in (a) free-running and (b) injection-locked states.

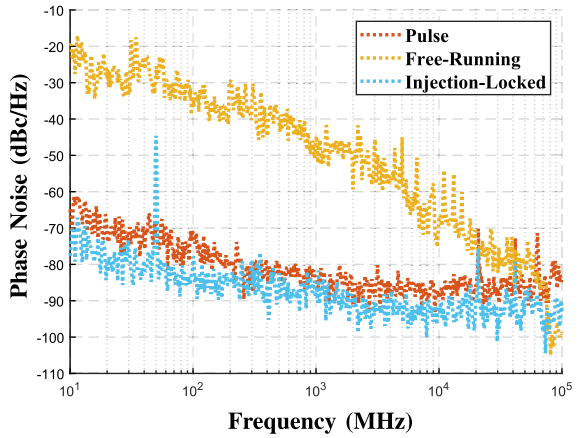


Fig. 18. Phase noise of injected pulse, free-running oscillator, and injection-locked oscillator.

Allan deviation floor. In addition, the power consumption of the whole clock generation circuit is 6.8 μW.

The performance of this design is compared to previous clock generation circuits in battery-free wireless systems, as shown in table I. Compared to conventional methods utilizing crystal or RF powering tone as the reference, our design achieves lowest power consumption. In addition, compared to conventional free-running oscillator, our method can get rid of the off-chip tuning. Moreover, our design only requires a single antenna for both WPT and clock recovery, realizing a single-chip wireless system.

V. CONCLUSION

Battery-free radios are promising in many IoT applications, while the crystal-less clock generation remains a design challenge in system miniaturization. The conventional designs recovery the clock directly from the RF WPT tone, suffering from high power consumption. In this paper, we proposed a clock generation technique based on the IM2 component of two wireless powering tones. As the IM2 frequency is much lower than the RF WPT frequency, the proposed IM2 injection locking circuits generates a low-noise clock signal while other interferes are filtered out. The chip implementation and measured results shows that: 1) The high RF frequency in WPT link results in a miniature antenna size of 2 mm×2 mm. 2) The low frequency of IM2 component reduce the power of clock generator to 6.8 μW, which is 35% lower than conventional RF-based clock recovery circuits. 3) Compared to a tuning oscillator, the proposed IM2 injection locking technique achieves 47 dB lower noise at 10 kHz offset, taking a die area of only 0.023 mm^2.

REFERENCES

[1] B. Zhao, N.-C. Kuo, B. Liu, Y.-A. Li, L. Iotti, and A. M. Niknejad, "A 5.8 GHz power-harvesting 116 μm×116 μm 'dielet' near-field radio with on-chip coil antenna," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2018, pp. 456–458.
[2] W. Biederman *et al.*, "A fully-integrated, miniaturized (0.125 mm^2) 10.5 μW wireless neural sensor," *IEEE J. Solid-State Circuits*, vol. 48, no. 4, pp. 960–970, Apr. 2013.
[3] A. Khalifa *et al.*, "The microbead: A 0.009 mm^3 implantable wireless neural stimulator," *IEEE Trans. Biomed. Circuits Syst.*, vol. 13, no. 5, pp. 971–985, Oct. 2019.
[4] B. Zhao, Y. Lian, A. M. Niknejad, and C. H. Heng, "A low-power compact IEEE 802.15.6 compatible human body communication transceiver with digital sigma-delta IIR mask shaping," *IEEE J. Solid-State Circuits*, vol. 54, no. 2, pp. 346–357, Feb. 2019.
[5] A. Bonfanti *et al.*, "A multi-channel low-power IC for neural spike recording with data compression and narrowband 400-MHz MC-FSK wireless transmission," in *Proc. ESSCIRC*, Sep. 2010, pp. 330–333.
[6] K. Abdelhalim, L. Kokarovtseva, J. L. Velazquez, and R. Genov, "915-MHz FSK/OOK wireless neural recording SoC with 64 mixed-signal FIR filters," *IEEE J. Solid-State Circuits*, vol. 48, no. 10, pp. 2478–2493, Oct. 2013.

[7] H.-G. Rhew *et al.*, "A fully self-contained logarithmic closed-loop deep brain stimulation SoC with wireless telemetry and wireless power management," *IEEE J. Solid-State Circuits*, vol. 49, no. 10, pp. 2213–2227, Oct. 2014.
[8] P. Yeon, M. S. Bakir, and M. Ghovanloo, "Towards a 1.1 mm^2 free-floating wireless implantable neural recording SoC," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Apr. 2018, pp. 1–4.
[9] M. ElAnsary *et al.*, "Bidirectional peripheral nerve interface with 64 second-order opamp-less $\Delta\Sigma$ ADCs and fully integrated wireless power/data transmission," *IEEE J. Solid-State Circuits*, vol. 56, no. 11, pp. 3247–3262, Nov. 2021.
[10] L. Xia, J. Cheng, N. E. Glover, and P. Chiang, "0.56 V, −20 dBm RF-powered, multi-node wireless body area network system-on-a-chip with harvesting-efficiency tracking loop," *IEEE J. Solid-State Circuits*, vol. 49, no. 6, pp. 1345–1355, Jun. 2014.
[11] R. Müller *et al.*, "A minimally invasive 64-channel wireless μECoG implant," *IEEE J. Solid-State Circuits*, vol. 50, no. 1, pp. 344–359, Jan. 2015.
[12] Y.-K. Lo *et al.*, "A fully integrated wireless SoC for motor function recovery after spinal cord injury," *IEEE Trans. Biomed. Circuits Syst.*, vol. 11, no. 3, pp. 497–509, Jun. 2017.
[13] K. Kotani, A. Sasaki, and T. Ito, "High-efficiency differential-drive CMOS rectifier for UHF RFIDs," *IEEE J. Solid-State Circuits*, vol. 44, no. 11, pp. 3011–3018, Nov. 2009.
[14] B. M. Helal, C. M. Hsu, K. Johnson, and M. H. Perrott, "A low jitter programmable clock multiplier based on a pulse injection-locked oscillator with a highly-digital tuning loop," *IEEE J. Solid-State Circuits*, vol. 44, no. 5, pp. 1391–1400, May 2009.
[15] A. Elkholy, M. Talegaonkar, T. Anand, and P. K. Hanumolu, "Design and analysis of low-power high-frequency robust sub-harmonic injection-locked clock multipliers," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 3160–3174, Dec. 2015.
[16] M. Kim, S. Choi, T. Seong, and J. Choi, "A low-jitter and fractional-resolution injection-locked clock multiplier using a DLL-based real-time PVT calibrator with replica-delay cells," *IEEE J. Solid-State Circuits*, vol. 51, no. 2, pp. 401–411, Feb. 2016.
[17] A. Musa, W. Deng, T. Siriburanon, M. Miyahara, K. Okada, and A. Matsuzawa, "A compact, low-power and low-jitter dual-loop injection locked PLL using all-digital PVT calibration," *IEEE J. Solid-State Circuits*, vol. 49, no. 1, pp. 50–60, Jan. 2014.
[18] C. Jung, D. Lee, Y.-H. Kim, D. Lee, and L.-S. Kim, "A 12 Gb/s 1.59 mW/Gb/s input-data-jitter-tolerant injection-type CDR with super-harmonic injection-locking in 65-nm CMOS," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 66, no. 12, pp. 1972–1976, Dec. 2019.
[19] A. Imani and H. Hashemi, "Distributed injection-locked frequency dividers," *IEEE J. Solid-State Circuits*, vol. 52, no. 8, pp. 2083–2093, Aug. 2017.
[20] S. Choi, S. Yoo, Y. Lim, and J. Choi, "A PVT-robust and low-jitter ring-VCO-based injection-locked clock multiplier with a continuous frequency-tracking loop using a replica-delay cell and a dual-edge phase detector," *IEEE J. Solid-State Circuits*, vol. 51, no. 8, pp. 1878–1889, Aug. 2016.
[21] M. Raj, S. Saeedi, and A. Emami, "A wideband injection locked quadrature clock generation and distribution technique for an energy-proportional 16–32 Gb/s optical receiver in 28 nm FDSOI CMOS," *IEEE J. Solid-State Circuits*, vol. 51, no. 10, pp. 2446–2462, Oct. 2016.
[22] B. Hong and A. Hajimiri, "A general theory of injection locking and pulling in electrical oscillators—Part I: Time-synchronous modeling and injection waveform design," *IEEE J. Solid-State Circuits*, vol. 54, no. 8, pp. 2109–2121, Aug. 2019.
[23] R. Adler, "A study of locking phenomena in oscillators," *Proc. IEEE*, vol. 34, no. 10, pp. 351–357, Oct. 1946.
[24] B. Mesgarzadeh and A. Alvandpour, "A study of injection locking in ring oscillators," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, vol. 6, May 2005, pp. 5465–5468.
[25] B. Mesgarzadeh and A. Alvandpour, "First-harmonic injection-locked ring oscillators," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Sep. 2006, pp. 733–736.
[26] Y.-C. Huang and S.-I. Liu, "A 2.4-GHz subharmonically injection-locked PLL with self-calibrated injection timing," *IEEE J. Solid-State Circuits*, vol. 48, no. 2, pp. 417–428, Feb. 2013.
[27] B. Razavi, "A study of injection locking and pulling in oscillators," *IEEE J. Solid-State Circuits*, vol. 39, no. 9, pp. 1415–1424, Sep. 2004.
[28] J. C. Chien and L. H. Lu, "Analysis and design of wideband injection-locked ring oscillators with multiple-input injection," *IEEE J. Solid-State Circuits*, vol. 42, no. 9, pp. 1906–1915, Sep. 2007.
[29] B. Hong and A. Hajimiri, "A phasor-based analysis of sinusoidal injection locking in LC and ring oscillators," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 1, pp. 355–368, Jan. 2019.
[30] B. Razavi, *Design of Analog CMOS Integrated Circuits*. New York, NY, USA: McGraw-Hill, 2001.
[31] G. R. Gangasani and P. R. Kinget, "Time-domain model for injection locking in nonharmonic oscillators," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 6, pp. 1648–1658, Jun. 2008.

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