An Ultra-Low Power Temperature to Digital Converter

V. F. C. van Hoek

EI - Laboratory

TU Delft Delft University of Technology

Electronic Instrumentation Laboratory

Challenge the future

An Ultra-Low Power Temperature to Digital Converter

for Medical Applications in 180 nm CMOS

by

V. F. C. van Hoek

in partial fulfillment of the requirements for the degree of

Master of Science
in Microelectronics

at the Electronic Instrumentation Laboratory,
Department of Electrical Engineering,
Delft University of Technology,
to be defended publicly on Tuesday, 9th of Juli at 12:30.

Supervisor:	Prof. dr. K. A. A. Makinwa	
Thesis committee:	Prof. dr. K. A. A. Makinwa	TU Delft
	dr. S. M. Alavi,	TU Delft
	dr. Q. Fan,	TU Delft.

An electronic version of this thesis is available at http://repository.tudelft.nl/.

TU Delft Delft University of Technology

Abstract

This thesis describes the design of an ultra-low power temperature to digital converter. It is intended to monitor the excess heat produced during the wireless charging of implantable medical devices such as pacemakers. The TDC is designed to achieve an accuracy of ±0.1 °C (3σ) from 27 °C to 47 °C, and ±0.3 °C (3σ) from -40 °C to 85 °C after a 1-point trim. It also achieves a resolution of 0.01 °C at 10 Sa/s. The low power consumption (155 nW) is made possible by the implementation of a self-biasing BJT-core. Its low power consumption, accuracy, and resolution make it ideally suited for clinical temperature monitoring.

Acknowledgements

First and foremost, I want to thank Professor Kofi Makinwa for all the opportunities, the discussions, and the support over the years. He is the mastermind behind most ideas and a master in supporting their execution. He supported me through some rough times and gave me the opportunity to finish in my own time. He always manages to come up with a plan, no matter how urgent the situation. I cannot but have great respect for his ability to come up with new ideas and his passion for his work.

The next person I want to thank is Bahman Yousefzadeh, my daily supervisor. Whenever I had a problem I could not solve on my own, I could go by his office, and he would make time for me, no matter how busy he was himself. I also want to thank Long Xu, who has been a great support in designing and reviewing my layout.

I want to extend another heartfelt thanks to Jan Angevare who helped me with layout, sometimes until early in the morning, reviewed a significant part of my thesis and dragged me away for some Belgian beers when I needed to take a break from work.

I would also like to thank the group at the Electronic Instrumentation Laboratory. Much work goes on in the background, work that enables us to do what we do. That's why I want to give special thanks to Joyce Siemers, Lukasz Pakula, Zu Yao Chang, and Ron van Puffelen, for maintaining the laboratory equipment, for helping me with my measurement setup and PCB design, and for helping me navigate through various forms of bureaucracy.

A special thanks to Marnix Abrahams for the many discussions, his sarcastic humor, and critical view whenever I got stuck during the writing of my thesis.

Another special thanks to Maartje Hodes for both motivating me to finish my thesis, and helping me deal with the stress.

Also a special thanks to my reviewers; Maarten van Hoek, Jan Angevare, Cagri Gürleyük, and Shoubhik Karmakar.

Next, I would like to thank Ton Slats, Martin Schumacher and Xavier van Rijnsoever, for all the free coffee, for their support and for allowing me to work in the Telligen Hal whenever I wanted.

Last but not least; a special thanks to my family and friends for their silent support and unwavering trust in me. Without you, this entire episode of my life would never have been possible!

V. F. C. van Hoek
Delft, Juli 2019

Contents

List of Figures xi

1 Introduction 1
- 1.1 System Requirements 1
  - 1.1.1 Clinical Temperature Monitoring Requirements 2
  - 1.1.2 Industrial Temperature Range Requirements 3
  - 1.1.3 System Requirements Summary 3
- 1.2 Temperature Sensor Type Selection 4
- 1.3 BJT based sensors 4
  - 1.3.1 Current State of the Art 6
  - 1.3.2 Design Focus 8
- 1.4 Project Goals 8
- 1.5 Thesis Outline 8

2 Sensor Design 9
- 2.1 Biasing Current 9
  - 2.1.1 Non-zero Base Current 9
  - 2.1.2 Collector Current 11
- 2.2 Dual Purpose Bandgap Design 12
  - 2.2.1 Sampled Biasing 13
  - 2.2.2 Sample and Hold Requirements 13
  - 2.2.3 Low-leakage Sample and Hold 14
  - 2.2.4 Dual Purpose Frontend 16
- 2.3 Sensor Start-up 16
- 2.4 Sensor Accuracy 17
  - 2.4.1 Dynamic Element Matching 17
  - 2.4.2 Chopping 18
  - 2.4.3 High-Swing Current Mirror 18
- 2.5 Final Frontend Design 19
  - 2.5.1 Temperature Behaviour 19

3 ADC Design 21
- 3.1 BJT-readout Analysis 21
- 3.2 Zoom ADC Topology 23
- 3.3 Coarse Conversion 23
  - 3.3.1 Guard-Banding 24
  - 3.3.2 Cold-start Conversion 25
- 3.4 Feedback DAC 25
  - 3.4.1 Multi-Capacitor DAC 26
  - 3.4.2 Single-Capacitor DAC 26

3.5 Fine Conversion . . . 27
3.5.1 Thermal Noise . . . 27
3.5.2 Quantisation Noise . . . 27
3.6 Accuracy Improvement Techniques . . . 28
3.6.1 System-level Chopping . . . 29
3.6.2 Dynamic Element Matching . . . 29
3.6.3 Correlated Double Sampling . . . 30
3.7 ADC Topology . . . 30

4 Implementation **33**
4.1 Trans-Conductance Amplifier Design . . . 33
4.1.1 Common-mode Feedback Circuit . . . 33
4.1.2 Gain . . . 33
4.1.3 Settling . . . 35
4.1.4 Output Swing . . . 35
4.2 Digital Back-end . . . 36
4.2.1 On-chip Digital . . . 36
4.2.2 Off-chip Digital . . . 37
4.3 TDC Layout . . . 38

5 Simulation Results **39**
5.1 Power Consumption . . . 39
5.1.1 Duty Cycled Power . . . 39
5.2 Accuracy . . . 40
5.2.1 Dynamic Element Matching . . . 42
5.2.2 Power Supply Sensitivity . . . 42
5.3 Resolution . . . 43
5.4 Benchmarking . . . 43

6 Conclusion **45**
6.1 Future Work . . . 45

A TDC Thermal-Noise Limited Resolution Calculation **47**

Bibliography **49**

List of Figures

1.1 Pacemaker placement with charging coil, based on images from [1],[2] 2
1.2 Accuracy vs. Power, plotted from a survey on temperature sensors, taken from [3]. 4
1.3 Temperature sensing principle of BJT based temperature sensor [4]. 5

2.1 Typical BJT based temperature sensor and biasing circuit setup. 10
2.2 Gummel-Poon plot showing the currents I_B and I_C and the gain factor β at 27 °C. 10
2.3 Temperature error over temperature due to β difference. 10
2.4 Accuracy over temperature and process corners for several values of r. 11
2.5 Test bench to determine the sensitivity of V_{BE} and ΔV_{BE} over temperature for different levels of I_{bias} with $r = 7$. 11
2.6 Sensitivity of ΔV_{BE_1} over temperature for multiple levels of I_{bias} with $r = 7$. . . . 12
2.7 Sensitivity of V_{BE} over temperature for multiple levels of I_{bias} with $r = 7$. 12
2.8 Proposed combined BJT frontend, configured as a biasing circuit. 12
2.9 Proposed combined BJT frontend, configured as a BJT-core. 12
2.10 Simple PMOS switch and capacitor sample and hold circuit with leakage paths shown in red. 13
2.11 Temperature error due to the sample and hold leakage current for $C_H = 25$ pF at 25 °C 13
2.12 Bootstrapped PMOS switch sample and hold circuit to reduce leakage. 14
2.13 Buffer controlled low leakage sample and hold circuit based on [5], with the new leakage current path shown in green. 14
2.14 Temperature dependent leakage current of the bootstrapped sampling switch after 100 ms. 15
2.15 Leakage current due to the offset of the sample and hold buffer. 15
2.16 Monte Carlo spread of the offset of the sample and hold buffer 15
2.17 Dual purpose frontend with sample and hold biasing circuit. 16
2.18 Startup sequence of the self-biased BJT-based temperature sensor for V_{BE_1}. . . . 17
2.19 Startup sequence of the self-biased BJT-based temperature sensor for V_{BE_2}. . . . 17
2.20 DEM circuit as implemented in the BJT-core. 17
2.21 DEM timing diagram where $A_{E,8}$ is smaller than the rest. 17
2.22 Cascode current mirror circuit 18
2.23 High swing current mirror circuit 18
2.24 Biasing circuit for the cascode of the high-swing current mirror. 19
2.25 Sensitivity of the temperature measurement to variations in the power supply. . 19
2.26 Simplified version of the final design of the dual purpose bandgap design with a high-swing cascode mirror and DEM switches. 20
2.27 Final BJT frontend output results V_{BE_1}, V_{BE_2} and ΔV_{BE} with $r = 7$ and $I_{bias} = 25$ nA over temperature. 20

2.28 Calculated temperature and temperature error based on V_{BE_1} and ΔV_{BE} over temperature. . . . 20

3.1 Bandgap TDC readout principle [6]. . . . 22
3.2 Increased the dynamic range of μ with respect to temperature over the military temperature range [6]. . . . 22
3.3 Behavior of X over the industrial temperature range, for $r = 7$ and $I_C = 25$ nA. 22
3.4 Block diagram of the Zoom ADC, split into a coarse conversion to determine k, and a fine conversion to determine μ'. . . . 23
3.5 (a)TDC coarse conversion thermometer; (b) Zoomed fine range of n to $n + 1$ based on the coarse conversion result. . . . 23
3.6 Block diagram of the coarse conversion to determine k. . . . 24
3.7 Comparison between linear ramp and SAR approach to determine k over clock cycles at room temperature. . . . 24
3.8 (a) Coarse conversion; (b) guard-banding; (c) fine range when $X > n + 0.5$; (d) fine range when $X < n + 0.5$ . . . 25
3.9 Multi-capacitor DAC single sided diagram. . . . 26
3.10 Multi-capacitor DAC timing diagram for two clock periods. . . . 26
3.11 Single-capacitor DAC single sided diagram. . . . 26
3.12 Single-capacitor DAC timing diagram. . . . 26
3.13 ENOB required over temperature (with r=7 and X_{range}=12) to achieve a target resolution of ±0.01 °C. . . . 28
3.14 Number of samples required to achieve a desired ENOB [7]. . . . 28
3.15 Block diagram of a 2nd-order feed-forward ΣΔ-modulator. . . . 28
3.16 System level chopping circuit adiagram. . . . 29
3.17 System level chopping timing diagram. . . . 29
3.18 Barrel shifting DEM scheme. . . . 29
3.19 CDS circuit diagram with differential integrator offset. . . . 30
3.20 CDS timing diagram. . . . 30
3.21 Second order feed-forward ADC circuit diagram. . . . 31
3.22 Second order feed-forward ADC timing diagram during both the coarse conversion and fine conversion. . . . 31

4.1 Current re-use OTA design based on [8]. Sizes are given as m · W/L and are in μm. . . . 34
4.2 Current re-use OTA design based on [8]. Sizes are given as m · W/L and are in μm. . . . 34
4.3 Switch capacitor based CMFB circuit that is used in both OTAs to set the common mode voltage. . . . 34
4.4 Bode plot of OTA_1. . . . 35
4.5 Bode plot of OTA_2. . . . 35
4.6 Differential output settling of OTA_1 with $f_s = 3$ kHz and feedback factor $a_1 = 1/8$. . . . 35
4.7 Differential output settling of OTA_2 with $f_s = 3$ kHz and feedback factor $a_2 = 1/2$. . . . 35
4.8 Non-overlapping clock generator circuit. . . . 36
4.9 Transition of the non-overlapping clock signals from $\phi_2 \Rightarrow \phi_1$. . . . 37

4.10 Transition of the non-overlapping clock signals from $\phi_1 \Rightarrow \phi_2$. 37
4.11 Block diagram of the shift register 38
4.12 TDC layout with labelled blocks. 38

5.1 Pie chart showing the power consumption distribution of the TDC. 40
5.2 Calculated temperature from the Monte Carlo simulation over the actual temperature. 41
5.3 Absolute temperature error of the Monte Carlo simulation over the actual temperature. 41
5.4 Untrimmed inaccuracy results of the TDC over temperature for a 10-points Monte Carlo simulation at 8 temperatures. 41
5.5 Trimmed inaccuracy results of the TDC over temperature for a 10-points Monte Carlo simulation at 8 temperatures. 41
5.6 Untrimmed accuracy of the BJT frontend from a 200-point Monte Carlo simulation. 41
5.7 PTAT trimmed accuracy of the BJT frontend from a 200-point Monte Carlo simulation. 41
5.8 Untrimmed inaccuracy results of the TDC over temperature for a 10-points Monte Carlo simulation at 8 temperatures with DEM. 42
5.9 Trimmed inaccuracy results of the TDC over temperature for a 10-points Monte Carlo simulation at 8 temperatures with DEM. 42
5.10 Sensitivity of the temperature measurement to variations in the power supply. . 42
5.11 FFT of a MATLAB model simulation generated output bitstream. 43
5.12 FFT of a TDC generated output bitstream over 6 seconds. 43

6.1 A current ratio based design of the BJT-core 46
6.2 Improvement to the power consumed by the mirrors used for current biasing. . 46
6.3 First order ΣΔ-modulator design to reduce power consumption. 46

1

Introduction

In the field of Bio-electronics, heartwarming advances in pacemaker design have been made. Despite this, they still need to be periodically replaced. Since this is associated with significant risks and usually requires invasive surgery, reducing the number of times a replacement is required is an important goal of the research in this field [9]. One common reason for pacemaker replacement is battery depletion. On average, a pacemaker battery lasts for about ten years. The average age of a pacemaker recipient is about 75, and 85% of pacemakers are implanted in people that are more than 65 [10],[11]. Being able to recharge the battery in the body would significantly increase pacemaker lifetime and thus reduce the number of replacements required, especially for the 15% that are younger than 65.

As it is impossible to connect a pacemaker directly to a charging station, the possibility of wireless charging has been researched [1]. One way of doing this is via induction coils. An external coil generates a changing magnetic field, which creates an AC signal in a second coil that is part of the pacemaker. However, induction coils also induce self-heating in the metal case of a pacemaker. This will cause tissue damage if it exceeds a few degrees Celsius [12].

To prevent tissue damage, measuring the local temperature is a necessity. A temperature sensor can be used for this purpose. Its output can then be translated to a digital signal which can then be used to adjust the power transfer accordingly to reduce the amount of excess heat produced. This type of temperature sensor is called a temperature to digital converter (TDC). To avoid draining the pacemaker's battery, the TDC's power consumption should then be as low as possible.

The objective of this work is twofold. The first is to create a clinical temperature monitoring system for the wireless charging of pacemakers, complying with the strict requirements that apply to electronics for pacemakers, with a focus on low power consumption. The second is to achieve state of the art performance over the industrial temperature range (-40 °C to 85 °C) to demonstrate the usefulness of the design in more general applications. An outline of this thesis and the content of each chapter is included at the end of this introduction. In the next section, the system requirements for both clinical temperature monitoring and the industrial temperature range are defined.

1.1. System Requirements

In order to achieve the desired performance and reach the current state of the art, the following design criteria need to be discussed: Temperature range, power consumption, accuracy, reso-

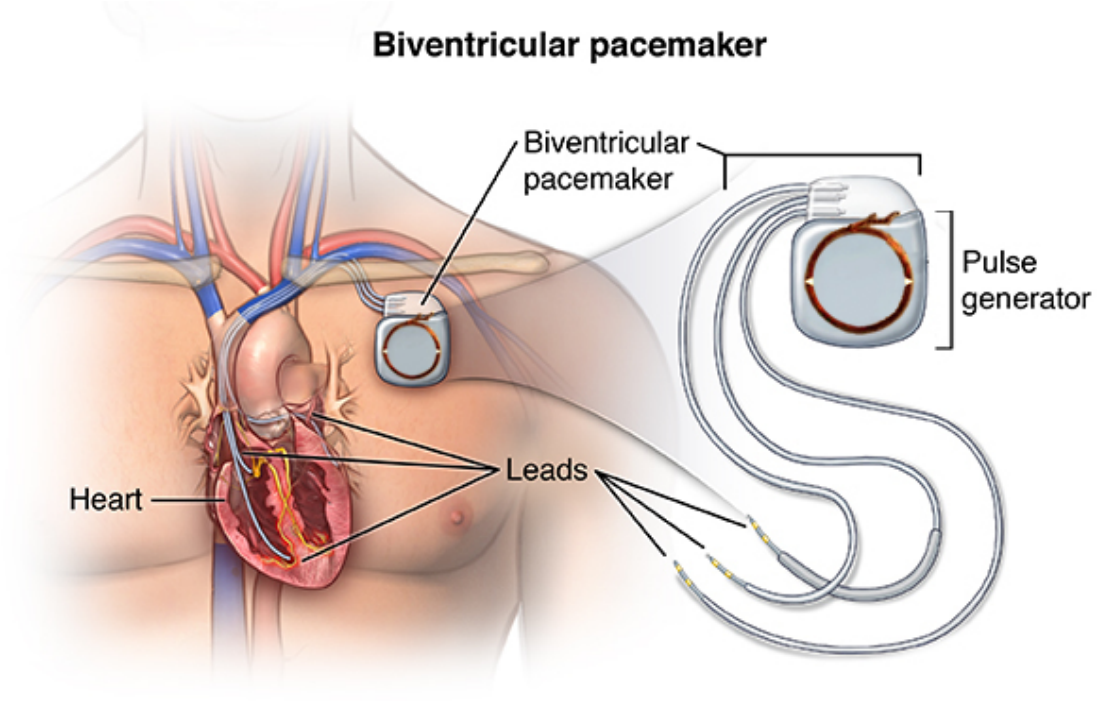

Figure 1.1: Pacemaker placement with charging coil, based on images from [1],[2]

lution, conversion time or sample rate, area, calibration methods, measurement environment, and technology. First, these design criteria will be discussed in the context of clinical temperature monitoring. Next, any changes or additional criteria required for the temperature sensor to work over a wider (industrial) temperature range will be discussed.

1.1.1. Clinical Temperature Monitoring Requirements

In clinical temperature monitoring systems, five design criteria require specific attention: Area, measurement environment, power consumption, accuracy, and resolution. These are considered to be the primary specifications for this temperature sensor. Conversion time, calibration methods, and technology are considered to be the secondary specifications. The following sections discuss these specifications in more detail.

Area and Measurement Environment

Ideally, the temperature sensor should be as close as possible to the charging coil. In medical applications, however, this can be a challenge and especially in the field of implants. Not only are there a limited number of places where it is safe to place implants but the space available in those places is also limited as well. Then there are the risks of rejection by the body and corrosion due to the harsh environment. Figure 1.1 shows a common pacemaker location. However, all of these criteria have to be met by the design of the pacemaker itself and thus are not of direct concern to the design of the TDC.

Power Consumption, Accuracy, and Resolution

The most important challenge for this TDC design, power consumption, is also the most difficult one to meet as it impacts both resolution and accuracy. A typical pacemaker control circuit requires 30 µW [10]. In order not to significantly impact battery lifetime, the TDC

should draw less than 1% of that power, implying a power consumption of 300 nW or less. The target is conservatively set at 100 nW.

Furthermore, as battery voltage tends to drop over time, care has to be taken that the measurement is not sensitive to the supply voltage. This cross sensitivity is often referred to as power supply sensitivity (PSS). The PSS should be in the order of ~0.1 °C/V to ensure sufficient accuracy over the lifetime of the battery.

The other challenges for the TDC lie in its required resolution and accuracy. As mentioned previously, internal tissue can be damaged if its temperature increases by only a few degrees Celsius. To be able to sense such temperature changes reliably, the TDC needs to have an accuracy of at least ±0.1 °C around body temperature [13]. Achieving this level of accuracy usually requires calibration. The accuracy requirement also imposes limits on the resolution of the TDC. As a rule of thumb, for calibration purposes the resolution needs to be an order of magnitude smaller than the target accuracy, so in this case, ±0.01 °C.

Conversion Time, Calibration, and Technology

As body temperature is a slowly changing signal, the conversion time of the TDC is not that critical. In practice, it is limited by the time it takes to achieve sufficient resolution. To remain competitive with the state of the art, the conversion time is set at 100 ms or 10 samples/s.

As mentioned before, calibration is often required to achieve a high level of accuracy. However, this takes time and thus, money. For this reason, only a 1-point calibration is allowed for this design. Furthermore, as the TDC will be part of the pacemaker, it would reduce cost and complexity to make the sensor in the same standard CMOS technologies as the pacemaker's own circuitry. The technology used in this project is the Taiwan Semiconductor Manufacturing Company (TSMC) 0.18 µm High-Voltage process.

1.1.2. Industrial Temperature Range Requirements

The requirements for the industrial temperature range are no different from those for clinical temperature monitoring except for the accuracy and the temperature range. Despite the increased temperature range (-40 °C to 85 °C), the inaccuracy should be less than ±0.3 °C to maintain a state of the art performance.

1.1.3. System Requirements Summary

All the previously mentioned requirements for both clinical temperature monitoring and measuring over the industrial temperature range are summarized in Table 1.1. With this list of requirements, a selection of temperature sensors can be analyzed and compared to determine which topology is most suitable for the target application.

[1]Relative Acc. = 2·Accuracy / T. Range · 100
[2]Res. FOM = Power·t_{conv}·Res.^{2}

Table 1.1: TDC specifications for use in clinical temperature monitoring and for the industrial temperature range.

T. Range [°C]	Power [µW]	Accuracy (±3σ) [°C]	Relative[1] Acc. [%]	Res. [°C]	t_{conv} [ms]	Res. FOM[2] [°C/V]	PSS [pJ°C^2]	Tech. [µm]
27 to 47	0.1	±0.1	1	0.01	100	1	~ 0.1	0.18
-40 to 85	0.1	±0.3	0.48	0.01	100	1	~ 0.1	0.18

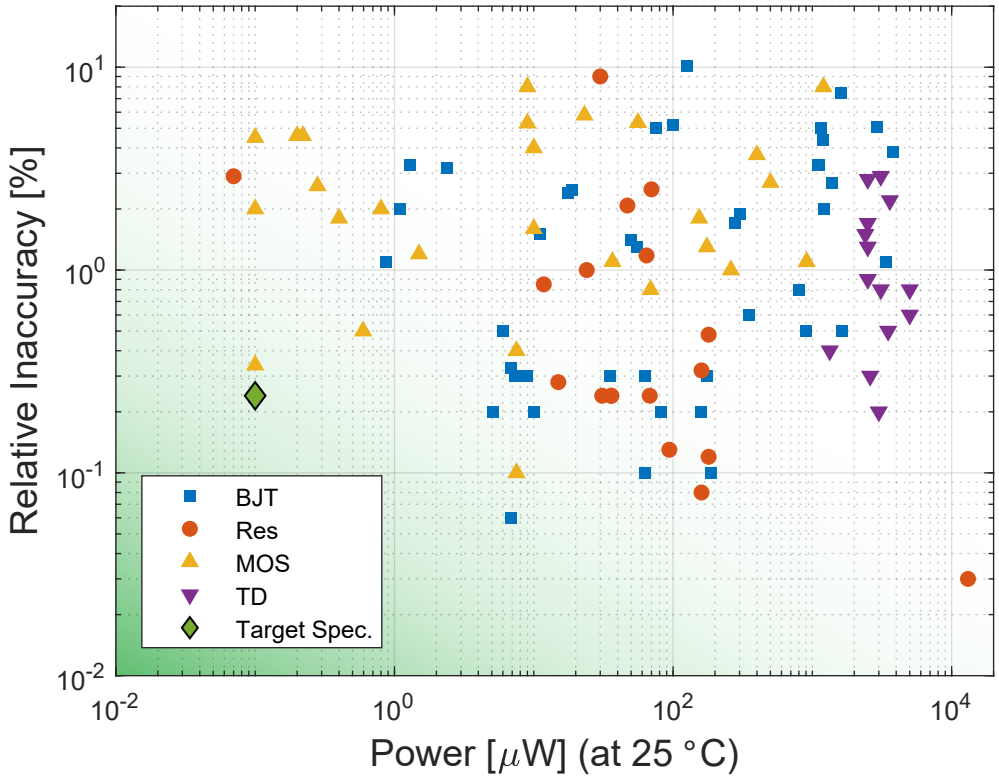

Figure 1.2: Accuracy vs. Power, plotted from a survey on temperature sensors, taken from [3].

1.2. Temperature Sensor Type Selection

Four kinds of temperature sensors might satisfy the requirements shown in Table 1.1: bandgap sensors, delay-based sensors, resistor-based sensors or Thermal-Diffusivity (TD) sensors. A quick survey of these four types based on the primary requirements will show which is most suited for clinical temperature monitoring applications.

In Figure 1.2 the trade-off between power consumption and accuracy has been plotted for a number of temperature sensors [3]. It can be seen that TD and resistor based sensors dissipate too much power for clinical temperature monitoring. MOSFET and BJT-based sensors show performance much closer to the targeted specifications. Of these the bandgap temperature sensors (both MOSFET and BJT) are amongst those with the lowest power. Of these bandgap sensors, a BJT based temperature sensor implementation has been chosen for its inherent accuracy and ease of implementation in the requested technology.

The next section gives a short introduction to a Bipolar Junction Transistor (BJT) based temperature sensors. A comparison is made with the current state of the art temperature sensors that focus on clinical temperature monitoring to establish the project goals.

1.3. BJT based sensors

BJT based temperature sensors work by forcing a current through a set of BJTs, called a BJT-core, to generate a temperature dependent voltage, as shown in Figure 1.3. In [14] a proportional to absolute temperature (PTAT) voltage is digitized with respect to a reference voltage, made from a PTAT voltage and a complementary to absolute temperature (CTAT) voltage. The

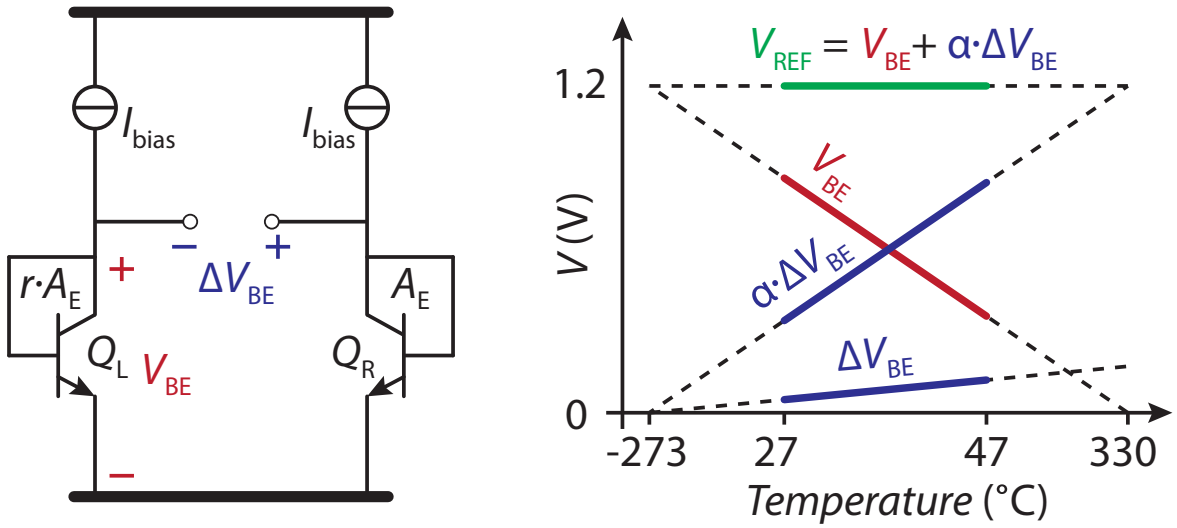

Figure 1.3: Temperature sensing principle of BJT based temperature sensor [4].

base-emitter voltage V_{BE} across a single BJT is CTAT and is described by equation (1.1). The differential voltage of two of these junctions with different current densities is the PTAT voltage ΔV_{BE} and is described by equation (1.2):

$$V_{BE}(T) = \frac{kT}{q} \ln\left(\frac{I_{bias}(T)}{I_S(T)}\right) \tag{1.1}$$

$$\Delta V_{BE}(T) = \frac{kT}{q} \ln(r) \tag{1.2}$$

By adding these two values with a ratio α a temperature independent voltage $V_{REF} = V_{BE} + \alpha \cdot \Delta V_{BE}$ can be generated (see Figure 1.3). Finally $\alpha \cdot \Delta V_{BE}$ can be compared against V_{REF} to perform a temperature measurement. The following equations show a common ratiometric measurement of μ and thus T,

$$\mu = \frac{\alpha \cdot \Delta V_{BE}}{V_{REF}} \tag{1.3}$$

$$T = A \cdot \mu + B \tag{1.4}$$

where A and B are linear fitting parameters to translate μ to temperature.

One of the advantages of using a BJT-core is that they require relatively low power for good accuracy, due to the ratiometric nature of the measurement. Using a ratio cancels out many errors associated with absolute value measurements.

Another advantage is that they only require a single point trim to achieve $\pm$0.1 °C inaccuracy or better over the industrial temperature range (-40 °C to 85 °C) [14],[8]. Trimming is time-consuming and therefore costly. With the introduction of voltage calibration in [15] a single point trim can be made with the help of an accurate reference voltage instead of an accurate temperature.

Next, the current state of the art TDCs for clinical temperature monitoring using a BJT-core, are compared to refine the project goals.

Table 1.2: Comparison of state of the art clinical temperature monitoring TDCs.

item	T. Range [°C]	Power [µW]	Accuracy (±3σ) [°C]	Relative[3] Acc. [%]	Res. [°C]	t_{conv} [ms]	Res. FOM[4] [pJ°C^2]	PSS [°C/V]	Tech. [µm]
Goal	27 to 47	0.1	±0.1	1	0.01	100	1	~ 0.1	0.18
[16]	25 to 45	1.1	±0.2	2	0.01	500	55	N/A	0.18
[17]	20 to 50	16	±0.1	0.666	0.01	100	1.6	N/A	0.18
[18]	20 to 50	2.205	-0.5/+0.25[5]	2.5	0.01	20	689	N/A	0.35
[19]	20 to 50	3[6]	±0.15	1	0.05	51.2	400	N/A	0.13

1.3.1. Current State of the Art

BJT based TDCs have often been used for clinical temperature monitoring, most notably [16], [17], [18] and [19]. A literature study on the current state of the art serves to determine the focus and goals of this design and to confirm the target specifications. Table 1.2 gives a summary of the aforementioned designs and compares them to the target specifications of this thesis. The key features of each design will then be briefly addressed, in the order that they appear in the table.

M. Law [16]

The first TDC [16], uses a current ratio based BJT pair to generate the temperature dependent voltages V_{BE} and $\alpha \cdot \Delta V_{\mathrm{BE}}$. Instead of directly digitizing the temperature as described in equation (1.4) a multi-ratio pre-gain stage is used to improve the energy efficiency of its analog to digital converter (ADC). Here $\alpha \cdot \Delta V_{\mathrm{BE}}$ is pre-amplified by k_1 or k_3 and V_{BE} by k_2 or k_4, dependent on the value of the bit-stream. The new ratiometric output μ' then becomes

$$\mu' = \frac{k_1 + k_2}{k_1 - k_3} \cdot \frac{\alpha \cdot \Delta V_{\mathrm{BE}}}{V_{\mathrm{REF}}} - \frac{k_2}{k_1 - k_3}$$

Half of the total system power of this design (0.57 μW of 1.1 μW) is consumed by the amplifier in its ADC. The other half is divided almost equally between the front-end and the control logic, respectively consuming 0.27 μW and 0.25 μW. The TDC achieves an accuracy of ±0.2 °C over a temperature range of 25 °C to 45 °C.

C. Deng [17]

The second TDC [17], sets out to improve the matching between the two BJTs (as shown in Figure 1.3) and reduce the influence of the gain error of a 24-bit ΣΔ-ADC. They do so by using only one BJT for two consecutive ADC conversions. In a first conversion, the BJT is biased at a unit current I_{bias}, while in a second conversion that same BJT is biased at $N \cdot I_{\mathrm{bias}}$. The result of the two conversions D_1 and D_2 can then be expressed as:

[3] Relative Acc. = 2·Accuracy / T. Range · 100
[4] Res. FOM = Power·t_{conv}·Res.^{2}
[5] Min-max Accuracy
[6] Includes glucose sensor readout

$$D_1 = \frac{(V_{\text{BE1}} + V_{\text{OS}}) \cdot G_{\text{ADC}}}{V_{\text{REF}}}$$
$$D_2 = \frac{(V_{\text{BE2}} + V_{\text{OS}}) \cdot G_{\text{ADC}}}{V_{\text{REF}}}$$

where V_{OS} is the ADC's input-referred offset voltage. The temperature is then calculated by combining both conversion results into a single equation,

$$T_{\text{out}} = \frac{K(D_1 - D_2)}{D_1 + M(D_1 - D_2)} = \frac{K(V_{\text{BE1}} - V_{\text{BE2}})}{V_{\text{BE1}} + M(V_{\text{BE1}} - V_{\text{BE2}})}$$

where K is a gain calibration coefficient and M is a temperature compensation coefficient. The TDC draws 900 μA at 25 °C during conversion, and 100 nA while in standby. It is duty-cycled and draws an average of 16 μW at a conversion rate of 10 Hz. While the average power consumption is much too high for the design proposed in this thesis, the idea of duty-cycling the system is a useful one.

The authors claim that, by combining two conversion results into one measurement, the offset and the gain errors of the ADC are reduced. However, they cannot be removed completely, since the results of two conversions i.e., two equations, cannot be used to solve for three unknown parameters. Using this technique they achieve an accuracy of ±0.1 °C over a temperature range of 20 °C to 50 °C. However, it comes at the cost of increased conversion time.

Part of the reason for the relatively high power consumption of this design is probably the high number of bits (24 bits) required to achieve their <0.001 °C resolution. Reducing this requirement to 0.01 °C should significantly reduce the required power consumption.

Z. Zheng [18]

The third TDC [18], is designed for use inside a retinal prosthesis. Here the outputs of a BJT pair are converted to a CTAT and PTAT voltage

$$V_{CTAT} = 2V_{BE}$$
$$V_{PTAT} = \frac{R_2}{R_1}\Delta V_{BE}$$

where R_1 and R_2 are chosen to ensure that V_{PTAT} and V_{CTAT} intersect around 37 °C.

These voltages are pre-amplified and then connected to a successive approximation register (SAR)-ADC instead of a ΣΔ-ADC as in the previous designs. SAR-ADCs are usually quite power efficient and have a short conversion time, making them suitable for use in power starved applications [20]. However, they have relatively low resolution of < 14 bits.

The TDC draws 210 μA from a 3V supply. However, due to a temperature conversion time of only 70 μs, the average power consumption can be reduced to 2.205 μW at 50 Hz by turning off the TDC during the rest of the 20 ms conversion time of the retinal prosthesis.

An inaccuracy of -0.5 °C to +0.25 °C after a 1-point calibration over a temperature range of 20 °C to 50 °C is measured on a single TDC. This does raise concern on the viability of SAR-ADCs for clinical temperature monitoring.

X. Chen [19]

The fourth and final TDC [19], is designed together with a glucose sensor interface, and shares the same ADC. The ADC is a 1st-order Zoom ΣΔ-ADC with the addition of a sampled current path that directly connects to the ΣΔ-ADC's integrator and acts as the glucose sensor interface.

Once again, the main focus in this design is on the power of the amplifier used in the integrator. The authors use a dynamically biased inverter based amplifier to reduce the impact on the power consumption as much as possible. The TDC consumes a total of 3 μW while achieving a peak-to-peak accuracy of ±0.15 °C over a range of 20 °C to 50 °C.

1.3.2. Design Focus

Most of the aforementioned TDCs focused on the design of an energy efficient ADC. Specifically on the amplifier, whether used as an integrator or as a pre-amplifier. As was shown in [8], the current they draw can be further reduced, and might be traded for increased conversion time in a ΣΔ-ADC.

Though the amplifier is often the most power consuming part of a TDC, the power consumption of the BJT frontend (BJT-core plus its biasing circuit) is also quite significant. In this thesis, we will focus on minimizing the power consumption of the BJT frontend and on scaling the ADC to obtain lower overall power consumption. The digital control logic should not be neglected, or it might dominate the power consumption of the TDC.

1.4. Project Goals

To summarize, the main goal of this research project is to reduce the power consumption of clinical temperature monitoring TDCs while maintaining state of the art performance.

The target for power consumption is set at 100 nW, a factor of 10 less than [16], the lowest of the TDCs mentioned above. This target is to be achieved by optimizing the power consumption of the BJT frontend, scaling the ADC accordingly and reducing the digital control logic as much as possible.

The performance is measured by the accuracy and resolution of the TDC. The targeted accuracy is ±0.1 °C (3σ) with a 1-point calibration around body temperature (from 27 °C to 47 °C) with a resolution target of 0.01 °C within a conversion time of 100 ms. These targets are set based on the requirements set by [13] and [21] together with current state of the art TDCs for clinical temperature monitoring.

A secondary goal is to maintain state of the art performance over the industrial temperature range. The target is to achieve an accuracy of ±0.3 °C (3σ) with a 1-point calibration over this temperature range while maintaining the same resolution and power consumption. Both these and the secondary requirements were summarized in Table 1.1.

1.5. Thesis Outline

The outline of this thesis is as follows; in Chapter 2 the BJT frontend will be discussed in more detail and its design will be presented. Then, in chapter 3 the design of the ADC will be discussed, while its implementation will be discussed in Chapter 4. The simulation results of the completed TDC will be presented and explained in Chapter 5. Finally, in Chapter 6, some conclusions are drawn, and suggestions for future work are given.

2

Sensor Design

In this chapter, the requirements of the BJT frontend are discussed, and its design is presented. As low power consumption is the main goal of this design, the parts of a BJT frontend that consume the most power are discussed first, in Section 2.1. Second, a low power design for the frontend is presented in Section 2.2 and its influence on the inaccuracy of the measurement is discussed. Third, two methods to improve the inaccuracy of the design are presented and discussed in Section 2.4. Last, the final design of the frontend is presented in Section 2.5.

2.1. Biasing Current

A BJT pair can be used both as a temperature sensor and as a biasing circuit. BJT based temperature sensors require both functions [6], leading to a (simplified) common architecture is shown in Figure 2.1. This figure shows a biasing circuit, whose current is copied to the BJT-core. As a biasing circuit, ΔV_{BE}, is forced across a resistor R_B to generate a PTAT current I_{bias}. As a BJT-core, each BJT uses their own collector current I_C to generate two CTAT voltages, V_{BE_1} and V_{BE_2}, and one PTAT voltage ΔV_{BE}. The collector current I_C determines V_{BE} and is given by:

$$I_C = I_S \cdot (e^{\frac{V_{BE}}{V_T}} - 1) \quad \text{with} \quad V_T = \frac{k_B T}{q} \tag{2.1}$$

where k_B is the Boltzmann constant and q the unit charge of an electron. The saturation current I_S is given by:

$$I_S = CT^{\eta} e^{(\frac{-qV_{g0}}{kT})} \tag{2.2}$$

2.1.1. Non-zero Base Current

Ideally, we want $I_{bias} = I_C$. However, due to the diode configuration of the BJTs (Figure 2.1), the biasing current $I_{bias} = I_C + I_B$ with the base current $I_B \neq 0$. In other words, the BJT has a finite current gain β, given by:

$$\beta = \frac{I_C}{I_B} \tag{2.3}$$

This finite current gain increases the total biasing current by a factor of $(1 + 1/\beta)$, and introduces a measurement error because β is not constant over I_{bias} (see Figure 2.2). At the desired

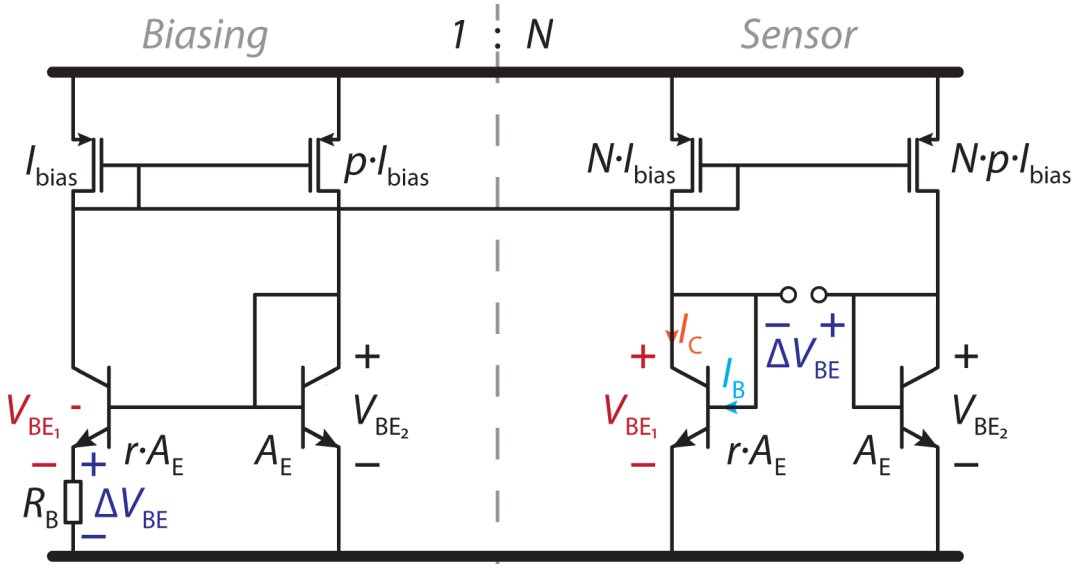

Figure 2.1: Typical BJT based temperature sensor and biasing circuit setup.

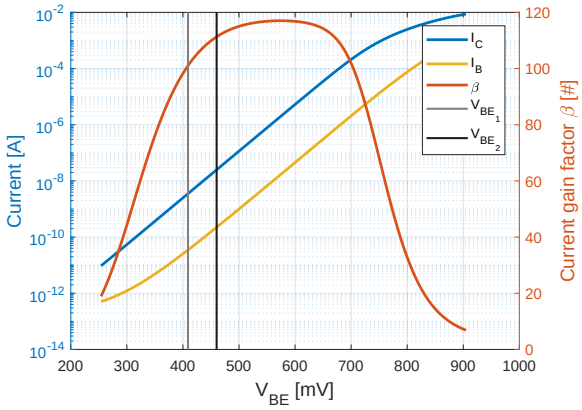

Figure 2.2: Gummel-Poon plot showing the currents I_B and I_C and the gain factor β at 27 °C.

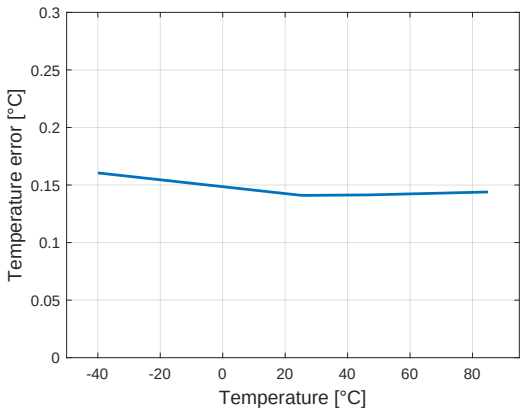

Figure 2.3: Temperature error over temperature due to β difference.

biasing points, shown by the grey and black lines in Figure 2.2, $\beta = 101$ and $\beta = 111$ for V_{BE_1} and V_{BE_2} respectively. The temperature error in ΔV_{BE} caused by the difference in β can be approximated by:

$$\sigma_{T,\Delta V_{BE}} = V_T \cdot ln\left(\frac{I_C(1+\frac{1}{\beta_{max}})}{\frac{I_C}{r}(1+\frac{1}{\beta_{min}})}\right)/S\Delta V_{BE} \tag{2.4}$$

For the given values of β, $\sigma_{T,\Delta V_{BE}} \approx 0.15$ °C. This is a large error given the accuracy budget of 0.1 °C around body temperature. However, this error is fairly constant over temperature, as can be seen from Figure 2.3. The error only varies by 0.4 m°C around body temperature and by 0.02 °C over the industrial temperature range.

The offset of this error can be absorbed during the sensor's calibration, leaving only the temperature dependent part as a source of error, which is negligibly small. Furthermore, I_{bias} is only $\sim 0.95\%$ larger than I_C. In the rest of this thesis, for a single BJT, the assumption $I_{bias} = I_C$ is used.

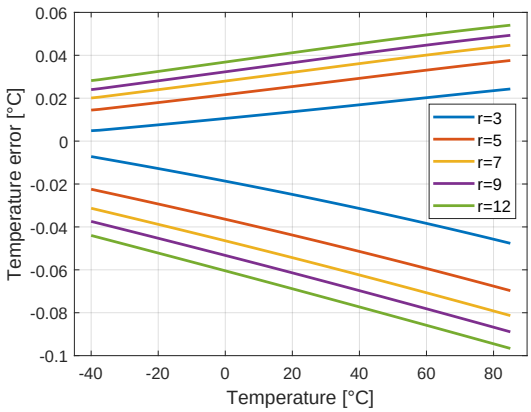

Figure 2.4: Accuracy over temperature and process corners for several values of r.

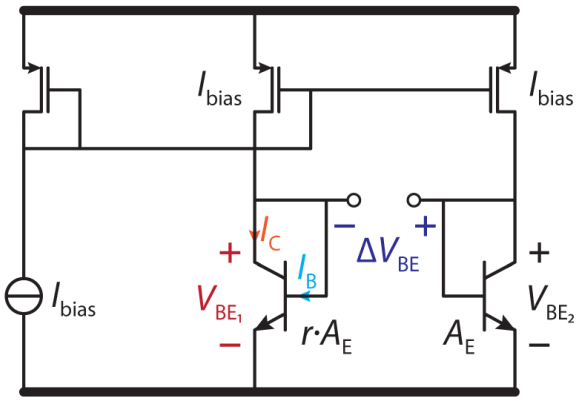

Figure 2.5: Test bench to determine the sensitivity of V_{BE} and ΔV_{BE} over temperature for different levels of I_{bias} with $r = 7$.

2.1.2. Collector Current

As the goal of this project is low power consumption, the aim is to reduce I_{bias}. However, I_S is not influenced by reducing I_{bias}, which limits the amount by which I_C, and thus I_{bias}, can be reduced. To achieve high accuracy, V_{BE} should not be influenced by I_S, in other words $I_C >> I_S$. Based on this assumption, the base emitter voltage V_{BE} becomes:

$$V_{BE} = V_T \cdot ln\left(\frac{I_C}{I_S}\right) \tag{2.5}$$

The differential voltage ΔV_{BE} becomes a linear function:

$$\Delta V_{BE} = V_T \cdot ln\,(p \cdot r) \quad \text{where} \quad p \cdot r = \frac{I_{C_2}}{I_{C_1}} \tag{2.6}$$

where p is the ratio of the two biasing currents and r is the ratio of the emitter areas between both BJT. In this design $p = 1$ and $r = 7$ is chosen, based on a trade-off between power consumption, resolution, ease of implementation and the fact that this is slightly more energy efficient than choosing the mathematically equivalent $p = 7$ and $r = 1$ [7].

The ratio r is created by adding several unit-sized BJTs in parallel in one branch. This ratio is higher than most TDC designs in literature. A higher ratio increases the sensitivity of ΔV_{BE} and thus improve the resolution [7]. However, increasing the ratio also increases the total biasing current, complicates matching and makes the accuracy over corners worse, as is shown in Figure 2.4. A ratio of $r = 7$ increases the sensitivity while not sacrificing too much accuracy over process corners.

Minimal Required Current

The minimum required current for one BJT can be determined by simulating $S_{\Delta V_{BE}} = \delta(\Delta V_{BE})/\delta T$. As ΔV_{BE} should be linear over temperature to enable accurate temperature measurements, its sensitivity should to be a constant. Figure 2.5 shows the simulated circuit, and Figure 2.6 the simulation results over temperature for multiple levels of I_{bias}. In this simulation $A_E = 10\mu m^2$, $r = 7$ and $p = 1$ in the TSMC $0.18\mu m$ process. It can be seen that $I_{bias} = 25$ nA is the lowest current for which $S\Delta V_{BE}$ is constant over the industrial temperature range (-40 °C to 85 °C).

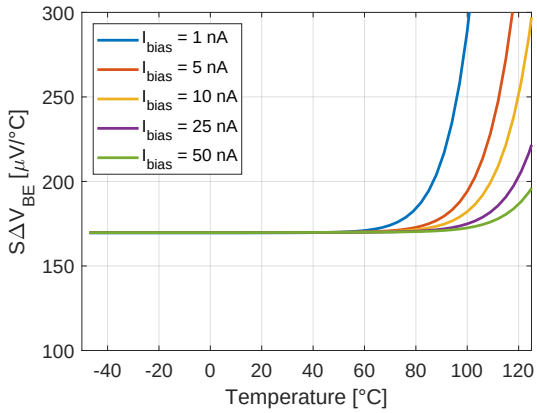

Figure 2.6: Sensitivity of ΔV_{BE_1} over temperature for multiple levels of I_{bias} with $r = 7$.

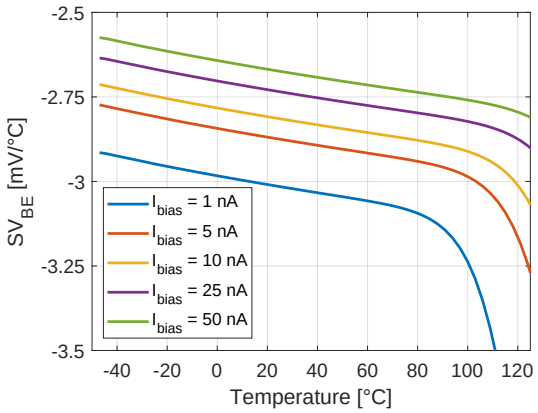

Figure 2.7: Sensitivity of V_{BE} over temperature for multiple levels of I_{bias} with $r = 7$.

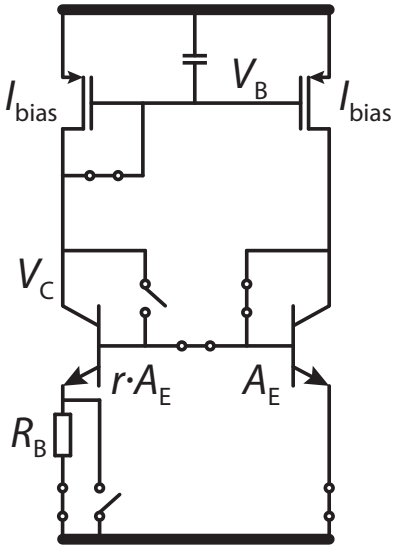

Figure 2.8: Proposed combined BJT frontend, configured as a biasing circuit.

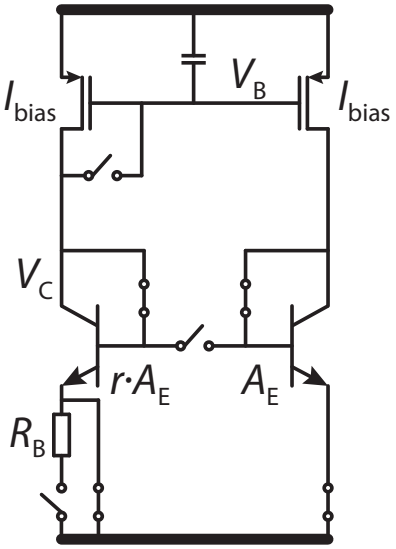

Figure 2.9: Proposed combined BJT frontend, configured as a BJT-core.

Due to its lower current density, V_{BE_1} sees the influence of I_{S} sooner than V_{BE_2}. Because of this, the sensitivity of ΔV_{BE} (Figure 2.6) shows an upward slope. With $I_{\mathrm{bias}} = 25$ nA and $r = 7$, the minimum current per unit A_{E} becomes $I_{\mathrm{C_{min}}} \approx 3.6$ nA. The next section discusses how I_{bias} can be accurately generated.

2.2. Dual Purpose Bandgap Design

To generate I_{bias} a biasing circuit is required. A secondary BJT pair traditionally generates the biasing current, as shown in Figure 2.1 (left). A current mirror then copies that current to the BJT-core, multiplied by a factor N to reduce the relative power dissipation of the biasing circuit (Figure 2.1). However, as the BJT-core is already designed to use the minimum required I_{bias}, scaling down the current is impossible. So both the biasing circuit and the BJT-core must use the same current levels. Using a traditional biasing scheme would thus double the power of the BJT frontend, so another approach is required.

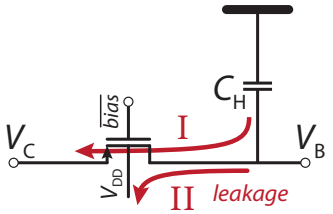

Figure 2.10: Simple PMOS switch and capacitor sample and hold circuit with leakage paths shown in red.

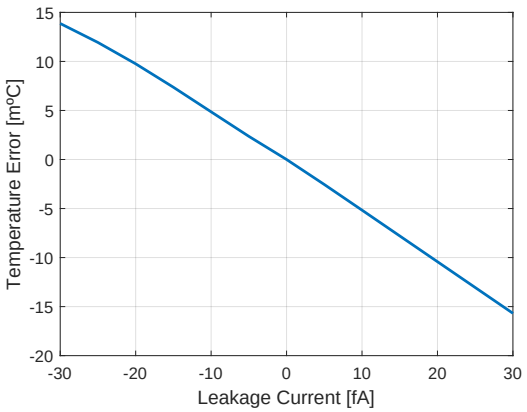

Figure 2.11: Temperature error due to the sample and hold leakage current for $C_H = 25$ pF at 25 °C

2.2.1. Sampled Biasing

As can be seen in Figure 2.1, the biasing circuit and the BJT-core are very similar. If both circuits could be merged it would effectively halve the power consumed in the frontend. In Figures 2.8 and 2.9 a circuit is proposed that can be configured either as a biasing circuit or as a BJT-core.

In the biasing configuration (Figure 2.8) ΔV_{BE} is forced across a resistor R_B to generate I_{bias}. In this design, $R_B = 2$ MΩ and it is realized as a non-salicided p+ poly HRI resistor. A current mirror then copies I_{bias} to the other BJT and generates a biasing voltage V_B, which is stored by a sample and hold circuit. When the circuit is used as a BJT-core (Figure 2.9), the held voltage V_B determines I_{bias} for both BJTs. Since it only takes a short time to set up V_B, this approach consumes much less power than the traditional approach.

2.2.2. Sample and Hold Requirements

The simplest sample and hold circuit consists of a PMOS switch that samples V_B on a capacitor C_H, as shown in Figure 2.10. The sample and hold circuit is required to hold V_B for 100ms. This is the conversion time required for a temperature measurement, and is determined by the minimal settling time per sample and the number of samples required by the ADC to achieve the target resolution. Both these time constraints will be discussed in more detail in Chapter 3.

The time that a voltage can be held on a capacitor depends on the leakage current through the sampling switch. The voltage droop on V_B due to that leakage current causes a time-dependent increase in V_{BE}, which causes a measurement error. A switch in parallel with an ideal leakage current source is used to model the transistor of Figure 2.10. The resulting temperature error after 100 ms is plotted versus the leakage current in Figure 2.11 for $C_H = 25$ pF. The slight jump around zero current is due to the finite resistance of the implemented switch. The large size of C_H is required to mitigate the temperature error caused by switch leakage. With an area of 0.02 mm^2, when implemented as a MIM capacitor, C_H will take up a large part of the chip area. However, as area is not part of the design specifications, this is of less concern.

For the leakage error not to be dominant, the additional error must be less than ±0.01 °C. From Figure 2.11 can be seen that the total leakage current can then be no larger than ±20 fA.

The leakage current through the switch consists of two parts, as shown in red in Figure 2.10. The first path (I) is through the depletion region and is due to the voltage difference between

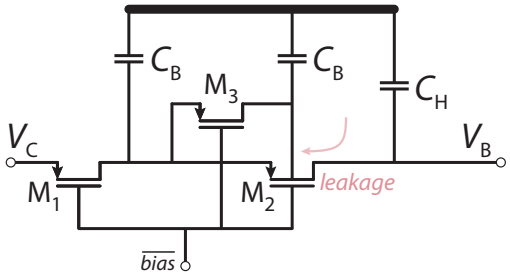

Figure 2.12: Bootstrapped PMOS switch sample and hold circuit to reduce leakage.

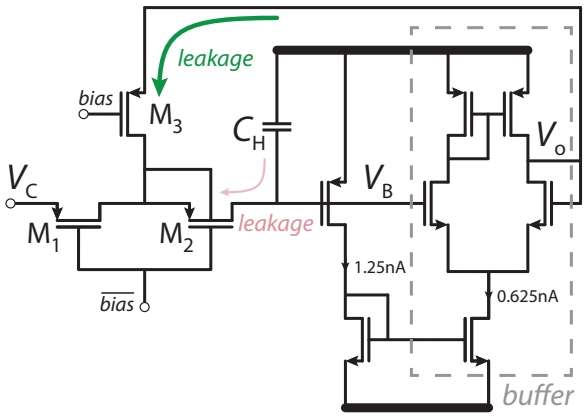

Figure 2.13: Buffer controlled low leakage sample and hold circuit based on [5], with the new leakage current path shown in green.

the drain and source regions of the transistor. The second path (II) is through the PN-diode to V_{DD} and is due to the voltage difference over this diode. A simulation of this circuit, shows the total leakage current of the PMOS switch to be ±275 fA over temperature with a maximal voltage difference of 495 mV, which is much larger than the ±20 fA allowed for the required accuracy.

Increasing the off resistance of the PMOS switch, by increasing its length, would reduce the leakage through the first path (I), but would also increase the charge injected into C_H, and so distort V_B. The leakage through the second path (II) can be reduced by decreasing the transistor width, which would reduce the diode area and thus the current. However, neither solution addresses the main cause of both leakage currents, the voltage difference across the switch.

2.2.3. Low-leakage Sample and Hold

Two circuits that can be used to reduce this voltage difference are shown in Figures 2.12 and 2.13. To determine which circuit is the most suitable for this design, the performance of both circuits is analysed.

Bootstrapped Sampling Switch

The first circuit (Figure 2.12) works by adding two additional sample and hold circuits, consisting of the switches M_1 and M_3, and the two capacitors $C_B = 3$ pF. These circuits bootstrap the original sampling switch (M_2) by sampling V_B on both C_B, removing the voltage difference. The switches M_1 and M_3 still leak, of course, which means that the voltage across M_2 will increase over time. A transient simulation of the circuit over the temperature range shows (Figure 2.14) that the leakage current through M_2 is less than ±20 fA after 100 ms.

Buffered Sample and Hold

As mentioned, Figure 2.13 shows another solution to reduce leakage. As proposed in [5], the single switch in Figure 2.10 is split into two switches, M_1 and M_2. A buffer is added after C_H and a third switch (M_3) applies the buffered biasing voltage V_O to the node between M_1 and M_2 when both these switches are open. The buffer only consumes 0.625 nW and a current mirror, used to provide the buffer's tail current, consumes another 1.25 nW. However, this mirror is also required for the biasing of the cascode of the high-swing current mirror as is discussed in

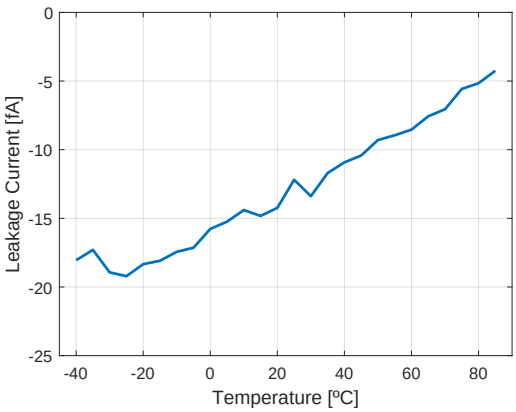

Figure 2.14: Temperature dependent leakage current of the bootstrapped sampling switch after 100 ms.

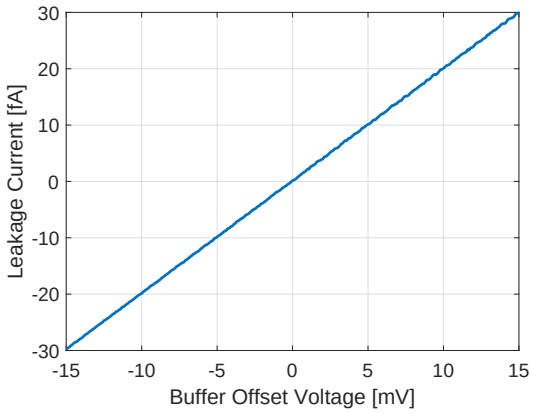

Figure 2.15: Leakage current due to the offset of the sample and hold buffer.

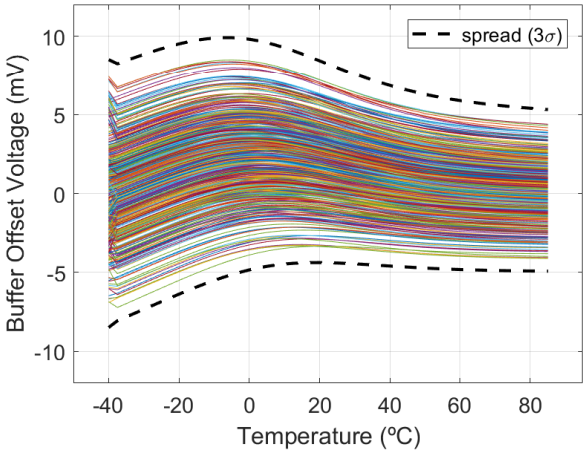

Figure 2.16: Monte Carlo spread of the offset of the sample and hold buffer

Section 2.4.3. While the circuit is holding V_B, the leakage currents of M_1 and M_3 are supplied by the buffer. The leakage through the both paths is now cancelled out because the voltage drop across M_2 is zero as $V_O = V_B$.

When $V_B \neq V_O$, e.g., due to offset in the buffer, there is still a leakage current. Figure 2.15 plots the total leakage current over the offset of the buffer. As can be seen, for a buffer offset of ±10 mV, the leakage current is ±20 fA, which was required for accuracy. The offset of the buffer is mainly dependent on process and varies with temperature. It can be reduced by increasing the area of the NMOS input pair and the PMOS current mirror.

A Monte Carlo simulation indicated that the optimal size of the NMOS input devices is 3 µm/16 µm, while that of the PMOS devices is 0.5 µm/16 µm. Figure 2.16 shows that the offset of the buffer is less than ±10 mV (3σ) over temperature and process, which causes a leakage current of ±20 fA, and thus a temperature error of ±0.01 °C.

Sample and Hold Comparison

The downside of the bootstrapped switch (Figure 2.12) is that is that it slows down the start-up of the circuit, is sensitive to charge injection of the sampling switches, and increases the area

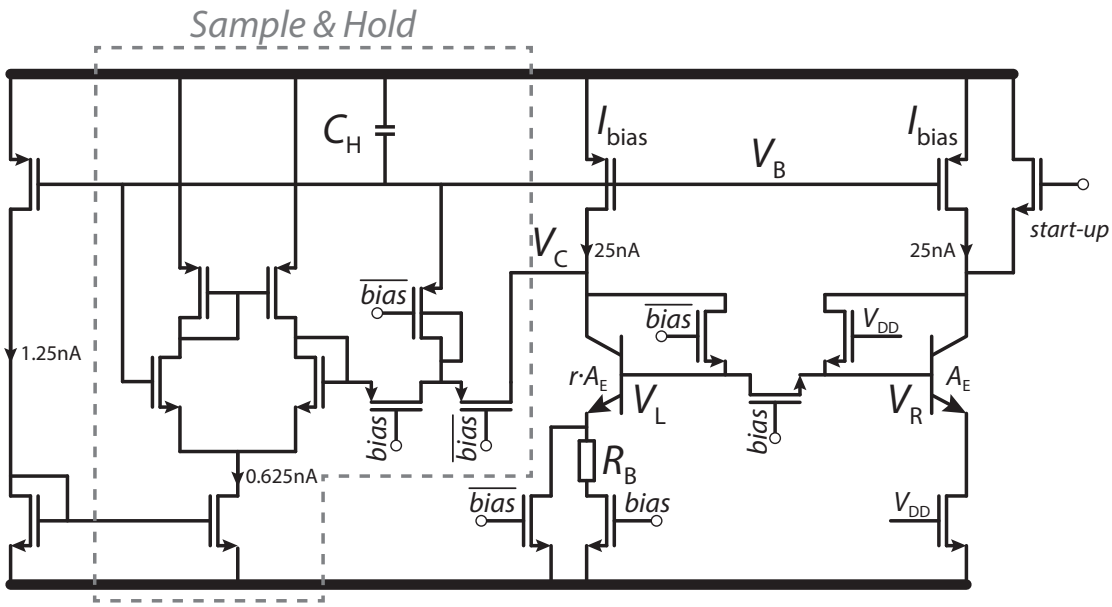

Figure 2.17: Dual purpose frontend with sample and hold biasing circuit.

of the chip by about 0.004 mm^2. However, as the capacitors are relatively large, the charge injection is negligible and it does not consume any static power nor suffers from offset like the buffered sample and hold circuit (Figure 2.13).

As the option of duty-cycling the TDC to reduce power consumption is considered, and the buffer only consumes 0.625 nW, the choice was made to use the buffered sample and hold circuit in this design.

2.2.4. Dual Purpose Frontend

Having found a way to keep the bias voltage V_B stable, it now becomes possible to merge the biasing circuit with the BJT-core. Figure 2.17 shows a simplified circuit diagram of the dual purpose BJT frontend. Two dummy switches, connected to V_{DD}, are added around the rightmost BJT to ensure equal offset and loading of both BJTs, as the transistors have a finite on-resistance. The total current required for the sample and hold circuit, consisting of an amplifier and a current mirror to provide the amplifier's tail current, is <2 nA, as shown in Figure 2.17. This current is significantly less than the 50 nA that a traditional biasing circuit would have required.

2.3. Sensor Start-up

To ensure the circuit starts up when power is applied, a switch is added in Figure 2.17. To limit the injected current, a long NMOS switch with a length of 10 µm and a width of 1 µm is used. The voltages V_L and V_R at the bases of both BJTs are shown for the start-up and biasing sequence of the BJTs frontend in Figures 2.18 and 2.19. As both bases are shorted in biasing configuration: $V_L = V_R = V_{BE_2}$. Once V_B has settled and the frontend is reconfigured as a BJT-core, a jump can be seen in Figure 2.17 as now $V_L = V_{BE_1}$. As was shown in both figures, the start-up is temperature dependent and it takes up to 5 ms at -40 °C for V_{BE_2} to settle. The spikes after biasing are due to the charging of the sampling capacitors. The signals that control both biasing and start-up are generated off-chip and are controlled via a shift register, which is explained in Section 4.2.1.

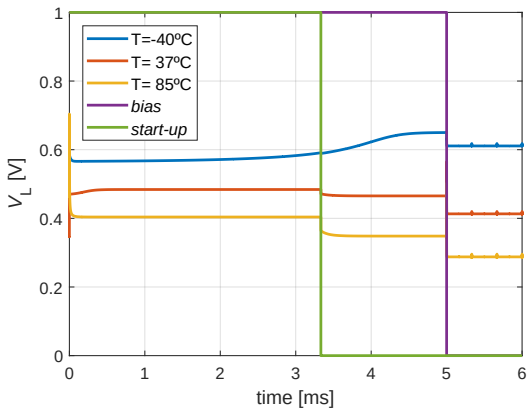

Figure 2.18: Startup sequence of the self-biased BJT-based temperature sensor for V_{BE_1}.

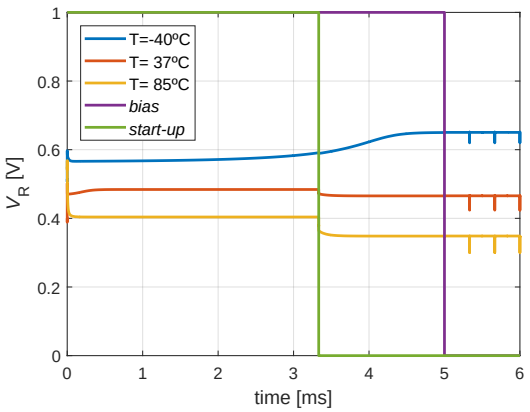

Figure 2.19: Startup sequence of the self-biased BJT-based temperature sensor for V_{BE_2}.

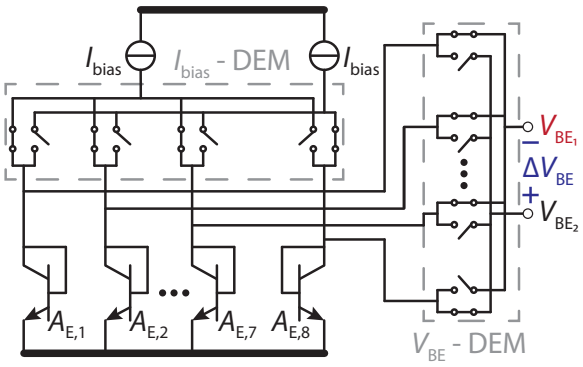

Figure 2.20: DEM circuit as implemented in the BJT-core.

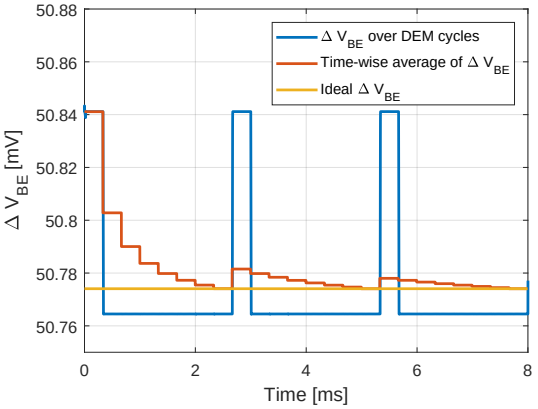

Figure 2.21: DEM timing diagram where $A_{E,8}$ is smaller than the rest.

2.4. Sensor Accuracy

For accurate temperature measurements it is required that the biasing currents match and that the current density ratio is exactly equal to r. Several techniques have been implemented to ensure this. To improve the overall matching, dummy devices have been added in layout surrounding the current mirror transistors, sampling capacitors and the BJTs. The layout of the entire TDC will be shown in Chapter 4. The accuracy of the current density ratio is solved by using DEM, and that of the matching of the biasing current is solved by chopping.

2.4.1. Dynamic Element Matching

The mismatch in the emitter area ratio introduces an offset error in ΔV_{BE} and both V_{BE}. Due to the stochastic nature of the error, it is not possible to reduce this error by using a static compensation circuit, and so dynamic element matching (DEM) is required.

A simplified diagram of the DEM circuit is shown in Figure 2.20. Here, the switches I_{bias}-DEM dynamically alter the configuration of the BJTs, moving the offset around between V_{BE_1} and V_{BE_2}. However, as each I_{bias}-DEM switch adds its on-resistance in series with its respective BJT, V_{BE_1} and V_{BE_2} cannot be sampled directly below the current sources. Therefore, the switches V_{BE}-DEM are introduced to create what is called a Kelvin connection. The added resistance of

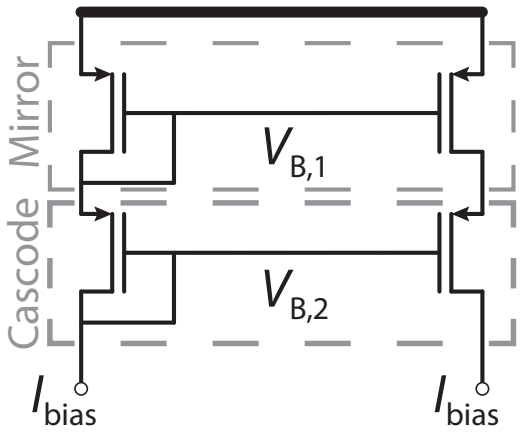

Figure 2.22: Cascode current mirror circuit

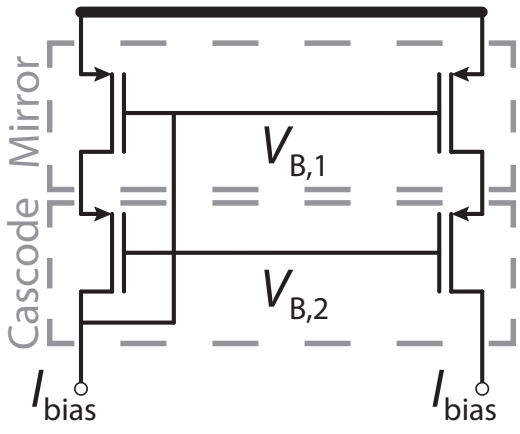

Figure 2.23: High swing current mirror circuit

the V_{BE}-DEM switches does not influence the sampling of either V_{BE}, as the current through the switch is zero when settled.

A full DEM cycle consists of steps equal to the number of BJTs, in this case, eight. In each step the ADC samples and integrates V_{BE_1} and ΔV_{BE}, effectively averaging the offset caused by the mismatch, as is shown for ΔV_{BE} in Figure 2.21. It should be noted that after each full DEM cycle the total error is perfectly cancelled.

2.4.2. Chopping

Both sets of DEM switches can also be used for chopping the sensor. The switches I_{bias}-DEM can chop the current sources, while the switches V_{BE}-DEM can chop the output. If two measurements are done back to back and the result of both is averaged, the mismatch between the two current paths is corrected.

2.4.3. High-Swing Current Mirror

To further improve accuracy, a cascoded current mirror is used, as shown in Figure 2.22. This ensures that the drain voltages of the basic current mirror are equal, reducing the effect of channel length modulation.

The downside is that cascoding two current mirrors significantly reduces the voltage swing at the output of the sensor, as both diode-connected transistors require a voltage drop of $V_T \approx 0.3$ V. As V_{BE} changes with temperature, the output of the sensors must have sufficient voltage headroom to encompass the entire temperature range. Using a high-swing current mirror [22] improves the voltage swing while maintaining the benefit of a cascoded current mirror. The high-swing current mirror is shown in Figure 2.23.

The cascode devices of the high-swing current mirror have to be biased. Figure 2.24 shows a simple biasing circuit. It consists of a tail current source and a diode connected stack of transistors to generate $V_{B,2}$. A capacitor $C_{H_2} = 1$ pF is added to reduce the sensitivity of $V_{B,2}$ to transient variations in the power supply. The entire circuit only requires another 1.25 nA, bringing the total current required to bias the BJT-core to 3.125 nA, which is still a lot less than the 50 nA mentioned before.

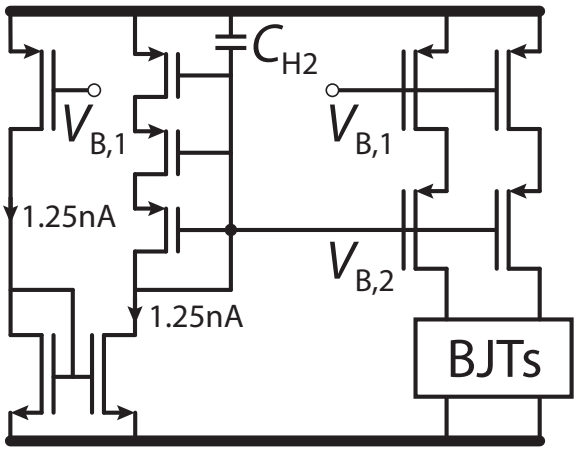

Figure 2.24: Biasing circuit for the cascode of the high-swing current mirror.

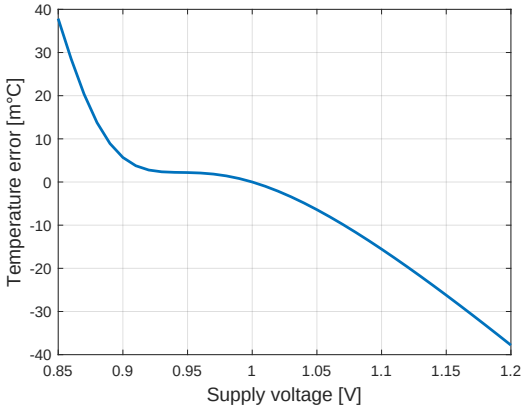

Figure 2.25: Sensitivity of the temperature measurement to variations in the power supply.

Reduced Power Supply

The reduction of I_C has the additional benefit of reducing V_{BE}. This reduction, in combination with the high-swing current mirror, enables us to further reduce power consumption by lowering the TDC's supply voltage. In the TSMC 0.18 μm technology, circuits are usually powered by a 1.8 V supply, which can be lowered to 1 V in this design.

Care has to be taken that the circuit does not become sensitive to variations in the supply, so for this design the PSS is set at 0.1 °C/V. Figure 2.25 shows the temperature error of the sensor when the source is swept from 0.85 V to 1.2 V, normalized around 1 V. As can be seen, the PSS is highly non-linear. Over the plotted range the sensor has a PSS of 0.16 °C/V, which is slightly too high. However, from 0.9 V to 1.1 V the PSS does drop below the design target, to 0.09 °C/V.

2.5. Final Frontend Design

The final design of the BJT frontend is shown Figure 2.26. It consists of a dual purpose circuit that can be switched from a biasing circuit to a BJT-core. To maintain the correct biasing while used as a BJT-core, a low-leakage sample and hold circuit is added. A DEM circuit ensures an accurate current ratio r on average. It can also be used as a chopper to improve the matching of the biasing currents. A high-swing current mirror is used to lower the supply voltage and further improve the matching between the biasing currents. The power consumed by the BJT frontend is 53 nW, of which only 3 nW is consumed by the biasing circuit.

2.5.1. Temperature Behaviour

The temperature sensitive signals V_{BE_1}, V_{BE_2} and ΔV_{BE} of the final BJT frontend are plotted in Figure 2.27. As shown in equations (1.3) and (1.4) the temperature can be determined by

$$\mu = \frac{\alpha \cdot \Delta V_{\mathrm{BE}}}{V_{BE_1} + \alpha \cdot \Delta V_{\mathrm{BE}}} = \frac{\alpha \cdot \Delta V_{\mathrm{BE}}}{V_{\mathrm{REF}}} \quad \Rightarrow \quad T = A \cdot \mu + B$$

where $\alpha = 15.86$, $A = 472$ and $B = -279$. The resulting temperature is plotted over the actual temperature in Figure 2.28, together with the temperature error. As can be seen, the calculated temperature closely follows the actual temperature, showing a 3rd order error only of ±0.009 °C. The other results of the BJT frontend will be presented in Chapter 5.

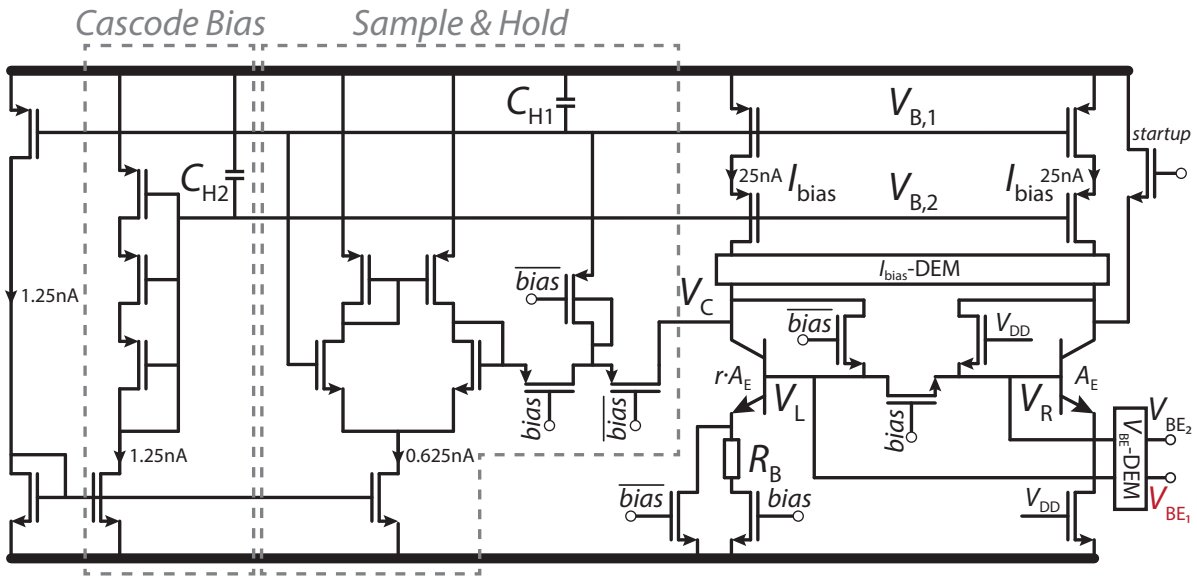

Figure 2.26: Simplified version of the final design of the dual purpose bandgap design with a high-swing cascode mirror and DEM switches.

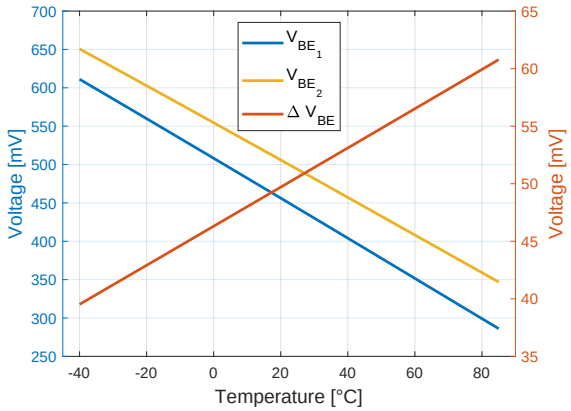

Figure 2.27: Final BJT frontend output results V_{BE_1}, V_{BE_2} and ΔV_{BE} with $r = 7$ and $I_{\mathrm{bias}} = 25$ nA over temperature.

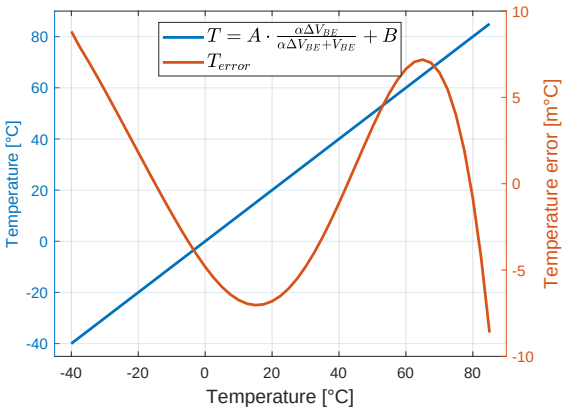

Figure 2.28: Calculated temperature and temperature error based on V_{BE_1} and ΔV_{BE} over temperature.

3

ADC Design

This chapter focuses on the design and requirements of the ADC. It should achieve the required resolution (0.01 °C) and power consumption (50 nW), while maintaining the sensor's accuracy. In Section 3.1, the interaction between the BJT front-end and the ADC is discussed, followed by a description of the ADC's top-level design in Section 3.2. The ADC's operation is split into a coarse-conversion phase (see Section 3.3), and a fine-conversion phase (see Section 3.5). Both phases require the use of a feedback DAC, which will be discussed in Section 3.4. Techniques to improve ADC accuracy are discussed in Section 3.6 and the final topology of the ADC is presented in Section 3.7.

3.1. BJT-readout Analysis

A ΣΔ-ADC, or ΣΔ-modulator, is often used to read out temperature sensors because it trades conversion speed for resolution. This makes it ideally suited for temperature sensors, since temperature changes are rather slow, but usually need to be digitized with high resolution. The ADC shown in Figure 3.1 [6], operates by digitizing V_{PTAT} respective to a temperature independent reference voltage V_{REF} as shown in equation (3.1).

$$\mu = \frac{V_{\text{PTAT}}}{V_{\text{REF}}} = \frac{\alpha \cdot \Delta V_{\text{BE}}}{V_{\text{BE}_1} + \alpha \cdot \Delta V_{\text{BE}}} \tag{3.1}$$

Digitizing temperature this way is rather inefficient because the resulting μ changes by only 30% over the military temperature range, as can be seen in Figure 3.2. Alternatively, the range of μ can be increased to 90% by evaluating:

$$\mu = \frac{2\alpha \cdot \Delta V_{\text{BE}} - V_{\text{BE}_1}}{V_{REF}} \tag{3.2}$$

but this comes at the cost of increased complexity [6].

From equation (3.1) it can be observed that all temperature information is present in the two voltages V_{BE_1} and ΔV_{BE}. The equation can be rewritten as:

$$\mu = \frac{\alpha \cdot \Delta V_{\text{BE}}}{V_{\text{BE}_1} + \alpha \cdot \Delta V_{\text{BE}}} = \frac{\alpha}{\frac{V_{\text{BE}_1}}{\Delta V_{\text{BE}}} + \alpha} = \frac{\alpha}{X + \alpha} \tag{3.3}$$

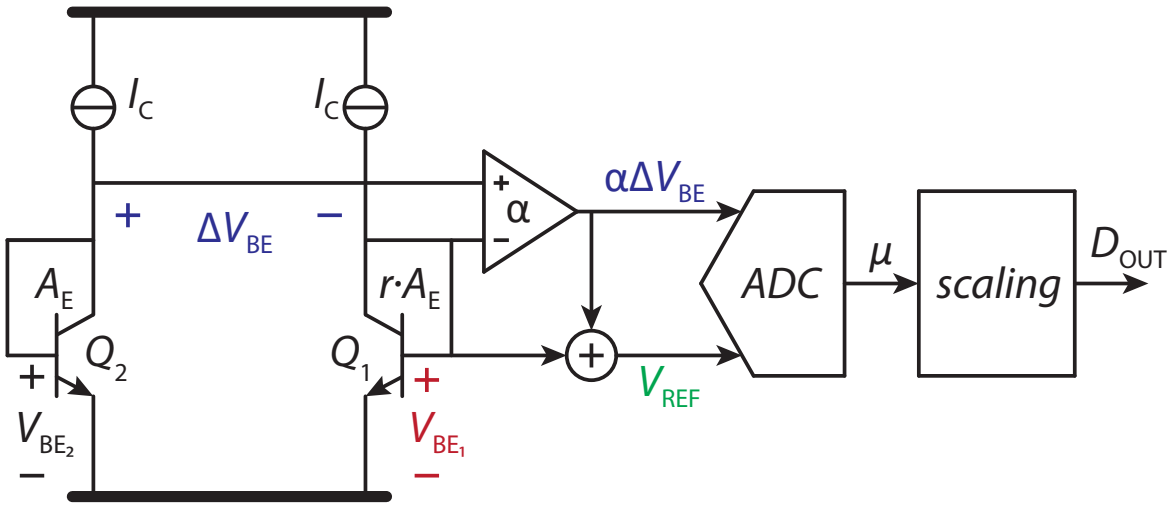

Figure 3.1: Bandgap TDC readout principle [6].

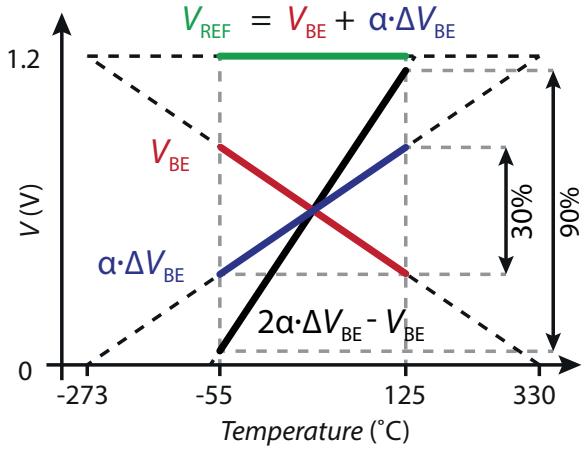

Figure 3.2: Increased the dynamic range of μ with respect to temperature over the military temperature range [6].

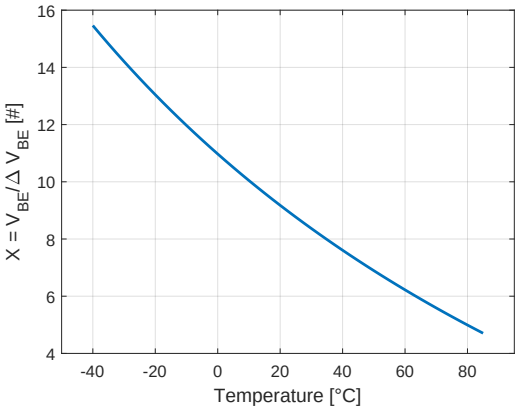

Figure 3.3: Behavior of X over the industrial temperature range, for $r = 7$ and $I_C = 25$ nA.

where $X = V_{BE_1}/\Delta V_{BE}$. This suggests that only the ratio X needs to be digitized to perform a temperature measurement. Figure 3.3 illustrates X as a non-linear function of temperature, where X ranges from 4 to 16 over the industrial temperature range (with current density ratio $r = 7$ and $I_C = 25$ nA). Since the range of X is larger than 1, the ratio can be divided into an integer and a fractional part:

$$X = \frac{V_{BE_1}}{\Delta V_{BE}} = n + \mu' \tag{3.4}$$

where n represents the integer part, and μ' the fractional part of X. This effectively cuts the ratio X into several integer steps that can be digitized separately. It enables the use of a two-step approach [7], which greatly improves the efficiency of the ADC. Another advantage of digitizing X is that a PTAT trim can be performed, by simply adding an offset to X. The downside is that a digital back-end is required to obtain the PTAT output μ from equation (3.3). Because of these reasons, this design uses a two-step or Zoom ADC to digitize X.

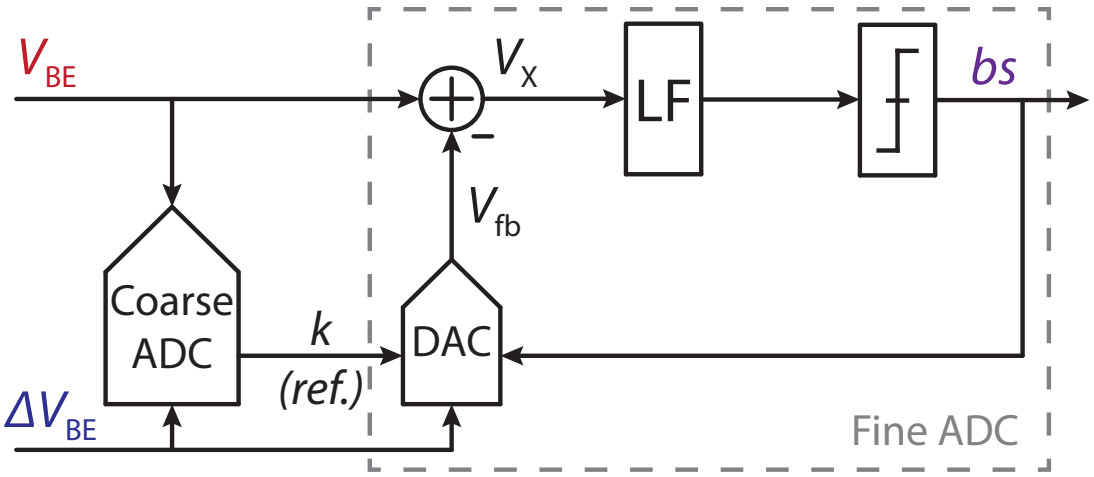

Figure 3.4: Block diagram of the Zoom ADC, split into a coarse conversion to determine k, and a fine conversion to determine μ'.

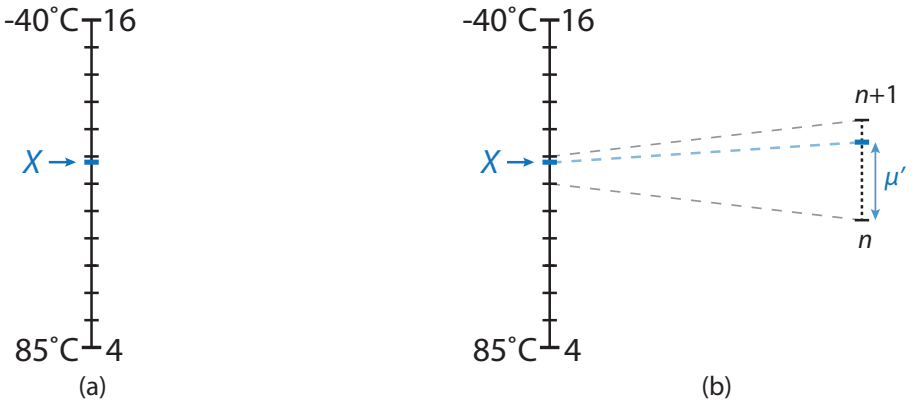

Figure 3.5: (a)TDC coarse conversion thermometer; (b) Zoomed fine range of n to $n+1$ based on the coarse conversion result.

3.2. Zoom ADC Topology

The block diagram of the proposed Zoom ADC is shown in Figure 3.4 and is based on the design presented in [4]. The ADC's operation is split into a coarse conversion and a fine conversion. The coarse conversion determines n, giving a rough estimate of X, as is shown in Figure 3.5(a). The fine conversion then uses this estimate to set the references of the ΣΔ-modulator to $n \cdot \Delta V_{BE}$ and $(n+1) \cdot \Delta V_{BE}$, as shown in Figure 3.5(b). This zooming reduces the ΣΔ-modulator's range, thereby reducing the quantization noise of the ΣΔ-modulator, and so improving its power-efficiency. Next, the coarse conversion topology is presented, and inherent conversion errors are addressed.

3.3. Coarse Conversion

The coarse conversion gives a rough estimate of the temperature by determining n. As was shown in Figure 3.5, to facilitate the fine conversion, n has to conform to $n \cdot \Delta V_{BE} < V_{BE} < (n+1) \cdot \Delta V_{BE}$. Figure 3.6 shows the block diagram of the coarse conversion step. Here, a gain

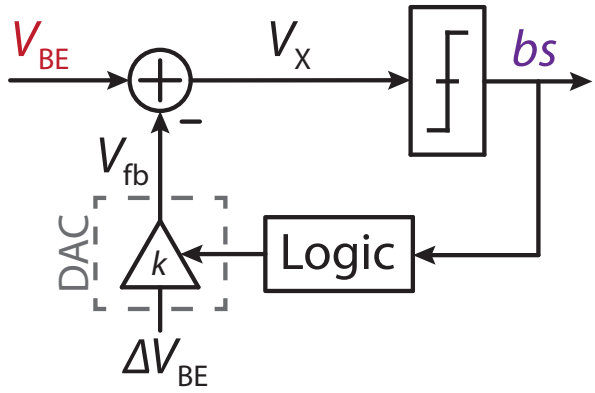

Figure 3.6: Block diagram of the coarse conversion to determine k.

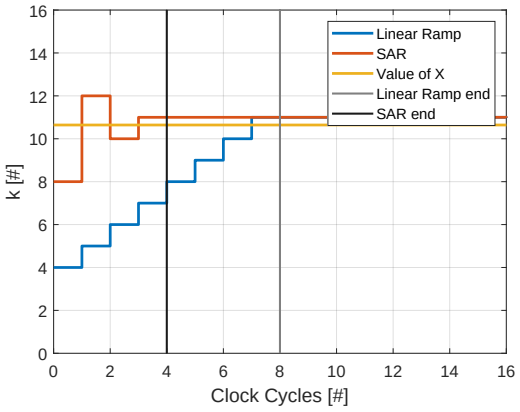

Figure 3.7: Comparison between linear ramp and SAR approach to determine k over clock cycles at room temperature.

factor k, created by a digital to analog converter (DAC), is used to generate a signal V_{fb}:

$$V_X = V_{BE} - V_{fb} = V_{BE} - k \cdot \Delta V_{BE} \tag{3.5}$$

A comparator then evaluates the sign of V_X and the logic then updates k accordingly to find the value of k for which:

$$(k-1) \cdot \Delta V_{BE} < V_{BE} < k \cdot \Delta V_{BE} \tag{3.6}$$

at which point, X is between $k-1$ and k, i.e., $n = k-1$.

There are two approaches to determine k, by using a 13-bit linear ramp ADC or a 4-bit SAR-ADC. Figure 3.7 shows a comparison between the linear ramp and SAR in terms of the number of clock cycles required at room temperature. As can be seen, the SAR-ADC requires fewer clock cycles per conversion. However, compared to the approximately 300 clock cycles required by the ΣΔ-modulator (as is explained later) this difference is negligible. So, for ease of implementation, the 13-bit linear ramp approach is used, where k is ramped from 4 to 16 until the comparator output switches.

3.3.1. Guard-Banding

Errors in the coarse conversion, e.g., due to sampling noise or mismatch, can cause a situation in which X lies outside the range of the references of the fine conversion. This has a higher probability of occurring when X is close to n or $n+1$. Furthermore, a 2nd-order ΣΔ-modulator only uses about 75% of its reference range effectively [23]. Over-ranging can be used to mitigate both these sources of error.

The over-ranging step γ reduces the effectiveness of zooming in the fine conversion and increases the output swing required by the integrator (discussed in Section 4.1). Writing the equation for the ΣΔ-conversion, an expression for μ'', which accounts for γ, can be found:

$$\begin{aligned} \mu'' \cdot [V_{BE} - (n+1+\gamma) \cdot \Delta V_{BE}] + (1-\mu'') \cdot [V_{BE} - n \cdot \Delta V_{BE}] = 0 \\ \Rightarrow \mu'' = \frac{V_{BE} - n \cdot \Delta V_{BE}}{(1+\gamma) \cdot \Delta V_{BE}} \end{aligned} \tag{3.7}$$

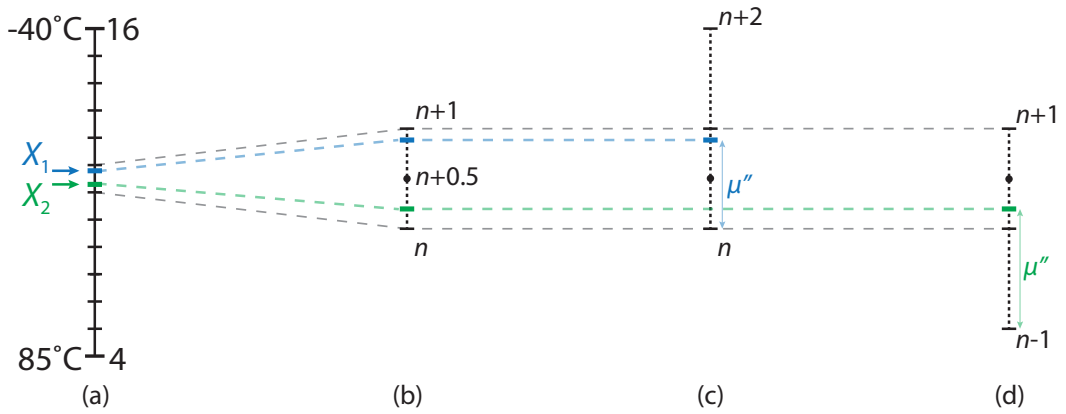

Figure 3.8: (a) Coarse conversion; (b) guard-banding; (c) fine range when $X > n + 0.5$; (d) fine range when $X < n + 0.5$

Consequently equation (3.4) changes to $X_{new} = n + (1 + \gamma) \cdot \mu''$, effectively reducing the resolution of the fine conversion by a factor of $1 + \gamma$.

An over-ranging solution is implemented in [4]. The fine range is extended by the minimal over-ranging step of $\gamma = 1$, and so an additional conversion step is required to determine if this step is added on the top or bottom of the range, as is shown in Figure 3.8. This so called guard-banding checks if $X < (n + 0.5)$ and the fine range is shifted accordingly:

$$V_{\text{fb}} = \begin{cases} n \cdot \Delta V_{\text{BE}} & \text{when } bs = 0 \\ (n+2) \cdot \Delta V_{\text{BE}} & \text{when } bs = 1 \end{cases} \quad \text{when } X > n + 0.5$$
$$\begin{cases} (n-1) \cdot \Delta V_{\text{BE}} & \text{when } bs = 0 \\ (n+1) \cdot \Delta V_{\text{BE}} & \text{when } bs = 1 \end{cases} \quad \text{when } X < n + 0.5 \tag{3.8}$$

3.3.2. Cold-start Conversion

Body temperature is usually a slow-changing signal (<1 °C/s), and so a previous measurement result (X_{prev}) can be used to set the new fine range. However, this approach cannot be used at start-up, thus requiring an initial coarse conversion: the cold-start conversion. This approach saves the power consumed by the coarse conversion, simplifies the operation of the TDC and is not influenced by mismatch in the feedback DAC. For these reasons the cold-start conversion approach is used in this design.

3.4. Feedback DAC

Comparing the block diagram of the coarse conversion (Figure 3.6) to the fine conversion of the Zoom-ADC (Figure 3.4), it is clear that these topologies are very similar. To simplify the design process and ensure matching, both parts of the ADC use the same DAC. For the fine conversion the DAC needs to be able to select V_{fb} from multiple references, as given by equation (3.8), which can be generated with either a multi-capacitor or a single-capacitor DAC.

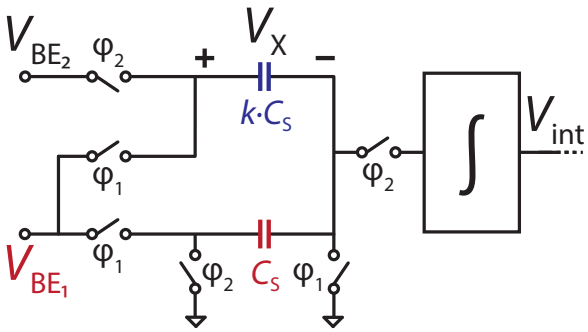

Figure 3.9: Multi-capacitor DAC single sided diagram.

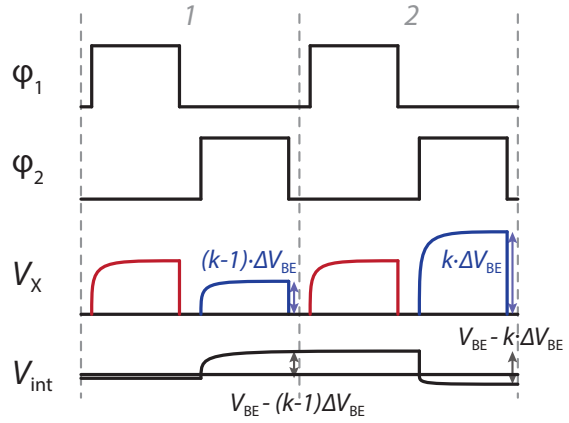

Figure 3.10: Multi-capacitor DAC timing diagram for two clock periods.

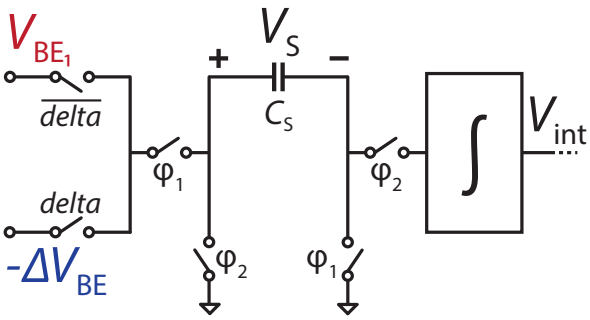

Figure 3.11: Single-capacitor DAC single sided diagram.

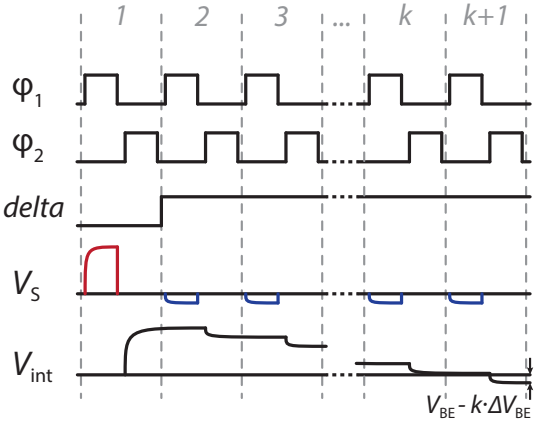

Figure 3.12: Single-capacitor DAC timing diagram.

3.4.1. Multi-Capacitor DAC

In [7], the DAC consists of k parallel capacitors, which sample either V_{BE_1} or V_{BE_2}. A simplified circuit of this implementation is shown in Figure 3.9. During ϕ_1 the circuit samples V_{BE_1} on $(k+1)\cdot C_{\mathrm{S}}$ and then during ϕ_2 it samples V_{BE_2} on $k\cdot C_{\mathrm{S}}$ to obtain the desired V_{X}, as is shown in Figure 3.10. The advantages of this approach are that the DAC produces an output within a single clock cycle, and that the integrated charge Q_{X} is cancelled to first order:

$$Q_{\mathrm{X}} = C_{\mathrm{S}}(V_{\mathrm{X}}) = C_{\mathrm{S}}(V_{\mathrm{BE}} - k\cdot\Delta V_{\mathrm{BE}}) \tag{3.9}$$

This charge cancellation reduces the speed and swing requirements of the integrator. The downside of this approach is that DEM is required to mitigate the effect of mismatch in the parallel capacitors.

3.4.2. Single-Capacitor DAC

As the name suggests, this topology uses a single sampling capacitor C_{S} that consecutively samples V_{BE} and then k times $-\Delta V_{\mathrm{BE}}$. A simplified circuit of such an implementation is shown in Figure 3.11, where the signal $delta$ selects the input voltage. Each separate charge is integrated,

which over time generates a voltage proportional to V_X. Because there is only one capacitor C_S, there is no issue with mismatch and therefore no need for DEM. However, the timing of this sampling method is more complicated, as can be seen from the timing diagram in Figure 3.12. The number of samples to obtain Q_X now depends on k and the integrator has to handle a charge swing up to:

$$Q_{max} = max \begin{cases} -k \cdot Q_{\Delta V_{BE}} \\ Q_{V_{BE}} \end{cases} \tag{3.10}$$

which shows that $Q_{max} >> Q_X$. The integrator will thus require a larger output swing and the DAC requires multiple cycles to converge. Because of these reasons a multi-capacitor DAC is used in this design.

3.5. Fine Conversion

After n is determined by the coarse conversion, the ΣΔ-modulator determines the fraction μ''. Its resolution is limited by quantization and thermal noise, which, in turn, depend on the fine range, the order of the loop filter and the number of samples [23]. To determine these last two parameters, first, equations for both the quantization noise and the thermal noise need to be derived.

3.5.1. Thermal Noise

Ideally, a ADC is thermal noise limited. By calculating the sampled thermal noise based on [24], the resolution (σ_T) of the TDC can be shown (see Appendix A) to be:

$$\sigma_T \approx A \cdot \frac{\alpha \cdot \Delta V_{BE}}{V_{REF}^2} \sqrt{\frac{(7/3) \cdot k_B T \cdot X}{N \cdot C_S}}. \tag{3.11}$$

Here A is the gain factor from μ to temperature and N is the number of samples. To minimize σ_T, the product $N \cdot C_S$ must be maximized. C_S is limited to 134 fF by settling, and so N must be increased to 320 to achieve the target resolution. In this design, X is small compared to other state of the art designs because of reduced I_C and increased current density ratio r, which helps to improve the energy efficiency.

3.5.2. Quantisation Noise

The effective number of bits (ENOB) required to achieve the desired quantization noise level is derived in [7]:

$$ENOB \approx log_2 \left(\frac{X_{range}}{\Delta X} \right) - 1 \tag{3.12}$$

and is plotted in Figure 3.13 over temperature for $r = 7$ and $X_{range} = X_{max} - X_{min} = 12$. The required ENOB to achieve the target resolution over the temperature range is 12.4 bits. Figure 3.14 shows that an ideal first order modulator with guard-banding requires ~770 samples, while a second order modulator requires ~50 samples to achieve the 12.4 bits. Since the number of samples required by the thermal noise is 320, a second order modulator is required.

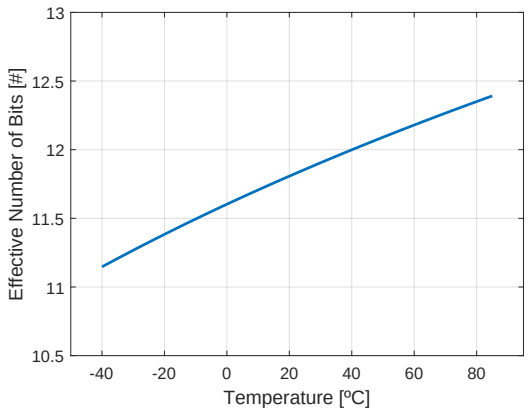

Figure 3.13: ENOB required over temperature (with r=7 and X_{range}=12) to achieve a target resolution of ±0.01 °C.

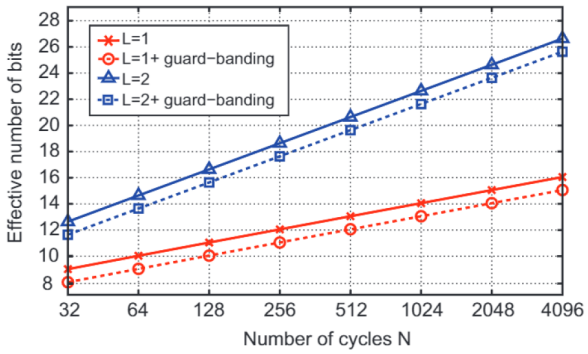

Figure 3.14: Number of samples required to achieve a desired ENOB [7].

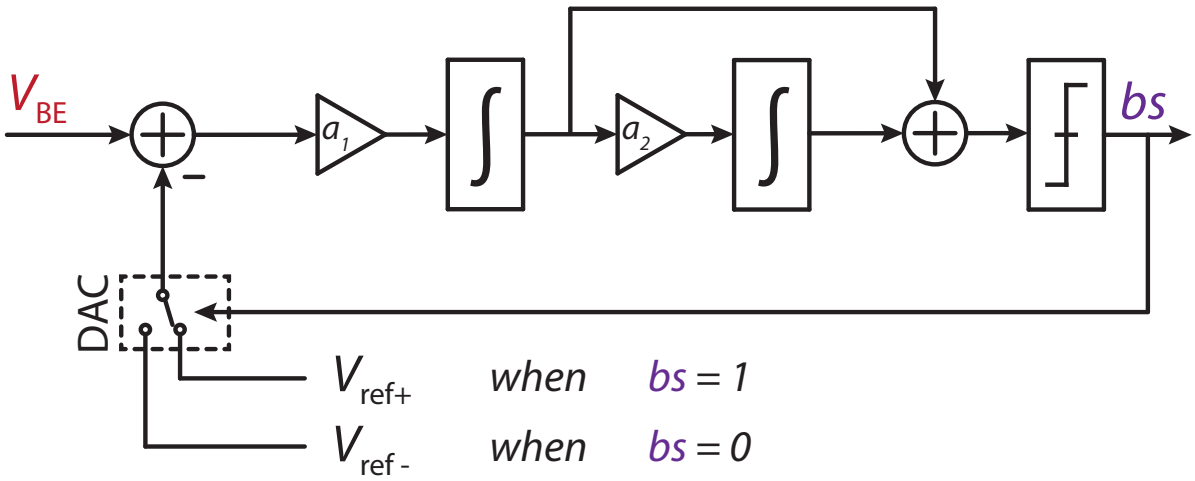

Figure 3.15: Block diagram of a 2nd-order feed-forward ΣΔ-modulator.

Figure 3.15 shows the block diagram of the 2nd-order feed-forward ΣΔ-modulator. The gain factors $a_1 = 1/8$ and $a_2 = 1/2$ are chosen based on the output swings of the respective integrators. These choices are discussed in more detail in Section 4.1.

3.6. Accuracy Improvement Techniques

The mismatch of the sampling capacitors and the input stages of the used operational transconductance amplifiers (OTAs) have the most influence on the accuracy of the ADC. Issues caused by mismatch can be split into three parts: First, mismatch between the left and right halves of the differential structure is compensated by chopping, see Section 3.6.1. Second, mismatch of the sampling capacitors is reduced using DEM, see Section 3.6.2. Third and last, mismatch in the first integrator causes offset, which is canceled by correlated double sampling (CDS), see Section 3.6.3.

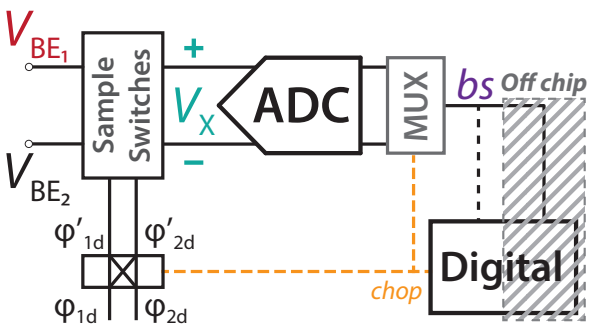

Figure 3.16: System level chopping circuit adiagram.

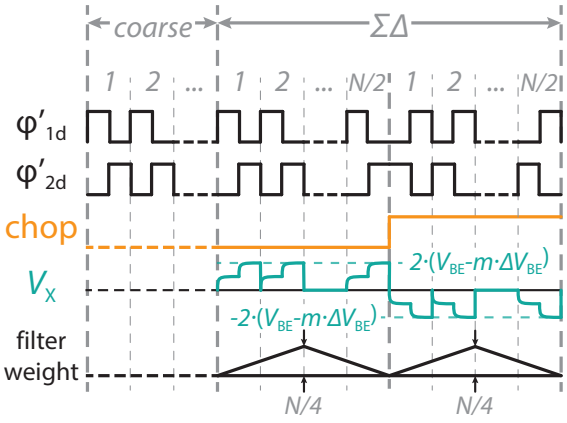

Figure 3.17: System level chopping timing diagram.

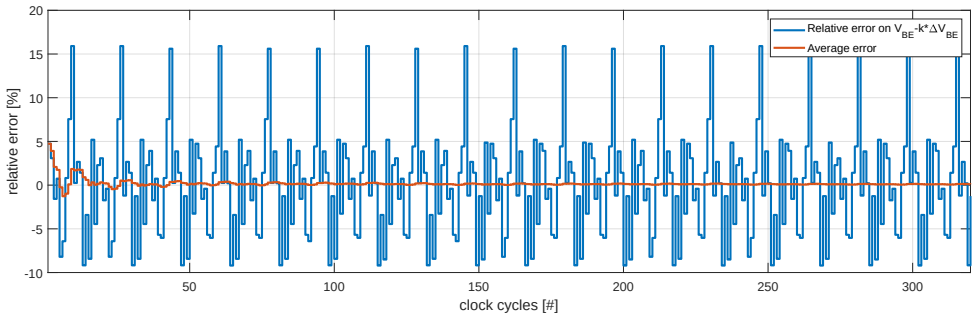

Figure 3.18: Barrel shifting DEM scheme.

3.6.1. System-level Chopping

System-level chopping is used to filter out systematic errors between the two differential halves. Since V_{BE_1} and V_{BE_2} are not differential signals, but two different signals, they cannot be chopped. Instead, the clock signals controlling the sampling switches are chopped, as shown in Figure 3.16. This changes the polarity of V_X, thus effectively chopping the input of the ADC, as is shown in Figure 3.17. The output of the ADC is chopped using a MUX. Both chop phases use half the number of samples, effectively keeping the same conversion time. This approach increases quantization noise, but the design is still thermal noise limited.

3.6.2. Dynamic Element Matching

To reduce the error caused by the mismatch between the unit sampling capacitors C_S, DEM is used. Unfortunately, the ratio k changes after each ΣΔ-cycle; which complicates the task of ensuring that each capacitor is used in all positions evenly. Still, the error caused by the mismatch can be reduced significantly, as was shown in [4]. A mismatch simulation on the sampling capacitors of the ADC shows the effectiveness of DEM (Figure 3.18). The configuration of the sampling capacitors is barrel-shifted by a single step after each ΣΔ-cycle. Since k changes during the conversion, data-weighted averaging is required to cancel the error completely. However, due to the large amount samples taken by the ΣΔ-modulator, the averaging effect of DEM reduces the error significantly to about 0.01%, as can be seen from Figure 3.18.

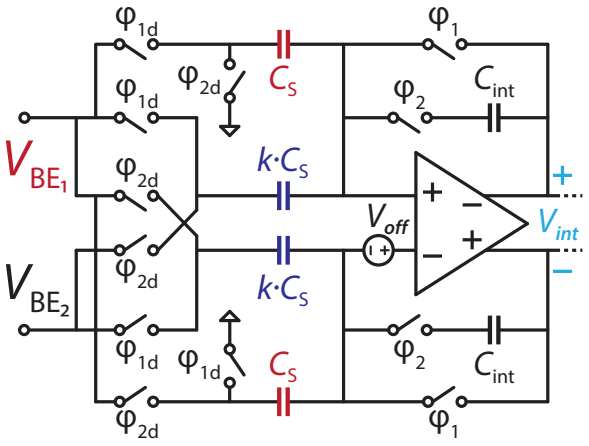

Figure 3.19: CDS circuit diagram with differential integrator offset.

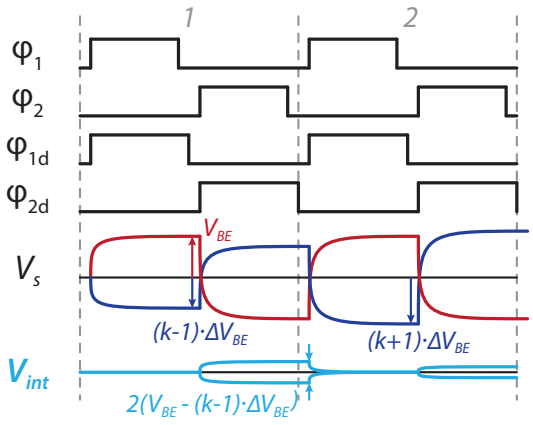

Figure 3.20: CDS timing diagram.

3.6.3. Correlated Double Sampling

The differential CDS circuit and its timing diagram are shown in Figure 3.19 and 3.20 respectively. Using CDS, the differential offset of the integrator is cancelled. During ϕ_1, the input is sampled and the integrator is shorted to store V_{off} on the back-plates of the sampling capacitors, and so the total stored charge is $[(k+1)\cdot V_{\text{BE}_1} - k\cdot V_{\text{BE}_2} + (2k+2)\cdot V_{\text{off}}]\cdot C_{\text{S}}$. During ϕ_2, the stored charge on the capacitors is $[(k)\cdot V_{\text{BE}_2} - (k+1)\cdot V_{\text{BE}_1} + (2k+2)\cdot V_{\text{off}}]\cdot C_{\text{S}}$ and the difference in charge is integrated into C_{int}, which is:

$$V_{\text{int}} = 2(V_{\text{BE}} - k\cdot\Delta V_{\text{BE}})\cdot\frac{C_{\text{S}}}{C_{\text{int}}}. \tag{3.13}$$

3.7. ADC Topology

The ADC topology is shown in Figure 3.21. Here, the input is sampled on the DEMed sampling capacitors by the sampling and chopping switches. The total charge is integrated on the first stage using CDS. A capacitor ratio implements the feedforward gain to the second stage integrator. The 2nd integrator can be bypassed for the cold-start coarse conversion. The comparator checks the polarity of the second stage output voltage and then the digital control logic controls the feedback.

Figure 3.22 shows the timing of the ADC. During the coarse conversion, the first stage acts as a gain stage, and so is reset after each step. To prevent shorts during switching, ϕ_1 and ϕ_2 are designed to be non-overlapping. The comparator is triggered by ϕ_{eval} just before the end of ϕ_2 to prevent charge injection from the ϕ_2 switches into the second stage. How these timing signals are generated will be discussed in Section 4.2.1.

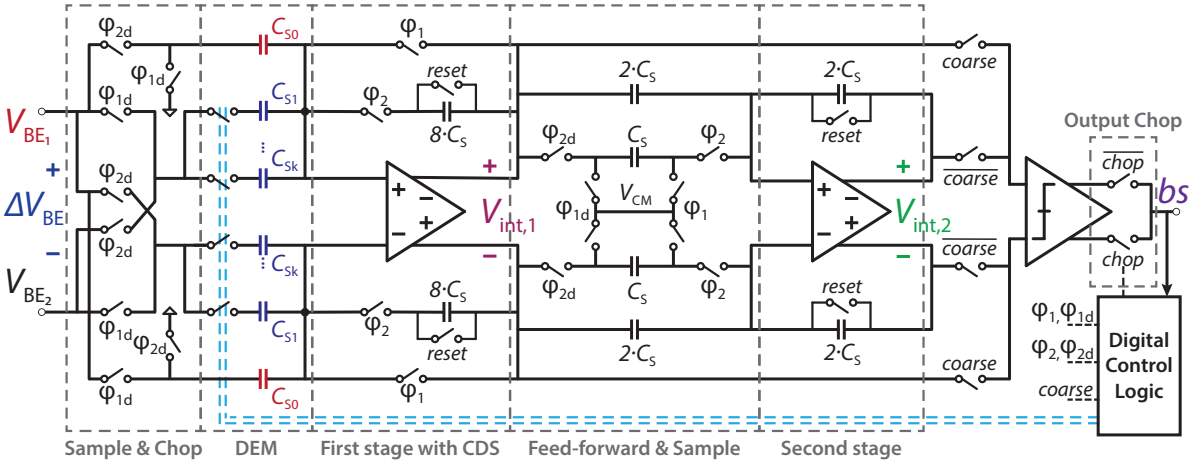

Figure 3.21: Second order feed-forward ADC circuit diagram.

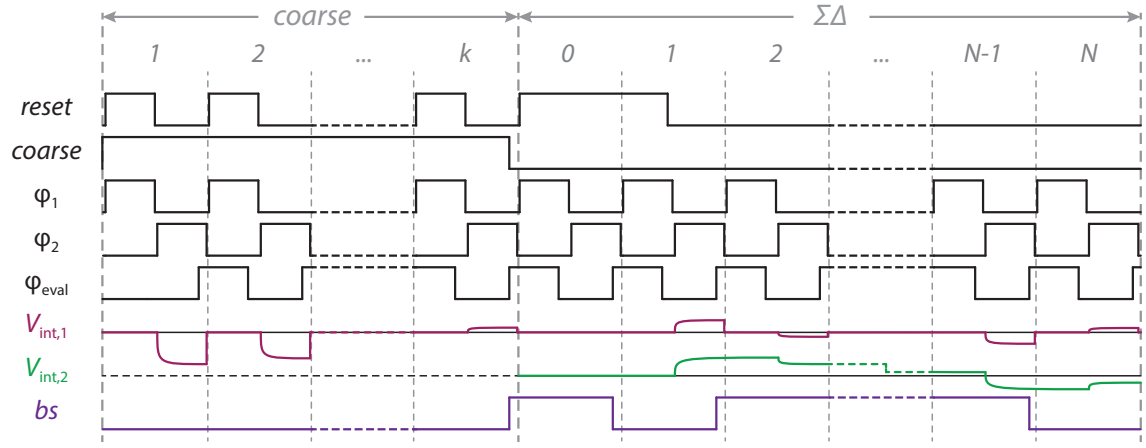

Figure 3.22: Second order feed-forward ADC timing diagram during both the coarse conversion and fine conversion.

4

Implementation

In this Chapter, the implementation of the ADC is discussed. Section 4.1 discusses the design of both OTAs. The digital control circuits of the complete TDC are discussed in Section 4.2. In the next chapter, the simulation results of the complete TDC are presented and discussed.

4.1. Trans-Conductance Amplifier Design

Both OTAs are based on the energy efficient cascoded current re-use OTA of [8] and consume 480 nA and 120 nA respectively from a 1.8 V supply. For OTA_1 (Figure 4.1), only the transistor sizes are changed, while OTA_2 (Figure 4.2) makes use of the cascode biasing of OTA_1. OTA_1 draws only 50 nA of a 1V supply, of which 10 nA is used for biasing the cascodes, and OTA_2 consumes 20 nA.

4.1.1. Common-mode Feedback Circuit

Since the ADC is a discrete time circuit, the common-mode of the OTAs can be controlled by a switched-capacitor common-mode feedback (CMFB) circuit, as shown in Figure 4.3. This CMFB topology has the advantage that it consumes no static power. The sampled charges are equalized in ϕ_2 and the resulting common-mode feedback voltage V_{cmfb} is given by:

$$\frac{V_{\text{out},+} \cdot C_S + V_{\text{out},-} \cdot C_S - V_{\text{cmfb}} \cdot 2C_S}{2C_S} = \frac{V_{\text{cm,ref}} \cdot 2C_S + V_{\text{cb}} \cdot 2C_S}{2C_S} \tag{4.1}$$

$$\Rightarrow \quad V_{\text{cmfb}} \approx V_{\text{out,cm}} - V_{\text{cm,ref}} + V_{\text{cb}} \tag{4.2}$$

.

4.1.2. Gain

The finite gain of an OTA causes leakage and gain errors, as is discussed in [6]. The temperature error due to finite gain can be expressed as [6]:

$$\epsilon_A < \frac{1}{4}[\%/^\circ C] \cdot \Delta T. \tag{4.3}$$

The required open-loop gain $A_{0,1} \cdot A_{0,2}$ is given by:

$$A_{0,1} \cdot A_{0,2} = \frac{a_1 \cdot a_2}{\epsilon_A}\left(\frac{b}{a_1} - \frac{1}{2}\right) \tag{4.4}$$

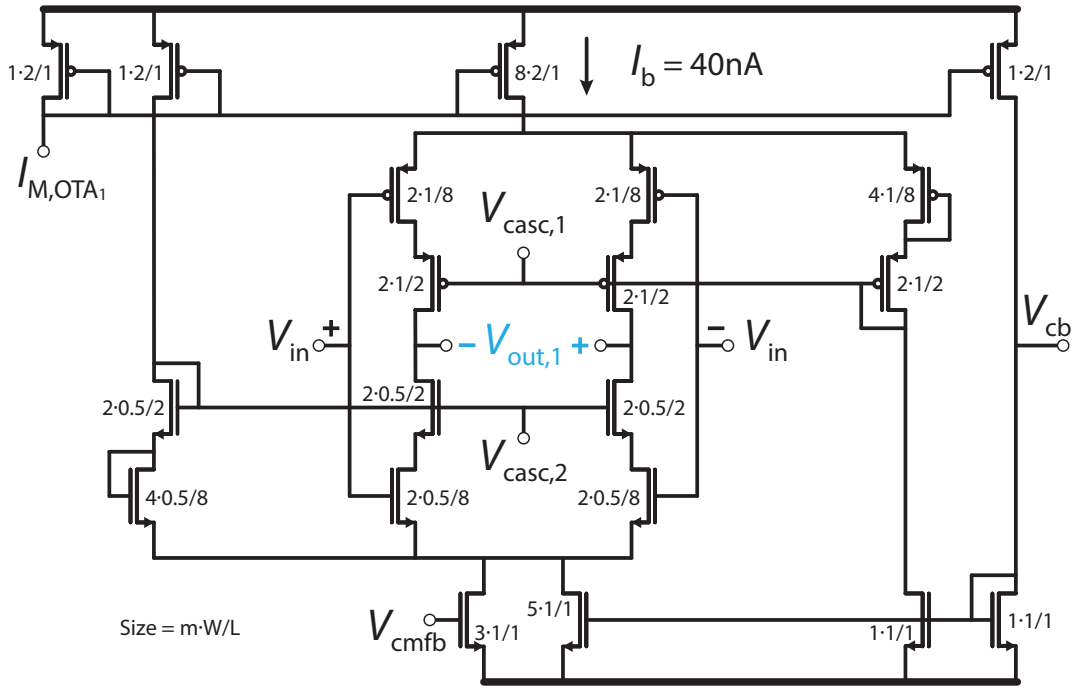

Figure 4.1: Current re-use OTA design based on [8]. Sizes are given as m · W/L and are in μm.

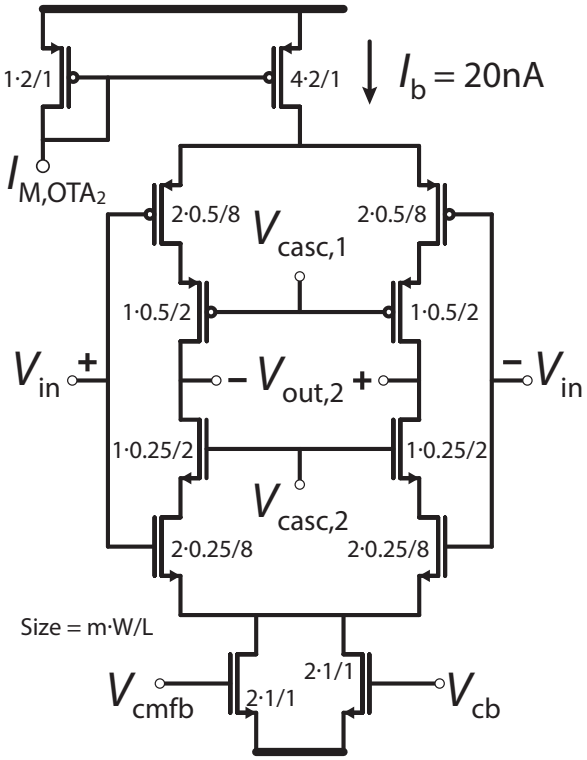

Figure 4.2: Current re-use OTA design based on [8]. Sizes are given as m · W/L and are in μm.

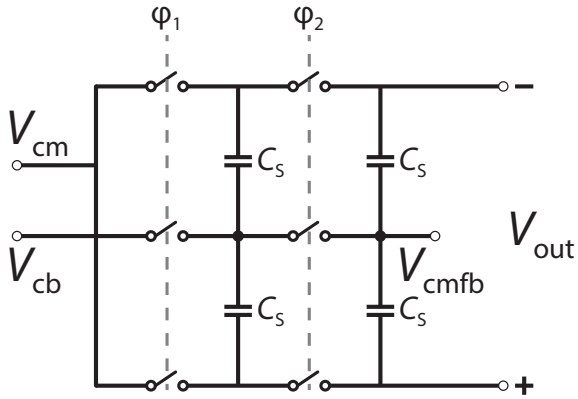

Figure 4.3: Switch capacitor based CMFB circuit that is used in both OTAs to set the common mode voltage.

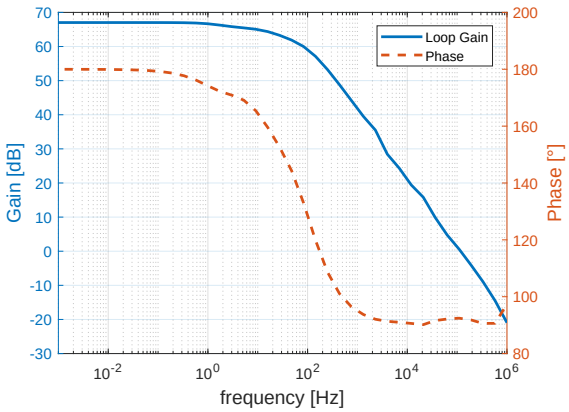

Figure 4.4: Bode plot of OTA_1.

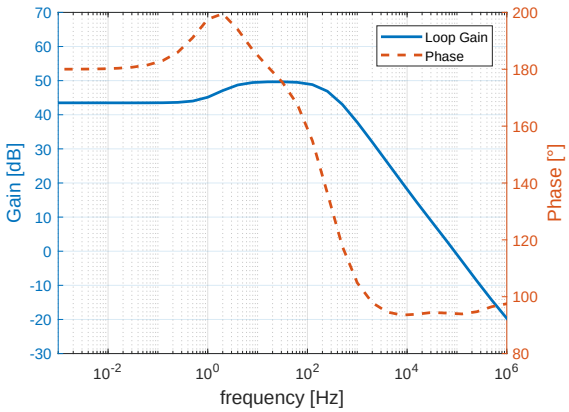

Figure 4.5: Bode plot of OTA_2.

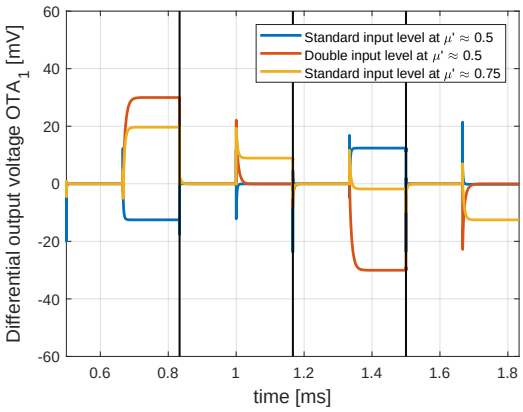

Figure 4.6: Differential output settling of OTA_1 with $f_s = 3$ kHz and feedback factor $a_1 = 1/8$.

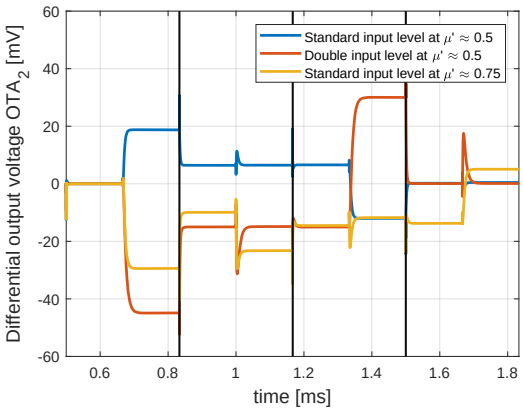

Figure 4.7: Differential output settling of OTA_2 with $f_s = 3$ kHz and feedback factor $a_2 = 1/2$.

with $\Delta T = \pm 0.01$ °C and $a_1 = 1/8$, the required combined gain $A_{0,1} \cdot A_{0,2} = 86$ dB. Figures 4.4 and 4.5 show that $A_{0,1} = 66$ dB and $A_{0,2} = 43$ dB, leading to a total DC gain $A_{0,1} \cdot A_{0,2} = 109$ dB. Using the same formulas, the effective error due to integrator leakage becomes $\Delta T_{\text{eff}} \approx 0.0007$, so the total loop gain is more than sufficient for these errors to be considered insignificant.

4.1.3. Settling

Incomplete settling of V_{out} results in integration errors. As a rule of thumb, the bandwidth of the OTAs should be at least $10 \cdot f_s = 33$ kHz to prevent such errors [6]. As can be seen from Figures 4.4 and 4.5, the bandwidths of OTA_1 and OTA_2 are ~100 kHz and ~50 kHz respectively, which is more than sufficient. The waveform of the output of OTA_1 and OTA_2 are shown in Figures 4.6 and 4.7 respectively, showing that both outputs settle within half a clock period.

4.1.4. Output Swing

A reduced power supply (from 1.8 V to 1 V) limits the output swing of both OTAs. The required output swing depends on the fine range of the ΣΔ-modulator (equation (3.8)) and a_1 or a_2 of the respective integrator. The maximal required swing per integrator is given by:

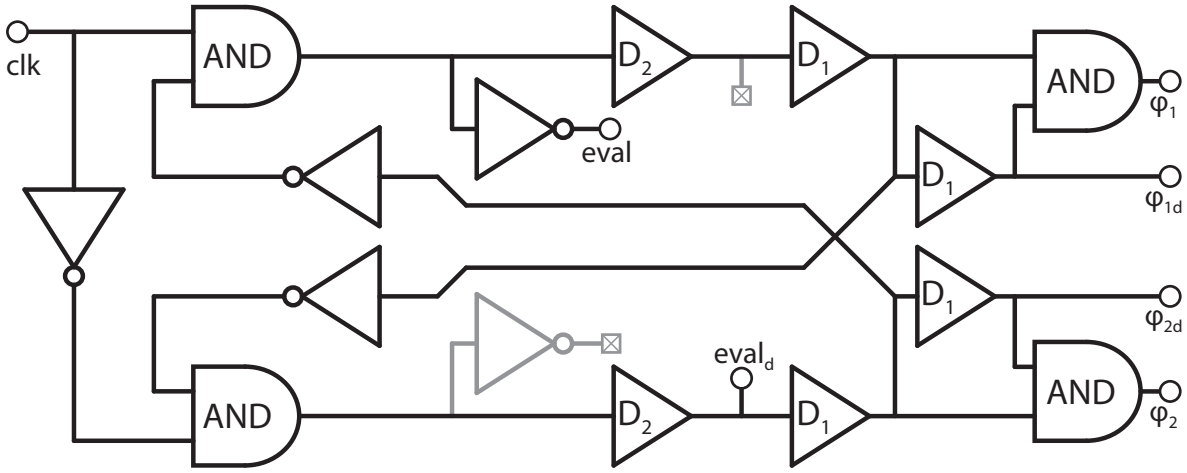

Figure 4.8: Non-overlapping clock generator circuit.

$$V_{\text{out,1,max}} = \frac{2}{a_1} \cdot (2 \cdot \Delta V_{\text{BE}}) \tag{4.5}$$

$$V_{\text{out,2,max}} = 2 \cdot (V_{\text{out,1}} + \frac{1}{a_2} \cdot (V_{\text{out,1}})) \tag{4.6}$$

where $a_1 = 1/8$ and $a_2 = 1/2$. The required output swing is ±15 mV and ±22.5 mV for OTA_1 and OTA_2 respectively. As can be seen from Figures 4.6 and 4.7 both OTAs achieve this swing. A small scaling factor like $a_1 = 1/8$ increases the input referred noise contribution of later stages. However, increasing the factor a_1 causes the integrator to clip.

4.2. Digital Back-end

The digital back-end of the TDC consists two parts; an on-chip part and an off-chip part. The on-chip part consists of a comparator, a clock generator, and a shift register. The off-chip part consists of an FPGA which controls k and decimates the bitstream.

4.2.1. On-chip Digital

The design of the clock generator and the comparator are the most critical part of the on-chip digital because these consume the most power. The comparator uses a dynamic latch based on [25] that consumes an average current of 10 nA.

Non-overlapping Clock Generator

The clock signals of the ΣΔ-modulator are generated from one master clock and, to prevent shorts during switching, are made non-overlapping. The clock circuit is based on a traditional non-overlapping clock generator and is shown in Figure 4.8. All clock outputs are connected to a set of buffers (not shown) to separate the digital power domain from the analog power domain. The greyed-out cells and outputs are to ensure symmetric loading of the circuit.

The delay cells D_1 and D_2 consume the most power. These cells ensure the non-overlap of clock phases by creating a 'dead-zone'. Longer delays also consume more power, and so these delays are kept to the minimal required to ensure non-overlap over process and temperature.

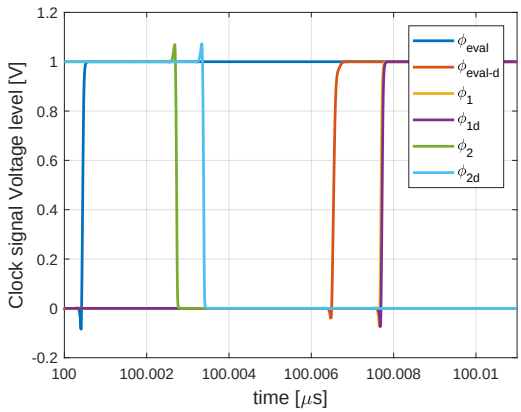

Figure 4.9: Transition of the non-overlapping clock signals from $\phi_2 \Rightarrow \phi_1$.

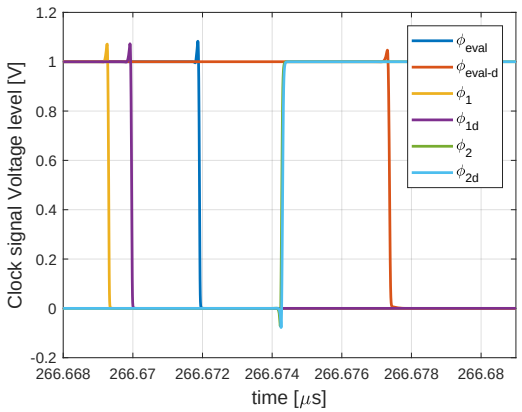

Figure 4.10: Transition of the non-overlapping clock signals from $\phi_1 \Rightarrow \phi_2$.

The crossover points of the resulting waveforms are shown in Figures 4.9 and 4.10 for $\phi_1 \Rightarrow \phi_2$ and $\phi_2 \Rightarrow \phi_1$ respectively. The average power consumption of the clock generator is 15 nW.

Shift Register

Figure 4.11 shows the complete shift register. The data D_{in} and clock signal clk_{SR} at the left drive the TDC Control bits part of the shift register. The next four parts of the shift register are '*BJT DEM and chopping*', '*Cap. sel.* V_{BE}', '*Cap. ratio* V_{ref-}' and '*Cap. ratio* V_{ref+}'. These four parts can be set to extend the shift register or to barrel-shift mode dependent on the external *load* signal, where the selection bits are shifted around for DEM. The MUXs on the clock signals select between ϕ_{eval}, to DEM on every sample, or to clk_{SR} to load new settings. The bitstream selects between '*Cap. ratio* V_{ref-}' and '*Cap. ratio* V_{ref+} containing n and $n+2$ respectrively. All settings are updated in the *Buffer registers* during the dead-zone by ϕ_{eval-d}.

The TDC operates in four main modes: start-up, bias, coarse conversion and fine conversion, and are set by the *start-up*, $bias$ and $coarse$ bits. The $reset$ resets both integrators, $chop$ enables system-level chopping, and *DEM-*C_S*-on* and *DEM-BJT-on* enable the DEM of the sampling capacitors or BJTs respectively. The OTA_1 *Out* and OTA_2 *Out* signals are debugging signals to connect the differential output an OTA to output pads. Because the register only has to be written a few times per conversion, it's power consumption is insignificant.

4.2.2. Off-chip Digital

The off-chip digital is implemented in a FPGA. The FPGA drives the shift register and the clock input of the clock generator. Furthermore, the FPGA samples the output of both the coarse conversion and the fine conversion. The coarse conversion is used to determine n, and the bitstream of the fine conversion is decimated, using a sinc^2 filter, to determine μ''. The temperature is then calculated using:

$$X = n + (1+\gamma)\mu'' \quad \Rightarrow \quad \mu = \frac{\alpha}{(\alpha + X)} \quad \Rightarrow \quad T = A \cdot \mu + B$$

The power required by the FPGA is not uncluded in the overall power consumption.

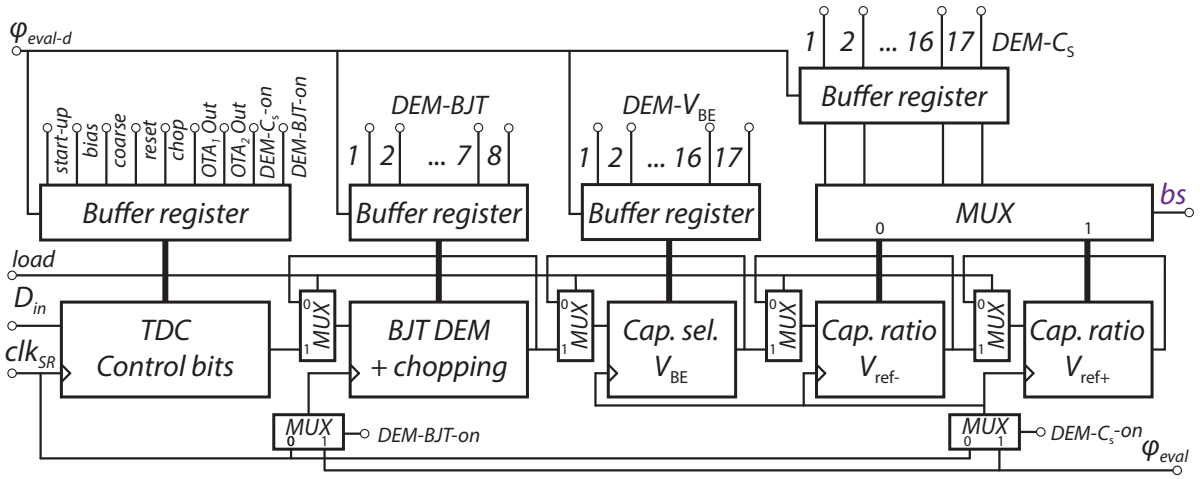

Figure 4.11: Block diagram of the shift register

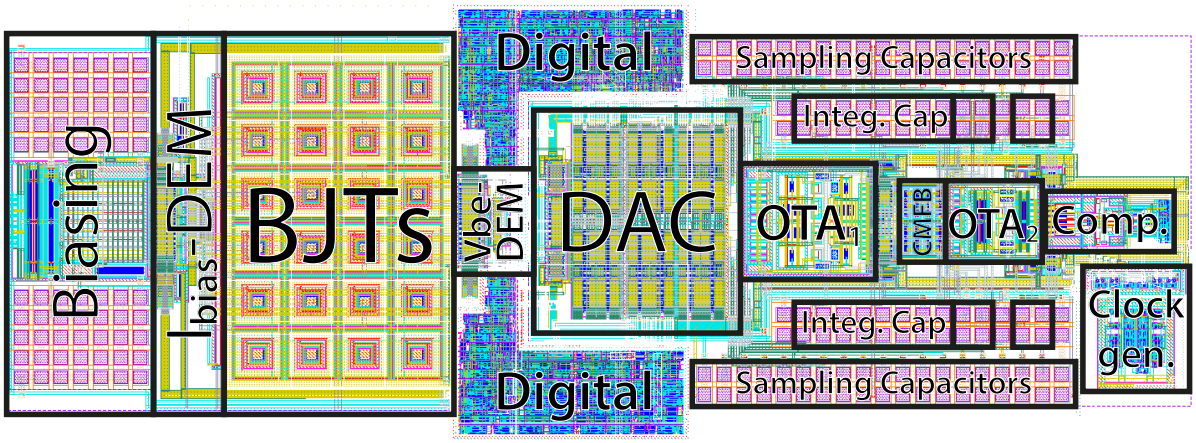

Figure 4.12: TDC layout with labelled blocks.

4.3. TDC Layout

The layout of the TDC is shown in Figure 4.12. It occupies 0.10 mm². Starting from the left, the *Biasing* block contains the high-swing current mirror and the sample and hold circuit. To improve matching, dummies have been placed around both the current mirror and the sampling capacitors, and the current mirror is laid out in an A-B-B-A pattern. Next, the *Switching* block contains the switches controlling the mode of the BJT-core, the I_C-*DEM* switches and the biasing resistor R_B. This is followed by the block of *BJTs*, with dummies. Then, the *Sampling* block contains both the V_{BE}-*DEM* switches and the sampling switches. The large *DAC* block contains the DEM and selector switches for the sampling capacitors. The *Digital* blocks contain the Shift register, split in two for layout purpose. The remaining blocks, except the *Clock gen.* block, make up the ΣΔ-modulator.

From this layout, the various parasitic capacitances and resistances of the entire circuit are extracted, and then used in a top level simulation to determine the expected performance of the TDC.

5

Simulation Results

In this chapter, the simulation results of the TDC are compared with the target specifications (summarized in Table 5.1), starting with the power consumption in Section 5.1. This is followed by the accuracy in Section 5.2 and then by the resolution in Section 5.3. Finally, the results are compared to state of the art sensors in the field of clinical temperature monitoring, as well as general purpose TDCs that cover the industrial temperature range, in Section 5.4.

5.1. Power Consumption

The target for power consumption is set at 100 nW. The TDC consumes a total power of 155 nW, more than the given specifications. However, the 155 nW is still less than 1% of the power consumption of a typical pacemaker control circuit. The power consumed per segment is shown in Figure 5.1. The figure shows that most of the power is consumed by the combined parts of the ADC, which consume 90 nW in total. The OTAs alone consume 65 nW while the clock divider and comparator combined consume another 25 nW. The mirrors used for current biasing consume 12.5 nW, much more than expected. By optimization of some parts, e.g., the current biasing mirrors, the power consumption could be reduced to some extent, as is shown in Section 6.1. However, even then the power consumption does not achieve the given specification, showing that this specification is not feasible in the given technology.

5.1.1. Duty Cycled Power

To reduce its effective power consumption, the TDC can be duty-cycled. At one measurement per second, with a conversion time of the TDC is 100 ms, the effective power consumption

[1]Relative Acc. [%] = 2·Accuracy / T. Range · 100
[2]Res. FOM [pJ°C^2] = Power·t_{conv}·Res.^{2}

Table 5.1: TDC specifications for use in clinical temperature monitoring and for the industrial temperature range.

T. Range [°C]	Power [µW]	Accuracy ($\pm 3\sigma$) [°C]	Relative[1] Acc. [%]	Res. [°C]	t_{conv} [ms]	PSS [°C/V]	Res. FOM[2] [pJ°C^2]	Tech. [µm]
27 to 47	0.1	±0.1	0.5	0.01	100	~ 0.1	1	0.18
-40 to 85	0.1	±0.3	0.24	0.01	100	~ 0.1	1	0.18

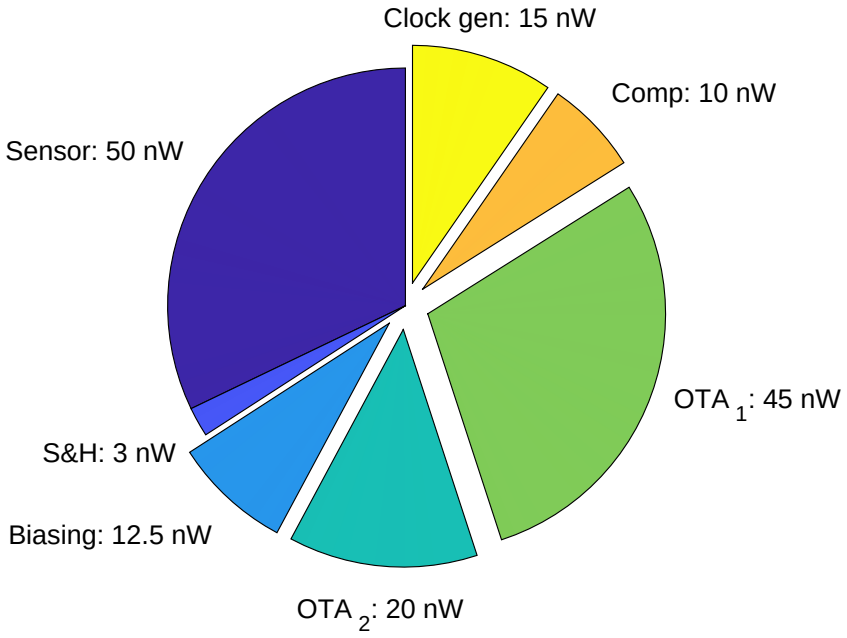

Figure 5.1: Pie chart showing the power consumption distribution of the TDC.

of the sensor can be reduced to 16 nW. The effective power consumption can be reduced even further considering that the TDC's primary purpose is to monitor the heat produced by wireless charging. During the rest of the time the TDC can be either turned off or used sporadically (1 Sa/min) as an internal body temperature monitor. So, while the absolute power consumption doesn't meet the requirements, the TDC is still viable for clinical temperature monitoring by duty cycling the TDC between measurements.

5.2. Accuracy

The body's sensitivity to minute changes in temperature requires measurements to be done with great accuracy: ±0.1 °C between 27 °C and 47 °C, and ±0.3 °C over the industrial temperature range (-40 °C and 85 °C). The parasitic capacitances are extracted from the TDC's layout and used in a transient Monte Carlo simulation of 10 runs at 8 temperature points to determine the accuracy of the TDC. Figure 5.2 plots the measured temperature of which the error is shown in Figure 5.3. As the figure shows, the TDC suffers from a third order systematic error of up to ±0.4 °C.

After using a third order fit to remove the systematic error, the remaining untrimmed inaccuracy is ±0.16 °C (3σ) over both ranges, as is plotted in Figure 5.4. After a 1-point trim at 37 °C, as is shown in Figure 5.5, the accuracy improves to ±0.1 °C over the industrial temperature range, and to ±0.03 °C between 27 °C and 47 °C.

These results are not statistically significant, which becomes apparent when compared to the expected spread of ±0.2 °C (3σ) based on the simulations of the BJT core, shown in Figures 5.6 and 5.7. However, the results show that the accuracy is mainly determined by the BJTs

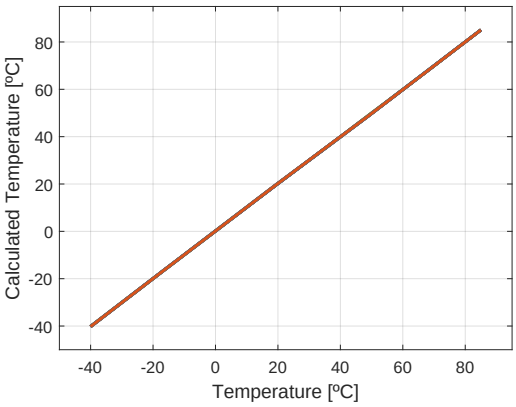

Figure 5.2: Calculated temperature from the Monte Carlo simulation over the actual temperature.

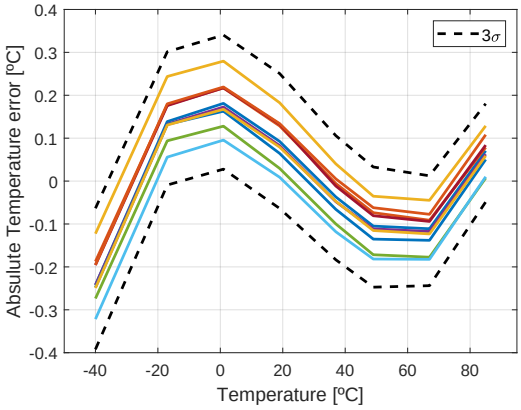

Figure 5.3: Absolute temperature error of the Monte Carlo simulation over the actual temperature.

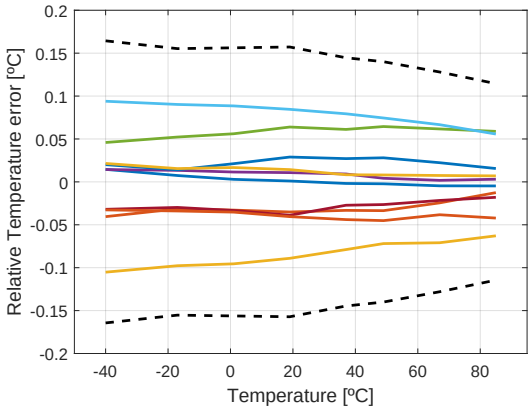

Figure 5.4: Untrimmed inaccuracy results of the TDC over temperature for a 10-points Monte Carlo simulation at 8 temperatures.

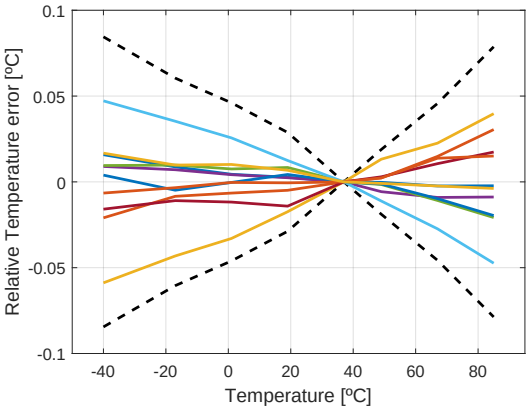

Figure 5.5: Trimmed inaccuracy results of the TDC over temperature for a 10-points Monte Carlo simulation at 8 temperatures.

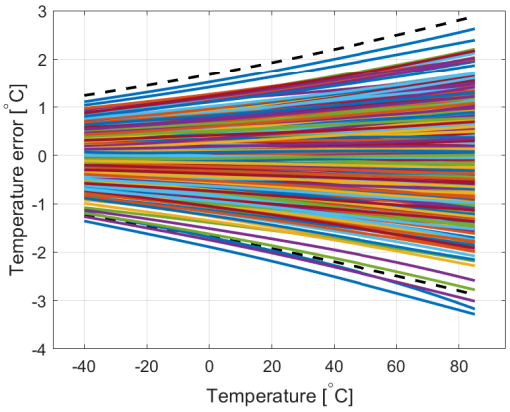

Figure 5.6: Untrimmed accuracy of the BJT frontend from a 200-point Monte Carlo simulation.

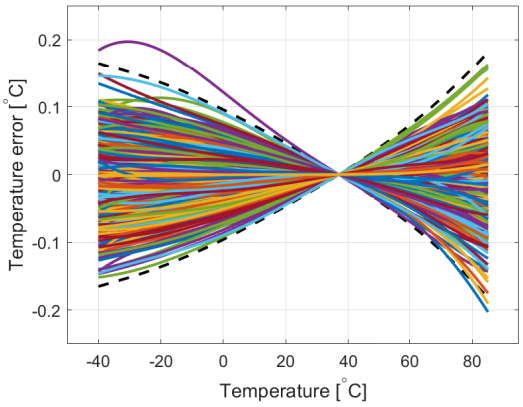

Figure 5.7: PTAT trimmed accuracy of the BJT frontend from a 200-point Monte Carlo simulation.

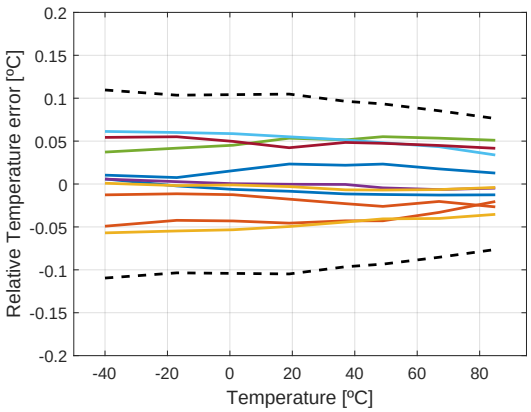

Figure 5.8: Untrimmed inaccuracy results of the TDC over temperature for a 10-points Monte Carlo simulation at 8 temperatures with DEM.

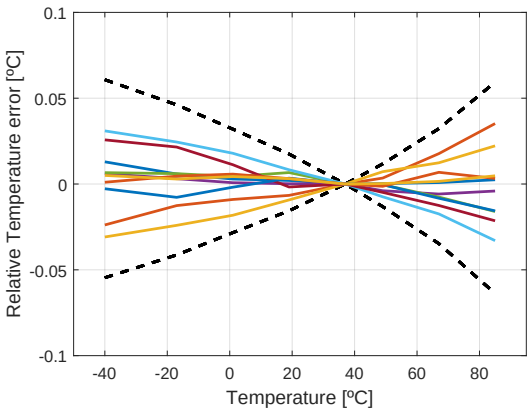

Figure 5.9: Trimmed inaccuracy results of the TDC over temperature for a 10-points Monte Carlo simulation at 8 temperatures with DEM.

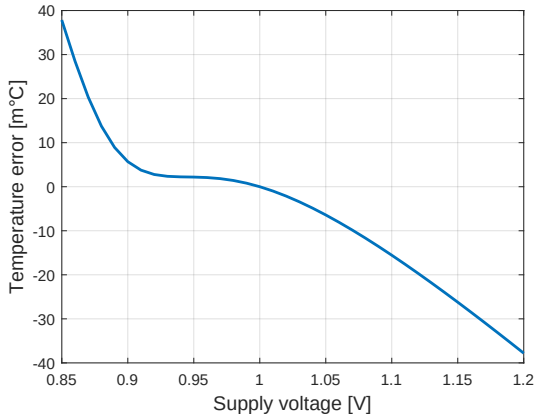

Figure 5.10: Sensitivity of the temperature measurement to variations in the power supply.

5.2.1. Dynamic Element Matching

DEM is used to improve the accuracy of the TDC and the results are shown in Figures 5.8 and 5.9. The same Monte Carlo seed as for the accuracy measurement was used. As can be seen from the figures, by using DEM, the untrimmed accuracy improves from ±0.17 °C to ±0.11 °C while the trimmed accuracy improves from ±0.085 °C to ±0.06 °C over the industrial temperature range. However, as the data is not statistically significant it is difficult to draw any final conclusion of the effectiveness of DEM.

5.2.2. Power Supply Sensitivity

To reduce the power consumption as much as possible, the power supply was reduced to 1 V, as was shown in Chapter 2.4. However, this makes the circuit more sensitive to variations in the power supply. In Figure 5.10 the simulated PSS of the TDC is shown to be 0.15 [°C/V] from 0.85 V to 1.2 V. Only between 0.9 V and 1.05 V, the PSS ≤ 0.1 [°C/V], and the TDC is not significantly influenced by variations in the power supply.

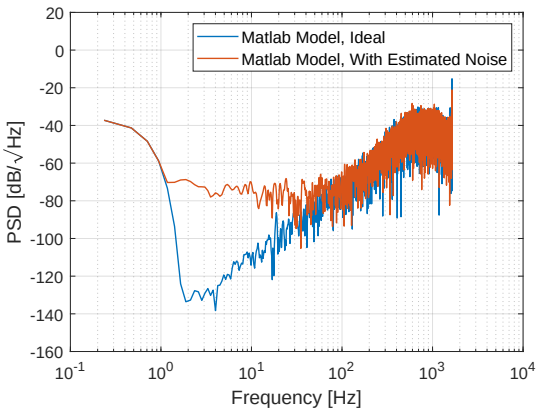

Figure 5.11: FFT of a MATLAB model simulation generated output bitstream.

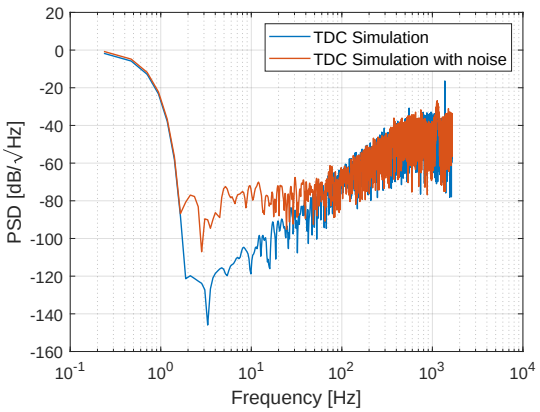

Figure 5.12: FFT of a TDC generated output bitstream over 6 seconds.

5.3. Resolution

A Matlab model of the 2nd order ΣΔ-modulator has been used to check the noise shaping of the ΣΔ-modulator and to determine the design parameters to achieve a thermal noise limited resolution of 0.01 °C. The FFT result of both the quantisation and thermal noise limited model simulations are plotted in Figure 5.11.

A transient noise simulation over 6 seconds of the finished TDC is performed to ensure that it is indeed thermal noise limited, and the noise limit is similar to the estimated thermal noise. The result of this simulation is plotted in Figure 5.12. As can be seen from the two figures, the ΣΔ-modulator indeed shapes the noise as intended and the thermal noise limit of the TDC is as expected.

5.4. Benchmarking

The discussed results show that the TDC is well suited to be used in clinical temperature monitoring. These results are summarized in Table 5.2 and compared to the current state of the art.

The proposed design is shown to be the second lowest in terms of absolute power, only beaten by [26], which is an all CMOS design. It uses bulk-connected PMOS devices as sensing elements and pays for it in accuracy and resolution. In terms of resolution FOM and relative accuracy, the proposed design achieves similar results as [17] but beats it on power consumption. It does zo by trading resolution, as 0.01°C is sufficient for clinical temperature monitoring. Over the industrial temperature range the design can keep up with the state of the art on all aspects. However, it must be noted that the results in this design are simulation results and not measurement results. The measured performance is expected to be somewhat worse.

[3]Relative Acc. = 2·Accuracy / T. Range · 100
[4]Res. FOM = Power·t_{conv}·(Res.)^2
[5]Peak-to-peak inaccuracy
[6]Including glucose sensor
[7]Estimated from paper

Table 5.2: Comparison table with the state of the art in both clinical temperature monitoring and industrial temperature range TDCs.

Item	T. Range [°C]	Power [µW]	Accuracy (3σ) [°C]	Relative[3] Acc. [%]	Res. [°C]	t_{conv} [ms]	Res. FOM[4] [pJ°C^2]	PSS [°C/V]	Calib. [# pts]	Tech. [µm]	Year
This work	**27 - 47**	**0.155**	**±0.05**	**0.5**	**0.01**	**100**	**1.55**	**0.15**	**1**	**0.18**	**2019**
	-40 - 85	**0.155**	**±0.2**	**0.32**	**0.01**	**100**	**1.55**	**0.15**	**1**	**0.18**	**2019**
[16]	25 - 45	1.1	±0.2	2	0.01	500	55	N/A	1	0.18	2016
[17]	20 - 50	16	±0.1	0.666	0.001	100	1.6	N/A	1	0.18	2016
[18]	20 - 50	2.205	-0.5/+0.25[5]	2.5	0.125	20	689	N/A	1	0.35	2018
[19]	20 - 50	3[6]	±0.15	1	0.05	51.2[7]	400[7]	N/A	1	0.13	2019
[26]	-20 - 80	0.011	-0.9/+1.2[5]	2.4	0.145	839	190	3.8	2	0.18	2019
[27]	-45 - 130	200	±0.3	0.34	0.003	1.8	3.2	0.1	1	0.7	2017
[28]	0 - 100	11.0	±0.2	0.4	0.01	3.4	3.8	N/A	1	0.18	2018
[8]	-55 - 125	8.3	±0.06	0.07	0.015	5	7.8	0.01	1	0.16	2017
[29]	-20 - 100	0.075	±0.21	0.34	0.073	8	3.2	0.13	2	0.18	2017

6

Conclusion

An ultra-low temperature to digital converter for clinical temperature monitoring has been proposed. Simulation results show that it achieves excellent performance: ±0.05 °C inaccuracy, from 27 °C to 47 °C. It also achieves good performance over the industrial temperature range. Regrettably, it was not possible to achieve the specified 100 nW power consumption, but the design still manages to achieve a respectable 155 nW, which is less than 1% of the power consumption of a typical pacemaker control circuit. Furthermore, it achieves the lowest resolution FOM compared to other TDCs designed for clinical temperature monitoring.

6.1. Future Work

There are three parts of the sensor whose power consumption can be lowered. First of all, an emitter area ratio can be replaced by a current ratio to create the current density ratio r. This would potentially reduce the power of the sensor from 53 nA to ~31 nA. Although using an emitter area ratio is slightly more energy efficient, the goal of this design is to reduce the absolute power of the sensor. A new topology is shown in Figure 6.1. Care must be taken that the voltages V_{BE_1} and V_{BE_2} sampled by the DAC capacitors still settle accurately within one clock phase.

Second, the power consumed by the distribution of the current biasing was an oversight in the design so far, and can be significantly reduced. It is possible to reduce the power consumption of this part from 12.5 nW to 5 nW or less by reducing the mirroring ratio, as is shown in Figure 6.2. To ensure matching, the length of the current mirrors could be increasing.

Third, the ΣΔ-modulator can be made a first order modulator which would save the power of OTA_2. To remain thermal noise limited, the size of C_S can be reduced, while N is increased, both by a factor of about 2.5 to keep their product the same. The reduction of C_S will allow for a higher sampling frequency, keeping the conversion time about the same. To maintain sufficient loop gain, the gain of OTA_1 should be increased from 66 dB to 74 dB [6], which might consume some additional power in OTA_1, but will save the 20 nW from OTA_2.

These three changes combined would improve the power consumption of the design to roughly 110 nW, just 10% off target.

Another approach can be to replace the BJT-core with a DT-MOS based design. As was shown in [7], a DT-MOS design allows for both low current and power supply voltage to be used but comes at the cost of worse accuracy (factor ~2x).

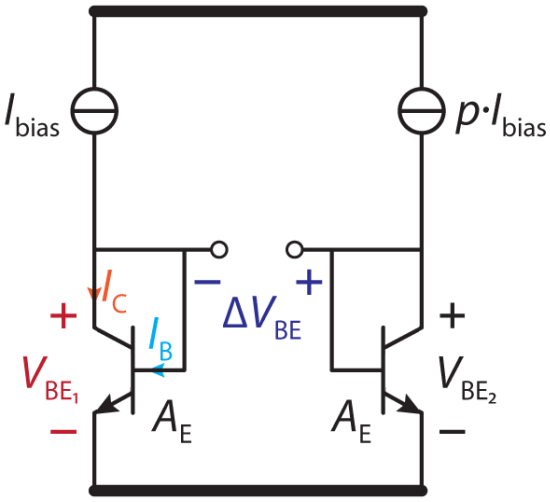

Figure 6.1: A current ratio based design of the BJT-core

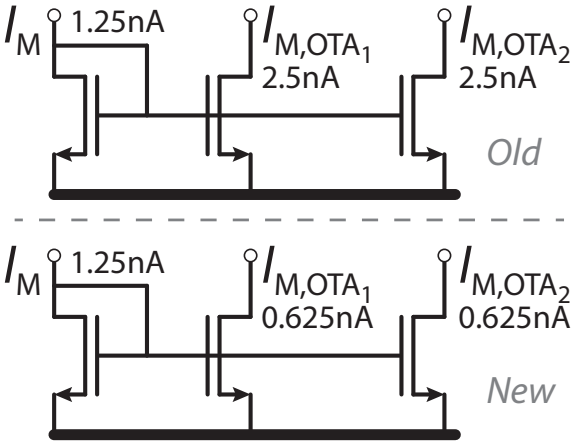

Figure 6.2: Improvement to the power consumed by the mirrors used for current biasing.

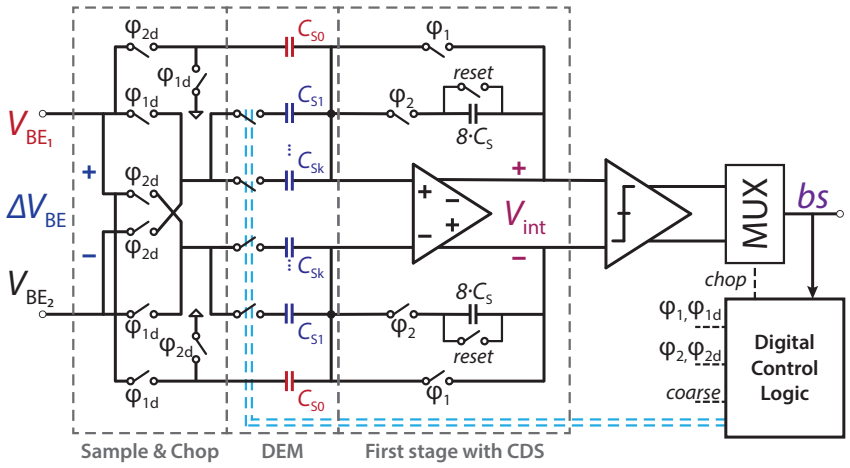

Figure 6.3: First order ΣΔ-modulator design to reduce power consumption.

A

TDC Thermal-Noise Limited Resolution Calculation

In the complete TDC the resolution is designed to be thermal noise limited. To obtain this, first a function of the resolution has to be derived based on the thermal noise. As can be seen from equation A.1 the thermal noise forms an additional term in the charge transfer

$$Q_{\text{acc}} = N\left[(Q_{V_{\text{BE}}} - (n-1)Q_{\Delta V_{\text{BE}}})(1-\mu') + (Q_{V_{\text{BE}}} - (n+1)Q_{\Delta V_{\text{BE}}})\mu'\right] + q_{n,acc} \tag{A.1}$$

where N is the number of cycles of the ΣΔ-modulator. As $X = n + \mu'$, this equation can be reduced to

$$Q_{\text{acc}} = N(Q_{V_{\text{BE}}} - XQ_{\Delta V_{\text{BE}}}) + q_{n,acc} \tag{A.2}$$

Solving equation A.2 for X gives

$$X = \frac{Q_{V_{\text{BE}}}}{Q_{\Delta V_{\text{BE}}}} + \frac{q_{n,acc}}{N \cdot Q_{\Delta V_{\text{BE}}}} \tag{A.3}$$

The total noise acquired during a full conversion of the ΣΔ-modulator can be described as the quadratic sum of the noise on V_{BE} and X times ΔV_{BE}, times the number of sample N

$$q^2_{n,acc} = N(q^2_{n,V_{\text{BE}}} + X \cdot q^2_{n,\Delta V_{\text{BE}}}) \tag{A.4}$$

Substituting this in the noise dependent part of equation A.3 a function for the deviation σ_X of X can be found as follows

$$\sigma_X = \frac{\sqrt{N(q^2_{n,V_{BE}} + X \cdot q^2_{n,\Delta V_{BE}})}}{N \cdot Q_{\Delta V_{BE}}} \tag{A.5}$$

$$= \frac{1}{Q_{\Delta V_{BE}}} \cdot \sqrt{\frac{q^2_{n,V_{BE}} + X \cdot q_{n,}\Delta V^2_{BE}}{N}} \tag{A.6}$$

$$\approx \frac{q_{n,}\Delta V_{BE}}{Q_{\Delta V_{BE}}} \cdot \frac{X}{N} \tag{A.7}$$

$$= \frac{1}{\Delta V_{BE}} \sqrt{\frac{(1+\rho) k_B T X}{N C_S}} \tag{A.8}$$

Now that σ_X has been determined, a function for σ_T can be found by using $\mu = \alpha/(\alpha + X)$ and $T = A \cdot \mu + B$

$$\sigma_T = A \cdot \frac{\alpha}{(\alpha + X)^2} \cdot \frac{1}{\Delta V_{BE}} \cdot \sqrt{\frac{(1+\rho) \cdot k_B T X}{N C_S}} \tag{A.9}$$

$$= \frac{A \cdot \alpha \cdot \Delta V_{BE}}{V^2_{REF}} \sqrt{\frac{(1+\rho) \cdot k_B T X}{N \cdot C_S}} \tag{A.10}$$

$$\approx \frac{A \cdot \alpha \cdot \Delta V_{BE}}{V^2_{REF}} \sqrt{\frac{(7/3) \cdot k_B T X}{N \cdot C_S}} \tag{A.11}$$

This shows that the resolution (σ_T) increases with X and decreases with N and C_S. The estimation of $\rho = 4/3$ is based on [24].

List of Terms

ADC analog to digital converter.

Bipolar Junction Transistor A bipolar junction transistor uses two junctions between two semiconductor types, n-type and p-type and is a type of transistor that uses both electron and hole charge carriers.

BJT Bipolar Junction Transistor.

cascoded A cascode is used to improve the performance of an analog circuit by either improving the input–output isolation or the high output impedance, or increasing the input impedance or the bandwidth.

CDS correlated double sampling.

chopping The switching of both input and output polarity of a system to get rid of a structural offset, or low frequency noise, by transferring the signal to a higher frequency and filtering the rest..

CMFB common-mode feedback.

CMOS complementary metal-oxide-semiconductor.

CTAT complementary to absolute temperature.

current mirror A current mirror is designed to copy a current from one transistor to another by forcing a current dependent voltage accross the primary transistor and then use that voltage to control the current in the secondary transistor..

DAC digital to analog converter.

DEM dynamic element matching.

ENOB effective number of bits.

FFT Fast Fourier Transformation.

FPGA Field Programmable Gate Array.

FPGA A field-programmable gate array Field Programmable Gate Array (FPGA) is an integrated circuit designed to be configured by a customer or a designer after manufacturing..

industrial temperature range The industrial temperature range is from -40°C to 85°C.

Metal-Insulator-Metal Capacitor A capacitor that is made from metal sheats of two consecutive metal layers with a (doped) insulator in between..

Metal-oxide-semiconductor field-effect transistor A metal-oxide-semiconductor field-effect transistor is a type of transistor that changes conductivity with the amount of applied voltage. It has an insulated gate (metal) on top of a doped silicon channel (semiconductor) with an oxide in the middel.

military temperature range The military temperature range is from -55°C to 125°C.

MIM Metal-Insulator-Metal.

mismatch Every IC process is susceptible to variation. Process variation is stochastic in nature and only introduced during the production process because of gradients in doping levels across the chip as well as deviations in the lithography. As these variations degrade the matching of circuit components its effects are often referred to as mismatch..

MOSFET metal-oxide-semiconductor field-effect transistor.

NMOS N-type metal-oxide-semiconductor.

operational trans-conductance amplifier Something about OTAs.

OTA operational trans-conductance amplifier.

PMOS P-type metal-oxide-semiconductor.

PSS power supply sensitivity.

PTAT proportional to absolute temperature.

SAR successive approximation register.

TD Thermal-Diffusivity.

TDC temperature to digital converter.

Thermal noise limited In ADCs differentiation is made between quantisation noise and thermal noise. Quantisation noise comes from the discrete interval of the digital signal while thermal noise is a form of white noise that is temperature dependent. As quantisation noise is easier to reduce than thermal noise, ADCs are usually designed to be thermal noise limited..

thermistor A resistor who's resistive value depends on temperature. They can have either a positive or negative temperature dependency..

thermistor temperature dependent resistor.

TSMC Taiwan Semiconductor Manufacturing Company.

Bibliography

[1] T. Campi, S. Cruciani, F. Palandrani, V. De Santis, A. Hirata, and M. Feliziani, *Wireless power transfer charging system for AIMDs and pacemakers,* IEEE transactions on microwave theory and techniques **64**, 633 (2016).

[2] S. Kang and M. Snyder, *Overview of Pacemakers and Implantable Cardioverter Defibrillators (ICDs),* https://www.urmc.rochester.edu/encyclopedia/content.aspx?contenttypeid=85&contentid=p00234, (Accessed: 24-September-2018).

[3] K. A. A. Makinwa, *Smart Temperature Sensor Survey,* (2018), (Accessed: 2018-05-26).

[4] K. Souri, Y. Chae, K. Makinwa, *et al.*, *A CMOS temperature sensor with a voltage-calibrated inaccuracy of 0.15° C (3σ) from -55° C to 125° C,* IEEE Journal of Solid-State Circuits **48**, 292 (2013).

[5] V. Ivanov, R. Brederlow, and J. Gerber, *An Ultra Low Power Bandgap Operational at Supply from 0.75 V,* IEEE Journal of Solid-State Circuits **47**, 1515 (2012).

[6] M. A. Pertijs and J. Huijsing, *Precision Temperature Sensors in CMOS Technology* (Springer Science & Business Media, 2006).

[7] K. Souri and K. A. Makinwa, *Energy-Efficient Smart Temperature Sensors in CMOS Technology* (Springer, 2017).

[8] B. Yousefzadeh, S. H. Shalmany, and K. A. A. Makinwa, *A BJT-Based Temperature-to-Digital Converter With ±60 mK (3 σ) Inaccuracy From −55 °C to +125 °C in 0.16-µm CMOS,* IEEE Journal of Solid-State Circuits **52**, 1044 (2017).

[9] R. K. Shepard and K. A. Ellenbogen, *Leads and longevity: How long will your pacemaker last?* EP Europace **11**, 142 (2009).

[10] V. S. Mallela, V. Ilankumaran, and N. S. Rao, *Trends in Cardiac Pacemaker Batteries,* Indian Pacing and Electrophysiology Journal **4.4**, 201–212 (2004).

[11] D. Birnie, K. Williams, A. Guo, L. Mielniczuk, D. Davis, R. Lemery, M. Green, M. Gollob, and A. Tang, *Reasons for Escalating Pacemaker Implants,* The American Journal of Cardiology **98**, 93 (2006).

[12] A. Nixdorf-Miller, D. M. Hunsaker, and J. C. Hunsaker III, *Hypothermia and hyperthermia medicolegal investigation of morbidity and mortality from exposure to environmental temperature extremes,* Archives of pathology & laboratory medicine **130**, 1297 (2006).

[13] E. F. J. Ring, H. Mcevoy, A. Jung, J. Zuber, and G. Machin, *New standards for devices used for the measurement of human body temperature,* Journal of Medical Engineering & Technology **34**, 249 (2010).

[14] M. A. P. Pertijs, K. A. A. Makinwa, and J. H. Huijsing, *A CMOS Smart Temperature Sensor With a 3σInaccuracy of ±0.1° C from -55° C to 125° C,* Solid-State Circuits, IEEE Journal of **40**, 2805 (2005).

[15] M. A. P. Pertijs, A. L. Aita, K. A. A. Makinwa, and J. H. Huijsing, *Voltage calibration of smart temperature sensors,* in *SENSORS, 2008 IEEE* (2008) pp. 756–759.

[16] M. Law, S. Lu, T. Wu, A. Bermak, P. Mak, and R. P. Martins, *A 1.1μWCMOS Smart Temperature Sensor With an Inaccuracy of ±0.2 °C (3σ)for Clinical Temperature Monitoring,* IEEE Sensors Journal **16**, 2272 (2016).

[17] C. Deng, Y. Sheng, S. Wang, W. Hu, S. Diao, and D. Qian, *A CMOS Smart Temperature Sensor With Single-Point Calibration Method for Clinical Use,* IEEE Transactions on Circuits and Systems II: Express Briefs **63**, 136 (2016).

[18] Z. Zheng, M. Chen, J. Zhou, and G. Wang, *A CMOS Temperature Sensor With Single-Point Calibration for Retinal Prosthesis,* in *2018 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)* (IEEE, 2018) pp. 147–150.

[19] X. Chen, L. Li, X. Tan, N. Yan, J. Wang, and L.-R. Zheng, *A Temperature Sensor with Glucose Sensor Interface Based on Configurable Incremental Sigma Delta ADC,* IEICE Electronics Express , 16 (2019).

[20] D. D Toraskar, M. Mattada, and H. Guhilot, *Comparison between Voltage Domain and Time Domain ADCs-A Review,* **5** (2016), 10.17148/IJARCCE.2016.55142.

[21] D. S. Moran and L. Mendal, *Core Temperature Measurement,* Sports Medicine **32**, 879 (2002).

[22] E. Sackinger and W. Guggenbuhl, *A High-swing, High-impedance MOS Cascode Circuit,* IEEE Journal of Solid-State Circuits **25**, 289 (1990).

[23] J. Markus, J. Silva, and G. C. Temes, *Theory and Applications of Incremental ΔΣ Converters,* IEEE Transactions on Circuits and Systems I: Regular Papers **51**, 678 (2004).

[24] R. Schreier, J. Silva, J. Steensgaard, and G. C. Temes, *Design-oriented estimation of thermal noise in switched-capacitor circuits,* IEEE Transactions on Circuits and Systems I: Regular Papers **52**, 2358 (2005).

[25] L. Xu, J. H. Huijsing, and K. A. A. Makinwa, *A 10khz-bw 93.7db-snr chopped ΔΣ adc with 30v input cm range and 115db cmrr at 10khz,* in *2017 IEEE Asian Solid-State Circuits Conference (A-SSCC)* (2017) pp. 49–52.

[26] T. Someya, A. M. Islam, T. Sakurai, and M. Takamiya, *An 11-nW CMOS Temperature-to-Digital Converter Utilizing Sub-Threshold Current at Sub-Thermal Drain Voltage,* IEEE Journal of Solid-State Circuits (2019).

[27] G. Wang, A. Heidari, K. A. Makinwa, and G. C. Meijer, *An accurate bjt-based cmos temperature sensor with duty-cycle-modulated output,* IEEE Transactions on Industrial Electronics **64**, 1572 (2017).

[28] R. Wei and X. Bao, *A Low Power Energy-Efficient Precision CMOS Temperature Sensor,* Micromachines **9**, 257 (2018).

[29] K. Yang, Q. Dong, W. Jung, Y. Zhang, M. Choi, D. Blaauw, and D. Sylvester, *9.2 a 0.6 nj-0.22/+ 0.19° c inaccuracy temperature sensor using exponential subthreshold oscillation dependence,* in *2017 IEEE International Solid-State Circuits Conference (ISSCC)* (IEEE, 2017) pp. 160–161.