# Single Grain Si TFTs and Circuits based on the μ-Czochralski Process

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*To my parents and love*

# Contents

# Chapter 1

# Introduction

*This chapter provides an overview of the latest developments in silicon (Si) based thin-film transistors (TFTs). Various issues related to polycrystalline Si technology are discussed. Using the* μ*-Czochralski process in excimer laser crystallization offers a precise control of the location of grains in two dimensions (2D). It provides an effective way to eliminate grain boundaries (GBs) from the TFT channel and thus to fabricate TFTs inside single grains (SG TFTs). Finally, the goal and content of this thesis are presented.*

## 1.1 Historical Overview

The concept of thin-film transistors (TFTs) was introduced by P. K. Weimer in *IRE Transactions on Electron Devices* in 1961 [1]. Ten years later Brody et al. constructed the first active matrix liquid crystal display (AMLCD) using TFTs as switching elements [2]. TFTs made from various semiconductor materials, e.g. CdSe, InSb, and Ge, were investigated only in the early 1980s. Meanwhile, despite some successful demonstrations of CdSe TFT-LCDs, the progress of industrial applications remained slow until possibilities for doping amorphous silicon (a-Si) by the glow discharge technique were reported. Spear and LeComber fabricated the first a-Si TFT in 1979 [3]. Their results stimulated research and development activities on a-Si TFTs.

Mass production of large-area a-Si TFT-LCDs began in the late 1980s [4]. The majority of AMLCDs were produced with a-Si TFTs rather than polycrystalline silicon (poly-Si) TFT-LCDs, which were used only in a small segment of the TFT-LCD industry. This was because at that time only high-

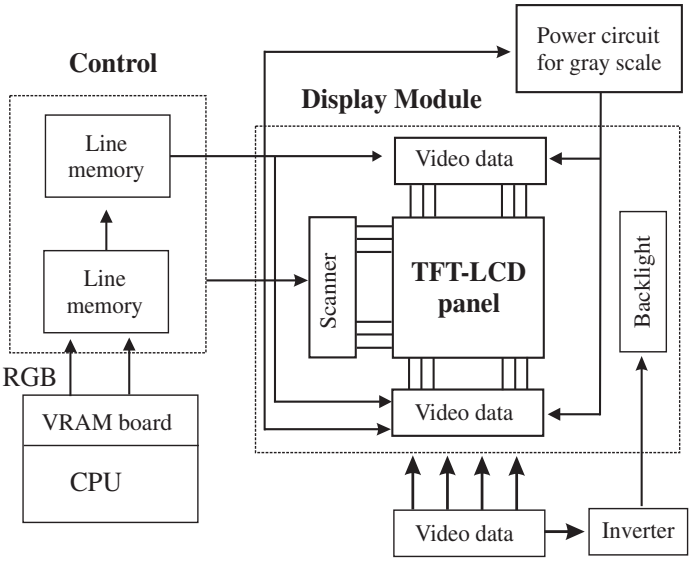


Figure 1.1: Schematic view of a poly-Si TFT-LCD panel that integrates peripheral circuitry.

temperature poly-Si TFTs were available. Nowadays there is an ever growing demand of TFT-LCDs for flat panel displays (FPDs) in many fields – such as office automation equipment, consumer electronics, mobile phones, digital cameras, camcorders, personal digital assistants (PDAs), game machines, PC monitors, TVs, automobile panels, health monitoring systems, and military systems.

A recent development in poly-Si TFT technology has breathed new life into many non-LCD applications, where transistors are required to enhance specific functions or to stabilize the operation of the device. Figure 1.1 shows a schematic diagram of a TFT-LCD panel integrated with controller, power supply, and driver circuits. If the performance of TFTs is improved and approaches that of silicon-on-insulator (SOI) TFTs at low temperature ($<$ 350°C), it will be feasible to integrate the complete system on glass. Three-dimensional (3D) integrated circuits (ICs) provide a possible future application for such high performance TFTs. Other major applications are DRAMs, EEPROMs, TFT contact imagers, and fingerprint sensors [5].

## 1.2 Issues in Poly-Si TFT Technology

Silicon TFTs are typically composed of a-Si, which can be deposited in various sequences. The material, mechanical, and chemical properties of the film can affect electrical characteristics of the TFT. A-Si TFT-LCDs have become the standard for the mass production of AMLCDs. Although the production lines are well established and costs are relatively low, a-Si TFT technology has some serious drawbacks. The most important is the low carrier mobility (1 $cm^2/Vs$), i.e., the speed at which carriers can move through each transistor [6]. Another disadvantage of this technology is the instability of the TFTs. Poly-Si TFTs offer significantly higher carrier (electron and hole) mobilities and better stability than a-Si TFTs. Higher carrier mobility may open the way for several improvements: (a) Reduced device dimensions, allowing for higher aperture ratio, increased brightness and reduced power consumption; (b) Higher pixel driving TFT on-current, resulting in a reduced sensitivity to RC delay time and a large reduction in pixel charging time; (c) Monolithic integration of CMOS drivers and other circuit elements, enabling reduced thickness and weight, higher reliability, and lower cost. Using poly-Si TFT rather than a-Si TFT technology in AMLCDs facilitates meeting the standards for high quality displays.

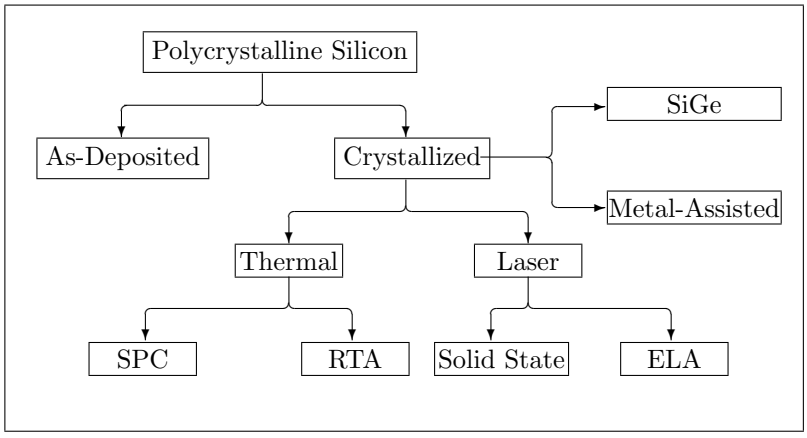


Figure 1.2: Poly-Si film formation techniques.

In general, there are two fundamental ways to produce the poly-Si films [7]:

(1) High-temperature deposition of the Si film directly in the polycrystalline phase, referred to as *as-deposited poly-Si*; and (2) Phase transformation to polycrystalline, referred to as *crystallized poly-Si*, by means of a crystallization step, during which energy in some form (thermal energy, phonon energy) is supplied to the as-deposited Si film to accomplish the phase transformation. Figure 1.2 illustrates the different approaches of producing poly-Si films [8].

**High-Temperature Poly-Si Films**

Poly-Si films are deposited directly in the polycrystalline phase at high temperatures ($> 600°C$). Direct deposition of poly-Si films makes the process simple and reduces the production costs. However, before adopting such a process widely, certain problems need to be considered. These problems are related to the film quality: in terms of grain size and defect density the microstructure of as-deposited poly-Si films tend to be of inferior quality. A typical manifestation of this is the increased surface roughness of as-deposited poly-Si films, which tends to give rise to surface scattering at the insulator/poly-Si interface and thus to degrade the performance of the TFT device.

Secondly, poly-Si films can be produced by the phase transformation of a-Si into poly-Si. Figure 1.2 shows a variety of processes by which crystallized poly-Si can be formed. Phase transformation to poly-Si can be achieved either at high or low temperatures. Solid-phase crystallization (SPC) processes [9, 10] are able to transform amorphous Si into poly-Si at high temperatures ($> 600°C$). In most cases they take place in diffusion furnaces over a long period of time. Since a compromise has to be found among annealing time, annealing temperature, and film quality, the thermal budget of the process tends to exceed the limit imposed by the glass substrate. Although poly-Si films are easy to obtain, annealing time is too long, which decreases the throughput. The use of rapid thermal annealing (RTA) [11, 12] allows for the efficient reduction of the thermal budget and the annealing time, which results in a substantially higher throughput than with SPC. Nevertheless the grain size of the poly-Si film annealed by RTA is much smaller than that obtained by SPC.

**Low-Temperature Poly-Si Films**

Several methods have been proposed in the literature to reduce the processing temperature and thus obtain better quality poly-Si films – for example using composite films, in which one layer provides nucleation seeds and the other layer of a-Si is converted into poly-Si, or employing various alloys to enhance

Si crystal growth at low temperatures (e.g., SiGe and metal-assisted crystallization methods [13] among others). The major drawbacks of these techniques are that poly-Si grains have a needle-like shape and they are contaminated by external impurities during the annealing process.

| ***TFT fabrication process*** | ***Mobility [$cm^2/Vs$]*** |
|---|---|
| Conventional poly-Si | 20–50 |
| Excimer laser poly-Si | 50–200 |

Table 1.1: Electron mobility in poly-Si TFTs produced using different processes.

Over the last decade activities have focused on the development of new technologies for improving the quality of poly-Si films using excimer laser crystallization (ELC) [14]. The basic principle of laser crystallization is the transformation from amorphous to crystalline Si by melting the Si layer for a very short time. A very high quality poly-Si results from the subsequent solidification. The ELC process is widely used in manufacturing TFTs as it is much faster than other existing techniques and can produce large grains of poly-Si with a low dislocation density at low temperatures ($< 600°C$). The mobilities obtained with excimer laser and conventional poly-Si techniques are compared in Table 1.1. The main advantages of the ELC process are the following: (i) crystallization from the melt, resulting in high quality, almost defect-free grains; and (ii) compatibility with low-cost glass substrates, since the high temperatures are sustained only for a very short time. Because of its short duration, thermal strain on low-temperature substrates does not damage the substrates.

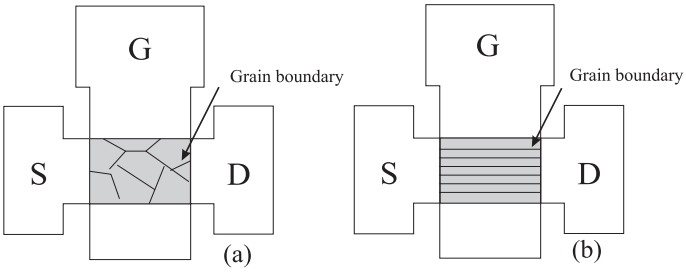


Figure 1.3: Schematic planar view of a (a) poly-Si TFT; (b) 1D location-controlled poly-Si TFT.

Conventional ELC can produce grain sizes in the range of 100 nm to 500 nm, depending on the a-Si film thickness [15]. Moreover, the grain sizes produced by conventional ELC are highly non-uniform with randomly oriented GBs, as shown in Figure 1.3 (a), which results in non-uniform device characteristics. Therefore recent research efforts on ELC have focused on developing methods to increase the grain size, as GBs are a major factor in limiting carrier transport in the TFT channel. Among these methods, substrate heating [16] and the dual-beam method [17] are commonly used. However, these methods require complicated laser annealing systems and create grains at arbitrary positions on the substrate. A maximum grain size of 1 µm is achieved and the field-effect electron mobility approaches 200 $cm^2/Vs$. Due to the randomness of the location of GBs, as shown in Figure 1.3(a), device-to-device uniformity of the TFT performance significantly deteriorates despite the enhancement of the average performance. Thus, the control of the GB location is essential for ensuring the uniformity of large-grained TFTs, which is in principle achieved by the location control of Si grains. Various methods for controlling GB locations have been proposed for the excimer laser crystallization process. These can be classified according to the number of controlled dimensions : one (1D) or two (2D).

The grain location is controlled in 1D by the lateral growth of the molten Si. Several modulated excimer laser annealing methods have been proposed to realize large grains, such as sequential super lateral growth (SLG) [18], selectively enlarging laser crystallization (SELAX) [19], continuous-wave (CW) laser lateral crystallization [20], phase-modulated excimer laser annealing (PMELA) [21], and so on. The grain size varies from 1 µm to 10 µm. To produce high performance TFTs, the channel is thus positioned parallel to the GBs, as shown in Figure 1.3(b). The field-effect electron mobility of TFTs approaches 400 $cm^2/Vs$, and a rather high subthreshold swing is obtained due to the presence of GBs. However, the number of these parallel GBs vary from device to device, leading to large variations in the characteristics. The best solution would be eliminating these GBs completely from the active channel of the device. This can be accomplished by controlling the location of the grains precisely in 2D. This possibility will be discussed later in this chapter.

**Conduction in Poly-Si Films**

Conduction of the carriers in poly-Si films is certainly different from conduction in a single-crystal silicon because of the presence of GBs, since the latter strongly affect carrier transportation in the film. They introduce a discontinuity in the periodic lattice and can be observed as planar defects or dislocations.

The boundary planes are filled with dangling bonds and strained bonds, which lead to electronic states in the forbidden gap. These dangling bonds typically lead to deep states, whereas strained bonds introduce tail states. Electronic states in the forbidden gap act as trapping centers for the carriers, enhancing their recombination or generation.

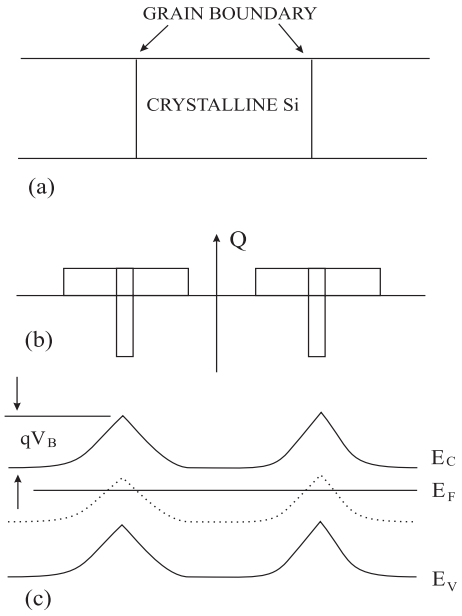


Figure 1.4: (a) Poly-Si film with grain boundaries; (b) charged depletion region forms in the grains around the grain boundaries; (c) band bending in the energy diagram caused by the charged depletion region.

Based on the following assumptions, Seto [22] developed a comprehensive model for carrier transport phenomena in poly-Si films: (i) Grains are identical. (ii) Grain boundary thickness is negligible. (iii) Traps are initially neutral and become charged by trapping a free carrier. (iv) Only one type of impurity atom is present (monovalent trapping) and uniformly distributed.

Trapping free carriers at the GBs creates a potential barrier at the boundary. The height of the potential barrier strongly depends on the dopant concentration and the trap density. An increase in the number of the carriers trapped at the GB leads to an increase in the height of the potential barrier. Above a critical doping density, all traps at the GB will be filled and

the remaining carriers will reduce the width of the depletion region, leading to a decrease in the height of the barrier. This behavior of the poly-Si film is illustrated in Figure 1.4. If the doping density is

$$N_{\mathrm{D}} < \frac{N_{\mathrm{t}}}{L}\ [\mathrm{cm}^{-3}], \tag{1.1}$$

the potential barrier height increases with $N_{\mathrm{D}}$ [23]:

$$qV_{\mathrm{B}} = \frac{qN_{\mathrm{D}}L^2}{8\varepsilon}\ [\mathrm{eV}], \tag{1.2}$$

while for

$$N_{\mathrm{D}} > \frac{N_{\mathrm{t}}}{L}\ [\mathrm{cm}^{-3}] \tag{1.3}$$

the potential barrier height decreases as

$$qV_{\mathrm{B}} = \frac{qN_{\mathrm{t}}^2}{8\varepsilon N_{\mathrm{D}}}\ [\mathrm{eV}], \tag{1.4}$$

where $qV_{\mathrm{B}}$ is the barrier height, $N_{\mathrm{D}}$ the doping concentration, $N_{\mathrm{t}}$ the trap density, $L$ the grain size, and $\varepsilon$ the dielectric constant of Si. In poly-Si TFTs a similar reduction in the height of the GB potential barrier is observed.

**Electrical Behavior of Poly-Si TFTs**

The electrical behavior of poly-Si TFTs is described on the basis of field-effect transistors (FETs). Their performance is evaluated by four parameters, which define the figure of merit: (i) Field effect mobility or on-current; (ii) Subthreshold swing; (iii) Threshold voltage; and (iv) Off-current.

***Field effect mobility.*** $\mu_{\mathrm{FE}}$ is one of the most important parameters to characterize poly-Si TFTs. Carrier transport in intrinsic or moderately doped poly-Si is dominated by the potential barrier at the GBs. Since the potential barrier is high, conductivity is low. By applying a vertical electric field, however, the potential barrier can be brought down. In the GB trap model the drain current $I_{\mathrm{DS}}$ can be written as [24]

$$I_{\mathrm{DS}} = \frac{WC_{\mathrm{ox}}\mu_{\mathrm{FE,e}}}{L}(V_{\mathrm{GS}} - V_{\mathrm{TH,n}})V_{\mathrm{DS}}\exp\left(-qV_{\mathrm{B}}/kT\right), \tag{1.5}$$

where $W$ and $L$ are the channel width and channel length of the TFT, while $V_{\mathrm{GS}}$, $V_{\mathrm{DS}}$, and $V_{\mathrm{TH,n}}$ are the gate voltage, drain voltage, the threshold voltage,

respectively, and $k$ is Boltzmann's constant. $\mu_{\mathrm{FE,e}}$ is the electron mobility and $C_{\mathrm{ox}}$ is the gate-oxide capacitance per unit area. Assuming that the thickness of the poly-Si film is proportional to $1/(V_{\mathrm{GS}} - V_{\mathrm{TH,n}})$ and all traps are filled with a trap state density $Q_{\mathrm{t}}$, the potential barrier [25] at the GB is

$$V_{\mathrm{B}} \sim \frac{Q_{\mathrm{t}}^2}{(V_{\mathrm{GS}} - V_{\mathrm{TH,n}})^2}. \tag{1.6}$$

This implies that for high $V_{\mathrm{GS}}$ the traps at the GBs do not impede the flow of carriers. Consequently the carrier mobility should approach that of a MOSFET. However, experimental results do not support this conclusion. The disparity could partially be attributed to the fact that tail states have been neglected in this GB trap model.

***Subthreshold swing.*** $S$ is a typical parameter to describe the quality of turn-on characteristics, where the device is controlled solely by the modulation of carriers in the channel by the gate voltage. It is defined as the amount of gate voltage required to increase/decrease the drain current by one order of magnitude. The subthreshold swing of the transfer characteristics is defined as

$$S = \frac{dV_{\mathrm{GS}}}{d\log(I_{\mathrm{DS}})}, \tag{1.7}$$

A lower subthreshold swing ensures a high performance of the TFT. A classical expression of the subthreshold swing for MOSFET is given as [26];

$$S = \frac{kT}{q} \ln 10 \left(1 + \frac{C_{\mathrm{depl}}}{C_{\mathrm{ox}}}\right), \tag{1.8}$$

in which $C_{\mathrm{depl}}$ is the capacitance of the depletion region in the channel and $C_{\mathrm{ox}}$ is the gate capacitance. This equation does not take the interface trap density in account. The capacitance of the interface states $C_{\mathrm{it}}$ is parallel to the depletion capacitance. It can be included in Eq. 1.8 by replacing $C_{\mathrm{depl}}$ by $C_{\mathrm{depl}} + C_{\mathrm{it}}$,

$$S = \frac{kT}{q} \ln 10 \left(1 + \frac{C_{\mathrm{depl}} + C_{\mathrm{it}}}{C_{\mathrm{ox}}}\right), \tag{1.9}$$

This suggests that the subthreshold swing is affected by the interface states as well as bulk states and generally independent of the drain voltage and the gate voltage. However, in reality, it might increase with drain voltage due to short-channel effects.

***Threshold voltage.*** Another important TFT parameter is $V_{\mathrm{TH}}$, defined as the gate-source voltage at which conduction electrons begin to appear in the channel. A low threshold voltage is needed to assure that the TFT operational regime is within a reasonable voltage range. In the transfer characteristics, the threshold voltage can be determined at the onset of the transition to on-current.

***Off-current.*** $I_{\mathrm{OFF}}$ is defined as the minimum current in the transfer characteristics of the TFT. A high $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ratio is desirable for TFT operation. Therefore the transistor should have a high $I_{\mathrm{ON}}$ and a low $I_{\mathrm{OFF}}$.

## 1.3 2D Location-Controlled Grains

To realize a high TFT performance with minimum variations in the characteristics from transistor to transistor, the active channel region of the device must be inside a single grain. A TFT fabricated inside a single grain is called a *single-grain (SG) TFT*. However, it is indispensable to control the location of the grain for fabricating SG TFTs. This situation is illustrated in Figure 1.5. Formation of the TFT channel region inside a single grain imposes two requirements.

***1. Location control.*** To fabricate the TFT inside a single grain, the location of the grain must be controlled precisely in two dimensions (2D). In this way the grain is obtained at a predetermined position in the Si film.

***2. Grain Size.*** If the size of the location-controlled grain is larger than that of the TFT channel region, a TFT with a single crystalline channel can be fabricated.

To fulfill these conditions, several ELA methods have been proposed for controlling the location of large Si grains in 2D. The most widely used methods are briefly described below.

***Dual beam with thick oxide portion (DBTOP)*** is the first method to control the location of large Si grains in 2D with one shot of ELA [27]. This method makes use of the spatial geometrical variation of the sample. This approach permits the control of complete and incomplete melting areas of the Si film. Selectively increased thickness of the underlying $SiO_2$ (bump) produces an imposed temperature non-uniformity along the $Si/SiO_2$ interface. As a result of the increased thermal capacitance of the thicker bump region, the lowest temperature always occurs at the center of the bump and a large grain of 5 µm is obtained at a precise position on top of the $SiO_2$ layer. This

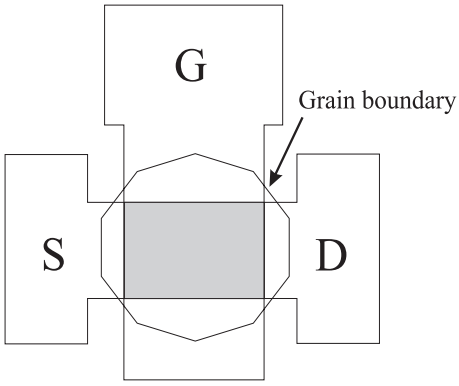


Figure 1.5: Schematic planar view of a SG TFT designed inside a location-controlled grain in 2D.

method is very sensitive to the structure of the bump and also the laser energy that reduces the yield of large grains.

***Dot sequential lateral solidification (Dot-SLS)*** enables the formation of near-single-crystal Si grains [28]. This method is based on the solidification of molten Si in the SLG regime. Dot-SLS is the extended version of SLS, with the crystallization and irradiation sequence carried out without pausing. Dot-SLS requires several shots of laser irradiation to get the location-controlled grain. This reduces the production throughput. A precise optical alignment of the laser beam increases the cost and complexity. This technique is still used only in laboratories.

***Advanced phase modulated excimer laser annealing (PMELA)*** is another advanced method to control the location of grains in 2D by modulating the intensity of the irradiated light, using a phase modulator placed between the sample and the laser [29]. This produces a light intensity gradient on the sample surface by interference. A temperature gradient triggers lateral grain growth from the edge of the completely molten Si region, whereby large crystal grains are grown laterally at predetermined positions. In PMELA, laser light intensity distribution is a key factor in growing uniform and large Si grains. However, the non-uniformity of the excimer laser light reduces the yield. Besides, the precise optical alignment of the laser beam increases the complexity of this method.

***The* µ-*Czochralski process*** is able to control the location of the grain precisely at a predetermined position in 2D [30]. This method has been developed at Delft University of Technology. The location of the grain is precisely con-

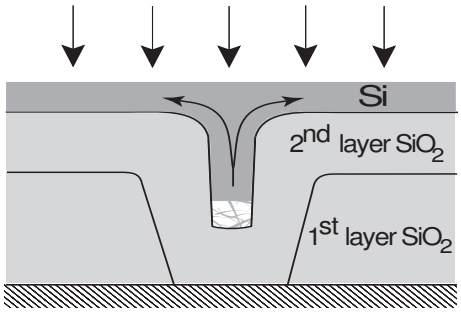


Figure 1.6: Schematic diagram of the µ-Czochralski process.

trolled by modifying the substrate with conventional photolithography rather than by spatially modifying the incident laser energy density. A small-diameter cavity is formed in an insulating layer and then it is filled with a-Si. After one shot of laser irradiation, a vertical growth starts in the cavity, where a small

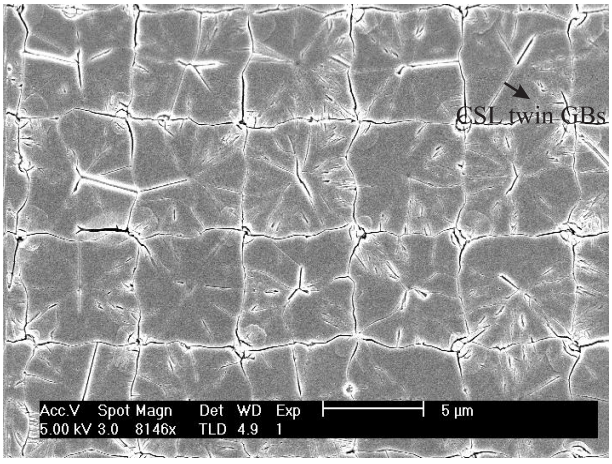


Figure 1.7: SEM image of location-controlled grains fabricated using the µ-Czochralski process.

amount of unmolten Si at the bottom serves as a seed during crystallization. In this phase grain occlusion occurs in the cavity. For this reason the cavity is called a *grain filter*. As a result of filtering, only one grain reaches the top of the cavity, which will be the seed for the lateral growth of the single grain. Figure 1.6 shows the structure of the µ-Czochralski process. The diameter of the cavity and the laser energy density are the two important parameters in the µ-Czochralski process. Figure 1.7 shows a matrix of grains after defect etching with a pitch of 5 µm. To obtain large location-controlled grains, this method is more attractive than any other existing technique. It works for a large range of energy densities and has a high yield for single grains. Moreover, its throughput is high, as only one shot of laser is needed to produce the large grain. This method of realizing high performance SG TFTs and digital circuits is described in detail in the next chapters of the present thesis.

## 1.4 The Goal of this Research

One of the goals of this research is to obtain high performance n- and p-channel SG Si TFTs at a process temperature of 350°C. Another goal is the realization of CMOS digital circuits using these high performance SG Si TFTs. The µ-Czochralski process was used to fabricate the TFT inside a single grain to ensure high performance and good uniformity. For n-channel SG Si TFTs fabricated inside a location-controlled grain by the µ-Czochralski process $\mu_{\mathrm{FE,e}}$ values of 430 $\mathrm{cm}^2$/Vs and $S$ values of 0.45 V/dec. were found [31]. This performance might be limited by the coincidence site lattice (CSL) inside the location-controlled grains, as shown in Figure 1.7. To improve the performance of n- and p-channel SG Si TFTs to the level of SOI transistors, the effects of the CSL GBs on the TFT characteristics are investigated. The channel of the SG Si TFT was positioned in various directions with respect to the grain filter. At the position that corresponds to a current direction parallel to the CSL GBs, the performance of the TFT approaches that of SOI transistors. Next, the electrical reliability of these (n- and p-channel) SG Si TFTs were investigated by applying either drain bias stress or gate bias stress. Finally CMOS digital circuits of inverters and ring oscillators were realized with SG Si TFTs. In the inverter design a single grain covers both (n- and p-) channels of the TFT.

In general, transistors with a thin film ($\sim$ 70 nm) are required to avoid short-channel effects and to ensure compatibility with LTPS production. However, the quality and size of the grain both decrease for thinner Si films. A new process has been developed to increase the grain size by employing a cap-

ping layer of $SiO_2$ on top of the a-Si before crystallization. This improves the bulk Si quality and the interface quality between Si and $SiO_2$. This has been demonstrated using performance data of SG TFTs fabricated with a capping layer of $SiO_2$ as part of the gate insulator. CMOS digital circuits have been realized with the newly developed process for producing thin Si films.

## 1.5 Chapter Structure of the Thesis

Figure 1.8 shows the structure of this thesis. Chapter 1 gives an overview of TFTs – from a-Si to poly-Si. A brief description of 2D location-controlled grains fabricated using the µ-Czochralski process is also given.

Chapter 2 deals with the design and fabrication process of SG Si TFTs based on the µ-Czochralski process. The effects of CSL GBs on n- and p-channel SG Si TFTs are addressed in this chapter. The effects of crystallization energy on SG Si TFT performance is also discussed. A longer-pulse excimer laser is introduced for further improvement of the performance of SG Si TFTs.

SG Si TFTs are a potential candidate for digital and analog circuits. However, the stability of TFTs is very important in digital and analog applications. Chapter 3 examines the electrical and thermal reliability of n- and p-channel Si TFTs inside a single grain. The reliability of SG Si TFTs is investigated under drain and gate bias stress. In the last section of this chapter the carrier transport mechanisms in SG TFTs are investigated by characterizing the activation energy of the drain current.

Chapter 4 presents the design and performance of SG CMOS inverters fabricated using the µ-Czochralski process. In the SG CMOS inverter design both (n- and p-) TFT channels are inside a single grain. A ring oscillator is designed by cascading an odd number of SG inverters in a circular chain. Propagation gate delay is estimated using the ring oscillator.

Chapter 5 deals with the effects of a $SiO_2$ capping layer on the Si film in excimer laser crystallization by the µ-Czochralski process. During crystallization, the $SiO_2$ capping layer acts as an anti-reflection layer and a heat reservoir. The thickness of the $SiO_2$ capping layer is optimized to achieve minimum reflectance. The $SiO_2$ capping layer efficiently enlarges the location-controlled grains as it reduces the solidification rate of molten Si. SG TFTs with a thin Si layer were fabricating using this $SiO_2$ capping layer as part of the gate insulator. Finally, SG CMOS inverters and ring oscillators were fabricated with this process for thin Si films.

The summary of this research done over the past four years and recommendations for the future are listed in Chapter 6.

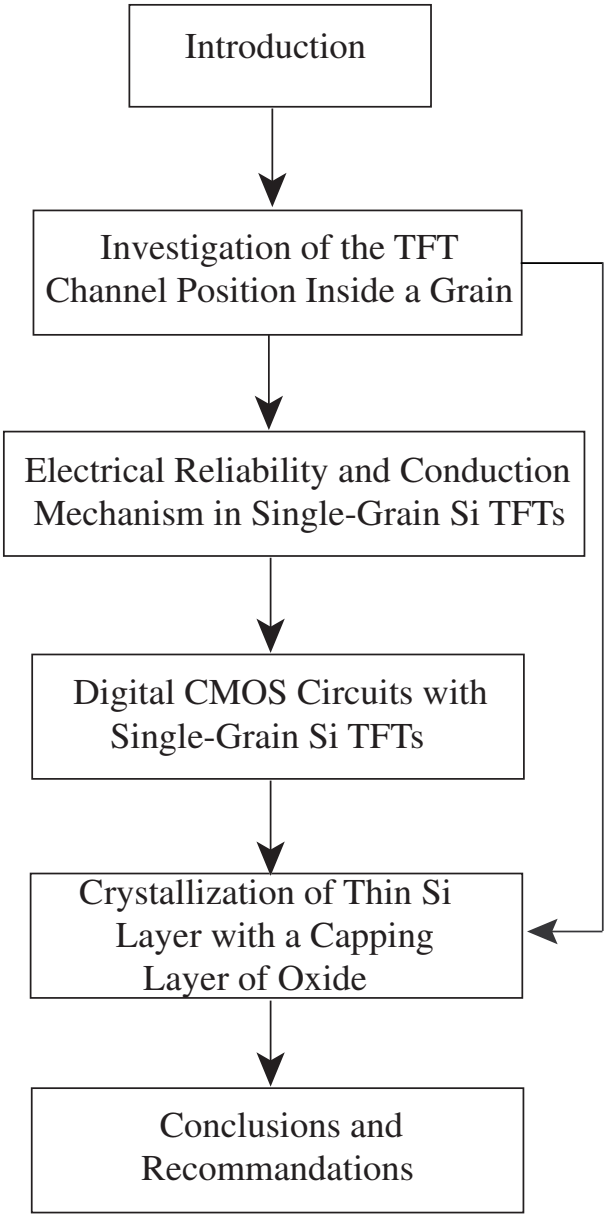


Figure 1.8: Schematic structure of the thesis.

# Chapter 2

# Investigation of the TFT Channel Position Inside a Grain

*This chapter presents the* µ-*Czochralski process for controlling the grain location in 2D during excimer laser crystallization. Coincident site lattice (CSL) twin GBs originated from the grain filter affect the characteristics of SG Si TFTs. This was investigated by positioning the TFT channel in various directions with respect to the grain filter. SG TFTs with a current direction parallel to the CSL twin GBs showed a dramatic improvement in the characteristics as carriers are not impeded by the CSL GBs. SG Si TFTs have high average* $\mu_{FE}$*s values: 600 cm*$^2$*/Vs for electrons and 273 cm*$^2$*/Vs for holes. Using longer-pulse (200 ns) excimer lasers improves the microstructure of the grain, increasing* $\mu_{FE,e}$ *up to 644 cm*$^2$*/Vs for electrons. Effects of the crystallization energy and Si thickness on the characteristic values are examined. Finally, the effects of vacuum annealing are also analyzed.*

## 2.1 Introduction

SG Si TFTs fabricated inside location-controlled grains using the µ-Czochralski process showed an average $\mu_{\mathrm{FE,e}}$ of 430 cm$^2$/Vs and a rather high $S$ value, 0.45 V/dec. [31]. The $S$ value is still higher than those of MOSFETs [26] and reported recently in [32] for poly-Si TFTs. In previous studies the channel

of the SG Si TFT was located above the grain filter. The characteristics might be limited by defects near the bottom of the grain filter. Furthermore, location-controlled grains have planar defects, which are mainly coincident site lattice (CSL) twin boundaries and are radially distributed from the grain filter center. It has been reported that defective planes perpendicular to the current flow direction impede the on-current [33]. In this chapter we investigate the influence of the channel position on SG Si TFT characteristics. We designed the TFT channel with and without a grain filter and with various current flow directions including parallel and perpendicular to the planar defects. The characteristics of n- and p-channel SG Si TFTs are expected to improve by positioning the channel parallel to these planar defects. Furthermore, the effects of crystallization energy, post-process annealing, and Si thickness on the performance of SG Si TFTs are also examined.

## 2.2 The μ-Czochralski Process

This section presents the process flow of grain filter and location-controlled grain formation by the μ-Czochralski process [30]. This method provides a precise way to control the location of the grain in 2D. Figure 2.1 shows the fabrication process of the grain filter. Using conventional lithography (ASML PAS 5000/50 wafer stepper), cavities with a characteristic size of 1.0 μm were patterned on an oxidized c-Si wafer. The diameter of the cavities is reduced by the deposition of an oxide layer using tetra ethyl ortho silicate (TEOS) by means of plasma-enhanced chemical vapor deposition (PECVD) (based on Novellus Concept One System) at 350°C. In this way an optimum cavity diameter ($\phi_{GF} \approx 100$ nm) is obtained.

Next, a layer of a-Si is deposited by low-pressure plasma chemical vapor deposition (LPCVD) (Tempress Omega-M diffusion furnace) at 550°C. The layer of a-Si is crystallized by excimer laser irradiation at an elevated substrate temperature of 450°C. The sample is irradiated with one shot of excimer laser. The Si is molten to a certain depth of the cavity; however, it is not completely molten, and a portion of the a-Si remains solid at the bottom of the cavity, as shown in Figure 2.2(b). Solidification then starts from the solid Si layer, which acts as a seed, inside the cavity. In the vertical growth phase grains are occluded from the cavity, i.e., grains are filtered. This is why the cavity is also known as a grain filter. When the grain reaches the top of the grain filter, the lateral growth phase of the grain starts. Lateral growth continues until solidification occurs in the surrounding Si film. Figure 2.2(a) shows the SEM image of location-controlled grains after Secco etching. Here the grain

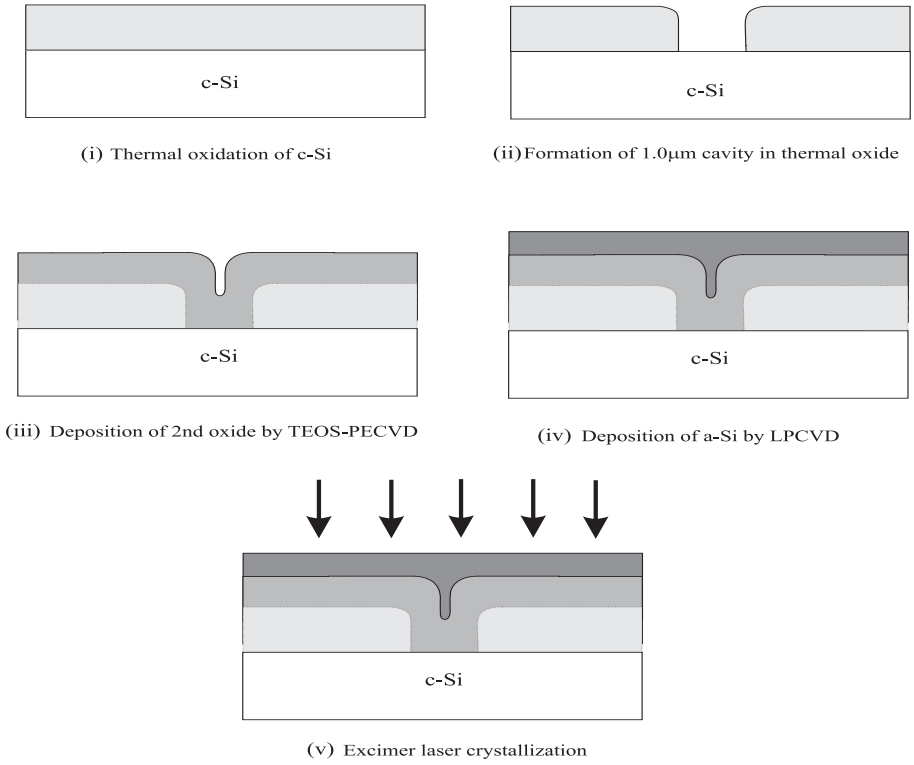


Figure 2.1: Schematic diagram of the formation of a location-controlled grain in the μ-Czochralski process.

filters are arranged in a grid with a separation of 5 μm, shorter than the maximum achievable grain size of 7 μm. This configuration generates a grid of square-shaped grains, since grains collide with one another.

## 2.3 Design of Single Grain TFTs

TFTs with a top gate coplanar self-aligned structure are designed in such a way that the single grain covers the entire channel area of the TFT. In a previous study, the channel of the SG TFTs was located above the grain filter [31]. The characteristic values of SG Si TFTs might be limited by defects near the bottom of the grain filter. Furthermore, the location-controlled grain has

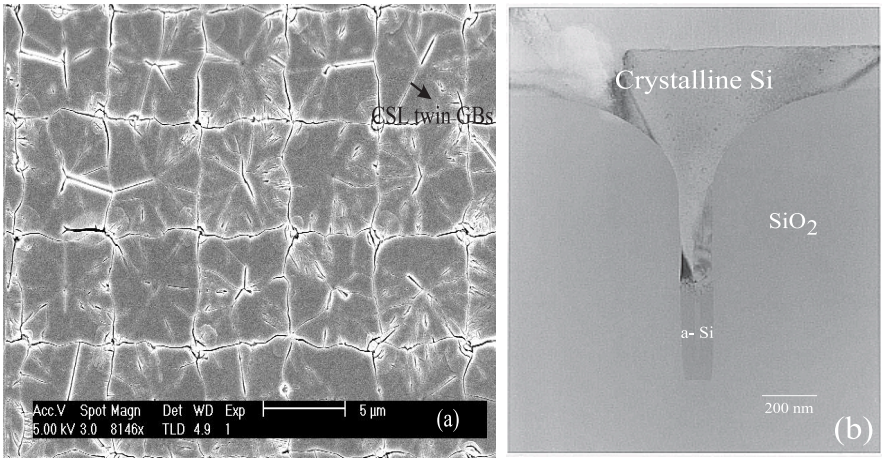


Figure 2.2: (a) SEM image of location-controlled grains fabricated using the µ-Czochralski process. White dots show the corners of the grains where four grains collide with one another. (b) Cross-sectional TEM image of a location-controlled single grain, showing that grain growth starts at the interface of molten and solid Si.

planar defects, which are mainly coherent Σ3 and Σ9 twin boundaries, radially distributed from the center of the grain filter [34]. It has been suggested that some of the Σ9 planes that are perpendicular to the current flow direction impede the on-current.

In the present study the channel of the TFT inside the location-controlled grain is placed at various positions so that the TFT should have various current flow directions with respect to these defects. First the channel is positioned on top of the grain filter (*C* position), as in [31]. Second, the channel position is shifted away from the grain filter, keeping the direction of current flow parallel to the planar defects. This position is referred to as the *X* position. Third, the channel is placed at the position where the direction of current flow is perpendicular to the planar defects. This is called the *Y* position. Finally the channel is designed in *XY* plane, where these planar defects are diagonal with respect to the direction of current flow (*XY* position). Figure 2.3 shows the schematic diagram of the TFT channel inside a location-controlled single grain. The shift in the channel position with respect to the grain filter is 1.5 µm for each channel position. Figure 2.4 shows the mask design of a TFT at the *X* position inside a location-controlled single grain that follows the design

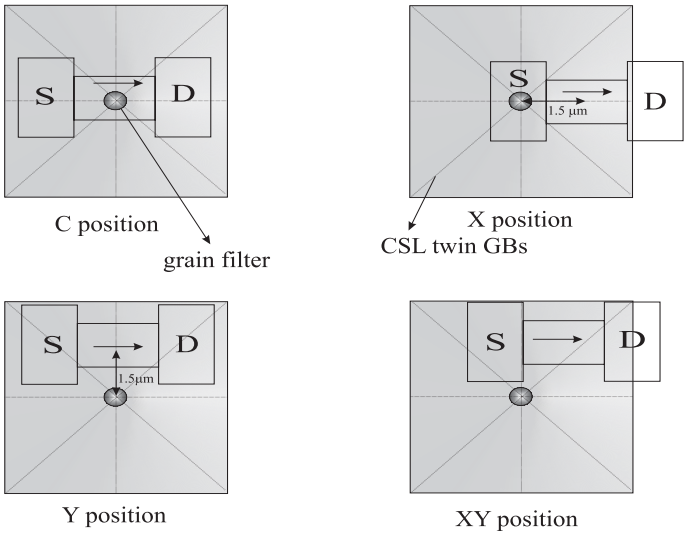


Figure 2.3: Schematic diagram of TFT channels at various positions inside a location-controlled single grain.

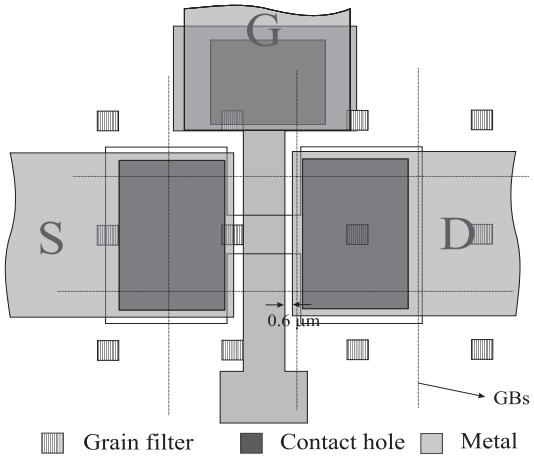


Figure 2.4: Design of a top gate coplanar self-aligned TFT with a shift in the $X$ direction inside a location-controlled single grain.

rules for 0.6 µm technology.

## 2.4 Fabrication of Single-Grain TFTs

The schematic diagram of the fabrication process flow of n-channel SG Si TFTs at the *C* position is shown in Figure 2.5.

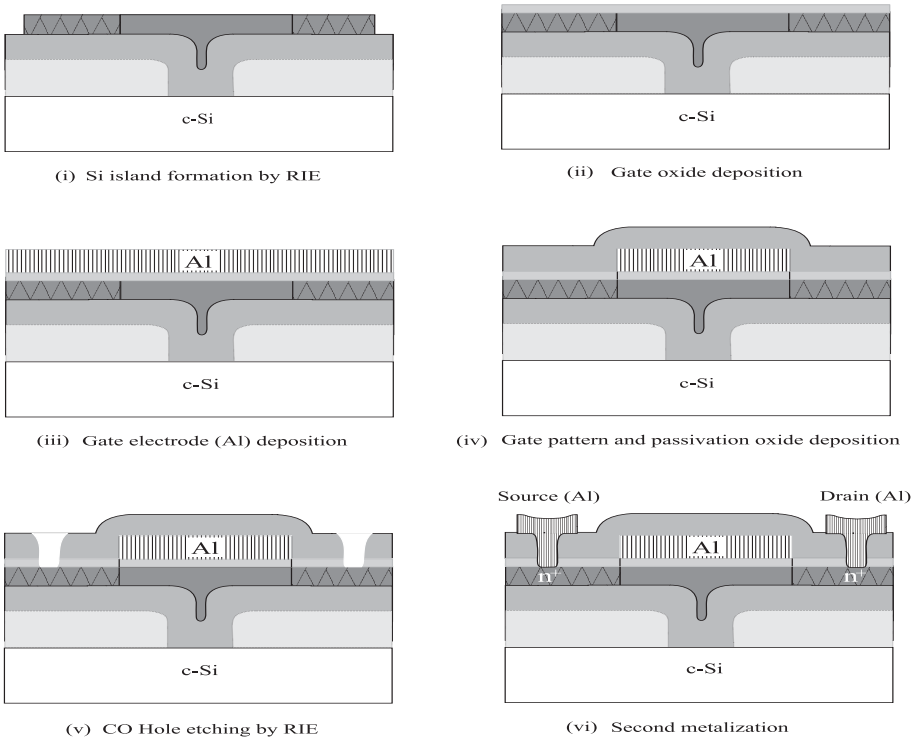


Figure 2.5: Process flow for the fabrication of a SG Si TFT inside a location-controlled grain with the channel of the TFT at the *C* position.

As mentioned in the previous section, 2D location-controlled grains are fabricated by the µ-Czochralski process using excimer laser crystallization. Next, an oxygen plasma treatment is carried out to passivate trap states and dangling bonds in bulk Si [35]. Then the crystallized Si film is patterned into islands by reactive ion etching. The design of the channel region of the

TFTs is such that the single grain covers the entire channel area. Next low-temperature ($< 350°C$) $SiO_2$ is deposited to produce a gate insulator. The gate electrode is then formed by depositing sputtered Al (Trikon Technology Sigma 201 cluster tool) at room temperature. Using the Al gate pattern as a mask, the source/drain region is either doped by impurity implantation and activated by excimer laser annealing or doped by an ion shower and then annealed at 300°C for four hours in ambient $N_2$. After depositing inter-layer TEOS-PECVD $SiO_2$, the contacts to the Al gate and the source/drain are both made in a single step. The step-by-step listing of the process is given in Appendix A2.

### 2.4.1 Low-Temperature Oxides

To obtain high-performance TFTs, besides high-quality Si a high-quality gate oxide – including low bulk and interface density – is also indispensable, since the characteristic values of field-effect devices (MOSFETs and TFTs) are limited by the quality of the gate insulator (bulk and interface properties). The quality of the gate insulator depends on the thermal budget. Although a lot of effort has been put into producing high-quality gate insulator films at low thermal budgets ($< 350°C$) using the LTPS technique, these mainly focused on deposition methods such as TEOS-PECVD, LPCVD, APCVD, and plasma CVD. In spite of these efforts, electrical characteristics of the deposited insulator films are not comparable to those of thermal oxides, since low-temperature oxides have higher defect densities. It was recently reported that the electrical characteristics of electron cyclotron resonance (ECR) plasma oxides grown at low temperatures on c-Si wafers using an oxygen plasma are comparable to those of thermal oxides due to the absence of plasma damage [36]. TEOS-PECVD oxides have also been reported to have good interface characteristics despite the plasma damage to the substrate.

#### ECR-PECVD Oxide

In our experiments we used ECR-PECVD and TEOS-PECVD oxides as gate insulators in the fabrication of SG TFTs. Metal-oxide semiconductor (MOS) capacitors were fabricated to characterize these oxides.

A 115 nm thick ECR-PECVD $SiO_2$ layer was deposited on a p-type c-Si wafer ($\rho = 2$–$5\,\Omega \cdot \mathrm{cm}$) at Seiko-Epson Research Center, Japan. Then a MOS capacitor was patterned with an Al electrode as a metal gate. The process flow of the fabrication of MOS capacitors is given in Appendix A3. The surface area of the MOS capacitor is $6.4 \times 10^3\,\mu\mathrm{m}^2$. For the electrical char-

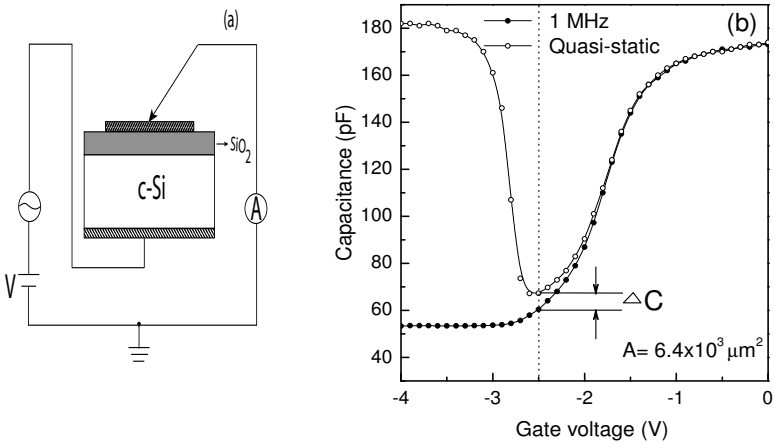


Figure 2.6: (a) Schematic diagram of the MOS capacitor measurement. (b) High-frequency and quasi-static C-V characteristics of the MOS capacitor formed by a 115 nm thick ECR-PECVD $SiO_2$ layer. $D_{it}$ at mid-gap is estimated to be $2.1 \times 10^{10}\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$.

acterization of the MOS capacitor, capacitance-voltage (C-V) measurements were performed. Figure 2.6(a) shows the schematic diagram of the MOS capacitance measurement. Quasi-static C-V measurements were performed on a Hewlett Packard (HP) 4156C Precision Semiconductor Parameter Analyzer, whereas high-frequency measurements were done with an HP 4284A LCR meter. Figure 2.6(b) shows the quasi-static and high-frequency C-V characteristics. The interface density of states ($D_{it}$) of the oxide layer is given by

$$D_{it} = \frac{C_{ox}}{q}\left(\frac{C_{lf}/C_{ox}}{1-C_{lf}/C_{ox}} - \frac{C_{hf}/C_{ox}}{1-C_{hf}/C_{ox}}\right) \tag{2.1}$$

[37], where $C_{ox}$ is the capacitance per unit area, $C_{lf}$ is the quasi-static capacitance, and $C_{hf}$ is the high-frequency capacitance measured at 1 MHz. $D_{it}$ at mid-gap is estimated to be $2.1 \times 10^{10}\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$. This result shows that the interface quality of ECR-PECVD oxide is comparable to that of thermal oxide ($D_{it} = 1.07 \times 10^{10}\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$). This makes ECR-PECVD oxide a suitable candidate for gate insulator in TFT fabrication. In spite of the low $D_{it}$, it is

not used in the mass production of TFTs due to its inherent disadvantages: (i) bad step coverage; (ii) $D_{\mathrm{it}}$ increases with decreasing thickness; and (iii) the presence of mobile protons in the bulk, which destabilizes the AC operation of the TFT [38].

**TEOS-PECVD Oxide**

Low-temperature TEOS-PECVD oxide has been used as gate insulator in the mass production of LTPS because of its excellent step coverage. However, a typical $D_{\mathrm{it}}$ of the TEOS-PECVD $SiO_2$ is on the order of $10^{11}\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$ [39] due to inherent plasma damage to the substrate and residual impurities in the PECVD reactor. Recently, the $D_{\mathrm{it}}$ value of TEOS-PECVD $SiO_2$ has been improved at Seiko-Epson Research Center, Japan by applying an oxygen plasma directly after oxide deposition in the PECVD reactor. In this experiment, an 80 nm thick TEOS-PECVD oxide layer was deposited on an n-type c-Si wafer. After patterning the MOS capacitor with Al as a gate, the C-V measurement was performed with an HP 4156C parameter analyzer and an LCR meter.

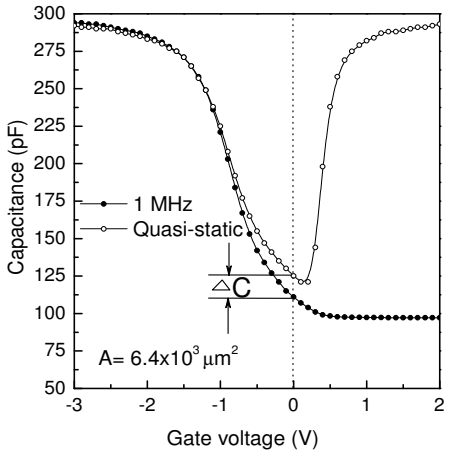


Figure 2.7: High-frequency and quasi-static C-V characteristics of the MOS capacitor formed by an 80 nm thick TEOS-PECVD $SiO_2$ layer. $D_{\mathrm{it}}$ at mid-gap was estimated to be $2.52 \times 10^{10}\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$.

Figure 2.7 shows the quasi-static and high-frequency C-V characteristics

of the TEOS-PECVD oxide. From Eq. (2.1), $D_{\mathrm{it}}$ at mid-gap was estimated to be $2.52 \times 10^{10}\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$. These results confirm that TEOS-PECVD and ECR-PECVD are appropriate candidates for high-quality gate insulators in the fabrication of low-temperature SG Si TFTs.

### 2.4.2 Dopant Activation at Low Temperature

Low-temperature SG Si TFTs have stimulated an interest in various applications in the microelectronics industry, because their performance is comparable to MOSFETs. For low-temperature processing, dopants must be activated at low temperature and the source/drain regions of the SG Si TFT must have a low resistance. However, activation efficiency decreases with decreasing temperature, since a larger amount of the impurity atoms cannot reach substitutional sites of the Si lattice. This gives rise to serious degradation in the characteristics. Excimer laser annealing at room temperature and ion shower methods have recently been reported to be highly effective in activating dopants and yield very low resistances. In this research work we used either excimer laser annealing or the ion shower doping method for source/drain doping.

#### Excimer Laser Activation

Low-cost production of TFTs requires low-temperature processes, therefore the impurity doping technique is critical. Excimer laser annealing is very practical to activate dopants at low temperature with high activation efficiency [40].

A XeCl excimer laser system (XMR UVP 7100) is used for the crystallization of a-Si and the activation of the dopants. Figure 2.8 shows the schematic diagram of the excimer laser system. The pulse has a full width at half maximum of 56 ns at a wavelength of 308 nm. The laser beam passes through a homogenizer, which transforms the Gaussian shaped beam into a top-hat profile with variable beam size. The maximum beam size is $2 \times 2\,\mathrm{cm}^2$. The total transmittance of the system is 78% at best and energy can be decreased by introducing attenuators in the beam. Dopants are implanted into the source/drain region by an ion implanter (Varian E500 HP Medium Current). Then the excimer laser is used to activate the dopants at room temperature. For 250, 100, and 50 nm thick Si films, the excimer laser conditions have been optimized for minimizing the sheet resistance of the regions at room temperature. The amount of dopant and the laser energy density are listed in Table 2.1. The main advantage of excimer-laser activation is that it provides an abrupt profile with no dopant diffusion beyond the solid/liquid interface and a high activa-

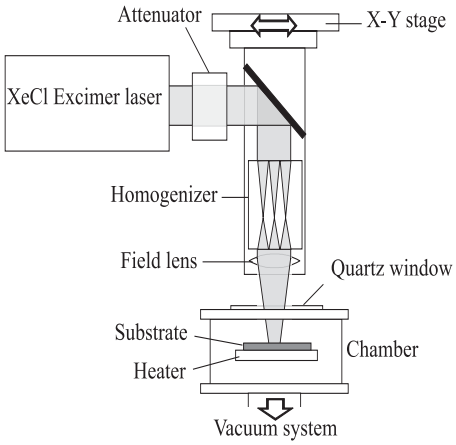


Figure 2.8: Schematic diagram of the excimer laser system.

tion of the dopant (even above solid solubility). Besides, light is diffracted from the edges of the Al gate electrode. Secondly, dopants diffuse laterally under the gate, which gives rise to higher $I_{\mathrm{OFF}}$ in the TFTs.

| ***Si thickness [nm]*** | $B^+/P^-$ ***dopants*** $[cm^{-2}]$ | ***Activation energy*** $[J/cm^2]$ |
|---|---|---|
| 250 | 1E16 | 0.3 (5 shots) |
| 100 | 4E15 | 0.3 (5 shots) |
| 50 | 2E15 | 0.275 (5 shots) |

Table 2.1: Dopant amounts and activation conditions for different Si thicknesses.

### Ion Shower Doping

Low-cost production of SG Si TFTs requires high productivity and low-temperature impurity annealing. Productivity is enhanced by introducing a new doping technique for large-area devices, the ion shower doping technique, which utilizes a bucket ion source of a radio-frequency-generated ion source at a low temperature [41,42]. Figure 2.9 shows the schematic diagram of the ion shower doping system in which high-density and uniform-discharge plasma is formed

by thermally emitted electrons and a magnetic field.

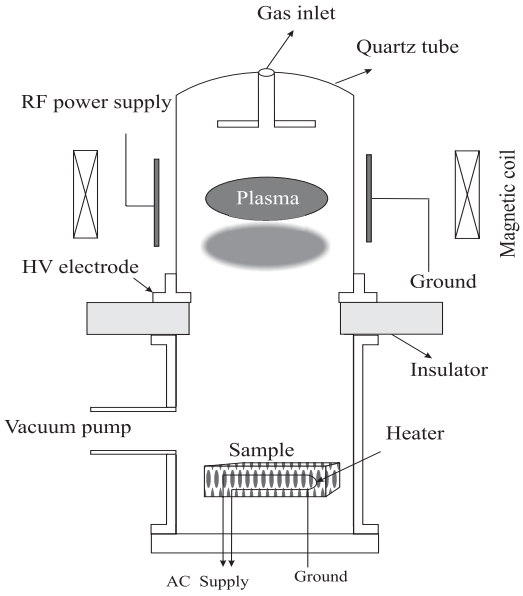


Figure 2.9: Schematic diagram of the ion shower doping setup.

The ion beam is extracted from the arc discharge chamber and irradiated into the sample. For phosphorus doping, phosphine gas ($PH_3$) diluted with hydrogen is introduced into the plasma chamber, whereas for boron doping, borane ($BH_3$) diluted with hydrogen is used. The magnetic field ensures the high efficiency of the ionization. The ions are accelerated by the voltage towards the sample. The total number of irradiated ions is calculated from the measured current density of the sample and the irradiation time. This method uses a large-area ion beam, which is easily controlled at low accelerating voltages. The accelerating voltage must be sufficiently low, in order to prevent ions from penetrating the A1 gate electrode. This technique offers a higher productivity than selective ion implantation, because dopants are activated during doping. The activation efficiency of the dopants is comparable to that of the ELA process, however the activation efficiency of boron is slightly lower because of the presence of hydrogen ions. Ion shower doping does not show any edge effect near the Al gate electrode and the SG Si TFTs have lower $I_{\mathrm{OFF}}$ than in the ELA method due to the absence of lateral dopant diffusion. SG Si

TFTs used for the research presented in this thesis were also doped with the ion shower method at Seiko-Epson Research Center, Japan.

## 2.5 Electrical Characterization of TFTs

The electrical characterization of TFTs was done using a Hewlett Packard 4156B Precision Semiconductor Parameter Analyzer. Each structure was measured with *Medium Integration Time* to ensure suppression of the capacitive current and zero delay time. The field-effect mobilities for electrons and holes are determined from drain current versus drain voltage measurements in the linear region. Mobility is defined as the maximum of the second derivative of the drain current with respect to drain voltage and gate voltage ($d^2I_{\mathrm{DS}}/dV_{\mathrm{DS}}dV_{\mathrm{GS}}$) at a low drain voltage. The off-current, subthreshold swing, and threshold voltage are determined from the drain current versus gate voltage curve at a constant drain voltage.

## 2.6 N-Channel Single-Grain TFTs

The performance of SG Si TFTs is limited by CSL twin GBs [43]. The effects of these CSL twin GBs were analyzed by positioning the channel in various directions with respect to the grain filter. In this section we shall discuss the effects of channel position, crystallization energy, pulse duration of the excimer laser, and Si thickness on the performance of SG Si TFTs.

### 2.6.1 Effects of Channel Position

To investigate the effects of the channel position inside a location-controlled grain, the position of the TFT channel was shifted in the $X$ and $Y$ directions and in a combination of them ($XY$) with respect to the center of the grain filter ($C$), as shown in Figure 2.3, while the current flow direction was kept fixed along the $X$ direction. The channel shift from the center of the grain filter was 1.5 µm. The cross section of the n-channel SG Si TFT is shown in Figure 2.10 for different channel positions. The channel length and width were 1.87 µm and 2.03 µm, respectively, measured by SEM. Table 2.2 shows the average characteristic values with standard deviation for n-channel SG TFTs with a 250 nm thick Si layer and a 120 nm thick ECR-PECVD $SiO_2$ layer as gate insulator, fabricated at various positions inside a location-controlled grain. The crystallization energy density of the excimer laser was 1.025 J/cm$^2$. The source/drain regions of these SG Si TFTs were doped using the ion shower

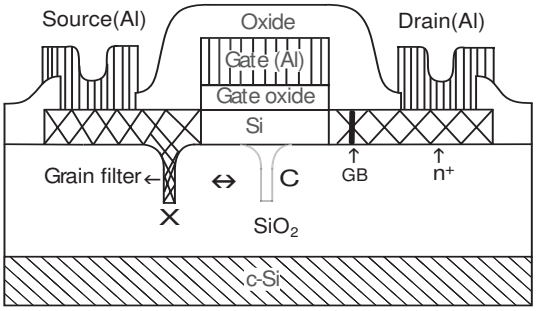


Figure 2.10: Schematic structure of an n-channel SG Si TFT fabricated inside a location-controlled grain with different channel positions.

technique at Seiko-Epson Research Center, Japan. As a reference, silicon on insulator (SOI) TFTs with a Si thickness of 250 nm and ⟨100⟩ orientation were fabricated under the same process conditions. To provide a statistical basis for the TFT characteristics, 16 transistors were measured for each position and each process condition.

| ***TFTs*** | ***Position*** | $\mu_{FE,e}[cm^2/Vs](\sigma\%)$ | $S[V/dec.](\sigma\%)$ | $V_{TH}[V](\sigma\%)$ |
|---|---|---|---|---|
| SG | *X* | 597±101(17%) | 0.21±0.03(13%) | 1.7±0.2(11%) |
| | *Y* | 528±57(10%) | 0.25±0.04(14%) | 1.8±0.3(15%) |
| | *XY* | 505±55(7%) | 0.22±0.01(6%) | 1.9±0.1(6%) |
| | *C* | 471±32(7%) | 1.1±0.13(12%) | 0.86±0.3(32%) |
| SOI | | 727±18(2.4%) | 0.18±0.006(3.6%) | 1.1±0.09(8%) |

Table 2.2: Characteristic values of n-channel SG TFTs with a 250 nm thick Si layer and a 120 nm thick ECR-PECVD $SiO_2$ layer as gate insulator. The crystallization energy density was 1.025 J/cm$^2$. The TFT channel was undoped.

Data in Table 2.2 show that SG Si TFTs at the *X* position have the highest $\mu_{\mathrm{FE,e}}$, lowest *S*, and lowest $I_{\mathrm{OFF}}$ values, while SG Si TFTs at the *C* position have the lowest $\mu_{\mathrm{FE,e}}$ and highest *S* values. The highest $\mu_{\mathrm{FE,e}}$ for SG Si TFTs (597 cm$^2$/Vs) at the *X* position is attributed to the fact that the carriers do not feel the CSL twin boundaries, which are parallel to the direction of current flow. Figure 2.11 shows the transfer characteristics of SG Si TFTs with ECR-PECVD $SiO_2$ and TEOS-PECVD $SiO_2$ as gate insulator for various channel

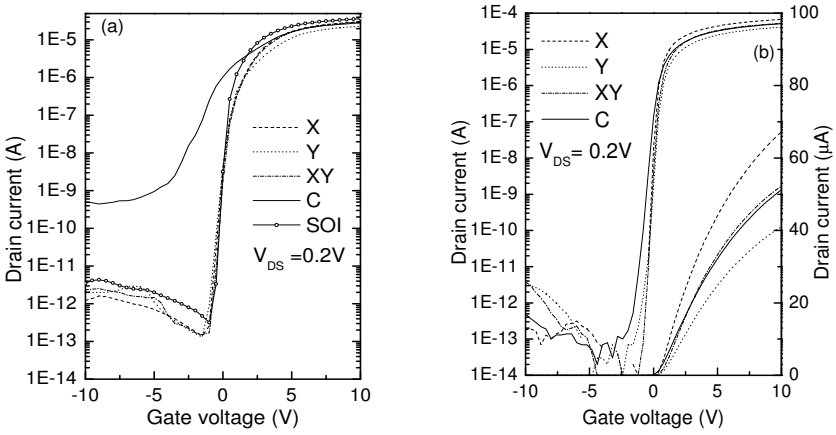


Figure 2.11: (a) $I_{DS}$-$V_{GS}$ characteristics of n-channel SG TFTs with a 250 nm thick Si layer and a 120 nm thick ECR-PECVD $SiO_2$ layer as gate insulator, for various channel positions in the location-controlled grain. The crystallization energy density was 1.025 J/cm$^2$. The TFT made with SOI wafer is also plotted as a reference. (b) $I_{DS}$-$V_{GS}$ characteristics of the n-channel SG TFTs with a 250 nm thick Si layer and a 30 nm thick TEOS-PECVD $SiO_2$ layer as gate insulator, for various channel positions in the location-controlled grain.

positions. By shifting the channel position from the top of the grain filter (*C*), the transfer characteristics for both gate insulators are improved. The *S* value of the TFTs with ECR-PECVD $SiO_2$ is dramatically improved by shifting the channel position with respect to the grain filter. This improvement arises from avoiding the grain filter – which has a high density of trap states at the bottom – from the active channel region.

### 2.6.2 Effects of Crystallization Energy Density

The quality and size of the location-controlled grain depend on the crystallization energy density. The size is proportional to the crystallization energy density [44]. The quality of the grains can be evaluated by the performance of the SG Si TFTs. N-channel SG Si TFTs were fabricated with various crystallization energy densities to investigate its effects on TFT characteristics.

Figure 2.12(a) shows the average $\mu_{FE,e}$ as a function of the laser energy

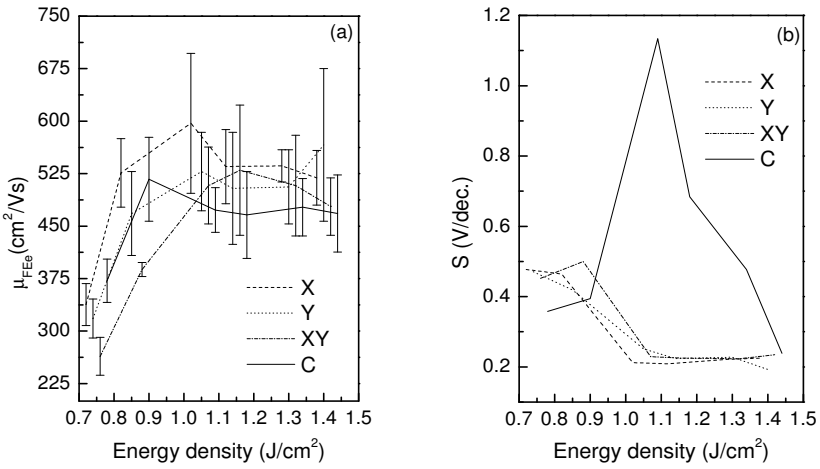


Figure 2.12: (a) Average $\mu_{\mathrm{FE,e}}$ and (b) average $S$ value of SG Si TFTs with a 250 nm thick Si layer and a 120 nm thick ECR-PECVD $SiO_2$ gate insulator as functions of the crystallization energy density. The curves correspond to different channel positions with respect to the grain filter.

density for each position of the SG Si TFT with ECR-PECVD $SiO_2$ as gate insulator. At low energy densities the *C* position gives the highest $\mu_{\mathrm{FE,e}}$ as the grain size is not large enough to cover the channel for other positions at such energy densities, while saturation of $\mu_{\mathrm{FE,e}}$ occurs at the highest energy density for the *XY* position, as this position is farthest from the grain filter. $\mu_{\mathrm{FE,e}}$ increases with energy density up to a maximum value. This is due to the increased melt depth in the grain filter and hence a decreased number of planar defects (random or CSL twin GBs), which are generated during the crystallization process with higher irradiated energy densities. $\mu_{\mathrm{FE,e}}$ slightly decreases at high irradiated energy densities. This could be due to increased surface or interface roughness. Figure 2.12(b) shows $S$ as a function of the laser energy density for SG Si TFTs with ECR-PECVD $SiO_2$ as gate insulator. A trend similar to $\mu_{\mathrm{FE,e}}$ is observed for $S$ except for the behavior of the TFTs at the *C* position, where an abnormal peak is found at moderate energy densities. This is not well understood but might be attributed to the fact that when the melt depth reaches a void inside the grain filter, the total number

of trap states increases. Similar trends are obtained for $I_{OFF}$ and $V_{TH}$, which both improve with increasing crystallization energy density. It is concluded from the above discussion that SG Si TFT characteristics improve up to an optimum crystallization energy density, as the quality improves and the size of the grain increases. Twin GBs and planar defects are reduced at this optimum crystallization energy density.

### 2.6.3 Effects of Pulse Duration

Increasing the pulse duration of the excimer laser light is expected to have a favorable influence on the crystallized Si film quality [45]. The solidification duration of the molten Si can be increased by using a longer-pulse excimer laser. An elongated solidification of the molten Si leads to a larger grain and a better microstructure [46]. To investigate the effects of using a longer-pulse excimer laser (SOPRA VEL15, pulse duration = 200 ns) for irradiation, n-channel SG Si TFTs with a 250 nm thick Si layer were fabricated at various crystallization energy densities. The above duration is much larger than the standard excimer laser pulse duration (56 ns).

| ***TFTs*** | ***Position*** | $\mu_{FE,e}[cm^2/Vs](\sigma\%)$ | $S[V/dec.](\sigma\%)$ | $V_{TH}[V](\sigma\%)$ |
|---|---|---|---|---|
| SG | *X* | 644±63(9.8%) | 0.20±0.03(15%) | 1.6±0.24(14%) |
| | *Y* | 546±52(9.7%) | 0.25±0.04(15%) | 1.7±0.25(14%) |
| | *XY* | 508±60(12%) | 0.25±0.015(7%) | 2.1±0.09(4%) |
| | *C* | 507±29(6%) | 0.43±0.18(41%) | 1.5±0.34(23%) |
| SOI | | 727±18(2.4%) | 0.18±0.006(3.6%) | 1.1±0.09(8%) |

Table 2.3: Characteristic values of n-channel SG TFTs with a 250 nm thick Si layer and a 120 nm thick ECR-PECVD $SiO_2$ layer as gate insulator, for longer-pulse excimer laser with an energy density of 1.63 J/cm$^2$. The TFT channel was undoped.

Table 2.3 shows the average characteristic values with standard deviation for n-channel SG TFTs with a 250 nm thick Si layer and a 120 nm thick ECR-PECVD $SiO_2$ layer as gate insulator for various positions inside a location-controlled grain. The crystallization energy density of the long-pulse excimer laser was 1.63 J/cm$^2$. The characteristic values clearly show that the $\mu_{FE,e}$ value is higher for SG Si TFTs fabricated using a long-pulse laser than a short-pulse laser. This is attributed to the fact that the long-pulse excimer laser

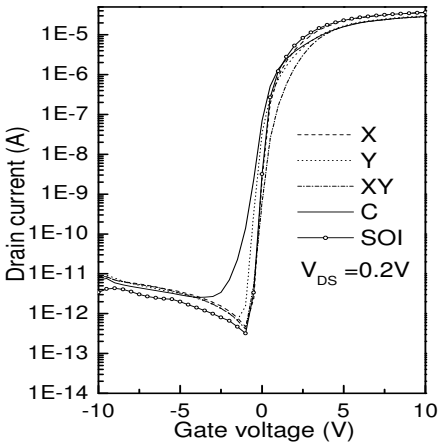


Figure 2.13: $I_{DS}$-$V_{GS}$ characteristics for various TFT positions in the location-controlled grain for n-channel SG TFTs with a 250 nm thick Si layer and a 120 nm ECR-PECVD $SiO_2$ layer as gate insulator, fabricated with a long-pulse excimer laser. The energy density of the excimer laser was 1.63 J/cm$^2$. The TFT made with SOI wafer is also plotted as a reference.

creates crystallized films with a better microstructure because heat conduction to the substrate is slow during solidification and hence the solidification time is long.

Figure 2.13 shows the transfer characteristics of SG TFTs with a 250 nm thick Si layer and a 120 nm thick ECR-PECVD $SiO_2$ layer as gate insulator at various positions. The energy density of the excimer laser was 1.63 J/cm$^2$. It is obvious from the transfer characteristics of the TFTs that channel position effects are still present, and that a shift along the direction of current flow (i.e., *X* shift) gives the highest on-current and the best *S* value. However, channel position effects are less pronounced than in TFTs crystallized with a short-pulse excimer laser. The improved characteristics of the TFT in position *C* are attributed to the improved Si quality in the grain filter, as the melt depth is increased by using a long-pulse laser. Thus crystallization with a long-pulse laser produces fewer twin boundaries and planar defects inside the grain than crystallization with a short-pulse laser.

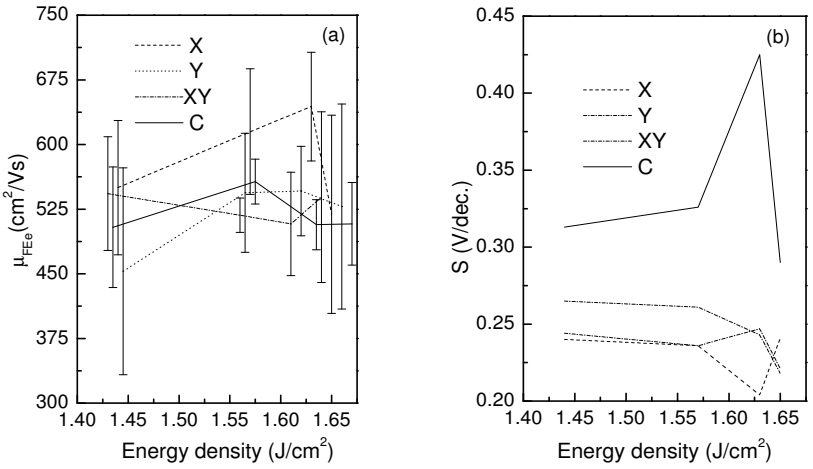


Figure 2.14: (a) Average $\mu_{\mathrm{FE,e}}$ and (b) average $S$ value of SG TFTs with a 250 nm thick Si layer and a 120 nm thick ECR-PECVD $SiO_2$ gate insulator as functions of the energy density. The curves correspond to different channel positions with respect to the grain filter. The TFTs were fabricated using a long-pulse excimer laser.

Figure 2.14 shows the average $\mu_{\mathrm{FE,e}}$ and $S$ values as functions of the laser energy density for each position of the SG Si TFTs fabricated with a long-pulse laser. The same trends are seen as for a short-pulse excimer laser, with improved $\mu_{\mathrm{FE,e}}$ and $S$ values. This again favors the conclusion that Si crystallized with a long-pulse laser has a better microstructure than Si crystallized with a short-pulse laser.

### 2.6.4 Effects of Silicon Thickness

The quality and size of the grain depend very much on the thickness of the Si film [47]. It was demonstrated that the lateral growth of the Si grain is limited by the heat stored in the molten Si, which decreases with decreasing Si thickness. Hence the grain size decreases for thinner Si films. Moreover, the number of planar defects inside the grain is higher in thin Si films because of the increased solidification rate of the molten Si.

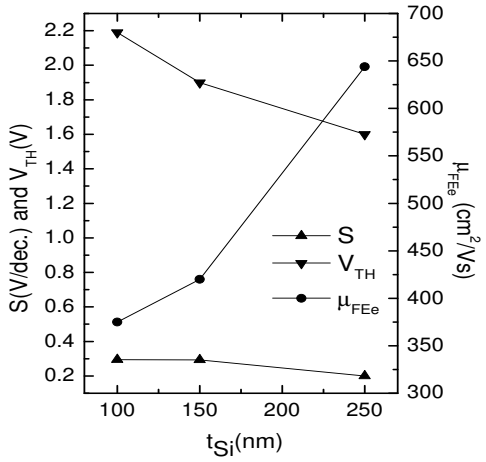


Figure 2.15: $S$, $V_{\mathrm{TH}}$, and $\mu_{\mathrm{FE,e}}$ of SG Si TFTs with an ECR-PECVD $SiO_2$ (120 nm) gate insulator as functions of the Si thickness for the $X$ position of the channel with respect to the grain filter. TFTs were produced with a longer pulse duration.

SG Si TFTs with 100, 150, and 250 nm thick Si layers crystallized with a long-pulse (200 ns) excimer laser were fabricated to investigate the effects of Si thickness on the characteristic values. The thickness of the ECR-PECVD $SiO_2$ gate insulator was 120 nm in each case. Figure 2.15 shows $S$, $V_{\mathrm{TH}}$, and $\mu_{\mathrm{FE,e}}$ as functions of the Si thickness. $\mu_{\mathrm{FE,e}}$ decreases and $S$ increases with decreasing Si thickness. This degradation is attributed to the fact that the total number of defects inside the grain increases for decreasing Si thickness. The numerical value of $S$ is given by Eq. (1.9). It can be modified as following;

$$S = \frac{kT}{q} \ln 10 \left( 1 + \frac{qN_{\mathrm{bt}}t_{\mathrm{Si}} + qD_{\mathrm{it}}}{C_{\mathrm{ox}}} \right), \tag{2.2}$$

where $C_{\mathrm{depl}} = qN_{\mathrm{bt}}t_{\mathrm{Si}}$, $C_{\mathrm{it}} = qD_{\mathrm{it}}$, $N_{\mathrm{bt}}$ is the bulk trap state density per unit volume, $t_{\mathrm{Si}}$ is the thickness of Si, and $C_{\mathrm{ox}}$ is the gate oxide capacitance per unit area. An increase in $S$ suggests that $N_{\mathrm{bt}} \times t_{\mathrm{Si}}$ increases although $t_{\mathrm{Si}}$ decreases. This means that $N_{\mathrm{bt}}$ increases significantly with decreasing $t_{\mathrm{Si}}$. This conclusion is also supported by the observation that $V_{\mathrm{TH}}$ increases with decreasing Si film

thickness.

## 2.7 P-Channel Single-Grain TFTs

N-channel SG Si TFTs fabricated using the µ-Czochralski process show high performance. To realize any digital or analog circuits, p-channel SG Si TFTs should also have high performance. In this section we discuss the performance of p-channel SG Si TFTs.

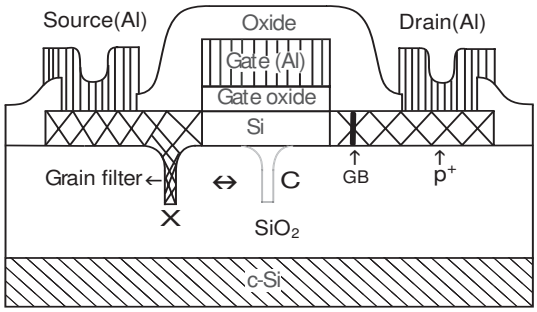


Figure 2.16: Schematic structure of a p-channel SG Si TFT fabricated inside a location-controlled grain with different channel positions.

Figure 2.16 shows the schematic structure of a p-channel SG Si TFT fabricated inside a location-controlled grain at various channel positions. The channel length and width are the same as for the n-channel SG Si TFT, 1.87 µm and 2.03 µm, respectively. We used the same SG TFT design as presented in Section 2.3.

### 2.7.1 Effects of Channel Position

As shown in Section 2.6.1, the performance of an n-channel SG Si TFT improves dramatically by positioning the channel (i.e. direction of current flow) parallel to the planar defects inside a location-controlled grain. It is expected that the performance of p-channel SG TFTs is also improved by positioning the channel of the TFT parallel to the planar defects. To investigate the effects of the channel position inside a location-controlled grain for p-channel SG Si TFTs, a TFT design similar to that shown in Figure 2.3 was used.

Table 2.4 shows the average characteristic values with standard deviation for p-channel SG TFTs with a 250 nm thick Si layer and an 80 nm thick

| *Position* | $\mu_{FE,h}[cm^2/Vs](\sigma\%)$ | $S[V/dec.](\sigma\%)$ | $V_{TH}[V](\sigma\%)$ |
|---|---|---|---|
| *X* | 273±27(11%) | 0.14±0.04(24%) | $-2.2 \pm 0.38$(17%) |
| *Y* | 202±26(13%) | 0.15±0.02(21%) | $-2.3 \pm 0.52$(24%) |
| *XY* | 219±44(20%) | 0.18±0.02(8%) | $-3.36 \pm 0.58$(23%) |
| *C* | 228±22(10%) | 0.16±0.03(16%) | $-3.3 \pm 0.64$(25%) |

Table 2.4: Characteristic values of p-channel SG TFTs with a 250 nm thick Si layer and an 80 nm thick ECR-PECVD $SiO_2$ layer as gate insulator. The energy density of the short-pulse excimer laser was 1.025 J/cm$^2$. The TFT channel was undoped.

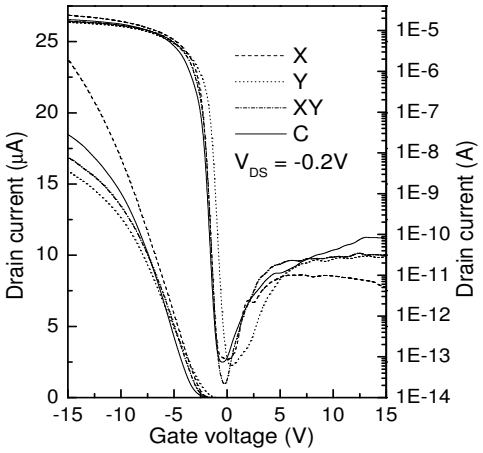


Figure 2.17: $I_{DS}$-$V_{GS}$ characteristics for various TFT positions in the location-controlled grain for p-channel SG Si TFTs with a 250 nm thick Si layer and an 80 nm thick ECR-PECVD $SiO_2$ layer as gate insulator, fabricated using a short-pulse excimer laser.

ECR-PECVD $SiO_2$ layer as gate insulator. Data in Table 2.4 show that SG Si TFTs at the *X* position have the highest $\mu_{FE,e}$ values. The higher $\mu_{FE,e}$ value (273 cm$^2$/Vs) for p-channel SG Si TFTs at the *X* position is attributed to the fact that carriers are not impeded by the twin boundaries because the latter

are parallel to the direction of current flow. Nevertheless there is only a slight improvement in the $S$ value. The above results demonstrate that electrons are more sensitive to planar defects than holes.

Figure 2.17 shows the transfer characteristics for each channel position of p-channel SG Si TFTs with a 250 nm thick Si layer and an 80 nm thick ECR-PECVD $SiO_2$ layer as gate insulator. These samples were crystallized with a short-pulse excimer laser at an energy density of 1.025 J/cm$^2$. By shifting the channel position from the top of the grain filter ($C$), the transfer characteristics were improved.

### 2.7.2 Effects of Crystallization Energy Density

The performance of SG Si TFTs strongly depends on the crystallization energy density, as the grain size and quality both depend on it. P-channel SG Si TFTs were fabricated with various crystallization energy densities to investigate its effects on the electrical characteristics.

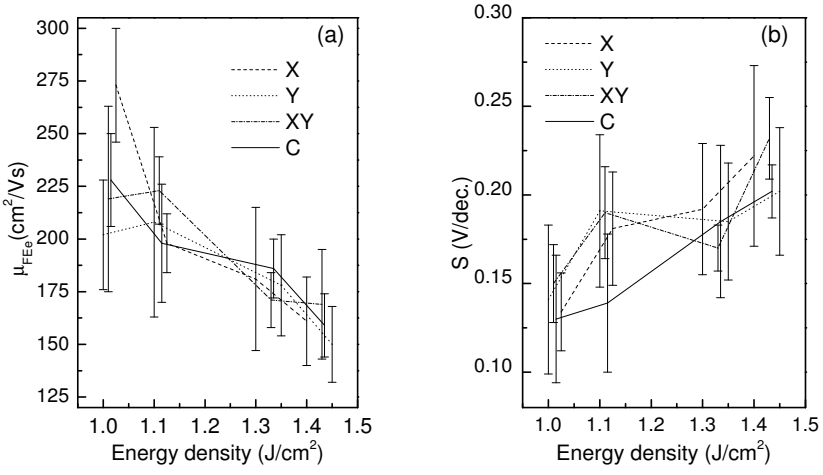


Figure 2.18: (a) Average $\mu_{\mathrm{FE,e}}$ and (b) average $S$ value of SG Si TFTs with a 250 nm thick Si layer and an 80 nm thick ECR-PECVD $SiO_2$ gate insulator as functions of the crystallization energy density of the short-pulse laser. The curves correspond to different channel positions with respect to the grain filter.

Figure 2.18(a) shows the average $\mu_{FE,e}$ of a p-channel SG Si TFT as a function of the laser energy density for various channel positions for TFTs with an 80 nm thick ECR-PECVD $SiO_2$ layer as gate insulator. The highest $\mu_{FE,e}$ value was obtained at the same energy density as for n-channel SG Si TFTs. This is advantageous for the fabrication of high performance CMOS circuits designed with SG Si TFTs. SG Si TFTs designed at the *X* position have the highest $\mu_{FE,e}$ value, as the flow direction of the carriers is parallel to the orientation of planar defects inside the grain. Nevertheless $\mu_{FE,e}$ slightly decreases at higher energy densities. This might be due to an increase in the surface roughness. This behavior of the p-channel SG Si TFT is similar to its counterpart, the n-channel SG Si TFT.

Figure 2.18(b) shows the average *S* value as a function of the laser energy density for different channel positions in p-channel SG Si TFTs with an 80 nm thick ECR-PECVD $SiO_2$ layer as gate insulator. A trend similar to $\mu_{FE,e}$ is observed for *S*, which also increases after an optimum crystallization energy density. However, no significant improvement in *S* is offered by shifting the channel position in various directions with respect to the current flow. This is not well understood but might be attributed to the fact that in the subthreshold regime carriers in p-channel SG Si TFTs are not too much influenced by the nature of planar defects inside the grain. Similar trends are obtained for $I_{OFF}$ and $V_{TH}$, which both degrade slightly with increasing laser energy density.

### 2.7.3 Effects of Channel Doping

To operate any CMOS circuit at low supply voltage, it is important to keep $V_{TH}$ near zero for both (n- and p-channel) TFTs. P-channel SG Si TFTs fabricated with an ECR-PECVD $SiO_2$ gate insulator have a very high (negative) $V_{TH}$. To control the $V_{TH}$ value of p-channel SG Si TFTs, the channel was implanted with boron.

For a 250 nm thick Si layer, the channel boron-implantation dose was varied between $2.5 \times 10^{11}\,cm^{-2}$ and $2.5 \times 10^{12}\,cm^{-2}$. Figure 2.19 shows the effects of channel boron implantation on the characteristic values of p-channel SG Si TFTs. As the doping concentration increases, the conductivity of the bulk Si also increases. The increased conductivity of the channel region gives rise to a degradation in $I_{OFF}$, while the slight degradation in $\mu_{FE,e}$ is due to increased impurity scattering in the channel region.

On the other hand, as shown in Figure 2.20, $V_{TH}$ approaches to zero with increasing channel boron-implantation dose. However, there is a significant degradation in *S* with increasing doping concentration. The degradation of *S* is attributed to the fact that some field lines originating from the gate terminate

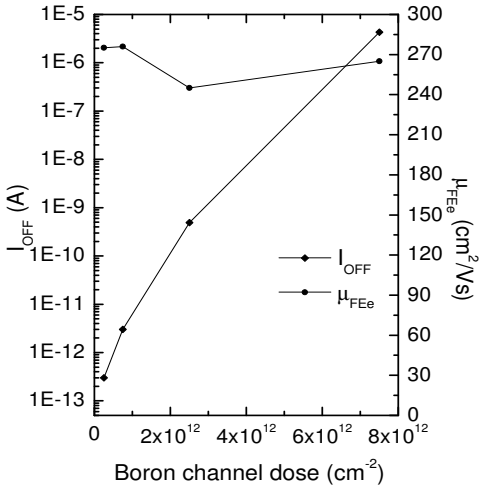


Figure 2.19: Effects of boron channel implantation on $\mu_{\mathrm{FE,e}}$ and $I_{\mathrm{OFF}}$ in p-channel SG Si TFTs.

on acceptor ions and hence reduce the number of accumulated holes at the interface. The channel boron-implantation dose should therefore be as low as possible to get better subthreshold characteristics for the SG Si TFTs. $V_{\mathrm{TH}}$ can be controlled by employing different low-temperature oxide that has low levels of fixed charges.

### 2.7.4 Effects of Silicon Thickness

It was mentioned in Section 2.6.4 that the performance of n-channel SG Si TFTs decreases with decreasing Si thickness, as the total number of defects inside a location-controlled grain increases. These defects have an adverse effect on the characteristics of n-channel SG Si TFTs.

The performance of p-channel SG Si TFTs with 100 nm and 250 nm thick Si layers were analyzed to investigate the effects of Si thickness. The thickness of the ECR-PECVD $SiO_2$ gate insulator was 80 nm in each case. The characteristic values ($S$, $V_{\mathrm{TH}}$, and $\mu_{\mathrm{FE,e}}$) of the p-channel SG Si TFTs with different Si thickness values are tabulated in Table 2.5. $\mu_{\mathrm{FE,e}}$ decreases and $S$ increases with decreasing Si thickness. These are attributed to the fact that the total number of defects inside the grain increases for decreasing Si thick-

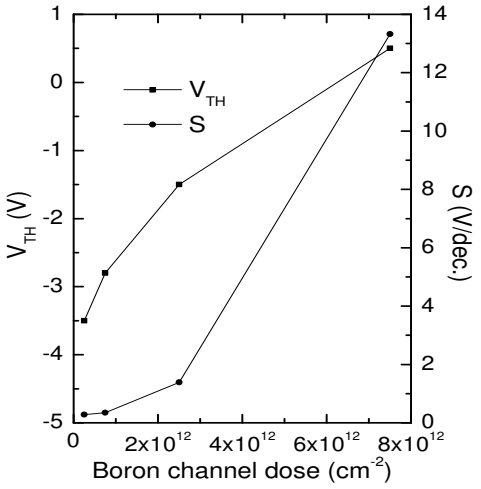


Figure 2.20: Effects of channel boron implantation on $V_{\mathrm{TH}}$ and $S$ in p-channel SG Si TFTs.

| ***Si thickness [nm]*** | $\mu_{FE,h}$ ***[cm²/Vs]*** | ***S [V/dec.]*** | $V_{TH}$ ***[V]*** |
|---|---|---|---|
| 250 | 273 | 0.14 | −2.2 |
| 100 | 114 | 0.22 | −1.7 |

Table 2.5: Characteristic values of p-channel SG Si TFTs with an 80 nm thick ECR-PECVD $SiO_2$ layer as gate insulator for different Si thicknesses.

ness. As specified in Eq. (2.2), $S$ is proportional to $N_{\mathrm{bt}} \times t_{\mathrm{Si}}$. The increase in $S$ suggests that $N_{\mathrm{bt}} \times t_{\mathrm{Si}}$ increases although $t_{\mathrm{Si}}$ decreases. This means that $N_{\mathrm{bt}}$ increases significantly with decreasing $t_{\mathrm{Si}}$. This conclusion has already been drawn for n-channel SG Si TFTs, which also exhibit the same trends in the characteristics.

## 2.8 Effects of Post-Process Annealing

Crystallized bulk Si and its interface with a low-temperature oxide have trap states, and this affects the electrical properties of TFTs adversely. These trap

states can be passivated either by vacuum annealing or hydrogenation. Post-process vacuum annealing of SG Si TFTs was done in a PECVD furnace at 350°C for 45 minutes in ambient $N_2$. Post-process vacuum annealing can also improve the contact resistance between Si and Al.

### 2.8.1 N-Channel Single-Grain TFTs

N-channel SG Si TFTs with a 250 nm thick Si layer and an 80 nm thick ECR-PECVD $SiO_2$ layer as gate insulator were treated with post-process vacuum annealing for 45 minutes. Figures 2.21 and 2.22 show the effects of post-process annealing on $\mu_{\mathrm{FE,e}}$, $S$, $V_{\mathrm{TH}}$, and $I_{\mathrm{OFF}}$ for n-channel SG Si TFTs. Post-process annealing improves $\mu_{\mathrm{FE,e}}$ significantly for all channel positions inside the grain. The same trends are obtained for $S$, $V_{\mathrm{TH}}$, and $I_{\mathrm{OFF}}$, although $S$ and $I_{\mathrm{OFF}}$ increase for TFTs fabricated on top of the grain filter ($C$). The decrease in $S$ and $I_{\mathrm{OFF}}$ for $X$, $Y$, and $XY$ channel positions indicate a quality improvement both in bulk Si and at the interface between Si and $SiO_2$. The degradation of $S$ and $I_{\mathrm{OFF}}$ for the $C$ channel position indicates that there are bulk defects inside the grain filter that become dominant only after annealing, as before annealing they are screened by interface defects.

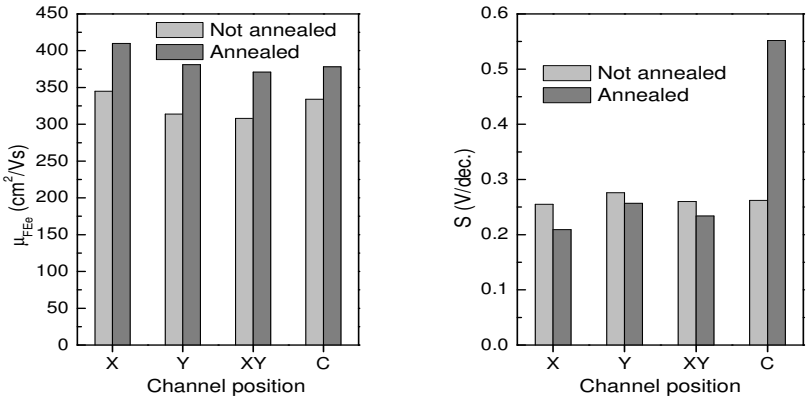


Figure 2.21: Effects of post-process annealing on $\mu_{\mathrm{FE,e}}$ and $S$ for n-channel SG Si TFTs.

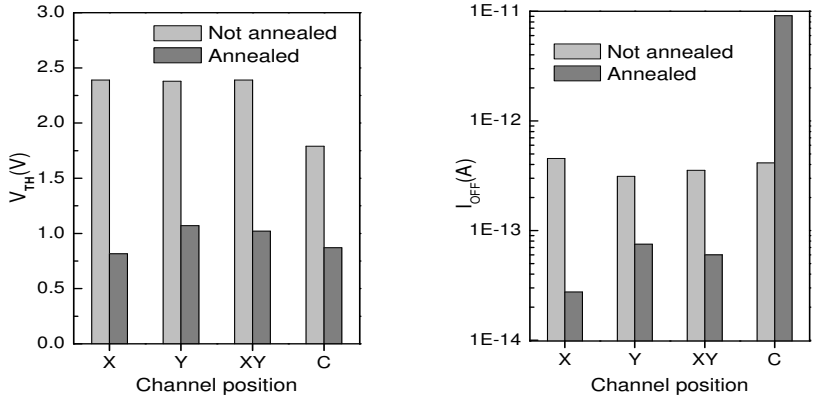


Figure 2.22: Effects of post-process annealing on $V_{\mathrm{TH}}$ and $I_{\mathrm{OFF}}$ for n-channel SG Si TFTs.

### 2.8.2 P-Channel Single-Grain TFTs

To investigate the effects of post-process annealing, p-channel SG Si TFTs with a 250 nm thick Si layer and an 80 nm thick ECR-PECVD $SiO_2$ layer as gate insulator were treated with post-process vacuum annealing for 45 minutes.

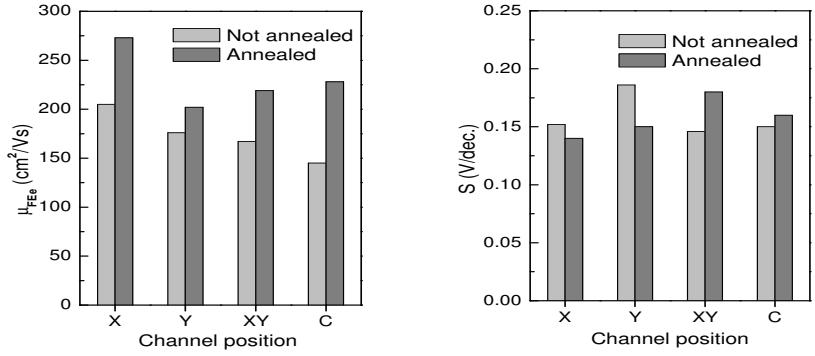


Figure 2.23: Effects of post-process annealing on $\mu_{\mathrm{FE,e}}$, and $S$ for p-channel SG Si TFTs.

Figure 2.23 and 2.24 show the effects of post-process annealing on $\mu_{FE,e}$, $S$, $V_{TH}$, and $I_{OFF}$ for p-channel SG Si TFTs. The increase in $\mu_{FE,e}$ for all channel positions indicates an improvement in both the bulk properties of Si and the contact resistance between Si and Al. The value of $S$ is only slightly changed by vacuum annealing. The same trends were obtained for $V_{TH}$ and $I_{OFF}$ as for $S$ in p-channel SG Si TFTs.

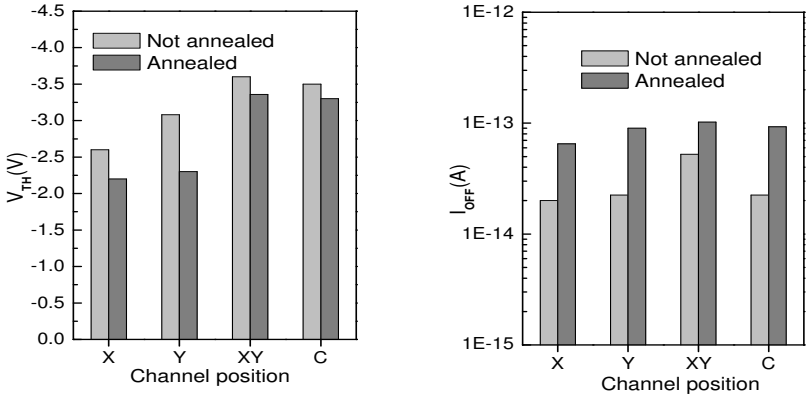


Figure 2.24: Effects of post-process annealing on $V_{TH}$ and $I_{OFF}$ for p-channel SG Si TFTs.

## 2.9 Conclusion

In this chapter the dependence of the characteristics of SG Si TFTs on the channel position inside a location-controlled grain was investigated for both (n- and p-channel) types of SG Si TFTs. For n-channel SG Si TFTs with a 250 nm thick Si layer, $\mu_{FE,e}$ dramatically improved (from 471 cm$^2$/Vs to 597 cm$^2$/Vs) by positioning the current direction parallel to the planar defects radially grown from the grain filter. This is because planar defects – mainly CSL twin GBs – are parallel to the current flow direction in the TFT and hence do not impede the motion of carriers. Furthermore, by avoiding the channel from the grain filter, $S$ is also dramatically improved (from 1.1 V/dec. to 0.2 V/dec.). This suggests that there is a high defect trap density in the grain filter. However, SG Si TFTs crystallized with long-pulse excimer lasers have

higher $\mu_{FE,e}$ values (644 $cm^2/Vs$) than those crystallized with a short-pulse excimer laser. This suggests that Si crystallized with long-pulse excimer lasers has a better microstructure because heat conduction to the substrate is slow during solidification and hence the solidification rate is low.

In p-channel SG Si TFTs with a 250 nm thick Si layer, $\mu_{FE,e}$ also improves (from 228 $cm^2/Vs$ to 273 $cm^2/Vs$) by positioning the current direction parallel to the planar defects radially grown from the grain filter. Nevertheless no significant improvement in $S$ is achieved by avoiding the channel from the grain filter. P-channel SG Si TFTs with ECR-PECVD $SiO_2$ as gate insulator showed high (negative) $V_{TH}$. This was controlled by the optimum amount of boron implantation in the channel. $I_{OFF}$ and $S$ degrade for excessive amounts of boron in the channel. The characteristic values of both types (n- and p-channel) of TFTs degrade with decreasing Si film thickness. This is attributed to the fact that more twin GBs are formed in thin Si films during crystallization, as the total amount of heat in Si decreases, and hence the solidification rate increases.

Finally, the characteristic values of SG Si TFTs are improved by post-process vacuum annealing. However, the performance of n-channel SG Si TFTs at channel position $C$ degrades after post-process vacuum annealing. This is due to the bulk defects inside the grain filter.

# Chapter 3

# Electrical Reliability and Conduction Mechanism in Single-Grain Si TFTs

*The first part of this chapter deals with the electrical reliability of SG Si TFTs under hot carrier stress and high gate bias stress. SG Si TFTs offer higher reliability than poly-Si TFTs because of the absence of high-angle GBs inside the channel of the TFT. When negative gate bias stress is applied, SG TFTs show a hump in the subthreshold characteristics because carriers are trapped at the edge of the channel, whereas they are stable against positive gate bias stress. The second part of this chapter investigates the carrier transport mechanisms inside SG TFTs. Negative activation energy supports the idea that carrier transport inside the channel of the SG TFT is due to acoustic phonon scattering rather than thermionic emission. This distinguishes SG Si TFTs from poly-Si TFTs.*

## 3.1 Introduction

The performance of low-temperature SG Si TFTs is almost as high as that of SOI transistors. Due to their high performance and low-temperature process, SG TFTs are widely expected to be applicable in areas like system circuits (CPU, memory), active matrix LCDs, 3D ICs, DRAMs, EEPROMs, and TFT OLEDs. The realization of integrated systems on panel with SG TFTs re-

quires not only high performance but also high electrical reliability. At a high level of integration, long-term reliability of SG TFTs will be an important issue because of the miniaturization of the channel dimension of the transistors. The reliability of SG Si TFTs has not yet been tested under electrical stress, therefore this research focuses on the investigation of the electrical reliability of SG Si TFTs. Hot carrier effects are the most common phenomena to occur in TFTs when the supply voltage is relatively high [48]. They lead to floating body effects such as the kink effect, hysteresis, or even device breakdown. In the "on" state of the SG Si TFT the CSL twin GB traps capture the carriers, giving rise to a slight reduction of the carrier mobility, as discussed in Chapter 2. In the "off" state the boundary traps might assist carrier generation in the depletion layer that can lead to an increase in the leakage current. At high gate electric fields, carrier trapping and de-trapping might occur in the gate insulator of the TFT. This gives rise to defect formation at the interface ($Si/SiO_2$).

The first part of the chapter deals with the reliability of n- and p-channel SG Si TFTs tested under electrical stress by applying a voltage at the drain or gate electrode and keeping the other electrodes at ground potential. A drain stress voltage causes hot carrier generation, while a gate stress voltage is expected to enhance the trapping of carriers in the gate insulator.

In the second part of the chapter the conduction mechanisms inside a SG Si TFT are investigated. It is well established in the literature that phonon scattering of carriers is responsible for conduction in single-crystalline Si MOSFETs [26]. However, thermionic emission over the potential barrier is the main mechanism in poly-Si TFTs which have random GBs inside the channel of the TFT [49]. Conduction in SG Si TFTs is expected to be dominated by phonon scattering as there are no high angle random GBs inside the channel. To specify the dominant conduction mechanism, the thermal behavior of SG Si TFTs is analyzed.

## 3.2 Electrical Degradation Mechanisms

**Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs)**

The reliability of any integrated circuit depends on the capability of individual transistors to withstand the electric field in the channel of the transistor.

Figure 3.1 shows the schematic diagram of impact ionization due to a high lateral electric field in a n-channel bulk MOSFET. When a high drain voltage is applied, electrons in the channel gain enough energy to cause an avalanche

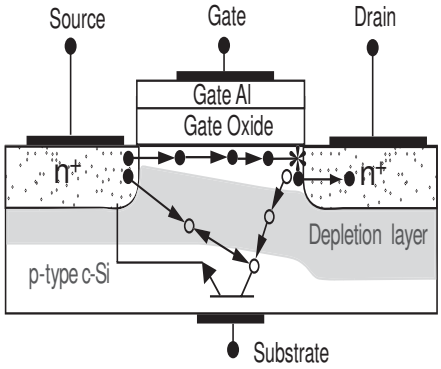


Figure 3.1: Hot carrier effect in an n-channel MOSFET.

breakdown at the drain. These high-energy electrons as well as some of the electron-hole (e-h) pairs generated by impact ionization might be injected into the gate oxide depending on the acquired energy and the gate-drain voltage. To reach the gate oxide, the acquired energy of the electron must be higher than the height of the oxide barrier height (3.2 eV) [50]. Lower-energy electrons are swept to the drain, whereas the generated holes are directed to the lowest potential terminal, i.e., the substrate, and accumulate there. The accumulated holes increase the potential of the substrate, which, in turn, reduces the barrier at the source junction, and a hole current flows into the source. This hole current makes the source-substrate p-n diode forward biased, so now electrons are also injected as minority carriers into the p-type substrate. These electrons arrive at the drain and create further e-h pairs through avalanche multiplication. The positive feedback between avalanche breakdown and parasitic bipolar transistor (PBT, i.e., n-p-n) action gives rise to transistor breakdown at lower drain voltages. As a result of the PBT action, the transistor shows a high drain current, generally called the *kink current*.

The hot carrier effect is less pronounced in p-channel MOSFETs than in n-channel transistors, simply because the mobility, mean free path, energy, and ionization rate are substantially lower for holes than for electrons. Moreover, there is no PBT (p-n-p) action due to the lower gain. This is why p-channel MOSFETs do not show any kink current [51].

**Silicon-on-Insulator MOSFETs**

Several general reliability issues related to SOI devices have been reported, but the floating body effect [52], the self-heating effect [53], and the edge effect [54] are the most common in SOI technology. Figure 3.2 illustrates the cross section of a n-channel SOI MOS device.

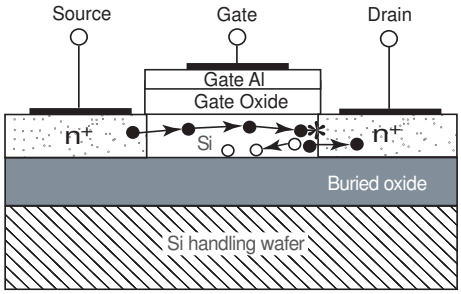


Figure 3.2: Cross section of an n-channel SOI MOSFET.

Hot carrier induced degradation is more complex in SOI devices than in bulk devices because of the existence of two interfaces (two oxides and two channels). The hot carrier effect in SOI devices causes an increase in the body potential. This is known as the *floating body effect* [55]. This is the root of several undesirable effects like the kink effect in the characteristics, the reduction of drain breakdown voltage, etc. Self-heating of thin SOI devices is also a serious problem. It is primarily due to the poor thermal conductivity of the buried $SiO_2$, which acts as a barrier for heat dissipation. It is responsible for the performance degradation in SOI devices: a decrease in $\mu_{FE,e}$ and $V_{TH}$, and an increase in $I_{OFF}$ and $S$, etc. Another important performance limiting factor is the edge effect in SOI devices, which is due to the high electric field at the edge of the channel, since device isolation is generally accomplished by reactive ion etching of the Si layer. This activates the parasitic transistor at a lower $V_{TH}$ and subthreshold characteristics that show a hump [56].

**Poly-Si Thin Film Transistors**

Figure 3.3 shows the cross section of a poly-Si TFT, which has a similar structure to an SOI device apart from some important differences, above all the high defect density by small grains and the random crystal orientation. Poly-Si TFTs show the same hot carrier effects as bulk MOS devices, and the same

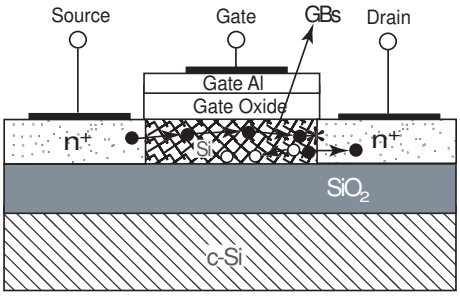


Figure 3.3: Schematic cross-sectional view of an n-channel poly-Si TFT.

floating-boating effects [57], self-heating effects, and edge effects as SOI MOS devices [58]. However, a lower stability is reported for poly-Si TFTs, which is explained in terms of the high density of in-grain and GB defects [59]. The presence of the GB traps enhances avalanche breakdown as well as the kink effect in poly-Si TFTs. Localized defects in bulk poly-Si due to impact ionization increase the surface potential in n-channel poly-Si TFTs and create a high-resistivity region, whereas in p-channel poly-Si TFTs the injection of hot electrons into the gate oxide reduces the effective channel length. This is known as the *channel shortening effect* [60].

Poor properties of the gate insulator and a rough poly-Si/oxide interface give rise to further degradation of TFTs under a high gate electric field, which induces carrier trapping in the gate oxide due to tunneling of electrons into oxide traps at low biases, Fowler-Nordheim injection, and trapping at high bias [61]. Tunneling and trapping are more important in poly-Si TFTs than in MOSFETs and SOI devices because of the poor interface quality. Two types of interface traps might be generated in these processes: (i) donor-like interface traps that are neutral when filled with an electron and positively charged when empty; (ii) acceptor-like traps that are negatively charged when filled with an electron and neutral when empty.

**Single-Grain Si Thin Film Transistors**

Single-grain Si TFTs are designed in such a way that the 2D location-controlled single grain covers the active channel area of the TFT. Figure 3.4 shows the cross-sectional view of a SG TFT, which is very similar to that of an SOI device due to the absence of high-angle random GBs, which are dominant in poly-Si TFTs. However, the presence of CSL twin GBs distinguish SG TFTs

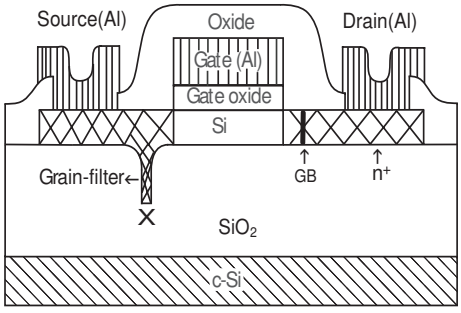


Figure 3.4: Schematic cross-sectional view of an n-channel SG Si TFT inside a location-controlled grain.

from SOI devices. The high performance of SG Si TFTs makes them a suitable candidate for several applications. The reliability of SG Si TFTs would be an important issue for circuit applications. Because of the absence of high-angle random GBs, one expects that the reliability of SG Si TFTs is better than that of poly-Si TFTs. In the next sections we shall investigate the reliability of n- and p-channel SG Si TFTs under different bias conditions. The TFTs are tested under the hot carrier effect, the kink effect, $V_{\mathrm{TH}}$ variations, and high gate bias stress.

## 3.3 Reliability of N-Channel Single Grain Si TFTs

In this section the reliability analysis of n-channel SG Si TFTs is performed under high drain bias stress and high gate bias stress. The characteristics of TFTs show kink effect and $V_{\mathrm{TH}}$ variations under high drain bias, while high gate bias stress creates traps in the oxide layer.

### 3.3.1 Hot Carrier Effect

The hot carrier analysis of n-channel SG Si TFTs was carried out by applying a static stress on the drain junction, varying either the voltage or the stress time, with the two other electrodes connected to the ground. N-channel poly-Si TFTs were also stressed under the same conditions as a reference. Figure 3.5(a) shows the transfer characteristics of an n-channel SG Si TFT with a channel length of 1.87 µm and a channel width of 2.03 µm, subjected to different drain voltage stresses. Crystallization energy density was kept

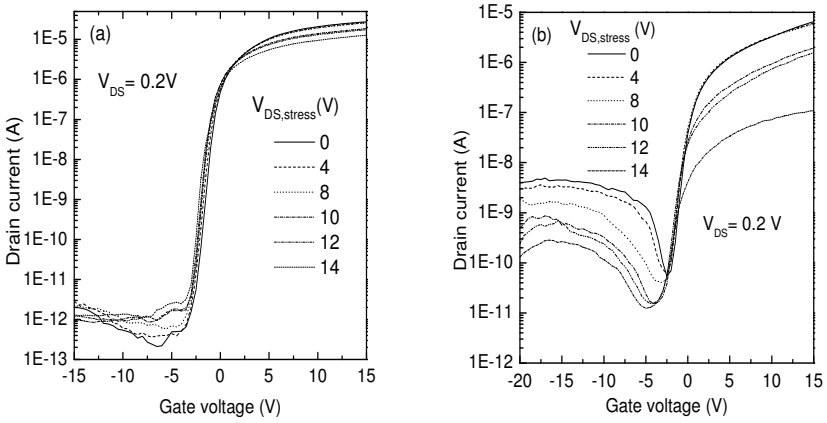


Figure 3.5: Transfer characteristics of n-channel (a) SG Si TFTs and (b) poly-Si TFTs for various drain bias values and a fixed stress time of 300 seconds.

constant at 1.3 J/cm$^2$. The stress time was fixed at 300 seconds. As the stress drain voltage increases, the on-current is slightly degraded, while the subthreshold swing hardly changes. This seems to be caused by the hot carriers which are generated by impact ionization. The hot carriers slightly damage the interface near the drain junction, decreasing the on-current [62].

To compare the endurance of SG Si TFTs with poly-Si TFTs under static stress, reliability tests were also performed on poly-Si TFTs with the same channel dimensions, fabricated by conventional excimer laser crystallization. Figure 3.5(b) shows the transfer characteristics of an n-channel poly-Si TFT for different drain voltage stresses. The stress time was fixed at 300 seconds in this case, too. On-current degradation is caused by hot carriers. In poly-Si TFTs the degradation of the on-current is more severe than in SG Si TFTs. This is due to the enhancement of hot carrier effects by high-angle GBs, as shown in Figure 3.3. These high-angle GBs trap the carriers and form a potential barrier that impedes conduction [59]. Unlike in poly-Si TFTs, no high-angle random GBs are present in the active channel region of SG Si TFTs. This is why SG Si TFTs have better stability characteristics than poly-Si TFTs.

### 3.3.2 The Kink Effect

The major parasitic effects in TFTs are related to the build-up of positive charge due to the accumulation of holes in the substrate, generated by impact ionization at high lateral electric fields. This is generally referred to as the *floating body effect*. One particular consequence of the floating body effect is the kink effect. Figure 3.6(a) shows the output characteristics of an n-channel SG Si TFT; the kink current is indicated at high drain bias. It is similar to SOI devices. The high kink current causes a premature breakdown of such TFTs [57].

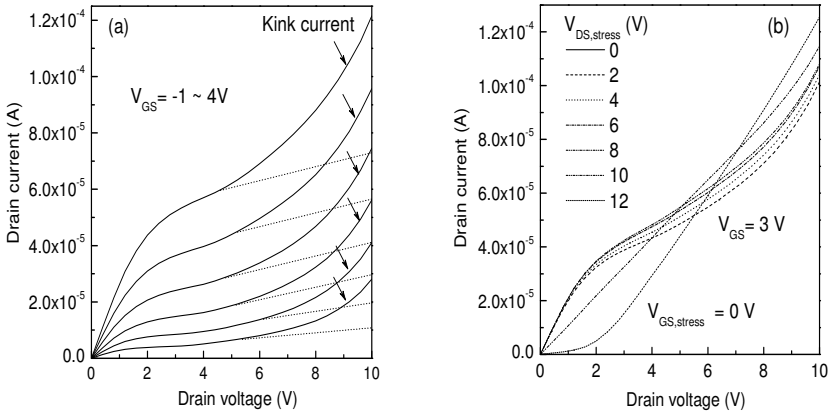


Figure 3.6: (a) Kink effect in the output characteristic of an n-channel SG TFT. (b) Effect of the drain bias stress on the kink current in a SG Si TFT. The channel length is 1.87 µm and the channel width is 2.03 µm.

Figure 3.6(b) shows the effect of the drain bias stress on the kink current in a SG Si TFT. The drain electrode is biased with different voltages (0–12 V) for a fixed time of 300 seconds, whereas the gate and source electrodes are kept at ground potential. The high electric field caused by the drain bias stress enhances impact ionization. As a result, the kink current increases dramatically. Furthermore, at high drain bias stress ($V_{\mathrm{DS,stress}}$ = 12 V), the drain current decreases in the linear regime. The decrease of the linear current is caused by the high-resistivity region near the drain junction created by impact ionization. This kink effect leads to an increased current and transconductance

in the saturation region. It has detrimental effects on circuit applications, especially on analog circuits.

### 3.3.3 Changes in the Threshold Voltage

The threshold voltage $V_{\mathrm{TH}}$ is an important parameter for the operation of a circuit. It is very sensitive to the injection of carriers in the gate oxide as well as the creation of traps by high supply voltages. Changes in $V_{\mathrm{TH}}$ are a measure of device stability. The degradation of TFTs resulting from drain hot carrier injection causes a change in $V_{\mathrm{TH}}$ and the transconductance ($G_{\mathrm{m}}$). Figure 3.7 shows the degradation of $V_{\mathrm{TH}}$ and $G_{\mathrm{m}}$ as functions of the stress time. The severest degradation conditions applied were $V_{\mathrm{GS,stress}} = 5$ V and $V_{\mathrm{DS,stress}} = 12$ V. As the stress time increases, more carriers are generated because of the hot carrier effect, and some of them are injected into the gate oxide to cause a shift in $V_{\mathrm{TH}}$. There is a decrease in the on-current because of the creation of bulk defects by impact ionization [62]. As a result, $G_{\mathrm{m}}$ is degraded, as shown in Figure 3.7(b). As the stress time is prolonged, both bulk and interface defects increase in number. For constant applied stress voltages the shift in $V_{\mathrm{TH}}$ and the change in $G_{\mathrm{m}}$ are proportional to stress time.

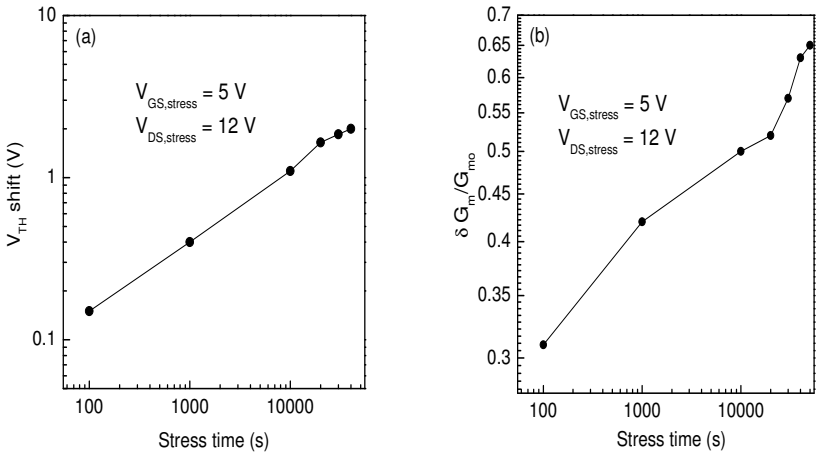


Figure 3.7: Degradation of (a) $V_{\mathrm{TH}}$, and (b) $G_{\mathrm{m}}$ of a SG Si TFT as functions of the stress time.

### 3.3.4 Effects of Crystallization Energy

As mentioned in Section 2.6.2, the performance of SG Si TFTs depends on the crystallization energy density. At low crystallization energy densities the grain size is small. As the crystallization energy density increases, the melt depth in the grain filter and the grain size both increase [47]. For larger melt depths obtained with higher crystallization energies the number of random twin GBs inside the grain decreases. The degradation of SG Si TFTs depends on planar defects and CSL twin GBs in the active channel region of the TFT [59].

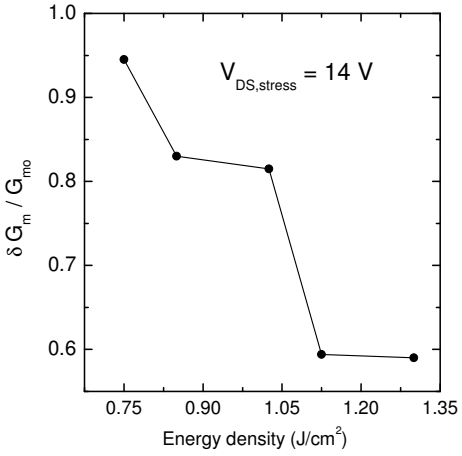


Figure 3.8: Degradation of $G_{\mathrm{m}}$ in a SG Si TFT as a function of the crystallization energy density.

Figure 3.8 shows the degradation of $G_{\mathrm{m}}$ as a function of the crystallization energy density after a strong drain bias stress with 14 V for 300 seconds. This degradation is caused by the hot carrier effect. It is evident that SG Si TFTs degrade faster at low than at high energy densities. This is because a TFT crystallized at low energy density contains a higher number of planar defects and twin GBs inside the grain; they trap hot carriers, building up a potential barrier. At higher crystallization energies SG Si TFTs are more stable, since the grain size and the grain quality both improve with increasing crystallization energy.

### 3.3.5 Effects of High Gate Field Stresses

The development of TFT technology requires high-quality and durable $Si/SiO_2$ interfaces. To study the interface degradation due to vertical electric fields, either a negative or a positive voltage is applied to the gate electrode for a fixed time, while the two other electrodes are kept at zero potential.

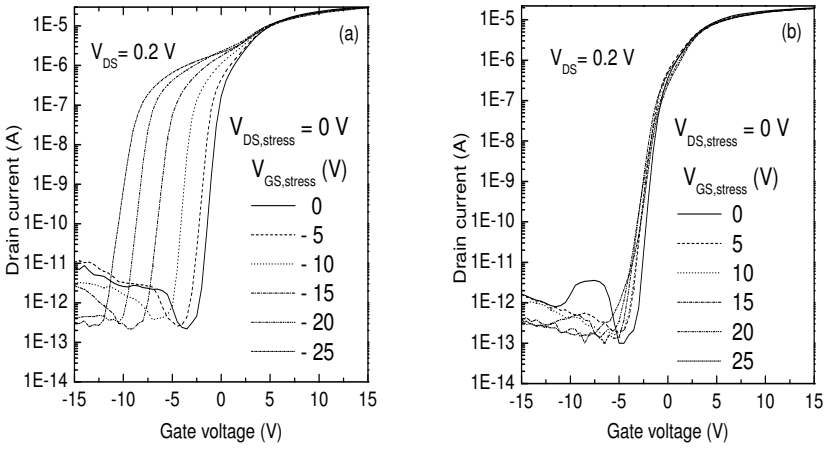


Figure 3.9: Transfer characteristics of an n-channel SG Si TFT for various (a) negative and (b) positive gate bias values and a fixed stress time of 300 seconds.

Figure 3.9(a) shows the subthreshold characteristics of an n-channel SG Si TFT under different negative $V_{GS,stress}$ voltages applied for 300 seconds. Under this stress the TFTs show a peculiar behavior. As the negative $V_{GS,stress}$ increases, a hump appears in the characteristics, whereas the minimum off-current decreases with $V_{GS,stress}$. This is because the electric field is higher at the edges of the rather thick Si island, as the ECR-PECVD $SiO_2$ gate insulator has a low step coverage. The thin gate insulator at the edge enhances the non-uniform trapping of positive charges under negative $V_{GS,stress}$ and triggers an early turn-on of the edge channel (parasitic transistor) [54, 60]. Intolerable consequences include double subthreshold slope and lower pseudo-threshold voltage. The off-current reduction is also related to the reduction of the local electric field. This is due to the presence of positive charges at

the oxide/semiconductor interface that partially screen the negative charges on the gate electrode. The build-up of positive charges in the gate oxide is the consequence of hot-hole injection. This can be summarized as follows: 1) Formation of oxide traps that are positively charged during bias stress; 2) Creation of acceptor-like interface states located in the upper half of the band gap [54].

Figure 3.9(b) shows the transfer characteristics of an n-channel SG Si TFT under various positive $V_{\mathrm{GS,stress}}$ voltages applied for 300 seconds. There is no significant change in $V_{\mathrm{TH}}$, nevertheless the transfer characteristics of the transistor are slightly affected. Hardly any change in the on-current is observed when a high stress voltage ($V_{\mathrm{GS,stress}} = 25$ V) is applied. The degradation in the transfer characteristics is probably not due to electron trapping (which should only give rise to parallel shifts in the $I_{\mathrm{DS}}$-$V_{\mathrm{GS}}$ characteristics) but rather to the generation of some mid-gap defects in the interface or the bulk Si near the Fermi level, since the subthreshold current in TFTs is dominated by such defects [61]. The effects of high gate field stresses on the TFT characteristics can be summarized as follows: 1.) SG TFTs are very stable under positive gate stresses; however 2.) under negative gate stresses they show a hump in the characteristics, caused by the parasitic channel at the side wall of the SG Si TFT.

## 3.4 Reliability of P-Channel Single Grain TFTs

The reliability of p-channel SG Si TFTs is also important for the proper operation of circuits. However, a p-channel TFT is more stable than its counterpart, the n-channel TFT. The reliability of p-channel SG Si TFTs were studied under high $V_{\mathrm{DS,stress}}$ and high $V_{\mathrm{GS,stress}}$, by applying electrical stress on the drain and gate electrodes, respectively.

### 3.4.1 Hot Carrier Effect

The hot carrier effect in p-channel TFTs is less important than in n-channel TFTs as the hole mean free path in Si is about one-half of the electron mean free path, so holes scatter more frequently and fewer of them reach high enough energies to create interface states. The hot carrier analysis of p-channel SG Si TFTs was carried out by applying a static stress for different drain bias stresses for a fixed time.

Figure 3.10(a) shows the transfer characteristics of a p-channel SG Si TFT with a channel width of 2.03 µm and a channel length of 1.87 µm for different

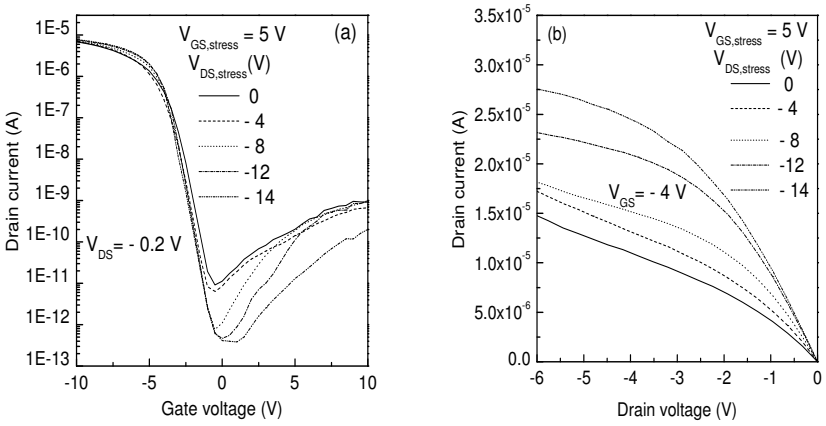


Figure 3.10: (a) Transfer characteristics and (b) output characteristics of a p-channel SG TFT for various drain biases with a fixed stress time of 300 seconds.

$V_{\mathrm{DS,stress}}$ voltages. The stress time was fixed at 300 seconds. An increase in the on-current is clearly seen in the output characteristics shown in Figure 3.10(b), while the off-current decreases as the drain bias stress is increased. Under drain bias stress, the hot electrons trapped in the gate oxide near the drain junction decrease the effective channel length of the p-channel SG Si TFT [60, 63], increase the on-current. The trapped electrons also reduce the electric field near the drain and thus they can significantly reduce the off-current.

### 3.4.2 Effects of High Gate Bias Stresses

A high (negative or positive) $V_{\mathrm{GS,stress}}$ is applied on the gate electrode of a p-channel SG Si TFT for a constant time. Figure 3.11(a) shows the subthreshold characteristics of a p-channel SG Si TFT under different negative $V_{\mathrm{GS,stress}}$ voltages applied for 300 seconds. As the negative stress is increased, both the on-current and the off-current decrease. The decrease in the on-current indicates the creation of trap states at the interface as the subthreshold swing also degrades. The decrease in the off-current suggests the generation of acceptor-like traps due to the high $V_{\mathrm{GS,stress}}$ [61].

Figure 3.11(b) shows the transfer characteristics of a p-channel SG Si TFT

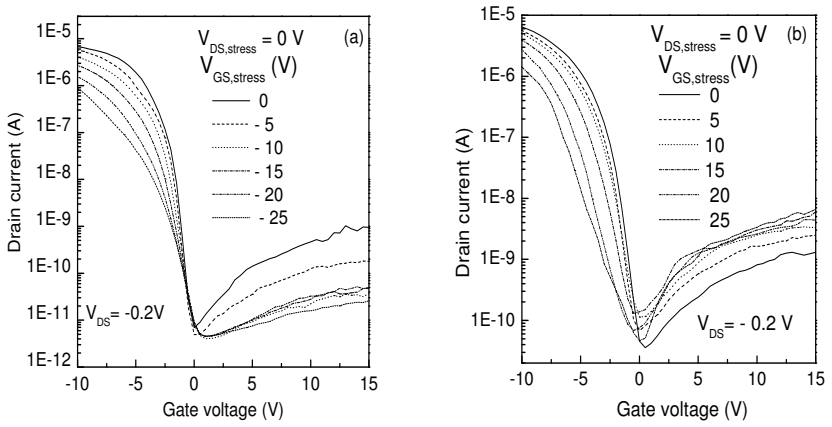


Figure 3.11: Transfer characteristics of a p-channel SG Si TFT for various (a) negative and (b) positive gate biases applied for a fixed stress time of 300 seconds.

under various positive $V_{\mathrm{GS,stress}}$ voltages applied for 300 seconds. The on-current decreases with increasing gate bias stress, and a shift is observed in $V_{\mathrm{TH}}$. On the other hand, the off-current increases with increasing $V_{\mathrm{GS,stress}}$. $V_{\mathrm{TH}}$ and $S$ are closely related to the trap states located near the mid-band gap. The shift in $V_{\mathrm{TH}}$ and the degradation of $S$ indicate the generation of trap states in the mid-band gap. However, the degradation of the on-current is related to the increase in the number of strain bond tail states at the interface [64].

## 3.5 Temperature-Dependent Carrier Transport in TFTs

So far we have studied the electrical reliability of SG Si TFTs. However, it is also important to investigate the temperature-dependent carrier transport mechanisms in these TFTs because temperature modifies the characteristics (especially $I_{\mathrm{OFF}}$) of the TFTs, thereby affecting the operation of the circuits. In the next section we shall discuss the leakage current mechanism in poly-Si TFTs and then turn to the thermal behavior of the SG Si TFTs.

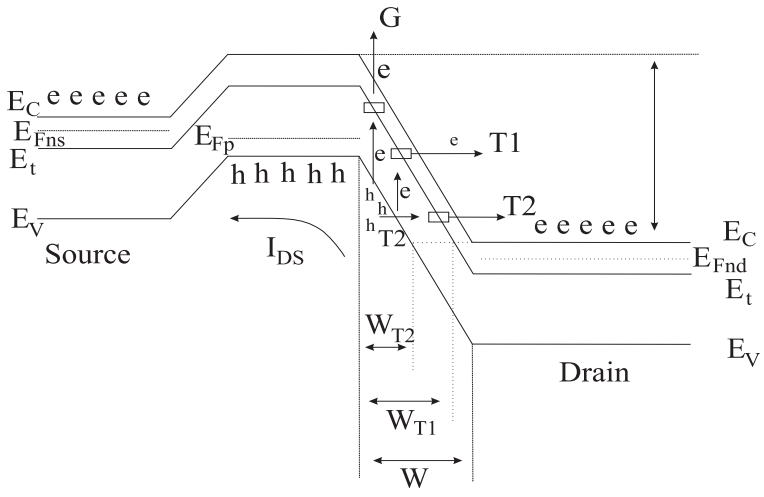


Figure 3.12: Basic band diagram of an n-channel poly-Si TFT with three different leakage current mechanisms (G: thermal-generation current, T1: field-enhanced thermionic current, T2: field-emission current; $E_{\mathrm{Fns}}$: quasi-Fermi level of electron at source, $E_{\mathrm{Fp}}$: quasi-Fermi level of hole, $E_{\mathrm{Fnd}}$: quasi-Fermi level of electron at drain).

### 3.5.1 Temperature-Dependent Leakage Current in Poly-Si TFTs

In conventional poly-Si TFTs, leakage current (also known as the "off-current") arises from the generation-recombination (G-R) of carriers in the depletion region at the drain junction. The leakage current mechanism is strongly related to the nature and density of the gap states in GBs [65, 66]. Figure 3.12 illustrates the energy band diagram of an n-channel poly-Si TFT showing various leakage current mechanisms. Several mechanisms have been proposed including thermal generation-recombination, field-enhanced thermal (Frenkel-Poole) emission, tunneling through the barrier via traps at constant energy, and thermionic field emission (trap-to-band tunneling).

When a negative gate potential is applied to an n-channel TFT, holes accumulate in the channel, and so p-n junctions are formed between the channel and the drain (or source). When a positive potential is applied to the drain, a reverse biased p-n junction is formed between the drain and the channel and a forward biased p-n junction between the source and the channel. When the drain voltage is very low, the leakage current is dominated by thermally

generated carriers, denoted by G in Figure 3.12 [67,68]. This current is caused by the flow of holes in the valance band generated by trapping electrons in GB states. The drain field makes the holes in the valance band flow through the channel and then they recombine with the electrons at the source region. The electrons trapped in the GB states are thermally excited towards the conduction band and drift to the drain. The leakage current therefore depends on the drain voltage but not on the gate voltage. When the drain voltage is in the intermediate range, the leakage current is generated by thermionic field emission of electrons [69], indicated as T1 in Figure 3.12. In this case, the electrons in the valence band are thermally excited to the traps and then tunnel to the conduction band quantum mechanically. Therefore the leakage current increases with the gate voltage because of the decrease in the barrier width (W). If the gate voltage is high enough, the leakage current is governed by field-enhanced tunneling, denoted by T2 in Figure 3.12 [64]. The electrons in the valance band are field assisted to tunnel towards the conduction band via GB traps. The leakage current is therefore independent of temperature as is the tunnelling probability of the carriers.

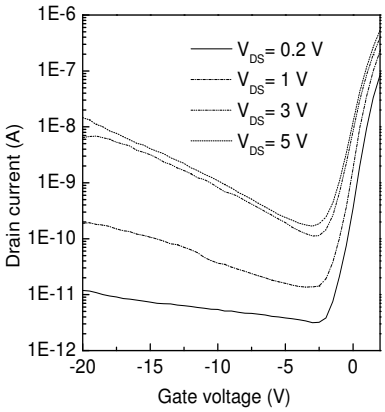


Figure 3.13: Drain current vs gate voltage in an n-channel poly-Si TFT, measured at various drain bias voltages.

Figure 3.13 shows the leakage current of a poly-Si TFT at different drain biases. Thermal generation is seen to be the dominant mechanism at low drain bias, whereas field-enhanced tunnelling becomes more important as the drain

bias increases. In poly-Si TFTs, the temperature dependence of the current of mobile carriers in equilibrium with trapped charges is given by [70];

$$I_{\mathrm{OFF}} = I_0 e^{-E_{\mathrm{a}}/kT}, \tag{3.1}$$

where $I_0$ is a constant independent of temperature and $E_{\mathrm{a}}$ is the drain current activation energy, which measures the difference between the edge of the conduction band and the energy of grain boundary states within $kT$ of the Fermi level. At zero gate bias and low drain bias $E_{\mathrm{a}}$ is expected to be about half the band gap ($E_{\mathrm{g}}/2$), and it is expected to decrease either by increasing or decreasing gate biases [71].

Material properties of SG Si TFTs are very different from those of poly-Si TFTs as there are no high-angle GBs in the channel. In SG Si TFTs the activation energy of the drain current, $E_{\mathrm{a}}$, is expected to be as large as the band gap in Si, $E_{\mathrm{g}}$.

### 3.5.2 Thermal Behavior of N-Channel Single-Grain TFTs

To gain an insight into carrier conduction mechanisms in n-channel SG Si TFTs we performed temperature analysis on the devices. Figure 3.14(a) shows the transfer characteristics of n-channel SG Si TFTs measured at various temperatures between $-10^{\circ}$C and $180^{\circ}$C, over the $-20$ to 20 V gate voltage ($V_{\mathrm{GS}}$) range. At low temperatures the leakage current is dominated by field-enhanced thermionic emission since it depends on $V_{\mathrm{GS}}$ [68]. However, at high temperatures the thermal generation mechanism becomes dominant. As temperature is increased, the threshold voltage decreases as the depletion capacitance increases because of an increase in the intrinsic carrier concentration [72].

Figure 3.14(b) shows the Arrhenius plot of the drain current in n-channel SG Si TFTs. It is clear from the plot that in the off-regime ($V_{\mathrm{GS}} = -20\,\mathrm{V}$) the current increases with decreasing temperature, whereas in the on-regime ($V_{\mathrm{GS}} = 20\,\mathrm{V}$) it decreases with increasing temperature.

The average slope of the curves in the Arrhenius plot gives the potential barrier height or activation energy ($E_{\mathrm{a}}$) in either regime [73]. Figure 3.15(a) shows the activation energy as a function of $V_{\mathrm{GS}}$ for different values of $V_{\mathrm{DS}}$. At $V_{\mathrm{GS}} = 20\,\mathrm{V}$ $E_{\mathrm{a}}$ drops to a negative value ($-0.0019\,\mathrm{eV}$), which does not occur in a typical poly-Si TFT [66]. As shown in the Arrhenius plot, $E_{\mathrm{a}}$ remains negative even at room temperature. The negative value indicates that the bulk trap state density is very low so current transport is governed by acoustic phonon scattering as in MOSFETs [26, 67]. This is consistent with the fact that in a location-controlled grain there are no high-angle random GBs which

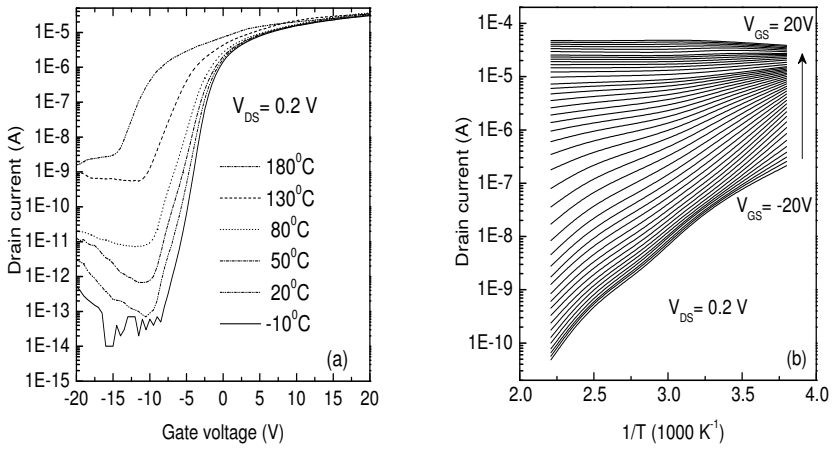


Figure 3.14: (a) Drain current vs gate voltage in an n-channel SG Si TFT, measured at various temperatures. (b) Arrhenius plot of the drain current in an n-channel SG Si TFT at different gate voltages. The average slope of each line gives the activation energy.

would create a potential barrier, and that CSL GBs have negligible effect on the on-state. In the off-regime with moderate gate bias, the $E_{\mathrm{a}}$ value peaks at 0.9 eV, which is close to the band gap value of Si. This suggests that carrier generation centers are not located at mid-gap but close to the band edge; this may be caused by the remaining coherent twin GBs in the location-controlled grain. $E_{\mathrm{a}}$ decreases with decreasing $V_{\mathrm{GS}}$ or increasing $V_{\mathrm{DS}}$, indicating a field-enhanced thermionic emission [74, 75].

Figure 3.15(b) shows the activation energy in the on-state ($E_{\mathrm{a,ON}}$) versus crystallization energy density. As crystallization energy density increases, $E_{\mathrm{a,ON}}$ changes from positive to negative. This suggests that the number of defects creating mid-gap states at low energy densities (e.g., random GBs) is reduced as a result of the high laser energy density, and hence the melt depth becomes larger in the grain filter, enhancing grain selection during growth. Figure 3.16 shows a log-log plot of $\mu_{\mathrm{FE,e}}$ vs temperature for n-channel SG TFTs. For temperatures below 350 K $\mu_{\mathrm{FE,e}}$ decreases with temperature with a slope of $-1.86$, which is very close to the theoretical value of single-

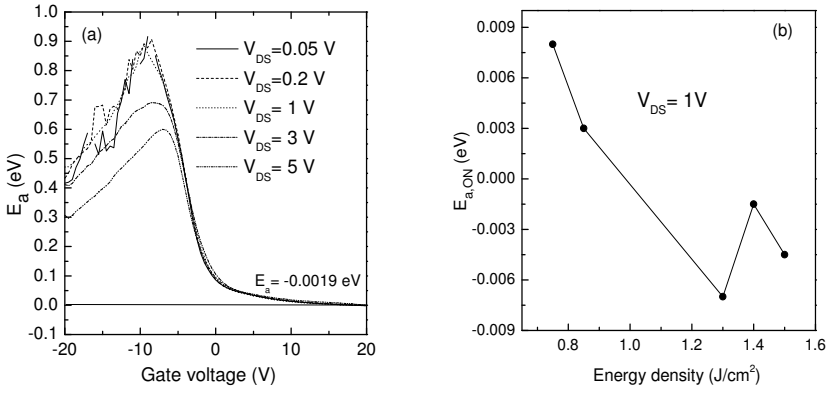


Figure 3.15: (a) Dependence of the potential barrier height on gate and drain voltages for n-channel SG TFTs. (b) The variation of the potential barrier height in the on-regime with crystallization energy density.

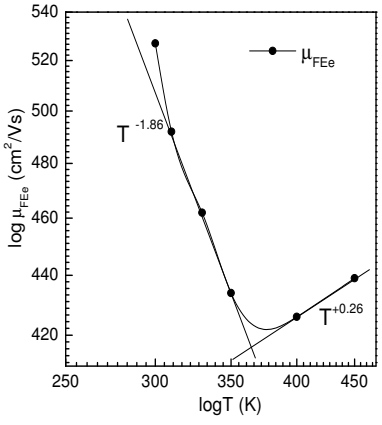


Figure 3.16: Variations of the field-effect mobility of electrons with temperature.

crystalline Si ($-1.5$) [26]. This finding supports the explanation that current transport is governed by acoustic phonon scattering. For temperatures higher than 350 K the observed temperature coefficient of $\mu_{\mathrm{FE,e}}$ is positive. This is due to thermionic emission over the potential barrier at CSL GBs inside the location-controlled grain.

### 3.5.3 Thermal Behavior of P-Channel Single-Grain TFTs

To analyze the thermal behavior of location-controlled p-channel SG Si TFTs, similar measurements were performed as for n-channel SG Si TFTs. Figure 3.17(a) shows the transfer characteristics of p-channel SG Si TFTs measured at various temperatures between 30°C and 190°C, over the $-20$ to 20 V gate voltage ($V_{\mathrm{GS}}$) range. The off-current mechanisms identified in p-channel SG TFTs are similar to those in n-channel devices. At low temperatures the leakage current is dominated by field-enhanced thermionic emission since it depends on $V_{\mathrm{GS}}$. However, at high temperatures the thermal generation mechanism is observed. The activation energy ($E_{\mathrm{a}}$) of the drain current was calculated using the Ar-

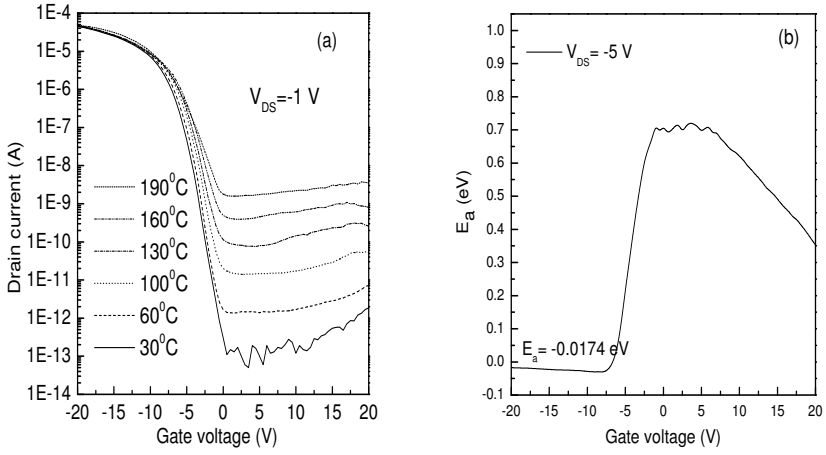


Figure 3.17: (a) Drain current vs gate voltage for a p-channel SG TFT measured at various temperatures. (b) Potential barrier vs gate voltage for a p-channel SG TFT.

rhenius plot. Figure 3.17(b) shows $E_a$ as a function of $V_{GS}$. In the on-regime, $E_a$ drops below zero, which again supports the idea that current transport is dominated by acoustic phonon scattering rather than the potential barrier. Moreover, the height of the potential barrier (0.71 eV) strongly supports the idea that traps are located near the band edge rather than near the mid-band gap.

## 3.6 Conclusion

An electrical stress analysis of SG Si TFTs was performed to determine their endurance. For comparison, poly-Si TFTs with the same physical dimensions were also tested under hot carrier stress. SG Si TFTs showed better stability than poly-Si TFTs due to the absence of high-angle GBs. Both (n- and p-channel) SG Si TFTs were subjected to high gate field stresses. For negative stresses n-channel SG Si TFTs show a hump in the subthreshold characteristics as hot holes are trapped at the side wall of the TFT, reducing the threshold voltage of the side-wall channel, whereas acceptor trap states are generated in p-channel SG Si TFTs. On the other hand, n-channel SG Si TFTs are stable under positive gate field stress and p-channel SG Si TFTs show a significant degradation in the on-current because of the generation of strain band tail states along with mid-band gap defects, which modify $V_{TH}$ and $S$.

Carrier transport mechanisms were investigated in both (n- and p-channel) SG Si TFT types. Both types have a negative activation energy in the on-regime. This strongly supports the idea that carrier transport in SG Si TFTs is governed by acoustic phonon scattering. This distinguishes SG Si TFTs from the poly-Si TFTs, in which it is dominated by the potential barrier.

# Chapter 4

# Digital CMOS Circuits with Single-Grain Si TFTs

*This chapter deals with the performance of digital CMOS circuits realized using SG Si TFTs. Both (n- and p-channel) SG Si TFTs were integrated in a SG CMOS inverter in such a way that the location-controlled single grain covers the channel area of both TFTs. The design and the fabrication process flow of SG CMOS inverters are also discussed. AC and DC characterization of SG CMOS inverters were performed. The propagation gate delay of SG CMOS inverters was estimated using a 101-stage ring oscillator. A result of 0.7 ns was obtained at a supply voltage of 8 V. For the given device condition ($L$ = 1.24 µm) this propagation gate delay is shorter than that of poly-Si circuits.*

## 4.1 Introduction

A growing demand for new TFT applications in microelectronics and large-area electronics has generated an increasing need for high performance TFTs [76]. The past decade has witnessed tremendous research and development efforts toward the realization of high-performance TFTs and circuits based on them. High carrier mobility in poly-Si and long-term device stability have enabled the integration of row and column drive circuitry in AMLCD matrices, and also opened the way for some additional functionalities such as image reversal, aspect ratio control, and level shifting. Furthermore, carrier mobility in poly-Si TFTs has steadily increased over the past years, so much so that the characteristic values of recent TFTs are close to those of single-crystalline Si. In the

previous chapters it was demonstrated that SG (n- and p-channel) Si TFTs show high performance, close to that of SOI transistors at low temperatures ($< 350°C$). It is expected that the degree of circuit integration will continue to increase as SG Si TFTs are implemented in these circuits, so entire systems may soon be formed on a single panel. As systems become more complex, they will require other circuit elements besides displays and circuitry – such as memories, CPUs, solar cells, touch sensors, as well as analog-to-digital and digital-to-analog converters. Smart cards or data cards with simple memory and circuitry, as well as displays and RF communication devices may also be realized with this technology.

This work represents a step forward in these respects, with the development of complementary metal-oxide semiconductor (CMOS) digital circuits (such as inverters and ring oscillators) with SG Si TFTs. This chapters deals with the theory and design of SG CMOS Si TFT inverters, and it also presents the process flow for the fabrication of SG CMOS circuits. Since both (n- and p-) channels are fabricated inside a single grain, such circuits are expected to deliver higher performance than TFTs fabricated using any other present-day low-temperature technology. A ring oscillator was also fabricated using a large number of SG CMOS inverters to determine propagation gate delay.

## 4.2 Poly-Si TFT Circuits by Excimer Laser Crystallization

Excimer laser crystallization of a-Si is a most common technique for realizing low-thermal-budget poly-Si TFTs on an arbitrary substrate. Good quality poly-Si TFTs have been fabricated on insulator substrates from the mid-1990s [77]. During the late 1990s, excimer laser crystallization was used to produce high mobility ($> 100\,\mathrm{cm}^2/\mathrm{Vs}$) TFTs on glass for the first time [78]. Continued efforts in this field yielded devices with mobility values in excess of 200 $\mathrm{cm}^2/\mathrm{Vs}$ and functional digital circuits were fabricated on glass substrates for the first time [79]. The lower carrier mobility in poly-Si TFTs limits their applications in large-area electronics. Significant developments in excimer laser crystallization techniques represented a real breakthrough in materials and process technology. Using the µ-Czochralski process TFTs can be fabricated inside a location-controlled grain (SG TFT) with excimer laser crystallization. Performance values close to those of SOI transistors were obtained with the µ-Czochralski process as there are no high-angle GBs in the SG TFT channel. To explore the feasibility of using SG Si TFTs fabricated using

the μ-Czochralski process in circuits, operating digital circuits made with SG Si TFTs have to be realized first. Inverters are at the core of all digital and analog circuits. Once their operation is clearly understood, the design of more complex circuits is greatly simplified. The operation and theory of CMOS static inverters are explained in the next section.

## 4.3 The Theory of CMOS Static Inverters

Inverters are the simplest logic gates implemented in logic operations. A CMOS static inverter is realized by connecting a p- and an n-device in series, as shown in Figure 4.1. To determine the voltage transfer characteristics of the inverter, the output voltage $V_{\text{out}}$ is measured as a function of the input voltage $V_{\text{in}}$. The operation region of the CMOS inverter can be divided into five parts, as shown in Figure 4.2 [80].

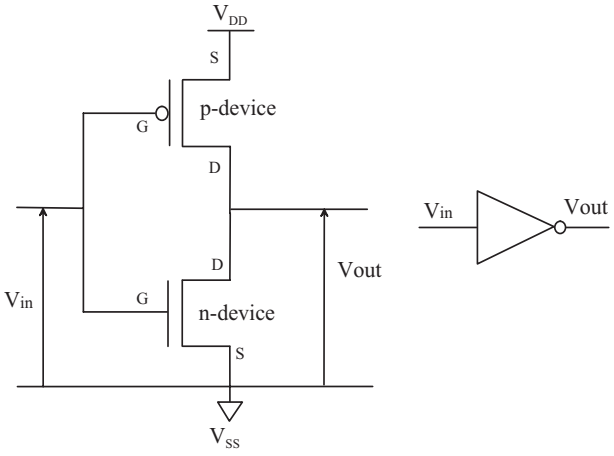


Figure 4.1: Schematic structure of a CMOS TFT static inverter.

**Region A.** In this region the n-device is in cutoff mode and p-device is in linear mode. The output voltage is

$$V_{\text{out}} = V_{\text{DD}}, \tag{4.1}$$

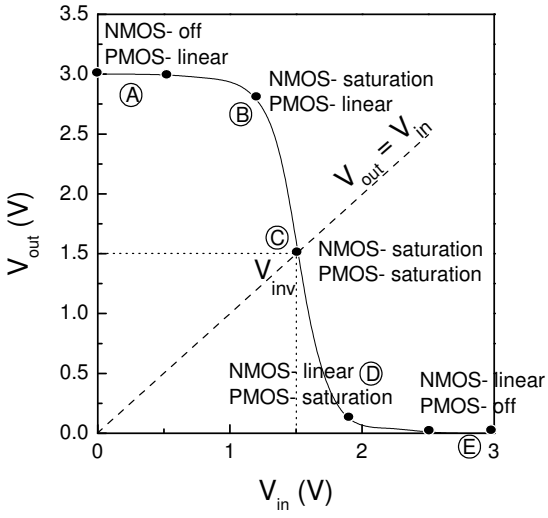


Figure 4.2: Voltage transfer characteristics of a static CMOS inverter. For each region the operation modes of the transistor are marked.

**Region B.** In this region the p-device is in its linear mode while the n-device is in saturation. The output voltage $V_{\text{out}}$ is given by

$$V_{\text{out}} = (V_{\text{in}} - V_{\text{TH,p}}) + \sqrt{(V_{\text{in}} - V_{\text{TH,p}})^2 - 2(V_{\text{in}} - \tfrac{1}{2}V_{\text{DD}} - V_{\text{TH,p}})^2 - \frac{\beta_{\text{n}}}{\beta_{\text{p}}}(V_{\text{in}} - V_{\text{TH,n}})^2}, \tag{4.2}$$

where $V_{\text{TH,p}}$ and $V_{\text{TH,n}}$ are the threshold voltages for p- and n-devices, respectively, and the $\beta$ are the grain factors of the (n- and p-type) transistors. $\beta$ depends on the process parameters as well as the device geometry, and is defined as

$$\beta = \frac{\mu\varepsilon}{t_{\text{ox}}} \cdot \frac{W}{L}, \tag{4.3}$$

where $W$ is the channel width and $L$ is the channel length.

**Region C.** Both the n- and p-devices are in saturation. This region exists for a single value of $V_{\text{in}}$. Possible values of $V_{\text{out}}$ in this regime satisfy the

inequalities

$$V_{in} - V_{TH,n} < V_{out} < V_{in} - V_{TH,p}, \tag{4.4}$$

Here the device is assumed to behave like an ideal current source that is independent of the drain voltage. In reality the drain current slightly increases with increasing drain voltage, thus the slope is finite in region C.

**Region D.** In this region the p-device is in saturation mode, while the n-device is in its nonsaturated mode. The output voltage is

$$V_{out} = (V_{in} - V_{TH,n}) + \sqrt{(V_{in} - V_{TH,n})^2 - \frac{\beta_p}{\beta_n}(V_{in} - V_{DD} - V_{TH,p})^2}, \tag{4.5}$$

**Region E.** In this region the p-device is in cutoff mode and the n-device is in linear mode. The output is

$$V_{out} = V_{SS}, \tag{4.6}$$

It is clear from the transfer characteristics of the inverter that the transition between the two states is very abrupt. This is highly desirable because noise immunity is maximized. Table 4.1 summaries the operation of the CMOS inverter in different regions.

| ***Region*** | ***Condition*** | ***p-device*** | ***n-device*** | ***Output*** |
|---|---|---|---|---|
| A | $0 < V_{in} < V_{TH,n}$ | nonsaturated | cutoff | $V_{out} = V_{in}$ |
| B | $V_{TH,n} \le V_{in} < V_{DD}/2$ | nonsaturated | saturated | Eq. (4.2) |
| C | $V_{in} = V_{DD}/2$ | saturated | saturated | $V_{out} = V_{in}$ |
| D | $V_{DD}/2 < V_{in} \le V_{DD} - \lvert V_{TH,p}\rvert$ | saturated | nonsaturated | Eq. (4.5) |
| E | $V_{in} > V_{DD} - \lvert V_{TH,p}\rvert$ | cutoff | nonsaturated | $V_{out} = V_{SS}$ |

Table 4.1: CMOS inverter operation in different regions.

### 4.3.1 The Threshold Voltage of the Inverter

The threshold voltage ($V_{inv}$) of an inverter is defined at the point where $V_{in} = V_{out}$ [81]. Its value can be obtained graphically from the intersection of the voltage transfer characteristics with the line $V_{in} = V_{out}$, as shown in Figure 4.2. At this point both PMOS and NMOS are saturated, and the expression for $V_{inv}$ is obtained by equating the current through the transistors:

$$\frac{\beta_n}{2}(V_{inv} - V_{TH,n})^2 = \frac{\beta_p}{2}(V_{DD} - V_{inv} - |V_{TH,p}|)^2, \tag{4.7}$$

which yields

$$V_{\mathrm{inv}} = \frac{\sqrt{\beta_{\mathrm{p}}/\beta_{\mathrm{n}}} \cdot (V_{\mathrm{DD}} - |V_{\mathrm{TH,p}}|) + V_{\mathrm{TH,n}}}{1 + \sqrt{\beta_{\mathrm{p}}/\beta_{\mathrm{n}}}}. \tag{4.8}$$

This leads to the conclusion that $V_{\mathrm{inv}}$ should be one-half of the available voltage swing ($V_{\mathrm{DD}}/2$) to obtain symmetrical characteristics when $\beta_{\mathrm{p}} = \beta_{\mathrm{n}}$ (assuming that the threshold voltage of the PMOS and the NMOS transistors are comparable).

### 4.3.2 The ratio $\beta_{\mathrm{n}}/\beta_{\mathrm{p}}$

The transfer characteristics of the inverter depend very sensitively on the ratio $\beta_{\mathrm{n}}/\beta_{\mathrm{p}}$ [80]. In order to explore the variations of the transfer characteristics with $\beta_{\mathrm{n}}/\beta_{\mathrm{p}}$, the transfer curve is measured for several values of $\beta_{\mathrm{n}}/\beta_{\mathrm{p}}$ and plotted in Figure 4.3.

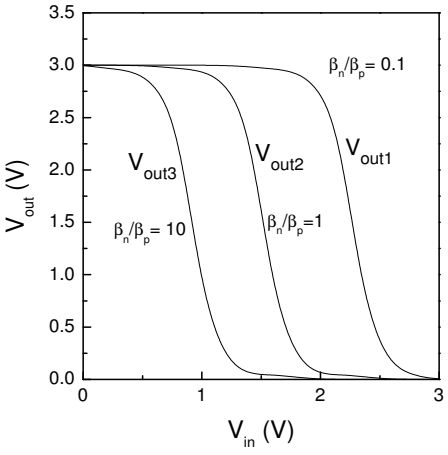


Figure 4.3: Influence of the ratio $\beta_{\mathrm{n}}/\beta_{\mathrm{p}}$ on the DC characteristics of the inverter.

It is readily seen that the threshold voltage $V_{\mathrm{inv}}$ of the inverter, where $V_{\mathrm{in}} = V_{\mathrm{out}}$, depends on $\beta_{\mathrm{n}}/\beta_{\mathrm{p}}$. Thus for a given process, $\beta_{\mathrm{n}}/\beta_{\mathrm{p}}$ can be changed by changing the channel dimensions. It can be seen from Figure 4.3 that as the

ratio $\beta_n/\beta_p$ decreases, the transition region shifts from left to right, however the output voltage transition remains sharp. For CMOS inverters a ratio

$$\frac{\beta_n}{\beta_p} = 1 \tag{4.9}$$

is desirable, since it allows a capacitive load to charge and discharge in equal times, providing equal current-source and sink capabilities. To obtain symmetrical characteristics and to maximize the noise margin, the PMOS transistor has to be $(\beta_n/\beta_p)$ times wider than the NMOS transistor.

### 4.3.3 Noise Margin

Noise margin is a parameter closely related to the transfer voltage characteristics of the inverter. It permits one to determine the allowable noise voltage on the input of a gate so that the output is not affected.

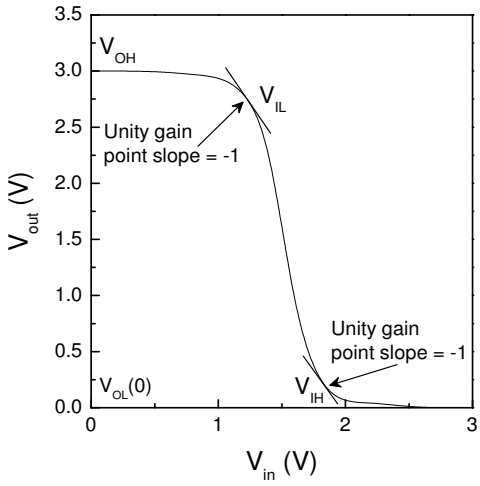


Figure 4.4: Noise margin of a CMOS static inverter.

It is specified in terms of two parameters: low noise margin, $NM_L$, and high noise margin, $NM_H$. These are given by

$$NM_L = |V_{IL,max} - V_{OL,max}|, \tag{4.10}$$

$$NM_{\mathrm{H}} = |V_{\mathrm{OH,min}} - V_{\mathrm{IH,min}}|, \tag{4.11}$$

where, $V_{\mathrm{IL,max}}$ = maximum low input voltage, $V_{\mathrm{OL,max}}$ = maximum low output voltage, $V_{\mathrm{OH,min}}$ = minimum high output voltage, $V_{\mathrm{IH,min}}$ = minimum high input voltage. The voltage levels $V_{\mathrm{IL,max}}$, $V_{\mathrm{OL,max}}$, $V_{\mathrm{OH,min}}$, and $V_{\mathrm{IH,min}}$ are shown in Figure 4.4. It is obvious that these margins have to be larger than 0 for a large digital circuit to be functional, and by preference should be as large as possible. This implies that the transfer characteristics should change abruptly, that is, the gain should be large in the transition region. If $NM_{\mathrm{L}}$ and $NM_{\mathrm{H}}$ are very low for a gate then the gate may be susceptible to switching noise.

## 4.4 Digital CMOS Circuits with Single-Grain TFTs

### 4.4.1 Design of Single-Grain Inverters and Ring Oscillators

Using TFTs with a top gate coplanar self-aligned structure, we designed a digital CMOS inverter with SG Si TFTs inside a location-controlled grain. In our CMOS inverter design the single grain covers the channel area of both (n- and p-channel) TFTs, as shown in Figure 4.5.

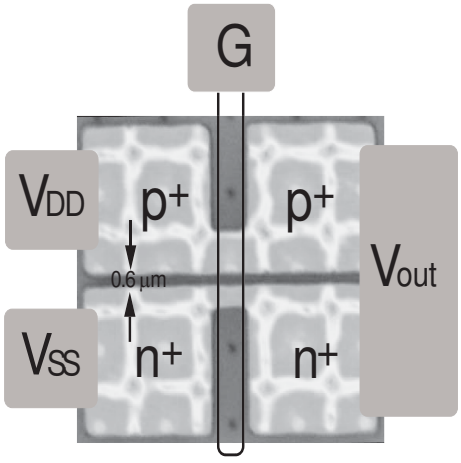


Figure 4.5: Optical image of the SG CMOS inverter made of TFTs.

It was discussed in Chapter 2 that $\mu_{\mathrm{FE}}$ is lower in the p-channel TFT than in the n-channel TFT. To ensure equal charging and discharging time for

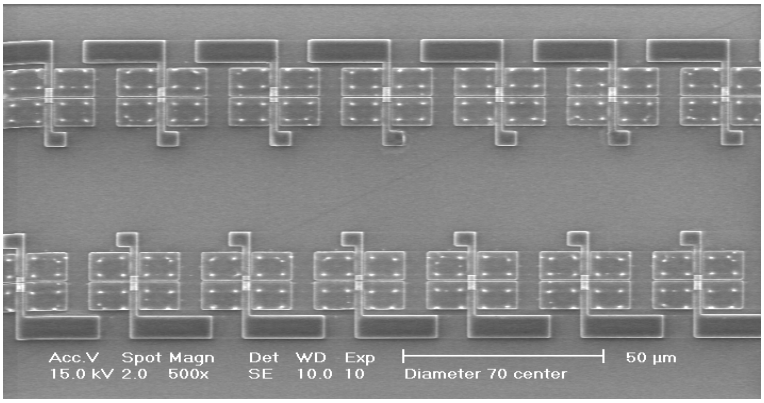


Figure 4.6: SEM image of a ring oscillator designed with SG TFTs

capacitive loads, the p-channel SG Si TFT is chosen to be twice as wide as the n-channel SG Si TFT. Figure 4.5 shows the optical image of the SG CMOS inverter, with both TFT channels inside a single grain. The SG CMOS inverter was designed with 0.6 µm design rules. This is the minimum line width that can be patterned on a wafer. A ring oscillator was designed by cascading an odd number of the SG CMOS inverters in a circular chain. Figure 4.6 shows the SEM image of the ring oscillator.

### 4.4.2 Fabrication of Single-Grain TFT Circuits

The schematic diagram of the process flow for the fabrication of single-grain CMOS TFT circuits is shown in Figure 4.7. First a grain filter grid is patterned in a thermally grown oxide layer on a c-Si wafer. Next a 250 nm thick a-Si layer is deposited by LPCVD, using silane ($SH_4$) at 550°C. To control the $V_{TH}$ parameter of the TFTs, both (n- and p-) channels were implanted with impurities. The channel doping dose and the type of impurity ions are shown in Table 4.2 for different gate oxides of the TFT channel.

Next, the samples are crystallized with one shot of XeCl excimer laser ($\lambda$ = 308 nm, pulse duration = 56 ns) at an elevated temperature of 450°C. After crystallization, a grid of location-controlled grains is obtained, as shown in Figure 2.2(b). Then an oxygen plasma treatment is carried out to passivate trap states and dangling bonds in the bulk Si. Next, a crystallized Si film is patterned into islands by reactive ion etching. The channel regions of the inverter are designed in such a way that the single grain covers the channel

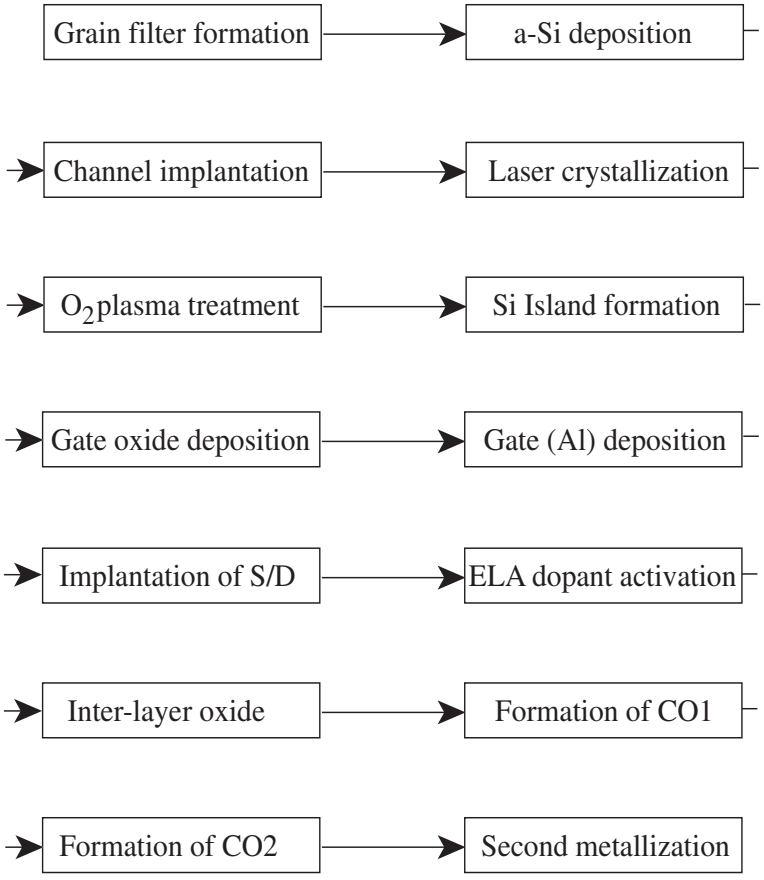


Figure 4.7: Process flow for the fabrication of SG CMOS TFT inverters.

regions of both TFTs, as shown in Figure 4.5. In the next step – done at Seiko-Epson Research Center, Japan – a gate insulator (either ECR-PECVD or TEOS-PECVD $SiO_2$) is deposited. Then a gate electrode is formed with sputtered Al at room temperature. The channel widths for n- and p-channel TFTs, measured by SEM, are 1.43 µm and 2.75 µm, respectively, whereas channel lengths are equal, 1.24 µm. Next, the source and the drain are implanted with a boron ion dose of $1 \times 10^{16}\,\mathrm{cm}^{-2}$ for the p-channel and a phosphorus ion dose of $1 \times 10^{16}\,\mathrm{cm}^{-2}$ for the n-channel, by covering either one of region by a photoresist. The dopants are activated by excimer laser annealing at

| *Oxide type and thickness* | *n-channel dose[$cm^{-2}$]* | *p-channel dose[$cm^{-2}$]* |
|---|---|---|
| 80 nm ECR-PECVD $SiO_2$ | $1 \times 10^{11}$(P) | $5 \times 10^{11}$(B) |
| 30 nm TEOS-PECVD $SiO_2$ | $2.5 \times 10^{11}$(B) | $2.5 \times 10^{11}$(P) |

Table 4.2: Channel implantation dose for SG CMOS inverters with different types of gate oxide.

room temperature. After the activation of the dopants, an inter-layer of $SiO_2$ is deposited. After making an ohmic contact to Si, the final electrodes are patterned. The schematic cross-sectional view of the SG CMOS TFT inverter is shown in Figure 4.8.

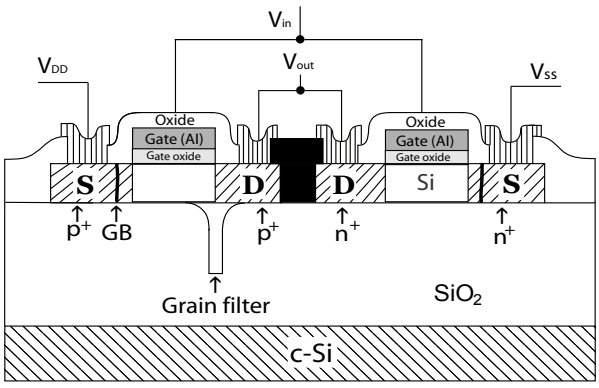


Figure 4.8: Schematic cross-sectional view of a SG CMOS TFT inverter.

### 4.4.3 Characterization of Digital Circuits

An inverter is characterized by its voltage transfer characteristics and its dynamic characteristics. The voltage transfer characteristics determine the logic function and $V_{\mathrm{inv}}$. It is measured using a CASCADE probe station with an HP4156A parameter analyzer, as shown in Figure 4.9. The dynamic characteristics determine the rise and fall times of the input pulse. They are measured using a pulse generator and a Tektronix TDS 2024 oscilloscope. The gate of the inverter receives its input pulse from the pulse generator and its output pulse is detected by the oscilloscope. Measurements were done with a pico probe, which has a very low external capacitance, on the order of a pF. The


Figure 4.9: Measurement setup for the SG inverter and the ring oscillator.

physical reason for delay is the existence of parasitic capacitances associated with the TFT. The standard circuit for measuring the propagation gate delay $t_p$ is a ring oscillator, which consists of an odd number ($N$) of inverters. As the number of inverters is odd, this circuit does not have a stable operating point and oscillates. The oscillation period $T$ is determined by the propagation time of a signal transition through the complete chain: $T = 2t_pN$. The propagation delay $t_p$ is directly related to the speed and performance of the gates. Generally, it is defined as the average of the rise time $t_r$ and the fall

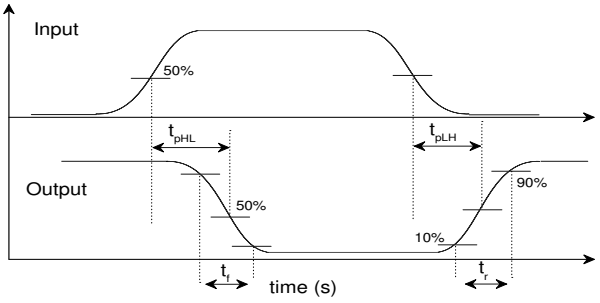


Figure 4.10: Definition of the propagation delay and rise and fall times.

time $t_f$ of the output transition. The rise and fall times are both measured between the 10% and 90% points of the waveform, as show in Figure 4.10. Propagation delay indicates how quickly the gate responds to a change at its

input. It specifies the delay experienced by a signal when passing through a gate. It is measured between the 50% transition points of the input and output waveforms, as shown in Figure 4.10:

$$t_{\mathrm{p}} = \frac{t_{\mathrm{p,L–H}} + t_{\mathrm{p,H–L}}}{2}, \tag{4.12}$$

where $t_{\mathrm{p,L–H}}$ is the gate response time for a low to high output transition, while $t_{\mathrm{p,H–L}}$ refers to a high to low transition.

### 4.4.4 Characterization of Single-Grain CMOS TFT Inverters

Figure 4.11 shows the voltage transfer characteristics of SG CMOS inverters with an 80 nm thick ECR-PECVD and a 30 mm thick TEOS-PECVD $SiO_2$ layer.

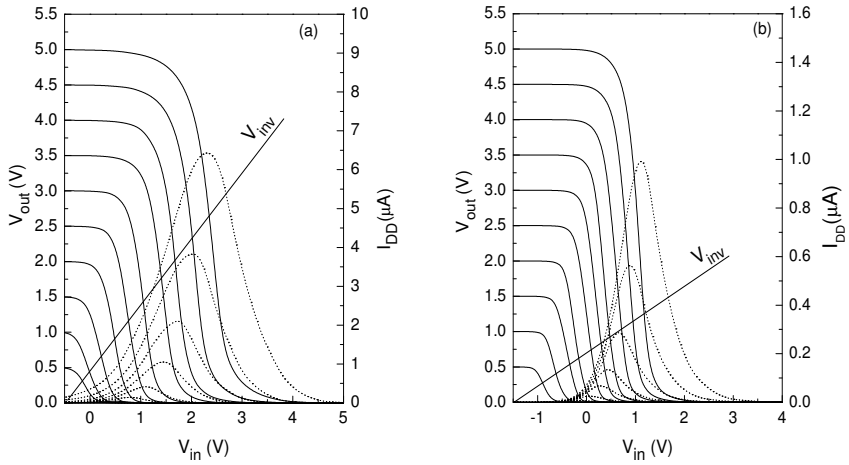


Figure 4.11: Voltage transfer characteristics of a SG CMOS TFT inverter with (a) a 80 nm thick ECR-PECVD $SiO_2$ layer; (b) a 30 nm thick TEOS-PECVD $SiO_2$ layer as gate insulator.

These inverters show a full rail-to-rail swing and full-range abrupt voltage transfer characteristics. In TFTs with an ECR-PECVD $SiO_2$ gate insulator $V_{\mathrm{inv}}$ was estimated to be 2.35 V at the supply voltage of 5 V – that is about

one-half of the supply voltage –, while it was found to be lower in TFTs with a TEOS-PECVD $SiO_2$ gate insulator because of the deviation of the $\beta$ ratio from unity. The propagation gate delay of the inverter is determined from the dynamic characteristics of the SG CMOS inverter.

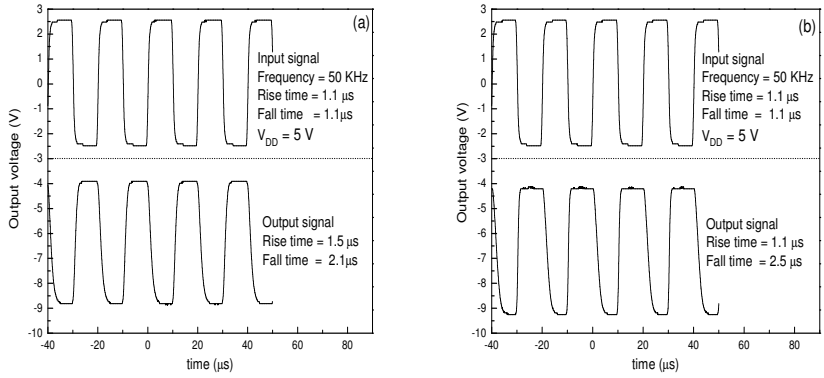


Figure 4.12: Dynamic characteristics of the SG CMOS TFT inverter with (a) an 80 nm thick ECR-PECVD $SiO_2$ layer; (b) a 30 nm thick TEOS-PECVD $SiO_2$ layer as gate insulator.

Figure 4.12 shows the dynamic characteristics of SG CMOS inverters with an ECR-PECVD and a TEOS-PECVD $SiO_2$ layer as gate insulator. A 50 kHz input pulse is applied to the gate of the inverter, whereas $V_{DD}$ is kept constant at 5 V. The output characteristics of the inverter show a 180° phase shift relative to the input pulse. This guarantees the inverter operation of the single-grain CMOS TFT inverter. The rise and fall times of the output pulse were estimated as 1.5 µs and 2.1 µs for TFTs with an ECR-PECVD $SiO_2$ layer and as 1.1 µs and 2.5 µs for TFTs with a TEOS-PECVD $SiO_2$ layer as gate insulator. These large rise and fall times are plausibly due to the high parasitic capacitance associated with the SG inverter. This parasitic capacitance is minimized by the ring oscillator.

### 4.4.5 Ring Oscillators with Single-Grain Inverters

To estimate the gate delay of single-grain CMOS inverters accurately, a 101-stage ring oscillator was designed. The ring oscillator was fabricated using

the same process as for single-grain CMOS inverters. The design of the ring oscillator is shown in Figure 4.6.

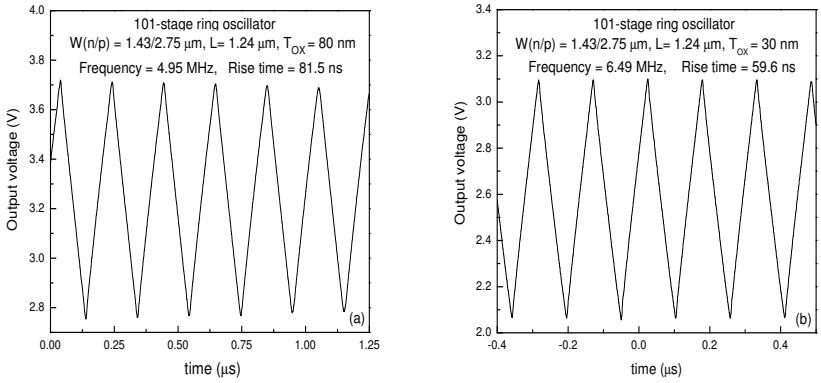


Figure 4.13: Output characteristics of a 101-stage ring oscillator with (a) an 80 nm thick ECR-PECVD $SiO_2$ layer; (b) a 30 nm thick TEOS-PECVD $SiO_2$ layer as gate insulator.

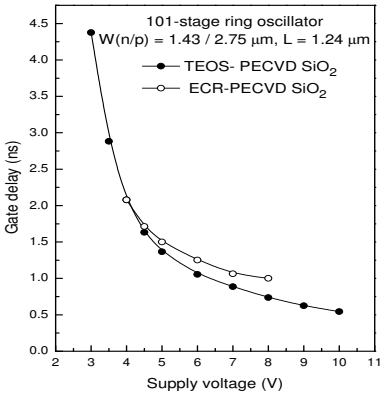


Figure 4.14: Gate delay as a function of the supply voltage.

Figure 4.13 shows the characteristics of two ring oscillators, with an 80 nm thick ECR-PECVD $SiO_2$ layer and a 30 nm thick TEOS-PECVD $SiO_2$ layer as gate insulator. The thickness of the Si layer is 250 nm and the channel length of the inverter is 1.24 µm in both cases. With an 80 nm thick ECR-PECVD $SiO_2$ gate insulator, the ring oscillator operates at a frequency of 4.95 MHz at a supply voltage of 8 V. The rise time of the output wave was estimated to be 81.5 ns. On the other hand, the ring oscillator with a 30 nm thick TEOS-PECVD $SiO_2$ gate insulator operates at a frequency of 6.49 MHz at the same supply voltage and its rise time was estimated to be 59.6 ns. This decrease in the propagation delay is attributed to the improved characteristic values of SG TFTs with a 30 nm thick TEOS-PECVD $SiO_2$ gate insulator, as observed in the characteristics of the single-grain inverter.

Figure 4.14 shows how the propagation delay depends on the supply voltage for both gate insulator types. The propagation delay shows an inversely proportional dependence on the supply voltage. These results show that the SG inverter gives the shortest propagation delay in TFTs for given device dimensions ($L = 1.24$ µm and supply voltage = 8 V) [82].

## 4.5 Conclusion

SG CMOS TFT inverters were fabricated for the first time inside a location-controlled grain using the µ-Czochralski process and excimer laser crystallization. The SG CMOS TFT inverter shows a full swing between low and high logics. To estimate the propagation delay, a 101-stage ring oscillator was also fabricated by cascading SG CMOS inverters. The propagation gate delay in the ring oscillator with a 30 nm thick TEOS-PECVD $SiO_2$ layer as gate insulator was 0.7 ns at a supply voltage of 8 V, which is shorter than in conventional poly-Si circuits. In summary, SG CMOS inverters and ring oscillators were realized using SG Si TFTs fabricated with a low-temperature process ($< 350°C$). This result represents a great step toward the realization of systems on glass in large-area electronics and 3D circuit integration.

# Chapter 5

# Crystallization of Thin Si Layer with a Capping Layer of Oxide

*This chapter describes a new method for enlarging location-controlled grains. As the thickness of the Si film decreases, so does the maximum grain size because of the increased solidification rate of the molten Si. The maximum grain size is increased by applying a capping layer of $SiO_2$ on the Si layer before crystallization. Owing to the heat stored in it this capping oxide delays the solidification of the molten Si during crystallization. Furthermore, the oxide capping layer is used as a part of the gate insulator to improve the quality of the interface between Si and $SiO_2$. Single grain (SG) TFTs (n- and p-channel) fabricated using a capping oxide as a part of gate insulator show higher performance than SG TFTs without a capping oxide. The propagation gate delay of SG CMOS inverters was estimated to be 3.1 ns at a supply voltage of 8 V.*

## 5.1 Introduction

For a 250 nm thick Si layer, a large grain of 7 µm is obtained using the µ-Czochralski process in excimer laser crystallization. SG Si TFTs fabricated inside the location-controlled grain have very high average $\mu_{\mathrm{FE,e}}$ (600 $\mathrm{cm}^2$/Vs) and $\mu_{\mathrm{FE,h}}$ (273 $\mathrm{cm}^2$/Vs) values, as discussed in Chapter 2. However, thinner Si

films are usually required to ensure compatibility with current LTPS processes and better stability in the TFT characteristics. It was shown that a decrease in the thickness of the Si film reduces the size of the location-controlled grains and also increases the number of CSL twin GBs, hence impairing the TFT properties [47]. The $SiO_2$ capping layer (C/L) on top of the Si layer has been reported to be effective in increasing the grain size in conventional excimer laser crystallization [83, 84] as well as in the μ-Czochralski process [85]. This C/L serves both as a heat reservoir and an anti-reflection coating.

In this chapter we propose a thin $SiO_2$ C/L (the thermal conductivity of $SiO_2$ is $\kappa_{SiO_2} = 1.4\,\mathrm{W\,m^{-1}\,K^{-1}}$) on top of the thin Si layer to increase the grain size in the μ-Czochralski process. This new layer increases the total amount of stored heat in the molten Si layer, and so elongates the solidification period. This leads to a significant increase in grain size, even in 50 nm thick Si layers. The C/L also introduces an optical path difference between light rays reflected from the bottom and the top of the C/L. Experimental and simulation results show that this optical path difference has an anti-reflection effect which depends strongly on the thickness of the $SiO_2$ C/L. Using the μ-Czochralski process, SG Si TFTs with a $SiO_2$ C/L as part of the gate insulator were fabricated with different Si thicknesses. Higher performances were obtained with this newly developed process, even for thin Si films. This is due to the improved properties of bulk Si and the $Si/SiO_2$ interface. SG CMOS inverters with thin Si layers were also realized using this new process. The propagation gate delay was estimated with a ring oscillator designed with SG CMOS inverters.

## 5.2 Crystallization with an Oxide Capping Layer

### 5.2.1 Theory

We propose a new way to enlarge the grain size in thin Si films when the μ-Czochralski process is used. The basic idea is to store heat in a C/L to postpone the onset of nucleation. Figure 5.1 shows the schematic diagram of samples with and without a $SiO_2$ C/L. This $SiO_2$ C/L has two effects in the crystallization of an a-Si layer: heat storing [86] and anti-reflection [84].

#### Enhanced Heat Storing

After the laser irradiation of the Si layer, a certain amount of heat, $Q_{Si}$, is stored in it. The temperature $T$ of the molten Si changes linearly with $Q_{Si}$. Heat diffusion is negligible in the lateral direction as there are no variations

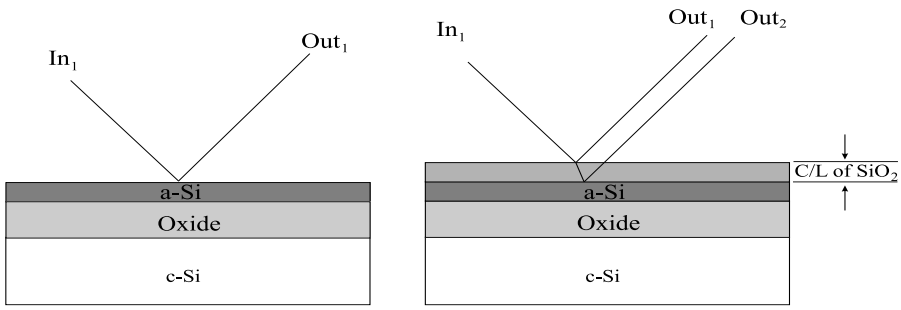


Figure 5.1: Schematic diagram of the reflection and transmission of laser irradiation from different interfaces.

in the light intensity along that direction. There is, however, a heat flow of flux density $\Gamma_V$ in the vertical direction toward the substrate. This reduces the temperature of the molten Si. The time constant, $\tau$, of the temperature decay of the molten Si is given by

$$\tau = \frac{Q_{Si}}{\Gamma_V}. \tag{5.1}$$

The total amount of heat stored in the system, $Q$, is given by

$$Q = Q_{Si} + Q_{SiO_2}. \tag{5.2}$$

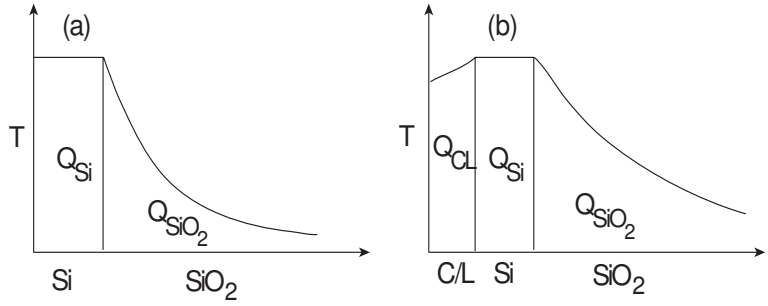


Figure 5.2: Schematic diagram of the temperature profile for structures (a) without a capping layer; (b) with a capping layer.

There is a direct way to achieve a larger $Q$ value: by choosing a thicker Si layer – however, very thick Si layers are unacceptable for device applications. We propose to increase $Q$ by covering the surface of the Si layer with a C/L of $SiO_2$, since its thermal conductivity, $\kappa_{SiO_2}$ is lower than that of Si. In this case the total amount of heat stored in the system, $Q$, is given by

$$Q = Q_{CL} + Q_{Si} + Q_{SiO_2}, \tag{5.3}$$

where $Q_{CL}$ is the amount of the heat stored in the oxide capping layer. This layer temporarily stores the heat delivered by the high temperature molten Si layer during the irradiation time and subsequently returns it to the Si layer when the temperature drops. Figure 5.2 shows the temperature profiles of two structures, without and with a capping layer. The oxide capping layer reduces the temperature gradient at the back interface. This means that the capping layer can increase the $Q$ value, which helps to enlarge the grain size.

However, the effect of the C/L is limited: a thick capping layer can also serve as a heat sink [87]. It was demonstrated in the literature that after the laser irradiation ($0 < t < 56\,\text{ns}$) of the samples with a $SiO_2$ C/L heat is initially delivered to the C/L from the molten Si layer. When the molten Si is cooling down ($t > 54\,\text{ns}$), a part of the heat stored in the capping layer diffuses back to the Si layer. Thus, the capping layer serves predominantly as a heat reservoir and the Si layer can, in turn, remain in a liquid phase for a longer time than in samples without a $SiO_2$ C/L. If the $SiO_2$ C/L returns only a part of the total heat delivered by the molten Si layer, keeping another part to itself, it can behave as a heat sink. This heat-sink effect becomes more pronounced for thicker C/Ls. In our experiments we used a thin $SiO_2$ C/L, which served as a heat reservoir rather than a heat sink. A thin $SiO_2$ C/L helps to enlarge the diameter of 2D location-controlled grains in the μ-Czochralski process.

**Anti-Reflection**

In addition to the heat storage effect, the $SiO_2$ C/L also serves as an anti-reflection layer during laser irradiation. The anti-reflection effect of a thin $SiO_2$ C/L is explained by thin film optics, which deals with reflection from and transmission through the interfaces of multilayer systems. Figure 5.1 shows the schematic diagram of reflection and transmission in the multilayer system used in our experiments. Reflection and transmission at a flat surface are determined by the Fresnel amplitude coefficients $(r,t)$ [88]:

$$r = \frac{\tilde{\eta}_0 - \tilde{\eta}_1}{\tilde{\eta}_0 + \tilde{\eta}_1}, \tag{5.4}$$

$$t = \frac{2\tilde{\eta}_0}{\tilde{\eta}_0 + \tilde{\eta}_1}. \tag{5.5}$$

Here $\tilde{\eta}_0 = \tilde{\eta}_0 - i\tilde{\kappa}_0$ and $\tilde{\eta}_1 = \tilde{\eta}_1 - i\tilde{\kappa}_1$ are the complex indices of refraction for the two media ($SiO_2$ and a-Si). $r$ and $t$ are also complex quantities. Reflectance and transmittance are defined as

$$R = |r|^2 = \left| \frac{\tilde{\eta}_0 - \tilde{\eta}_1}{\tilde{\eta}_0 + \tilde{\eta}_1} \right|^2 \tag{5.6}$$

$$T = \left| \frac{\tilde{\eta}_1}{\tilde{\eta}_0} \right| \cdot |\tilde{t}|^2 = \frac{4|\tilde{\eta}_0 \tilde{\eta}_1|}{|\tilde{\eta}_0 + \tilde{\eta}_1|^2} \tag{5.7}$$

We therefore have

$$R + T = 1. \tag{5.8}$$

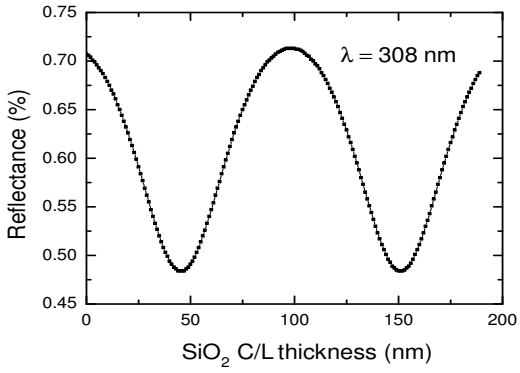


Figure 5.3: Variations of reflectance with the thickness of the $SiO_2$ C/L at a constant wavelength, $\lambda = 308\,\text{nm}$.

From Eqs. (5.6) and (5.7) one can calculate the reflectance and the transmittance for the given refractive indices of $SiO_2$ ($\eta_0 = 1.46$) and a-Si, ($\eta_1 =$

3.4). A large fraction of the incident light is transmitted through the $SiO_2$ layer and only a small fraction is reflected. An opto-electronic simulator – *Advanced Semiconductor Analysis (ASA)*, developed at Delft University of Technology – was used to calculate the reflectance and transmittance at the top and bottom of the layers in our multilayer system [89]. An important feature of the ASA program includes the calculation of the profile of the reflected and transmitted light. The thickness of the $SiO_2$ C/L was optimized to achieve maximum transmittance of the incident light. In the optical simulation of our multilayer system, the thickness of the Si layer (250 nm), the thickness of the $SiO_2$ C/L (0–200 nm), the refractive indices of a-Si ($\eta_1 = 3.4$) and $SiO_2$ ($\eta_0 = 1.46$), and the wavelength of the excimer laser ($\lambda = 308$ nm) were used as input parameters.

Figure 5.3 shows the variations of reflectance at the top surface of the $SiO_2$ C/L. Reflectance varies periodically with the thickness of the C/L. This is due to the interference of light waves. The thickness of the C/L introduces an optical path difference – and thus a phase difference – between light rays reflected from the top and bottom of the C/L. If the reflected light rays are in the same phase, constructive interference occurs, while if they are out of phase, destructive interference is observed. This is why reflectance varies with the thickness of the C/L. In our simulations the first reflectance minimum was obtained at a C/L thickness of 48.5 nm. For this reason a 50 nm thick $SiO_2$ layer was applied as a C/L on top of the a-Si layer in the µ-Czochralski process.

### 5.2.2 Experiment

#### TEOS-PECVD Oxide Capping Layer

As a capping layer during crystallization, we used TEOS-PECVD oxide, which was deposited at Delft Institute of Microelectronic and Submicrontechnology (DIMES), TUDelft. Investigating the interface properties of this oxide is very important, as it is used as a part of the gate insulator in TFTs. To determine the interface quality of this oxide, we fabricated a MOS capacitor with a 100 nm thick TEOS-PECVD oxide layer, deposited at 350°C on ⟨100⟩ p-type c-Si wafer ($\rho = 0.1$–$1\ \Omega \cdot \mathrm{cm}$) because in SG Si TFTs crystallized with a $SiO_2$ C/L the total thickness of the gate insulator is 100 nm. The MOS capacitor has an Al electrode as a metal gate.

A quasi-static C-V measurement was performed with an HP 4156C parameter analyzer, and high-frequency measurements were done with an LCR meter. Figure 5.4 shows the quasi-static and high-frequency C-V characteristics. From Eq. (2.1), $D_{\mathrm{it}}$ at mid-gap was estimated to be $1.02 \times 10^{11}\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$.

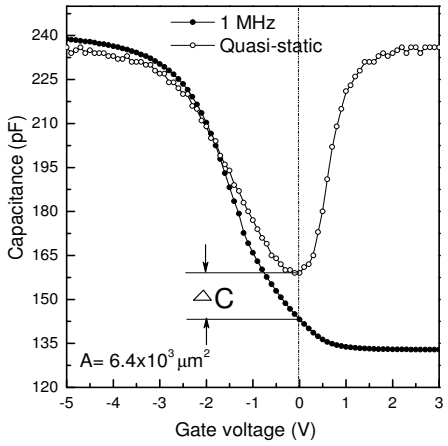


Figure 5.4: High-frequency and quasi-static characteristics of a metal-oxide semiconductor (MOS) capacitor with a 100 nm thick TEOS-PECVD $SiO_2$ layer. $D_{it}$ at mid-gap is $1.02 \times 10^{11}\,cm^{-2}eV^{-1}$.

However, this oxide has a higher interface density of states than the oxide used in the previous chapters. As the Si layer is irradiated by the laser light during crystallization, the temperature exceeds the melting point of a-Si, so one may expect an improvement in the oxide quality due to annealing during the crystallization of Si.

**Excimer Laser Crystallization**

Figure 5.5 shows the schematic diagram of a sample crystallized with a $SiO_2$ C/L in the µ-Czochralski process. The µ-Czochralski process was described in detail in Section 2.2. We shall only give a brief overview here. A grid of deep 100 nm-diameter cavities is made in thermally oxidized c-Si wafers using conventional photolithography and oxide deposition. Next, a 250 nm thick a-Si layer is deposited by LPCVD using $SiH_4$ at 550°C. Then a 50, 100, or 150 nm thick $SiO_2$ C/L is deposited using TEOS and oxygen at 350°C. Finally, the samples are crystallized with one shot of the excimer laser at an elevated temperature of 450°C.

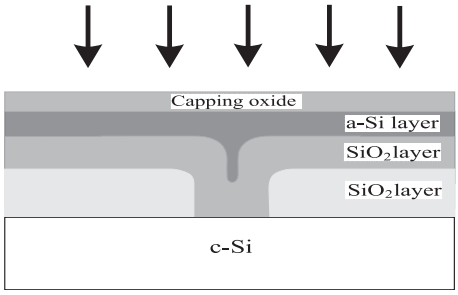


Figure 5.5: Schematic representation of the sample crystallized with a C/L in the µ-Czochralski process.

### 5.2.3 Characterization of Si Grains

To analyze the surface crystallographic orientations and the nature of GBs, SEM and EBSD (electron backscattering diffraction) analyses were performed on the grain grid obtained by laser crystallization with a capping oxide. SEM analysis was performed on Schimmel-etched samples.

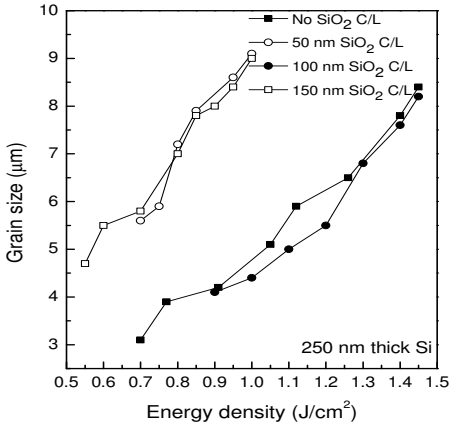


Figure 5.6: Variations of the grain size with the laser energy density for a 250 nm thick Si layer with a $SiO_2$ C/L. The thickness of the C/L varies from 0 to 150 nm.

Figure 5.6 shows the grain size as a function of the energy density of the excimer laser for a 250 nm thick Si layer with a 50, 100, or 150 nm thick $SiO_2$ C/L and without a $SiO_2$ C/L. It can be observed that when a 50 or 150 nm thick $SiO_2$ C/L is used, the maximum grain size significantly increases, up to 9.2 µm – whereas it is smaller with a 100 nm thick $SiO_2$ C/L or without a C/L. This is explained in terms of the heat stored in the $SiO_2$ C/L, which flows back into the underlying layers. This heat delays nucleation in the molten Si, which helps to elongate the solidification period, and hence the grain size increases. The $SiO_2$ C/L serves as a heat reservoir during the solidification of the Si layer. It is also observed that with a 50 or 150 nm thick $SiO_2$ C/L the same grain size is obtained at a lower energy density than with a 100 nm thick $SiO_2$ C/L or without a C/L. These variations with the thickness of the C/L are due to the anti-reflection effect that arises from the interference between reflected rays of the excimer laser. These results are in accordance with the simulation results presented in the previous section. Thus, a 50 nm thick $SiO_2$ C/L on top of a 250 nm thick Si layer increases the grain size very efficiently. Moreover, it also decreases the crystallization energy density at which large grains are obtained.

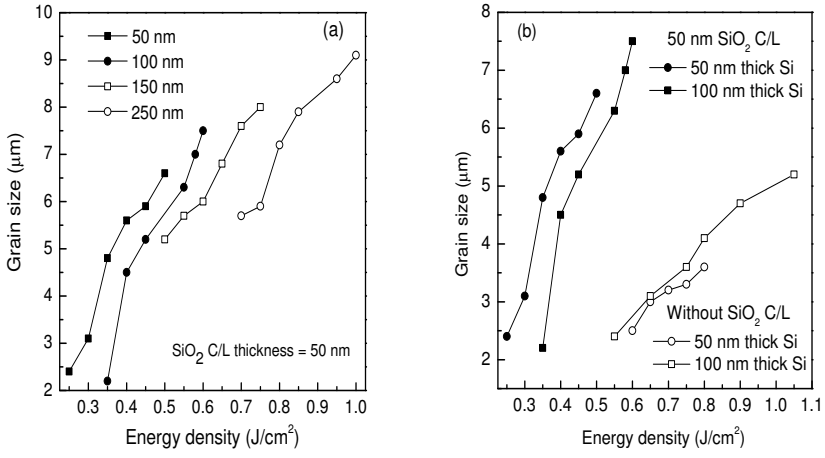


Figure 5.7: (a) Grain size as a function of the laser energy density for a 250 nm thick Si layer with a 50 nm thick $SiO_2$ C/L. (b) Comparison of the grain sizes obtained with and without a 50 nm thick $SiO_2$ C/L.

To increase the grain size for a thin (especially 50 nm and 100 nm thick) Si layer, a 50 nm thick $SiO_2$ C/L is used. Figure 5.7(a) shows the grain size as a function of the energy density for various thicknesses of the Si layer with a 50 nm $SiO_2$ C/L. The grain size increases with the Si thickness as the melt duration increases because of the increased heat storage in the Si layer. Figure 5.7(b) shows the variations of the grain size with energy density for 50 and 100 nm thick Si layers with and without a $SiO_2$ C/L. The grain size is larger with a 50 nm $SiO_2$ C/L than without it. Additionally, the crystallization energy required to melt the Si layer is lower with a 50 nm thick $SiO_2$ C/L than without it. The larger grain size is due to the heat reservoir effect of the C/L, while the reduction in the crystallization energy density needed to start the grain growth is due to its anti-reflection effect.

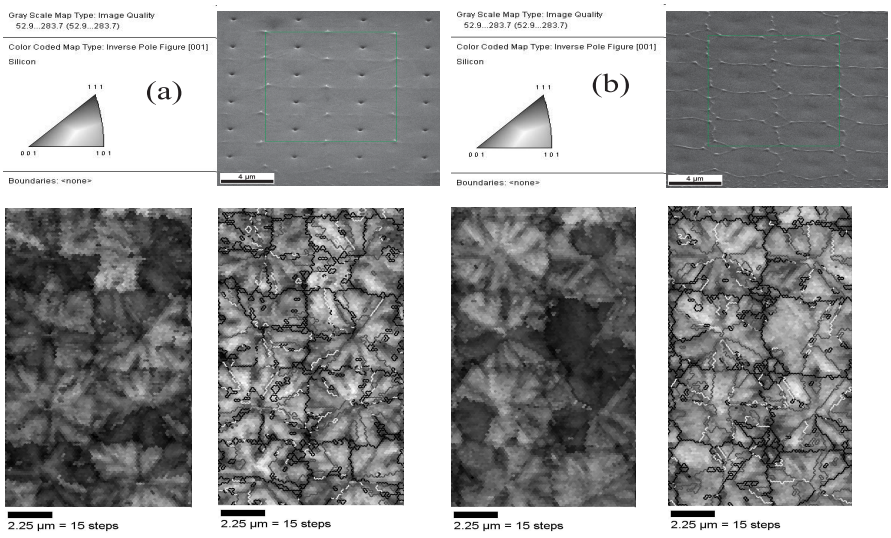


Figure 5.8: (a) EBSD mapping of the surface crystallographic orientation and GBs for a 50 nm thick Si layer crystallized with a 50 nm thick $SiO_2$ C/L. The $SiO_2$ C/L was etched away in BHF before the EBSD analysis. (b) EBSD mapping of the surface crystallographic orientation and GBs for a 50 nm thick Si layer crystallized without a $SiO_2$ C/L. White lines indicate CSL twin GBs, and black lines random GBs.

Figure 5.8 shows the mapping of the surface crystallographic orientations and the GBs, measured by electron backscattering diffraction (EBSD) for 50

nm thick Si islands crystallized with and without a 50 nm thick $SiO_2$ C/L. White lines indicate CSL twin GBs, and black lines random GBs. It can be seen that the dominant defects inside the location-controlled Si islands are CSL twin GBs. Hardly any random GBs are observed inside the Si islands. The surface crystallographic orientation is found to be random. CSL GBs inside the Si islands are predominantly $\Sigma 3$ and $\Sigma 9$ twin boundaries, which have negligible effect on the electrical performance of the TFTs.

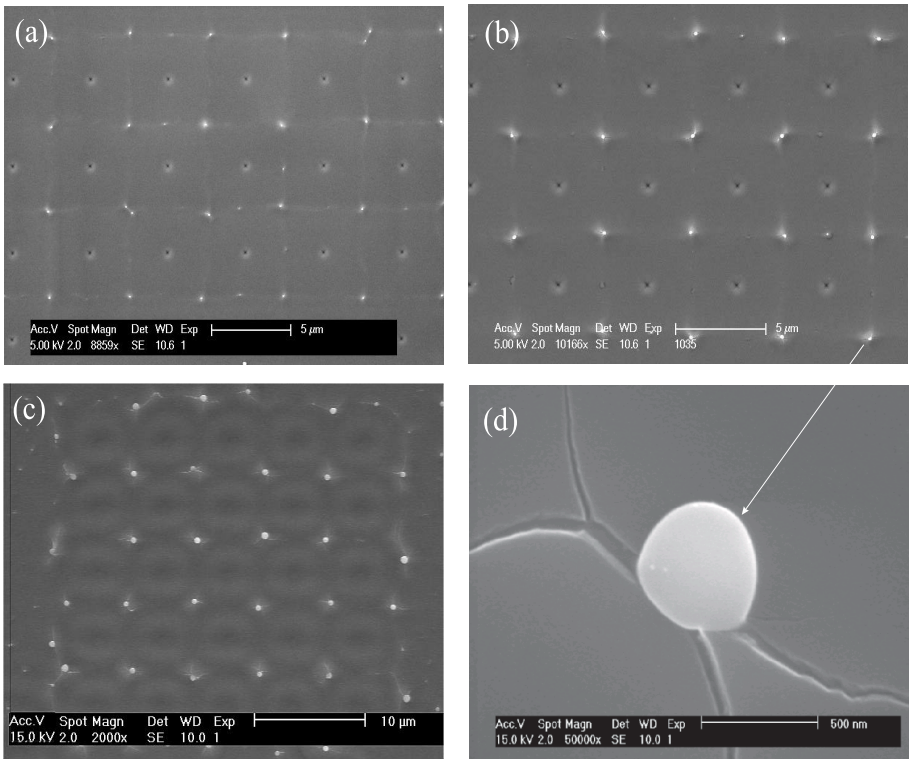


Figure 5.9: SEM image of a (a) 50 nm, (b) 100 nm, and (c) 250 nm thick Si layer crystallized with a 50 nm thick $SiO_2$ C/L. (d) SEM image of the protrusion formed during the crystallization with the $SiO_2$ C/L. White dots show the protrusions that appear only at the corners of square-shaped grains.

Figure 5.9 shows a SEM image of location-controlled grains in 50, 100, and 250 nm thick Si layers with a 50 nm thick $SiO_2$ C/L. A striking feature of

the SEM images is the presence of some protrusions, sprouts of Si through the $SiO_2$ C/L. These protrusions seem to be the same as in a conventional poly-Si layer with a C/L. While in the crystallization of conventional poly-Si with a $SiO_2$ C/L these protrusions are randomly distributed on the surface of the Si layer, in the μ-Czochralski process they are observed only at the corners of the square-shaped grains, where four grains collide. The size of these protrusions is proportional to the thickness of the Si layer.

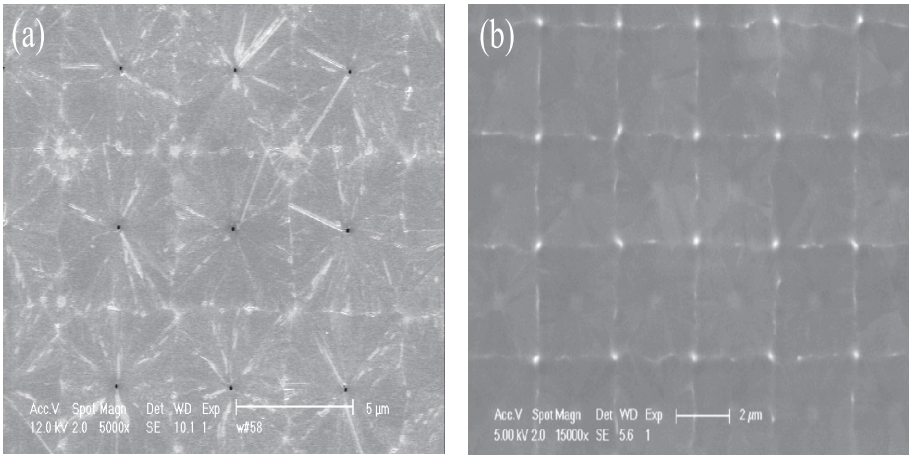


Figure 5.10: SEM image of a 50 nm thick Si layer crystallized (a) with a $SiO_2$ C/L, and (b) without a C/L. For capping oxide crystallization a dip is visible at the position of the grain filter. Its absence in the crystallization process without a $SiO_2$ C/L is due to the reflow of molten Si during solidification.

To analyze the topography of the grains and protrusions, the $SiO_2$ C/L was removed by wet etching in buffered hydrofluoric acid (BHF) (1:20). After the removal of the capping layer a dip at the position of grain filter was observed, as shown in Figure 5.10(a) – while the surface through the grain is planar in the sample crystallized without a $SiO_2$ C/L, as shown in Figure 5.10(b). This difference is due to the reflow of molten Si during solidification when the sample is crystallized without a $SiO_2$ C/L.

Figure 5.11 shows the AFM image of a grid of location-controlled grains for different Si thicknesses. The height and diameter of the protrusions are proportional to Si thickness, as the total volume of Si is increased. The height and diameter of the protrusions are successfully reduced by decreasing the Si thickness, and hence the Si volume, as plotted in Figure 5.12. The mean sur-

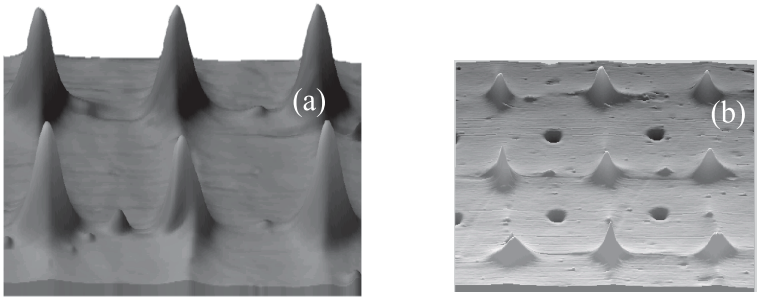


Figure 5.11: AFM image of a location-controlled grain grid for a (a) 250 nm, and (b) 50 nm thick Si layer. The height of the protrusions are seen to decrease with decreasing Si thickness.

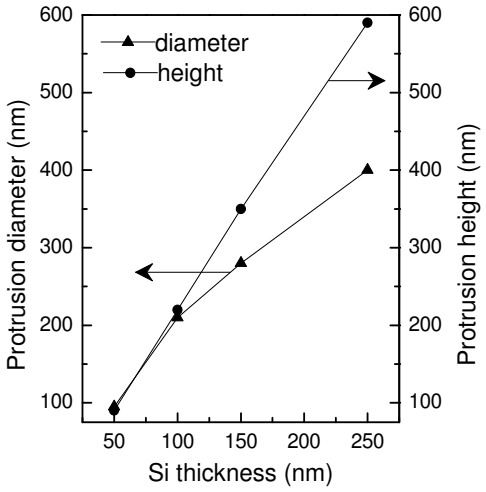


Figure 5.12: Height and diameter of the protrusions as functions of the thickness of the Si layer.

face roughness inside the planar area (outside the grain filter and the hillocks) where the TFT channel regions are located is 10 nm.

## 5.3 Fabrication Process Flow for SG TFTs with Capping Oxide Crystallization

Industrial applications generally require TFTs with a thin ($\sim$ 70 nm) Si film because of the improved stability in the TFT characteristics. Moreover, thin Si films are compatible with conventional low-temperature poly-Si (LTPS) TFT fabrication processes. However, the size of location-controlled grains decreases with decreasing Si film thickness. Crystallization with a $SiO_2$ C/L on top of the a-Si layer may, nevertheless, increase the grain size for thin Si films. To determine the electrical properties of thin Si films, SG TFTs were fabricated inside a location-controlled grain using an oxide capping as part of the gate insulator.

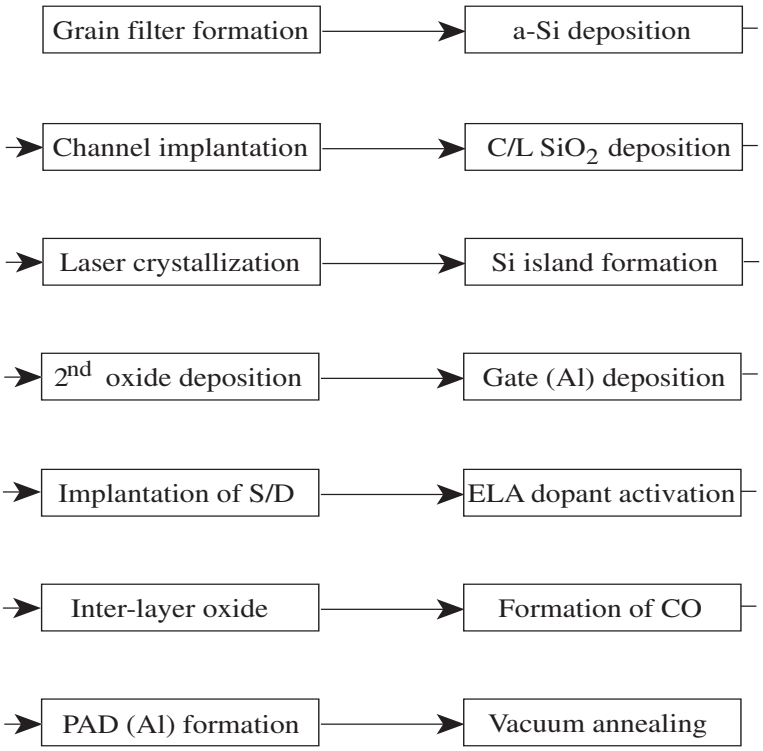


Figure 5.13: Process steps for the fabrication of SG TFTs using a capping oxide during crystallization.

The process steps for the fabrication of SG Si TFTs are shown in Figure 5.13. A detailed presentation of the µ-Czochralski is given in Section 2.2. First a grid of deep 100 nm-diameter cavities is made in thermally oxidized c-Si wafers using conventional photolithography and depositing another oxide layer. Next a 50 or 100 nm thick a-Si layer is deposited by LPCVD using $SiH_4$ at 550°C. After the deposition of a 50 nm thick $SiO_2$ C/L by TEOS-PECVD at 350°C the samples are crystallized with one shot of excimer laser ($\lambda$ = 308 nm, pulse duration = 56 ns) at an elevated temperature of 450°C. The crystallized Si film is then patterned into islands by reactive ion etching. Unlike in the conventional process, the Si surface is covered with a $SiO_2$ C/L to avoid any contamination due to additional cleaning. In the conventional TFT fabrication process this additional cleaning step might contaminate the Si surface. In our TFT channel region design the single grain covers the entire channel area. The position of the TFT channel with respect to the grain filter is such that the direction of current flow is parallel to the planar defects inside the grain, as shown in Figure 2.3, on page 21. Then an additional 50 nm thick TEOS-PECVD $SiO_2$ layer is deposited to cover the side walls of the Si islands. For comparison, SG Si TFTs without a $SiO_2$ C/L were also fabricated. In both cases, the total thickness of the gate insulator is 100 nm. The gate electrode is then formed with sputtered Al at room temperature. The source and drain were implanted with impurities using an Al gate pattern as a mask, and subsequently activated by excimer laser at room temperature. Afterwards an inter-layer oxide film is formed over the source and drain electrodes. Finally, vacuum annealing is performed for 45 minutes at 350°C.

### 5.3.1 Single-Grain TFT Characteristics

The oxide capping layer used in the crystallization of thin Si films not only helps to enlarge the grain size but also improves the bulk properties of the Si grain. Secondly, the interface quality between Si and $SiO_2$ is expected to improve if a $SiO_2$ C/L is used as part of the gate insulator in the TFT. To investigate the bulk properties of the Si and the interface properties between Si and $SiO_2$, n- and p-channel SG TFTs with 50 and 100 nm thick Si layers were fabricated, with and without a $SiO_2$ C/L (as part of the gate insulator), using the µ-Czochralski process.

Figure 5.14 shows the schematic cross-sectional view of an n-channel SG TFT fabricated with a $SiO_2$ C/L using the µ-Czochralski process. The design of the SG Si TFT is explained in Section 2.3. In this design the channel of the TFT is shifted by 1.5 µm with respect to the grain filter so that the direction of current flow should be parallel to the CSL twin boundaries inside the Si

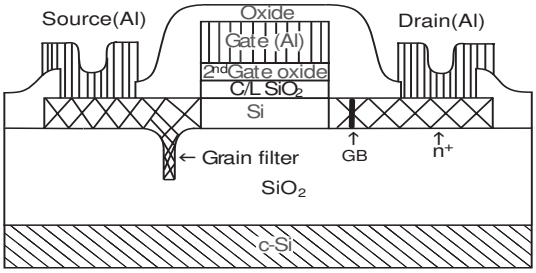


Figure 5.14: Schematic cross-sectional view of an n-channel SG Si TFT fabricated with a $SiO_2$ C/L, using the µ-Czochralski process.

islands. The channel length and width, measured by SEM, are 0.91 µm and 0.92 µm, respectively. Table 5.1 shows the characteristic values of n- and p-channel SG TFTs with 100 and 50 nm thick Si layers, with and without a $SiO_2$ C/L. It is readily seen that for both types of SG Si TFTs $\mu_{\mathrm{FE}}$ is higher and $S$ is lower when a $SiO_2$ C/L is used. The higher $\mu_{\mathrm{FE}}$ value is due to the larger grain size, which gives rise to an improvement in the bulk properties of Si, while the lower $S$ value strongly supports the idea that the interface between Si and $SiO_2$ is improved by laser irradiation, since $S$ is proportional to $D_{\mathrm{it}}$, as specified in Eq. (2.2).

| ***Characteristic Value*** | ***Si Thickness [nm]*** | ***With $SiO_2$ C/L*** | | ***Without $SiO_2$ C/L*** | |
|---|---|---|---|---|---|
| | | Electrons | Holes | Electrons | Holes |
| $\mu_{FE,e}$ $[cm^2/Vs]$ | 100 | 510 | 210 | 236 | 107 |
| | 50 | 405 | 177 | 210 | 95 |
| $S$ $[V/dec.]$ | 100 | 0.33 | 0.25 | 0.41 | 0.29 |
| | 50 | 0.25 | 0.31 | 0.40 | 0.37 |
| $V_{TH}$ $[V]$ | 100 | 1.3 | −0.98 | −1.1 | −4.3 |
| | 50 | 0.95 | −4.8 | 0.60 | −3.8 |
| $I_{OFF}$ $[A]$ | 100 | 4E-14 | 1E-14 | 1E-14 | 3E-14 |
| | 50 | 1E-14 | 1E-14 | 4E-13 | 4E-14 |

Table 5.1: Characteristic values of SG Si TFTs with a 100 nm thick gate insulator fabricated with and without a $SiO_2$ C/L.

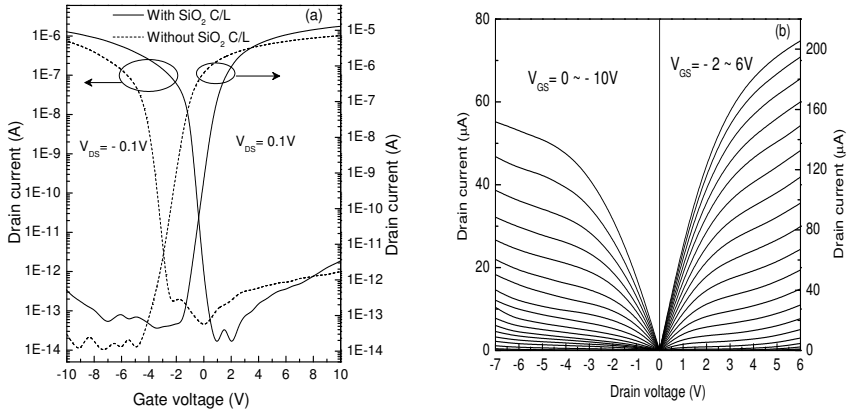


Figure 5.15: (a) Subthreshold characteristics and (b) output characteristic of a SG TFT with a 100 nm thick Si layer and a $SiO_2$ C/L.

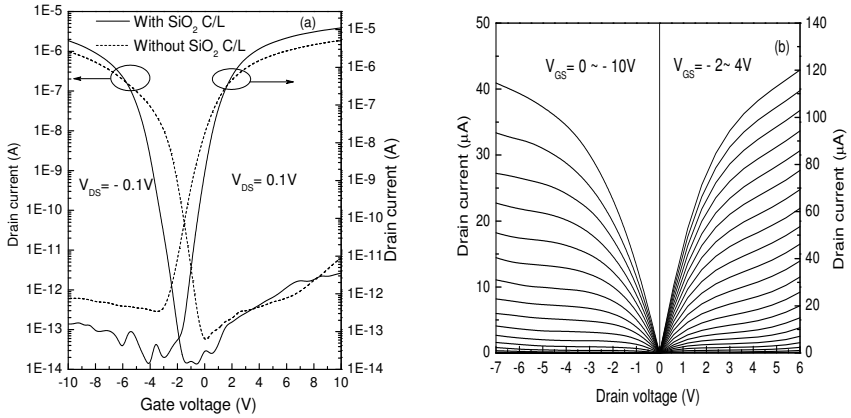


Figure 5.16: (a) Subthreshold characteristics and (b) output characteristic of a SG TFT with a 50 nm thick Si layer and a $SiO_2$ C/L.

Figures 5.15 and 5.16 show the subthreshold characteristics and the output characteristics for n- and p-channel SG Si TFTs with 100 and 50 nm thick Si

layers, respectively. It is evident from the subthreshold characteristics that in both (n- and p-channel) SG TFT types the on-current is higher when a $SiO_2$ C/L is applied. The output characteristics of SG Si TFTs with a $SiO_2$ C/L show low series resistance. Higher performance is offered by SG TFTs with a 100 nm than with a 50 nm thick Si layer because of the better microstructure inside the grain, due to the lower solidification rate of thicker Si layers. Thin Si layers thus have more planar defects and CSL GBs than thicker ones.

### 5.3.2 Single-Grain Inverters and Ring Oscillators

Crystallization of a-Si layers with a $SiO_2$ C/L using the µ-Czochralski process is a promising method to obtain high performance SG Si TFTs even with thin Si layers. To demonstrate the performance of these SG Si TFTs in circuits, we realized SG CMOS inverters and ring oscillators with thin Si films. We used the CMOS inverter and ring oscillator designs presented in Section 4.4.

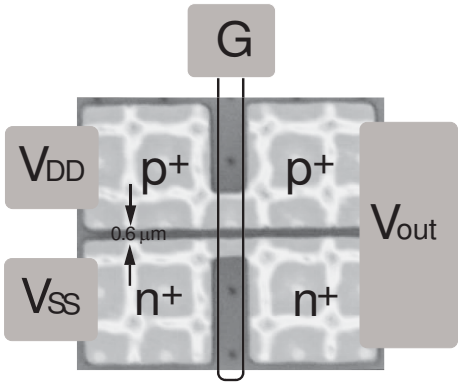


Figure 5.17: Optical image of a SG CMOS inverter made of TFTs.

In this design the n- and p-channel TFTs are both positioned inside a location-controlled single grain. The channel widths of the n- and p-channel TFTs, measured by SEM, are 1.43 µm and 2.75 µm, respectively, whereas the channel lengths are equal, 1.24 µm. Figure 5.17 shows the optical image of the SG CMOS inverter, with both channels inside a single grain. The theory and process flow for the fabrication of SG CMOS inverters and ring oscillators were presented in Section 4.4. We fabricated SG inverters and ring oscillators with 100 and 50 nm thick Si layers, using the newly developed method.

**Characteristics of Single-Grain Inverters and Ring Oscillators**

Figure 5.18 shows the static characteristics of single grain CMOS TFT inverters with 100 and 50 nm thick Si layers for various values of the supply voltage. The full swing between low and high voltages is clearly seen. The threshold voltage ($V_{\mathrm{inv}}$) of the inverters deviates from the ideal condition ($V_{\mathrm{inv}} = V_{\mathrm{DD}}/2$) because of the disparity in the on-currents for n-channel and the p-channel TFTs. The transition between low and high voltages is sharper for SG CMOS inverters with a 100 nm thick Si layer than with a 50 nm thick Si layer. This is due to the increased mobility in SG TFTs with a thick Si layer.

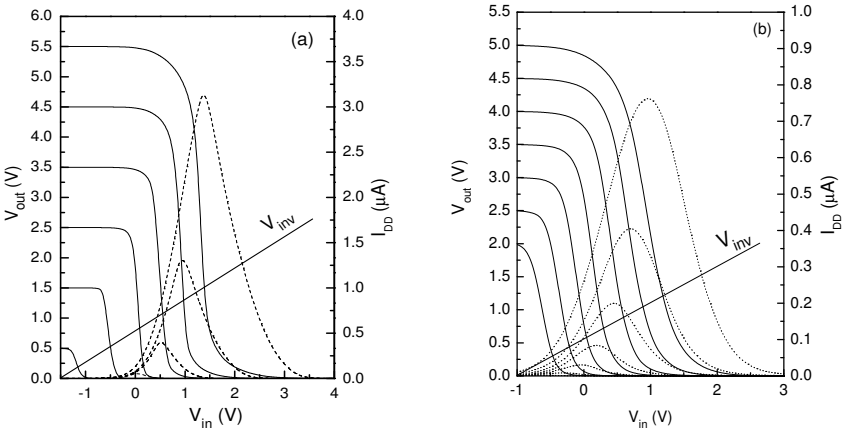


Figure 5.18: Static characteristics of SG CMOS TFT inverters with a (a) 100 nm; (b) 50 nm thick Si layer.

Figure 5.19 shows the dynamic characteristics of SG CMOS inverters with 100 nm and 50 nm thick Si layers at a supply voltage of 5 V. A constant frequency input pulse was applied to the gate of the inverter, and a constant supply voltage of 5 V was applied as $V_{\mathrm{DD}}$. The output of the inverter shows a 180° phase shift with respect to the input pulse. This guarantees the inverter-like operation of the SG CMOS inverter. The rise and fall times of the output pulse are 3.4 µs and 4.2 µs for 100 nm thick Si, and 7.5 µs and 9.7 µs for 50 nm thick Si. The smaller rise and fall times of the output pulse for SG CMOS inverters with thicker Si layers are due to the higher mobility in the TFTs.

To estimate the propagation gate delay, 101-stage ring oscillators were fab-

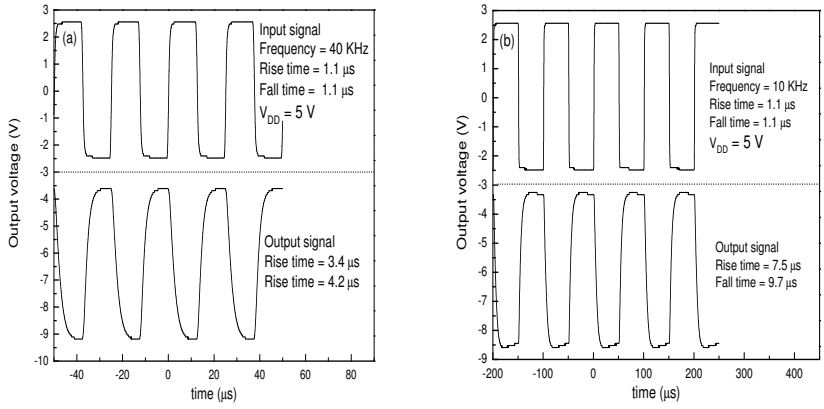


Figure 5.19: Dynamic characteristics of SG CMOS TFT inverters with (a) a 100 nm; (b) a 50 nm thick Si layer.

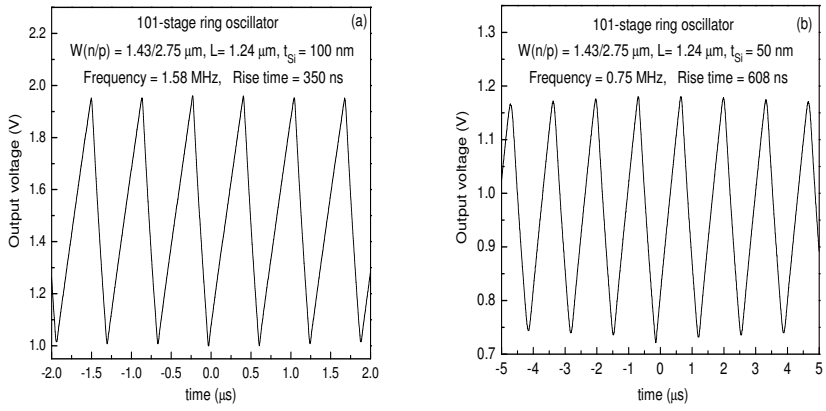


Figure 5.20: Dynamic characteristics of 101-stage ring oscillators with (a) a 100 nm; (b) a 50 nm thick Si layer, at a supply voltage of 8 V.

ricated by cascading SG CMOS TFT inverters with 100 and 50 nm thick Si layers in a circular chain. Figure 5.20 shows the dynamic characteristics of the ring oscillators at a supply voltage of 8 V. An oscillation frequency of 1.58 MHz was observed and a propagation gate delay of 3.1 ns was calculated in the ring oscillator made with 100 nm thick Si layers at a supply voltage of 8 V, while in the ring oscillator with 50 nm thick Si layers a frequency of 0.75 MHz and a propagation gate delay of 3.1 ns were found at the same supply voltage. The propagation gate delay is lower for 100 nm thick Si layers because of the better characteristic values of such SG TFTs.

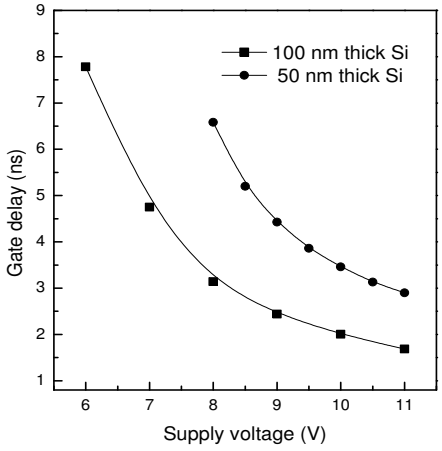


Figure 5.21: Gate delay as a function of the supply voltage.

Figure 5.21 shows the dependence of the gate delay on supply voltage for 50 and 100 nm thick Si layers. In both cases the dependence on the supply voltage is exponential.

## 5.4 Conclusion

The size of 2D location-controlled grains in thin Si layers is increased by employing a $SiO_2$ C/L on top of the Si layer prior to laser crystallization. The $SiO_2$ C/L serves as a heat reservoir during the solidification of the molten Si. This helps to elongate the lateral growth duration of Si even when the

$SiO_2$ layer is thin. Moreover, the optimum crystallization energy density is also smaller when a 50 nm thick $SiO_2$ C/L is used because of the decrease in the reflectance of the irradiated laser light. For thin Si layers, SG TFTs were fabricated inside location-controlled grains with and without a $SiO_2$ C/L. SG Si TFTs with a $SiO_2$ C/L have a $\mu_{FE,e}$ of 510 $cm^2/Vs$ and a $\mu_{FE,h}$ of 210 $cm^2/Vs$ when the Si thickness is 100 nm, and a $\mu_{FE,e}$ of 405 $cm^2/Vs$ and a $\mu_{FE,h}$ of 177 $cm^2/Vs$ when it is 50 nm. The higher carrier mobility for the 100 nm thick Si layer is due to the reduced number of CSL twin GBs inside the grain. On the other hand, the higher performance of SG Si TFTs with a $SiO_2$ C/L compared to TFTs without a C/L is due to the improved bulk properties of the Si grain and the improved interface between Si and $SiO_2$. SG CMOS TFT inverters with thin Si layers were fabricated inside location-controlled grains using the μ-Czochralski process. SG CMOS TFT inverters show a full swing between high and low logics. The propagation gate delay in a 101-stage ring oscillator was estimated to be 3.1 ns for 100 nm thick Si and 6.6 ns for 50 nm thick Si at a supply voltage of 8 V. This superior performance suggests that SG TFTs with thin Si layers provide an attractive possibility for future system circuit integration in AMLCDs and also for 3D integration of ICs.

# Chapter 6

# Conclusions and Recommendations

## 6.1 Conclusions

This thesis focuses on the design and fabrication of SG Si TFTs and circuits using the μ-Czochralski process in excimer laser crystallization at low temperatures ($< 350°C$). SG Si TFTs offer high performance, almost as high as SOI devices. Such high performance TFTs definitely improve the performance of circuits and increase the integration in AMLCD matrices. Furthermore, such TFTs can be suitable for system circuit integration on glass and also for 3D circuit integration. Below, the main conclusions of this research and some recommendations for the future are listed.

• SG Si TFTs designed with the channel position parallel to CSL twin GBs have higher electron mobility (597 $cm^2/Vs$) and subthreshold swing (0.21 V/dec.) than TFTs with the channel on top of the grain filter (471 $cm^2/Vs$ and 1.1 V/dec.). This dramatic improvement in the characteristic values is due to the fact that in this particular position CSL twin GBs originated from the grain filter are parallel to the direction of current flow. Similar trends are obtained for the mobility in p-channel SG Si TFTs. However, avoiding the grain filter does not lead to any significant improvement in the subthreshold swing. The highest hole mobility (273 $cm^2/Vs$) and subthreshold swing (0.14 V/dec.) values are obtained by choosing the channel position in such a way that the current direction should be parallel to CSL twin GBs.

• Crystallization with a longer-pulse excimer laser produces a better mi-

crostructure inside location-controlled Si grains because of the elongation of the solidification period. When the channel position is parallel to CSL twin GBs, SG Si TFTs fabricated with a longer-pulse excimer laser (SOPRA VEL15, pulse duration = 200 ns) have slightly higher $\mu_{FE,e}$ (644 $cm^2$/Vs) and $S$ (0.20 V/dec.) values than TFTs fabricated with a short-pulse excimer laser (XMR, pulse duration = 56 ns) [$\mu_{FE,e} = 597\,cm^2$/Vs, $S = 0.21$ V/dec.].

• The quality and size of location-controlled grains decrease for thinner Si films. This is due to the decreased solidification duration of the molten Si. Smaller grains with higher CSL GB densities are obtained for thin Si films. Consequently $\mu_{FE,e}$ is lower and $S$ is higher [375 $cm^2$/Vs and 0.30 V/dec. for n-channel, and 114 $cm^2$/Vs, and 0.22 V/dec. for p-channel SG Si TFTs] for 100 nm than for 250 nm thick Si films [597 $cm^2$/Vs, 0.21 V/dec.; and 273 $cm^2$/Vs, 0.14 V/dec.].

• For thin Si films the size of location-controlled grains is increased by using a thin $SiO_2$ C/L on top of the a-Si layer prior to crystallization. The thin $SiO_2$ C/L serves as an anti-reflection coating as well as a heat reservoir during crystallization. With a 50 nm thick $SiO_2$ C/L a grain diameter of 6.5 µm was achieved for a 50 nm thick Si layer, in comparison with a 3.5 µm grain without a $SiO_2$ C/L. This increase in the grain size is due to elongation of the solidification period, as the $SiO_2$ C/L stores the heat which then flows back to the molten Si when the temperature drops.

• The characteristic values show higher performance for SG Si TFTs fabricated using a $SiO_2$ C/L than for TFTs without a C/L. The higher performance is attributed to the larger grain size and smaller number of CSL twin GBs inside the grain. Moreover, SG TFTs with a $SiO_2$ C/L have a better $Si/SiO_2$ gate interface than TFTs without a $SiO_2$ C/L, since the C/L serves as a part of the gate insulator.

• These high performance TFTs were integrated into a SG CMOS inverter. The main feature of this inverter is that both (n- and p-channel) SG Si TFTs are inside a single grain. SG CMOS inverters show a full swing between high and low voltages, which guarantees digital operation. Propagation gate delay was estimated using a 101-stage ring oscillator, designed by cascading SG CMOS inverters in a circular chain. The propagation gate delay was measured to be 0.7 ns at 8 V for a 250 nm thick Si layer. The propagation gate delay is therefore shorter for the SG CMOS inverter than for a poly-Si device under the same conditions. This superior performance suggests that SG Si TFTs are attractive candidates for system circuit integration on glass and also for 3D circuit integration.

• The electrical reliability analysis of SG Si TFTs shows that they have better stability than poly-Si TFTs under hot carrier degradation, since SG Si

TFTs have no high-angle GBs. N-channel SG Si TFTs show a hump in the subthreshold characteristics with a negative gate bias stress, as hot holes are trapped at the side wall of the TFT, reducing the threshold voltage of the parasitic (side-wall) TFT, whereas acceptor trap states are generated in the p-channel SG Si TFT under this stress condition. On the other hand, n-channel SG Si TFTs are stable under positive gate field stress and p-channel SG Si TFTs show significant on-current degradation due to the generation of strain band tail states along with mid-band gap defects, which modify $V_{\mathrm{TH}}$ and $S$.

• The carrier transport mechanisms of both (n- and p-channel) SG Si TFT types were studied by calculating the activation energy of the drain current. Both SG Si TFT types have a negative activation energy in the on-regime. This strongly indicates that carrier transport in SG Si TFTs is governed by acoustic phonon scattering. This distinguishes SG Si TFTs from poly-Si TFTs, in which carrier transport mechanisms are dominated by the potential barrier.

## 6.2 Recommendations

This research opens an opportunity for the integration of SG Si TFTs with present low-temperature process technologies. However, there is still room for improvement in the performance of SG Si TFTs. Based on the work done and the experience gained during the past four years, I would like to make the following recommendations for future research.

• The threshold voltage of SG Si TFTs, especially p-channel devices, should be lowered for low-power applications. This can be done either by using a channel implantation that degrades the subthreshold swing or by modulating the work function of the gate material.

• A 3D computer simulation of SG Si TFTs should be performed to get an insight into the properties of the TFTs. The SG TFT structure is similar to the SOI structure except for the CSL GBs inside the single grain. It is therefore necessary to model the behavior of these CSL GBs during conduction in the TFT channel.

• To design circuits, the electrical parameters of SG Si TFTs have to be extracted from circuit simulations. A dedicated model is required for this because the characteristics of SG Si TFTs are different from what the existing models of poly-Si, SOI, and bulk Si MOSFET predict.

• The AC behavior of SG Si TFTs has to be analyzed, especially for analog applications.

• Circuits with SG TFTs should be designed in such a way that they are able to tolerate threshold voltage variations – as SG TFTs show large threshold

voltage variations.

- To minimize the variations in the characteristics, the crystallographic orientation of the Si grains must be controlled.

# Appendix A

# Flow Chart

## A.1 Fabrication of SG Si CMOS Inverters

1. **Substrate:** n-type ⟨100⟩ Si wafer $\rho = 7$–$21\ \Omega \cdot \mathrm{cm}$
2. **First marker oxidation**
3. **Measurement:** Oxide thickness on Leitz MPV-SP
4. **Coating and baking:** 1.4 µm Shipley SPR 3012, 95°C 1 minute
5. **Alignment and exposure:** Define the alignment marks
6. **Development:** 115°C 1 minute Shipley MF 322, 100°C 1 minute
7. **Number the wafers:** Use a glass pen
8. **Etching of oxide:** BHF (1:7), hydrophobic
9. **Cleaning:** Strip the photoresist in acetone 40°C, $HNO_3$ (100%) 10 minutes, rinse in demineralized water 3 minutes, $HNO_3$ (65%) 10 minutes, rinse in demineralized water 3 minutes, and dry
10. **Second marker oxidation**
11. **Measurement:** Oxide thickness on Leitz MPV-SP
12. **Coating and baking:** 1.4 µm Shipley SPR 3012, 95°C 1 minute
13. **Alignment and exposure:** Define the grain filter
14. **Development:** 115°C 1 minute Shipley MF 322, 100°C 1 minute
15. **Etching of oxide:** RIE 384T, $C_2F_6$:$CHF_3$ = 36:144 sccm, $p = 0.24$ mbar, $P = 300$ W, $t = 100$ s
16. **Cleaning:** Strip the photoresist in oxygen plasma, $HNO_3$ (100%) 10 minutes, rinse in demineralized water 3 minutes, $HNO_3$ (65%) 10 minutes, rinse in demineralized water 3 minutes and dry
17. **Oxide deposition:** PECVD TEOS oxide, $t = 870$ nm, TOES = 1.8 ml/min,

$O_2$ = 5 slm, $T = 350°C$, $p = 2.93$ mbar, $P = 1$ kW

18. **Deposition of a-Si:** LPCVD, $T = 550°C$, $p = 150$ mTorr, $SiH_4$ = 45 sccm
19. **Channel implantation:** Boron ions for p-channel or phosphorus ions for n-channel, $E$ = 5–30 keV, Dose = 1E12/cm$^2$
20. **Crystallization:** Excimer laser ($\lambda$ = 308 nm, pulse duration = 56 ns) $E = 1.2$ J/cm$^2$
21. **Cleaning:** $HNO_3$ (100%) 10 minutes, rinse in demineralized water 3 minutes, $HNO_3$ (65%) 10 minutes, rinse in demineralized water 3 minutes, and dry
22. **Oxygen plasma treatment:** Seiko-Epson, Japan
23. **Cleaning:** $HNO_3$ (100%) 10 minutes, rinse in demineralized water 3 minutes, $HNO_3$ (65%) 10 minutes, rinse in demineralized water 3 minutes, and dry
24. **Coating and baking:** 1.4 µm Shipley SPR 3012, 95°C 1 minute
25. **Alignment and exposure:** Define the Si island
26. **Development:** 115°C 1 minute Shipley MF 322, 100°C 1 minute
27. **RIE Etching of poly-Si:** Trikon Omega 201 plasma etcher, $T = 20°C$
28. **Cleaning:** Strip the photoresist in oxygen plasma, $HNO_3$ (100%) 10 minutes, rinse in demineralized water 3 minutes, $HNO_3$ (65%) 10 minutes, rinse in demineralized water 3 minutes and dry
29. **Gate oxide deposition:** ECR-PECVD oxide deposition at Seiko-Epson, Japan
30. **Cleaning:** $HNO_3$ (100%) 10 minutes, rinse in demineralized water 3 minutes, $HNO_3$ (65%) 10 minutes, rinse in demineralized water 3 minutes, and dry
31. **First metallization:** Sputtering of Al/Si, $t = 0.6$ µm, $T = 25°C$ in Trikon SIGMA
32. **Coating and baking:** 2.0 µm Shipley SPR 3017, 95°C 1 minute
33. **Alignment and exposure:** Define metal gate
34. **Development:** 115°C 1 minute Shipley MF 322, 100°C 1 minute
35. **Aluminium etching:** Trikon Omega 201 plasma etcher, $T = 25°$ C
36. **Aluminium fence removal:** Etchant $H_3PO_4$ (85%), $HNO_3$ (65%), $CH_3COOH$ (100%), and deionized water, $t = 30$ s
37. **Etching of oxide:** RIE 384T, $C_2F_6$:$CHF_3$ = 36:144 sccm, $p = 0.24$ mbar, $P = 300$ W.
38. **Cleaning:** Strip the photoresist in oxygen plasma, $HNO_3$ (100%) 10 minutes, rinse in demineralized water 3 minutes, rinse in demineralized water 3 minutes, and dry
39. **Source and drain implantation:** Boron ions for p-channel or phosphorus ions for n-channels, $E$ = 5–30 keV, Dose = 1E16/cm$^2$

40. **Cleaning:** $HNO_3$ (100%) 10 minutes, rinse in demineralized water 3 minutes, rinse in demineralized water 3 minutes, and dry
41. **Activation of dopants:** Excimer-laser annealing $E = 0.3$ J/cm$^2$, 80% overlap at room temperature.
42. **Cleaning:** $HNO_3$ (100%) 10 minutes, rinse in demineralized water 3 minutes, rinse in demineralized water 3 minutes, and dry
43. **Oxide deposition:** PECVD TEOS oxide, $t = 800$ nm, TOES = 1.8 ml/min, $O_2$ = 5 slm, $T = 350°$C, $p = 2.93$ mbar, $P = 1$ kW
44. **Etching of oxide:** RIE 384T, $C_2F_6$:$CHF_3$ = 36:144 sccm, $p = 0.24$ mbar, $P = 300$ W
45. **Oxide deposition:** PECVD TEOS oxide, $t = 600$ nm, TOES = 1.8 ml/min, $O_2$ = 5 slm, $T = 350°$C, $p = 2.93$ mbar, $P = 1$ kW
46. **Coating and baking:** 2.0 µm Shipley SPR 3017, 95°C 1 minute
47. **Alignment and exposure:** Open the contact hole to Si only-CO1
48. **Development:** 115°C 1 minute Shipley MF 322, 100°C 1 minute
49. **Etching of oxide:** RIE 384T, $C_2F_6$:$CHF_3$ = 36:144 sccm, $p = 0.24$ mbar, $P = 300$ W
50. **Cleaning:** Strip the photoresist in oxygen plasma, $HNO_3$ (100%) 10 minutes, rinse in demineralized water 3 minutes, rinse in demineralized water 3 minutes, and dry
51. **Dip etch:** HF 0.55%, $t = 2$ minutes
52. **Second metallization:** Sputtering of Al/Si, $t = 0.6$ µm, $T = 25°$C in Trikon SIGMA
53. **Coating and baking:** Negative photoresist, AZ 5214E, 95°C 1 minute
54. **Alignment and exposure:** Use the mask CO1 again
55. **Development:** 115°C 1 minute Shipley MF 322, 100°C 1 minute
56. **Aluminium etching:** Trikon Omega 201 plasma etcher $T = 25°$C
57. **Aluminium fence removal:** Etchant $H_3PO_4$ (85%), $HNO_3$, (65%), $CH_3COOH$ (100%) and deionized water, $t = 30$ s
58. **Cleaning:** Strip the photoresist in oxygen plasma, $HNO_3$ (100%) 10 minutes, rinse in demineralized water 3 minutes, rinse in demineralized water 3 minutes, and dry
59. **Coating and baking:** 2.0 µm Shipley SPR 3017, 95°C 1 minute
60. **Alignment and exposure:** Open the contact hole to Al gate only-CO2
61. **Development:** 115°C 1 minute Shipley MF 322, 100°C 1 minute
62. **Etching of oxide:** RIE 384T, $C_2F_6$:$CHF_3$ = 36:144 sccm, $p = 0.24$ mbar, $P = 300$ W
63. **Cleaning:** Strip the photoresist in oxygen plasma, $HNO_3$ (100%) 10 minutes, rinse in demineralized water 3 minutes, rinse in demineralized water 3 minutes, and dry

64. **Third metallization:** Sputtering of Al/Si with RF power, $t = 1.2$ µm, $T = 25°C$ in Trikon SIGMA
65. **Coating and baking:** 2.0 µm Shipley SPR 3017, 95°C 1 minute
66. **Alignment and exposure:** Define the Al PAD
67. **Development:** 115°C 1 minute Shipley MF 322, 100°C 1 minute
68. **Aluminium etching:** Trikon Omega 201 plasma etcher $T = 25°C$
69. **Aluminium fence removal:** Etchant $H_3PO_4$ (85%), $HNO_3$, (65%), $CH_3COOH$ (100%) and deionized water, $t = 30$ s
70. **Cleaning:** $HNO_3$ (100%) 10 minutes, rinse in demineralized water 3 minutes, rinse in demineralized water 3 minutes, and dry

## A.2 Fabrication of SG Si TFTs

1. **Substrate:** n-type ⟨100⟩ Si wafer $\rho = 7$–$21\ \Omega \cdot \mathrm{cm}$
2. **First marker oxidation**
3. **Measurement:** Oxide thickness on Leitz MPV-SP
4. **Coating and baking:** 1.4 µm Shipley SPR 3012, 95°C 1 minute
5. **Alignment and exposure:** Define the alignment marks
6. **Development:** 115°C 1 minute Shipley MF 322, 100°C 1 minute
7. **Number the wafers:** Use a glass pen
8. **Etching of oxide:** BHF (1:7), hydrophobic
9. **Cleaning:** Strip the photoresist in acetone 40°C, $HNO_3$ (100%) 10 minutes, rinse in demineralized water 3 minutes, $HNO_3$ (65%) 10 minutes, rinse in demineralized water 3 minutes, and dry
10. **Second marker oxidation**
11. **Measurement:** Oxide thickness on Leitz MPV-SP
12. **Coating and baking:** 1.4 µm Shipley SPR 3012, 95°C 1 minute
13. **Alignment and exposure:** Define the grain filter
14. **Development:** 115°C 1 minute Shipley MF 322, 100°C 1 minute
15. **Etching of oxide:** RIE 384T, $C_2F_6$:$CHF_3$ = 36:144 sccm, $p = 0.24$ mbar, $P = 300$ W, $t = 100$ s
16. **Cleaning:** Strip the photoresist in oxygen plasma, $HNO_3$ (100%) 10 minutes, rinse in demineralized water 3 minutes, $HNO_3$ (65%) 10 minutes, rinse in demineralized water 3 minutes and dry
17. **Oxide deposition:** PECVD TEOS oxide, $t = 870$ nm, TOES = 1.8 ml/min, $O_2$ = 5 slm, $T = 350°C$, $p = 2.93$ mbar, $P = 1$ kW
18. **Deposition of a-Si:** LPCVD, T = 550°C, $p = 150$ mTorr $SiH_4 = 45$ sccm, $t = 250$ nm, 100 nm, 50 nm
19. **Channel implantation:** Boron or phosphorus ions, $E$ = 5–30 keV, Dose

$= 1E12/cm^2$

20. **Crystallization:** Excimer laser ($\lambda$ = 308 nm, pulse duration = 56 ns) $E = 1.2$ J/cm$^2$
21. **Cleaning:** $HNO_3$ (100%) 10 minutes, rinse in demineralized water 3 minutes, $HNO_3$ (65%) 10 minutes, rinse in demineralized water 3 minutes, and dry
22. **Oxygen plasma treatment:** Seiko-Epson, Japan
23. **Cleaning:** $HNO_3$ (100%) 10 minutes, rinse in demineralized water 3 minutes, $HNO_3$ (65%) 10 minutes, rinse in demineralized water 3 minutes, and dry
24. **Coating and baking:** 1.4 µm Shipley SPR 3012, 95°C 1 minute
25. **Alignment and exposure:** Define the Si island
26. **Development:** 115°C 1 minute Shipley MF 322, 100°C 1 minute
27. **RIE Etching of poly-Si:** Trikon Omega 201 plasma etcher, $T = 20$°C
28. **Cleaning:** Strip the photoresist in oxygen plasma, $HNO_3$ (100%) 10 minutes, rinse in demineralized water 3 minutes, $HNO_3$ (65%) 10 minutes, rinse in demineralized water 3 minutes, and dry
29. **Gate oxide deposition:** ECR-PECVD oxide deposition at Seiko-Epson, Japan
30. **Cleaning:** $HNO_3$ (100%) 10 minutes, rinse in demineralized water 3 minutes, $HNO_3$ (65%) 10 minutes, rinse in demineralized water 3 minutes, and dry
31. **First metallization:** Sputtering of Al/Si, $t = 0.6$ µm, $T = 25$°C in Trikon SIGMA
32. **Coating and baking:** 2.0 µm Shipley SPR 3017, 95°C 1 minute
33. **Alignment and exposure:** Define metal gate
34. **Development:** 115°C 1 minute Shipley MF 322, 100°C 1 minute
35. **Aluminium etching:** Trikon Omega 201 plasma etcher $T = 25$°C
36. **Aluminium fence removal:** Etchant $H_3PO_4$ (85%), $HNO_3$, (65%), $CH_3COOH$ (100%) and deionized water, $t = 30$ s
37. **Etching of oxide:** RIE 384T, $C_2F_6$:$CHF_3$ = 36:144 sccm, $p = 0.24$ mbar, $P = 300$ W.
38. **Cleaning:** Strip the photoresist in oxygen plasma, $HNO_3$ (100%) 10 minutes, rinse in demineralized water 3 minutes, rinse in demineralized water 3 minutes, and dry
39. **Source and drain implantation:** Boron or phosphorus ions, $E$ = 5–30 keV, Dose = 1E16/cm$^2$
40. **Cleaning:** $HNO_3$ (100%) 10 minutes, rinse in demineralized water 3 minutes, rinse in demineralized water 3 minutes, and dry
41. **Activation of dopants:** Excimer-laser annealing $E = 0.3$ J/cm$^2$, 80% over-

lap at room temperature.
42. **Cleaning:** $HNO_3$ (100%) 10 minutes, rinse in demineralized water 3 minutes, rinse in demineralized water 3 minutes, and dry
43. **Oxide deposition:** PECVD TEOS oxide, $t = 800$ nm, TOES = 1.8 ml/min, $O_2$ = 5 slm, $T = 350°C$, $p = 2.93$ mbar, $P = 1$ kW
44. **Etching of oxide:** RIE 384T, $C_2F_6$:$CHF_3$ = 36:144 sccm, $p = 0.24$ mbar, $P = 300$ W
45. **Oxide deposition:** PECVD TEOS oxide, $t = 600$ nm, TOES = 1.8 ml/min, $O_2$ = 5 slm, $T = 350°C$, $p = 2.93$ mbar, $P = 1$ kW
46. **Coating and baking:** 2.0 µm Shipley SPR 3017, 95°C 1 minute
47. **Alignment and exposure:** Open the contact hole to Si and Al gate (Clean room class 100, front side)
48. **Development:** 115°C 1 minute Shipley MF 322, 100°C 1 minute
49. **Etching of oxide:** RIE 384T, $C_2F_6$:$CHF_3$ = 36:144 sccm, $p = 0.24$ mbar, $P = 300$ W
50. **Cleaning:** Strip the photoresist in oxygen plasma, $HNO_3$ (100%) 10 minutes, rinse in demineralized water 3 minutes, rinse in demineralized water 3 minutes, and dry
51. **Dip etch:** HF 0.55%, $t = 2$ minutes
52. **Second metallization:** Sputtering of Al/Si, $t = 1.2$ µm, $T = 25°C$ in Trikon SIGMA
53. **Coating and baking:** 2.0 µm Shipley SPR 3017, 95°C 1 minute
54. **Alignment and exposure:** Define the Al PAD
55. **Development:** 115°C 1 minute Shipley MF 322, 100°C 1 minute
56. **Aluminium etching:** Trikon Omega 201 plasma etcher $T = 25°C$
57. **Aluminium fence removal:** Etchant $H_3PO_4$ (85%), $HNO_3$, (65%), $CH_3COOH$ (100%) and deionized water, $t = 30$ s
58. **Cleaning:** $HNO_3$ (100%) 10 minutes, rinse in demineralized water 3 minutes, rinse in demineralized water 3 minutes, and dry

## A.3 Fabrication of MOS Capacitors

1. **Substrate:** p- or n-type ⟨100⟩ Si wafer $\rho = 0.1$–$1\ \Omega \cdot cm$
2. **Cleaning:** $HNO_3$ (65%) 10 minutes, rinse in demineralized water 3 minutes, and dry
3. **Dip etch:** HF 0.55%, $t = 2$ minutes
4. **Oxide deposition:** TEOS-PECVD oxide or ECR-PECVD oxide
5. **Metallization:** Sputtering of Al/Si, $t = 0.6$ µm, $T = 25°C$ in Trikon SIGMA on front side of wafer

6. **Dip etch: for back side:** HF (1:7), $t = 2$ minutes
7. **Metallization:** Sputtering of Al/Si, $t = 0.6$ µm, $T = 25°C$ in Trikon SIGMA on back side of wafer
8. **Coating and baking:** 2.0 µm Shipley SPR 3017, 95°C 1 minute
9. **Alignment and exposure:** Define metal gate
10. **Development:** 115°C 1 minute Shipley MF 322, 100°C 1 minute
11. **Aluminium etching:** Trikon Omega 201 plasma etcher $T = 25°C$
12. **Cleaning:** Strip the photoresist in oxygen plasma, $HNO_3$ (100%) 10 minutes, rinse in demineralized water 3 minutes, and dry
13. **Coating and baking:** HMDS only

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# Summary

The scope of applications for thin-film transistors (TFTs) is continuously expanding. The realization of high-speed electronic systems on an arbitrary substrate (e.g., glass or flexible polymers) generally requires high-quality silicon grains. Excimer laser crystallization of a-Si is an attractive technique for realizing low-temperature ($< 350°C$) poly-Si TFTs on an arbitrary substrate. The performance of poly-Si TFTs is limited by the small grains and the GBs. Therefore, enlargement of the grains and elimination of the GBs from the TFT channel are indispensable for achieving high performance TFTs. Using the μ-Czochralski process, the location of large grains can be controlled in 2D. GBs are thus eliminated by placing the TFT channel inside a location-controlled grain. In this way, a TFT inside a single grain (i.e., a SG Si TFT) can be fabricated. The present research focused on the development of high performance SG Si TFTs and circuits fabricated using the μ-Czochralski process.

First, low-temperature ($< 350°C$) ECR-PECVD and TEOS-PECVD oxides were characterized by capacitance-voltage measurements on MOS structures. The defect densities of interface states were estimated to be $2.1 \times 10^{10}\,\mathrm{cm^{-2}\,eV^{-1}}$ and $1.02 \times 10^{11}\,\mathrm{cm^{-2}\,eV^{-1}}$ for ECR-PECVD and TEOS-PECVD oxides, respectively. The density of interface states for ECR-PECVD oxides is comparable to that of thermal oxides ($1.07 \times 10^{10}\,\mathrm{cm^{-2}\,eV^{-1}}$).

The characteristic values of n-channel SG Si TFTs fabricated inside location-controlled grains with the μ-Czochralski process are $\mu_{\mathrm{FE,e}} = 430\,\mathrm{cm^2/Vs}$ and $S = 0.45$ V/dec. [31]. Their performance might be limited by CSL twin GBs, originated inside the location-controlled grains. The performance of SG Si TFTs can be improved to approach the performance of SOI transistors by positioning the TFT channel parallel to these CSL twin GBs. N-channel SG Si TFTs with a 250 nm thick Si layer then have a mobility of 597 $\mathrm{cm^2/Vs}$ and a subthreshold swing of 0.21 V/dec., while for p-channel SG Si TFTs the mobility is 273 $\mathrm{cm^2/Vs}$ and the subthreshold swing is 0.14 V/dec. This

higher performance is attributed to the fact that carriers do not encounter CSL boundaries because these are parallel to the direction of current flow.

The electrical reliability of SG Si TFTs was investigated under high drain and high gate voltage stress. SG Si TFTs offer better stability than poly-Si TFTs under high drain bias stress due to the absence of high-angle GBs. Both (n- and p-channel) SG Si TFTs were stressed under high gate field stress. For negative stress, n-channel SG Si TFTs show a hump in the subthreshold region, as hot holes are trapped at the side wall of the TFT, reducing the threshold voltage of the parasitic (side-wall) TFT, whereas acceptor trap states are generated in p-channel SG Si TFTs. On the other hand, n-channel SG Si TFTs are stable against positive gate field stress and p-channel SG Si TFTs show a significant degradation in the on-current due to the generation of strain band tail states and mid-band gap defects, which modify the threshold voltage and the subthreshold swing.

Carrier transport mechanisms were investigated for both (n- and p-channel) SG Si TFT types. They both have a negative activation energy in the on-regime. This strongly indicates that carrier transport in SG Si TFTs is governed by acoustic phonon scattering. This distinguishes SG Si TFTs from poly-Si TFTs, in which carrier transport mechanisms are dominated by the potential barrier.

Next, these SG Si TFTs were integrated in a CMOS inverter. The design of digital CMOS inverters had both (n- and p-channel) TFTs placed inside a single grain, i.e. a single-grain (SG) CMOS inverter was realized. The channel width was 1.43 µm for n-channel and 2.75 µm for p-channel TFTs, whereas the channel length was 1.24 µm in both cases. A full swing was observed between low and high logics. To estimate the propagation gate delay of SG CMOS inverters accurately, a 101-stage ring oscillator was designed by cascading SG CMOS inverters in a circular chain. The gate delay was estimated to be 0.7 ns at a supply voltage of 8 V, which is shorter than in similar devices produced by any other existing low-temperature technology under the given device conditions ($L = 1.24$ µm, supply voltage = 8 V).

Generally, transistors with thin ($\sim$ 70 nm) films are required to avoid short-channel effects and to ensure compatibility with low-temperature poly-Si (LTPS) TFT production methods. However, the quality and size of the grain decrease for thinner Si films. The size of the 2D location-controlled Si grain in thin Si films is increased by employing a capping layer of $SiO_2$ on top of the a-Si layer during the laser crystallization phase. The $SiO_2$ capping layer serves as a heat reservoir during the solidification of the molten Si layer. This helps to increase the lateral growth duration of Si even for thin $SiO_2$ layers. Moreover, the optimum crystallization energy density also decreases when a

50 nm thick $SiO_2$ capping layer is used because of the decreased reflectance of laser light. By employing a 50 nm thick capping layer on top of a 100 (50) nm thick Si film, the grain size is increased up to 7.5 (6.5) µm compared to 5.2 (3.5) µm without a $SiO_2$ capping layer.

For thin Si films, SG TFTs were fabricated inside location-controlled grains with a $SiO_2$ capping layer, which served as a part of the gate insulator. The carrier mobilities for SG Si TFTs with a $SiO_2$ C/L were $\mu_{FE,e} = 510\,cm^2/Vs$ and $\mu_{FE,h} = 210\,cm^2/Vs$ for a 100 nm thick Si layer and $\mu_{FE,e} = 405\,cm^2/Vs$ and $\mu_{FE,h} = 177\,cm^2/Vs$ for a 50 nm thick Si layer. The higher carrier mobility of the 100 nm thick layer is due to the smaller number of CSL twin GBs inside the grain. On the other hand, SG Si TFTs with a $SiO_2$ C/L offer higher performance than TFTs without a $SiO_2$ C/L because of the improved bulk properties of the Si grain and the improved interface between Si and $SiO_2$. SG CMOS TFT inverters with a thin Si layer were fabricated inside a location-controlled grain. The propagation gate delay in a 101-stage ring oscillator was estimated to be 6.6 ns for 50 nm thick Si and 3.1 ns for 100 nm thick Si at a supply voltage of 8 V. This superior performance suggests that SG TFTs with a thin Si layer are attractive candidates for system circuit integration in AMLCDs and also for the 3D integration of ICs.

# Samenvatting

Het toepassingsgebied voor dunne-film transistoren (thin-film transistors, TFTs) breidt zich onophoudelijk uit. Het maken van snelle elektronische systemen op willekeurige substraten (b.v., glas of flexibele polymeren), vereist siliciumkorrels van uitstekende kwaliteit. Excimer-laserkristallisatie van a-Si is een goede techniek om bij lage temperatuur poly-Si TFTs op een willekeurig substraat te realiseren. De prestatie van poly-Si TFTs wordt beperkt door de kleine korrelgrootte en de korrelgrenzen. Daarom is het vergroten van de korrels en het verwijderen van de korrelgrenzen van het TFT kanaal een eerste vereiste voor het realiseren van TFTs van hoge kwaliteit. Wanneer vooraf de locatie van de korrels bekend is kan in het fabricage proces het TFT kanaal zo geplaatst worden dat het kanaal korrelgrens vrij is en de gehele TFT binnen één enkele korrel wordt gefabriceerd. Voor het controleren van de locatie van de korrels in 2D kan het µ-Czochralski proces worden gebruikt. Het huidige onderzoek concentreerde zich op de van Si TFTs van hoge kwaliteit Si TFT's uit een enkele korrel en circuits vervaardigd met het µ-Czochralski proces.

Eerst werden de oxides ECR-PECVD en TEOS-PECVD bij lage temperatuur ($< 350^{\circ}$C) gekarakteriseerd met capaciteit-spanning metingen op MOS structuren. De dichtheid van interface toestanden werd geschat op $2,1 \times 10^{10}\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$ voor ECR-PECVD oxide en $1,02 \times 10^{11}\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$ voor TEOS-PECVD oxide. De dichtheid van interface toestanden is voor ECR-PECVD oxide vergelijkbaar met dat van thermische oxides ($1,07 \times 10^{10}\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$).

Kenmerkende waarden voor een enkel-korrellig n-kanaal van Si vervaardigd binnen plaats-gecontroleerde TFTs met het µ-Czochralski proces zijn $\mu_{\mathrm{FE,e}} = 430\,\mathrm{cm}^2/\mathrm{Vs}$ en $S = 0.45$ V/dec. [31] De prestatie van TFTs uit een enkele korrel wordt wellicht beperkt door het voorkomen van CSL tweeling korrelgrenzen binnen de plaats-gecontroleerde korrels. Door het TFT kanaal parallel te plaatsen aan de CSL tweeling korrelgrenzen kunnen de prestaties van Si TFTs uit een enkele korrel dusdanig worden verbeterd dat zij de prestaties van SOI

transistoren benaderen. N-type Si TFTs uit een enkele korrel met een Si laag van 250 nm dikte hebben een mobiliteit van 597 $cm^2/Vs$ en de helling beneden de drempelspanning is 0,21 V/dec., terwijl p-type Si TFTs uit een enkele korrel een mobiliteit van 273 $cm^2/Vs$ hebben en de hellings onder de drempelspanning 0,14 V/dec is. Deze betere prestatie wordt toegeschreven aan het feit dat de ladingsdragers geen CSL grenzen tegenkomen omdat deze parallel staan aan de richting van de stroom.

De elektronische betrouwbaarheid van Si TFTs uit een enkele korrel werd onderzocht door hoge spanningen op de gate en drain te zetten. Wanneer een hoge spanning op de drain wordt gezet, zijn TFTs uit een enkele korrel stabieler dan poly-Si TFTs. Dit komt doordat in een TFT uit een enkele korrel geen korrelgrenzen onder een grote hoek staan. Voor zowel n- als voor p-kanaal Si TFTs uit een enkele korrel werden hoge spanningen op de gate gezet. Wanneer er een negatieve spanning op een n-kanaal TFT uit een enkele korrel wordt gezet, verschijnt er een bobbel in dekarakestristiek van de TFT onder de drempelspanning. Deze bobbel wordt veroorzaakt door "hete" gaten die worden ingevangen door de "side wall" van de TFT, waar door deze de drempelspanning verlagen van de paracitaire (side-wall) TFT. Dit in tegenstelling tot een p-kanaal TFT, waar bij een hoge gate spanning acceptor toestanden worden gecrëeert. N-kanaal TFTs uit een enkele korrel zijn echter wel stabiel wanneer er een positieve gate spanning wordt toegepast. In dit geval vertoont een p-kanaal TFT een sterke degradatie in de aan-stroom door generatie van "strained band tail" toestanden en mid-bandgap toestanden, omdat deze de drempel spanning veranderen en de beneden drempelspanning schommeling.

De transport mechanismen werden onderzocht van de ladingdragers voor zowel n- als p-kanaal Si TFT uit een enkele korrel. Beide hebben een negatieve activeringsenergie wanneer het kanaal aan is. Dit wijst er sterk op dat het transport van ladingdragers in de enkel-korrelige Si TFTs sterk beïnvloed wordt door akoestische fonon verstrooiing. Dit onderscheidt enkel-korrelige Si TFTs van poly-Si TFTs, waarin de mechanismen voor het transport van ladingsdragers vooral door de potentiaal barrieres worden bïnvloed.

Daarna werden deze enkel-korrelige Si TFTs geïntegreerd in een CMOS inverter. In het ontwerp van de digitale CMOS inverters worden zowel de n- als de p-kanaal TFTs binnen een enkele korrel geplaatst, d.w.z. werd de hele CMOS inverter binnen een korrel gerealiseerd. De kanaalbreedte was 1,43 µm voor n-kanaal en 2,75 µm voor p-kanaal TFTs, terwijl de kanaallengte in beide gevallen 1,24 µm was. Een volledige omschakeling tussen hoog en laag niveau werd waargenomen. Om de vertraging van de enkel-korrelige CMOS inverters nauwkeurig te schatten, werd een ringsoscillator ontworpen door 101 enkel-korrelige CMOS inverters in serie te schakelen in een lus. De vertraging

werd geschat op 0,7 ns bij een voedingsspanning van 8 V Dit is sneller dan in enig ander lage temperatuur technologie is bereikt voor vergelijkbare circuits en componenten met (L = 1,24 µm en de voedingssaspnning = 8 V).

Over het algemeen worden transistoren met dunne ( 70 nm) films vereist om de effecten van een kort kanaal te vermijden en om poly-Si (LTPS) TFTs bij lage temperatuur te kunnen fabriceren. Echter, de kwaliteit en de grootte van de korrel worden slechter wanneer men dunne Si films gebruikt. De grootte van de 2D gecontroleerde korrel in een dunne film van Si wordt beter wanneer de a-Si laag is afgedekt met een laag van $SiO_2$ tijdens de laserkristallisatie. Het afdekken met een $SiO_2$ laag zorgt ervoor dat het gesmolten Si langzamer stolt. Dit helpt de laterale groei van de kristallen, zelfs voor dunne $SiO_2$ lagen. Tevens is minder laser-vermogen nodig wanneer een 50 nm dikke $SiO_2$ laag wordt gebruikt, omdat de reflectie wordt verminderd. Door een 50 nm dikke afdeklaag bovenop een Si film van 100 (50) nm dikte te plaatsen, wordt de korrelgrootte verhoogd tot 7,5 (6.5) µm in plaats van 5,2 (3.5) µm zonder een afdeklaag van $SiO_2$.

Met behulp van een afdekklaag hebben we TFTs uit een enkele korrel vervaardigd, waarbij de $SiO_2$ afdeklaag tevens als gate isolator diende. De mobilitiseten van de ladingdragers in enkel-korrelige Si TFTs met een $SiO_2$ afdeklaag waren $\mu_{FE,e} = 510\,cm^2/Vs$ en $\mu_{FE,h} = 210\,cm^2/Vs$ voor een Si laag van 100 nm dikte en $\mu_{FE,e} = 405\,cm^2/Vs$ en $\mu_{FE,h} = 177\,cm^2/Vs$ voor een Si laag van 50 nm dikte. De hogere ladingsdrager mobiliteit van de 100 nm dikke laag is toe te schrijven aan een kleiner aantal CSL tweeling grenzen binnen de korrel. Aan de andere kant leveren de Si TFTs uit een enkele korrel met $SiO_2$ afdeklaag hogere prestaties dan TFTs zonder een $SiO_2$ afdeklaag vanwege de betere bulkeigenschappen van de Si korrel en het betere interface tussen Si en $SiO_2$. CMOS TFT inverters zijn vervaardigd binnen een enkele locatie-gecontroleerde korrel. De vertraging van de inverters in een 101-stadium ringsoscillator werd geschat op 6,6 ns voor 50 nm dikke Si en 3,1 ns voor 100 nm dikke Si bij een voedingsspanning van 8 V. Door deze superieure prestaties zijn enkel-korrelige TFTs van een dunne laag van Si aantrekkelijke kandidaten voor de integratie van circuits in AMLCDs en ook voor de 3D integratie van ICs.

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# About the Author

Vikas Rana was born in Meerut, India in 1977. He received his M.Sc. degree in physics from C.C.S. University Meerut in 1999. He was awarded the Master of Technology (M. Tech.) degree in Solid State Materials in 2001 from the Indian Institute of Technology, Delhi. Since 2002 he has been working as a research member at the Delft Institute of Microelectronics and Submicrontechnology (DIMES), Delft, Netherlands. He has been an active member of the Laboratory of Electronic Components, Technology and Materials (ECTM) as a Ph.D. student. His main research activities focus on the location control of grains through a novel excimer laser crystallization method and the fabrication and characterization of high-performance TFTs inside a single grain. His main interests are material investigations of semiconductor devices. During his Ph.D. studies he presented his work in several conferences (IEDM, MRS, SID, ECS). He also chaired sessions in conferences. At present, he is a reviewer for the IEEE/OSA Journal of Display Technology.

Since june 2006, he has been working at Philips Semiconductor as a failure analysis engineer.

# List of Publications

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