60 GHz Beamforming Transmitter Design for Pulse Doppler Radar

By

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Abstract

Beamforming systems operating at millimeter-wave frequencies provide spatial selectivity, array gain and wide bandwidth, which benefit point-to-point Gb/s wireless communication network and high-resolution radar applications. In this thesis, a 60 GHz beamforming transmitter for a pulse Doppler radar is designed, which can be used for indoor presence detection. Our treatment includes system definition, proposing a system architecture, and circuit-level implementation.

The true-time-delay technique is explored to realize the UWB beamforming system. The most difficult part to realize such a system is to implement large delay range with fine delay resolution. Optimizations are performed in system and circuit levels. The group delay variation of a transmission line due to mismatch is investigated and appropriate system architecture is proposed. A trombone delay line structure is exploited to implement the true-time-delay element. In order to keep the characteristics of this delay line constant within the frequency of interest, the corresponding design methodology is developed. Besides, the delay performance between different paths will also be degraded by mismatch. It is preferred to make an amplifier with flat group delay within its operating bandwidth. The relationship between the bandwidth and group delay of an amplifier is studied. A power amplifier is presented with relatively flat group delay and sufficient output power.

The design is implemented in 130 nm SiGeC BiCMOS process. A delay range of 16 ps and delay resolution of 1.1 ps are achieved in our beamformer, which implies the beam can be steered from -75^{o} to 75^{o} with the steering resolution of 9.5^{o}. The differential power amplifier in the transmitter realizes a linear power gain of 32 dB with 11 GHz -3 dB bandwidth. The output power at 1 dB compression point is 12.5 dBm and peak PAE is 20 %.

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Chapter 1

Introduction

Over the past 40 years, we have witnessed the realization of all the wonders made by integrated electronics, predicted by G. Moore in his seminal 1965 paper [1]. Today, there has been no area of modern life untouched by the progress of microelectronics. Silicon technology has also made great progress over the last decade from a digitally oriented technology to one well suited for microwave and RF applications at a high level of integration [2]-[3]. That makes it possible for microwave and radio frequency circuit design to step the way from small-scale building blocks to complete systems-on-a-chip [4]-[5]. New research subjects are always being prompted to meet the aggressive performance specifications required by potential commercial applications, like 60 GHz WPAN-WLAN and 77 GHz radar transceiver [6]-[7]. The purpose of all of these is to create energy-efficient, healthy and eco-friendly living environment for our human beings.

This thesis will present a 60 GHz transmitter design of a pulse Doppler radar, which is used for indoor presence detection. The concept of presence detection is illustrated in Figure 1.1. The basic idea is to detect a person entering the room and make lighting, heating and ventilation in the room occupancy-driven. The proposed transmitter exploits the active beamforming technique to focus and steer an electromagnetic beam in order to increase channel capacity and satisfy the system specifications. The utilizing of beamforming technique can make the presence detection system more powerful since the person in the room can be not only detected but also localized. The design will be fabricated in ST Microelectronics' 130 nm SiGeC BiCMOS process [8].

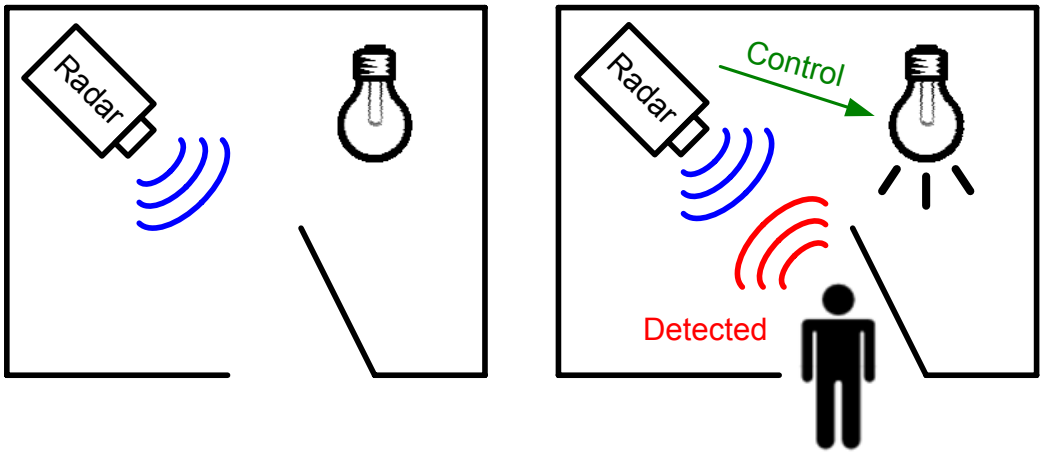

Figure 1.1: Illustration of indoor presence detection (The lighting turns on automatically when the person entering the room is detected).

1.1 Motivation

1.1.1 Radar Technology for Presence Detection

In order to detect that a person is entering the home environment, many technical solutions based on a large variety of physical phenomena are available, such as infrared, ultrasound and ultra wideband (UWB) radar based system. Infrared (IR) [9] is just below the visible spectrum of light in frequency and is radiated strongly by hot bodies. Many objects, such as people, are especially visible in the infrared wavelengths of light compared to objects in the background. However, IR-based system has limitations in detection range and bright environments, which is incapable of providing ubiquitous coverage for detection. The frequency range of ultrasound is outside the audible band and does not interfere with human hearing. It is a suitable technology for presence detection and range finding. This use is also called SONAR (sound navigation and ranging), the operating principle of which is similar to radar [10]. In many applications, however, the power consumption of ultrasound sensors is higher than other solutions, such as UWB radar, and also more costly [11].

Radar, which is an acronym for radio detection and ranging, is a technique that uses electromagnetic waves to identify range and speed of both moving and fixed objects. It is a

non-line-of-sight technology and has a detection range of a few tens of meters in free space, which makes it practical to cover large indoor areas. The UWB technology makes radar promising for use in high-resolution [12]. The development of IC technology makes the radar chipsets available at low cost. Nevertheless, relatively little research has been carried out in the radar-based indoor presence detection system. Thus, to investigate the feasibility of a presence detection radar module implemented in silicon technology is one of the motivations of this thesis.

1.1.2 60 GHz Unlicensed Frequency Band

In 2001, the Federal Communications Commission (FCC) in the US allocated 7 GHz in the 57-64 GHz band for unlicensed use [13]. In Europe, the conference on postal and telecommunication administration (CEPT) also opened up a frequency band of 57- 66 GHz. The bands around 60 GHz are available worldwide, as illustrated in Figure 1.2 [14].

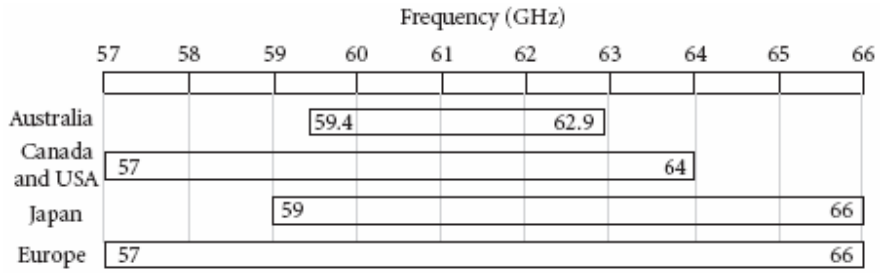

Figure 1.2: Spectra available around 60 GHz.

Fine range resolution is required in future presence detection systems, while better range resolution is enabled by wider bandwidth in the radar system. For a range resolution of 10 cm, a bandwidth of 1.5 GHz is needed [15]. Therefore, the opening of the wide free spectrum around 60 GHz is attractive and more than sufficient for cm-resolution radar system. In addition, the frequency band around 60 GHz are suggested for short range wireless application due to the free space path loss (FSPL). High atmospheric attenuation caused by oxygen resonance at 60 GHz permits dense frequency reuse and low interference between users [16]-[17]. Meanwhile, 60 GHz signals are greatly attenuated by concrete walls while ultra-wideband spectrum (3.1-10.6 GHz) has wall-penetrating property. All of these properties make 60 GHz band suitable for our indoor presence detection radar.

1.1.3 Active Beamforming Technique

Active beamforming [4] takes advantage of spatial directivity and array gain to imitate a directional antenna and increase spectral efficiency. Figure 1.3 features the advantages of a beamforming system. With a conventional individual antenna, the power is radiating in all directions and declining with the square of the distance. Most of the power is wasted in this case. An array of antennas with active beamforming focuses the radiating power. Besides, the beam can also be steered electronically. Beamforming technique will be exploited and integrated into our presence detection radar system, which can increase the detection range, improve the sensitivity and reduce interferes for other users. In addition, it also adds scanning ability to radar in the absence of mechanical movement. Therefore, the utilizing of active beamforming can make the presence detection radar system more powerful in that the person in the room can be localized as well as detected. On the basis of the information about the position of persons in a room, the appropriate lamps or heaters close to the person can be chosen. Integration of beamforming systems in silicon at millimeter wave frequency improves the system performance of potentially low-cost radar and could also be employed in gigabit-per-second wireless communication networks.

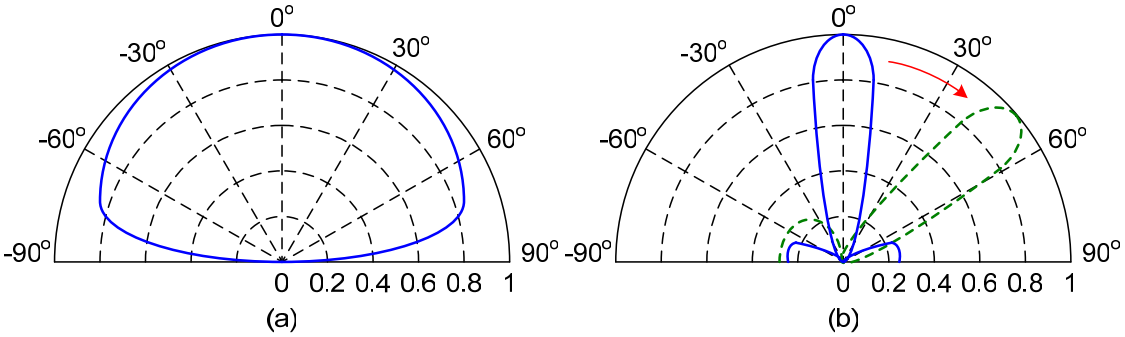

Figure 1.3: Radiation pattern of (a) individual antenna, (b) antenna array with active beamforming.

1.1.4 Advantages of SiGe Technology

The choice of a suitable powerful microelectronic technology is one of the most important issues for developing future transceiver, which is always a trade-off issue between cost and performance. For consumer applications, cost must be taken into account, which is mainly related to the transceiver RF front end. Traditionally, III-V semiconductors (GaAs and InP) provide solutions for millimeter wave application, where performance is traded off for higher cost. In the past few years, SiGe BiCMOS and RF-CMOS play important roles in building millimeter wave transceiver circuit blocks [18]-[20]. In addition, the complexity of beamforming systems is usually higher than that of normal single-path transceiver, which favors silicon technology over compound semiconductors due to its lower cost for a given chip area. Compared with RFCMOS, SiGe BiCMOS technology has advantages in design cycle time and performance versus cost [20]. Reducing current consumption is also one of the most important concerns in beamforming system to ensure the reliability of the chip, which also favors SiGe technology over RF-CMOS. In this work, a 130nm SiGeC BiCMOS process will be used.

1.1.5 Commercial Applications

Besides the technical factors, there is also commercial impetus to develop 60 GHz radar system. Nowadays, home automation concepts capture more and more people's attention [21]. Smart home environments are usually composed of a large number of networked sensors and actuators for decentralized indoor climate control and remote access to different functionalities and comfort functions. Therefore, presence detection and localization of objects or people can be an enabling technology for many smart home applications [11]. In addition, indoor security (intruder detection), image recognition and anti-collision vehicle can also be the potential applications by exploiting the radar based system.

1.2 Design Challenges and Objectives

In order to meet the system specifications and realize the presence detection radar with beamforming technique, all kinds of design challenges need to be overcome. In the system level, how the beamforming is implemented and which modulation scheme is used for the radar have significant impacts on the system architecture and overall performance. Different approaches must be studied and compared before finally making the appropriate decision. In the circuit level, no matter how the beamforming technique is implemented, it is always not easy to realize large beam steering range with fine beam steering resolution. The reason for that includes the high loss of silicon substrate, low-Q passive devices, large interconnects parasitics and high-frequency coupling issues. Besides, at millimeter-wave frequency, the low breakdown voltage and small current handling capability of the active devices will also compromise the implementation of millimeter-wave circuit module on silicon, especially the power amplifier. Achieving high gain at millimeter-wave frequencies implies burning huge current and dissipating enormous power. Therefore, thermal resistance of the chip and package must also be considered to ensure the reliable operation of the chip.

In consideration of the challenges inherent in the design and the motivations for this work, the following objectives have been specified:

First, study the feasibility of beamforming technique integrated in silicon at 60 GHz; choose the appropriate approach and system architecture to implement the technique and design a 60 GHz transmitter with beamforming technique, to form and steer a narrow electromagnetic beam for presence detection radar application, realizing occupancy-driven lighting (or others) control.

Second, develop some design knowledge of millimeter-wave circuit blocks, such as power amplifier, in silicon technologies. To author's knowledge, there is only one or two companies worldwide offering 130 nm SiGe BiCMOS technology with mm-wave capabilities. Since SiGe BiCMOS technology has its advantages in design cycle time and

performance versus cost, it is necessary to build circuits on similar technologies and develop some design knowledge in order to meet the potential consumer markets.

Third, the work of this thesis is part of EU-MEDEA+ project SIAM which aims at the establishment of silicon technology platforms for emerging high frequency and mm-wave consumer applications. Therefore, it is also necessary to investigate the 130 nm SiGeC BiCMOS process and its design kit in millimeter-wave applications. The measurement results could be used to further optimize the process and computer simulation models and therefore ultimately enable mass production.

1.3 Organization

Recent progresses in millimeter-wave transceivers with beamforming techniques are studied in Chapter 2. The principles, architectures and advantages of such systems will be addressed in detail. Afterwards, fundamentals of a radar system will also be explained. Based on these studies, the true-time-delay active beamforming technique and pulse modulation scheme are chosen to be implemented in the beamforming radar system.

A typical application scenario is described in Chapter 3. Based on system level analysis and link budget, the specification of each building block in the system will be defined. Minimizing the group delay variation is one of the most important concerns to realize such a system; appropriate system architecture is then proposed.

Chapter 4 and Chapter 5 describe the design methodology of each building block in the beamforming transmitter. How to minimize the group delay variation using circuit-level techniques will also be discussed in detail. The complete signal path is verified by top-level circuit simulation.

Finally, a summary of highlights and recommendations for the future work are given in chapter 6.

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Chapter 2

Active Beamforming and Radar Systems

In this chapter, active beamforming technique is introduced and the operating principle behind it is explained in detail. In narrowband systems, phase shifting elements are usually required to form the beam while true time delay elements are needed in wideband systems. The pros and cons of different realizations are compared and challenges in implementing the true time delay is discussed. Following an overview of existing beamforming systems on silicon ICs, we study the feasibility of realizing a UBW beamforming radar system in silicon.

2.1 Why Active Beamforming

Beamforming is a signal processing technique used for directional signal transmission or reception [1]. A beamformer works as a spatial filter, receiving or transmitting signals from a specific direction and attenuating signals from other directions. The spatial directivity and array gain properties of such systems can increase the spectral efficiency and channel capacity. This may also be achieved by directional antennas (e.g., parabolic dish). However, because of the passive nature of directional antennas, they can only be used when the relative location and orientation of neither the transmitter nor the receiver change quickly or frequently and are known in advance, which are not suitable to most consumer applications.

Fortunately, the electromagnetic beam can be steered not only mechanically but also electronically. That is where active beamforming got its name. The operating principle of the electronically controlled beamformer is shown in Figure 2.1. With n paths spaced a distance of d apart, the signal transmitted with a certain angle θ by n^{th} path experiences an excess delay τ_n:

$$\tau_n = (n-1)\frac{d\sin\theta}{c} = (n-1)\tau\,, \tag{2.1}$$

where c is the speed of light. The delay in each path is independent of the operating frequency. The signals transmitted by the first and n^{th} paths are given by

$$S_0(t) = A(t)\cos\left[\omega_c t + \varphi(t)\right] \tag{2.2}$$

and

$$S_n(t) = S_0(t-\tau_n) = A(t-\tau_n)\cos\left[\omega_c(t-\tau_n) + \varphi(t-\tau_n)\right], \tag{2.3}$$

where $A(t)$ and $\varphi(t)$ are the amplitude and phase of the signal and ω_c is the carrier frequency. Adjustable time-delay elements τ_k' is introduced to compensate the signal delay and phase difference simultaneously. The combined signal is expressed as

$$S_{sum}(t) = \sum_{k=0}^{n-1} S_k\left(t-\tau_k'\right) = \sum_{k=0}^{n-1} A\left(t-\tau_k-\tau_k'\right)\cos\left[\omega_c\left(t-\tau_k-\tau_k'\right) + \varphi\left(t-\tau_k-\tau_k'\right)\right]. \tag{2.4}$$

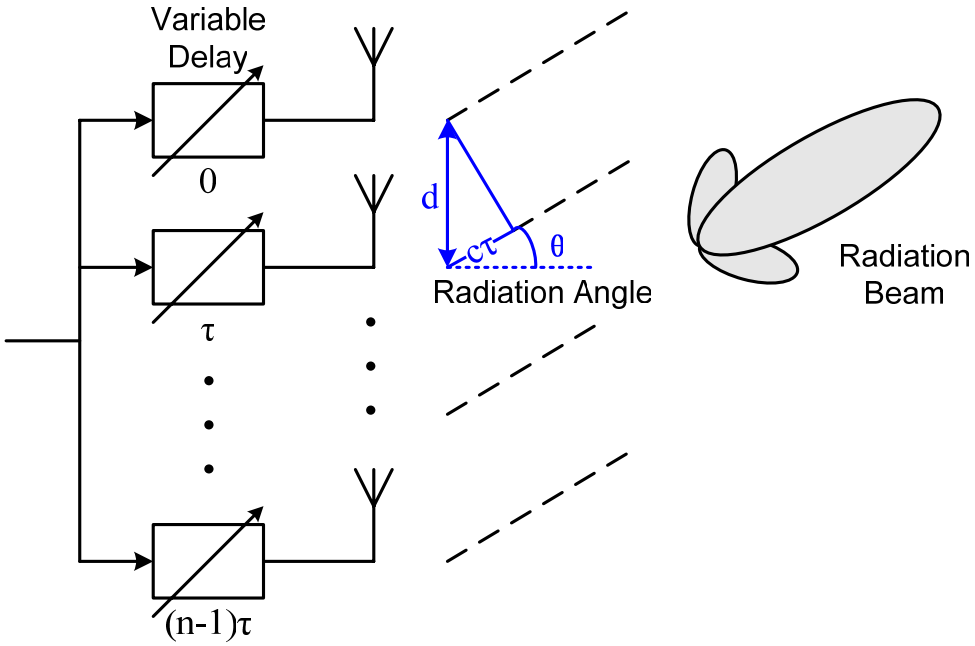

Figure 2.1: n-path beamforming system.

If $\tau_k' = \tau_k$, signals from a particular direction can be added coherently while signals from other directions are added destructively. The total output signal strength in the desired direction can be expressed by

$$S_{sum}(t) = nA(t)\cos\left[\omega_c t + \varphi(t)\right]. \tag{2.5}$$

Depending on the delay settings, the electromagnetic beam can also be steered electronically, so the array system can emulate a directional antenna's properties, such as improved gain and directivity, without mechanical reorientation of the actual antennas. It should also be noted that the complete radiation pattern of the array is determined not only by the array factor but also the field pattern of the individual antennas in each path.

2.1.1 Beamforming Transmitter

Beamformer at transmitter side mainly provides two advantages over the isotropic transmitter, featured in Figure 2.2. Firstly, the receiver can obtain much more power for the same total transmitting power. The improvement comes from the coherent addition of the electromagnetic fields in the desired direction and attenuation in other directions. In other words, the radiated power is focused. For a transmitter which generates P watts and has an effective antenna gain G, the effective isotropic radiated power (*EIRP*) transmitted by the array is increased by a factor of n^2, which is given by

$$EIRP = n^2 PG\,. \tag{2.6}$$

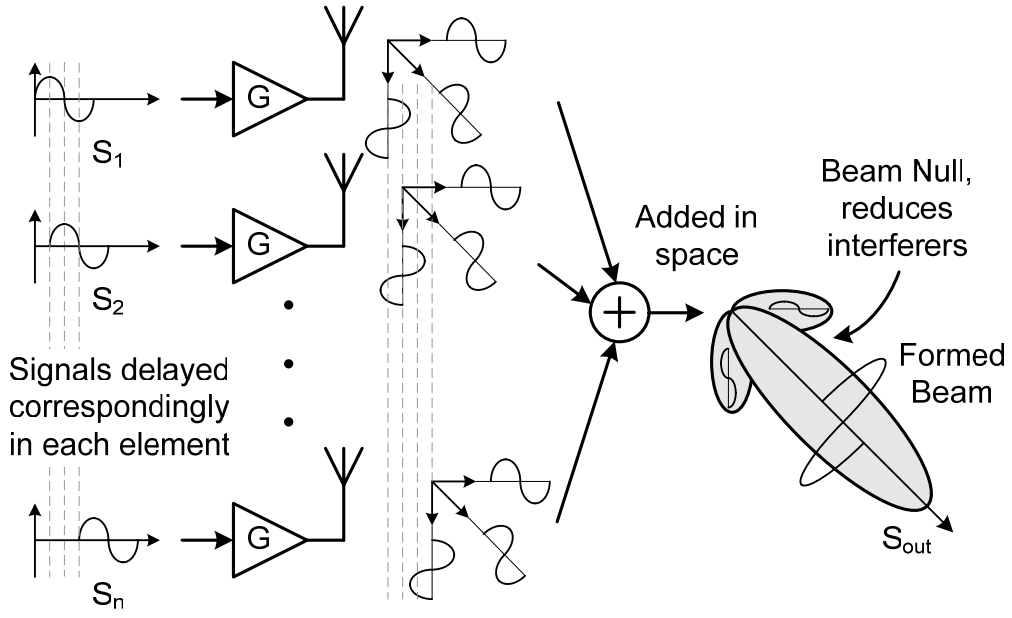

Figure 2.2: Beamformer at transmitter side reduces interferers and focuses radiated power.

The development in silicon technologies is occurring simultaneously in 130 nm SiGe BiCMOS [2] with f_T/f_{MAX} greater than 230/300 GHz and 65 nm RF-CMOS [3] with f_T/f_{MAX} up to 180/270 GHz. However, additional constraints, such as low breakdown voltage and current handling capabilities affect the over-all system performance, which compromise the implementation of millimeter-wave systems on silicon. System-lever power combining offered by active beamforming relaxes the performance requirements on individual active devices. Therefore, beamforming technique can be one of the promising solutions to implementing single-chip millimeter-wave transceivers on low-cost silicon technology.

Secondly, the interferers emitted by the transmitter are greatly reduced. Commonly used omni-directional communication systems radiate electromagnetic power in all directions. Besides the power wasted by an isotropic antenna, it also adds interference to other users. Currently, wireless communication networks have become more interference-limited than noise-limited [4], so increasing omni-directional transmit power might produce no net benefit to system capacity. A beamforming transmitter generates less interference at receivers that are not targeted. Therefore, the spectral efficiency can be improved by exploiting the spatial directivity of the beamformer.

Since receiver is not the subject of this thesis, the benefits from beamforming at receiver side are described briefly. The directivity and array gain lead to improved immunity to interferers and higher SNR at the receiver side. The former is due to the fact that the desired and interfering signals usually originate from different spatial locations and the spatial separation can be exploited to separate signals from interferes using a spatial filter, such as an active beamformer. The latter is because noise sources are usually uncorrelated while the delayed signals in each path are correlated. Thus, the output signal power is n^2 times improved while the output total noise power is around n times increased. In other words, an n-path receiver improves the sensitivity by $10\log(n)$ in decibels compared to a single-path receiver [5].

2.1.2 Array Parameters

The complete radiation pattern of a beamformer is determined by not only the field pattern of a single antenna, but also several array parameters, such as antenna spacing between different paths, number of paths and incident angle of the radiation beams. For isotropic antennas, consider a linear array made up of N paths equally spaced a distance d apart. As shown in Figure 2.1, the phase difference between adjacent paths equals

$$\phi = 2\pi\left(d/\lambda\right)\sin\theta, \tag{2.7}$$

where λ is the wavelength of the signal. For convenience, the amplitude of the signal at each path equals unity. The sum of all the voltages from individual paths can be written as

$$E_a = \sin\omega t + \sin\left(\omega t + \phi\right) + ... + \sin\left[\omega t + \left(N-1\right)\phi\right]$$

$$= \frac{\sin\left(N\phi/2\right)}{\sin\left(\phi/2\right)}\sin\left[\omega t + \left(N-1\right)\phi\right]. \tag{2.8}$$

The equation represents a sinewave of frequency ω with an amplitude of the form (sinNX)/(sin$X$). The magnitude of equation (2.8) is the field pattern of the array:

$$\left|E_a\left(\theta\right)\right| = \left|\frac{\sin\left[N\pi\left(d/\lambda\right)\sin\theta\right]}{\sin\left[\pi\left(d/\lambda\right)\sin\theta\right]}\right|. \tag{2.9}$$

The field-intensity pattern has zeros when the numerator is zero and the denominator is not zero, giving nulls in the pattern. The denominator and numerator are both zero whenever $\pi(d/\lambda)\sin\theta = 0, \pm\pi, \pm 2\pi, \ldots, \pm n\pi$. By applying l'Hopital's rule, it is found that $|Ea(\theta)|$ reaches its maximum and equals to N when $\sin\theta = n\lambda/d$. The maximum at $\theta = 0$ defines the main beam of the field-intensity pattern. The other maxima are called grating lobes and they are generally undesirable in that they can cause ambiguities with the main beam. The normalized radiation pattern of a linear array of isotropic elements (in which the phase shifter has been applied) is:

$$G\left(\theta\right) = \frac{\sin^2\left[N\pi\left(d/\lambda\right)\left(\sin\theta - \sin\theta_o\right)\right]}{N^2\sin^2\left[\pi\left(d/\lambda\right)\left(\sin\theta - \sin\theta_o\right)\right]}, \tag{2.10}$$

where θ_o is the incident angle. The maximum of this pattern occurs when $\sin\theta = \sin\theta_o$. According to equation (2.10), the radiation pattern of the array can be plotted and many array properties can be studied.

A. Antenna spacing

A larger spacing between antennas is generally preferred since it ensures less coupling between different antenna elements and also makes physical realization of the antennas easier. However, as can be seen from Figure 2.3, when the distance between adjacent antennas is larger than one half wavelengths, grating lobes appear in the radiation pattern. Therefore, $d=\lambda/2$ is a good choice for antenna separation. Practically, the radiation pattern of a single antenna is not isotropic, so the antenna spacing can be larger than half wavelength, especially in the wideband case. It will be shown in the following sections that the antenna spacing can be another design parameter which does not have to be fixed at one-half wavelength in the wideband beamformer.

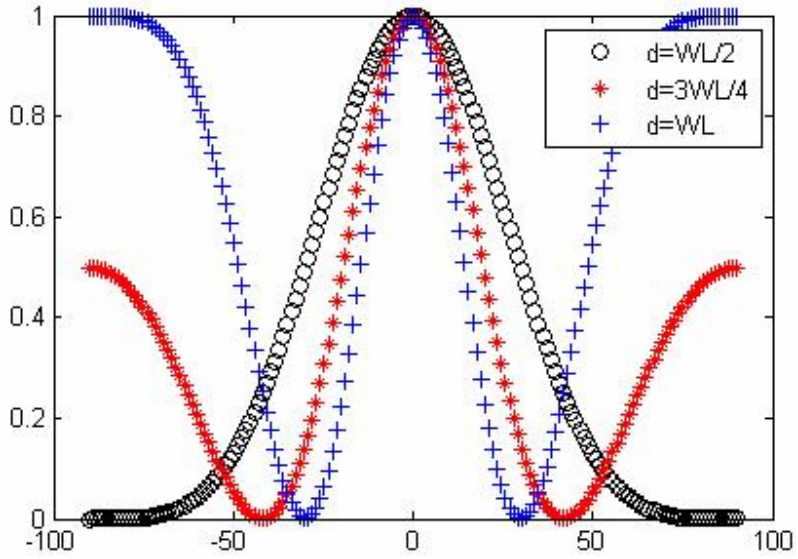

Figure 2.3: Two-element array pattern for different antenna spacing.

B. 3dB beamwidth

The 3dB beamwidth in the incidence plane can be derived from equation (2.10), depending on the length of the array (number of paths n times antenna spacing d) and the incident angle θ. If the incident angle is small, the 3dB beamwidth can be expressed by [6]

$$\theta_{3dB} = \frac{0.866\lambda}{nd\cos\theta}. \tag{2.11}$$

For a fixed antenna spacing of one-half wavelength, the beamwidths are approximately 24.8^o, 33.1^o and 46.8^o corresponding to the number of paths of 4, 3, 3 and incident angles of 0^o, 0^o, 45^o. The array length also determines the maximum required delay, so there is a tradeoff between the maximum achievable delay and the beam width of the radiation pattern.

C. Beam steering resolution

The beam steering resolution depends on the delay resolution, incident angle and antenna spacing. The relationship can be expressed as

$$\tau_{d\_res} = \left(\frac{d}{c}\right)\left(\sin\theta_{steer} - \sin\theta_{incident}\right), \tag{2.12}$$

where τ_{d_res} is the delay resolution, d is the antenna spacing, c is the speed of light, $\theta_{incident}$ is the incident angle and the difference between θ_{steer} and $\theta_{incident}$ can be regarded as the steering resolution. The beam steering resolution changes with the incident angle. For 1ps delay resolution, the steering resolution is 6.9^o if the incident angle is 0^o while it becomes 20.4^o if the incident angle is 60^o.

2.2 Approaches to Realize Active Beamforming

A beamformer is composed of several paths and signals in each path experience different delays in space. In order to form the desired radiation beam, a delay element must be implemented in each path to compensate for the spatial delay. For narrow-band signal, the delay element can be replaced by a phase shifter, which is easier to implement. However, true-time delay element is generally required by high-resolution radar system and integration of adjustable time delays in signal paths is more challenging.

2.2.1 Narrowband Approximation: Phase Shifter

In a beamformer, the signal transmitted/received with a certain angle θ by n^{th} path experiences an excess delay, τ_n. The signal function of the n^{th} path is given by equation (2.3) which is copied as below:

$$S_n(t) = A(t-\tau_n)\cos\left[\omega_c(t-\tau_n)+\varphi(t-\tau_n)\right]. \quad (2.13)$$

A uniform delay across frequency implies linear phase shifting over the whole frequency range, as shown in Figure 2.4. In a narrowband system, assuming the excess delay τ_n is much smaller than the time period of the highest modulation frequency, we have

$$A(t) \approx A(t-\tau_n), \varphi(t) \approx \varphi(t-\tau_n). \quad (2.14)$$

Thus, the uniform delay (linear phase shift) can be approximated with a constant phase shift:

$$\phi_n = \omega_c \tau_n. \quad (2.15)$$

Figure 2.5 graphically shows how the phase shifter can be implemented in the system and the mechanism by which the dispersion of signals is generated due to the narrowband approximation. Time delay in the RF path provides wideband beamforming (Figure 2.5 (a)) which can be replaced by a delay in the IF path and a phase shift in the LO path (Figure 2.5 (b)). Because of the narrowband approximation, the delay in the IF path can be eliminated and thus only phase shift in the LO path is needed, as shown in Figure 2.5 (c). The phase shift can also be implemented in the RF or IF paths. The choice of where to implement the phase shift is of importance to the final performance of the phased-array system. LO path phase shifting is usually preferred since the gain in each path of the transmitter or receiver is less sensitive to the amplitude variations at the LO ports of the mixers [7].

Error vector magnitude (EVM) is introduced due to the elimination of the delay in the signal path (Figure 2.5 (b-c)). The magnitude of the error is a function of the incidence angle of the beams, phase quantization error and the ratio between signal bandwidth and carrier frequency [8].

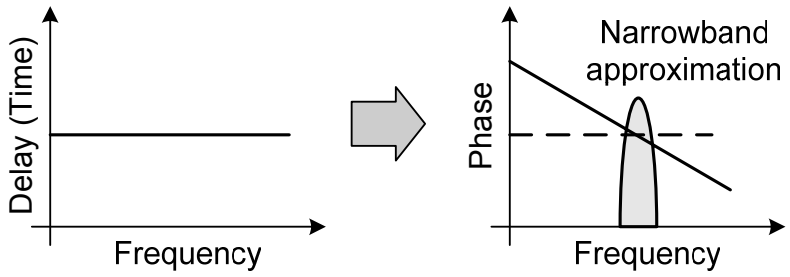

Figure 2.4: In narrowband, a certain delay corresponds to a constant phase shift.

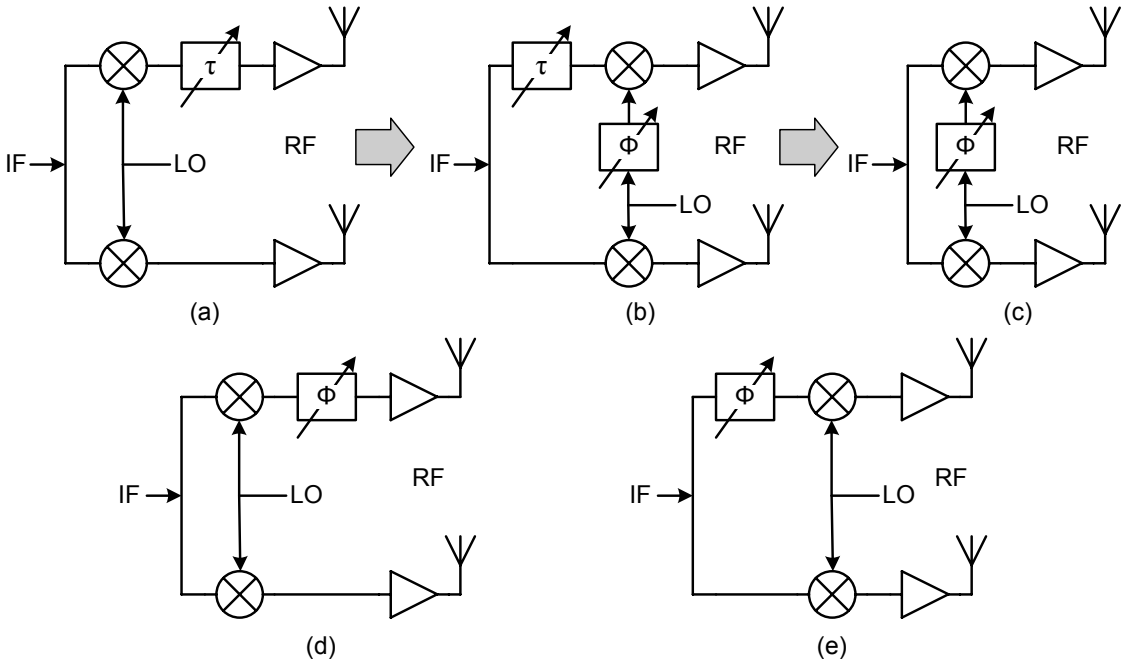

Figure 2.5: Narrowband approximation and the source of dispersion in phased array systems.

2.2.2 UWB Beamformer: True Time Delay

Since wider bandwidth results in better ranging resolution, UWB systems are more attractive in radar [9]. Although phase shifting is sufficient for many narrowband applications, it fails in UWB multi-antenna systems where true time delay is required. UWB impulse based radar systems utilize ultra short pulses in the time domain, corresponding to ultra-wide bandwidth in the frequency domain, to achieve fine range resolution. The analysis of UWB beamformer is much more complicated compared with narrowband single frequency beamformer. In this section, some features of UWB beamformer and its difference from narrowband phased-array system are explained in a qualitative way, with the help of Figure 2.6. Afterwards, possible solutions to true time delay realizations are discussed.

The signal waveform in narrowband phased array is a continuous sinewave, while it is discrete pulses in the UWB case. Due to the different signal waveforms, in the narrowband

phased array, the summation of sinusoidal signals with different phase shifts is still a sinusoid with the amplitude given by equation (2.10). However, the summation of discrete pulses does not necessarily result in another pulse with similar shape, as shown in Figure 2.6 (parts b, d and f). Since the frequency components are plentiful in UWB signals and the pulse width is usually much shorter than the pulse repetition time, the combined output waveform is rather arbitrary. Consequently, UWB arrays are usually lacking of distinct grating that commonly appears in the radiation pattern of narrowband phased array systems. Therefore, the antenna spacing can be another design parameter which is more or less fixed in narrowband phase array. From the output waveforms in Figure 2.6 (a-d), it can be speculated that there is no nulls in UWB case with a Gaussian signal as the signal waveform and also more energy is wasted in other directions. But if applying the second-derivative Gaussian signal, a more satisfactory radiation beam is formed because the negative portion of the time domain pulse cancels the positive portion. At a particular angle, nulls can also be observed when the second-derivative Gaussian signal is applied.

The beamwidth of a UWB array is now considered. In narrowband phased array, the beamwidth is inversely proportional to the array length L (number of elements times antenna spacing) and proportional to the signal period. In the UWB case, instead of the signal period, the pulse width ΔT (inversely proportional to the RF bandwidth BW) is one of the factors to determine the array field pattern, which can also be speculated form Figure 2.6 (c-f). The beamwidth of a UWB array is given by

$$\theta_{3dB} \alpha \frac{\Delta T c}{L} \alpha \frac{c}{L \cdot BW} \tag{2.16}$$

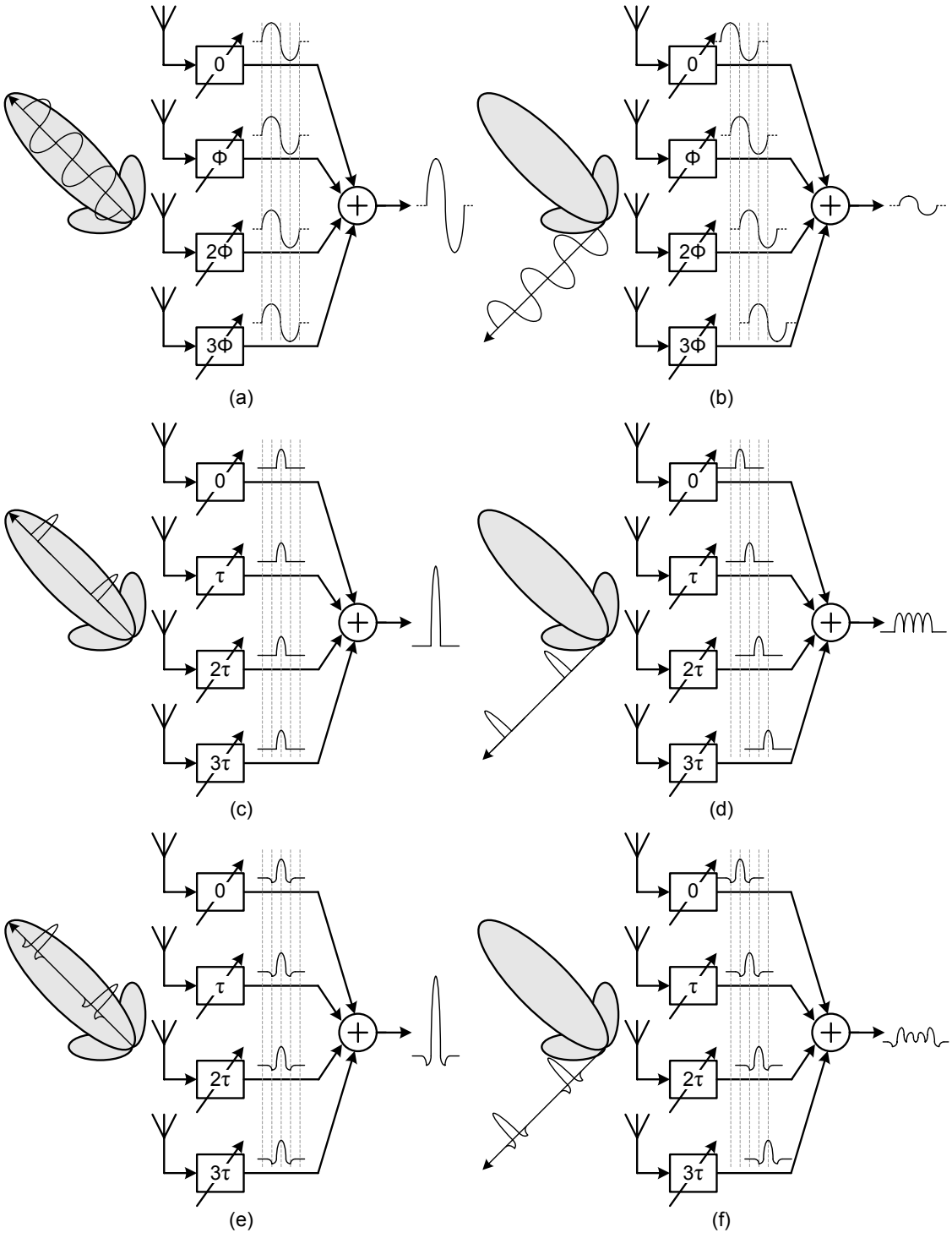

Figure 2.6: Combined output waveform for two different incident angle with the input waveform of (a-b) narrowband single frequency signal, (c-d) wideband Gaussian signal, (e-f) wideband second-derivative Gaussian signal.

The main challenge in realizing UWB beamformer at millimeter-wave frequencies is to implement a programmable true time delay element with fine delay resolution and large delay range. The delay of electromagnetic signals in a certain media is the traveled distance divided by wave velocity. Therefore, programmable time delay can be controlled by manipulating the property of the media, the velocity of the signal or the path length, as shown in Figure 2.7.

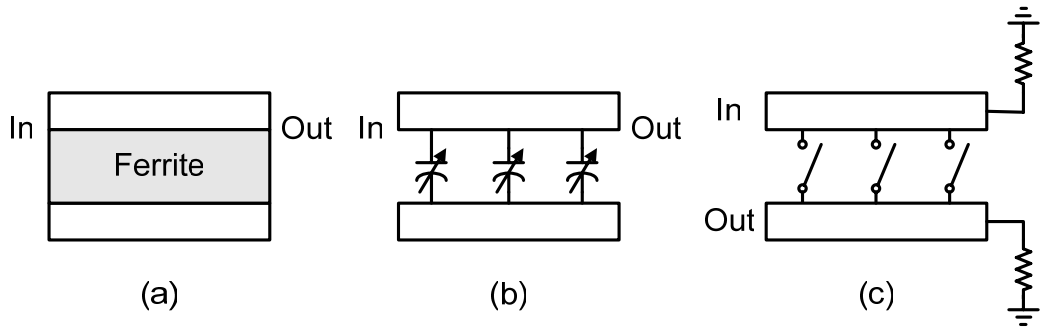

Figure 2.7: True time delay realizations by manipulating (a) property of the media, (b) velocity of the signal or (c) path length.

In Figure 2.7 (a), a ferrite is used which is a ceramic-like metal-oxide insulator material that possesses magnetic properties while maintaining good dielectric properties. The interaction of electromagnetic waves with the spinning electrons of the ferrite material can produce a change in the permeability of the ferrite, and thus a change in velocity [6]. However, it is not practical to implement ferrites on silicon ICs so this implementation won't be discussed further.

Figure 2.7 (b) proposes another solution to realize the true time delay which could be implemented on silicon ICs. Varactors are placed periodically along the length of a transmission line, enabling the effective shunt capacitance C_{eff} per unit length to be controlled. In this way, the signal velocity on chip and the delay per unit length can be manipulated according to equations (2.17) and (2.18). However, the characteristic impedance of the transmission line varies at the same time, according to equation (2.19). Therefore, the termination of these transmission lines should also be able to vary in order to avoid reflections which would distort the signal. In addition, the maximum achievable

delay will be limited by the tuning range of the varactors and the quality factor of the varactors which is quite low in millimeter-wave frequency range.

$$v_p = 1/\sqrt{L_{eff}C_{eff}} \tag{2.17}$$

$$t_d = \sqrt{L_{eff}C_{eff}} \tag{2.18}$$

$$Z_o = \sqrt{L_{eff}/C_{eff}} \tag{2.19}$$

The third solution is more promising to implement on silicon ICs, as shown in Figure 2.7 (c). The delay is varied by manipulating the length of the transmission line using some switches. The characteristic line impedance can remain constant if the switches have ideal properties (i.e., infinite high input and output resistance in both ON and OFF states). In this case, the delay resolution is limited by the parasitic capacitance of interconnects and switches while the maximum achievable delay is restricted by the attenuation of the line and the requirements of group delay variation.

A UWB beamformer can offer desired performance which is required by high-resolution radar system, but it should be emphasized that implementing programmable true time delay is more challenging compared with realizing variable phase shifting. The area consumed by the transmission lines and their loss are fairly large for integrated implementations on silicon ICs. Besides, it is not easy to control the delay resolution accurately due to the parasitics and reflections in the signal paths. Thus, parasitic extraction and EM simulation are usually required during the design, which increases the design cycle time.

2.3 Active Beamforming Systems on Silicon ICs

Active beamforming systems provide benefits at the system and circuit level. Such systems can be used for high-speed directional communications as well as for ranging and sensing applications, e.g., radar. Integration of a complete beamformer on silicon ICs results in low cost and high reliability. Numerous demonstrations of single-chip UWB beamformer and narrowband phased array system are reported in recent years [10]-[16].

The first fully integrated phased array receiver on silicon is demonstrated by H. Hashemi in 2004 [10]. Figure 2.8 shows the system diagram of the 24 GHz, 8-path phased array receiver. The receiver uses two-step down conversions with an IF of 4.8 GHz. A 19.2 GHz VCO is designed as a ring of eight differential amplifiers with tuned loads to generate 16 discrete phases. The phased array realizes phase shifting with 22.5° resolution at LO port of the first down-conversion mixer. A set of 8 phase-selectors apply the proper phase of the LO to the corresponding RF mixer for each path independently. The receiver is implemented in IBM 7HP SiGe BiCMOS technology with a bipolar f_T of 120 GHz. The die area is 3.5 mm × 3.3 mm.

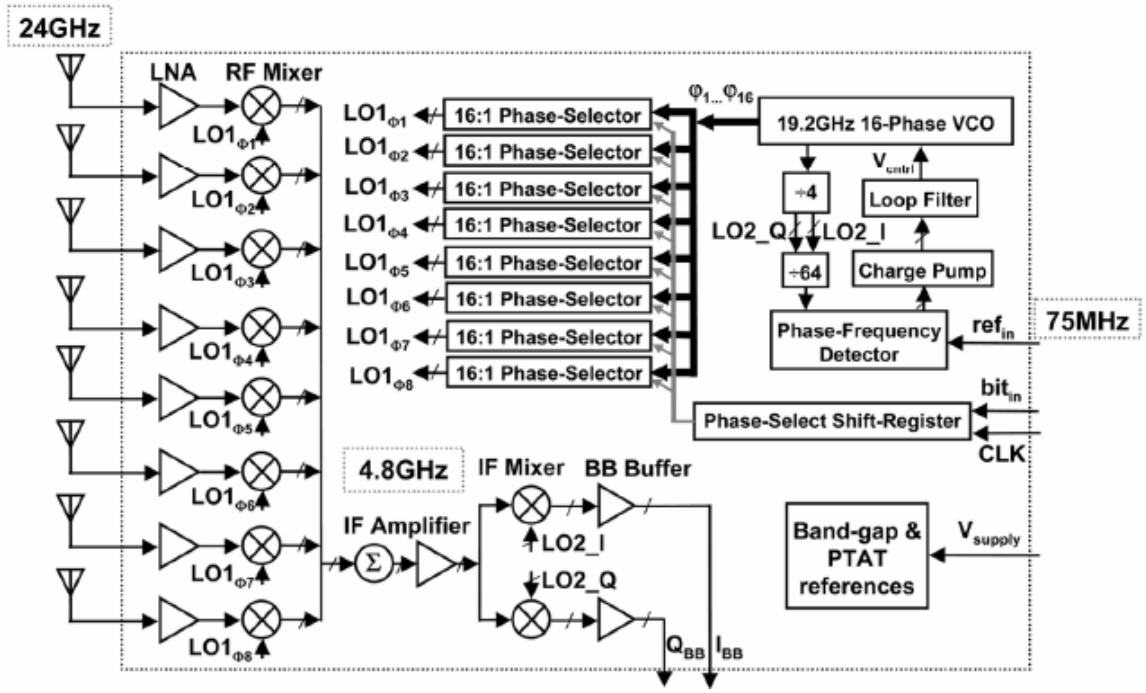

Figure 2.8: First fully integrated 24 GHz eight-path phased array receiver [10].

The main limitation of the above approach stems from the necessity to distribute all the LO phases to each element. This centralized scheme is not suitable for a system operating at millimeter-wave frequencies since the distribution of a large number of LO phases requires a huge transmission-line network with matched LO buffers. Reference [12] proposes a local LO-path phase shifting architecture, as shown in Figure 2.9. The phase rotator in each element generates the LO quadrature phase locally and then interpolates between the in-

phase and quadrature-phase LO signals to produce the desired phase shift in each path. The local phase shifting architecture scales well with an increase in the number of elements and the beam steering resolution is only limited by DAC resolution in practice. The 77 GHz 4-path transmitter is fabricated in 0.12 µm SiGe BiCMOS technology. The die area is 17 mm^2.

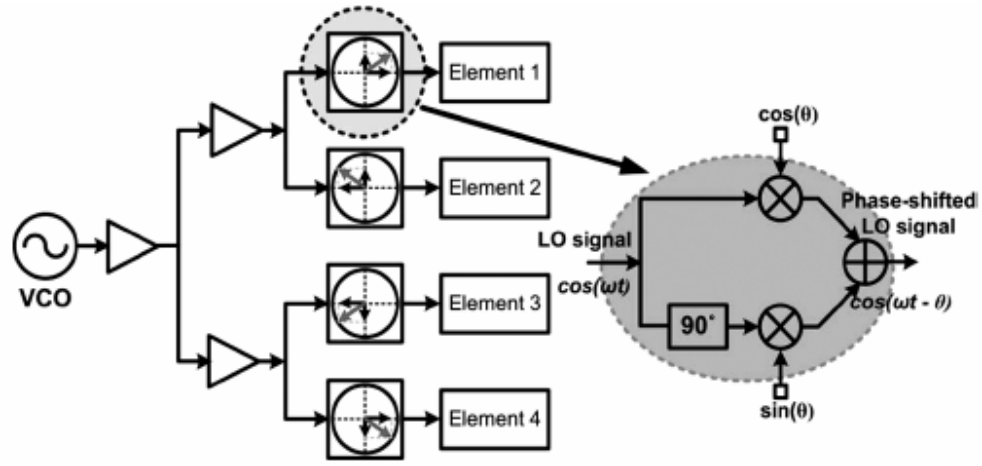

Figure 2.9: 77 GHz local LO-path phase-shifting phased array transmitter [12].

UWB communication and imaging systems have gained significant interest in a variety of commercial and military applications. A fully integrated 4-path 1-15 GHz UWB beamformer in 0.13 µm CMOS is presented in [15]. In order to save the chip area, a path-sharing concept was utilized. As shown in Figure 2.10 (a), the time-delay differences between adjacent paths are constant for any given incident angle. Thus, the delay paths can be configured in cascade so that the signals are combined locally after each delay path. The programmable-delay paths are incorporated as a tapped-delay trombone line matrix, as shown in Figure 2.10 (b). The trombone line is implemented as a quasi-distributed differential configuration where 188 on-chip spiral inductors are used. A number of path-select amplifiers were used to manipulate path lengths in the tapped-delay trombone line. The true time delay resolution is 15 ps while the group delay variation is approximately 5 ps. The maximum beam steering spatial angle is 45^o. The die area is 3.2 mm × 3.1 mm.

The quasi-distributed path-sharing UWB beamformer (Figure 2.10) gives a nice example to realize true-time delay, but the path-sharing concept fails for the UWB system at 60 GHz.

Firstly, in order to get the same beam steering resolution, the delay resolution of the UWB system at 60 GHz must be improved by a factor of six, compared with the one at 10 GHz. Although the spiral inductor can be replaced by the real transmission line, the two path-select amplifiers at each node limit the delay resolution. Secondly, the delay of the above example is dominated by the spiral inductor and parasitic capacitance, while the delay of all the interconnections affects more at 60 GHz since better delay resolution is required. That limits the path-sharing concept being used. Thirdly, reflections introduce large group delay variations at millimeter-wave frequencies. Therefore, it is important to ensure matched condition throughout all the signal paths. The complexity of the path-sharing architecture makes the design job more challenging.

In addition, some common problems exist in most reported beamforming systems on silicon ICs. For one thing, most of the chips consume too much area due to the complicated architecture. For another, they usually just realize the beamforming concept and do not have a specific application. More issues need to be considered and solved when implementing a complete system for a particular application, such as a 60 GHz UWB radar. In this thesis, a simple architecture is exploited to realize UWB beamformer with 16 ps delay range and 1.1 ps delay resolution, which is tailored for UWB radar applications.

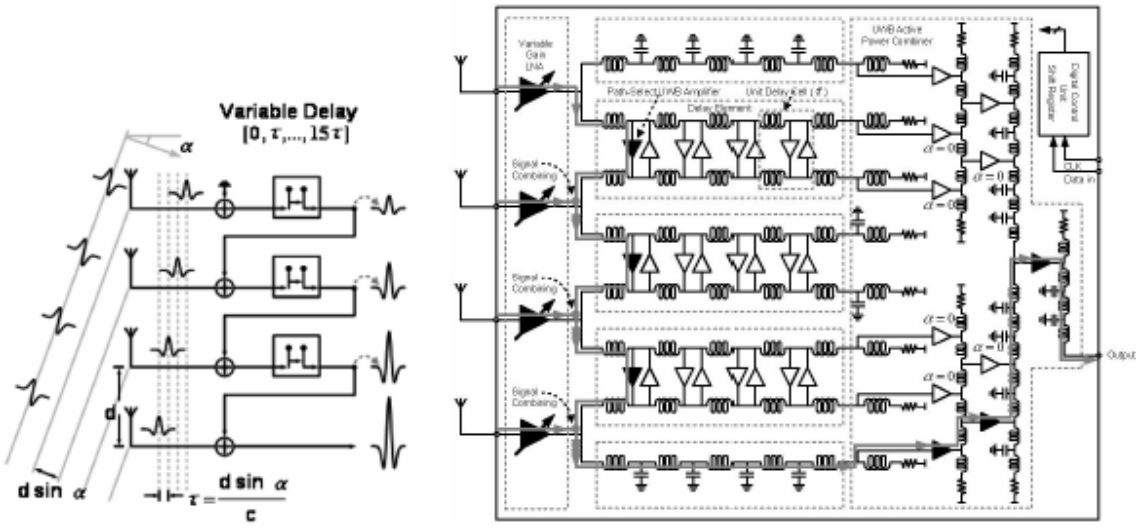

Figure 2.10: 1-15 GHz UWB beamformer, (a) path-sharing concept; (b) path-sharing 4-path UWB beamforming receiver [15].

2.4 Beamforming Radar System

Radar, which stands for radio detection and ranging, is a technique that uses electromagnetic waves to identify range, altitude, direction and speed of both moving and fixed objects, such as aircraft, weather formation and terrain. Traditionally, the radar system is physically large and quite expensive to implement, which limits its application to military, aviation and geography field. Thanks to the development of IC technologies, the radar system can now be integrated and operate in the millimeter-wave range where small physical-size antennas and wide bandwidths can be used. While omni-directional radar systems have great utility, beamforming techniques can be used to add selectivity and scanning to radar in the absence of mechanical movement. Potential applications for a low-cost beamforming radar are automotive car radar [17] and home automation systems [18].

2.4.1 Radar Basics

The operation of radar is illustrated in Figure 2.11. If a transmitter radiates power P_t in all directions through an antenna of gain G_t, the *EIRP* equals

$$EIRP = P_t G_t . \tag{2.20}$$

At a distance d from the antenna, the power density incident on the target is

$$S_t = \frac{EIRP}{4\pi d^2} \tag{2.21}$$

The incident power will be reflected in various directions. The ratio of power reflected back to receive antenna to total incident power is defined as RCS (radar cross section) σ. Therefore, the power density scattered back at the receive antenna equals

$$S_r = \frac{S_t \sigma}{4\pi d^2} . \tag{2.22}$$

The final received power is determined by the effective area of the receive antenna, A_e ($=\lambda^2 G_r/4\pi$). Thus the received power is given by

$$P_r = \frac{P_t G_t G_r \lambda^2 \sigma}{(4\pi)^3 d^4} . \tag{2.23}$$

This is called the *radar equation* which indicates that the received power varies as $1/d^4$. Assuming the minimum detectable power at the receiver is P_{min}, the maximum detectable range can be expressed as

$$d_{max} = \left(\frac{P_t G_t G_r \lambda^2 \sigma}{(4\pi)^3 P_{min}} \right)^{1/4} . \tag{2.24}$$

It should be noted that the above equation over-estimates the maximum range because it does not include many non-ideal effects, such as clutter, target fluctuations and multipath effects [6].

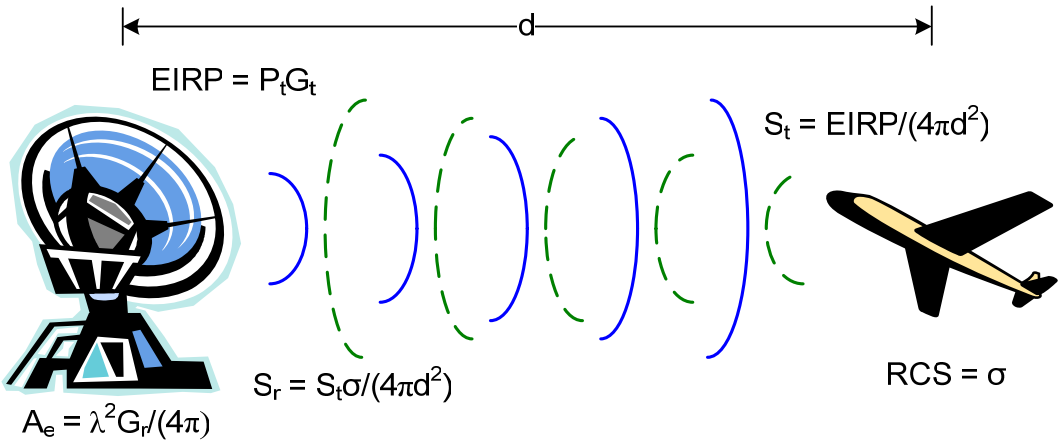

Figure 2.11: Operation of Radar System.

The maximum detectable range and the range between the radar and target are different concepts. In order to get the range information of the target, some kind of modulation schemes must be applied. If FM-CW radar is used, the range information can be obtained by measuring the frequency difference between the transmitted and received signals while time delay between the transmitted and reflected signals gives the range to the target if pulse Doppler radar is used.

In addition, if the target has a velocity component, the returned signal will be shifted in frequency relative to the transmitted frequency, due to the Doppler effect. If the transmitted frequency is f_o and the target velocity is v, the Doppler frequency is

$$f_d = \pm \frac{2vf_o}{c}. \tag{2.25}$$

The plus sign in equation (2.25) corresponds to an approaching target while the minus sign indicates a receding target. The Doppler frequency can be exploited in radar systems to determine the speed of targets.

A simple complete radar system is shown in Figure 2.12. The received echoes will be sent to a DSP module and the signal processing unit could analyze the returned wave to derive the information of targets, such as speed and distance. Usually, an object list comprising of Doppler (velocity), range and amplitude, will be contained in the system assisting the processing process. The external interface will also be included in some systems to interface with other functions, such as engine management, braking system and lighting control.

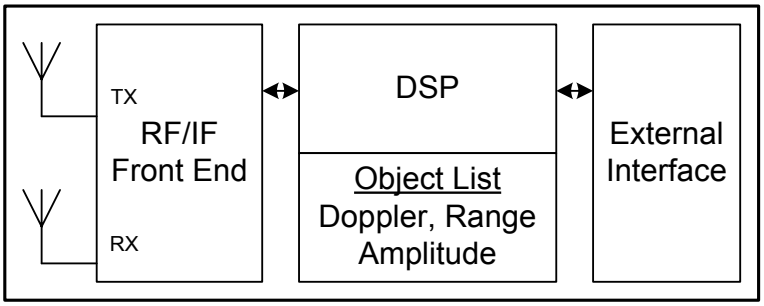

Figure 2.12: Simple schematic of a radar system.

2.4.2 Pulse Doppler Radar for Beamforming

The simple CW Doppler radar [18] cannot detect range information which is usually required in vehicular or smart-home applications. As mentioned before, in order to get the range information, some kind of modulation schemes must be applied. As shown in Figure 2.13, three radar modulation options are: classical frequency-modulated continuous-wave (FM-CW) radar, pseudorandom-noise (PN) coded continuous-wave radar and pulse Doppler radar. In a beamformer, several signal paths work in parallel. Although the beamforming technique offers some advantages to radar, the system is more complicated and the isolation between transmitter and receiver becomes more important. Therefore, a

simple system level architecture and better isolation between transmitter and receiver are main considerations when selecting the modulation scheme.

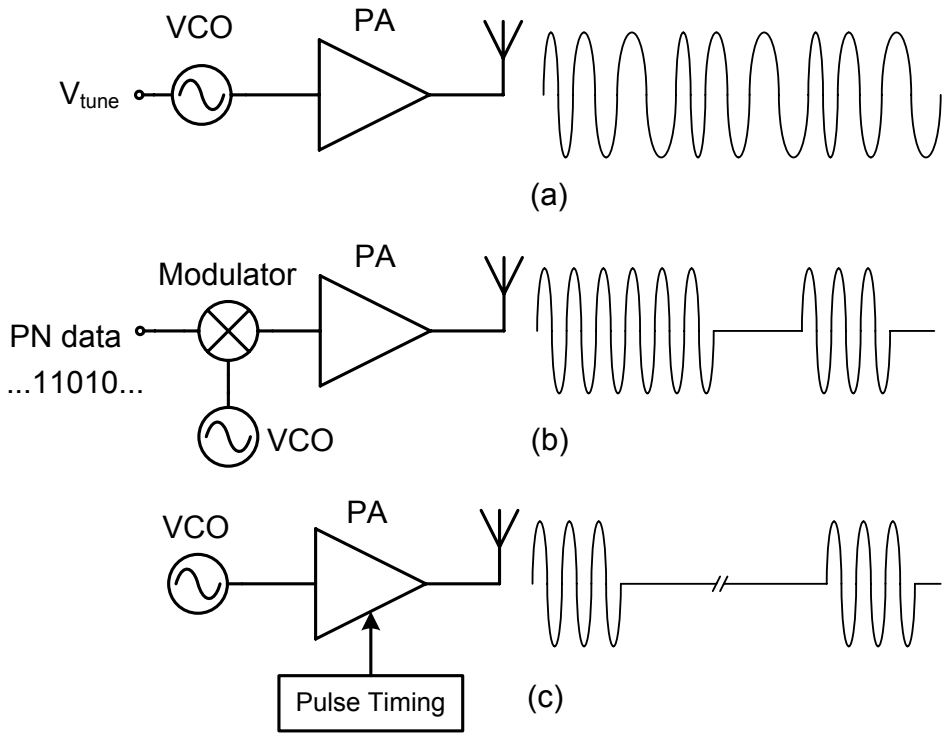

Figure 2.13: Modulation schemes (for simplicity, only transmitting parts are shown): (a) FM-CW, (b) pseudorandom noise coded and (c) pulsed mode.

FM-CW radar is a radar system where the frequency of the transmitted signal varies linearly and the reflected echo mixes with this transmitted signal to produce a beat signal. The resolution is related to how fast and over how wide a bandwidth it is possible to generate a well-defined chirp [19]. And the frequency sweeping linearity is an important parameter to target range detection [20]. All of these put stringent specification on the on-chip voltage controlled oscillator (VCO) design where wide tuning range and high tuning linearity are required. PN-coded radar, as a spread-spectrum system, has the flexibility in choosing the code. The ability to assign different codes to different systems makes it suitable for multi-radar unit system. The resolution is limited by the bit rate of the random codes while gigabit-per-second random codes are not difficult to generate in modern IC technology [21]. The principle disadvantage of above two modulation schemes is the isolation between the transmitter and receiver when one antenna is employed for both

transmitting and receiving, such as the beamforming radar. A substrate-integrated-waveguide circulator can be used to separate the transmitter and receiver [22], but it is not preferable to the integration of the whole system. The isolation between the two ports of a millimeter wave circulator is usually less 35 dB. Therefore, the leakage power from the circulator may still be larger than the reflected power. One of the possible solutions is to use digital signal processing to cancel the leakage power [23].

Pulse Doppler radar requires timing circuitry to modulate the output waveform. Due to its time-gated nature, it offers much better isolation between the transmitter and receiver with single antenna. In addition, pulse radar is also perhaps one of the simplest architectures to implement, thus potentially making it the most cost effective [19]. Both of these two properties make beamforming technique easier to integrate in a pulse radar system. The bottleneck to implement pulse Doppler radar is that it requires much higher peak output power for the same detection range as the above two methods. If the pulse repetition rate is 1%, 20 dB more peak power needs to be generated in order to get the same average transmitting power. It is not easy to deliver much power on silicon ICs at millimeter range due to the power handling capacity of a single transistor. Integration of the system in SiGe BiCMOS rather than RF-CMOS technology tempers the problem. Appealingly, the problem can also be alleviated by using the beamforming technique.

Before ending this chapter, two important parameters of pulse Doppler radar are introduced: pulse width τ and pulse repetition frequency PRF, which to some extent determine the performance of the radar system. Shown in Figure 2.14, the pulse Doppler radar transmits short pulses (pulse width τ) with relatively long intervals. The time delay between the transmitted and reflected signal T_R gives the range to the target. The maximum unambiguous range of the radar occurs when $T_R = 1/PRF$ and can be calculated as follows:

$$Range(unambiguous) = \frac{c}{2 \times PRF}. \tag{2.26}$$

For longer ranges, the echo returns after the transmission of the next pulse, which results in ambiguity of range. The range resolution is the ability of the radar to distinguish between

two targets with similar range. The range resolution is determined by the pulse width τ which is the smallest time interval that the radar can resolve, which is given by

$$Resolution = \frac{c \times \tau}{2}. \tag{2.27}$$

The blind speed is the speed which cannot be detected by the radar and also related to PRF. Since the PRF of the pulse Doppler radar is higher compared with moving target indicator (MTI) radar, the problem of blind speed is usually avoided [6]. For more information about pulse Doppler radar, readers can refer to [24].

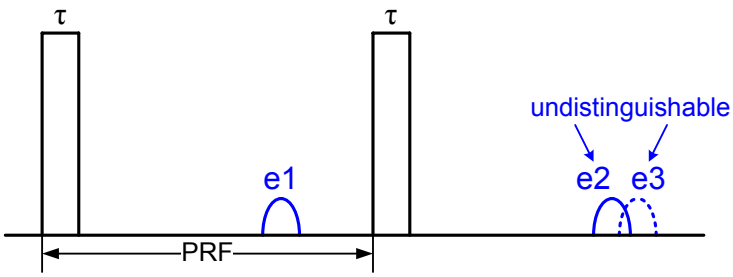

Figure 2.14: transmitted pulses and reflected echoes.

2.5 Conclusion

A brief introduction to the principles of operation of narrowband and broadband beamformers was presented in this chapter. The directivity leads to less interferences and array gain leads to improvement in the SNR of the receiver and EIRP of the transmitter. Note that such an improvement is predicated on the assumption of no coupling between different paths. Since true-time delay is preferable for UWB radar system, realizing true-time delay beamformer by manipulating the signal path length will be further exploited in the following chapters. To author's knowledge, no UWB beamforming radar with a certain modulation scheme has been reported. In following chapters, the transmitter part of a 60 GHz UWB beamforming radar will be discussed and designed. A simple architecture is exploited to realize UWB beamformer to save the chip area and satisfy the system specifications.

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Chapter 3

System Definition and Architecture

The objective of this thesis is to develop the transmitter front-end of a radar system for indoor presence detection application. A system level analysis of the 60 GHz beamforming transmitter is presented in this chapter. Together with the receiver, it constitutes the front-end of the presence detection radar. In section 3.1, the application scenario is described to illustrate how the entire system works. The system-level specifications are defined based on the link budget calculations covered in Section 3.2. Next, the design concepts of realizing true time delay are discussed in Section 3.3. The architecture and floorplan of the 60 GHz, 3-path beamforming transmitter are also proposed, which support the feasibility of realizing true time delay with 16 ps delay range and 1.1 ps delay resolution.

3.1 Application Scenario

The main usage of our presence detection radar is the detection and localization of objects (mainly people) in a room. The information will be used to control the lighting, heating and ventilation inside the room. Illustrated in Figure 3.1, the radar will be installed at the center of the ceiling, where the whole room can be monitored without obstacles. In addition, putting the radar there allows for the lowest transmit power and simple receiver design. The directivity of the beamformer is exploited in our presence detection radar. The beamformer has a 2-dimensional beam steering property. Therefore, the whole room could be scanned step by step, and each time only a small part of the room is monitored. Consequently, all the controlled home appliances, such as lighting, can be occupancy-driven. For instance, if a person is reading a book at the left side of the room, only the lamp on the left will be switched on. Therefore, it is an effective way to save energy and in line with the desire for sustainable development. As mentioned in Chapter 1, the radar is working at 60 GHz, which is suitable for short-range applications. The 60 GHz signal is greatly attenuated by concrete walls, so there is no need to worry about the interferers coming from other

wireless devices in other rooms. It is also attractive to set up a sensor network using UWB radars mounted in every room of the building. All of the information collected by the radars will be sent to the central processing unit and all of the facilities in the building can then be controlled globally. This intelligent and energy-efficient living environment is one important attribute of smart home [1]-[2].

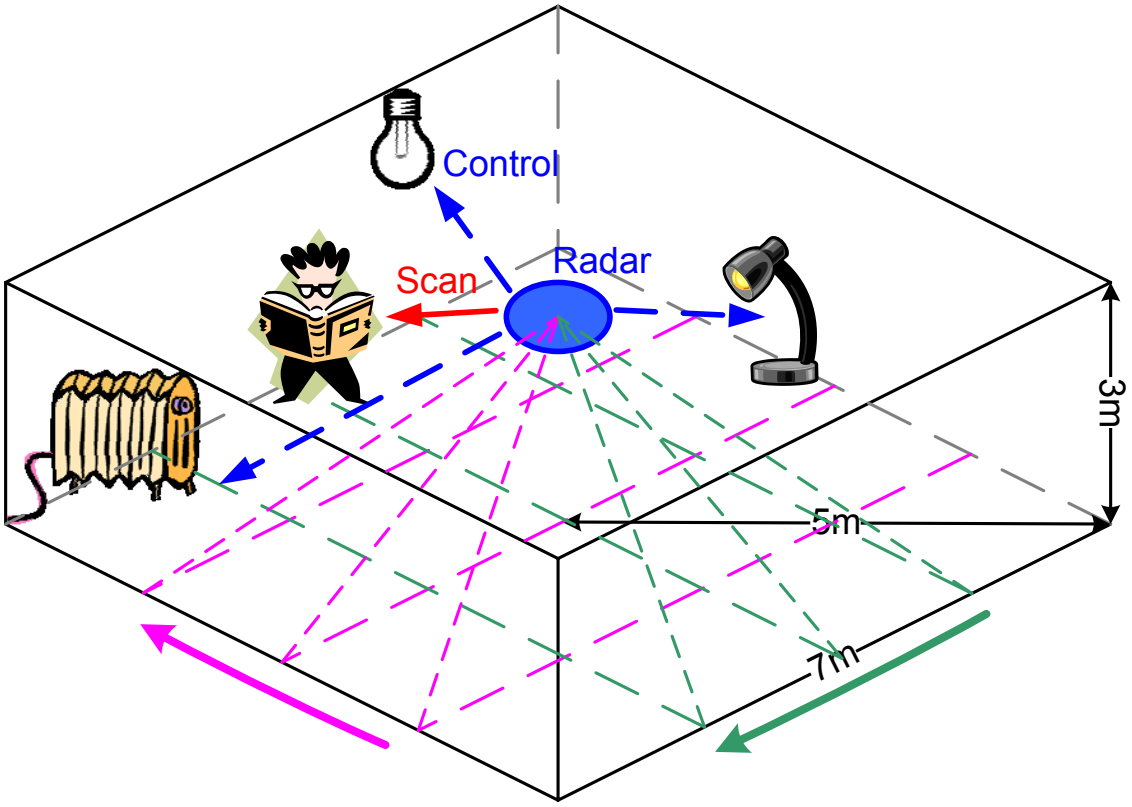

Figure 3.1: Application scenario of presence detection radar.

3.2 Link Budget

Based on the operation principles of the beamformer and radar presented in Chapter 2, and the application scenario described in Section 3.1, a 5-path beamformer is proposed to achieve two-dimensional beam steering property. Link budget calculations are covered in this section, from which system specifications is defined.

The first step in performing the link budget calculation is to determine the required signal strength at the receiver input, which is referred to as receiver sensitivity. The minimum input signal power can be defined as [3]:

$$P_{R,\min}\,|_{\mathrm{dBm}} = -174\ \mathrm{dBm/Hz} + 10\log B + NF\,|_{\mathrm{dB}} + SNR_{\min}\,|_{\mathrm{dB}}, \tag{3.1}$$

where B is the *IF processing bandwidth* in our radar system, and the sum of the first two terms defines the available thermal-noise power generated at the output of IF filter. Different from the wireless communication system where the bandwidth is defined by the data rate, the bandwidth of a pulse Doppler radar system depends mainly on the application. The higher the IF processing bandwidth, the faster the detected data can be updated. On the other hand, if the IF processing bandwidth is lowed, the radar system cannot receive enough power from a single pulse. In order to detect an object, the target must be hit by more pulses when the radar beam is scanned. The response time is then slowed. Detection of a radar signal depends on whether the receiver output is large enough to exceed a certain threshold. If the receiver output is sufficient to cross the threshold, a target is said to be present, and vice-versa. Therefore, if the radar receives many echo pulses from a target, the signal at the receiver can be averaged over several pulses to average out the effects of noise and enhance the signal level. Consequently, the radar sensitivity increases with the number of hits per target. A pulse Doppler radar usually measures range and speed of the target based on a coherent train of pulses [4] and the IF processing bandwidth required is normally much lower than the RF bandwidth. Here, the IF processing bandwidth is assumed to be 2 MHz, which is fast enough for our application. The total integrated noise power is P_N = -174 dBm/Hz + 10log$B$ = -111 dBm.

Noise figure (NF) is a measure of how much the SNR is degraded by the receiver path. Since the receiver part of our beamformer is not included in this project, 8dB is assumed for the NF of the total receiver path, based on the 60 GHz circuit modules designed and reported [5].

The minimum detectable signal-to-noise ratio ($\mathrm{SNR_{min}}$) is another important parameter to determine the minimum detectable signal, which is usually limited by the A/D converter in the analog front-end. In radar systems, digital signal processing (DSP) at the baseband can

mitigate the requirements of $SNR_{min.}$ One way to minimizing required SNR_{min} is a matched filter, which is typically now performed within the digital signal-processing function [4]. As mentioned in Chapter 2, the beamforming technique can also improve the SNR by 10log(n), which means the sensitivity can be improved by 7 dB for a 5-path beamformer. In the following calculation, the required SNR by the radar signal processing unit is simply chosen as 0 dB, which is not a stringent requirement for the reception part [5]. Therefore, the minimum detected input signal is $P_{R,min}$ = -174 dBm/Hz + 10log$B$ + NF + SNR_{min} = -103 dBm.

After obtaining the minimum detected input signal, the radar equation (equation 2.23) is used to determine the required output power of our transmitter. From equation (2.23), the minimum required output power (P_T) is

$$P_T = \frac{P_R (4\pi)^3 d^4}{G_T G_R \lambda^2 \sigma}. \tag{3.2}$$

The dimension of the room defines the maximum distance d that the EM waves travel. In an ordinary living space, like the one shown in Figure 3.1, the distance between the center of the ceiling and the bottom corner of the room is usually no more than 6 meters. The RCS of a target (e.g., a person), however, differs dramatically depending on the position, posture and direction of motion. The typical RCS of a person at microwave frequency is 0.1 to 1 m^2 [6]-[7]. G_T and G_R are the transmitter and receiver antenna gains, respectively. Due to the pulse-mode modulation scheme we are going to apply, they have the same value since transmission and reception will be done with the same antenna. According to previous work [5], a dipole antenna with 4 dBi antenna gain and hemispherical radiation pattern can be implemented in NXP Semiconductors' LAMP3 technology [8], which is a possible antenna solution to the whole beamforming system. Summing all these information up, the required transmitting power is 8.158 mW (9.1 dBm).

Furthermore, due to beamforming, the effective isotropic radiated power (EIRP) transmitted by the array is increased by n^2 times, as shown in Figure 3.2. The power expected from a single path can be further reduced by 14 dB for a 5-path beamformer, which is $P_t = P_T$ – 20log5 = -4.9 dBm.

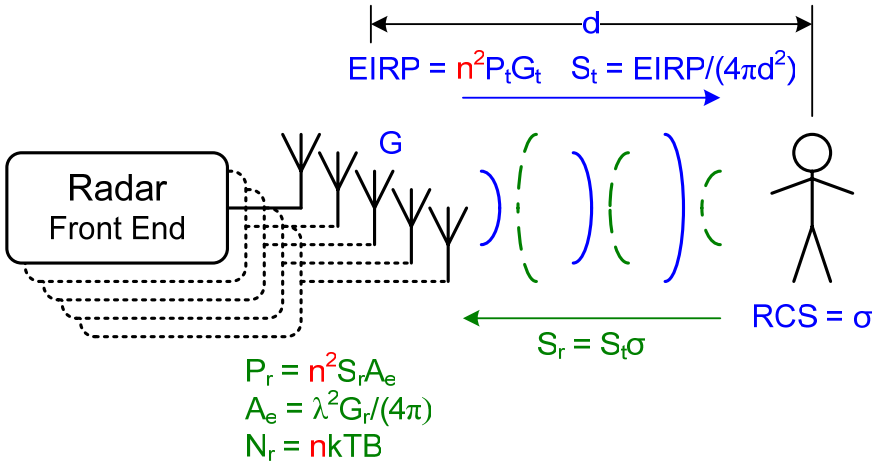

Figure 3.2: Radar front-end with beamforming link budget.

The power P_t derived above is the average power transmitted, which corresponds to the energy per unit time radiated by the radar. For a pulse Doppler radar, the transmitter waveform is a train of rectangular pulses of width τ and pulse repetition period T_p, the average power is related to the peak power of the pulse by:

$$P_t = \frac{\tau}{T_P} P_{pk} \,. \tag{3.3}$$

The pulse width is chosen to be 1 ns, which implies the range resolution can be 15 cm. The pulse repetition frequency is selected as 20 MHz and thus the maximum unambiguous range can be as far as 7.5 meters. Since the speed of target moving in a room (e.g., a person) is relatively slow (< 10 m/s), there will be no problem with speed ambiguity (minimum blind speed for 20 MHz PRF is 2.5 km/s). Having pulse width of 1 ns and PRF of 20 MHz, the transmitter in a single path needs to deliver approximately 12 dBm power to reach the requirements, which is 17 dB higher than the average radiating power.

The practical transmitted signal is always emitted with wide skirt of phase noise [3], which dominates the noise contribution close to the carrier frequency. Figure 3.3 depicts the ideal and practical operation of radar. Since the offset frequency (Doppler frequency) between transmitted and reflected signal is small, the reflected signal might be overwhelmed by clutter [6] and cannot be detected correctly.

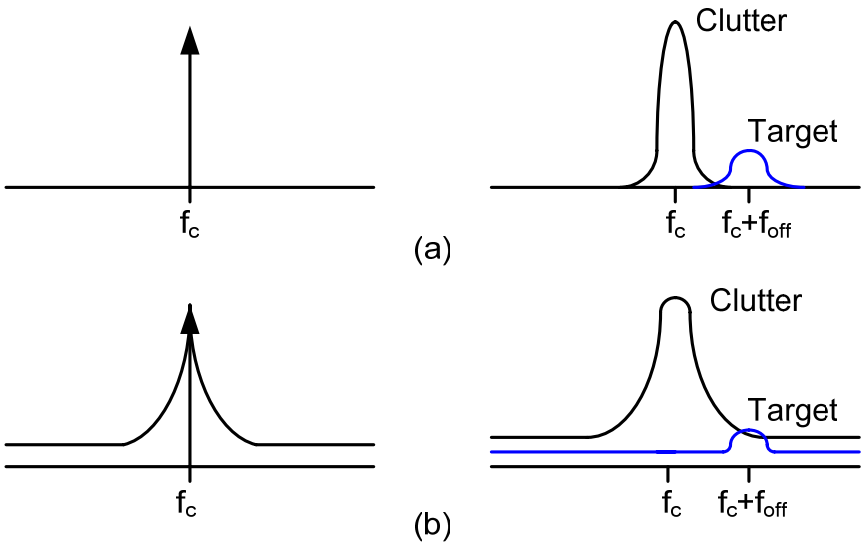

Figure 3.3: (a) ideal transmitted signal & corresponding received signal, (b) practical transmitted signal & corresponding received signal.

The effect of "range correlation" [9] helps to suppress the phase noise if the same LO signal is used for transmission and for downconversion of the reflected signal, featured in Figure 3.4. The shorter the time delay between the transmitted and reflected signals, the stronger the correlation will be and the more noise reduction can be expected. The residue phase noise after demodulation is given by [10]

$$S_{\Delta\phi}(f_o) = S_{\phi}(f_o)\left[4\sin^2\left(2\pi\frac{Rf_o}{c}\right)\right], \tag{3.4}$$

where S_ϕ is the phase noise in the received signal, f_o the offset frequency, c the speed of light, and R the target range. For the target range of 6 m and offset frequency of 2 kHz, the suppression equals -66 dB, which implies the phase noise is attenuated by 66 dB. For a lower offset frequency, the attenuation can be even higher. After range correlation is employed, the residue phase noise is usually lower than the thermal noise floor and the derivation of the link budget studied above still stands.

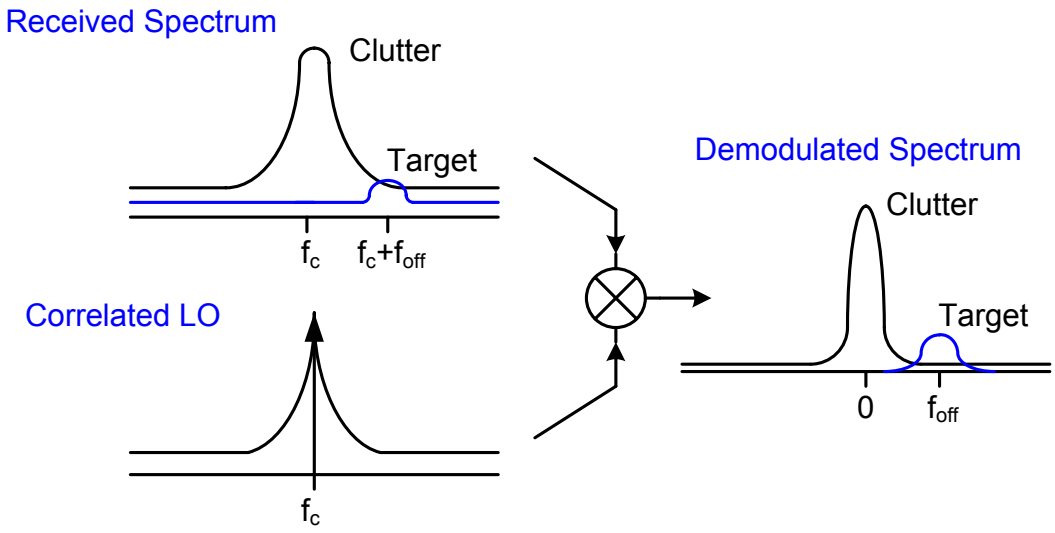

Figure 3.4: Illustration of range correlation effect on received signal.

Next, the beam-steering specification of the system is considered. Equation (2.12) describes that the beam steering resolution depends on the delay resolution and the incident angle, which is repeated as below:

$$\tau_{d\_res} = \left(\frac{d}{c}\right)\left(\sin\theta_{steer} - \sin\theta_{incident}\right), \tag{3.5}$$

where τ_{d_res} is the delay resolution, d is the antenna spacing, c is the speed of light, $\theta_{incident}$ is the incident angle and the difference between θ_{steer} and $\theta_{incident}$ can be regarded as the steering resolution. The antenna spacing is fixed as one-half of the wavelength of the 60 GHz signal (2.5 mm), in order to avoid the grating lobes. The delay resolution is chosen as 1.1 ps, which implies the steering resolution can be 9.5^o for the zero incident angle. As the angle of radiation becomes more oblique, the beam-steering resolution decreases. For indoor presence detection application, a radar mounted on the ceiling of a room can distinguish between two objects on the floor with a distance of 0.5 meters or so, with this beam steering resolution. Figure 3.5 shows that 15 discrete delays are generated and the beam can be steered from -75^o to $+75^o$. As mentioned in Chapter 2, the beam width depends on the length of the array (number of paths n times antenna spacing d) and the incident angle θ. In our case, the beam width is approximately 33^o and 47^o when the incident angle is 0^o and 45^o, respectively, if the radiation pattern of the antenna is isotropic. Therefore, even if the incident angle is 90^o, it can still be detected by the radar.

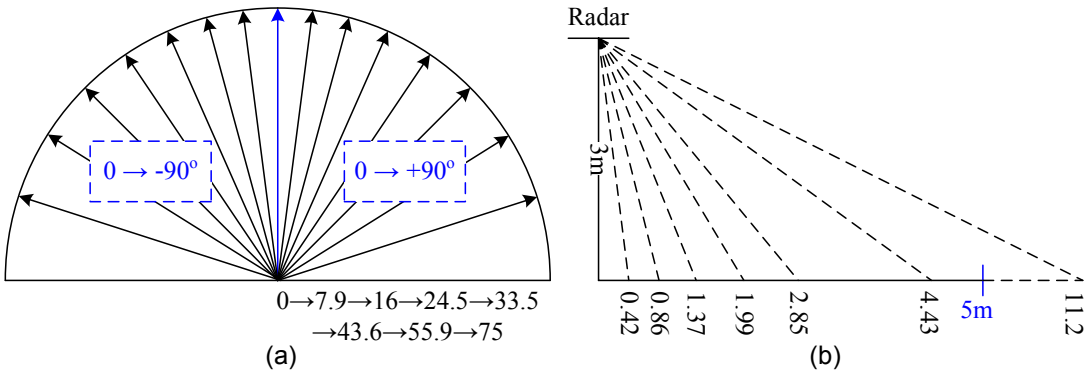

Figure 3.5: (a) beam steering range & resolution, (b) corresponding horizontal range resolution.

In summary, the link budget and system specification of 60 GHz pulse Doppler radar with beamforming is listed in Table 3.1.

3.3 System Architecture

The UWB beamformer described in this work is based on true time delay. The delay is varied by manipulating the signal path length. In order to scan the whole room with a focused beam, a two-dimensional beamformer must be exploited. One of the solutions is shown in Figure 3.6, which contains 5 delay paths. The delay in path 0 is fixed (0 ps) while the delay in other 4 paths can be varied from -8 ps to +8 ps, with a delay resolution of 1.1 ps. Paths 0, 1 and 2 mainly contribute to form the beam in one dimension while paths 0, 3 and 4 are used to form the beam in the other dimension. The final radiation pattern is the combined version of these two beams. In this work, only a one dimensional beamformer is realized in order to reduce the design time and chip area required for implementation. The system architecture and design concepts used in this work can be extended to realize a two-dimensional beamformer, which is a good reference to the future work.

Table 3.1: Link budget & system specification.

Name	Value	Comments
Carrier Frequency	60 GHz	typical (57 – 66 GHz)
Temperature	300 K	typical (-40^o – 120^o, junction temperature)
Oxygen Attenuation	10-16 dB/km	negligible
RCS (σ)	0.1~1 m^2	person
Max. Detection Range	6 m	RCS = 0.1 m^2
Object Velocity	0~10 m/s	indoor walk
Range Resolution	15 cm	pulse width 1ns
Beam Width	33^o	0^o radiation angle, 3 paths
Beam Steering Range	-75^o~75^o	15 discrete phases, 16 ps delay range
Beam Steering Resolution	9.5 ^{o}	0^o radiation angle, 1.1 ps delay resolution
Tx/Rx Antenna Gain	4 dBi	assumed
RF Bandwidth	10 GHz	57 – 66 GHz
IF Processing Bandwidth	2 MHz	application dependent
Noise Floor	-111 dBm	kTB_{IF}
SNR_{array}	0 dB	assumed
NF for RF Front-end	8 dB	estimated (LNA + Mixer)
Min. Rx Power	-103 dBm	kTB_{IF} + NF + SNR_{array}
Range Correlation Effect	-66 dB	6 m range, 2 kHz offset freq
Min. Tx Power		single path
@3 m, σ=0.1 m^2	0 dBm	pulse mode PA with 2% duty cycle; less power is required as pulse width increases.
@3 m, σ=0.5 m^2	-7 dBm	
@6 m, σ=0.1 m^2	12 dBm	
@6 m, σ=0.5 m^2	5 dBm	
IC Process	130 nm SiGe:C BiCMOS	

The realization of the delay path with large delay range and fine delay resolution is the most important innovation in this work. Optimizations are performed at the circuit and system levels, which are described in the following sections.

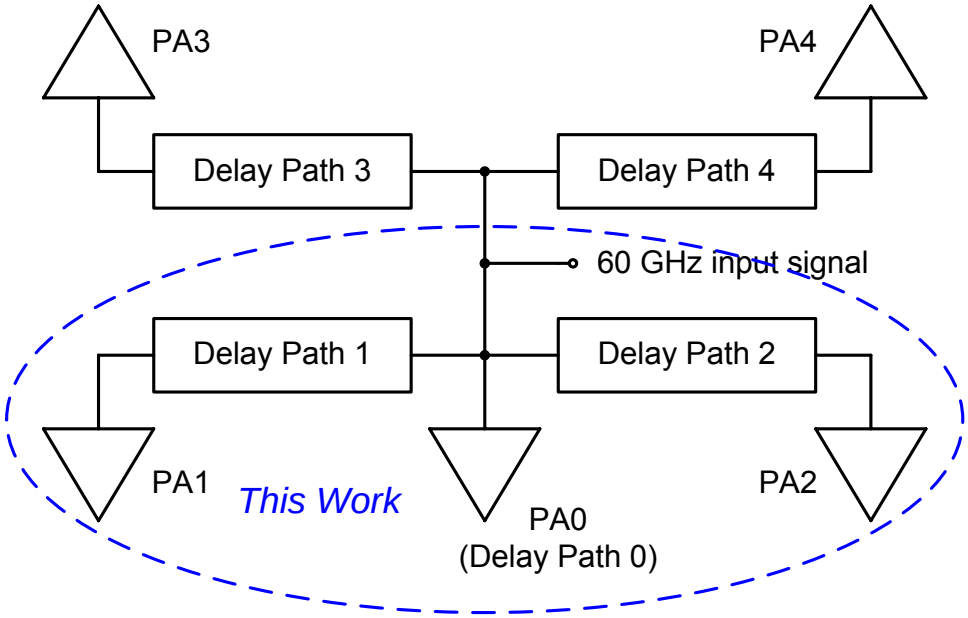

Figure 3.6: two-dimensional beamformer with 5 paths.

3.3.1 Group Delay Variation

The transit time of a signal through a device or a signal path can be measured by group delay [11]. Group delay is a useful measure of phase distortion and is defined by differentiating the phase response versus frequency, which is given by

$$t_d = -\frac{1}{2\pi}\frac{d\varphi}{df}. \tag{3.6}$$

A linear phase response is converted to a constant group delay (representing the average signal-transit time) while deviations from linear phase are transformed into deviations from constant group delay. Therefore, the variations in group delay can cause signal distortion, just as deviations from linear phase results in distortion.

A matched transmission line has a linear phase response between input and output, and the transit time of signal from one end to the other equals the length of the line divided by the

propagation velocity. Hence, it is promising to achieve the programmable delay by manipulating the signal path length. However, the effect of reflections from discontinuities at each end of the transmission line will introduce some delay variations. In order to minimize the impact of these reflections, the effect of discontinuities on the group delay of a transmission line is studied.

As shown in Figure 3.7, if the source impedance Z_S and the load impedance Z_L are different from the characteristic impedance Z_O of the transmission line, a fraction of the main wave traveling down the transmission line is reflected back towards the source, and then re-reflected once more to combine with the main wave traveling towards the load. In the case of small reflections (or a lossy transmission line), multiple reflections may be neglected, and only the dominant effect is considered. The combined wave is expressed as

$$V(z) = V^+ e^{-\alpha z} e^{-j\beta z} + \Gamma_L V^+ e^{-\alpha(2l-z)} e^{-j\beta(2l-z)} + \Gamma_S \Gamma_L V^+ e^{-\alpha(z+2l)} e^{-j\beta(z+2l)} \quad (3.7)$$

$$= V^+ e^{-\alpha z} e^{-j\beta z} \left(1 + \Gamma_L e^{-2\alpha(l-z)} e^{-j2\beta(l-z)} + \Gamma_S \Gamma_L e^{-2\alpha l} e^{-j2\beta l}\right), \quad (3.8)$$

where V^+ is voltage amplitude, α the attenuation constant, β the phase constant, l the length of transmission line, Γ_S the source reflection coefficient and Γ_L the load reflection coefficient. We assume that the reflection coefficients have no phase components.

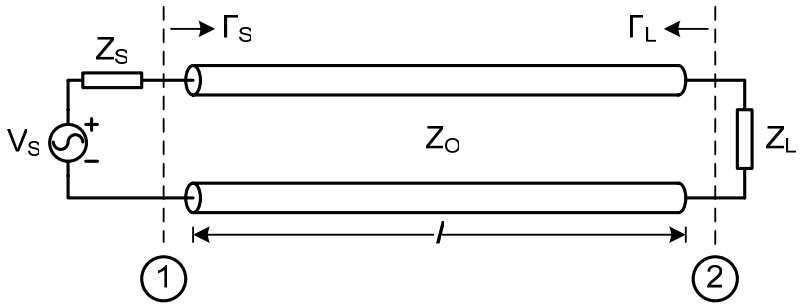

Figure 3.7: Transmission line with mismatch discontinuities at each end.

The reflected wave travels farther than the main wave, and thus its phase varies faster with frequency. As a result, the combined phase shift does not vary linearly with frequency but has a cyclical variation ($\Delta\varphi$) superimposed on the linear part. The deviation from the linear phase can be derived from equation (3.8). For simplicity, only the case where $z=l$ is considered and the extra phase equals

$$\Delta\varphi = -\arctan\frac{\Gamma_S\Gamma_L e^{-2\alpha l}\sin(\beta 2l)}{1+\Gamma_L+\Gamma_S\Gamma_L e^{-2\alpha l}\cos(\beta 2l)} \tag{3.9}$$

$$= -\arctan\frac{\Gamma_S\Gamma_L e^{-2\alpha l}\sin(2\omega l/v_p)}{1+\Gamma_L+\Gamma_S\Gamma_L e^{-2\alpha l}\cos(2\omega l/v_p)}, \tag{3.10}$$

where v_p is the propagation velocity. The delay variation can then be derived by taking the derivative of equation (3.10) versus angular frequency, which is given by

$$\Delta t_d = -\frac{d\Delta\varphi}{d\omega} \tag{3.11}$$

$$= \frac{d\left\{\arctan\dfrac{\Gamma_S\Gamma_L e^{-2\alpha l}\sin(2\omega l/v_p)}{1+\Gamma_L+\Gamma_S\Gamma_L e^{-2\alpha l}\cos(2\omega l/v_p)}\right\}}{d\omega} \tag{3.12}$$

$$= \frac{l}{v_p}\frac{2\Gamma_S\Gamma_L e^{-2\alpha l}\left[(1+\Gamma_L)\cos(2\omega l/v_p)+\Gamma_S\Gamma_L e^{-2\alpha l}\right]}{(1+\Gamma_L)^2+2(1+\Gamma_L)\Gamma_S\Gamma_L e^{-2\alpha l}\cos(2\omega l/v_p)+\Gamma_S^2\Gamma_L^2 e^{-4\alpha l}} \tag{3.13}$$

$$= \frac{l}{v_p}\frac{2\mathrm{A}\left[\cos(2\omega l/v_p)+\mathrm{A}\right]}{1+2\mathrm{A}\cos(2\omega l/v_p)+\mathrm{A}^2}, \tag{3.14}$$

in which

$$\mathrm{A} = \frac{\Gamma_S\Gamma_L}{1+\Gamma_L}e^{-2\alpha l}. \tag{3.15}$$

Therefore, the effective group delay is the "intrinsic" delay t_{d0} (with no reflections) superimposed by a delay variation Δt_d, which can be expressed by

$$t_d = t_{d0} + \Delta t_d \tag{3.16}$$

$$= \frac{l}{v_p} + \frac{l}{v_p}\frac{2\mathrm{A}\left[\cos(2\omega l/v_p)+\mathrm{A}\right]}{1+2\mathrm{A}\cos(2\omega l/v_p)+\mathrm{A}^2} \tag{3.17}$$

$$= \frac{l}{v_p}\left(1+\frac{2\mathrm{A}\left[\cos(2\omega l/v_p)+\mathrm{A}\right]}{1+2\mathrm{A}\cos(2\omega l/v_p)+\mathrm{A}^2}\right). \tag{3.18}$$

The effective group delay varies with frequency and the variation Δt_d is between the following limits:

$$-\frac{l}{v_p}\frac{2\mathrm{A}}{1-\mathrm{A}} \le \Delta t_d \le \frac{l}{v_p}\frac{2\mathrm{A}}{1+\mathrm{A}}. \tag{3.19}$$

For a 1 mm lossless transmission line and 50% mismatch ($\Gamma_S = \Gamma_L = 0.3$), the effective group delay versus frequency is plotted in Figure 3.8, assuming that the propagation velocity equals one-half speed of light. The frequency of delay variation is not singular and it also depends on the length of the transmission line, the reflection coefficient and the working frequency.

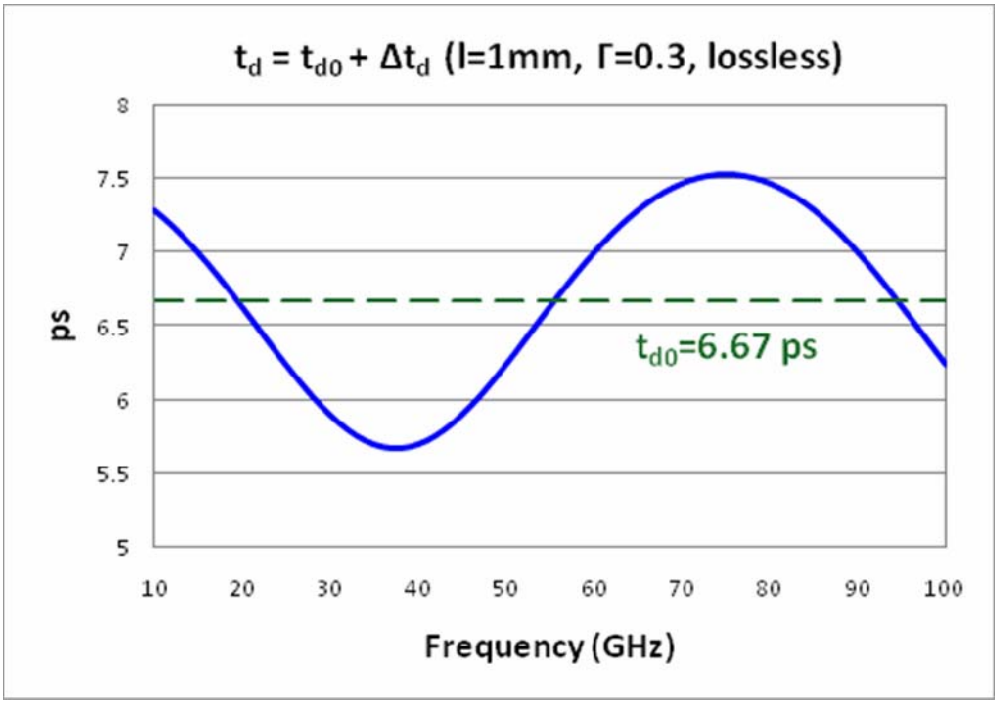

Figure 3.8: Group delay varies with frequency if mismatch exists.

Although the above derivation is simplified, the results are straightforward and insights can be obtained about how to reduce group delay variation. From equations (3.15) and (3.19), the magnitude of delay variation depends on the reflection coefficient, the length of transmission line and the attenuation constant. The delay deviations can be positive or negative and their limits are not necessarily equal, as shown in Figure 3.9. The transit time of a signal traveling through 1 mm transmission line is 6.67 ps while 13.3 ps is needed for 2 mm transmission line, assuming that v_p equals one-half speed of light. Compared with the "intrinsic" group delay, the magnitude of the delay variation can be a large fraction of the

total delay if the reflection coefficient is close to one. The magnitude of the delay variation increases nearly exponentially with the reflection coefficient. Therefore, matching at both ends of the transmission line is important to minimize the delay variation. Furthermore, if the transmission line is lossy, the magnitude of delay variation decreases because less signal power is reflected back. The typical value of the attenuation constant in used technology is 0.5 dB/mm (0.058 Np/mm), while 5 dB/mm is used to exemplify the influence of transmission line loss in Figure 3.9.

Conclusions can be drawn in order to minimize the group delay variation. Firstly, make the source and load impedance equal to the characteristic impedance of the transmission line. Since our system is working at 60 GHz, the bandwidth of these termination impedances should also be checked carefully to make sure that they have the correct value at the working frequency. Secondly, make the signal path as short as possible in order to reduce the "intrinsic" transit time, which has a direct relationship with the magnitude of group delay variation. Finally, it should also be mentioned that the characteristic of the on-chip transmission line is not constant in practical case; using differential transmission line instead of single-ended one is also helpful to minimize the group delay variation.

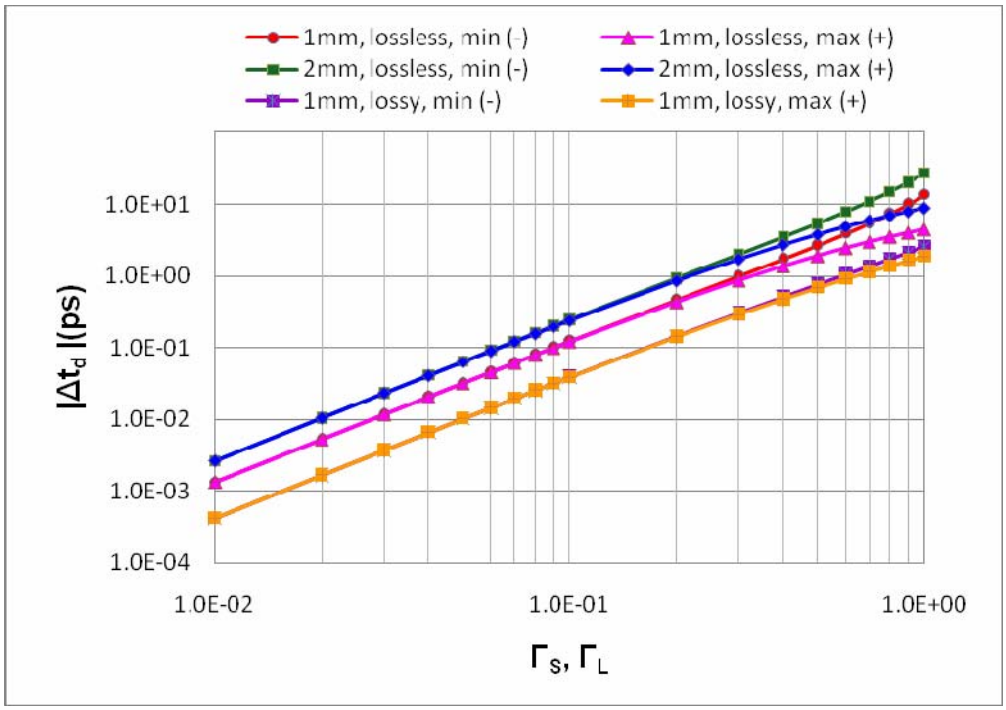

Figure 3.9: delay variation versus reflection coefficient.

3.3.2 The Concept of Loaded Transmission Line

The delay path in the system (see Figure 3.6) is featured in Figure 3.10. The structure consists of GSSG transmission lines and path-select amplifiers to achieve approximately 16 ps total delay with 1.1 ps delay resolution. The GSSG transmission line is used for differential signal transfer and the programmable delay is achieved by switching the signal path through one of the 15 path-select amplifiers. The loaded transmission line structure looks quite similar to the periodic structure [11], which is widely used in microwave filters. However, since the distance between the two amplifiers is much less than the wavelength, there is no stopband in our structure and the signal is only attenuated by the inherent loss of the line and the amplifier.

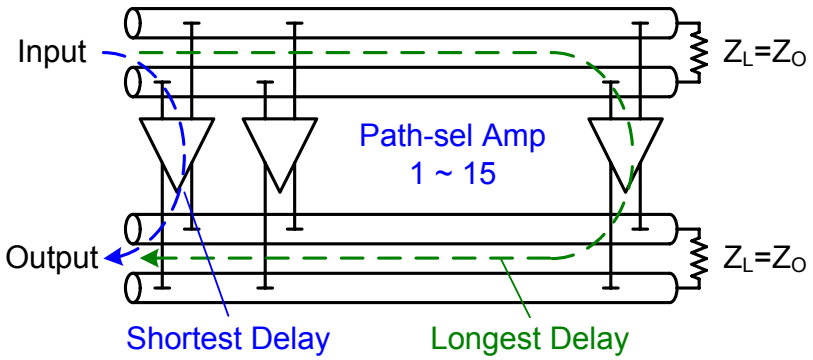

Figure 3.10: Single delay path.

The path-select amplifiers are periodically inserted into the delay path, so it is sufficient to analyze one section with one amplifier to get the whole picture of the delay path. As shown in Figure 3.11, L_{dm} and C_{dm} are the differential mode lumped inductance and capacitance of one GSSG transmission line section, respectively, while C_{amp} is the input or output capacitance of the path-select amplifier and G_{amp} is the input or output conductance of the path-select amplifier. Here, the loss of the transmission line and parasitic capacitance of interconnects are ignored. The model of this loaded transmission line is quite similar to the model of a normal transmission line and its characteristic impedance is expressed as:

$$Z_o = \sqrt{\frac{j\omega L_{dm}}{G_{amp} + j\omega\left(C_{dm} + C_{amp}\right)}}. \tag{3.20}$$

In order to achieve the optimum performance, it is important to maintain the characteristic impedance constant within the operating bandwidth. Therefore, the differential input and output resistances of the amplifier must be kept as high as possible (the differential input and output conductance G_{amp} are kept as low as possible) in both active and inactive states. For 5 fF capacitance, which is a reasonable estimation of the total effective capacitance of a single section, its reactance at 60 GHz is approximately 530 Ω. Therefore, the input and output resistances of the path-select amplifier should be at least 10 times larger than this value, no matter whether the amplifier is active or not.

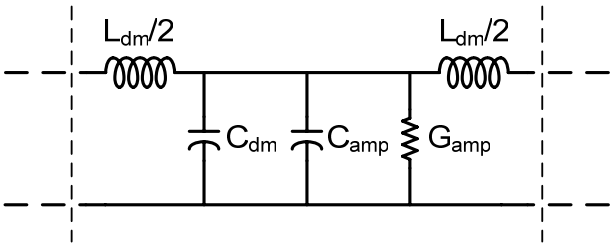

Figure 3.11: One section of differential mode equivalent circuit of a GSSG transmission line with an active switch amplifier.

On one hand, path-select amplifiers usually have different input and output impedance values in the on-state and off-state. When the amplifier is active, the input and output resistances usually have lower values. Therefore, some discontinuities may even occur at the location of the on-state amplifier, which will probably enlarge the group delay variation. On the other hand, the input and output resistances of the off-state amplifiers decrease at the rate of 20 dB/dec at high frequency (>1 GHz). When the values of these resistances are comparable to the value of the characteristic line impedance, the effective line impedance will decrease greatly and thus the group delay variation increases exponentially. Furthermore, the input and output capacitances have to be kept low as well. Otherwise, the effective loaded transmission line impedance will decrease and thus more power must be dissipated in the delay path to keep a reasonable output signal level. The design of the path-select amplifier and the analysis of its input and output impedance in both state will be discussed in Chapter 4 in detail. If the input and output resistances of the amplifiers are infinitely large, the effective characteristic line impedance $Z_{o,eff}$ and the delay time per section $t_{d,eff}$ can be expressed as

$$Z_{o,eff} = \sqrt{\frac{L_{dm}}{C_{dm} + C_{amp}}} \tag{3.21}$$

and

$$t_{d,eff} = \sqrt{L_{dm}\left(C_{dm} + C_{amp}\right)}\,. \tag{3.22}$$

Consequently, the loaded transmission line has a reduced characteristic impedance and increased delay with respect to the unloaded transmission line. Finally, to ensure flat group delay, the cutoff frequency [12] of the loaded line structure should be 10 times greater than the highest frequency of operation, which is given by

$$f_{cutoff} = \frac{1}{\pi\sqrt{L_{dm}\left(C_{dm} + C_{amp}\right)}}\,. \tag{3.23}$$

3.3.3 Architecture of 3-path Beamforming Transmitter

The architecture and floorplan of the 60 GHz 3-path beamforming transmitter is featured in Figure 3.12, aiming at satisfying all the system specifications, especially realizing fine delay resolution with minimum group delay variation. The beamformer is mainly composed of two parts: the delay path, which is used for generating the programmable delay, and the power amplifier, which is needed to emit the required output power.

In the signal path, the 60 GHz input signal is fed by an off-chip signal generator. Since it is almost impossible to have a low-impedance ground plane across the whole chip at microwave frequency, all the on-chip signals are differential. The differential signaling has local virtual ground and high immunity to "environmental" noise, which ensure the integrity of the signal. Therefore, the single-ended input signal is first converted in differential configuration by an active single-ended to differential converter. Then an active power splitter is used to split the signal power and feed them into the left and right delay paths. Another useful property of the active power splitter is to make good isolation between left and right paths. If the isolation is poor, the reflected wave from the right path will combine with the main wave in the left path and increase the group delay variation in the left signal path. As mentioned in the previous section, 15 path-select amplifiers are used

to manipulate the length of signal path. Controlled by the local decoder, each time there is only one amplifier works in ON state and all the other amplifiers are in OFF state. Again, in order not to load the GSSG transmission line too much, and also to make the characteristic impedance of the loaded line constant within the operating bandwidth, the input and output resistances of the switches must be kept as high as possible while the input and output capacitances of the switches must be made as low as possible. With these path-select amplifiers and GSSG transmission lines, a 16 ps delay range and 1.1 ps delay resolution can be achieved. The delay in the left signal path varies from -8 to +8 ps while the delay in the right signal path varies from +8 to -8 ps. The delay in the center path remains constant, which is the reference (i.e., 0 ps) delay. Afterwards, the delayed signals are amplified by three power amplifiers, respectively. Based on the link budget calculation, in order to detect a person standing in the corner of the room, 12 dBm output power is required from each amplifier in the worst case. Another specification for the power amplifier which has to be fulfilled is to minimize the group delay variation around the working frequency. Otherwise, all our efforts might be wasted if the matching between these three power amplifiers is not satisfactory. The difference between the signal transit time through these three power amplifiers will add to the delay between signals directly and degrade the final performance of the beamforming system.

Pulse modulation is used for the radar system. The timing circuitry on the bottom left of Figure 3.12 is used to provide the pulses which modulate the output signal of the power amplifier. Besides, supply and temperature insensitive biasing is also implemented on chip to ensure reliable operation of the system.

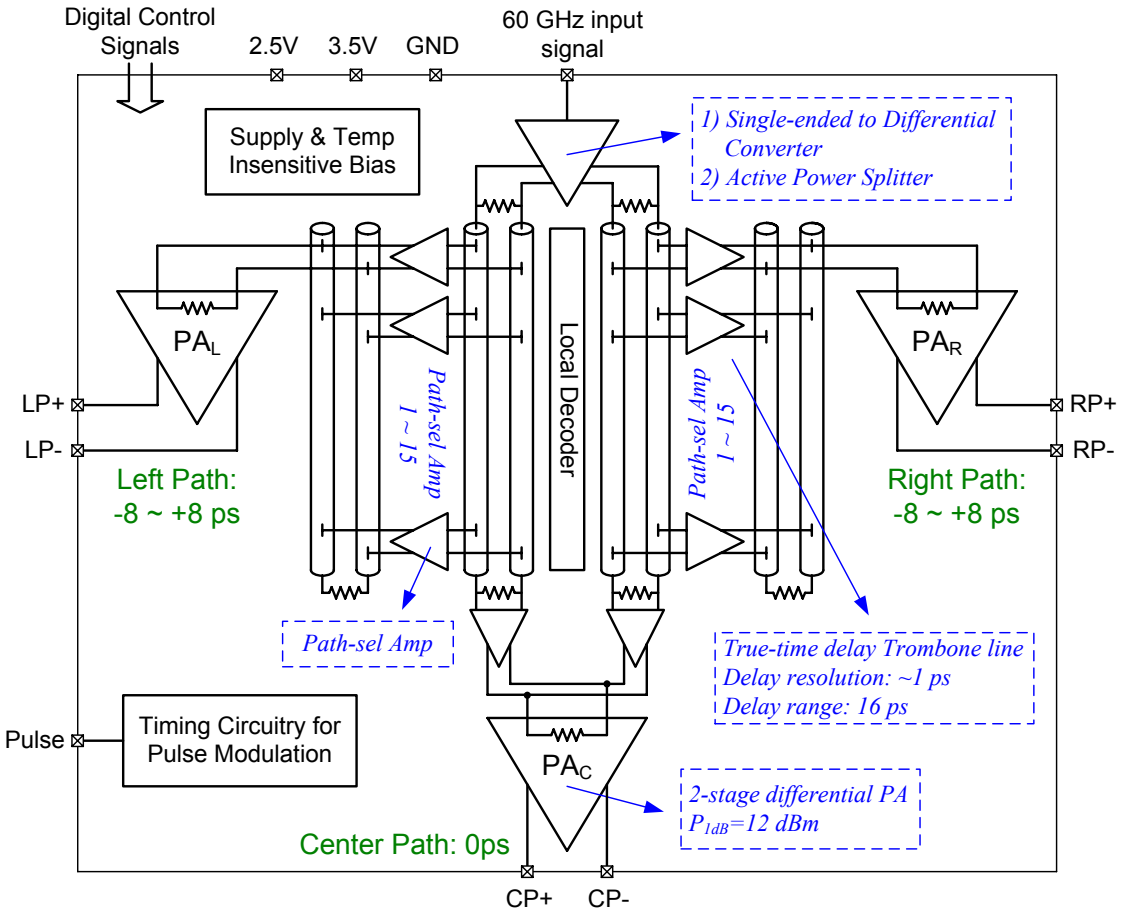

Figure 3.12: Architecture and floorplan of 60 GHz 3-path beamforming transmitter.

3.4 Conclusion

The presence detection radar is a component of the future smart-home systems and the application scenario was described in this chapter. Based on principles of beamforming and radar, a link budget calculation was used to determine the system specification. The design challenges to minimize the group delay variation were analyzed at the system and circuit levels. Finally, the architecture and floorplan of the 60 GHz 3-path beamforming transmitter was proposed, which provided the feasibility of realizing a true time delay with 16 ps delay range and 1.1 ps delay resolution. The circuit level design and implementation of the 3-path beamforming system will be described in the next chapter.

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Chapter 4

Trombone Delay Line Design

In this chapter, the circuit level implementation of trombone delay line in the beamforming transmitter is presented. Following a discussion of the device metrics, the design and verification of the delay line and bias blocks are performed.

4.1 Device Metrics

The beamforming transmitter will be implemented in 130nm SiGe BiCMOS process, which is dedicated to millimeter-wave applications, such as 60 GHz WLAN, 77 GHz automotive radar and 80 Gb/s optical communication. This technology offers a fully self-aligned 230 GHz f_T and 280 GHz f_{MAX} SiGeC HBT with BVCEO of 1.6 V. Dual V_T (high performance / low leakage) and dual gate oxide (1.2 V / 2.5 V) 130 nm CMOS devices are also available. For the back end of line, six copper metal layers with three thick metal layers (metal 4 to 6) ensure the excellent performance of passive devices at microwave frequency. The on-chip microstrip transmission line has a measured attenuation per unit length of 0.5 dB/mm at 80 GHz. This technology also offers MIM capacitors, spiral inductors and a variety of resistors, including high-resistance unsilicided poly resistor.

A figure-of-merit analysis was performed on a SiGeC HBT device (1 μm emitter length, 0 V base-collector voltage, 60^{o}C temperature, CBE structure), from which the circuit performance can be predicted. The curves in Figure 4.1 are obtained from Spectre circuit simulation. The transit frequency f_T optimistically predicts the gain-bandwidth product. From Figure 4.1, the gain is only around 3 at 60 GHz if the transistor is biased at 1 mA/μm. The unity power gain frequency f_{MAX} has more relevance to the actual situation in an amplifier, which is a useful metric in the LNA and PA design. Benefitting from low base resistance of the HBT device, the simulated peak f_{MAX} is 350 GHz at 1.5 mA biasing current. During circuit design, bias conditions and device size need to be selected carefully

in order to maximize the operating margin [1]. The available bandwidth f_A is the 3 dB bandwidth of a single-ended amplifier designed for 20 dB low-frequency voltage gain [2]. Such a high gain puts emphasis on the output bandwidth of a transistor to account for extra loading effects. It is a valuable metric for broadband amplifier design, such as current-mode logic (CML) circuits. f_{cross} is another device metric which is an indicator to the performance of cross-coupled LC VCOs [3].

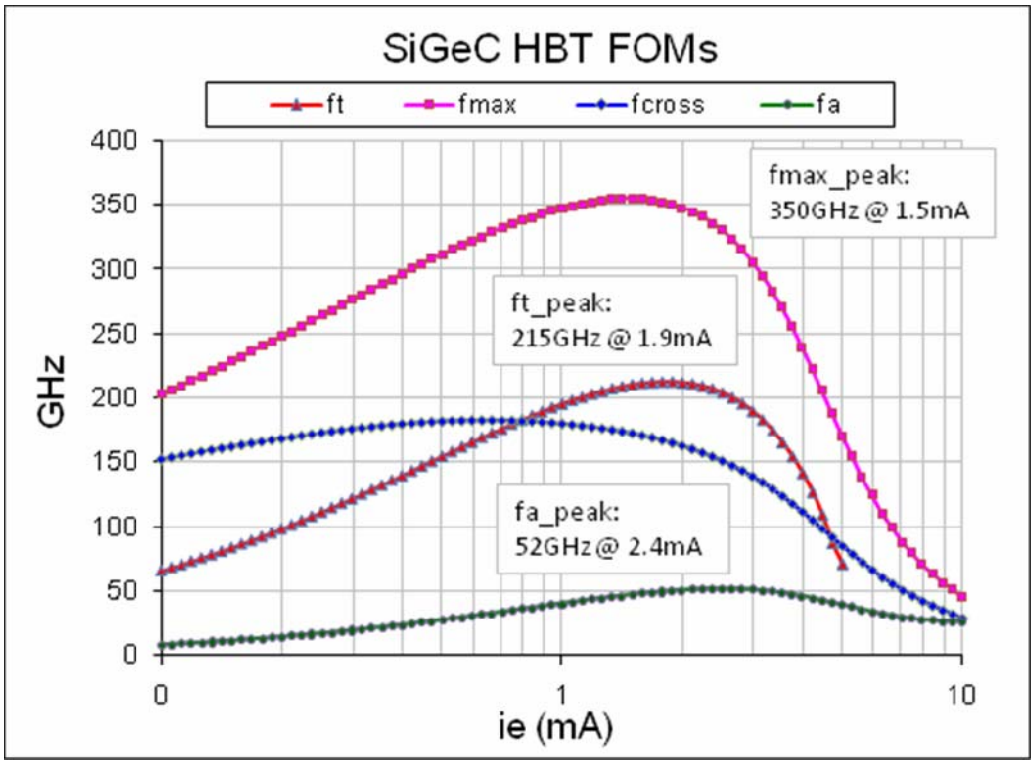


Figure 4.1: SiGeC HBT device FOMs in 130 nm BiCMOS technology.

4.2 Trombone Delay Line

The trombone delay line is the key block in the beamforming system, as shown in Figure 3.12. It includes path-select amplifiers, GSSG differential transmission lines and the local decoder. The local decoder is shared between the left and right paths. The trombone delay line is designed for 16 ps delay range and 1.1 ps delay resolution. In a media with ε_r of 4 (SiO_2), it takes 0.5 ps to travel through 75 μm line lengths. In considerations of the extra parasitic capacitances from the path-select amplifier and metal lines, the length of a single

section delay line is limited to 60 μm. For a 60 μm, 100 Ω differential line, the lumped inductance L_{dm} and capacitance C_{dm} are 40 pH and 4 fF, respectively. There is a trade-off when choosing the transistor size in the path-select amplifier. If the device size is small, the gain of the amplifier will be low. If the device size is large, the characteristic impedance of the loaded transmission line will decrease and more current has to be consumed to keep a reasonable output signal level. If the parasitic capacitance from the amplifier and metal lines is 3 fF, the line impedance is reduced to 75 Ω. More accurate iterations of the design are necessary to optimize the performance. In order to have relatively flat group delay, 70 GHz bandwidth is required for the path-select amplifier. In addition, since 15 amplifiers are placed periodically along the delay line, the isolation between the input and output of a single amplifier should be at least 65 dB. In that case, the combined leakage power from all of the inactive amplifiers can be 100 times less than the desired signal power. How fast the amplifier can be switched on and off depends on the application. A switching time of 0.1 μs is sufficiently fast for our presence detection radar. Table 4.1 lists a summary of the specifications for the trombone delay line, based on the analysis above and from Section 3.3.

4.2.1 Path-select Amplifier

4.2.1.1 Device Model

The specification of the path-select amplifier is critical. Since the Spectre simulation cannot offer much insight about how to optimize the circuit performance, a sufficiently accurate small signal model is indispensible for hand calculations.

Figure 4.2 shows the device model used. The component values in the figure are obtained for a transistor of 1 μm in emitter length. The values of all series resistances (R_b, R_e and R_c) can be scaled with the emitter length with sufficient accuracy. The junction capacitances (C_{je} and C_{cb}) depend on the emitter length and the voltage across the capacitance. The diffusion capacitance C_{diff} and the small-signal output resistance r_o are scaled with the biasing current, while the small signal input resistance r_π is determined by the biasing current and current gain of the transistor. The DC current gain of the 1 μm length transistor

is 150 and 88 at 1 and 2 mA biasing currents, respectively. That is why r_π decreases by nearly a factor of 4 when the biasing current increases from 1 to 2 mA. Although the model in Figure 4.2 is much simpler than the transistor model used by Spectre simulator, it is still complicated during calculation. Depending on which performance parameter you are going to inspect, some components can be ignored in order to gain insight. For example, when deriving the low frequency gain of the differential amplifier, R_e is the only series resistance that needs to be taken into account.

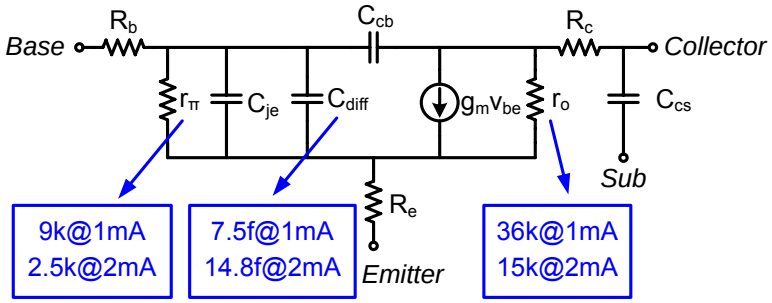


Figure 4.2: Small signal model for calculation (1 μm emitter length).

Table 4.1: Trombone delay line specifications.

Trombone Delay Line	
Delay Range	16 ps
Delay Resolution	1.1 ps
Unloaded Line Impedance	100 Ω (differential)
Temperature	60° (simulation setting)
Path-select Amplifier	
Input & Output Resistance	> 10 kΩ (both states)
Input & Output Capacitance	< 3 fF (both states)
3 dB bandwidth	> 70 GHz
Isolation	> 65 dB
Switching Speed	< 0.1 μs
Width (layout)	< 60 μm (limited by line length)
Current Consumption	10 mA
Supply Voltage	3.5 V

4.2.1.2 Path-select Amplifier Design

The path-select amplifier can be realized by using a differential pair. Since the values of r_π and r_o are on the order of kΩ, the input and output impedances of a differential pair are capacitive at high frequency, which meets the requirements of the path-select amplifier. However, there are two main problems with the use of a single differential pair. Firstly, the isolation between the input and output nodes is degraded by the collector-base capacitance, which can be solved by putting a cascode stage at the output. The cascode stage can further reduce the output capacitance. Secondly, the input capacitance of a differential pair is nearly twice as large as the desired value in the specification. In order not to lose too much signal power in the amplifier, the differential pair is biased close to peak f_T. The diffusion capacitance increases approximately linearly with the bias current and dominates the input capacitance close to peak f_T. The transistor input capacitance also increases due to Miller effect. Introducing an emitter follower stage at the input can mitigate the loading problem.

Figure 4.3 shows the schematic of the path-select amplifier. There is a trade-off between the gain and bandwidth when choosing the device sizes of the differential pair (Q_5 and Q_6). A longer emitter length results in smaller emitter series resistance, and thus increases the transconductance of the amplifier. However, the bandwidth may be limited at the interface between the emitter follower (Q_3 and Q_4) and the differential pair. In order to reduce the output capacitance, smaller sizes of the cascode stage (Q_7 and Q_8) are always preferable, which are limited by the electromigration design rules of the process. The device sizes and bias currents of the emitter follower (Q_3 and Q_4) are selected to ensure sufficient bandwidth. Another emitter follower stage (Q_1 and Q_2) is put at the input to further increase the input resistance and reduce the input capacitance. It must be emphasized that port impedances of the inactive amplifier are much more important to the performance of the trombone delay line. When the amplifier is inactive, the input capacitance is in linear proportion to the sizes of Q_1 and Q_2 while the input resistance is inversely proportion to these two transistors. CMOS transistors M_N and M_P are used to select the active path. Local decoupling capacitors (C_{D1}, C_{D2} and C_{D3}) provide a low-impedance AC ground. Some important performance parameters are discussed in following sections.

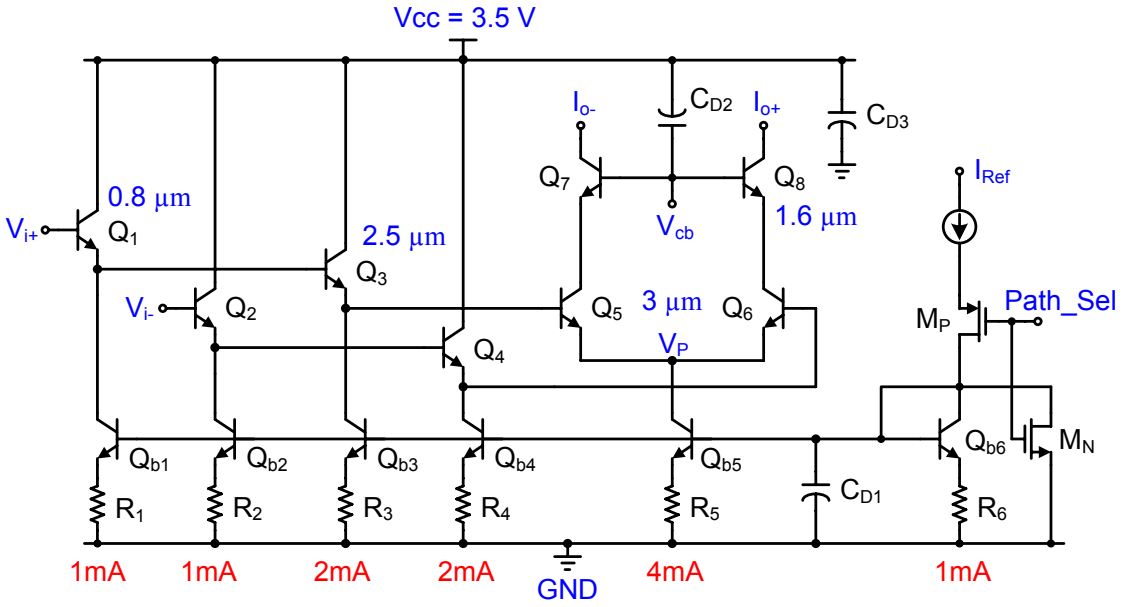


Figure 4.3: Path-select Amplifier.

4.2.1.3 Low Frequency Gain

The low frequency voltage gain of the emitter follower and current gain of the cascode stage are close to unity. Therefore, the gain of amplifier is determined by the transconductance of the differential pair and effective characteristic impedance of the differential loaded transmission line, which is given by

$$A_V = -g_m R_L = -\frac{I_c}{V_T} R_L, \tag{4.1}$$

where I_c equals one-half of the tail current of the differential pair and V_T equals 26 mV at 300 K. Assuming that the effective line impedance equals 80 Ω, the gain is (2 mA/26 mV) × 20 Ω = 1.54 = 3.74 dB. There is a large difference between the calculated and simulated results, as shown in Figure 4.4 for mainly two reasons. In the first place, the emitter series resistance degenerates the gain of the amplifier and the resulting gain is

$$A_V = -\frac{g_m}{1 + g_m R_e} R_L. \tag{4.2}$$

The emitter series resistance of a 3 µm transistor degenerates gain to –1.2 dB. Also, at high current levels, g_m approaches $I_c/2V_T$ due to high-level injection effects [4]. Biasing the

transistor near peak f_T is close to the region of high current level. Thus, the gain is further reduced to -5.1 dB. The gain from simulation is -4.5 dB, which is closer to -5.1 dB.

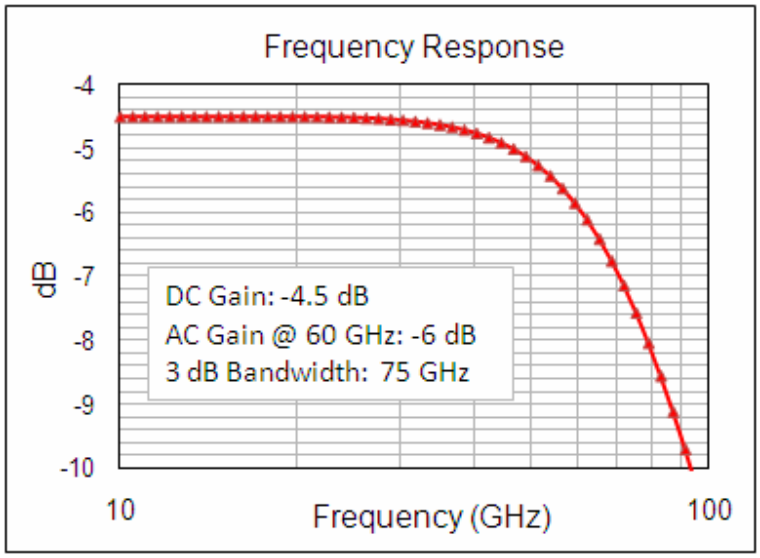
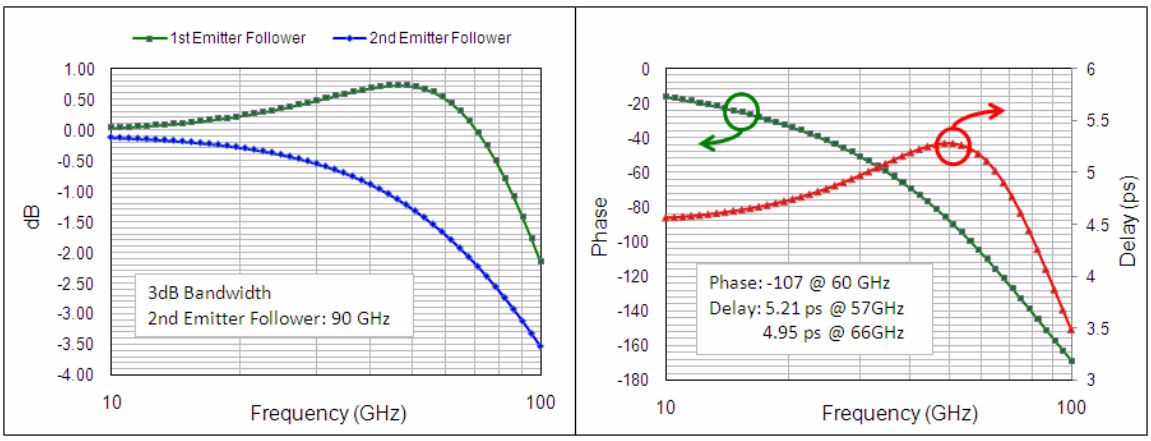


Figure 4.4: Gain & bandwidth of the path-select Amplifier.

4.2.1.4 Bandwidth and Group Delay

A wideband amplifier usually consists of several stages and each stage has a pole. In order to achieve the desired overall bandwidth, every stage must have sufficient bandwidth. The bandwidth of a wideband amplifier can be estimated by the method of open-circuit time constants [5]. The basic idea is to inspect the time constants of each node and find the effective time constants of the amplifier. This method is useful since it can also identify which node is responsible for bandwidth limitation. In our path-select amplifier, the limitation is at the input of the differential pair, mainly due to the large node capacitance. The device sizes of the differential pair (Q_5 and Q_6) and the emitter follower (Q_3 and Q_4), and the bias current of the emitter follower are optimized to maximize the gain-bandwidth product. As shown in Figure 4.4 and 4.5 (a), the bandwidths of the path-select amplifier and 2nd emitter follower stage (interface with the differential pair) are 75 and 90 GHz, respectively. Figure 4.5 (a) also illustrates that there is a peaking in the frequency response of the 1st emitter follower stage, which is due to the complex poles in the transfer function. The gain-peak property of the emitter follower at high frequency combined with frequency response of the following stages can be exploited to achieve an overall wider bandwidth [6].



(a) (b)

Figure 4.5: (a) frequency response of the emitter followers; (b) phase response and delay of the path-select amplifier.

Sufficient bandwidth is not only important to have gain flatness, but also essential to ensure flat group delay. This can be easily understood by examining the phase response of a low-pass RC network. As shown in Figure 4.6, the transit time for a signal traveling through the network is given by

$$t_d = -\frac{d\varphi}{d\omega} = \frac{d\left[\arctan(\omega RC)\right]}{d\omega} = \frac{RC}{1+\omega^2 R^2 C^2}. \tag{4.3}$$

Therefore, within the bandwidth, the group delay is defined by the RC time constant of the network while the delay reduces when the frequency is beyond the bandwidth of the network. Similarly, the group delay of an amplifier within the bandwidth is determined by the effective RC time constant, from which we can see the relationship between the frequency domain and time domain responses. As shown in Figure 4.5 (b), the group delay difference over 10 GHz (57 to 66 GHz) is less than 0.3 ps. Since the RF bandwidth of radiating signals is around 1 GHz, the delay resolution of our UWB beamforming system will not be affected by the path-select amplifier.

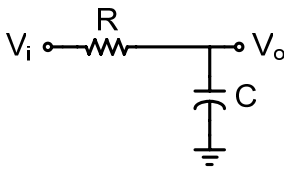
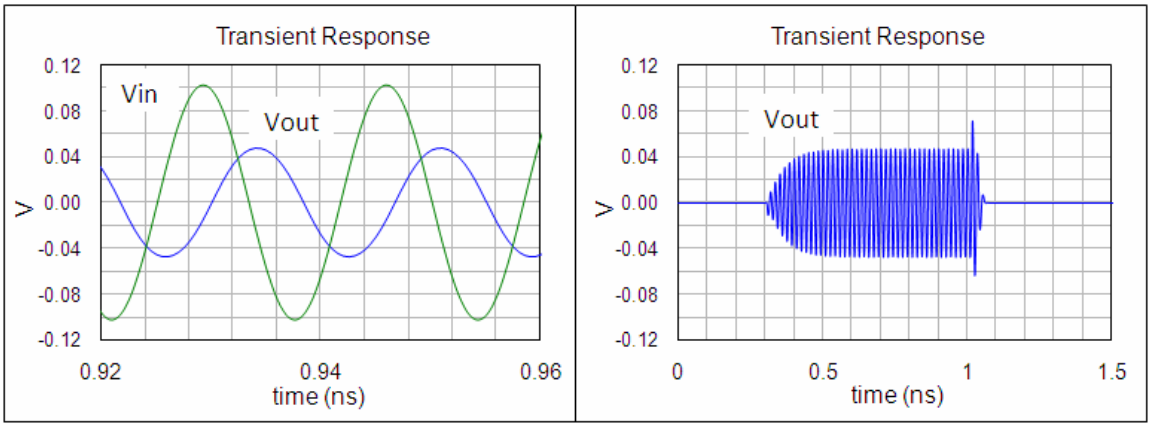


Figure 4.6: Low pass RC network.

4.2.1.5 Large-signal Performance

The large-signal behavior is important in part because it shows the operating range of the input voltage over which the circuit behaves almost linearly. Besides, the large-signal behavior of the amplifier is different from the small-signal behavior in several aspects. Firstly, when the differential input signal is small, the gain of the amplifier can be obtained by small-signal simulation. When the differential input signal level is large enough, the collector currents are independent of the input voltage because one of the transistors in the differential pair turns off and the other conducts all the tail current. The output power is then saturated. Therefore, the large-signal gain is time varying and the effective gain is "average gain". As shown in Figure 4.7 (a), if the peak-to-peak input voltage is 200 mV, the peak-to-peak output voltage is 95 mV. The corresponding large-signal gain is -6.5 dB, which is 0.5 dB smaller than the small signal gain at 60 GHz. Secondly, the large-signal bandwidth is limited by the slew rate [4] of the amplifier. Thus, there is a direct relationship between bandwidth and power consumption. Thirdly, for the common mode rejection (CMRR), if all the transistors are perfectly matched, the low-frequency CMRR is infinite in small signal case. However, in large signal case, due to the nonlinear property of the transistors, the "virtual ground" node (V_P, see Figure 4.3) of the differential pair will be modulated by the differential input signal at twice the input signal frequency. Because the output impedance of the tail current is quite low at 60 GHz (around 150 Ω), the tail current is modulated as well. Therefore, there can be common mode signals at the output even if the input signals are fully differential and all the components are perfectly matched.

The switching performance of the amplifier is also verified. As shown in Figure 4.4 (b), the amplifier can turn on and off within 1 ns, which is much better than the requirements. Benefiting from two emitter followers and one cascode stage, the isolation between the input and output of the amplifier is above 100 dB.



(a) (b)

Figure 4.7: Transient response of the path-select amplifier.

4.2.1.6 Analysis of Port Impedance

As discussed in Section 3.3, the port impedances of the path-select amplifier are of utmost importance to the performance of the beamforming transmitter. No matter whether the amplifier is active or not, the port resistances should be as high as possible while the port capacitances need to be as low as possible. Before studying the input and output impedance of the amplifier, let us consider the RC circuits of Figure 4.8. The transformation between the equivalent series and parallel RC circuits is very useful in the design of oscillators and matching networks [5], which can also simplify our analysis. The relationship between the two networks is given by

$$R_P = \left(1 + \frac{1}{\omega^2 R_S^2 C_S^2}\right) R_S = \left(Q_S^2 + 1\right) R_S \tag{4.4}$$

and

$$C_P = \frac{C_S}{1 + \omega^2 R_S^2 C_S^2} = \frac{Q_S^2}{Q_S^2 + 1} C_S, \tag{4.5}$$

where Q_S is the quality factor of the series combination, defined as $1/(R_S C_S \omega)$. If Q_S is relatively high (>5) and the bandwidth of interest is relatively narrow, the conversion changes the value of the resistance according to equation (4.4) while the value of the capacitance is nearly kept constant.

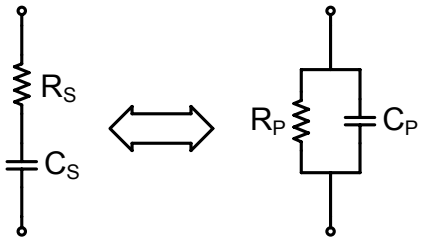


Figure 4.8: Equivalent series and parallel RC circuits.

Figure 4.9 shows the "half circuit" of the input and output stages. For simplicity, only the most relavant parasitic components are considered during the analysis. All the analysis conducted here is in single-ended mode for convenience while all the simulation results are obtained from the differential path-select amplifier.

Firstly, the input and output impedances of the amplifier in the OFF state are studied, which have more relevance to the characteristic of the loaded transmission line. As shown in Figure 4.9 (a), the equivalent series input resistance R_{Sin} is R_{b1}. In the OFF state, all bias currents in the amplifier are zero. The output node (node X1) of the input emitter follower is a high-impedance node. Therefore, the equivalent series input capacitance C_{Sin} can be expressed as

$$C_{Sin} = C_{cb1} + \frac{C_{be1}C_{X1}}{C_{be1} + C_{X1}}, \tag{4.6}$$

where $C_{X1} = C_{cb3} + C_{csb1} + C_{cbb1}$ (the series combination of C_{be3} and C_{X2} is ignored). The time constant $R_{Sin}C_{Sin}$ is almost independent of the input transistor (Q_1). Refering to equations (4.4) and (4.5), the equivalent parallel input resistance will decrease 20 dB for a tenfold increase in frequency. The equivalent parallel input capacitance equals to the equivalent series input one up to the frequency of $1/\ 2\pi R_{Sin}C_{Sin}$. These conclusions match the simulation results, as shown in Figure 4.10. In addition, equations (4.4) implies that the input resistance of the amplifer is nearly proportational to the series resistance R_b. Therefore, making the size of the input transistor (Q_1) smaller can not only reduce the input capacitance, but also increase the input resistance of the amplifier. The analysis of the output impedance of the amplifier in the OFF state is almost the same as the above process.

The simulation results of the output resistance and capacitance in OFF state are shown in Figure 4.11.

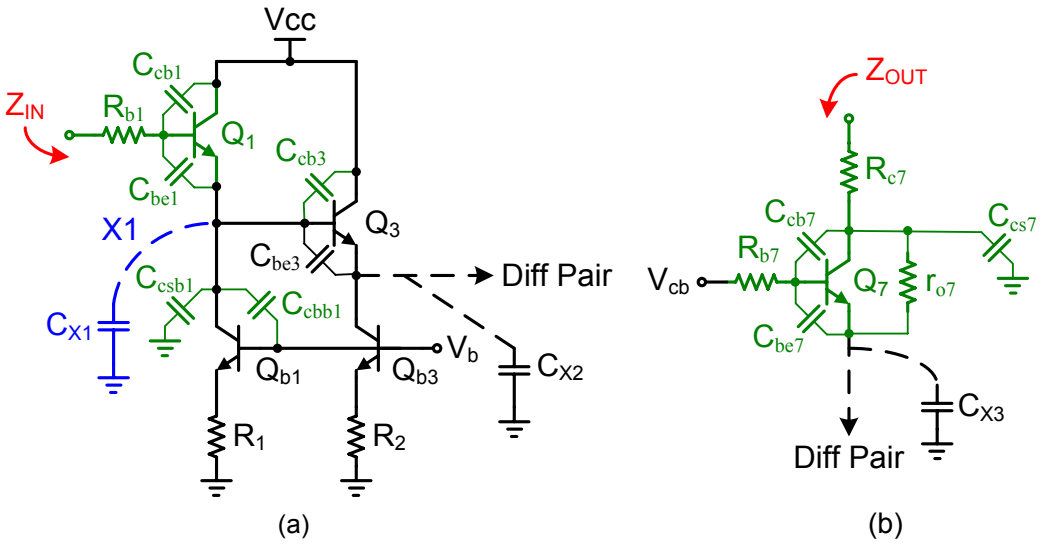
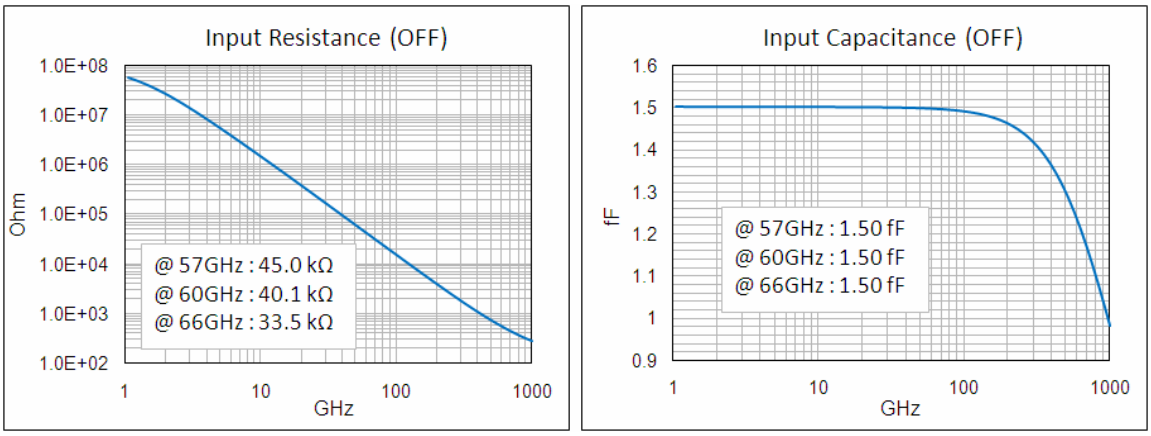
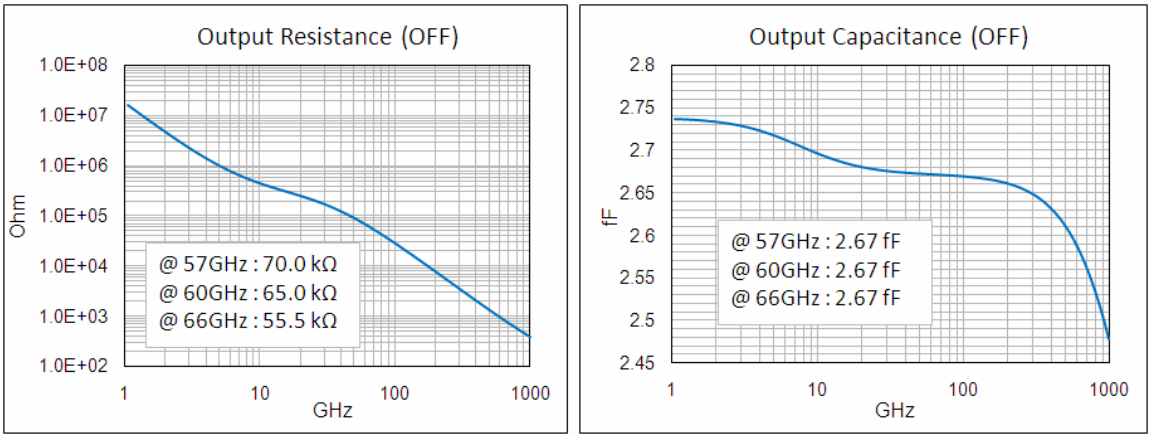


Figure 4.9: (a) input stage and (b) output stage of the differential path-select amplifier.



(a) (b)

Figure 4.10: Equivalent input parallel (a) resistance and (b) capacitance of the differential path-select amplifier in the OFF state.



(a) (b)

Figure 4.11: Equivalent output parallel (a) resistance and (b) capacitance of the differential path-select amplifier in the OFF state.

Let us now turn to the port impedance analysis in the ON state. For simplicity, only the high frequency region (> 10 GHz) is considered, and then the small signal input resistance r_π and output resistance r_o of the device are ignored. The input impedance can be represented by Figure 4.12. The capacitance C'_{X1} at the emitter of Q_1 presents itself as a series combination of a negative resistance R_β and a capacitance C'_{X1} in the base branch due to the β–transform [1]. Therefore, the equivalent series input resistance can be zero at a certain frequency. This resonant frequency can be approximately expressed as

$$f_o = \sqrt{\frac{f_T}{2\pi R_{b1} C'_{X1}}} . \tag{4.7}$$

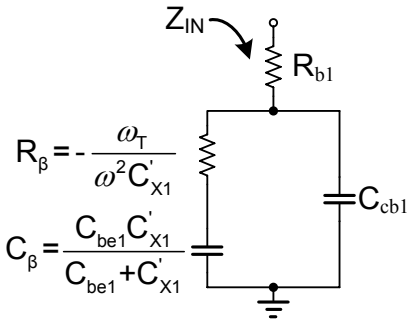
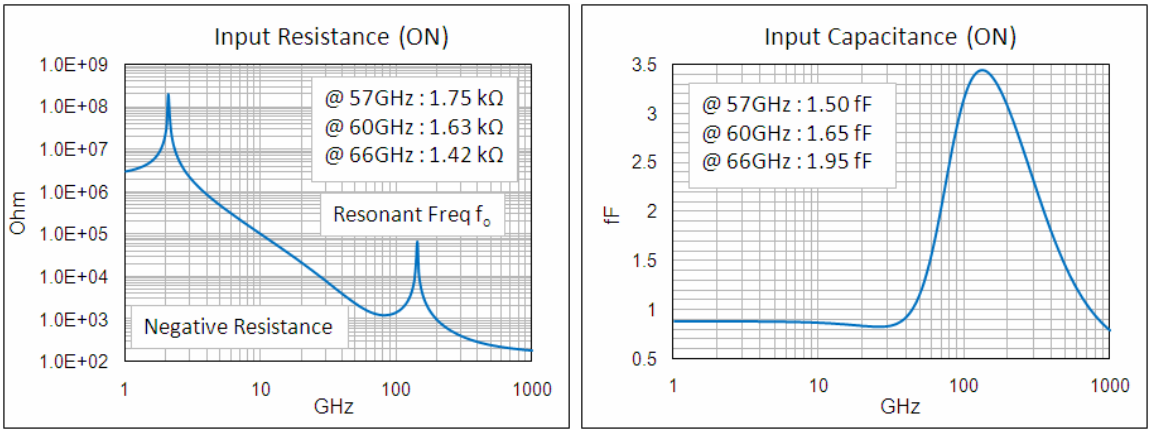


Figure 4.12: Input impedance of the amplifier in the ON state.

When the frequency is well below f_o, R_β dominates the R_β C_β network. The equivalent series input resistance and capacitance approximately equal R_β and C_{cb1}, respectively. At the

resonant frequency, the equivalent series input resistance goes to zero (the equivalent parallel input resistance becomes infinite) and the equivalent series input capacitance equals $C_{cb1} + C_{\beta}$. Figure 4.13 shows the simulation results, conforming to our analysis. Note that the input resistance is only 1.6 kΩ in the ON state, which is comparable with the capacitive reactance (around 500 Ω) of a 60 μm loaded transmission line. This will affect the characteristic impledance of the loaded transmission line. Consequently, there could be discontinuities at the input of the ON-state amplifier, which may deteriorate the delay resolution.



(a) (b)

Figure 4.13: Equivalent input parallel (a) resistance and (b) capacitance of the differential path-select amplifier in the ON state.

It is not straightforward to analyze the output resistance of the path-select amplifier. Small signal analysis is performed here to obtain the result. Figure 4.14 (a) shows the small signal model of the output cascode stage. In order to simplify the analysis, the impedance in the base branch can be represented by a combination of C_{X4}, R_{X4} and R_{b7}. Since R_{b7} is small and the reactance of C_{X4} is close to 500 Ω at 60 GHz, R_{b7} dominates this parallel RC network and C_{X4} and R_{X4} are neglected in the following analysis. The impedance at the emitter are mainly capacitive, represented by C_{X5}. C_{X5} approximately equals to the sum of C_{X3} and C_{be7}. Therefore, the small signal node equations are given by

$$I_X = \frac{V_b}{R_{b7}} + j\omega C_{X5} V_e , \tag{4.8}$$

$$j\omega C_{X5}V_e = g_m\left(V_b - V_e\right) \tag{4.9}$$

and

$$\frac{V_b}{R_{b7}} = j\omega C_{cb7}\left(V_X - V_b\right). \tag{4.10}$$

Solving these three equations, the output impedance is given by

$$Z_{OUT} = \frac{V_X}{I_X} = \frac{g_m R_{b7} + \dfrac{C_{X5}}{C_{cb7}} + \dfrac{g_m}{j\omega C_{cb7}} + j\omega C_{X5}R_{b7}}{g_m + j\omega C_{X5}\left(1 + g_m R_{b7}\right)} \tag{4.11}$$

$$= \frac{g_m^2 R_{b7}\left(1 - \dfrac{C_{X5}}{C_{cb7}}\right) + \omega^2 C_{X5}^2 R_{b7}\left(1 + g_m R_{b7}\right) + \dfrac{1}{j\omega}\left\{\dfrac{g_m^2}{C_{cb7}} + \omega^2 C_{X5}\left[\left(1 + g_m R_{b7}\right)\dfrac{C_{X5}}{C_{cb7}} + g_m^2 R_{b7}^2\right]\right\}}{g_m^2 + \omega^2 C_{X5}^2\left(1 + g_m R_{b7}\right)^2} \tag{4.12}$$

$$\approx R_{b7}\left(1 - \frac{C_{X5}}{C_{cb7}}\right) + \frac{1}{j\omega C_{cb7}} (\text{ignore all } \omega^2 \text{ terms}). \tag{4.13}$$

Equation (4.13) shows the output resistance can be negative if the value of C_{X5} is larger than the value of C_{cb7}. Figure 4.15 verifies our conclusions and shows peakings in the frequency response. This negative resistance can be easily canceled if a small resistor is connected to the collector of the cascode transistor. The output capacitances have almost the same value and frequency response in both states.

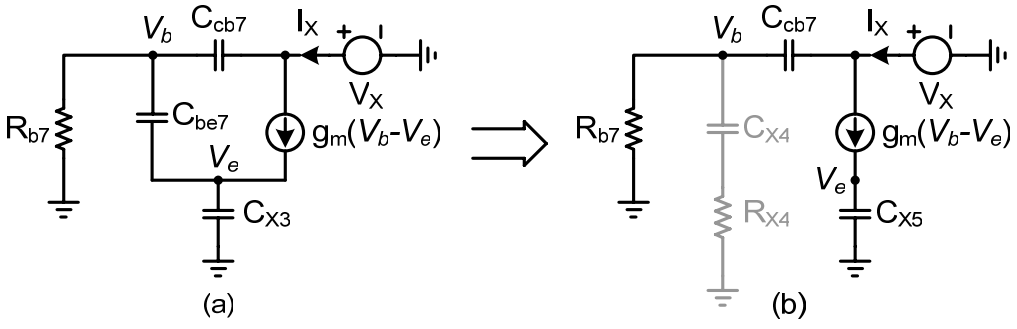
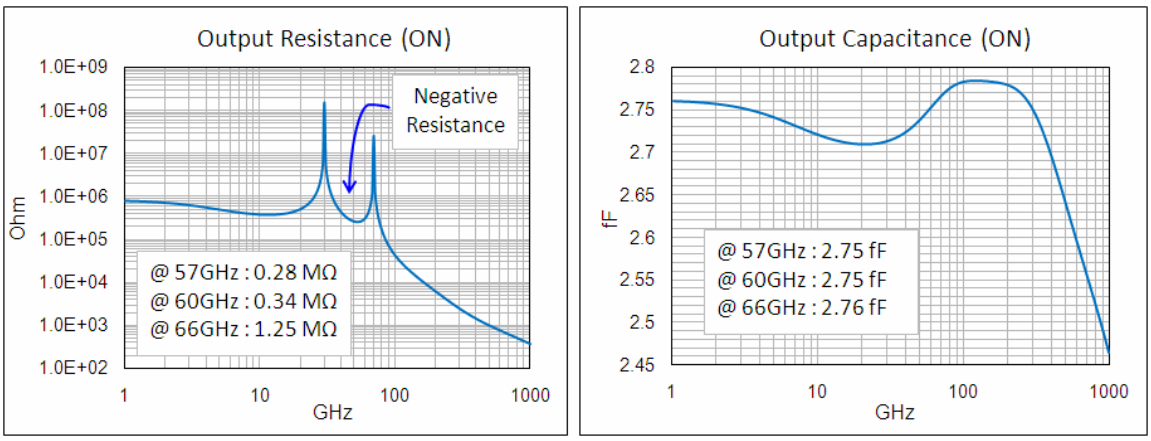


Figure 4.14: (a) small signal model to calculate the output impedance in ON state; (b) simplified model.



(a) (b)

Figure 4.15: Equivalent output parallel (a) resistance and (b) capacitance of the differential path-select amplifier in OFF state.

4.2.2 Local Decoder

The local decoder is used to determine which path-select amplifier is active and thus the length of the signal path can be manipulated. All the decoding output signals are active low. Therefore, the decoder is placed near the path-select amplifier in order to have the same ground level. As shown in Figure 4.16, the local decoder is put between the left delay path and right delay path (also see Figure 3.12). In order to reduce power consumption, four path-select amplifiers share one decoder. The ratio between the PMOS and NMOS transistors in the INV and NAND gates are chosen so that the threshold voltage of the gates are set midway between the supply and ground. In addition, sizes of all the transistors are optimized to ensure that all gates have enough strength to drive the following stages [7].

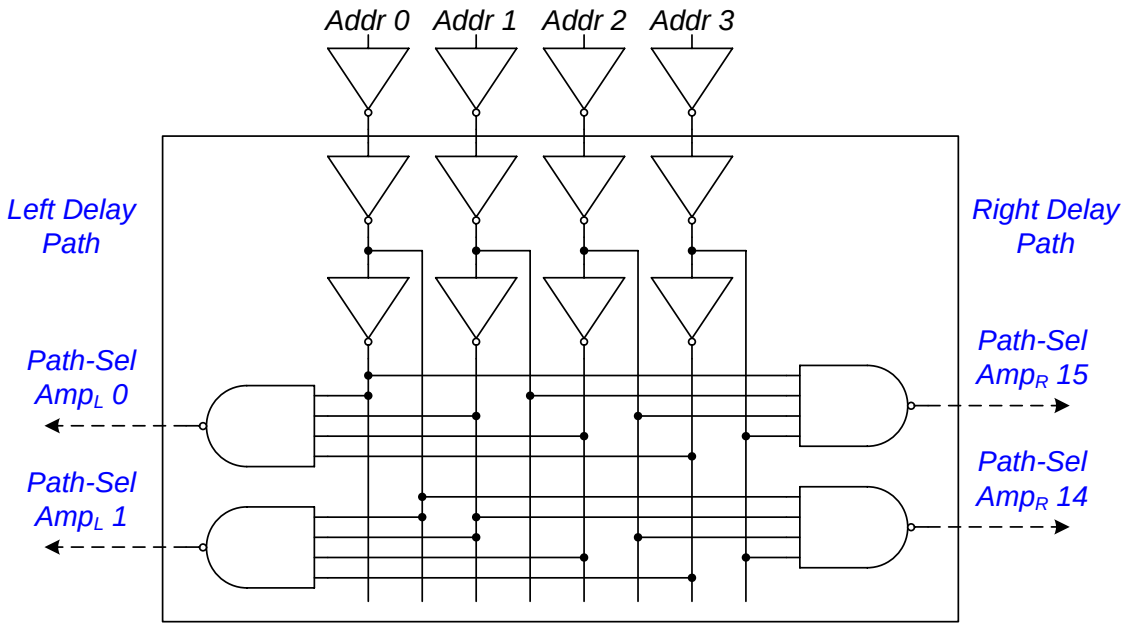


Figure 4.16: Local decoder.

4.2.3 Differential Transmission Line[1]

In order to predict the final performance of the beamformer, it is essential to analyze and design the transmission lines. As shown in Figure 4.17, the differential coplanar waveguide structure with ground shielding is proposed for in this design. The coplanar waveguide is implemented in top-level metal. The width of the signal lines is 4 μm and the spacing between two signal lines is 10 μm, so that higher differential characteristic impedance can be expected. The ground shielding is implemented in metal 2 in order to minimize the ground path losses due to capacitive coupling to the substrate, which is often the dominant source of high frequency loss. Control signals (e.g., decoding signals) can still run in the lowest metal layer (metal 1) with negligible impact on the electrical characteristics of the transmission line. Therefore, the floorplan of the beamformer can be simplified.

For the trombone delay line, the proposed transmission line implementation has the following merits [8]: Firstly, the coplanar waveguide has low high-frequency loss. This is because it has a nearby low-impedance return path and the substrate is also shielded by

[1] The differential transmission line is designed by Dr. Hugo Veenstra.

metal 2. Secondly, this configuration has excellent shielding from the environments so that other lines or circuits can be placed nearby. Thus, chip area can be saved. Thirdly, since the coplanar waveguide is shielded from the substrate, the potential slow-wave effects are avoided. Therefore, the transmission line can have well-defined and controlled characteristic impedance and delay over a wide frequency range.

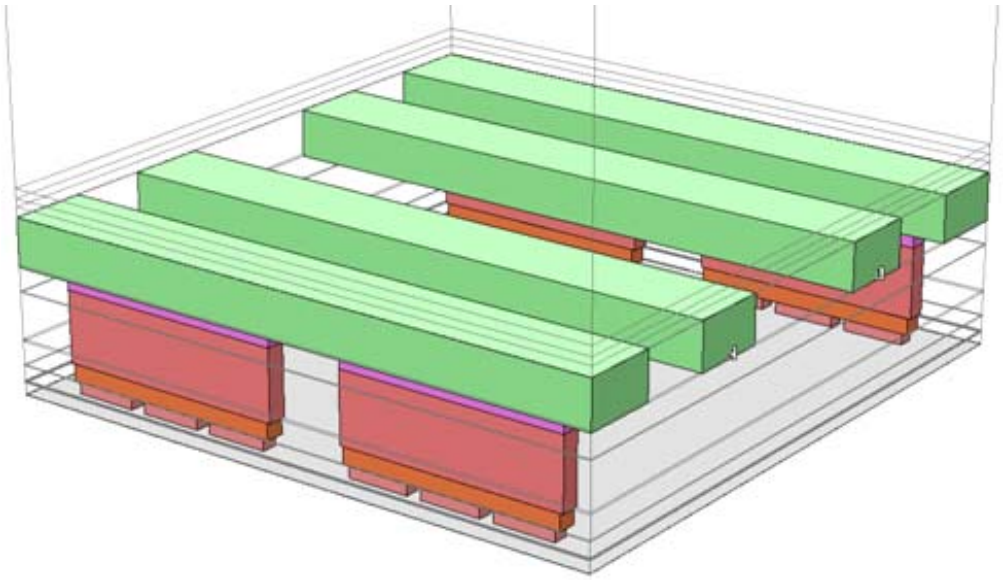


Figure 4.17: GSSG differential transmission line (Courtesy H. Veenstra, Philips Research).

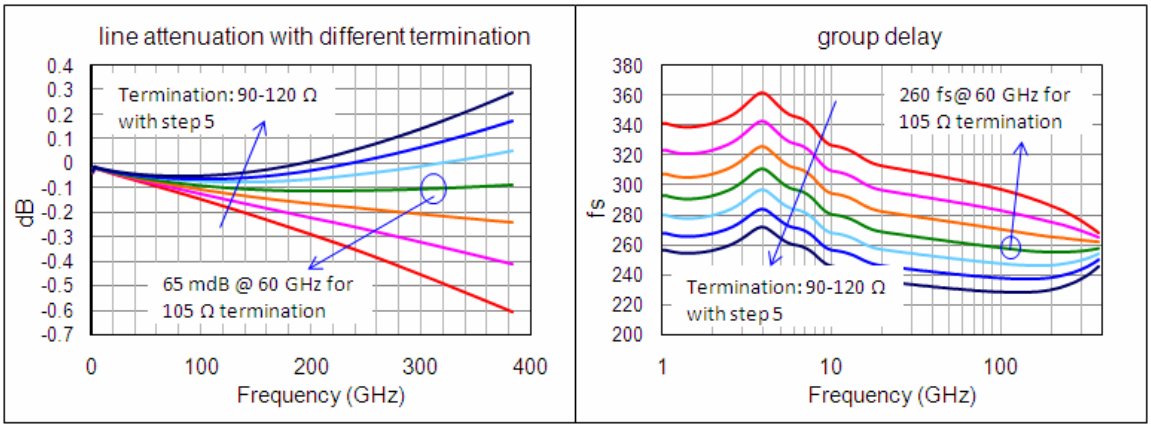
The differential coplanar waveguide is designed and simulated with EM-Sonnet [9], which is capable of 3D EM analysis for planar structures. A 40 µm differential coplanar waveguide is simulated and corresponding results are listed in Table 4.1. In the final design, the co-planar as grounds will conduct the power supply. Therefore, the two ac ground planes are locally connected through vias and metal 1 to ensure that they operate at the same voltage level. In addition, local decoupling capacitors are placed between metal 2 and 6 to ensure a good ac ground.

The S-parameters of the 40 µm line section were obtained from EM-Sonnet and further simulated with the Cadence Spectre simulator. The characteristics of the transmission lines

are shown in Figure 4.18 and 4.19. From Figure 4.18, the differential-mode characteristic impedance is approximately 105 Ω and the attenuation is around 1.6 dB/mm at 60 GHz.

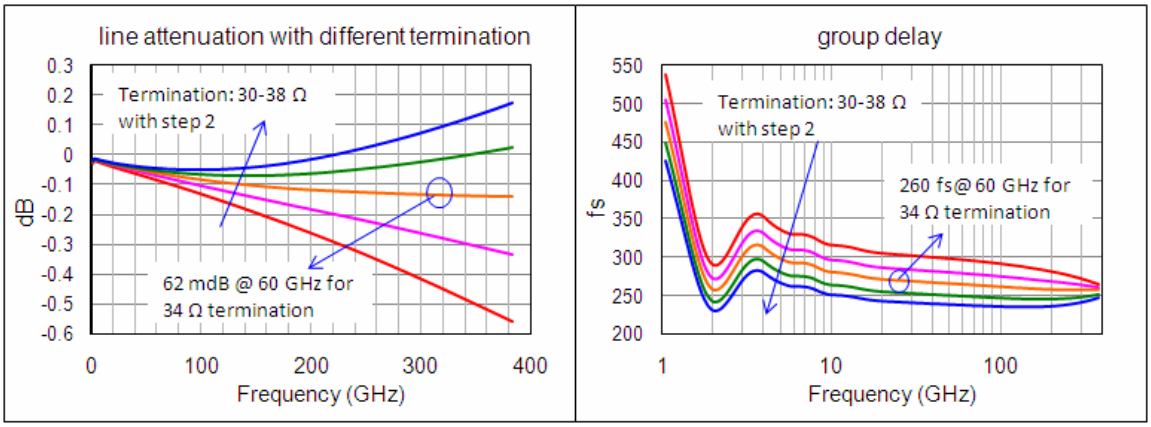
Table 4.2: Differential coplanar waveguide results @ 60 GHz.

Differential mode line impedance (Z_{odm})	105 Ω
Differential mode group delay (t_{odm})	6.6 ps/mm
Common mode line impedance (Z_{ocm})	34 Ω
Common mode group delay (t_{ocm})	6.6 ps/mm
Attenuation (α)	1.5 dB/mm
Relative dielectric constants (ε_r)	3.92



(a) (b)

Figure 4.18: (a) attenuation and (b) group delay for a 40 μm transmission line in differential mode (the termination changes from 90 to 120 Ω with 5 Ω steps).



(a) (b)

Figure 4.19: (a) attenuation and (b) group delay for a 40 μm transmission line in common mode (the termination changes from 30 to 38 Ω with 5 Ω steps).

Although the S-parameters model can also be used to verify the performance of the transmission line, it is not scalable. A lumped-element circuit model provides more flexibility, as shown in Figure 4.20. L (in H/m), C_c (in F/m), C_g (in F/m) and R (in Ω/m) are distributed line parameters, and K is the inductive coupling factor [10]. This model is scalable with the length of the transmission line l. One of the problems of this model is that all the losses are subject to the series resistance R, which will affect the characteristic impedance of the transmission line. However, the model can still be used with sufficient accuracy at 60 GHz since the reactance of the lumped inductor is much higher than the series resistance in the model. The relationship between the values of these lumped elements and the characteristic parameters of the transmission line can be expressed by following equations:

$$L = l \times \frac{\sqrt{\varepsilon_r}}{c} \times \left(Z_{ocm} + 0.25 Z_{odm} \right), \tag{4.14}$$

$$C_c = l \times \frac{\sqrt{\varepsilon_r}}{c} \times \left(\frac{1}{Z_{odm}} - \frac{0.25}{Z_{ocm}} \right), \tag{4.15}$$

$$C_g = l \times \frac{\sqrt{\varepsilon_r}}{2c} \times \frac{1}{Z_{ocm}}, \tag{4.16}$$

$$R = l \times \frac{Z_{od}\left(1-10^{\alpha/20}\right)}{2\times 10^{\alpha/20}}, \tag{4.17}$$

and

$$K = \frac{Z_{ocm} - 0.25Z_{odm}}{Z_{ocm} + 0.25Z_{odm}}. \tag{4.18}$$

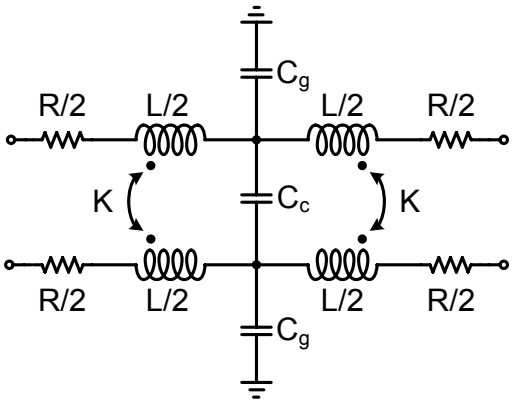


Figure 4.20: Lumped-element circuit model for a transmission line.

4.2.4 Characteristics of the Loaded Transmission Line

The main parts of the trombone delay line are composed of the path-select amplifiers and the differential transmission lines. Both have been discussed in the previous sections. Figure 4.21 shows one "delay section" in the trombone delay line. Each section consists of four 30 μm transmission line models, one amplifier and some parasitic capacitors. The parasitic capacitances come from the metal interconnects. The area capacitances of these parasitics can be estimated. However, it is not straightforward to obtain the fringe contribution of these parasitics. Some formulas can be used to calculate fringe capacitances for simple structures [5], but they are not accurate enough to be applied here. Since interconnects between the transmission line and amplifier run in the thick top metals (metal 5 and 6), the fringe components are relatively large. The parasitic extraction of the path-select amplifier was performed. As mentioned early, the layout still needs to be improved. In the following simulation, three 1 fF lumped capacitors (C_d and C_g) are added to the input and output of the amplifier.

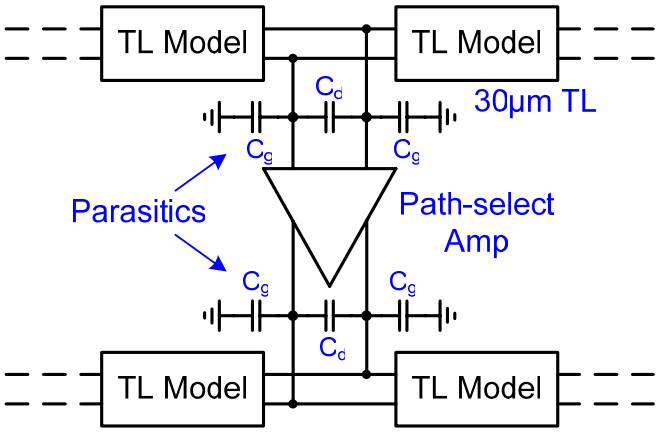
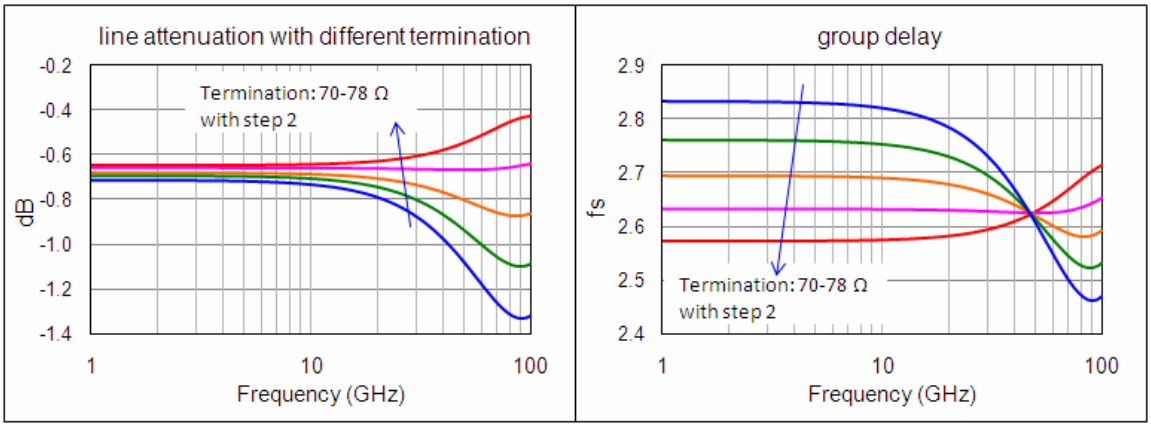
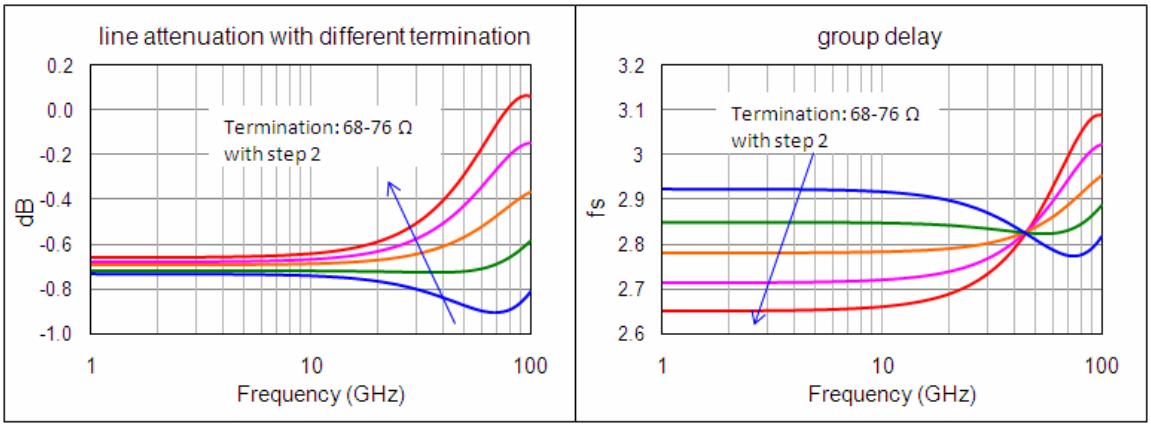


Figure 4.21: One delay section of loaded TL.

A loaded transmission line composed of five "delay section" is used to study the characteristics of the loaded transmission line, the length of which is around quarter wavelength of this structure at 60 GHz. Figure 4.22 (a-b) shows the attenuation and group delay of the loaded transmission line at the input of the amplifier in the OFF state while Figure 4.22 (c-d) shows the corresponding values at the output of the amplifier. The line impedance is reduced due to the capacitive loading and the attenuation is increased because of the port resistance of the amplifier. As shown in Figure 4.22, the behavior of the loaded transmission line is different from the behavior of the normal transmission line. This is because the input and output resistances of the amplifier decrease at the rate of 20 dB/dec with frequency. Therefore, the line impedance decreases accordingly and becomes unmatched with the fixed terminations at high frequency (~100 GHz). The characteristic impedance and delay of the loaded transmission line can also be obtained from equation (3.21) and (3.22). Both simulation and calculation results are listed in Table 4.2. When simulating the characteristics of the loaded line in the ON state, all five amplifiers are switched on. There are differences between the simulated and calculated line impedance values. One of the reasons is that the input and output resistances of the amplifier are ignored during the calculation. The attenuation of the on-state, input loaded line is quite low. This is because a negative resistance feed energy into the line instead of consuming energy.



(a) (b)



(c) (d)

Figure 4.22: (a, c) attenuation and (b, d) group delay for the loaded TL section at input and output of the amplifier in OFF state.

Table 4.3: Characteristics of the loaded transmission line section @ 60 GHz.

	Z_{od} (Ω, Cal)	Z_{od} (Ω, Sim)	t_d (ps/mm, Sim)	α (dB/mm, Sim)
Input (OFF)	78	76	7.88	2.0
Output (OFF)	73	70	8.48	2.1
Input (ON)	77	74	7.20	0.4
Output (ON)	72	70	8.66	1.8

4.2.5 Trombone Delay Line Simulation Results

The entire trombone delay line is simulated with different settings. The path-select amplifier along the delay line is enabled one by one and the corresponding group delays are shown in Figure 4.23. The delay resolution is roughly 1.1 ps. The variation or ripple in the group delays increases at higher frequency. This is attributed to the port resistances of the amplifiers, which decrease dramatically at high frequency. The line impedance therefore decreases with frequency. Hence, greater mismatch exists between the loaded line impedance and the termination. Another reason is that the load of the path-select amplifier changes with different delay settings. This may also introduce extra group delay variation.

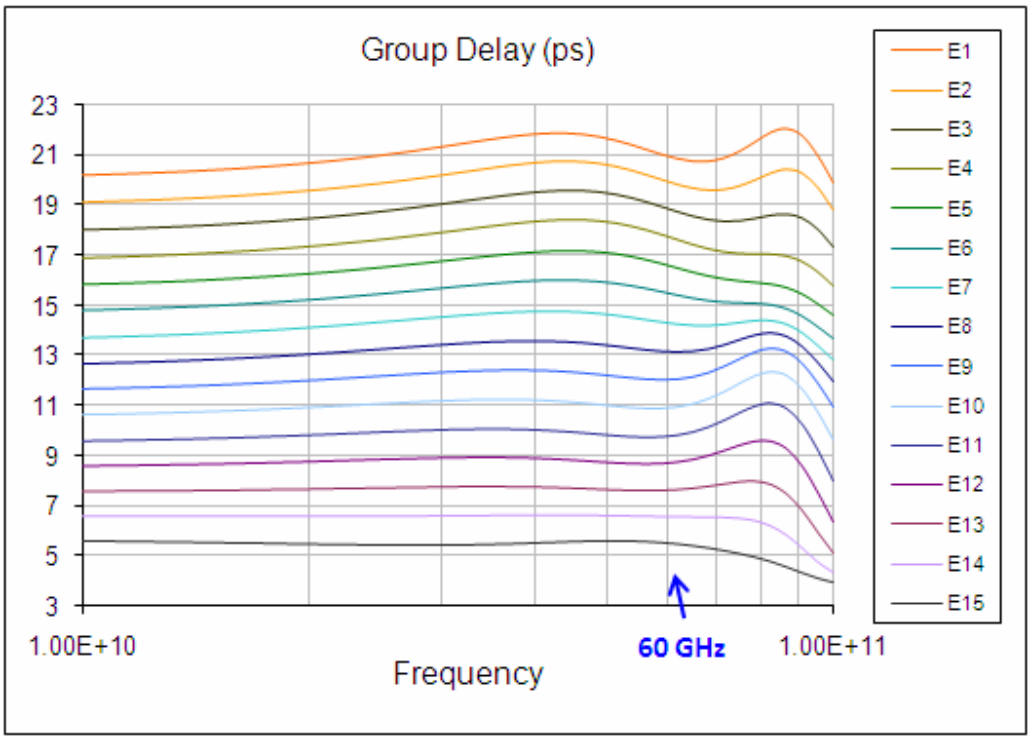
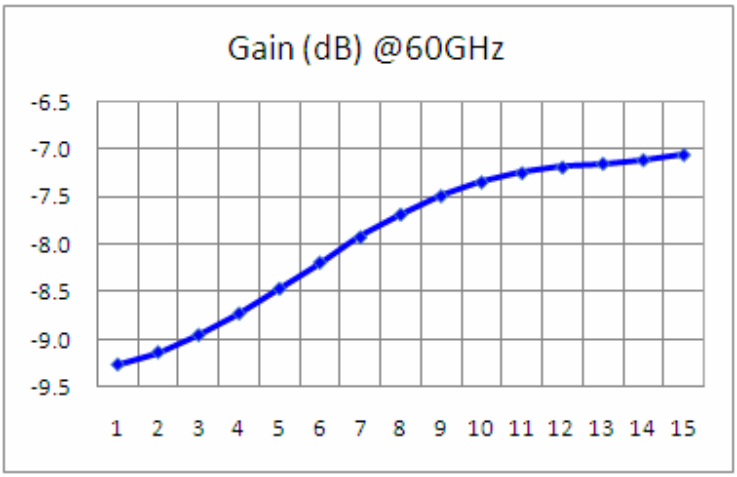


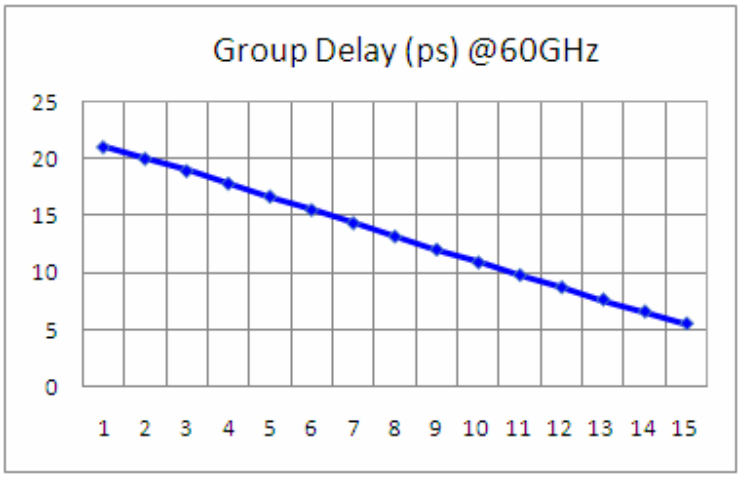
Figure 4.23: Group delay of the trombone delay line with different delay settings.

The performance of the trombone delay line at 60 GHz is illustrated in Figure 4.24. Because of the relatively high losses of the loaded transmission line, the gain varies about 2 dB between the shortest path and the longest path. This implies that the formed beam may not have the desired radiation pattern when the incident angle is large. There are two solutions. The first one is to implement a variable gain power amplifier to compensate for

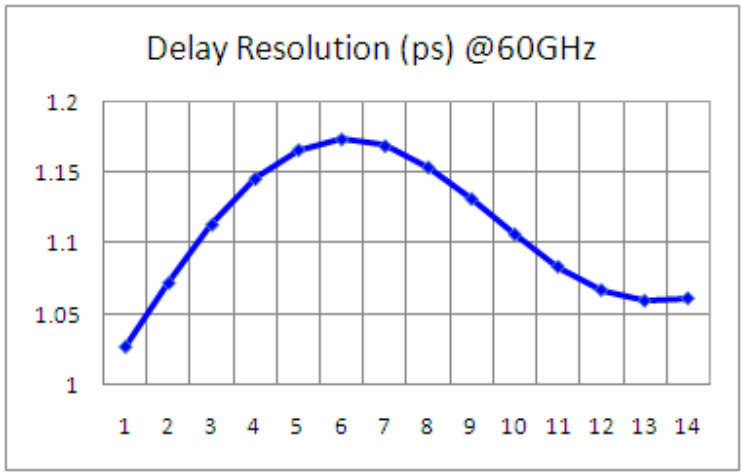
the different losses associated with the different signal paths. The gain resolution depends on the number of settings realized in the power amplifier. However, it is usually not easy to linearly program the gain of a power amplifier. A more practical way is to make the path-select amplifiers in the trombone delay line with different gains. The amplifier in the shorter path has a smaller gain while the amplifier in the longer path would have greater gain. Since the gain of the path-select amplifier mainly depends on the differential pair, it is possible to realize path-select amplifiers with different gains and identical port impedances. The delay range for the trombone line is around 16 ps. From Figure 4.24 (c), the delay resolution is approximately 1.1 ps with a deviation less than 0.1 ps for different delay settings.



(a)



(b)



(c)

Figure 4.24: (a) gain, (b) group delay and (c) delay resolution of the loaded TL @ 60 GHz.

4.2.6 Layout of Trombone Delay Line

The trombone delay line is composed of GSSG differential transmission lines and 15 path-select amplifiers. Figure 4.25 shows the layout of the trombone delay line, the area of which is 900×145 μm^2. In order to preserve the performance of the trombone delay line, the layout of path-select amplifier is crucial. As shown in Figure 4.26, symmetry is carefully considered in the differential signal paths to reduce the common mode noise and offset. Input and output stages are placed closest to the transmission lines at the input and output, respectively, so that the parasitic capacitances at the input and output can be reduced. The differential pair and the cascode stage are placed relatively far away from each other, but the parasitic capacitances at their interface have negligible impact on the output capacitance of the amplifier. Power and bias signals are routed using maximally capacitive, minimally inductive and resistive metal lines. In addition, local decoupling capacitors are placed to provide a low-impedance AC ground. The area of the path-select amplifier is 60×65 μm^2.

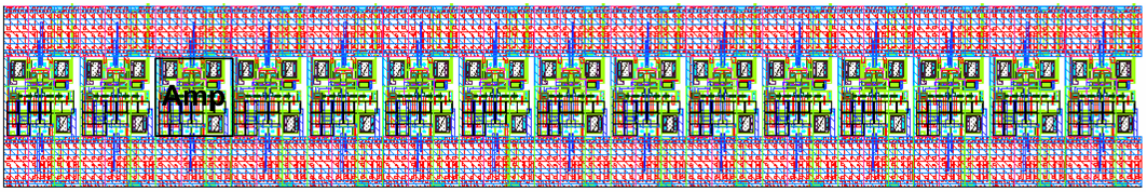


Figure 4.25: Layout of trombone delay line.

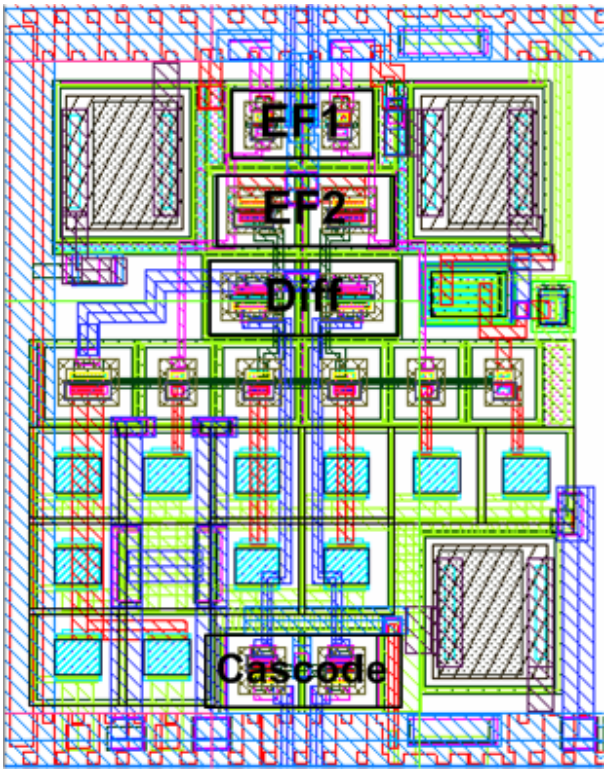


Figure 4.26: Layout of path-select amplifier

4.3 Single-ended to Differential Converter and Power Splitter

Although the VCO can provide a differential output signal, it is not implemented in this chip. A single-ended to differential converter simplifies the interfacing, and a balun is not needed to drive the external reference input signal. As shown in Figure 4.27, the input is AC coupled and provides 50 Ω input matching. The input resistance of the converter is the parallel combination of the resistances looking into the upper path (R_2, Q_2) and downer path (R_1, Q_1), which is given by

$$R_{in} = \left(\frac{1}{g_{m1}} + R_1\right) // \left(\frac{1}{g_{m2}} + R_2\right), \tag{4.19}$$

where g_{m1} and g_{m2} are the transconductance of $Q_1$and Q_2, respectively. This input configuration has the advantage of wideband input matching. Since the signals will see different parasitics in the upper path (cascode) and downer path (current mirror), R_1 is made a bit smaller than R_2 to obtain a good balancing of the differential output signal. In order to have sufficient bandwidth at the output of the converter, the emitter follower stages are inserted to make the capacitive loading smaller. The signal power is split at the input of the cascode stage and the split signals are fed into the left and right delay paths directly. The cascode stages may see different load impedances in the left and right delay paths, especially when large mismatch exists. However, since the transmission line impedances are relatively low compared with the output impedances of the cascode stages, the input impedances of the cascode stages will not be affected by the loads. Therefore, the signal power can be equally split into the left and right paths. This shielding property also ensures a good isolation between the left and right delay paths, which helps to reduce the group delay variations. Besides, due to the common mode rejection property of the differential pair, more balancing signals can be expected at the output of the differential pair. In order to provide gain at 60 GHz, 27 mA currents is required by this circuit.

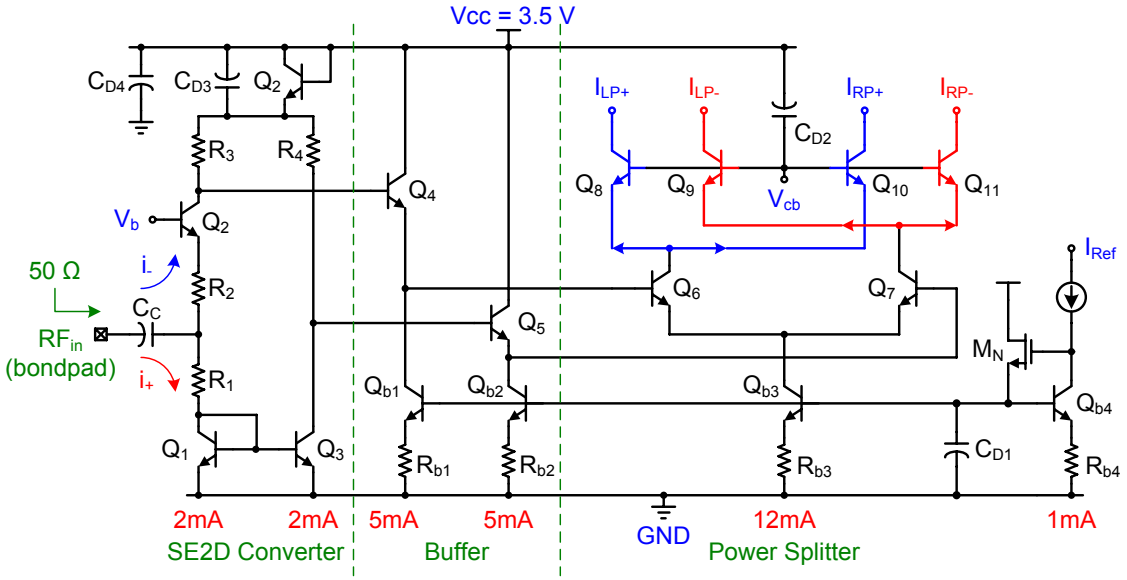


Figure 4.27: Single-ended to differential converter and power splitter.

Small signal simulation results are shown in Figure 4.28. The total small signal DC gain of single-ended to differential amplifier and the power splitter is -0.6 dB while -3 dB bandwidth is roughly 65 GHz. The differences between the two outputs (I_{LP+} and I_{LP-}) are illustrated in Figure 4.28 (b–d). Within the bandwidth, the phase, gain and group delay differences are less than 1^{o}, 0.1 dB and 100 fs, respectively. It indicates that nearly perfect balanced differential outputs have been achieved. As shown in Figure 4.29 (a), the input return loss is below -15 dB up to 80 GHz, which indicates the input matching is acceptable over a wide frequency range. Figure 4.29 (b) shows the time domain output waveforms at the output of the power splitter.

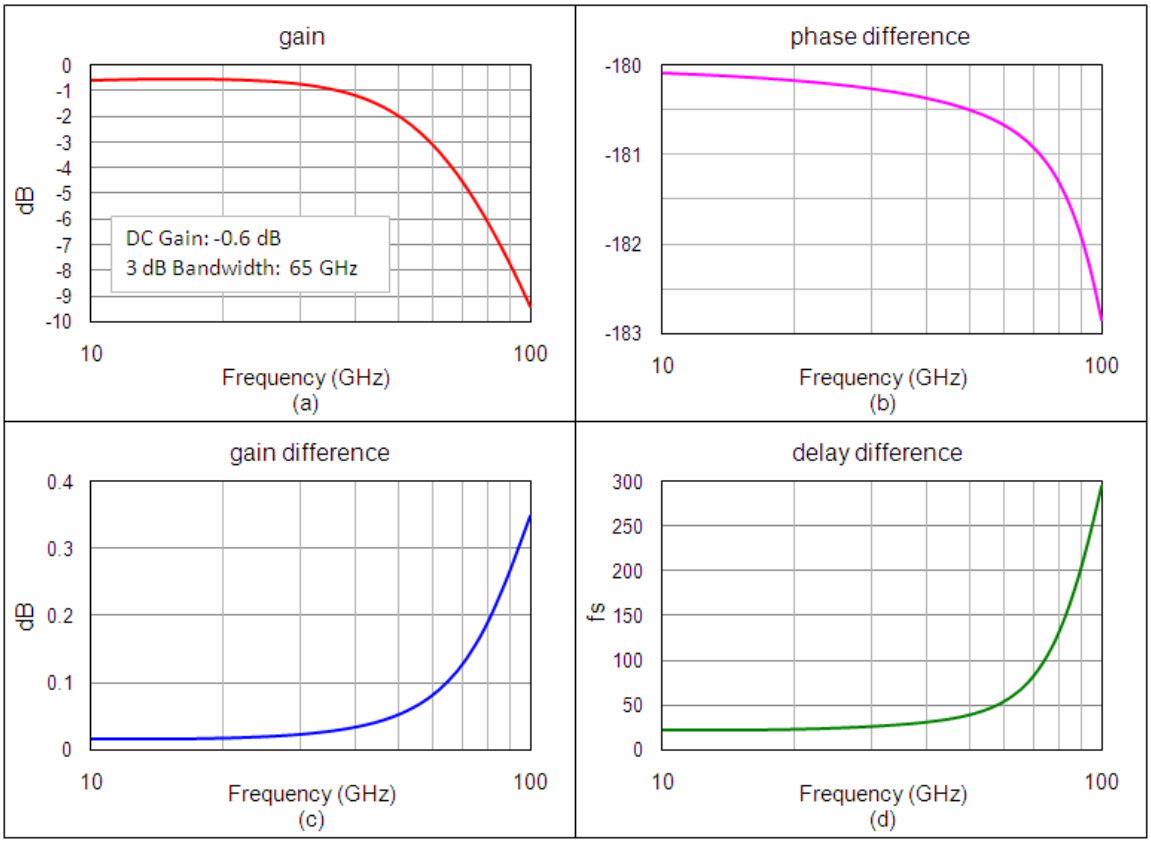


Figure 4.28: (a) frequency response of the entire amplifier, (b)-(d) phase, gain and group delay difference between the positive and negative signals at the output of power splitter.

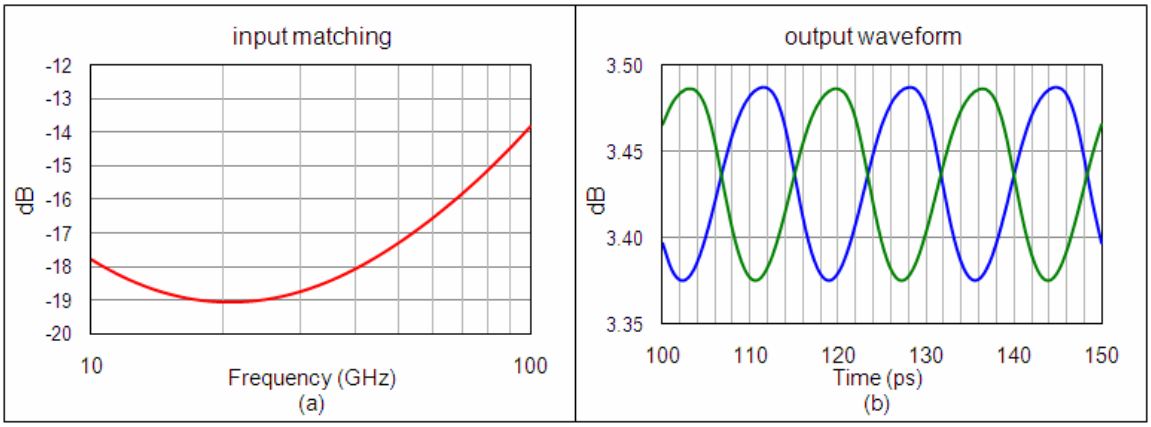


Figure 4.29: (a) input matching, (b) output waveform at the output of the power splitter.

4.4 Bias Circuits

A supply and temperature insensitive bias circuit is essential to ensure reliable operations of the chip under different conditions. The supply voltage across the chip may not be constant, especially at microwave frequencies [7]. The bias current delivered to the circuit blocks must be immune to this power supply variations. A PTAT (proportional to absolute temperature) current source is necessary to make the transconductance of a transistor insensitive to temperature. Then, the small signal gain of the transistor can be stable over temperature variations. However, a temperature insensitive reference current is preferred in order to make the large-signal gain constant and have the same saturated power. Large signal operation has more relevance to our beamforming transmitter. Therefore, a supply and temperature insensitive bias circuit will be implemented. It needs to be mentioned that, for the same contact numbers or metal width, less current can be conducted at higher temperature. The reliability design rules are met at 125°C in our design.

To stabilize the reference current over supply voltage variations, a circuit topology like "peaking current source" [11] is used. As shown in Figure 4.30, V_{pk} can be expressed by

$$V_{pk} = V_{2D} - I_D R_2 \tag{4.20}$$

$$= \frac{2kT}{q} \ln\left(\frac{I_D}{I_S}\right) - I_D R_2, \tag{4.21}$$

where I_D is the bias current of Q_1 and Q_2. Take the derivative of V_{pk} over I_D, we have

$$\frac{dV_{pk}}{dI_D} = \frac{2kT}{qI_D} - R_2 . \tag{4.22}$$

The above equation indicates that if $2kT/q$ equals $I_D R_2$, V_{pk} won't vary with I_D. It also implies that V_{pk} is insensitive to the supply voltage. Therefore, if transistors Q_1 and Q_2 are biased at $I_D=2kT/qR_2$, a variation in the supply voltage should not be transferred to V_{pk}. The design process can be simply conducted as follows: first, choose a proper biasing current I_D for Q_1 and Q_2; then, the resistor R_2 is optimized to satisfy the stabilization condition analyzed above. Because of the parasitics of the transistors, the exact value of R_2 needs to be further verified by simulation. The current source on top of V_{D2} is implemented by R_1. This resistor does not need to be accurate since small changes in R_1 can be regarded as small changes in the biasing current. If V_{pk} is used to bias a current source, the resulting reference current should also insensitive to the supply voltage theoretically.

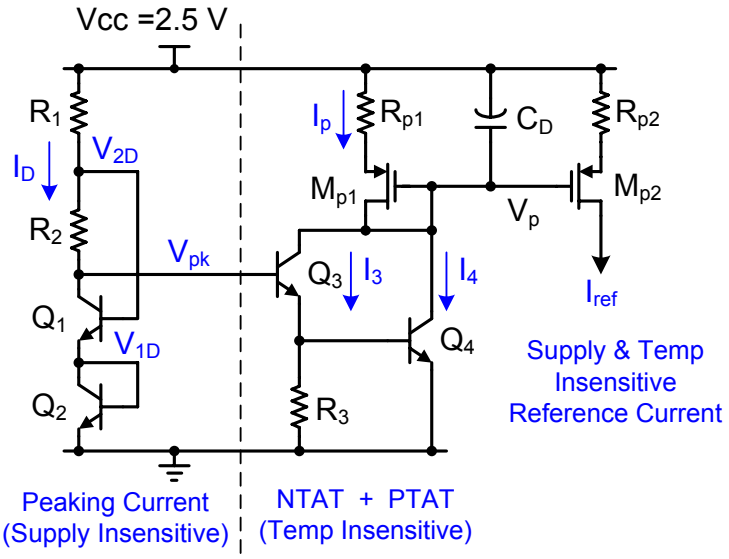
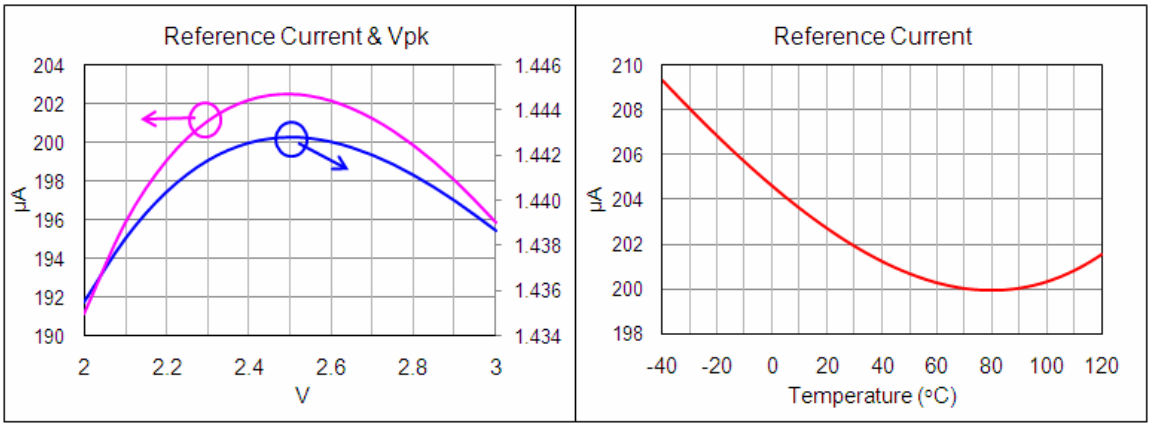


Figure 4.30: Supply and temperature insensitive reference current source.

The temperature dependence of the reference current source is now studied. The diode voltage dependence over temperature of a SiGe HBT in the BiCMOS technology is 0.9625 mV/K, which is smaller than that of a silicon bipolar transistor. The resistors used in this circuit are P+ unsalicided poly resistor with a temperature dependence of -103 ppm/K, which has negligible impact on the overall performance. The simulated V_{pk} over temperature is 2.1563 mV/K. It is approximately twice as large as the value of a single

diode. Due to the exponential relationship between the base-emitter voltage and the collector current of a bipolar transistor while a linear voltage-current relationship in a resistor, most voltage variation of V_{pk} will drop on R_3. Therefore, I_3 has a NTAT (negative to absolute temperature) current behavior. Because of the same reason, I_D is mirrored to I_4 and thus I_4 has a PTAT current behavior. The ratio between the sizes of Q2 and Q3 is optimized and a desired temperature insensitive reference current is achieved.

Figure 4.31 shows the reference current only has 5 percent variations when the supply voltage varies from 2 to 3 V or the temperature changes between -40 and 120 ^{o}C.



(a) (b)

Figure 4.31: (a) reference current & V_{pk} versus supply voltage at 60^{o}C, (b) reference current versus temperature.

4.5 Conclusion

In this chapter, the true time delay elements were realized by a trombone line structure where the length of the delay path was manipulated. The simulated delay range is 16 ps and the delay resolution is around 1.1 ps. The design methodology of the trombone delay line is to keep the line property as constant as possible across the operating frequency range. The designs of single-ended to differential converter, active power splitter and reference current generator are also discussed in this chapter.

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Chapter 5

Power Amplifier and Complete Signal Path

The design of the differential power amplifier is performed in this Chapter. The circuit topology, multi-stage design and matching network will be discussed in detail. Finally, the performance of the power amplifier and complete signal path are verified via simulation.

5.1 Design Considerations

A 60 GHz differential power amplifier (PA) is discussed in this section. Although a high efficiency power amplifier is preferable for the sake of power consumption, conventional high efficiency PAs require as much as 6 dB higher drive power than a linear Class A amplifier. Due to the high loss in the trombone delay line, we cannot expect a high driving power at the input of the power amplifier. In addition, a linear gain of 10 dB is often a luxury for silicon ICs at microwave frequency (say 60 GHz). Therefore, Class A is chosen in order to maximize the output power.

5.1.1 Circuit Specifications

The link budget calculation performed in Chapter 3 indicates 12 dBm output power from each path is required to fulfill the specification. From Figure 4.27, a 100 mV signal can be fed into the trombone delay lines. Figure 4.7 shows the large signal gain is -6 dB with the 100 mV input signal. Thus, -17.5 dBm ($(50\ mV)^2$ / ($2 \times 70\ \Omega$)) output power can be expected from the output of the path-select amplifier. Considering that another 2 dBm power will be lost in the transmission lines, the power gain of the power amplifier should be 31.5 dB to achieve 12 dBm output power. However, the above conclusions are obtained when the input amplifier (single-ended to differential converter and power splitter) and the path-select amplifier work near the linear region and are not saturated. In extreme case, the input amplifier will saturate first and the maximum power can be obtained from the

trombone delay line is around -16 dBm. Therefore, a 30 dB gain power amplifier is able to deliver 12 dBm output power. As mentioned in Chapter 3, constant group delay is another specification in our power amplifier. Since the RF bandwidth of a pulse mode radar is around 1 GHz, it is better to make the group delay variation of the power amplifier less than 1 ps over 1 GHz bandwidth. Thus, the mismatch between the power amplifiers in three signal paths will not have an obvious impact on the delay resolution of the beamformer. Besides, the input impedance of the power amplifier is matched to the characteristic impedance of the loaded transmission. Table 5.1 summaries the specification of the power amplifier.

It has been shown that the advanced SiGe HBT technologies can meet the demands of relatively high output power at millimeter-wave frequencies [1]-[3]. In order to fulfill the design goals listed in Table 5.1, a number of constraints were considered, as described in the following sections.

Table 5.1: Power amplifier specifications.

Bandwidth	57 – 66 GHz
1 dB compression output power (P_{1dB})	12 dBm
Small signal power gain (G_{Tmax})	30 dB
Group delay variation	1 ps/GHz
Input impedance	70 Ω
Supply voltage	2.5 V

5.1.2 Circuit Topology

Power amplifiers are typically the most power-consuming blocks in RF and microwave transceivers. In order to have higher efficiency, single-ended power amplifiers are usually favored. However, differential topologies are also commonly used in the millimeter-wave frequencies, which simplifies the design process and improve the reliability of the circuit. The differential power amplifier has three advantages. Firstly, it is not easy to make a low-

impedance ground plane in the millimeter-wave frequency range. At 60 GHz, a 10 pH inductance in the ground plane adds 4 Ω reactance to the AC ground of the single-ended amplifier stage, and this degeneration inductance reduces power output and gain. The virtual ground nature of the differential pair provides a local AC ground and the unwanted effects from the ground inductance can be avoided. Secondly, the differential topology can provide 3 dB extra output power, which is valuable at 60 GHz. Thirdly, the transformation ratio between the antenna impedance and the optimum load of the power amplifier can be reduced by a factor of 4. This improves the efficiency of any output matching network. Above all, a differential power amplifier architecture will be exploited, which also simplify the interface between the trombone delay line and the power amplifier.

Whether to utilize the cascode stage also deserves discussion. In principle, the use of a cascode stage requires a higher supply voltage and efficiency is thus reduced for the same output power. However, the open-base collector-emitter breakdown voltage (BV_{CEO}) is governed by Johnson limit [4], which indicates a lower BV_{CEO} at higher frequencies. The cascode stage can provide low external resistance at base and excess electrons caused by impact ionization can then have a low-impedance path to flow out of the base terminal. Therefore, the breakdown voltage is maximized and limited by the reverse breakdown voltage of the collector-emitter junction BV_{CER}. It should be emphasized that it is not easy to have AC ground at base of the cascode stage because the current gain at 60 GHz is less than 5. The differential topology can somehow cancel the large base-current swing. Only a small decoupling capacitor is needed at the base to account for base currents asymmetries [1]. Therefore, the cascode stage will be exploited for this reliability purpose. Another important reason to have a cascode stage at the output is to achieve good isolation. Since three power amplifiers are working at the same time, the isolation between the output and input becomes stricter. The cascode stage can improve the isolation and enhance the stability of the power amplifier. In addition, cascode stage provides extra power gain.

5.1.3 Selection of Device Size, Geometry and Bias Point

The performance of the power amplifier is limited by the gain and bandwidth of the active devices used in the design. In order to maximize the gain at the operating frequency, the next step is to select appropriate size, geometry and bias point for the active device. Figure 5.1 shows the f_{MAX} versus emitter current density for different device sizes and geometries. "8 μ" means the emitter length of the device is 8 μm while "1B1E" means the device has one base stripe and one emitter stripe. Devices with multiple base and emitter stripes usually outperform those with single base and emitter stripe when the emitter length of the device is relatively long (> 4 μm). This is mainly because the parasitic base resistance is minimized. However, a device with shorter emitter length (8 μm) outperforms the one with longer emitter length (16 μm). This may be due to the overall time constant R_bC_μ increases with the emitter length in this process. "8 μ, 4B2E" configuration is chosen.

The emitter current density should also be large enough to realize a high gain-bandwidth product (i.e., a large f_{MAX}). The power amplifier operates with large signals. For a higher large signal power gain, it is better to bias the transistor a bit higher than the peak bias f_{MAX} point. Besides, the emitter current density is also limited by the reliability design rule.

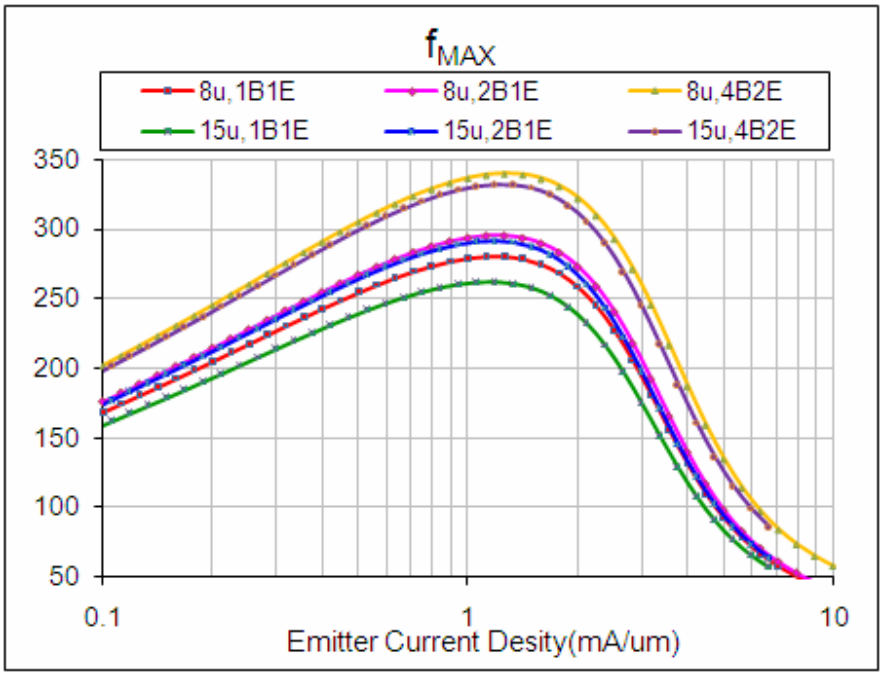


Figure 5.1: f_{MAX} versus current density for varying device size & geometry.

5.1.4 Single Stage Amplifier Characterization

Once the circuit topology, device size and bias point are determined, it makes sense to verify the maximum power gain and stability of a single stage differential cascode amplifier. Figure 5.2 shows the maximum power gain is around 30 dB at 60 GHz. The gain is larger than the value estimated from the f_{MAX} of the transistor and the extra power gain comes from the differential topology and the cascode stage. Rollett's stability factor k is less than 1 around the frequency of interest. The amplifier stage is not unconditionally stable and the stability of the final design needs to be further checked.

The maximum power gain is the limit for the power amplifier since conjugate matching is assumed at the input and output of the amplifier. In the real design, some gain is traded off for higher output power and wider bandwidth. Therefore, a two stage amplifier is required to achieve 30 dB gain at 60 GHz.

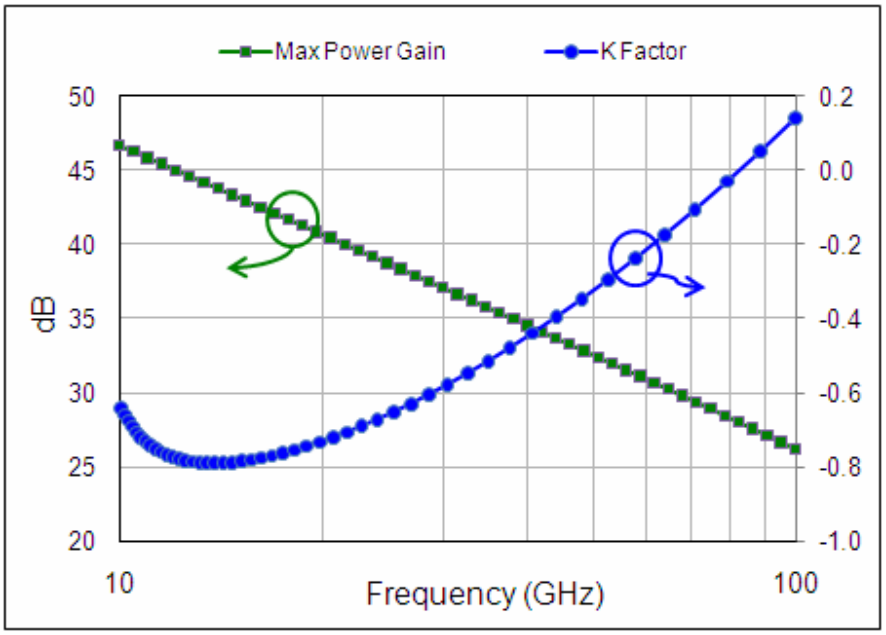


Figure 5.2: Maximum power gain and stability factor of a single stage.

Figure 5.3 shows the simplified block diagram of the two-stage differential amplifier. Center-tap connections in the middle of the transmission lines are used to feed the supply

and the base bias voltage for the differential pairs. These transmission lines are also part of the matching networks. Pulse modulation (PM) of the output signals is realized by modulating the base bias of the differential pair in the 2nd stage.

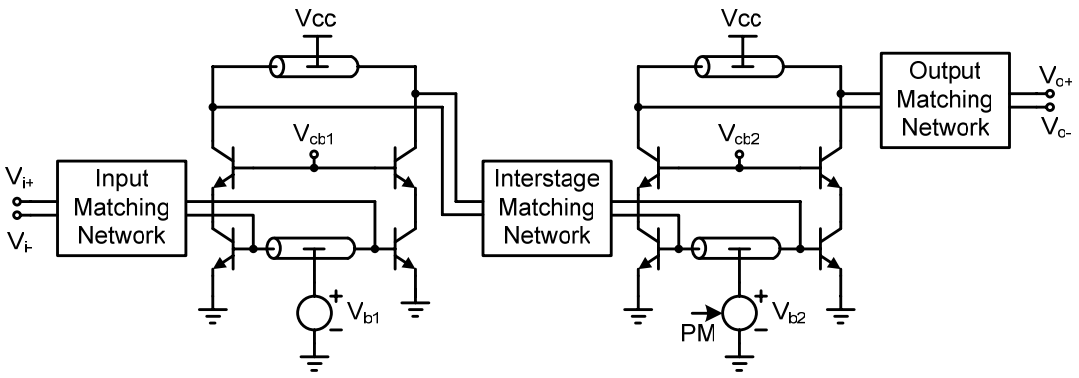


Figure 5.3: Simplified block diagram of two-stage differential PA.

5.2 Output Stage

The PA design begins with the output stage. The design and optimization methodology are described in this section. In the first place, the output stage needs to deliver the required output power. Due to the voltage or current limitations of the active devices, load line theory [5] is adopt to choose the optimum load impedance and maximize power transfer. In the second place, since the output stage is the most power-hungry module in the power amplifier, the loss in the output stage, including the output matching network, has the most impact on the overall efficiency of the power amplifier. In our approach, as shown in Figure 5.4, the supply voltage is chosen as 2.5 V and the bias current is set as 20 mA. The output node can swing between 1.5 and 3.5 V while all the transistors work in active region. Therefore, the optimum load impedance is 100 Ω. No additional output matching network is needed and the output power and efficiency can be increased at the same time. A 356 pH spiral inductor is used to resonate out the parasitic capacitances of the output transistors. For the same inductance, the equivalent line length of an inductor is shorter than that of a transmission line and less loss can be expected. The width and diameter of the inductor are optimized to achieve a higher quality factor at 60 GHz. In the final design, the parasitics of the bondpad and the transmission between the output of the power amplifier and the

bondpad should also be considered. The value of the inductor may decrease, but the use of a inductor with smaller value would better the final performance in our case.

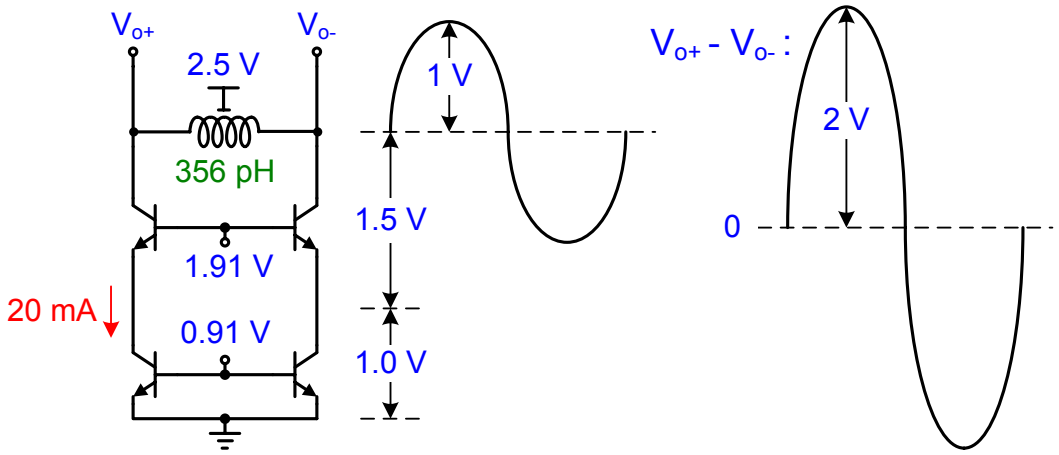


Figure 5.4: Output stage and output waveform of the power amplifier.

5.3 Driver Stage

The driver stage provides the desired signal power to the output stage and exhibits the required input impedance to the source. The device sizes in the driver are normally determined by the required input power of the output stage. However, since the group delay variation across the frequencies of interest is one of the most stringent specifications in this design, the design methodologies adopted here is different.

The relationship between the bandwidth and group delay of a low-pass RC network has been derived in Section 4.2.1.4, which indicates the group delay of the network will reduce by a factor of 2 at the -3 dB bandwidth point. In order to minimize the delay variations, either the absolute group delay should be reduced, or the bandwidth of the network needs to be increased. Both imply that more supply current is required. The group delay of a two stage power amplifier is double the delay range (~16 ps) realized in the trombone line. Therefore, even if the power amplifier has a bandwidth of 10 GHz, the delay variation across 1 GHz may still be larger than 1 ps. If mismatch exists, all our efforts to reduce the delay variations in the trombone delay line may be wasted. Layout of the three paths

requires special attention to minimize this mismatch. To provide some design margin, it is better to keep the delay variation across 1 GHz less than 1 ps. The bandwidth is limited at the output of the driver stage. As shown in Figure 5.5, although the inductor L can be merged into the matching network, it is clearer to separate them and see how they limit the bandwidth of power amplifier. In the first place, there is usually a big difference between the input impedance of the output stage and the optimum load of the driver. The ratio between the two limits the bandwidth of the matching network [5]. In order to increase the bandwidth of the matching network, the ratio between the transistor areas for the two stages is selected as 4. In the second place, the inductor L is used to resonate out the parasitic capacitance at the output of the driver. The bandwidth of the load (LC tank) may be narrower than desired if an inductor with high quality factor (Q) is applied. Therefore, a high Q inductor is not preferable to use here. Although a low Q inductor will increase the loss, it is easier to implement and has negligible impact on the overall efficiency of the power amplifier. A transmission line with 1.5 dB/mm loss will be exploited here to realize the inductance.

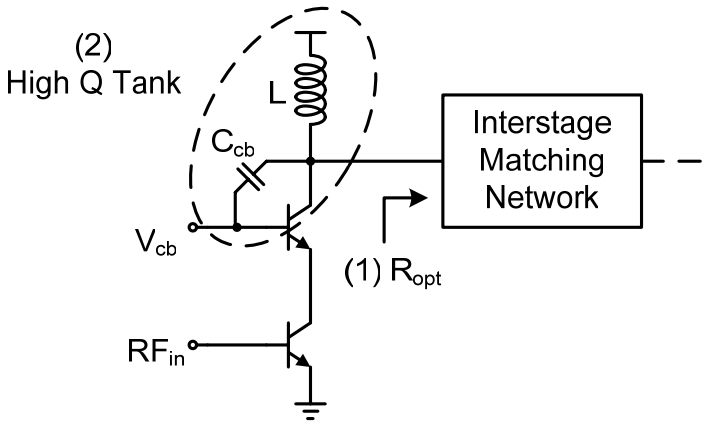


Figure 5.5: Bandwidth limitation in the driver stage.

5.4 Matching Networks

The matching network is an essential part to realize impedance transformation. Compared with the "L" type matching network, "Π" or "T" topologies [6] provide more freedom to specify the bandwidth or impedance transformation ratio of the matching network. However, they are usually only suitable to narrowband applications. There are wideband

matching techniques where multi-section "L" type matching networks are used, but the component values in these matching networks are usually not practical to implement on chip (either too large or too small). Therefore, the simple "L" type matching network is usually the practical and efficient way to perform on-chip impedance transformation. In addition, transmission line elements are often used to realize on-chip matching networks, especially in the millimeter wave frequency range.

Figure 5.6 shows a commonly used high pass "L" type matching network where C can also act as the DC-blocking capacitor between stages and L can be used to feed the bias. The goal of the matching network is to transform R_2 to R_1. R_{Ls} is the loss of the inductor. The quality factor of the inductor increases with frequency while that of the capacitor decreases with frequency. However, the capacitor in the network is assumed lossless because the quality factor of the capacitor used is still 20 dB larger than that of the inductor. It is reasonable especially when the inductor is realized by a short-stub transmission line.

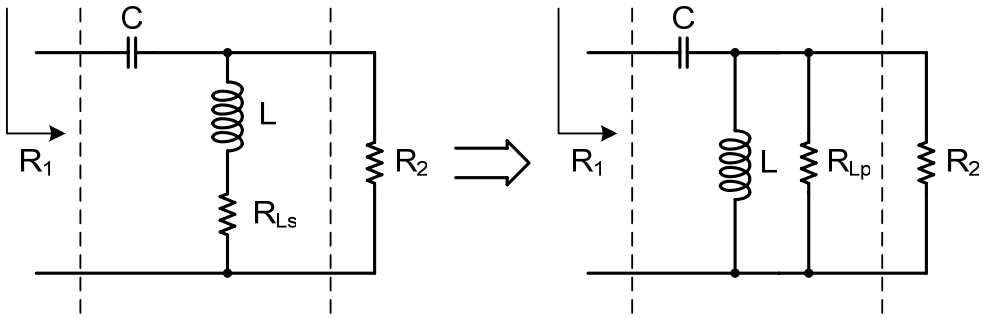


Figure 5.6: high pass "L" type matching network.

Let Q_t and Q_{to} represent the total Q of the network when the inductor is lossy and lossless, respectively. They are given by

$$Q_{t0} = \sqrt{\frac{R_2}{R_1} - 1} \tag{4.23}$$

and

$$Q_t = \sqrt{\frac{R_2 \,//\, R_{Lp}}{R_1} - 1}\,. \tag{4.24}$$

The relationship between the two and the loss of the matching network can be expressed as [7]

$$Q_t \approx Q_{t0}\left(1-\frac{Q_{t0}}{2Q_L}\right) \tag{4.25}$$

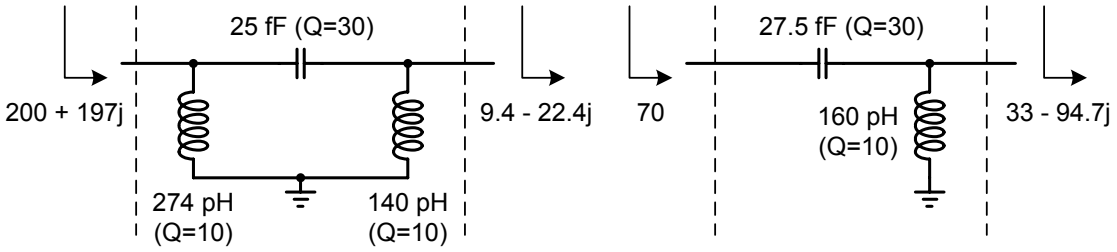
and

$$\eta_{loss} = \frac{R_2}{R_{Lp}} \tag{4.26}$$

$$\approx \frac{Q_{t0}}{Q_L}\left(1+\frac{Q_{t0}}{2Q_L}\right), \tag{4.27}$$

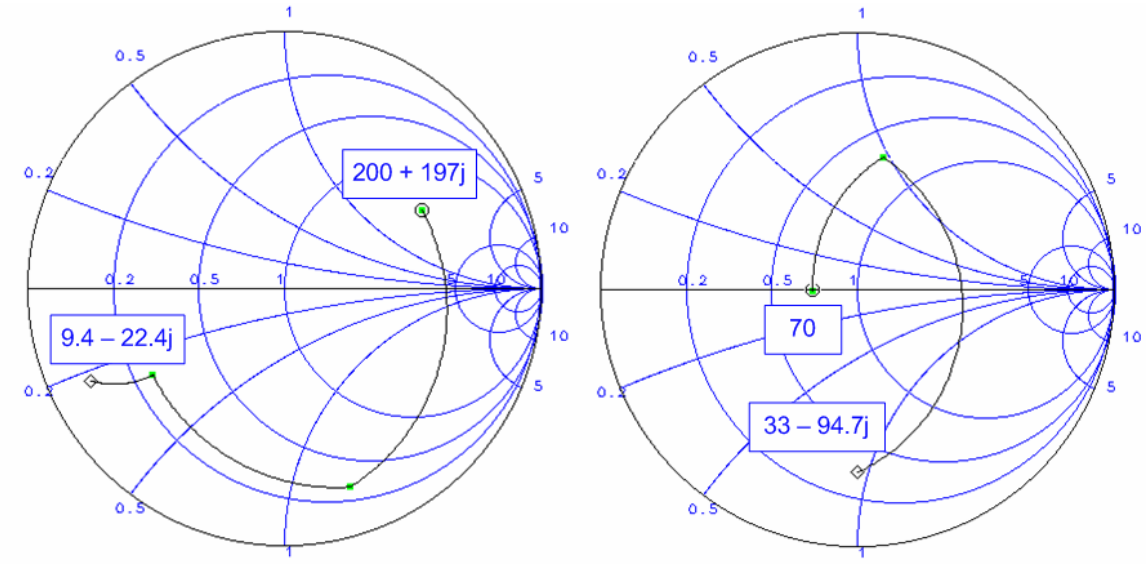
where the η_{loss} is defined as the ratio of the power dissipated in the on-chip inductor to the power delivered to the load and Q_L is the quality factor of the inductor. If Q_{to} = 3 and Q_L = 10, approximately 35 % power is lost in the on-chip network. Equation (4.27) also implies that low Q matching network is less lossy.

Let us return to the design of interstage and input matching network. L type high pass matching networks are used here. As shown in Figure 5.7 (a), the interstage matching network transforms the input impedance of the output stage to the optimal load for the driving stage. Optimization is exploited to choose the inductance and capacitance values that minimize the total area used by the matching network. Figure 5.7 (b) shows the input matching network, which transforms the input impedance of the driving stage to the characteristic impedance of the loaded transmission line. Smith charts of both matching networks are shown in Figure 5.8. The inductances in the matching networks are realized by differential transmission lines with 120 Ω characteristic impedance and similar quality factors. Table 5.2 shows the electrical length and corresponding physical length of these transmission lines in the interstage and input matching networks.



(a) (b)

Figure 5.7: (a) interstage & (b) input matching networks.



(a) (b)

Figure 5.8: Smith charts of (a) interstage & (b) input matching networks.

Table 5.2: Electrical and physical length of transmission lines.

	Electrical Length	Physical Length
Interstage Match		
short stub (L1)	40.5°	285 µm
short stub (L2)	23.5°	165 µm
Input Match		
short stub (L3)	27°	187 µm

5.5 Pulse Modulation

For a pulse Doppler radar, the output signals have to be modulated. The output stage of the power amplifier must be fully switched off within 0.5 ns in order to detect the objects nearby (0.15 m). In the OFF mode, the RF carrier leakage at the output should be kept as low as possible so that the dynamic range in the radar application can be preserved. Reference [8] uses a differential pair with tail current biasing as the output stage, and switches this tail current sink to modulate the output power. The tail current sink costs more than 0.5 V voltage headroom, which reduces the efficiency of the power amplifier. Another disadvantage is the poor current handling capacity of CMOS transistors; the sizes of the switching transistors have to be large in order to reduce the voltage drop across these switches. Thus, it consumes a large amount of current to drive these switches and will not be adopt here.

Figure 5.9 shows another two approaches to apply pulse modulation scheme. In Figure 5.9 (a), anti-phase pulse signals are used to switch the base bias voltage of the output stage. The ratio between the sizes of (M_{P2}, M_{N2}) and (M_{P1}, M_{N1}) is consistent with the current ratio between the reference current and bias currents of the output stage. One of the problems is that in large signal operation, the positive and negative swings of the base currents are asymmetric due to the nonlinear property of the transistors. Consequently, the sum of the base currents of Q_1 and Q_2 is not zero but a rippling current. The DC component of this rippling current is not zero which has to be fed by bias circuits. Therefore, the voltage drops across M_{P1} and M_{P2} could be different and they are signal-level dependent. In large signal operation, the base bias voltages of Q_1 and Q_2 are unpredictable. A safer approach is shown in Figure 5.9 (b). M_1 is used to steer the reference current when the amplifier is in the OFF state, M_3 acts as β-helper and C_S is exploited to improve the stability of the bias circuits.

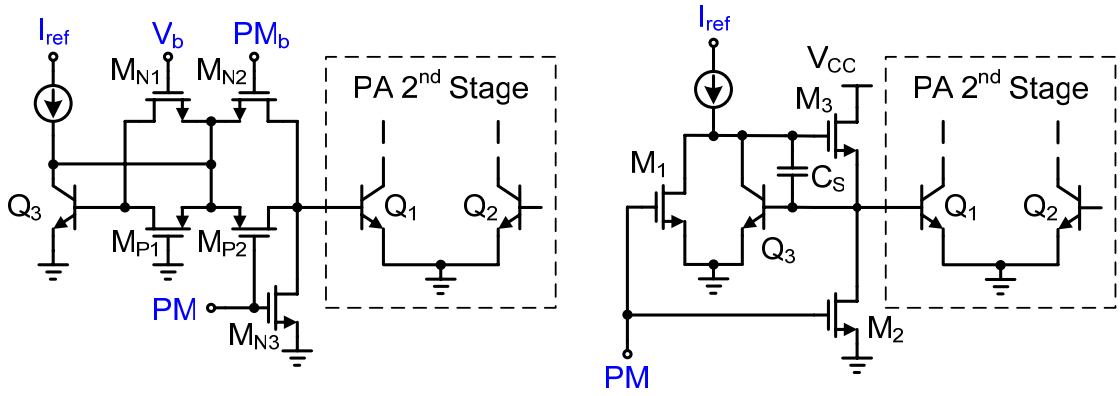


Figure 5.9: Two approaches to switching bias in the output stage.

When the output stage of the power amplifier is switched, the output signal will potentially ring at two frequencies. The ringing around 60 GHz is due to the LC tank at the output of the power amplifier. The high frequency settling time cannot be reduced unless the quality factor of the tank is reduced. The ringing at low frequency (around 6 GHz) is due to the undamped feedback loop in the bias circuits. A long low frequency settling time will affect the pulse mode operation of the amplifier. As shown in Figure 5.10, open loop analysis is used to see how C_S can improve the stability of the loop. The loop is broken at the base of M_3. For convenience, the simplest transistor model is used and C_1 and C_2 account for the parasitic capacitances at each node. The node equations are given by

$$j\omega C_1 v_x = g_{M1}\left(v_i - v_x\right) + j\omega C_S\left(v_i - v_x\right) \tag{4.28}$$

and

$$v_o = -g_{Q1} v_x / j\omega C_2 . \tag{4.29}$$

Solving above equations, we obtain

$$\frac{v_o}{v_i} = -\frac{g_{Q1}\left(g_{M1} + j\omega C_S\right)}{j\omega C_2\left[g_{M1} + j\omega\left(C_S + C_1\right)\right]} . \tag{4.30}$$

The transfer function contains two poles and one zero which can be express as

$$f_{P1} = 0 , \tag{4.31}$$

$$f_{P2} = -\frac{g_{M1}}{2\pi\left(C_S + C_1\right)} \tag{4.32}$$

and

$$f_Z = -\frac{g_{M1}}{2\pi C_S}. \tag{4.33}$$

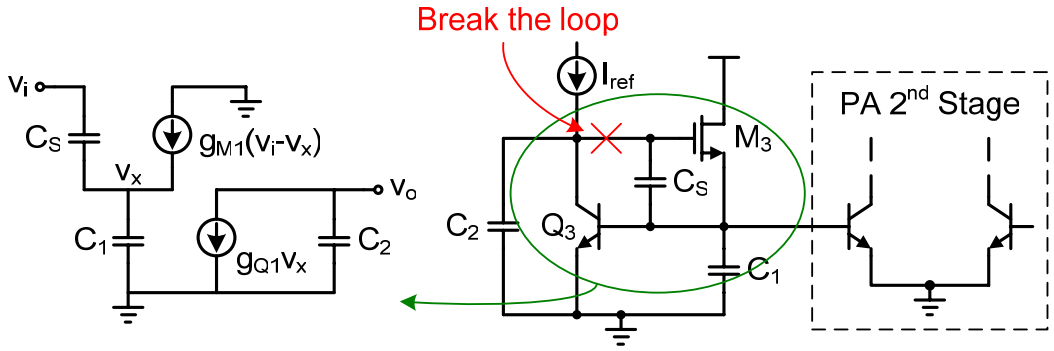


Figure 5.10: Open loop analysis of the bias circuit.

The dominant pole f_{P1} in the loop remains in low frequency. Interestingly, if C_S is much larger than C_1, the non-dominant pole f_{P2} and the zero f_Z can cancel with each other. Therefore, there is only on pole in the open loop response and the stability of the loop is guaranteed.

The last thing which needs to be mentioned is that it takes some time to turn on a transistor. A 1ns width pulse cannot necessarily result in a 1ns pulsed output signals. Therefore, the transmitted power is also reduced, which is related to the detection range of the radar. In order to restore the pulse width, some logic gates are used to widen the effective pulse width. As shown in Figure 5.11, this logic circuit is often used to generate non-overlapping clock signal [9]. If a 1 ns pulse is applied at the input, the effective pulse width at the output is approximately 1.2 ns.

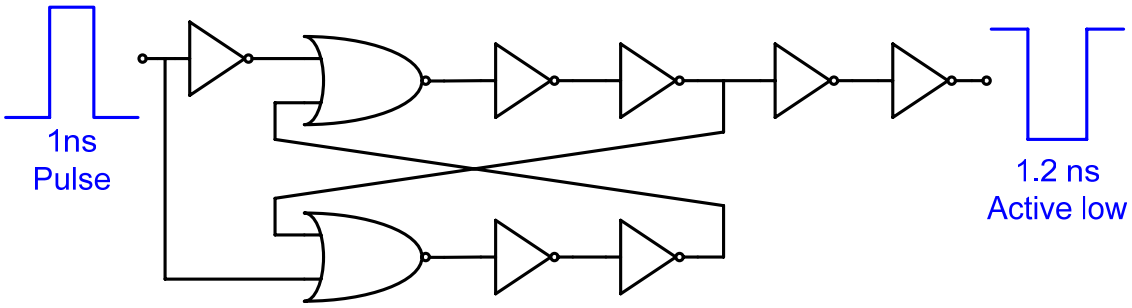


Figure 5.11: Set-reset flip-flop circuit to increase the effective width of the pulse signal.

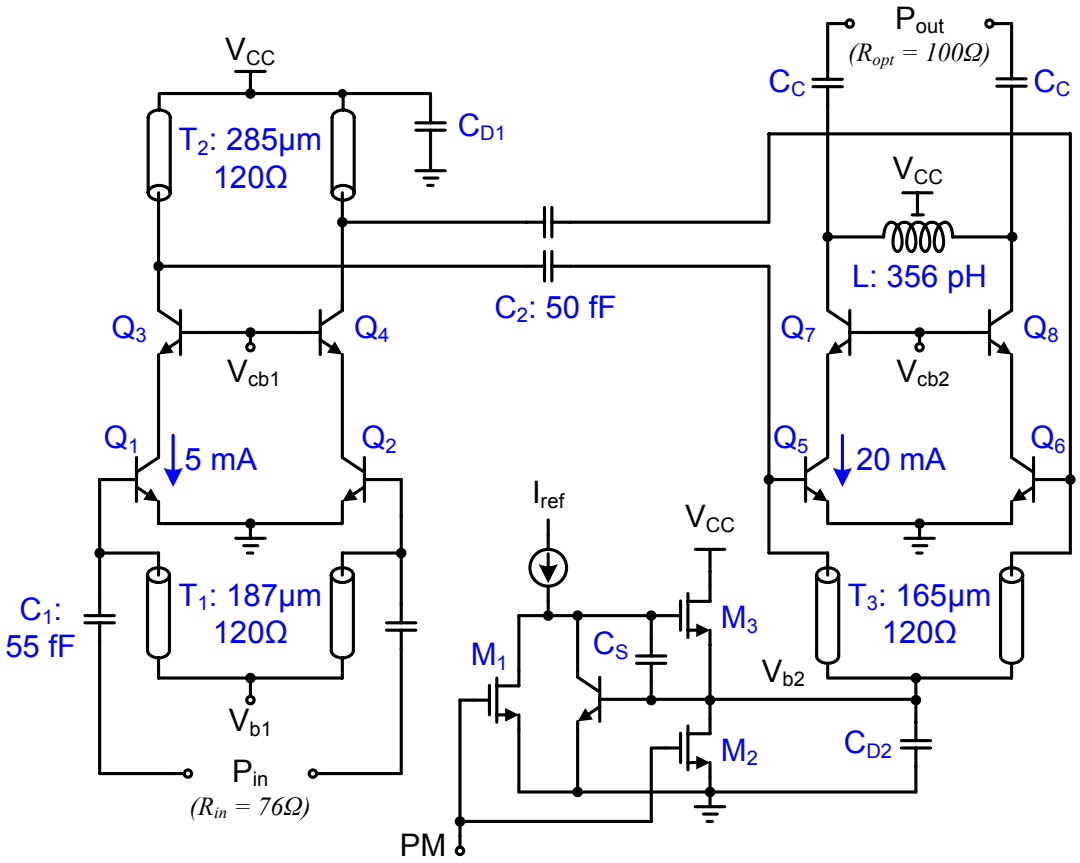


Figure 5.12: Simplified diagram of two-stage power amplifier.

5.6 Power Amplifier Simulation Results

The final schematic of the two-stage differential power amplifier based on the methods discussed above is shown in Figure 5.12. Each stage is biased by on-chip supply and

temperature insensitive current source. The AC coupling capacitors are placed at the output. Besides, decoupling capacitors are connected to the voltage supply node. The small signal and large signal simulation results are summarized in this section. All the simulations are performed for the nominal process technology models at a temperature of 60^{o}C.

The small signal power gain S21 and the group delay of the power amplifier are plotted in Figure 5.13. The maximum power gain is 31.8 dB at 60 GHz and the -3 dB bandwidth is 12 GHz (54-66 GHz). Such a high bandwidth is tailored to minimize the delay variation within the required frequency band. Between 57 and 63 GHz, the maximum delay difference is less than 3.5 ps. In the range of 63 and 66 GHz, the group delay varies at the rate of 2 ps/GHz. A flatter group delay can be obtained simply by increasing losses in the transmission line used for interstage matching. If the quality factor of the transmission line is reduced to 5, the delay variation in the range of 57 and 66 GHz can be less than 5 ps. However, the maximum power gain decreases by approximately 3 dB at the same time. From Figure 5.13, we can clearly see the relationship between the bandwidth and group delay variation, as discussed in Section 5.3.

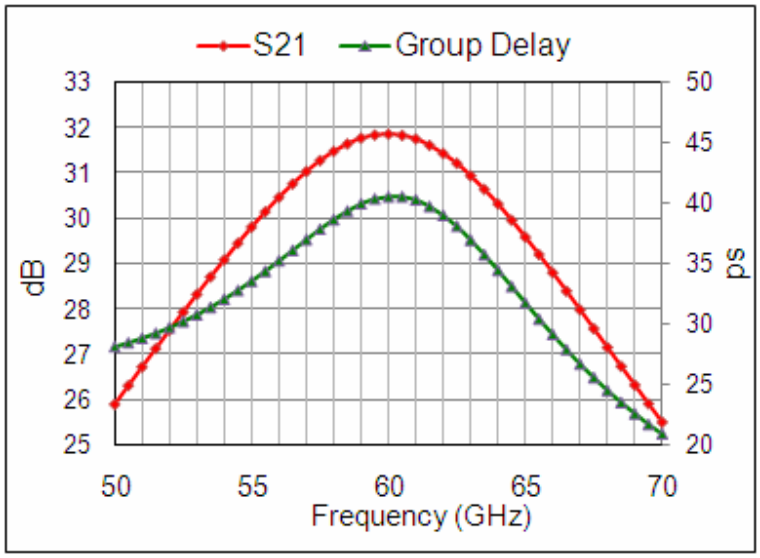


Figure 5.13: Small signal gain S21 and group delay.

Figure 5.14 shows the input reflection coefficient S11 is less than 10 dB between 54 and 70 GHz. The output coefficient S22 is just below 0 dB. This is because the output stage is only

tailored for “load line” match. Therefore, the impedance match between the transmission lines (both on-chip and off-chip) and antenna becomes important. Otherwise, an isolator has to be placed between the output stage and the antenna in order to avoid signal reflections from degrading the delay resolution. The isolation (S12) between the output and input of the power amplifier is below -90 dB between 50 and 70 GHz.

The simulated output power versus input power transfer curve at 60 GHz is plotted in Figure 5.15. At 1 dB compression point, the output power and the power gain is 12.5 dBm and 31 dB, respectively. It implies the required input power should be -18.5 dBm, which is delivered via the trombone delay line. The saturated output power is 17.5 dBm. Figure 5.16 shows the power added efficiency (PAE) of the two stage power amplifier. The power dissipated in the bias circuits is also included, which accounts for more than one-fifth of the total power consumption. Benefiting from the high f_{MAX} achieved by a single transistor, the maximum PAE is above 20. At 1 dB compression point, PAE is around 10.

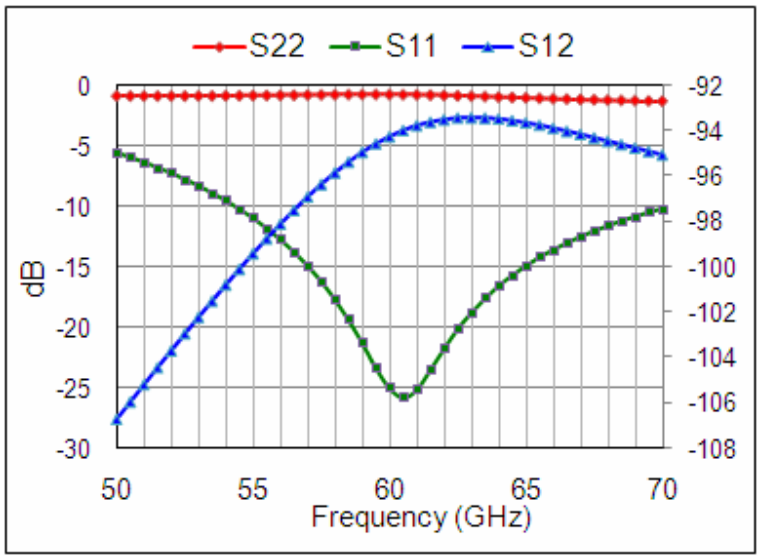


Figure 5.14: Reflection coefficient S11, S22 and reverse transmission coefficient S12.

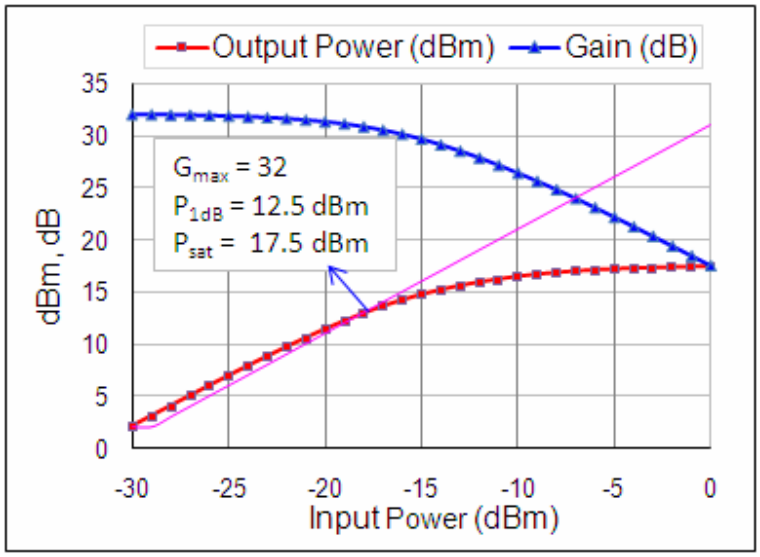


Figure 5.15: Output power and power gain @ 60 GHz.

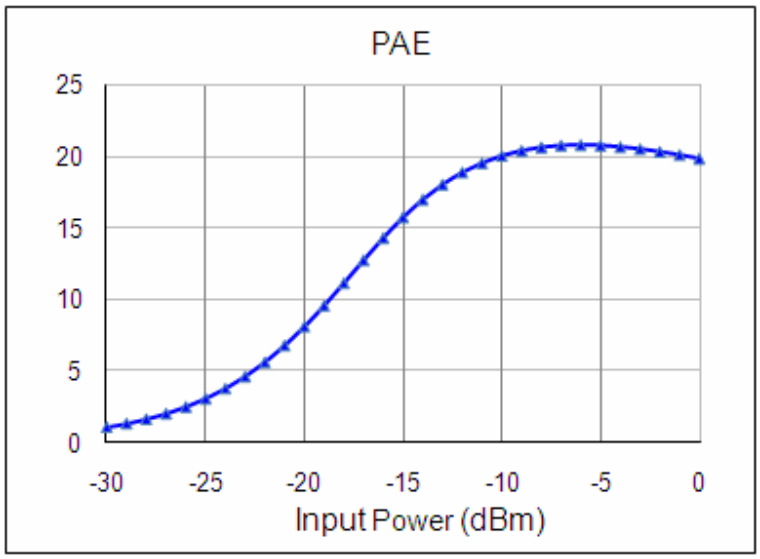
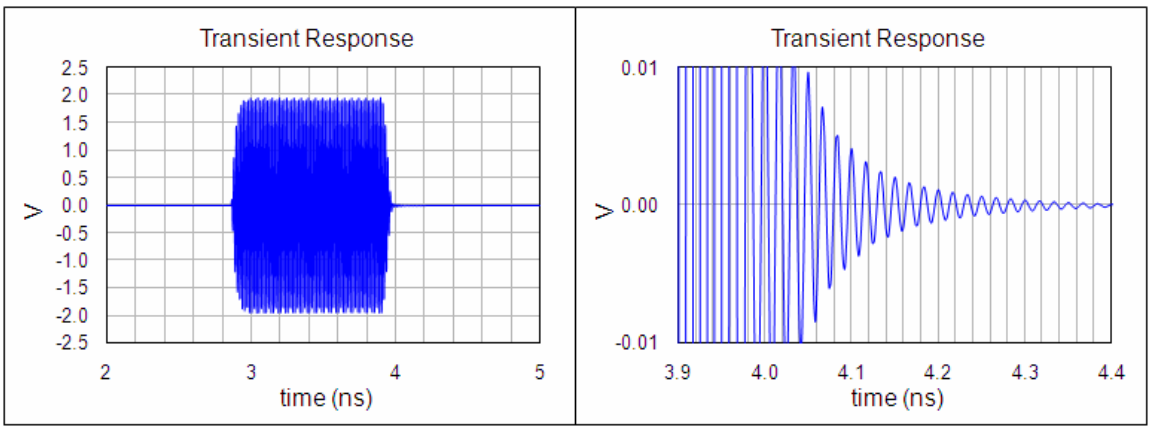


Figure 5.16: Power added efficiency (PAE) @ 60 GHz.

Figure 5.17 shows the pulsed output signal. The width of the pulse is 1 ns. When the power amplifier is switched off, the output power reduces from 12 dBm to -55 dBm within 0.5 ns. Since the presence detection radar is assumed to be placed at the center of the ceiling in a room, almost no objects will be detected within 1 ns (the distance between the object and radar should be less than 15 cm). The carrier leakage power can be as low as -65 dBm after the amplifier has stabilized in the OFF state.



(a) (b)

Figure 5.17: (a) 1ns width output signal, (b) power amplifier switched off within 0.5 ns.

5.7 The Complete Signal Path

The complete three signal paths are simulated, which includes the single-ended to differential converter and power splitter at the input, the left and right trombone delay lines and three power amplifiers. All the simulations are performed for the nominal process technology models at a temperature of 60^{o}C.

Figure 5.18 shows the group delays of the 15 different delay paths. The delay path is controlled by the local decoder. The delay difference between two paths is around 1.1 ps across the frequency range from 50 and 70 GHz. Figure 5.19 shows the corresponding voltage gains of the 15 delay paths. Due to the loss the transmission line, there is 2 dB gain difference between shortest and longest paths. The center frequency moves to 59 GHz and the 3 dB bandwidth is around 11 GHz (53 – 64 GHz).

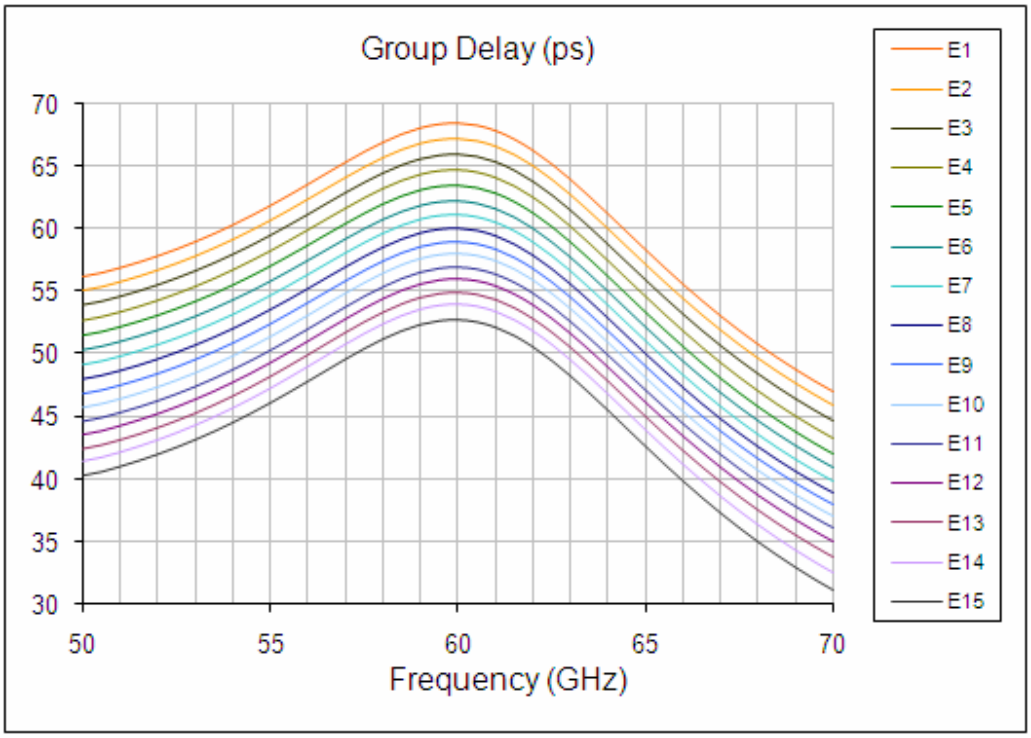


Figure 5.18: Group delay of the 15 signal paths.

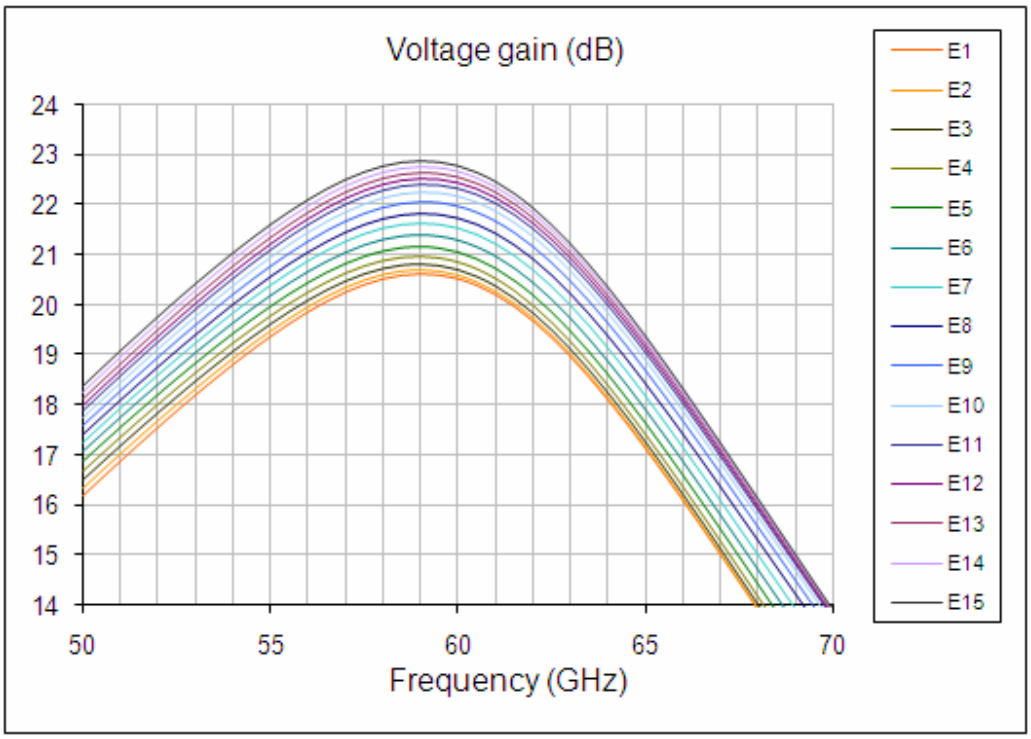


Figure 5.19: Gain of the 15 signal paths.

Figure 5.20 shows the delays in three paths with different delay settings at 60 GHz. The delay range is around 16 ps (from 52.5 to 68.5 ps). Figure 5.21 shows the delay resolutions at 60 GHz, which is less than 0.15 ps between the maximum deviating point and 1.1 ps. Figure 5.22 shows the corresponding gains in three paths at 60 GHz. The gains of the shortest and longest paths are 22.7 and 20.5 dB, respectively.

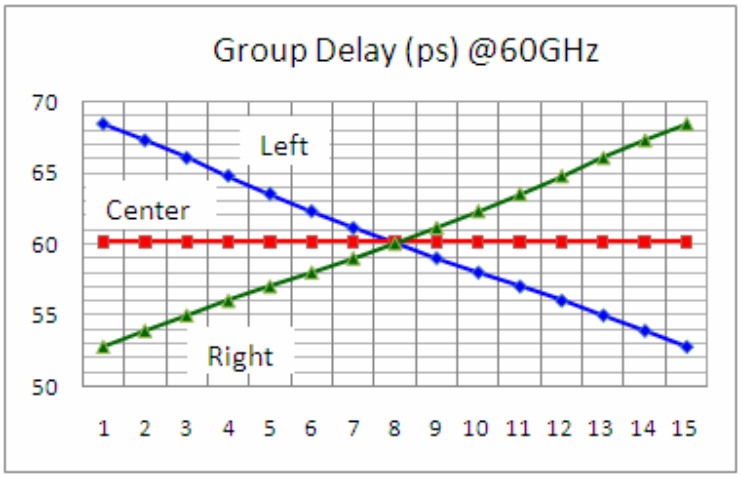


Figure 5.20: Group delay of the three paths @ 60 GHz with different delay settings.

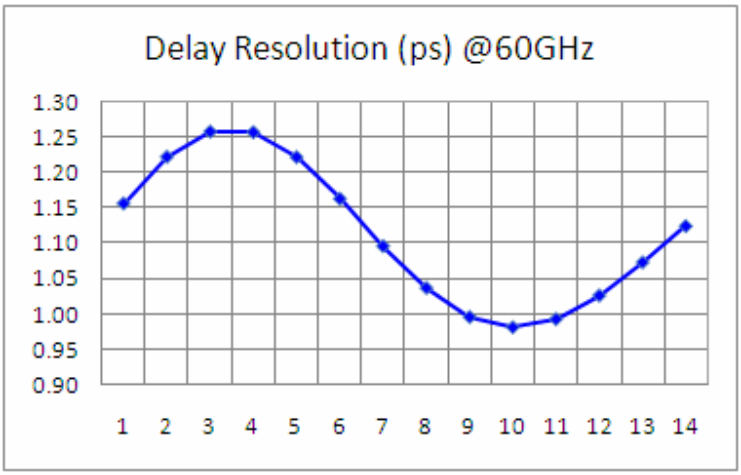


Figure 5.21: Delay resolution of the left path @ 60 GHz with different delay settings.

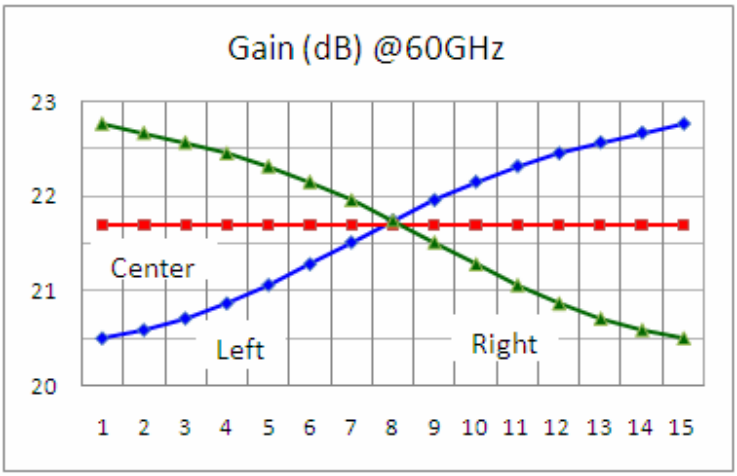
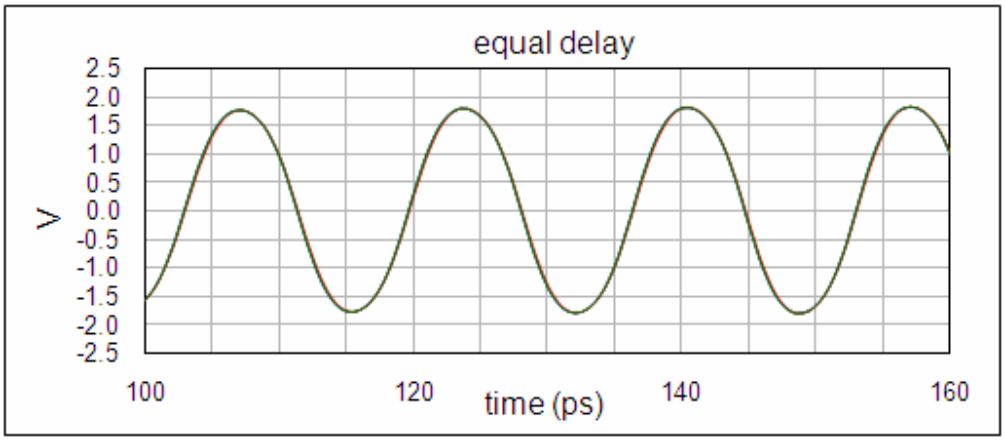


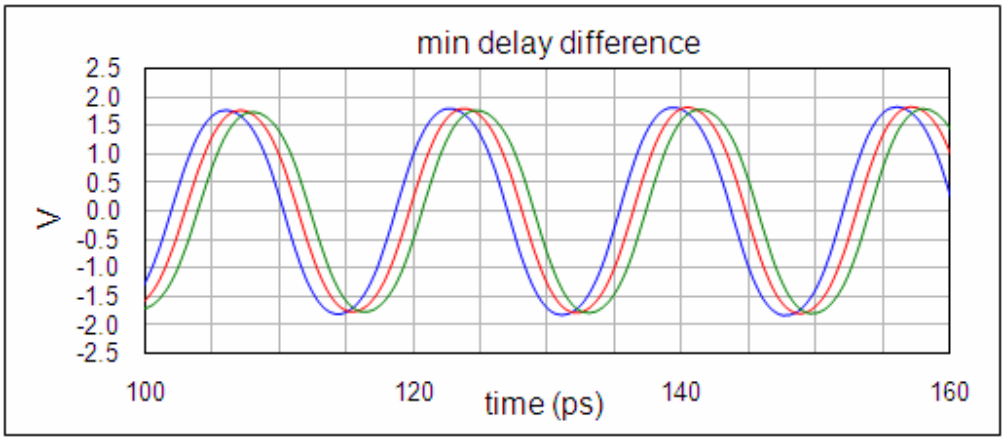
Figure 5.22: Gain of the left, center & right paths @ 60 GHz with different delay settings.

Figure 5.23 shows the large signal simulation results with three different situations. In Figure 5.23 (a), the delay difference between three paths is zero while minimum and maximum delay differences are shown in Figure 5.23 (b) and (c), respectively. The input signal is a 60 GHz sinusoidal signal with the amplitude of 240 mV.

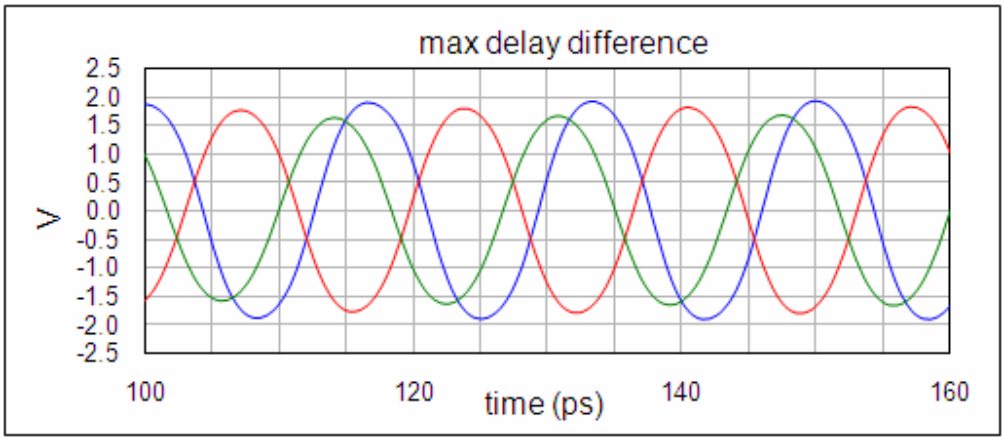
Table 5.3 summarizes the performance of the 3-path beamforming transmitter. The beam forming and steering performances will be degraded by the gain errors and delay variations with different delay settings. The gain error of 2 dB between the shortest and longest paths may cause that the desired beam cannot be formed properly when the incident angle is large. The gain loss in the trombone delay line can be restored by applying variable gain path-select amplifiers. The delay variation of 0.15 ps is negligible when the incident angle is zero and may result in a beam steering error of 2^{o} when the incident angle is 45^{o}. These steering errors are acceptable in ordinary presence detection radars. Above all, the beamforming transmitter presented in this thesis can be used for indoor presence detection. An ordinary living space with the size assumed in Chapter 3 can be monitored with the beam steering resolution of 9.5^{o}.



(a)



(b)



(c)

Figure 5.23: Three paths with (a) equal delay, (b) minimum delay difference (~1.1 ps) and maximum delay difference (~ 8 ps).

Table 5.3: Performance of the 3-path beamforming transmitter.

	Values	Comments
Supply Voltage	3.5 & 2.5 V	3.5 V: Trombone Delay Line 2.5 V: PA and Digital Circuits
Delay Range	52.5 - 68.5 ps (16 ps)	beam steering range: from -75^o to 75^o
Delay Resolution	~ 1.1 ps	beam steering resolution: ~ 9.5^o
Delay Variation	< 0.15 ps	beam steering error < 2^o (Inc. angle 45 ^{o})
-3 dB bandwidth	11 GHz	53 – 64 GHz
Voltage Gain	20.5 dB (longest path) 22.7 dB (shortest path)	2 dB is lost in the trombone delay line
Output Power P_{1dB}	12.5 dBm	Max. detection range > 6 m
Power Consumption	250mW + 480mW (PA works continuously)	Converter & Splitter: 30 mA × 3.5 V Delay path: 12 mA × 3.5 V × 3 Biasing: ~5 mA × 3.5V Power Amplifier: 64 mA × 2.5 V × 3
Area	1.7 mm × 1.5mm = 2.55 mm^2	Estimation

5.8 Conclusion

In this chapter, the design of a 60 GHz differential power amplifier was presented. The power amplifier is tailored for minimizing the delay variations and delivering sufficient output power. The small signal power gain is 32 dB and the output power at 1 dB compression point is 12.5 dBm. Finally, the complete signal path was verified. The simulated delay range is 16 ps and the delay resolution is around 1.1 ps.

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Chapter 6

Conclusions and Recommendations

Beamforming systems operating at millimeter-wave frequencies provide spatial selectivity, gain and wider bandwidth when compared to single antennas, which benefit radar applications. In this thesis, a 60 GHz beamforming transmitter for a pulse Doppler radar is designed. The pulse Doppler radar transmitter is tailored for indoor presence detection, which may be an enabling technology for future smart home applications.

The feasibility of realizing a UWB beamforming radar system on a silicon IC was considered in Chapter 2 of this thesis. Various techniques that are required to implement such systems were explored, and potential challenges when attempting to implement a true-time delay element were addressed. In Chapter 3, link-budget calculations were performed based on a typical household environment. The performance requirements for the radar transmitter were specified and appropriate system architecture proposed. The design of a beamforming transmitter, including simulation results in a 0.13um BiCMOS technology were presented in Chapter 4 and 5.

The key contributions and innovations of this work are:

1. Group delay variations of a transmission line due to mismatch have been investigated and system architecture for a true-time-delay beamformer was proposed.
2. A design methodology required to make the characteristics of a loaded transmission line constant within its operating bandwidth were developed.
3. The relationship between the bandwidth and group delay of an amplifier was analyzed and an approach to the design of a power amplifier with flat group delay within its operating bandwidth was developed.

6.1 Conclusions

The following paragraphs detail the contributions presented in this thesis. Some conclusions are drawn in order to address the feasibility of implementing a UWB beamformer.

Firstly, in order to save design time and address a "first run" working chip, the following steps were taken: 1) chose or developed specific techniques, such as true-time-delay element and pulse-mode modulation scheme, which were tailored for high-resolution radar application; 2) both chip- and board-level floorplans were considered to check whether the proposed techniques can satisfy the desired requirements; 3) perform link budget and power budget calculations to specify the design targets for each building block; 4) benchmark the active and passive components in the design library in order to identify potential performance limitations for each building block.

Secondly, from the simulation results, feasibility of a UWB beamformer with 16 ps delay range and 1.1 ps delay resolution was shown, which implies that the beam can be steered from -75^{o} to 75^{o} with a steering resolution of 9.5^{o}. A state of the art SiGe BiCMOS technology offers excellent performance from the active devices and good quality passive components for operation at 60GHz, making it possible to design a power amplifier with more than 10 dBm output power, 10 GHz -3 dB bandwidth and 20% peak PAE.

Thirdly, it was determined that the most difficult aspect to realize in a true-time-delay beamformer is implementation of a large delay range with fine delay resolution. In our case, the delay resolution is limited by the parasitics of the path-select amplifier and its width in layout. The delay range is limited by the requirements of the delay resolution and the line attenuation. With the proposed technique, it is almost impossible to realize more than 25 ps delay range with 1 ps delay resolution. As shown in Figure 3.9, the group delay variations of a signal running through a transmission line increase linearly with the length of the line and exponentially with the reflection coefficient. In order to achieve the requirements of large delay range with fine delay resolution, three approaches have been taken in system and circuit levels, which are described in following paragraphs:

A system architecture is proposed to avoid the potential factors which limit the group delay resolution, as shown in Figure 3.12. Since the delay varies linearly with the length of the transmission line due to mismatch, all the interconnects in the signal paths are kept as short as possible. The transmission lines in the signal paths are nearly only exploited for generate the required delay and the layout floorplan is made compact. For the same reason, good isolation between the left and right delay paths is achieved by an active power splitter.

Because the group delay variation varies nearly exponentially with the reflection coefficient, it is of utmost importance to make the characteristics of a "loaded transmission line" constant within the frequency of interest. A path-select amplifier with double emitter followers at the input and a cascode stage at the output, are used to periodically load the transmission line and manipulate the length of signal paths. Port impedance analysis of the amplifier shows that the input and output parallel equivalent resistances in "off state" amplifier decrease at the rate of 20dB/dec with frequency. In order to keep the line characteristic impedance constant, the input and output resistance of the amplifier should always be 10 times larger than the capacitive reactance of the lumped capacitor at that location within the bandwidth. The port resistance in the "off state" is inversely proportion to the transistor emitter length. Therefore, keeping the transistors at the input and output nodes small in area can improve the performance of the loaded transmission lines. It was found that the amplifier in the "on state" shows a negative input resistance. Optimization has been performed to raise the absolute value of this resistance to -1.6 kΩ. However, the characteristics of the loaded transmission line may still be affected, as shown in Table 4.2.

In case that the power amplifiers in the three output paths suffer from mismatch, the group delay variations of the power amplifier may also have impact on the delay resolution. As shown in Chapter 4, the group delay of a RC low-pass network reduces by one-half at its -3dB bandwidth. The group delay of our two-stage power amplifier is approximately twice as large as the delay range achieved in the beamformer. Therefore, although the bandwidth of the RF signals in the system is approximately 1 GHz, the bandwidth of the power amplifier must be widened to 10 GHz in order to achieve a flat group delay. Both the gain-bandwidth trade-off in a single stage and the impedance transformation ratio between

stages (which affects the bandwidth of matching network) were considered to achieve the desired bandwidth of 10 GHz.

6.2 Recommendations for Future Work

The design and results presented in this report are a first step towards realizing a beamforming radar system. Based on the results and conclusions of this thesis, following paragraphs summarizes recommendations for the coming testchip tapeout and subsequent future work.

6.2.1 Gain Variations with Different Delay Settings

Due to the lossy transmission lines, the gain difference between the shortest and longest delay paths is around 2 dB, which implies that the formed beam may not have the desired radiation pattern when the incident angle is large. The on-chip microstrip transmission lines provided in the design kit for the BiCMOS technology show less attenuation from simulation. However, better performance cannot be expected from the transmission lines designed in this work due to the trade-off between the impedance, attenuation and area in the transmission line design. A programmable gain power amplifier can be implemented to compensate for the gain loss. A better approach is to make the path-select amplifier in the trombone delay line with different gains. The amplifier in the shorter path has lower gain while the amplifier in the longer path has higher gain. Since the gain of each amplifier is specified individually, the compensation can be perfect in principle. The gain of the path-select amplifier mainly depends on the differential pair, so it is possible to realize the path-select amplifiers with different gains but the same port impedances. From simulation results, it will be difficult to realize higher gain from the path-select amplifier. Therefore, the gain of the amplifier in the shortest path needs to be reduced by 2 dB. The output power can still be preserved by making the amplifier at the input of the chip saturated.

6.2.2 Layout of Power Amplifier

Power amplifier design is iterative in nature. All interconnects may detune the center frequency of the matching network and they must be considered during circuit design. One potential problem arises from the fact that the base bias voltage of the differential pair is fed by an electrically long transmission line. The junction temperature of transistors in the bias circuit and power amplifier may differ, leading to **thermal runaway** [1]. Ballasting resistors placed in series with the base or emitter of the amplifying transistors can solve this problem, but the RF performance of the power amplifier (e.g., gain and output power) is traded-off for reliability. Reference [2] uses a folded transmission line and the bias is fed through the center tap. In this case, the bias circuit may be placed near the amplifier. Although the differential topology of the power amplifier avoids the effect of inductive reactance in the ground plane to some extent, this inductive reactance can still affect the circuit in large-signal operation. Reference [3] recommends that all ground nodes in the power amplifier be connected internally before connecting them to an external ground. If the amplifier sees the same internal ground node, performance can be less affected by the length (and hence parasitic inductance) of the ground path. In addition, it is also essential to consider power distribution, local decoupling capacitors and isolation rings during layout.

6.2.3 Modulation scheme

Pulse modulation scheme was adopted for this work. The main supporting reason is that the isolation between the transmitter and receiver via time duplexing is provided by this scheme. Otherwise, a circulator has to be inserted between the antenna and transceiver for isolation. An off-chip circulator may complicate the board-level floorplan, since the spacing between antennas is only 2.5 mm. There are scarce publications about circulators implemented on silicon ICs. Even if it is possible to make on-chip circulators, the isolation between two ports is probably less than 25 dB.

In this design, the output impedance of the power amplifier is unmatched to the transmission line impedance at the output for the required output power. It is usually not a problem in most applications when the line impedance matches the antenna impedance [4].

However, output mismatch will increase the group delay variations, so additional isolation (e.g., via an isolator) may be required. To implement a passive isolator has the same problem as to implement a circulator. It is also not practical to insert active switches at the output of power amplifier at 60 GHz. If an appropriate solution cannot be found, the match between antenna and the routing transmission lines must be taken care of.

If an on-chip circulator is possible, then a pseudo-random number modulation scheme can also be considered. One of the advantages is that only one stage power amplifier is able to satisfy the specification. The group delay variation can be reduced and will not have impact on the delay resolution of the beamformer.

6.2.4 Two-dimensional Beamformer

A 5-path two-dimensional beamformer can be extended based on the 3-path one described in this thesis, by adding another two paths. However, the board-level floorplan will be more complicated. One possible solution is to mount the chip on one side of the board (e.g., top) and place the antennas on the other side of the board (i.e., bottom). Signal lines may then be routed with sufficient space to make the line lengths between bondpad and antenna equal. The feasibility of this approach needs to be verified. The implementation of the antenna is a subject for future work in beamforming transceiver development.

Chapter 2 describes the radiation pattern of one-dimensional beamformer, which assumes that the delays between all of the neighboring paths are equal and equal output power is generated in each path. However, this is not the case in a two-dimensional beamformer. Figure 6.1(a)-6.1(c) show that the delay between different paths depends on not only the incident angle, but also the direction the radar is scanning. Besides, if each path still generates the same output power, the desired radiation pattern may not be obtained. As shown in Figure 6.1 (a), there are three elements in the middle but only one element in the upper and downer sides, respectively. It is better for elements in the middle to generate less power in order to form the desired beam. Therefore, a look-up table is needed to program the delay and output power according to the desired direction, as well as incident angle.

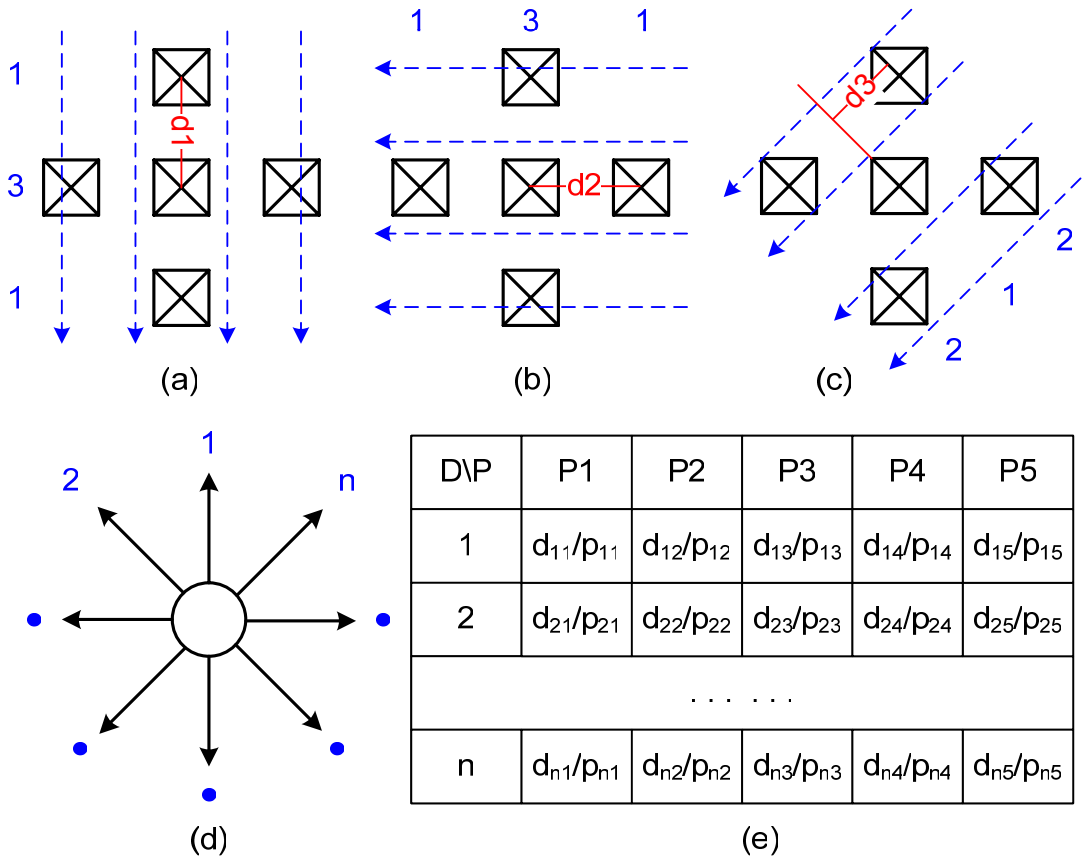

Figure 6.1: In different directions, (a-c) the delay between neighboring paths and the transmit power required by each path are different; (d-e) look-up table is required to configure the output power and delay of each path.

6.2.5 UWB Beamforming Transceiver

It is preferable to integrate the transmitter and receiver on the same chip, especially for the radar system. Figure 6.2 proposes a potential solution. Two-way path-select amplifiers are used so that the trombone delay line can be shared by the transmitting and receiving signal paths. The transmission lines in the center path can be saved and the center path can reuse the left and right delay paths. Local signal combining technique [5] can be exploited to make it work. However, in order to minimize group delay variations, it is better to make a separate center path. With the transmission line structure used in this thesis, it is estimated that the chip area will be increased by less than 0.05 mm^2. The delay resolution is degraded

by applying two-way path-select amplifiers. However, 2 or 3 ps delay resolution is still acceptable for the indoor presence detection applications.

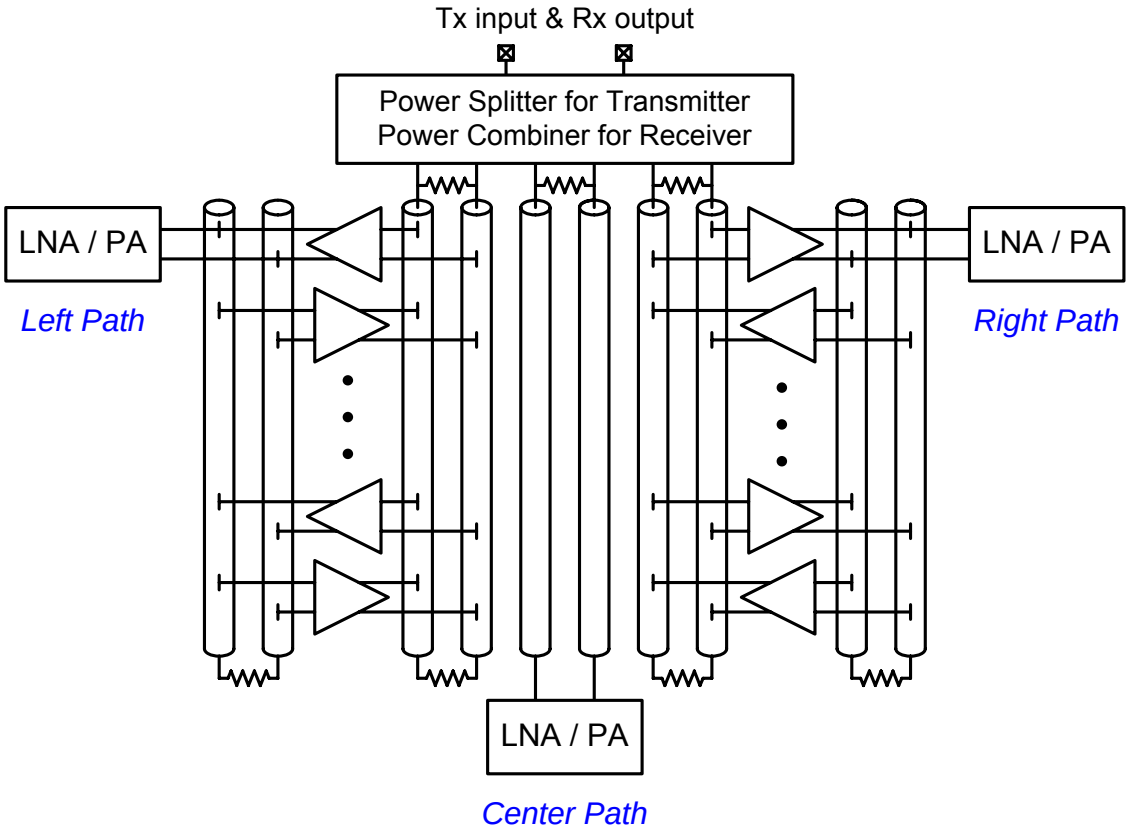

Figure 6.2: Simplified diagram of the beamforming transceiver.

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