EMC oriented ISR design

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Abstract

Electromagnetic Compatibility (EMC) is a growing issue in the automotive industry. Integrated Circuits (IC's) must adhere to strict Electromagnetic Emission (EME) and Electromagnetic Susceptibility (EMS) regulations to ensure safety in the automotive vehicle. The Internal Supply Regulator (ISR) plays a critical role in the EMC performance of an IC.

In this thesis, four types of linear regulator topologies are defined, based on the output stage: NMOS series, PMOS series, NMOS shunt, and PMOS shunt. Several important parameters are defined to describe the performance of a regulator. These are used to compare the four topologies. Only shunt regulators were found able to have good performance in both emission and Power Supply Rejection (PSR). Unfortunately, they come with some disadvantages, especially in power efficiency.

A dual loop concept is proposed in order to alleviate these disadvantages. The concept is analyzed on system level and specifications are determined for the system blocks. The system blocks were then implemented on circuit level. Simulations have been performed on each system block. They confirm an improvement in terms of emission and PSR compared to the ISR that is currently used within NXP. Especially the performance in emission shows great improvement; The attenuation for all frequencies in the band of interest is approximately 30dB. A power efficiency that is only slightly larger than the series topologies has been achieved.

Acknowledgements

I would like to thank a number of people who have helped me through the challenging process of research and writing this thesis. The rough circumstances in my personal life has made your support more important than ever.

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Last but not least, my dear family, who give me courage, love and full support. I will always keep you with me.

Contents

List of Abbreviations

A-BCD	Advanced Bipolar CMOS DMOS. A process used in the NXP automotive branch. This work has also been implemented in the A-BCD process.
CRL	Current Regulation Loop. The feedback loop that regulates the DC quiescent current (I_Q) to a certain reference current (I_{REF}).
ECU	Engine Control Unit. Electrical unit inside the automotive vehicle that interfaces between the sensors and the engine.
EMC	Electromagnetic Compatibility. The situation where multiple electronic devices can function in the same environment without disturbing one another.
EME	Electromagnetic emission. Radiation caused by varying currents inside a conductive object.
EMI	Electromagnetic interference. Interferences that propagate through non-conductive materials as electromagnetic radiation. Can be picked up by other circuits and reduce their performance.
EMS	Electromagnetic susceptibility. The vulnerability of an electric circuit towards EMI.
GBW	Gain-Bandwidth. The gain of an amplifier multiplied by its bandwidth is a commonly used parameter to describe speed performance.
GO	Used when referring to the Gate Oxide capacitor. This type of capacitor makes use of the capacitance between the poly silicon gate and the substrate.
HV domain	High Voltage domain. Circuit domain where the supply voltage exceeds 1.8V.
ISR	Internal Supply Regulator. Circuit block that converts the external supply voltage to an on chip supply voltage.
KCL	Kirchoffs Current Law. Basic law stating that the amount of current going in to a circuit node must be equal to the amount of current going out of that node.
LP product	Loopgain Poles product. Product of the loop gain and poles within a feedback loop. This product can be used to estimate the bandwidth capabilities of the loop.

LV domain	Low voltage domain. Circuit domain where the supply voltage does not exceed 1.8V.
MIM capacitor	Metal-Insulator-Metal capacitor. A type of capacitor that utilizes the capacitance between two metal layers.
PSR	Power Supply Rejection. Small signal gain from the supply voltage to the output node of the regulator.
PWM	Pulse Width Modulator. A circuit block that converts an analog input signal to a digital pulse width modulated output.
SOI technology	Silicon on Insulator technology. Technology where the bulk of the silicon wafer is separated from the thin top layer by an oxide layer. Has the advantage that certain areas on the wafer may be isolated using STI.
TA	Transconductance Amplifier. Amplifier that has a voltage input and a current output.
UGF	Unity Gain Frequency. The frequency at which the gain is equal to unity.
VRL	Voltage Regulation Loop. The feedback loop that regulates the output voltage to a voltage proportional to a bandgap reference.

Chapter 1

Introduction

In the early days of the automotive industry, most systems where realized mechanically as electronic solutions were found too unreliable. The large boost in the IC industry has made it possible to make electrical systems more reliable with decreased manufacturing costs. The modern car is now equipped with a large number of smart sensors, some even fulfilling critical functions. For example, sensors are used in: engine control, brake control, tire pressure monitoring, transmission, and much more [3]. Some of these sensors can be located close to the engine or to the brakes, therefore they need to work in very harsh environment conditions: e.g. in contact with chemicals or in a wide temperature range spanning from -40°C up to 175°C. Furthermore components that are supplied from the car battery have to deal with large supply variations caused by e.g. cold cranking, ignition switch bounce, load dumps or other effects [1].

1.1 Problem statement

Sensors in the automotive vehicle are connected to the Engine Control Unit (ECU) by cable. These cables can reach lengths up to three meters and will emit and radiate electromagnetic fields. As the number of sensors in a single vehicle is increasing and the automotive safety requirements are harsh, Integrated Circuit (IC) designers face a challenging Electromagnetic Compatibility (EMC) problem.

1.1.1 Goal

The Internal Supply Regulator (ISR) is a circuit block that plays a key role in the EMC behavior of the IC. However, in a lot of ISR designs, the emphasis is on other specifications, e.g. power efficiency or drop-out voltage. EMC is often considered in the final phase of the design and adjustments are made if the requirements are not met.

The goal of this thesis is to increase the EMC performance of the ISR by considering EMC in an early stage of the design phase. The use of an external capacitor is undesired as it would substantially increase the total cost and size of the product. The ISR that is being used in the KMA3xx angular sensor family is chosen as a reference for performance.

1.1.2 Scope

The scope of this thesis is the design of an ISR with improved EMC performance. Only the core and startup circuitry of the regulator will be investigated, while other auxiliary circuits are not implemented or ported from the reference design. Examples of parts that will not be investigated are: the bandgap reference, circuits for testability, and calibration circuits. The bandgap reference of the reference design was re-used during the design of the new ISR.

The design is implemented in the Advanced Bipolar CMOS DMOS (A-BCD) process which is a Silicon On Insulator (SOI) technology supporting High Voltage (HV) applications. Table 1.1 shows the most interesting features of the process.

Specification	**CMOS14 A-BCD**
Minimum feature size	0.14μm
Handle wafer	SOI
Metal layers	5
Metal type	Aluminum
Gate Oxide thickness 1	2.9nm
Gate Oxide thickness 2	7.2nm
Vias	Tungsten
Shallow Trench Isolation	yes
Medium Trench Isolation	yes
MIM capacitors	yes

Table 1.1: Specifications of the A-BCD process.

1.2 EMC in IC's

Before beginning to investigate proper design for EMC in the ISR, some fundamental knowledge about EMC in IC's is necessary. EMC can be described as the situation in which several electronic devices can operate simultaneously without affecting each others functionality. The need for EMC is caused by the existence of Electromagnetic Interference (EMI). In order to achieve an electromagnetic compatible situation, devices must conform to a set of rules regarding Electromagnetic Emission (EME) and Electromagnetic Susceptibility (EMS). The relations between these terms are shown in figure 1.1.

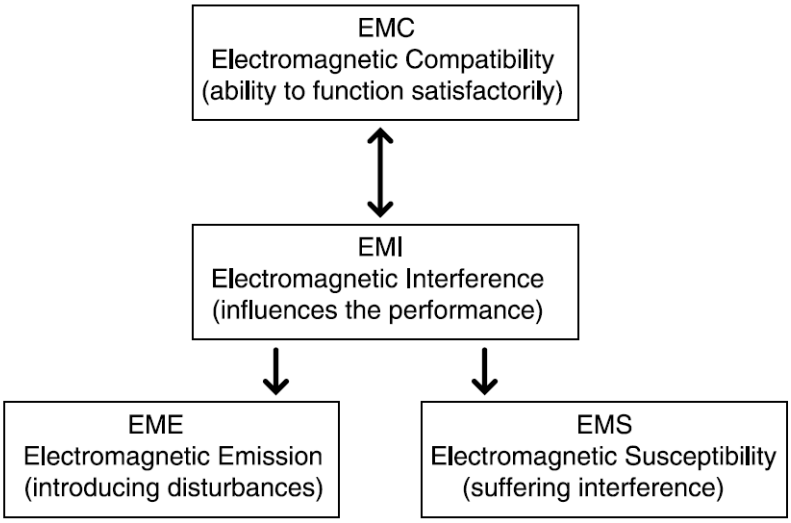

Figure 1.1: Interrelationships in EMC [5]

All conductive objects can both emit and radiate electromagnetic fields and thus behave as an antenna. The measure in which a conductive object will act as an antenna is dependent on the so called 'electrical length'.

$$Electrical \quad length = \frac{L}{\lambda} = \frac{fL}{c} \tag{1.1}$$

Conductors that have an electrical length smaller than $1/20$ or even $1/50$, in case of large impedance mismatches, can be considered to be electrically short [5].

Electrically short conductors can be accurately described by basic circuit theory. For electrically long devices, the effect of electromagnetism needs to be taken into account. Table 1.2 shows the electrical length of a set of relevant conductors in the functional setup of the IC.

It can be seen that for frequencies up to 1GHz, the IC tracks, IC bondwires, package leads and pins may be considered electrically short. The external wiring has a maximum length of 3 meters in the application and must be considered to be electrically long for frequencies above 5MHz.

	Physical length	EMI frequency	Electrical length
IC tracks	10μm-1mm	150kHz 1GHz	0 0-0.003
IC bondwires, package leads, pins	1mm-1cm	150kHz 1GHz	0 0.003-0.03
PCB tracks	1cm-10cm	150kHz 1GHz	0 0.03-0.3
External wiring	10cm-10m	150kHz 1GHz	0-0.005 0.3-30

Table 1.2: The electrical length for several conductive objects in the setup of an IC [5].

Figure 1.2 shows the power supply of the KMA3xx, provided by the ECU. An external capacitor (C_{EXT}) is located inside the package to reduce the EMI picked up and radiated by the power cable.

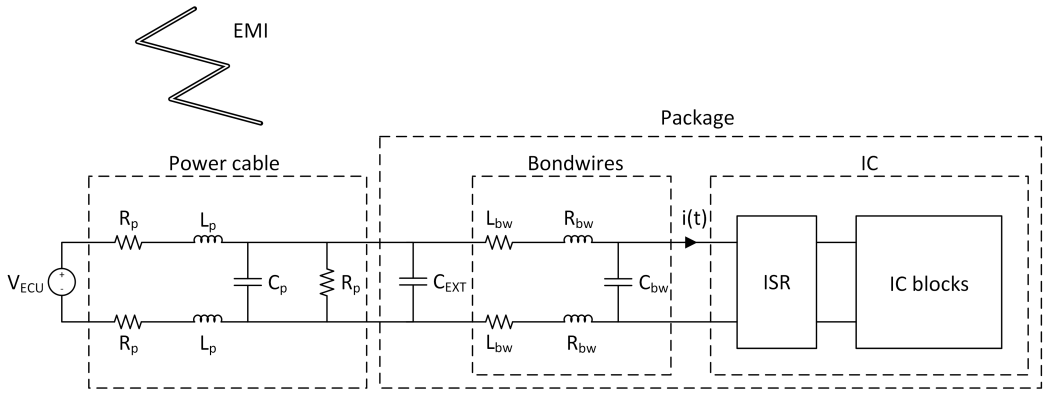

Figure 1.2: Model of the KMA3xx angular sensor connected to the power source through a power cable.

In general, EMI can be further subdivided into three coupling methods:

1. Inductive interference: Interferences that are emitted and radiated through near field coupling are called inductive interferences. A magnetic or electric field is generated on one side and received by an antenna of the same type (a magnetic loop antenna or electric dipole antenna). Examples are crosstalk or the coupling between two magnetic coils.

2. Radiated interference: Interferences that are emitted and radiated through far field coupling are called radiated interferences. An accelerating voltage or current will generate an electric or magnetic field respectively. The generated field will generate a field of the opposite type and radiation occurs. An example is the electromagnetic field while switching a large current on or off.

3. Conducted interference: Interferences that are introduced through coupling by a common impedance are called conducted interferences. Conducted interference happens when two current loops share a common impedance so that the current loops start to interact. An example is the power supply variation due to fast switching digital circuits.

All three types of EMI may be picked up and/or emitted through the power cable. By

limiting the bandwidth of the current going into the ISR (i(t)), all three types of EME can be reduced.

1.3 Introduction to the ISR

In this section, the function of the ISR and its architecture is explained. A comparison is made between linear regulators and switched regulators. Note that an important convention is used to distinguish DC signals from AC signals:

$$V_x = V_X + v_x \tag{1.2}$$

Here V_x is a voltage that contains a DC component, V_X, and an AC component, v_x. This convention is used throughout the thesis.

1.3.1 Function

The function of the ISR is to supply internal blocks in the IC with a stable DC voltage. Its output impedance should be low so that the output voltage is independent on the current drawn from the supply. External interferences should be suppressed.

Digital circuits are in general quite robust against variations on the supply. However, the fast switching nature of digital circuits demand fast peaking load currents from the supply, polluting the supply voltage. Analog circuits, on the other hand, are usually quite sensitive to variations on the supply. As their current consumption is more constant than in digital circuits, they are less polluting. In order to keep the analog supply clean from variations, the analog and digital domains are often isolated by using a separate ISR, .

The ISR must also ensure a proper start-up after a voltage is applied to the supply pins of the IC.

1.3.2 Linear regulators versus switched regulators

Many approaches of designing a voltage regulator exist in literature. A widely accepted way to categorize the voltage regulator is by defining two main categories: linear regulators and switched regulators.

In this section, the architecture of both categories will be discussed and their main advantages and disadvantages will be presented. Both categories make use of a Voltage Regulation Loop (VRL) to regulate the output voltage (V_{out}) to a voltage proportional to a bandgap voltage (V_{REF}).

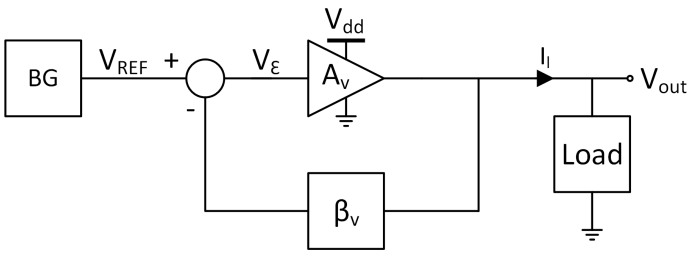

Figure 1.3: Architecture of a linear regulator.

Linear regulator

The basic linear regulator architecture (figure 1.3) consists of a bandgap reference, a voltage amplifier, and a feedback network (β_v).

As the maximum output voltage (V_{out}) of the voltage amplifier is the supply voltage (V_{dd}), the linear regulator is only used to realize a V_{out} that is lower than V_{dd}. To achieve a certain voltage drop from V_{dd} to V_{out}, the minimum amount of dissipated power (P_{MIN}) in the output stage of the voltage amplifier is given by:

$$P_{MIN} = (V_{DD} - V_{OUT})I_L \tag{1.3}$$

This power dissipation results in a lot of heat production and therefore puts a limit on the maximum I_L that can be provided. Also due to this dissipation, the linear regulator is in general not very power efficient.

The simplicity of the design, makes it possible to design the voltage amplifier for high speeds, so that the bandwidth of the VRL may approach the f_t of the technology [6].

Switched regulator

The switched regulator architecture (figure 1.4) utilizes a Pulse Width Modulator (PWM) to drive one or multiple switches that dynamically connect/disconnect energy storage elements (inductors and capacitors) to the circuit.

The use of energy storage elements allows an output voltage (V_{out}) that is higher or lower than the supply voltage (V_{dd}). As the energy storage elements are ideally loss-less, high power efficiency's (between 80% and 95%) can be achieved [6]. Less power is dissipated than in the linear regulator, and so heat production is less of a problem. This makes the switched regulator more suitable for providing large load currents (I_L).

The use of a switch in the output stage, driven by a clocked signal, will cause a voltage ripple at the output. This ripple is often unacceptable for sensitive analog circuits. The switched output stage draws fast transient currents from the supply, i.e. a large bandwidth current. As discussed in section 1.2, this results in unwanted EME.

In order to keep the switched regulator stable, the bandwidth of the VRL must be about a decade below the driving frequency of the PWM (f_{drive}) [6]. Therefore the maximum attainable bandwidth of the VRL lies about a decade below the f_t of the technology.

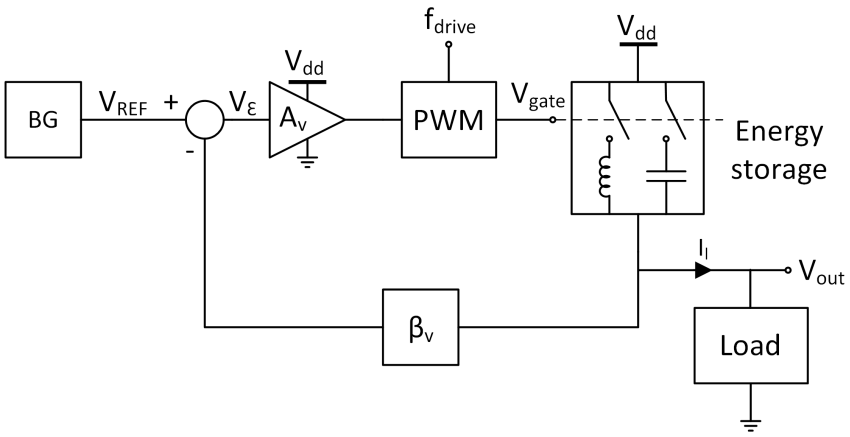

Figure 1.4: Architecture of a switched regulator.

Comparison

Table 1.3 shows the strengths and weaknesses of the two main architectures.

	Linear	**Switched**
Output voltage range	-	+
Power efficiency	-	++
Maximum output power	-	+
EMC	+	–
Output noise	+	-
Bandwidth	+	-
Simplicity	+	-

Table 1.3: Comparison between the switched

The main advantages of the switched regulator architecture are power related. Although power consumption is not negligible in the automotive sensors application, it is not critical. Due to better EMC performance and bandwidth capabilities the focus in this thesis will be on the linear regulator.

1.4 Topologies

As explained in the previous section, generally a lot of power is dissipated in the output stage of the voltage amplifier and so large transistors are required. The characteristics of these transistors are dominant in the performance of the ISR. For this reason the voltage amplifier of figure 1.3 is split into a Transconductance Amplifier (TA) and an output stage (figure 1.5).

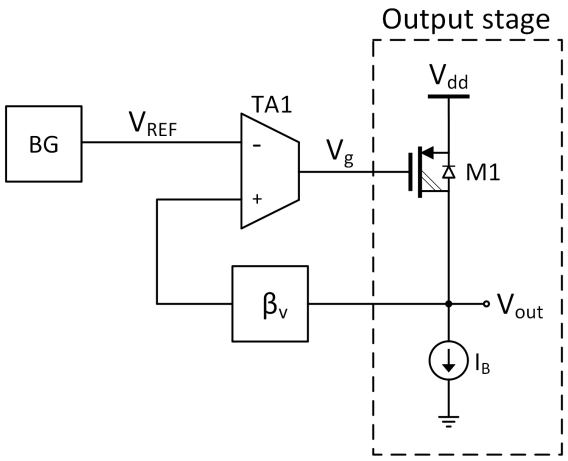

Figure 1.5: Linear regulator topology with the voltage amplifier split into a TA and an output stage.

In figure 1.5, the output stage is a common source amplifier formed by M1 and bias current source I_B. Four possibilities are identified as suitable candidates for an output stage (figure 1.6).

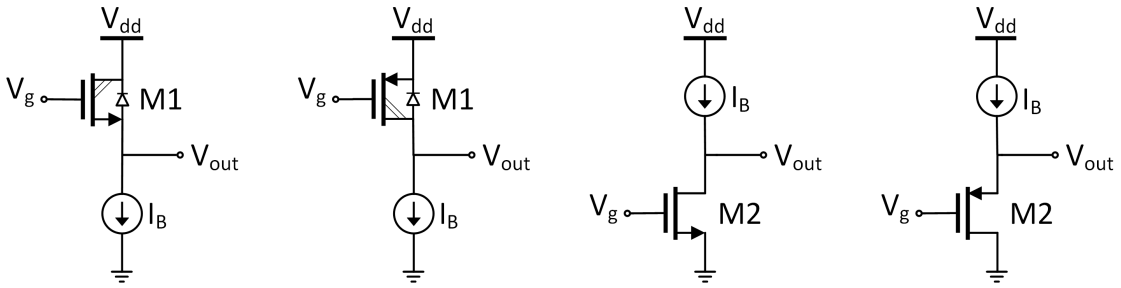

Figure 1.6: The output stages for the four different topologies. From left to right: NMOS series, PMOS series, NMOS shunt, and PMOS shunt.

Topologies where the transistor is located between the supply (V_{dd}) and the output (V_{out}) are referred to as 'series regulators'. If the regulating transistor is located between V_{out} and ground, the regulator is considered a 'shunt regulator'. The four topologies are referred to as NMOS series, PMOS series, NMOS shunt, and PMOS shunt respectively. As the application requires a high breakdown voltage, high side transistors are implemented as HV transistors. The properties of the HV transistor will be discussed in section 1.4.2.

1.4.1 Open loop approach

At low frequencies, the performance of the regulator is mainly dominated by the VRL. After the Unity Gain Frequency (UGF) of the VRL, the loop may be considered to be broken and the performance of the regulator is only determined by the output stage.

In this thesis, an open loop approach is used to be able to compare the performance of the different output stages.

1.4.2 The high voltage transistor

As mentioned in section 1.1, the supply voltage from the car battery can vary due to numerous reasons. Although the ECU provides regulation, the KMA3xx family still needs to withstand supply voltages up to 20V. To meet this requirement, the HV transistor (figure 1.7), available in the A-BCD process, needs to be used.

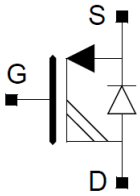

Figure 1.7: Symbol of the HV transistor.

These transistors have an extend drain to enable a maximum V_{DS} of 60V. The downside of this extended drain is that the parasitic overlap capacitance between drain and gate ($C_{GD,ov}$) is substantially large. Body and source are internally connected and so the high voltage transistor must be considered as an unsymmetrical device that has a back-gate diode. Figure 1.8 shows the cross section of a HV PMOS transistor.

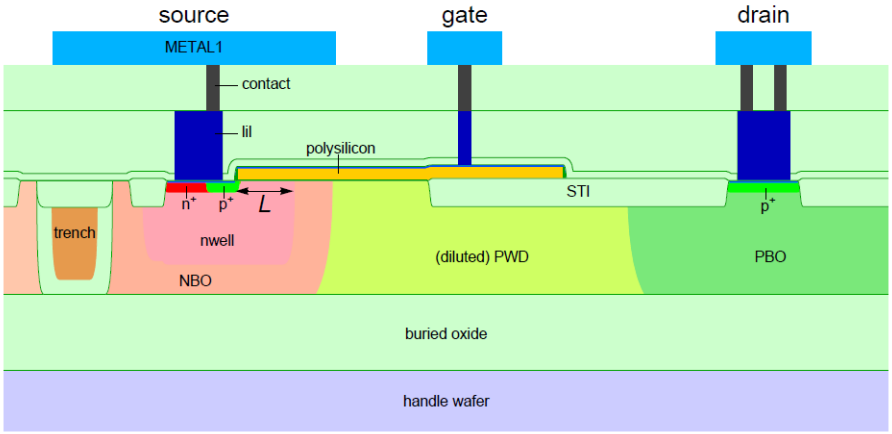

Figure 1.8: Cross section of a HV PMOS transistor.

1.4.3 Non-ideal current source

Until now, the bias current source has been represented by an ideal source. However, the parasitics of the current source are not negligible and need to be taken into account.

In series topologies, the current source is connected in parallel to the output (V_{out}). As the output voltage is kept stable by the VRL, current source I_B can be implemented by a resistor (figure 1.9).

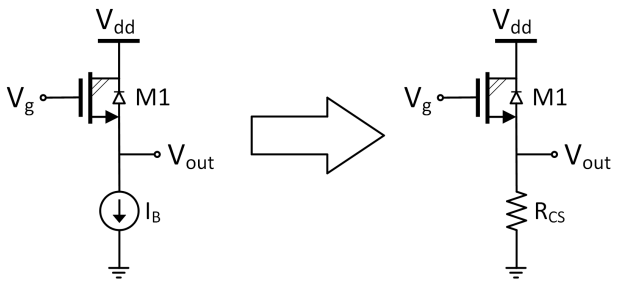

Figure 1.9: Implementation of bias current source I_B in series topologies.

In the shut topologies, the current source is connected to the supply (V_{dd}) and so a HV transistor is necessary to implement the current source. The current source is modeled as in figure 1.10.

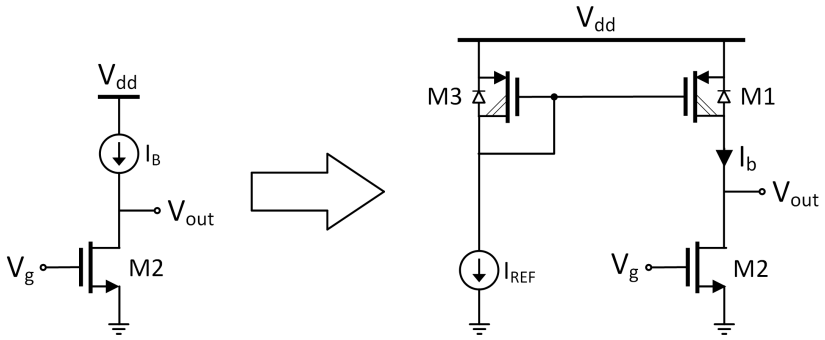

Figure 1.10: Implementation of bias current source I_B in shunt topologies.

The DC reference current (I_{REF}) flows to ground and decreases power efficiency. To avoid a large power loss it must be kept small. In this work, the ratio considered to be acceptable is:

$$I_{REF} = \frac{I_B}{1000} \tag{1.4}$$

It follows that:

$$(W/L)_1 = \frac{(W/L)_3}{1000} \tag{1.5}$$

1.5 Outline of this thesis

In this chapter a problem statement and some background knowledge was given to help understand the research problem. Chapter 2, presents several performance parameters. These are then used to analyze and compare the different topologies. The main focus is on parameters that affect the EMC performance. Based on the findings in chapter 2, a new topology is proposed in chapter 3. The topology is examined on both system level and circuit level. In chapter 4, the simulation results of the proposed topology are shown. Finally a conclusion is given in chapter 5.

Chapter 2

Performance of standard topologies

In this chapter several performance parameters are defined and explained. The parameters described in this chapter are commonly used in literature about linear voltage regulators. Symbolic expressions are found for the performance parameters of the four topologies that were defined in section 1.4. The expressions that were found for the Power Supply Rejection (PSR) and emission are verified by simulation.

In section 2.2, the results of the performance analysis are summarized. A table containing the advantages and disadvantages of eacht topology is presented.

Finally, the architecture of the ISR inside the KMA3xx family is shown in section 2.3.

2.1 Performance parameters

Many parameters exist to characterize the performance of different voltage regulators [2]. The most essential parameters are described in this section.

2.1.1 Power supply rejection

In this section the concept of Power Supply Rejection (PSR) is described and compared by deriving equations. The PSR is an important parameter to indicate the regulators susceptibility to interferences. The resulting equations are verified with simulations.

Description

The PSR is a small signal parameter that represents the circuits capability to suppress a voltage disturbance on the supply line (v_{dd}), to the output (v_{out}).

$$PSR = \frac{\delta v_{dd}}{\delta v_{out}} \tag{2.1}$$

Ideally, v_{out} is totally independent from v_{dd}, resulting in an infinite PSR.

Figure 2.1 shows an example of the PSR of an internally compensated regulator over frequency. The loop gain is shown in red. The curve is divided into three regions [8]:

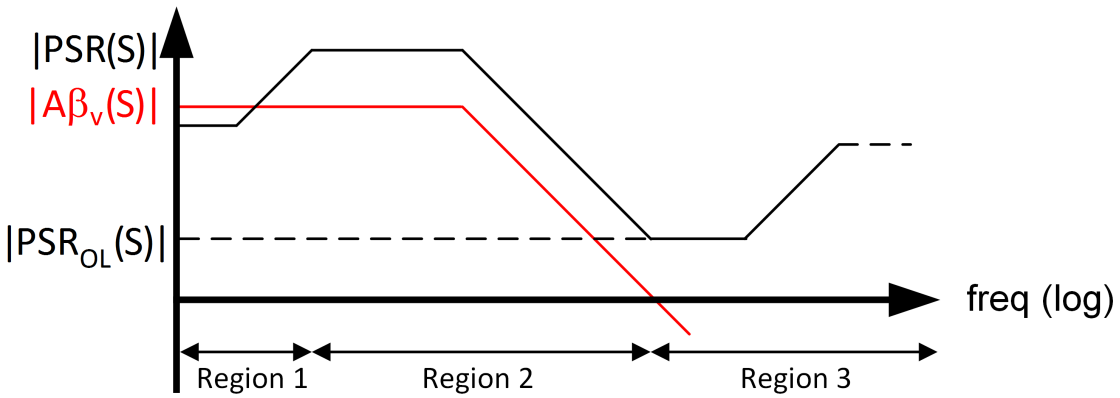

Figure 2.1: Example of a PSR curve for a voltage regulator.

In region 1, the PSR of the bandgap reference (PSR_{BG}) is dominant. Any disturbance seen on the bandgap voltage will be transferred to the output by the closed loop gain. The PSR of the regulator in region 1 (PSR_1) is given by:

$$\begin{aligned} PSR_1 &= \frac{A_v PSR_{BG}(s)}{1 + A(s)\beta_v} \\ &\approx \frac{PSR_{BG}(s)}{\beta_v} \end{aligned} \tag{2.2}$$

The output resistance of a bandgap circuit is in general quite high. The output is usually decoupled by a capacitor, resulting in a zero in PSR_{BG} at low frequency.

The PSR in region 2 (PSR_2) is no longer dominated by PSR_{BG} as its contribution is diminished by the decoupling capacitor. PSR_2 can be described as:

$$PSR_2 = PSR_{OL}[1 + A(s)\beta_v] \approx PSR_{OL}A(s)\beta_v \tag{2.3}$$

Where PSR_{OL} is the PSR of the regulator when the feedback loop would be broken. In region 3, the loop gain drops below unity. The loop can be considered to be broken and the PSR is completely determined by open loop PSR.

$$PSR_3 = PSR_{OL}[1 + A(s)\beta_v] \approx PSR_{OL}(s) \tag{2.4}$$

If the bandgap reference would have been supplied from the output of the regulator (V_{out}) instead of directly from the supply (V_{dd}), PSR_{BG} would be significantly higher and would not be the dominant factor in PSR_1. In this case the total PSR can be given by the single equation:

$$PSR = PSR_{OL}[1 + A(s)\beta_v] \tag{2.5}$$

Comparison

If the loop gain for all topologies is assumed to have an equal bandwidth, the difference in PSR performance is solely determined by PSR_{OL}. Therefore analyzing only the PSR_{OL} of the topologies is sufficient to compare the PSR performance. A thorough bandwidth analysis is done in subsection 2.1.9.

NMOS Series The transistor model of the open loop NMOS series topology is shown in figure 2.2. To increase the EMC performance at high frequencies, decoupling capacitor C_{DEC1} is added to the circuit.

In the NMOS series topology, both the output stage transistor (M1) and the TA must be implemented in the HV domain. The TA has to be supplied from V_{dd}, and thus it requires a high PSR.

In order to calculate the open loop PSR, the circuit is converted to its small signal equivalent (figure 2.3). The small signal load current is replaced by an open as it is not relevant when calculating the PSR.

The open loop PSR can be determined by using Kirchoffs Current Law (KCL) on the v_{out} node of the circuit:

$$i_{dd} = i_{dd,a} + i_{dd,b} = i_q \tag{2.6}$$

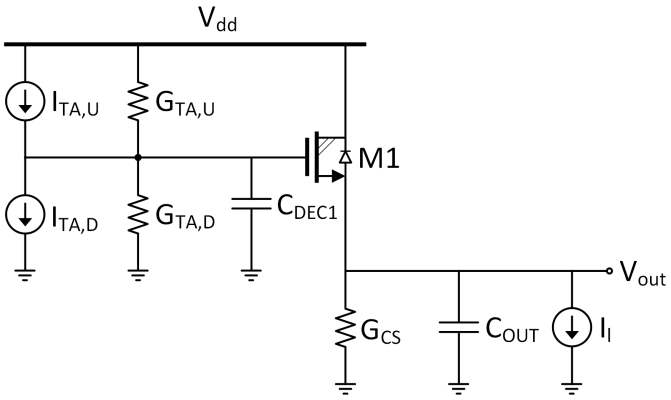

Figure 2.2: Open loop transistor model of the NMOS series regulator.

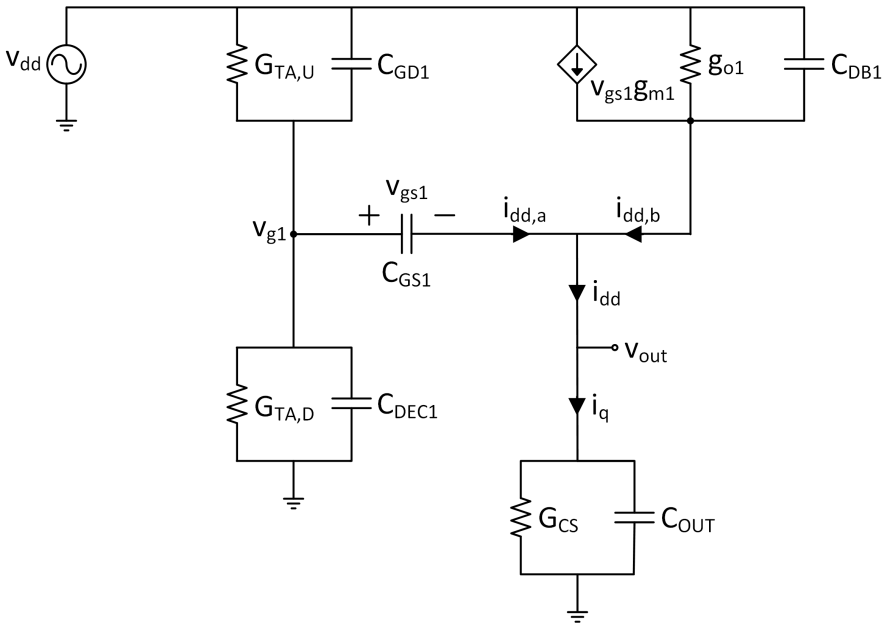

Figure 2.3: Small signal equivalent of the open loop NMOS series model.

In order to express i_{dd} in terms of v_{dd} and v_{out}, an expression for v_{g1} is found by using KCL on the v_{g1} node:

$$\begin{aligned}(v_{dd} - v_{g1})(G_{TA,U} + sC_{GD1}) &= v_{g1}(G_{TA,D} + sC_{DEC1}) + (v_{g1} - v_{out})sC_{GS1} \\ v_{g1} &= \frac{v_{dd}(G_{TA,U} + sC_{GD1}) + v_{out}sC_{GS1}}{G_{TA,U} + G_{TA,D} + s(C_{DEC1} + C_{GD1} + C_{GS1})}\end{aligned} \tag{2.7}$$

The currents are expressed in terms of nodal voltages and admittances:

$$\begin{aligned}i_{dd,a} &= (v_{g1} - v_{out})sC_{GS} \\ i_{dd,b} &= (v_{g1} - v_{out})g_{m1} + (v_{dd} - v_{out})(g_{o1} + sC_{DB1}) \\ i_q &= v_{out}(G_{CS} + sC_{OUT})\end{aligned} \tag{2.8}$$

A second order expression for PSR_{OL} is found by substituting the currents from equation 2.8 into equation 2.6 and substituting v_{g1} by equation 2.7.

$$PSR_{OL} = \frac{N(s)}{D(s)} = \frac{N_1 s^2 + N_2 s + N_3}{D_1 s^2 + D_2 s + D_3} \tag{2.9}$$

To simplify the resulting factors, the approximation is made that: $g_{m1} \gg (g_{o1} + G_{CS})$ and $C_{OUT} \gg (C_{GS1} + C_{DB1})$.

$$\begin{aligned}N_1 &\approx C_{OUT}(C_{DEC1} + C_{GD1} + C_{GS1}) - C_{GS1}^2 \\ N_2 &\approx (G_{TA,U} + G_{TA,D})C_{OUT} + g_{m1}(C_{DEC1} + C_{GD1} + C_{GS1}) - g_{m1}C_{GS1} \\ N_3 &\approx g_{m1}(G_{TA,U} + G_{TA_D}) \\ D_1 &\approx C_{GD1}C_{GS1} + C_{DB1}(C_{DEC1} + C_{GD1} + C_{GS1}) \\ D_2 &\approx g_{m1}C_{GD1} + G_{TA,U}C_{GS1} + (G_{TA,D} + G_{TA,D})C_{DB1} + g_{o1}(C_{DEC1} + C_{GD1} + C_{GS1}) \\ D_3 &\approx g_{m1}G_{TA,U} + g_{o1}(G_{TA,U} + G_{TA,D})\end{aligned} \tag{2.10}$$

PMOS Series The transistor model of the open loop PMOS series topology is shown in figure 2.4. To increase the EMC performance at high frequencies, decoupling capacitor C_{DEC1} is added to the circuit.

In the PMOS series topology, both the output stage transistor (M1) and the TA must be implemented in the HV domain due to the voltage range specification (subsection 1.4.2). To avoid current flow due to a small signal disturbance on the supply (v_{dd}), the signal on the gate of M1 should be identical to v_{dd}. This suggests that the preferred PSR of the TA is unity.

In order to calculate the open loop PSR, the circuit is converted to its small signal equivalent (figure 2.5). The small signal load current is replaced by an open as it is not relevant when calculating the PSR. The gate-source capacitance of M1 (C_{GS1}) adds to the decoupling capacitance (C_{DEC1}) and is not drawn for simplicity.

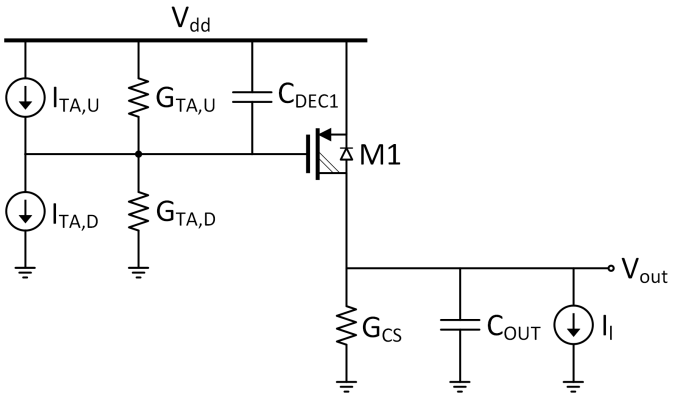

Figure 2.4: Open loop transistor model of the PMOS series regulator.

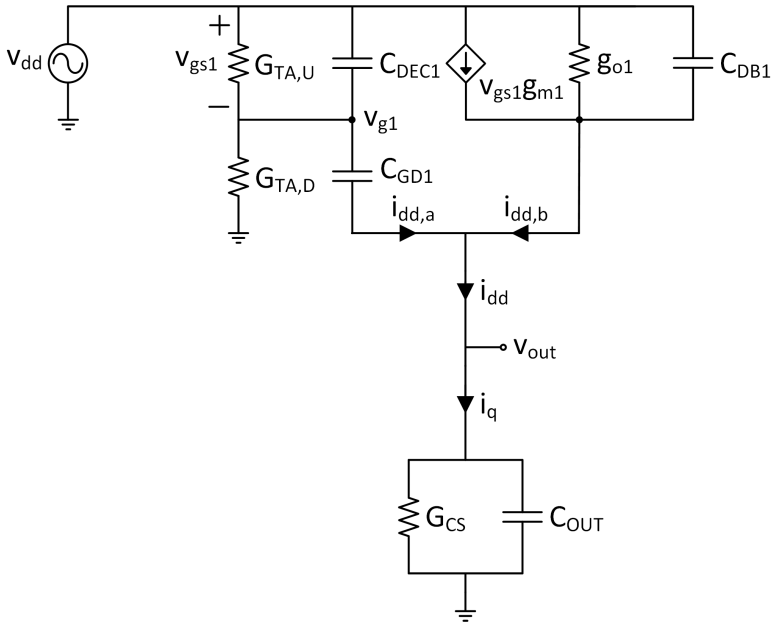

Figure 2.5: Small signal equivalent of the open loop PMOS series model.

The open loop PSR can be determined by using KCL on the v_{out} node of the circuit:

$$i_{dd} = i_{dd,a} + i_{dd,b} = i_q \tag{2.11}$$

In order to express i_{dd} in terms of v_{dd} and v_{out}, an expression for v_{g1} is found by using KCL on the v_{g1} node:

$$\begin{aligned}(v_{dd} - v_{g1})(G_{TA,U} + sC_{DEC1}) &= v_{g1}G_{TA,D} + (v_{g1} - v_{out})sC_{GD1} \\ v_{g1} &= \frac{v_{dd}(G_{TA,U} + sC_{DEC1}) + v_{out}sC_{GD1}}{G_{TA,U} + G_{TA,D} + s(C_{DEC1} + C_{GD1})}\end{aligned} \tag{2.12}$$

The currents are expressed in terms of nodal voltages and admittances:

$$\begin{aligned}i_{dd,a} &= (v_{g1} - v_{out})sC_{GD1} \\ i_{dd,b} &= (v_{dd} - v_{g1})g_{m1} + (v_{dd} - v_{out})(g_{o1} + sC_{DB1}) \\ i_q &= v_{out}(G_{CS} + sC_{OUT})\end{aligned} \tag{2.13}$$

A second order expression for PSR_{OL} is found by substituting the currents from equation 2.13 into equation 2.11 and substituting v_{g1} by equation 2.12.

$$PSR_{OL} = \frac{N(s)}{D(s)} = \frac{N_1 s^2 + N_2 s + N_3}{D_1 s^2 + D_2 s + D_3} \tag{2.14}$$

To simplify the resulting factors, the approximation is made that: $g_{m1} \gg (G_{TA,U} + G_{TA,D})$ and $C_{OUT} \gg C_{DB1}$.

$$\begin{aligned}N_1 &\approx C_{DEC1}C_{GD1} + C_{OUT}(C_{DEC1} + C_{GD1}) \\ N_2 &\approx g_{m1}C_{GD1} + (g_{o1} + G_{CS})(C_{DEC1} + C_{GD1}) + (G_{TA,U} + G_{TA,D})C_{OUT} \\ N_3 &\approx (g_{o1} + G_{CS})(G_{TA,U} + G_{TA,D}) \\ D_1 &\approx C_{DEC1}C_{GD1} + C_{DB1}(C_{DEC1} + C_{GD1}) \\ D_2 &\approx g_{m1}C_{GD1} + G_{TA,U}(C_{DB1} + C_{GD1}) + G_{TA,D}C_{DB1}) \\ D_3 &\approx g_{m1}G_{TA,D}\end{aligned} \tag{2.15}$$

NMOS Shunt The transistor model of the open loop NMOS shunt topology is shown in figure 2.6. To increase the EMC performance at high frequencies, two decoupling capacitances are added to the circuit: C_{DEC1} and C_{DEC2}.

In the NMOS shunt topology, both the output stage transistor (M2) and the TA can be implemented in the low voltage (LV) domain. The current source must be implemented in the HV domain due to the voltage range specification (subsection 1.4.2). The TA may be supplied from V_{out}, relaxing its requirement to have a high PSR.

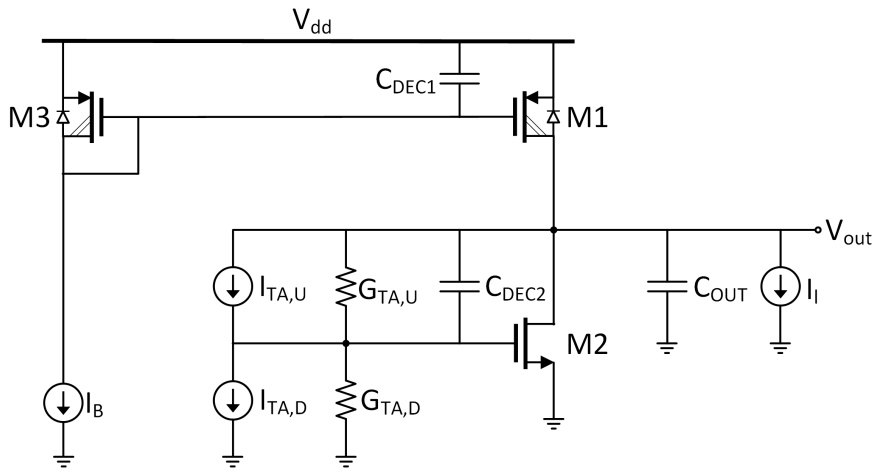

Figure 2.6: Open loop transistor model of the NMOS shunt regulator.

In order to calculate the open loop PSR, the circuit is converted to its small signal equivalent (figure 2.7). The small signal load current is replaced by an open as it is not relevant when calculating the PSR. The gate-source capacitance of M1 (C_{GS1}) and gate-drain capacitance of M2 (C_{GD2}) add to the decoupling capacitances (C_{DEC1} and C_{DEC2} respectively) and are not drawn for simplicity. The drain-bulk capacitance of M2 (C_{DB2}) is in parallel to the output capacitance (C_{OUT}) and is neglected.

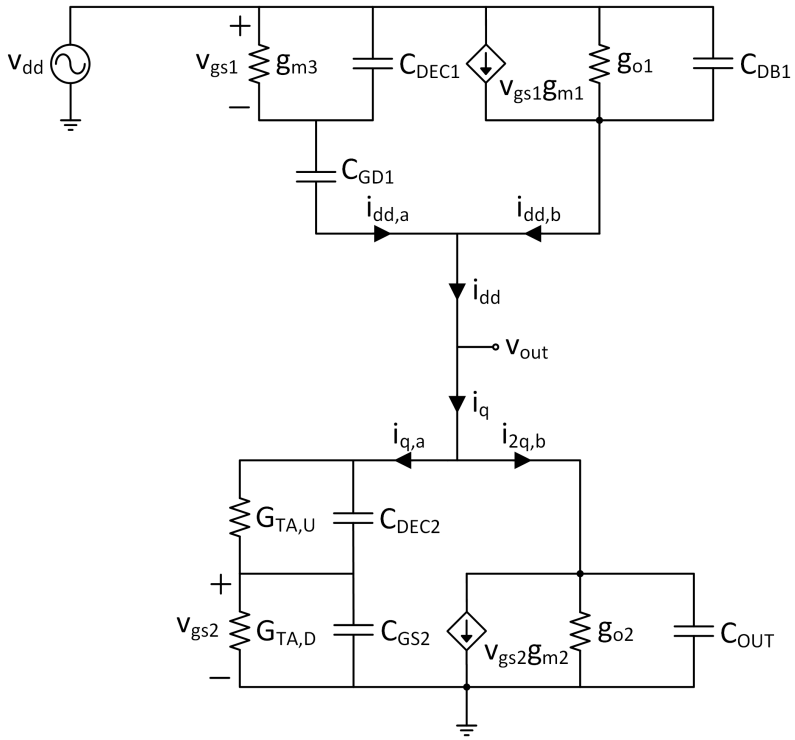

Figure 2.7: Small signal equivalent of the open loop NMOS shunt model.

The open loop PSR can be determined by using KCL on the v_{out} node of the circuit:

$$i_{dd} = i_{dd,a} + i_{dd,b} = i_q = i_{q,a} + i_{q,b} \tag{2.16}$$

The currents are expressed in terms of nodal voltages and admittances:

$$\begin{aligned} i_{dd,a} &= (v_{dd} - v_{out})Y_{dd,a} \\ i_{dd,b} &= (v_{dd} - v_{out})Y_{dd,b} \\ i_{q,a} &= v_{out}Y_{q,a} \\ i_{q,b} &= v_{out}Y_{q,b} \end{aligned} \tag{2.17}$$

The admittances can be easily seen from the circuit:

$$\begin{aligned} Y_{dd,a} &= \frac{sC_{GD1}(g_{m3} + sC_{DEC1})}{g_{m3} + s(C_{GD1} + sC_{DEC1})} \\ Y_{dd,b} &= \frac{sC_{GD1}}{g_{m3} + s(C_{DEC1} + C_{GD1})}g_{m1} + g_{o1} + sC_{DB1} \\ Y_{q,a} &= \frac{(G_{TA,U} + sC_{DEC2})(G_{TA,D} + sC_{GS2})}{G_{TA,U} + G_{TA,D} + s(C_{DEC2} + C_{GS2})} \\ Y_{q,b} &= \frac{G_{TA,U} + sC_{DEC2}}{G_{TA,U} + G_{TA,D} + s(C_{DEC2} + C_{GS2})}g_{m2} + g_{o2} + sC_{OUT} \end{aligned} \tag{2.18}$$

An expression for PSR_{OL} is found by substituting the currents from equation 2.17 into equation 2.16:

$$PSR_{OL} = \frac{\delta v_{dd}}{\delta v_{out}} = \frac{Y_{dd,a} + Y_{dd,b} + Y_{q,a} + Y_{q,b}}{Y_{dd,a} + Y_{dd,b}} \tag{2.19}$$

PMOS Shunt The transistor model of the open loop PMOS shunt topology is shown in figure 2.8. To increase the EMC performance at high frequencies, two decoupling capacitances are added to the circuit: C_{DEC1} and C_{DEC2}.

In the PMOS shunt topology, both the output stage transistor (M2) and the TA can be implemented in the LV domain. The current source must be implemented in the HV domain due to the voltage range specification (subsection 1.4.2). The TA may be supplied from V_{out}, relaxing its requirement to have a high PSR.

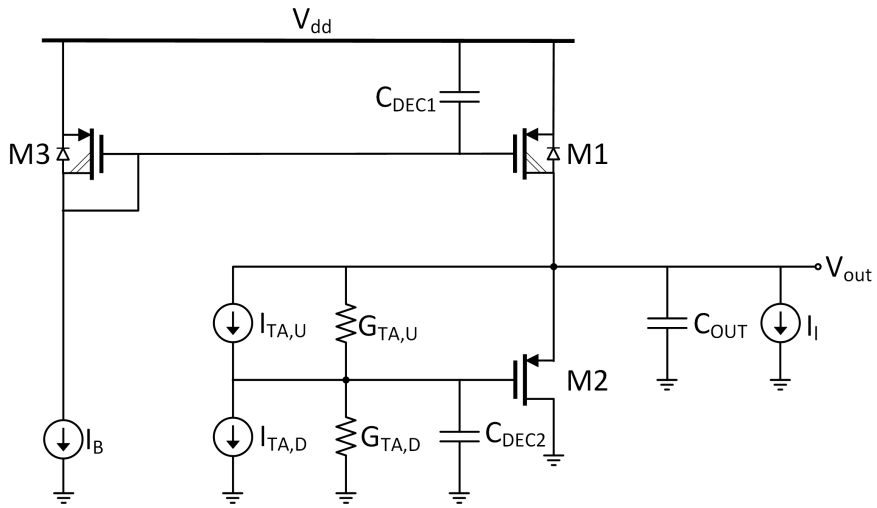

Figure 2.8: Open loop transistor model of the PMOS shunt regulator.

In order to calculate the open loop PSR, the circuit is converted to its small signal equivalent (figure 2.9). The small signal load current is replaced by an open as it is not relevant when calculating the PSR. The gate-source capacitance of M1 (C_{GS1}) and gate-drain capacitance of M2 (C_{GD2}) add to the decoupling capacitances (C_{DEC1} and C_{DEC2} respectively) and are not drawn for simplicity. The drain-bulk capacitance of M2 (C_{DB2}) is in parallel to the output capacitance (C_{OUT}) and is neglected.

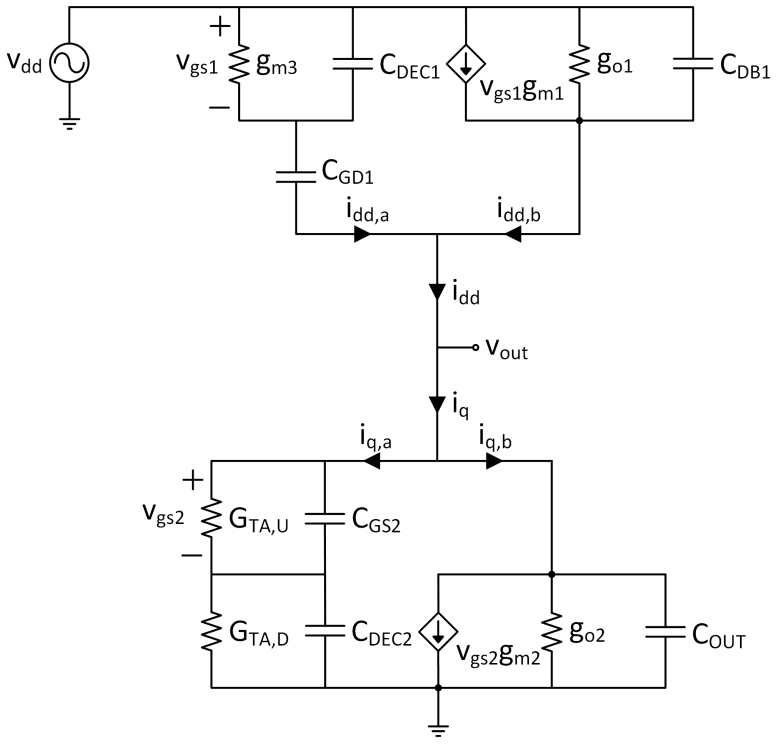

Figure 2.9: Small signal equivalent of the open loop PMOS shunt model.

The open loop PSR can be determined by using KCL on the v_{out} node of the circuit:

$$i_{dd} = i_{dd,a} + i_{dd,b} = i_q = i_{q,a} + i_{q,b} \tag{2.20}$$

The currents are expressed in terms of nodal voltages and admittances:

$$\begin{aligned} i_{dd,a} &= (v_{dd} - v_{out})Y_{dd,a} \\ i_{dd,b} &= (v_{dd} - v_{out})Y_{dd,b} \\ i_{q,a} &= v_{out}Y_{q,a} \\ i_{q,b} &= v_{out}Y_{q,b} \end{aligned} \tag{2.21}$$

The admittances can be easily seen from the circuit:

$$\begin{aligned} Y_{dd,a} &= \frac{sC_{GD1}(g_{m3} + sC_{DEC1})}{g_{m3} + s(C_{GD1} + sC_{DEC1})} \\ Y_{dd,b} &= \frac{sC_{GD1}}{g_{m3} + s(C_{DEC1} + C_{GD1})}g_{m1} + g_{o1} + sC_{DB1} \\ Y_{q,a} &= \frac{(G_{TA,U} + sC_{GS2})(G_{TA,D} + sC_{DEC2})}{G_{TA,U} + G_{TA,D} + s(C_{DEC2} + C_{GS2})} \\ Y_{q,b} &= \frac{G_{TA,D} + sC_{DEC2}}{G_{TA,U} + G_{TA,D} + s(C_{DEC2} + C_{GS2})}g_{m2} + g_{o2} + sC_{OUT} \end{aligned} \tag{2.22}$$

An expression for PSR_{OL} is found by substituting the currents from equation 2.21 into equation 2.20:

$$PSR_{OL} = \frac{\delta v_{dd}}{\delta v_{out}} = \frac{Y_{dd,a} + Y_{dd,b} + Y_{q,a} + Y_{q,b}}{Y_{dd,a} + Y_{dd,b}} \tag{2.23}$$

Model verification

The open loop PSR has been simulated using the transistor models from the A-BCD9 library. DC feedback was used to bias the output stage. The circuits used for simulation can be found in the appendix B. The small signal parameters of the circuit are shown in table 2.1.

The parameters are directly mapable to the small signal circuits from section 2.1.1 and can be used to verify the equations with the simulated models. Figure 2.10 shows the equations for the open loop PSR versus the simulated open loop PSR.

	Shunt		Series	
	NMOS	**PMOS**	**NMOS**	**PMOS**
$(W/L)_1$	3000/0.75	3000/0.75	1000/0.75	3000/0.75
$(W/L)_2$	200/0.16	600/0.16	N.A.	N.A.
g_{m1}	38.4mS	38.4mS	34.9mS	28.5mS
g_{m2}	32.7mS	31.3mS	N.A.	N.A.
g_{m3}	91.3μS	91.3μS	N.A.	N.A.
g_{o1}	6.9μS	6.9μS	3.4μS	3.7μS
g_{o2}	1.4mS	1.2mS	N.A.	N.A.
G_{CS}	N.A.	N.A.	1μS	1μS
C_{DB1}	383.9fF	383.9fF	190.8fF	383.3fF
C_{DEC1}	10pF	10pF	10pF	10pF
C_{DEC2}	1pF	1pF	N.A.	N.A.
C_{GD1}	1.4pF	1.2pF	569fF	1.1pF
C_{GS1}	8.6pF	8.6pF	3.6pF	8.5pF
C_{GS2}	0	0	N.A.	N.A.
C_{OUT}	100pF	100pF	100pF	100pF
I_L	5mA	5mA	5mA	5mA

Table 2.1: Values of the small signal parameters during simulation.

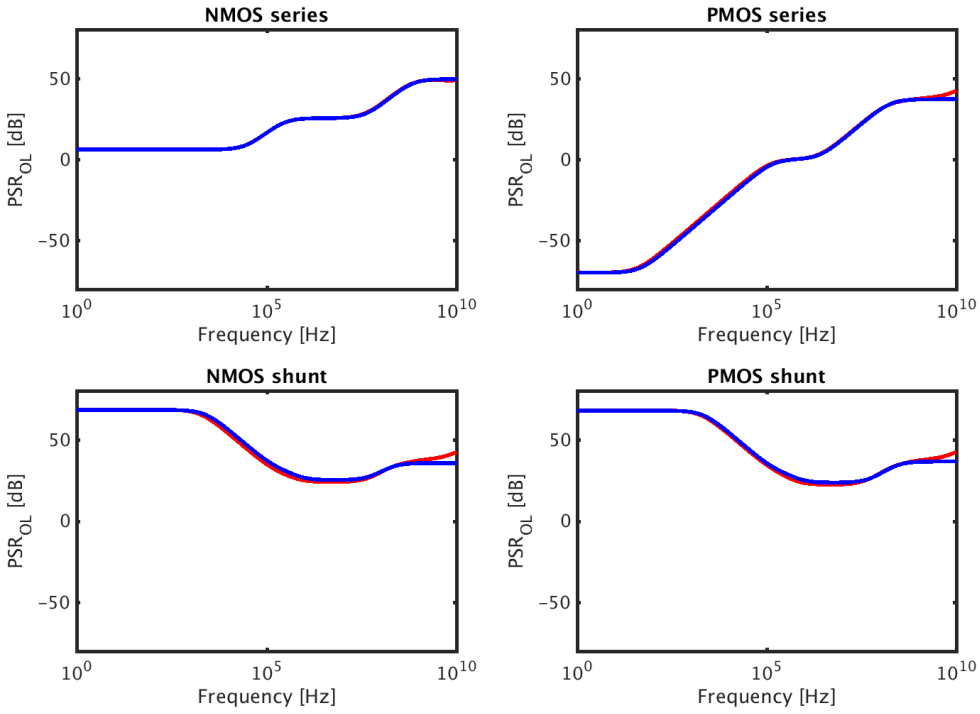

Figure 2.10: The simulated PSR_{OL} using the transistor models (blue) versus the calculated equation for the PSR_{OL} (red).

It can be seen that the transistor models show a zero at frequencies beyond 1GHz that is not included in the equations. This zero is caused by the finite drain resistance of the HV PMOS transistor in all topologies except for the NMOS series topology. Aside from this high frequency zero, the simulations match the equations quite well.

2.1.2 Emission

The analysis of emission is treated in the same manner as the PSR in the previous section. The emission is an important parameter to indicate how much the ISR is able to suppress interference caused by the load current.

Description

Emission is a small signal parameter that represents the change in current on the supply line (i_{dd}) if a change in load current (i_l) occurs. The emission is defined as:

$$Emission = \frac{\delta i_{dd}}{\delta i_l} \tag{2.24}$$

Ideally only the DC component of the load current is delivered from the supply node, resulting in zero emission. The influence of the VRL on emission is different for series and shunt regulators. This is due to the fact the the VRL increases the conductance seen to V_{dd} for series regulators and to ground for shunt regulators (figure 2.11).

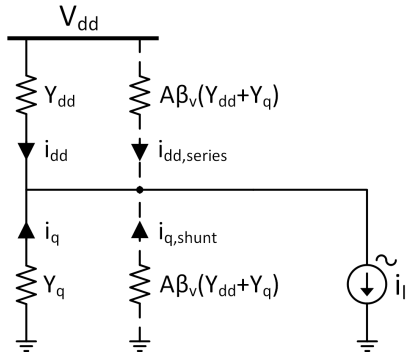

Figure 2.11: The VRL of the series or shunt topology result in a different conductance to ground.

Figure 2.12 shows an example of an emission response over frequency for a series regulator.

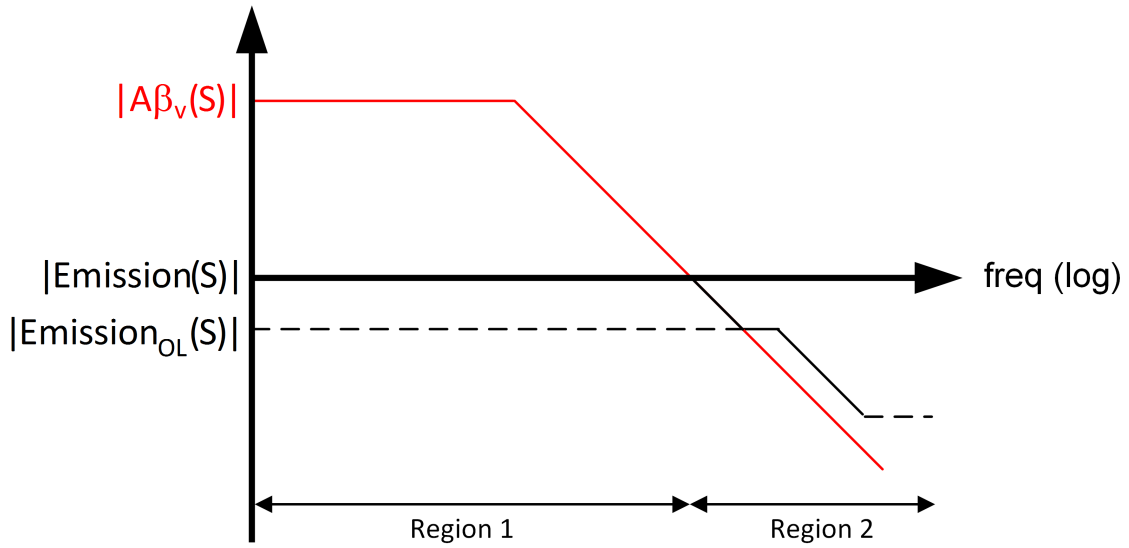

Figure 2.12: Example of an emission curve for a series regulator.

It can be seen that the regulation loop decreases the emission performance for a series regulator.

In region 1 the emission is mainly determined by the gain of the VRL. The VRL forces most of i_l to flow from $i_{dd,series}$. The emission in this region ($Emission_1$) is given by:

$$Emission_1(s) = \frac{Y_{dd} + (Y_{dd} + Y_q)A(s)\beta_v}{(Y_{dd} + Y_q)(1 + A(s)\beta_v)} \approx 1 \tag{2.25}$$

In region 2, the gain of the VRL drops below unity. The VRL can considered to be broken and the emission is completely determined by the open loop emission.

$$Emission_2(s) = \frac{Y_{dd} + (Y_{dd} + Y_q)A(s)\beta_v}{(Y_{dd} + Y_q)(1 + A(s)\beta_v)} \approx \frac{Y_{dd}}{Y_{dd} + Y_q} \approx Em_{OL} \tag{2.26}$$

Figure 2.13 shows an example of an emission response over frequency for a shunt regulator.

In contrast to the series regulator, the VRL increases the emission performance for a shunt regulator.

In region 1 the emission is mainly determined by the open loop emission and the gain of the VRL. The VRL forces most of i_l to flow from the parallel current branch ($i_{q,shunt}$).

$$Emission_1 = \frac{Y_{dd}}{(Y_{dd} + Y_q)[1 + A(s)\beta_v]} \approx \frac{Em_{OL}}{A(s)\beta_v} \tag{2.27}$$

In region 2, the loop gain drops below unity. The loop can be considered to be broken and the emission is completely determined by open loop emission.

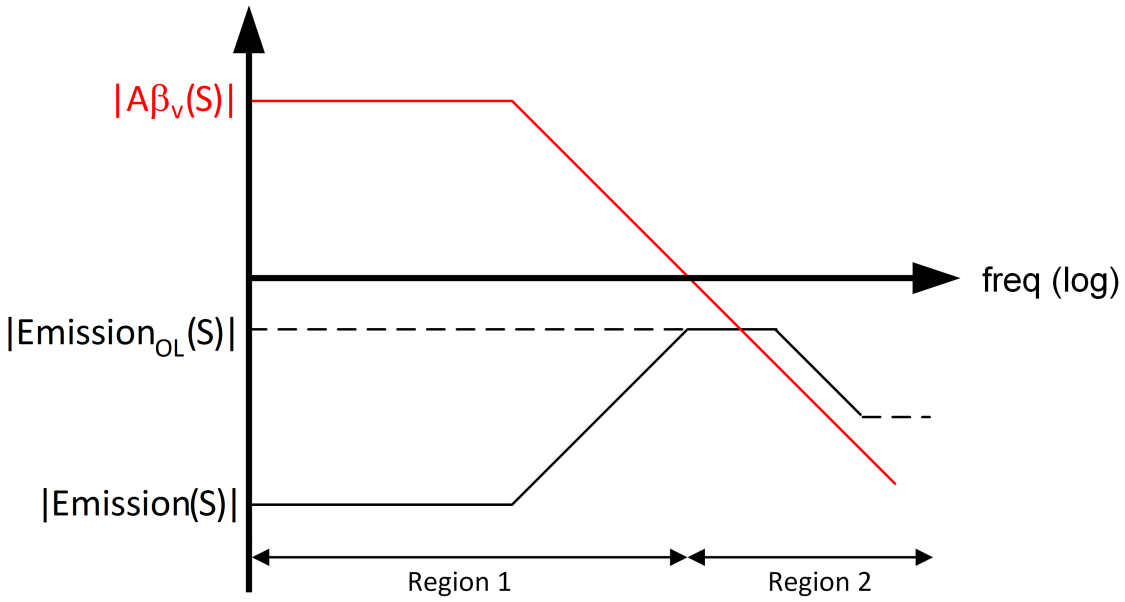

Figure 2.13: Example of an emission curve for a shunt regulator.

$$Emission_2 = \frac{Y_{dd}}{(Y_{dd} + Y_q)[1 + A(s)\beta_v]} \approx \frac{Y_{dd}}{Y_{dd} + Y_q} \approx Em_{OL} \tag{2.28}$$

Comparison

The same open loop approach as used in the previous section will be used. Analyzing the Em_{OL} of the topologies is sufficient to compare the emission performance of the four topologies.

NMOS Series In order to calculate the open loop emission, the same transistor model as used during the calculation of PSR_{OL} (figure 2.2) is converted to its small signal equivalent (figure 2.14). The small signal supply voltage is replaced by a short as it is not relevant when calculating the emission. The parasitics are simplified in the same way as during the calculation of the open loop PSR (subsection 2.1.1).

The small signal load current (i_l) is divided into a quiescent current (i_q) and a current coming from the supply (i_{dd}).

$$i_l = i_{dd} + i_q = i_{dd,a} + i_{dd,b} + i_{q,a} + i_{q,b} \tag{2.29}$$

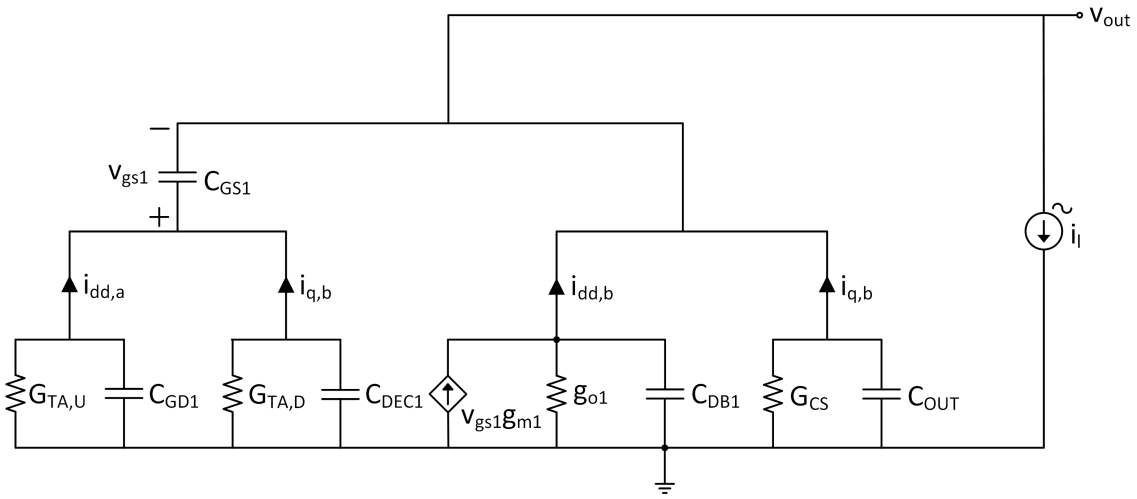

Figure 2.14: Small signal equivalent of the open loop NMOS series model.

Four admittances can be defined:

$$\begin{aligned}
Y_{dd,a} &= \frac{-i_{dd,a}}{v_{out}} = \frac{sC_{GS1}(G_{TA,U} + sC_{GD1})}{G_{TA,U} + G_{TA,D} + s(C_{DEC1} + C_{GD1} + C_{GS1})} \\
Y_{dd,b} &= \frac{-i_{dd,b}}{v_{out}} = \frac{G_{TA,U} + G_{TA,D} + s(C_{DEC1} + C_{GD1})}{G_{TA,U} + G_{TA,D} + s(C_{DEC1} + C_{GD1} + C_{GS1})} g_{m1} + g_{o1} + sC_{DB1} \\
Y_{q,a} &= \frac{-i_{q,a}}{v_{out}} = \frac{sC_{GS1}(G_{TA,D} + sC_{DEC1})}{G_{TA,U} + G_{TA,D} + s(C_{DEC1} + C_{GD1} + C_{GS1})} \\
Y_{q,b} &= \frac{-i_{q,b}}{v_{out}} = G_{CS} + sC_{OUT}
\end{aligned} \tag{2.30}$$

i_{dd} is a portion of i_l, which magnitude is determined by the admittances of equation 2.30. This results in an expression for Em_{OL}:

$$Em_{OL} = \frac{\delta i_{dd}}{\delta i_l} = \frac{Y_{dd,a} + Y_{dd,b}}{Y_{dd,a} + Y_{dd,b} + Y_{q,a} + Y_{q,b}} \tag{2.31}$$

PMOS Series In order to calculate the open loop emission, the same transistor model as used during the calculation of PSR_{OL} (figure 2.4) is converted to its small signal equivalent (figure 2.15). The small signal supply voltage is replaced by a short as it is not relevant when calculating the emission. The parasitics are simplified in the same way as during the calculation of the open loop PSR (subsection 2.1.1).

The small signal load current (i_l) is divided into a quiescent current (i_q) and a current coming from the supply (i_{dd}).

$$i_l = i_{dd} + i_q = i_{dd,a} + i_{dd,b} + i_{q,a} + i_{q,b} \tag{2.32}$$

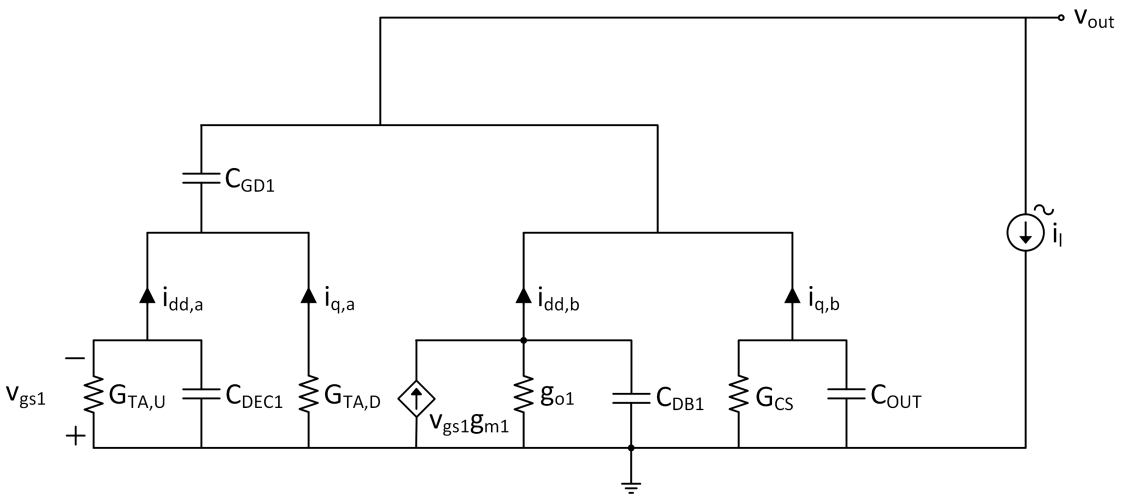

Figure 2.15: Small signal equivalent of the open loop PMOS series model.

Four admittances can be defined:

$$\begin{aligned} Y_{dd,a} &= \frac{-i_{dd,a}}{v_{out}} = \frac{sC_{GD1}(G_{TA,U} + sC_{DEC1})}{G_{TA,U} + G_{TA,D} + s(C_{DEC1} + C_{GD1})} \\ Y_{dd,b} &= \frac{-i_{dd,b}}{v_{out}} = \frac{sC_{GD1}}{G_{TA,U} + G_{TA,D} + s(C_{DEC1} + C_{GD1})} g_{m1} + g_{o1} + sC_{DB1} \\ Y_{q,a} &= \frac{-i_{q,a}}{v_{out}} = \frac{sC_{GD1}G_{TA,D}}{G_{TA,U} + G_{TA,D} + s(C_{DEC1} + C_{GD1})} \\ Y_{q} &= \frac{-i_{q}}{v_{out}} = G_{CS} + sC_{OUT} \end{aligned} \tag{2.33}$$

i_{dd} is a portion of i_l, which magnitude is determined by the admittances of equation 2.33. This results in an expression for Em_{OL}:

$$Em_{OL} = \frac{\delta i_{dd}}{\delta i_l} = \frac{Y_{dd,a} + Y_{dd,b}}{Y_{dd,a} + Y_{dd,b} + Y_{q,a} + Y_{q,b}} \tag{2.34}$$

NMOS Shunt In order to calculate the open loop emission, the same transistor model as used during the calculation of PSR_{OL} (figure 2.6) is converted to its small signal equivalent for the calculation of the emission (figure 2.16). The small signal supply voltage is replaced by a short as it is not relevant when calculating the emission. The parasitics are simplified in the same way as during the calculation of the open loop PSR (subsection 2.1.1).

The small signal load current (i_l) is divided into a quiescent current (i_q) and a current coming from the supply (i_{dd}).

$$i_l = i_{dd} + i_q = i_{dd,a} + i_{dd,b} + i_{q,a} + i_{q,b} \tag{2.35}$$

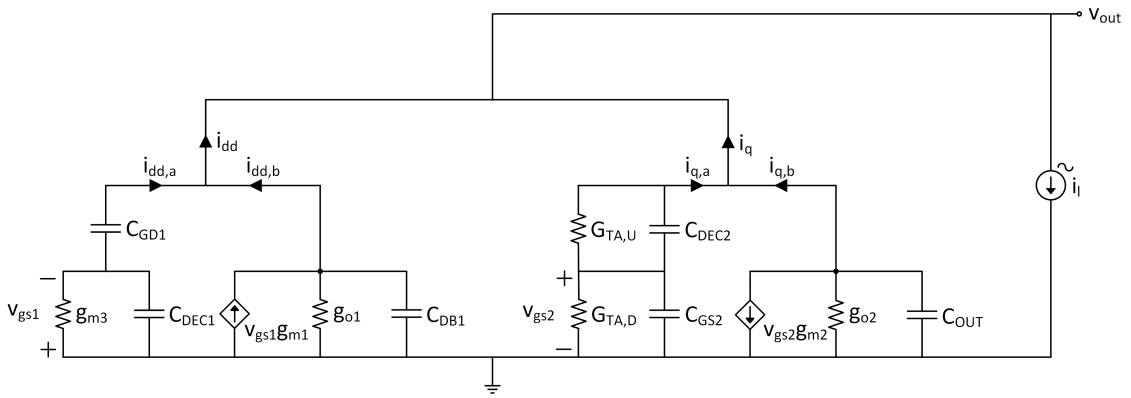

Figure 2.16: Small signal equivalent of the open loop NMOS shunt model.

Four admittances can be defined:

$$\begin{aligned} Y_{dd,a} &= \frac{-i_{dd,a}}{v_{out}} = \frac{sC_{GD1}(sC_{DEC1} + g_{m3})}{g_{m3} + s(C_{DEC1} + C_{GD1})} \\ Y_{dd,b} &= \frac{-i_{dd,b}}{v_{out}} = \frac{sC_{GD1}}{g_{m3} + s(C_{DEC1} + C_{GD1})} g_{m1} + g_{o1} + sC_{DB1} \\ Y_{q,a} &= \frac{-i_{q,a}}{v_{out}} = \frac{(G_{TA,U} + sC_{DEC2})(G_{TA,D} + sC_{GS2})}{G_{TA,U} + G_{TA,D} + s(C_{DEC2} + C_{GS2})} \\ Y_{q,b} &= \frac{-i_{q,b}}{v_{out}} = \frac{G_{TA,U} + sC_{DEC2}}{G_{TA,U} + G_{TA,D} + s(C_{DEC2} + C_{GS2})} g_{m2} + g_{o2} + sC_{OUT} \end{aligned} \tag{2.36}$$

i_{dd} is a portion of i_l, which magnitude is determined by the admittances of equation 2.36. This results in an expression for Em_{OL}:

$$Em_{OL} = \frac{\delta i_{dd}}{\delta i_l} = \frac{Y_{dd,a} + Y_{dd,b}}{Y_{dd,a} + Y_{dd,b} + Y_{q,a} + Y_{q,b}} \tag{2.37}$$

PMOS Shunt In order to calculate the open loop emission, the same transistor model as used during the calculation of PSR_{OL} (figure 2.8) is converted to its small signal equivalent (figure 2.17). The small signal supply voltage is replaced by a short as it is not relevant when calculating the emission. The parasitics are simplified in the same way as during the calculation of the open loop PSR (subsection 2.1.1).

The small signal load current (i_l) is divided into a quiescent current (i_q) and a current coming from the supply (i_{dd}).

$$i_l = i_{dd} + i_q = i_{dd,a} + i_{dd,b} + i_{q,a} + i_{q,b} \tag{2.38}$$

Four admittances can be defined:

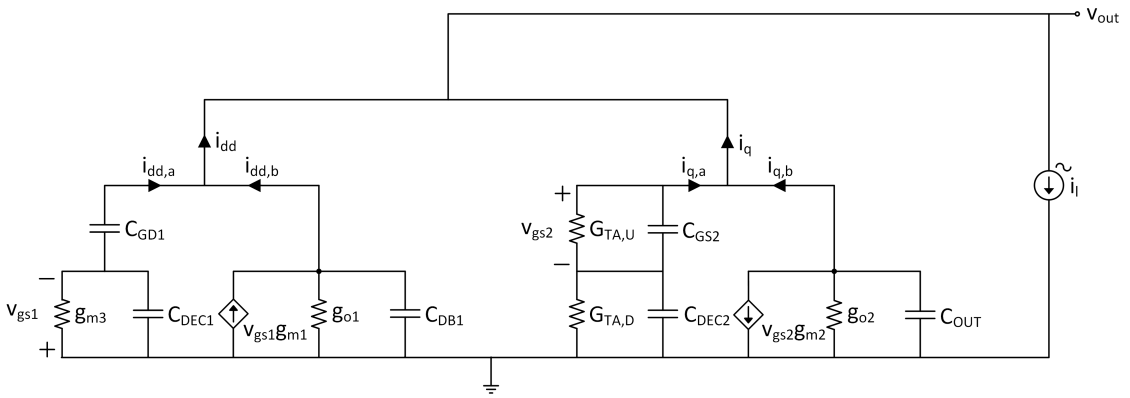

Figure 2.17: Small signal equivalent of the open loop PMOS shunt model.

$$
\begin{aligned}
Y_{dd,a} &= \frac{-i_{dd,a}}{v_{out}} = \frac{sC_{GD1}(g_{m3} + sC_{DEC1})}{g_{m3} + s(C_{GD1} + sC_{DEC1})} \\
Y_{dd,b} &= \frac{-i_{dd,b}}{v_{out}} = \frac{sC_{GD1}}{g_{m3} + s(C_{DEC1} + C_{GD1})} g_{m1} + g_{o1} + sC_{DB1} \\
Y_{q,a} &= \frac{-i_{q,a}}{v_{out}} = \frac{(G_{TA,U} + sC_{GS2})(G_{TA,D} + sC_{DEC2})}{G_{TA,U} + G_{TA,D} + s(C_{DEC2} + C_{GS2})} \\
Y_{q,b} &= \frac{-i_{q,b}}{v_{out}} = \frac{G_{TA,D} + sC_{DEC2}}{G_{TA,U} + G_{TA,D} + s(C_{DEC2} + C_{GS2})} g_{m2} + g_{o2} + sC_{OUT}
\end{aligned}
\tag{2.39}
$$

i_{dd} is a portion of i_l, which magnitude is determined by the admittances of equation 2.39. This results in an expression for Em_{OL}:

$$
Em_{OL} = \frac{\delta i_{dd}}{\delta i_l} = \frac{Y_{dd,a} + Y_{dd,b}}{Y_{dd,a} + Y_{dd,b} + Y_{q,a} + Y_{q,b}} \tag{2.40}
$$

Model verification

The open loop emission has been simulated using the transistor models from the A-BCD9 library. DC feedback was used to bias the output stage. The circuits used for simulation can be found in appendix C. The small signal parameters of the circuits can be found in table 2.1. The parameters are directly mapable to the small signal circuits from section 2.1.2 and can be used to verify the equations with the simulated models. Figure 2.18 shows the equations for the open loop emission versus the simulated open loop emission.

The same zero as in the PSR_{OL} (caused by the finite drain resistance of the HV PMOS) now occurs as a pole in the Em_{OL}. Apart from this pole, the simulation matches the equations quite well.

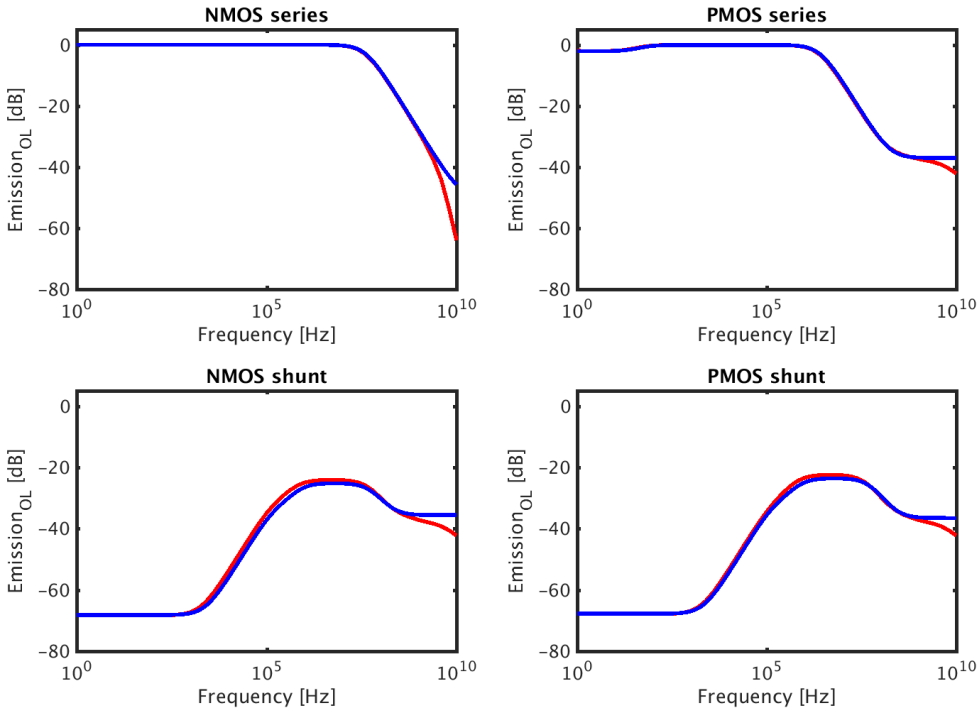

Figure 2.18: The simulated Em_{OL} using the transistor models (blue) versus the calculated equation for the Em_{OL} (red).

2.1.3 Minimum drop-out voltage

The minimum drop-out voltage ($V_{DO,min}$) is a parameter that indicates the minimum supply voltage ($V_{DD,min}$) under which the ISR can operate. The drop-out voltage (V_{DO}) during operation is often chosen to be slightly above $V_{DO,min}$ in order to have some margin for disturbances.

Description

$V_{DO,min}$ is defined as the difference between $V_{DD,min}$ and the specified output voltage (V_{OUT}).

$$V_{DO,min} = V_{DD,min} - V_{OUT} \tag{2.41}$$

Where $V_{DD,min}$ is defined as the supply voltage where V_{OUT} drops to 90% of its specified value. $V_{dd,min}$ should be determined under worst case conditions, i.e. maximum load current, maximum temperature, and slow transistors.

In this application, $V_{DD,min}$ is specified to be 3.5V and the ISR should regulate V_{OUT} to 1.8V. These specifications allow a maximum $V_{DO,min}$ of 1.7V.

Comparison

$V_{DO,min}$ is mostly determined by the output stage. During comparison, the topologies from figure 1.6 should be kept in mind.

NMOS series To determine $V_{DO,min}$ of the NMOS series topology, the basic architecture is shown in figure 2.19.

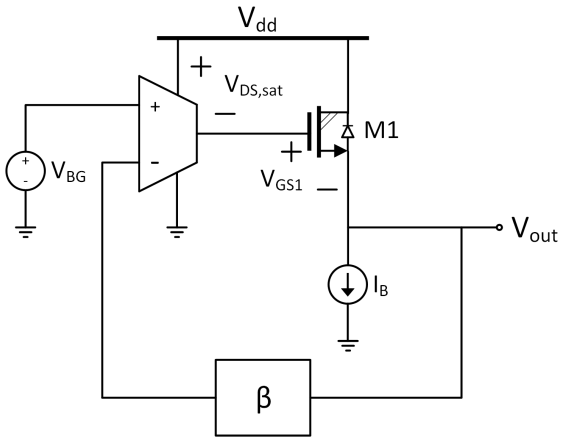

Figure 2.19: Basic architecture of the NMOS series topology.

In order for the NMOS to be in saturation, it must hold that $V_{GS1} > V_{TH1}$. In order to keep the output stage of the TA in saturation, the supply voltage should be at least $V_{DS,sat}$ above the output voltage of the TA. $V_{DO,min}$ is given by:

$$\begin{aligned} V_{DO,min} &= V_{GS1} + V_{DS,sat} \\ &= V_{TH1} + \sqrt{\frac{2I_L}{(W/L)_1 k_1}} + V_{DS,sat} \end{aligned} \tag{2.42}$$

To reduce $V_{DO,min}$, a large W/L ratio for M1 can be chosen at the cost of increased area and parasitics.

PMOS series During operation of the PMOS series topology the HV PMOS must stay in saturation. $V_{DO,min}$ of the PMOS series regulator is given by:

$$\begin{aligned} V_{DO,min} &= V_{DS,sat1} \\ &= \sqrt{\frac{2I_L}{(W/L)_1 k_1}} \end{aligned} \tag{2.43}$$

Shunt regulators In the shunt topologies the HV PMOS is operated as a current source. Just as in the PMOS series topology, this HV PMOS must stay in saturation during operation. The only difference with the PMOS series topology is the amount of current that runs through the HV PMOS. The $V_{DO,min}$ of the shunt topologies is given by:

$$\begin{aligned} V_{DO,min} &= V_{DS,satCS} \\ &= \sqrt{\frac{2I_B}{(W/L)_1 k_1}} \end{aligned} \tag{2.44}$$

2.1.4 Power efficiency

In many applications the power efficiency is an important property of the regulator. The maximum power efficiency of a linear regulator is often determined from system level by specifying the desired V_{DO}. The current efficiency (λ) then determines how close the actual power efficiency meets the maximum attainable power efficiency set by the V_{DO}.

Description

The power efficiency (η) of a linear regulator is defined as the ratio between the amount of power delivered to the load and the amount of power drawn from the supply. By expressing these powers in voltages and currents, the power efficiency can be expressed in terms of V_{DO}, the load current (I_L), the quiescent current (I_Q), and current used for auxiliary circuits (I_{AUX}).

$$\eta = \frac{P_L}{P_{DD}} = \frac{V_{OUT} I_L}{V_{DD}(I_L + I_Q + I_{AUX})} = (1 - \frac{V_{DO}}{V_{DD}})\lambda \tag{2.45}$$

Comparison

In general $I_{AUX} \ll I_Q$ and so λ is dominated by I_Q. In the following subsections, the design considerations that determine the magnitude of I_Q are discussed.

Series regulators In series regulators, the DC quiescent current (I_Q) is determined by bias current I_B. The DC current through the regulating transistor is given by:

$$I_D = I_L + I_B \tag{2.46}$$

Although it is possible to let I_B approximate zero, this is often not done as the regulator could switch off during low loading conditions. Generally a small value for I_B is chosen, making series regulators very power efficient.

Shunt regulators In shunt regulators, I_Q is determined by the difference between I_B and I_L. The DC current through the regulating transistor is given by:

$$I_D = I_B - I_L = I_Q \tag{2.47}$$

To avoid the regulator from switching off during high loading conditions, $I_B > I_{L,max}$. Consequently, I_Q is quite large during low loading conditions, making shunt regulators rather power inefficient. In addition, knowledge about I_L is required in order to minimize the power inefficiency.

2.1.5 Load regulation

Description

Load regulation is defined as the static dependency of the output voltage on the load current. It is a large signal parameter given by:

$$Load\,regulation = \frac{\Delta I_L}{\Delta V_{OUT}} \tag{2.48}$$

The load regulation is expressed in [A/V] and is only valid within a specified current range. As a change in load current also changes the biasing conditions of the output stage, the load regulation is non-linear. A first order approximation of the load regulation can be made through the small signal output conductance.

Comparison

The output conductance is reduced by the VRL. The closed loop output conductance is given by:

$$Load\,regulation \approx G_{OUT} = G_{OUT,OL}(1 + A_{DC}\beta_v) \tag{2.49}$$

Table 2.2 shows the open loop output conductances ($G_{OUT,OL}$) for the different topologies.

Topology	$G_{OUT,OL}$
NMOS series	$g_{o1} + G_{CS} + g_{m1}$
PMOS series	$g_{o1} + G_{cs}$
NMOS shunt	$g_{o1} + g_{o2} + \frac{G_{TA,U}G_{TA,D}}{G_{TA,U}+G_{TA,D}} + \frac{G_{TA,U}}{G_{TA,U}+G_{TA,D}} g_{m2}$
PMOS shunt	$g_{o1} + g_{o2} + \frac{G_{TA,U}G_{TA,D}}{G_{TA,U}+G_{TA,D}} + \frac{G_{TA,D}}{G_{TA,U}+G_{TA,D}} g_{m2}$

Table 2.2: Open loop conductances for the different topologies.

2.1.6 Line regulation

Description

Line regulation is defined as the static dependency of the output voltage on the supply voltage. It is a large signal parameter given by:

$$Line\,regulation = \frac{\Delta V_{DD}}{\Delta V_{OUT}} \tag{2.50}$$

Line regulation is expressed in [V/V] and is only valid within a specified supply voltage range. A change in supply voltage does not affect the biasing conditions and so the load regulation is linear. The line regulation is therefore equal to the DC value of the small signal PSR.

Comparison

The PSR of the topologies have already been extensively analyzed in section 2.1.1. Recall that the closed loop PSR is related to PSR_{OL} by the loop gain of the VRL:

$$Line\,regulation = PSR_{DC} = PSR_{OL,DC}(1 + A_{DC}\beta_v) \tag{2.51}$$

Table 2.3 shows the $PSR_{OL,DC}$ for the different topologies.

Topology	$PSR_{OL,DC}$
NMOS series	$\frac{g_{m1}(G_{TA,U}+G_{TA,D})}{g_{m1}G_{TA,U}+g_{o1}(G_{TA,U}+G_{TA,D})}$
PMOS series	$\frac{(g_{o1}+G_{cs})(G_{TA,U}+G_{TA,D})}{g_{m1}G_{TA,D}}$
NMOS shunt	$\frac{(g_{o1}+g_{o2})(G_{TA,U}+G_{TA,D})+G_{TA,U}G_{TA,D}+G_{TA,U}g_{m2}}{g_{o1}(G_{TA,U}+G_{TA,D})}$
PMOS shunt	$\frac{(g_{o1}+g_{o2})(G_{TA,U}+G_{TA,D})+G_{TA,U}G_{TA,D}+G_{TA,D}g_{m2}}{g_{o1}(G_{TA,U}+G_{TA,D})}$

Table 2.3: $PSR_{OL,DC}$ for the different topologies.

2.1.7 Load Transient

In a realistic system, the load current can be very dynamic. The ISR must have a well controlled response to load steps up to a certain magnitude and with a certain rise time.

Description

The load transient response shows the dynamic behavior of the output voltage ($V_{out}(t)$) caused by a step in the load current ($I_l(t)$). Important parameters to observe are the settling time and the peak amplitude of the output voltage.

The transient behavior can be predicted from the small signal output impedance [7]. Current steps with a large amplitude will deviate from this response due to large signal effects.

Comparison

The load step response can be approximated by doing an inverse Laplace transform on the output voltage ($V_{OUT}(s)$).

$$\begin{aligned} V_{out}(t) &= \mathcal{L}^{-1}\left\{V_{OUT}(s)\right\} \\ &= \mathcal{L}^{-1}\left\{\frac{-I_L(s)}{Y_{OUT}(s)}\right\} \end{aligned} \tag{2.52}$$

The VRL increases the output admittance of the output stage:

$$Y_{OUT}(s) = Y_{OUT,OL}(s)[1 + A(s)\beta_v] \tag{2.53}$$

The open loop output admittances ($Y_{OUT,OL}$) of the different topologies is given by:

$$Y_{OUT,OL}(s) = Y_{dd} + Y_q \tag{2.54}$$

Where Y_{dd} and Y_q are the admittances that were found in section 2.1.2.

Model verification

It can be seen that the equations match quite well with the simulated model, even for current steps of 1mA.

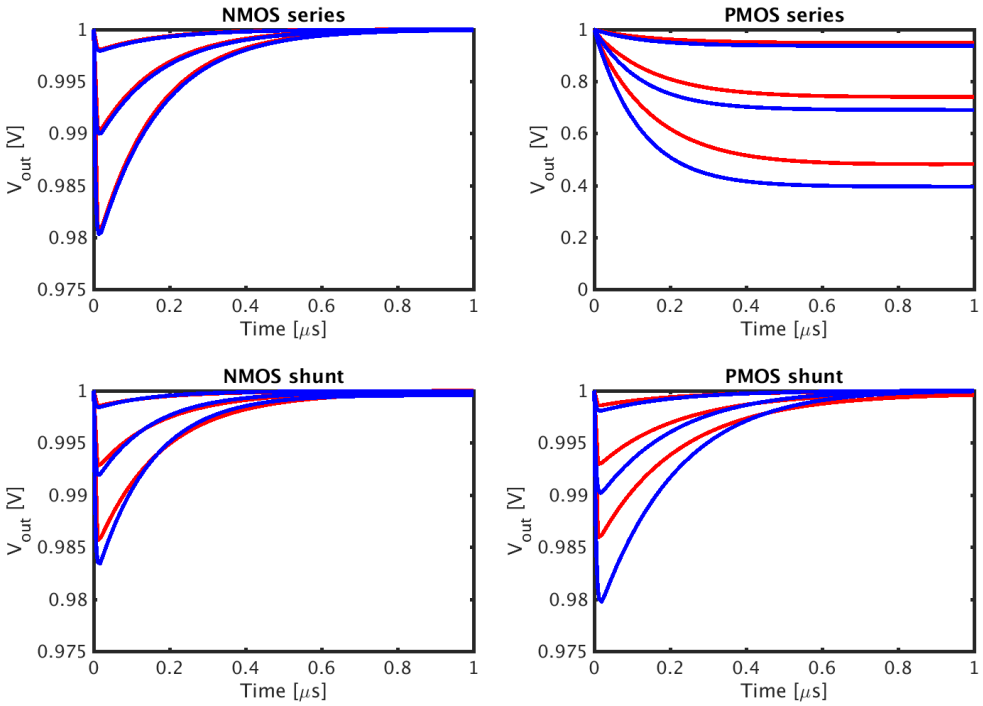

Figure 2.20: The simulated load transient response for load steps of 100uA, 500uA and 1mA. The response of the transistor models (blue) is compared to the Laplace transform of the output impedance of the model (red).

2.1.8 Line transient

The ISR must be able to cope with dynamic variations on the supply. As mentioned in chapter 1, the conditions in the automotive environment are quite harsh. The effects described in [1] can cause voltage peaks as high as 70V with rise times that can be as short as 5ns. Extensively large voltages are mostly handled by protection diodes within the IC. Nonetheless the ISR is directly supplied from the external supply and therefore needs to be robust against line variations.

Description

The line transient response shows the dynamic behavior of the output voltage ($V_{out}(t)$) caused by a step in the supply voltage ($V_{dd}(t)$). Important parameters to observe are the settling time and the peak amplitude of the output voltage.

The transient behavior can be predicted from the small signal PSR. Voltage steps with a large amplitude will deviate from this response due to large signal effects.

Comparison

The line step response can be approximated by doing an inverse Laplace transform on the output voltage ($V_{OUT}(s)$).

$$V_{out}(t) = \mathcal{L}^{-1}\{V_{OUT}(s)\} = \mathcal{L}^{-1}\left\{\frac{V_{DD}(s)}{PSR(s)}\right\} \tag{2.55}$$

The VRL increases the PSR of the output stage:

$$PSR(s) = PSR_{OL}(s)[1 + A(s)\beta_v] \tag{2.56}$$

For the PSR_{OL} expressions of the different topologies, see section 2.1.1.

Model verification

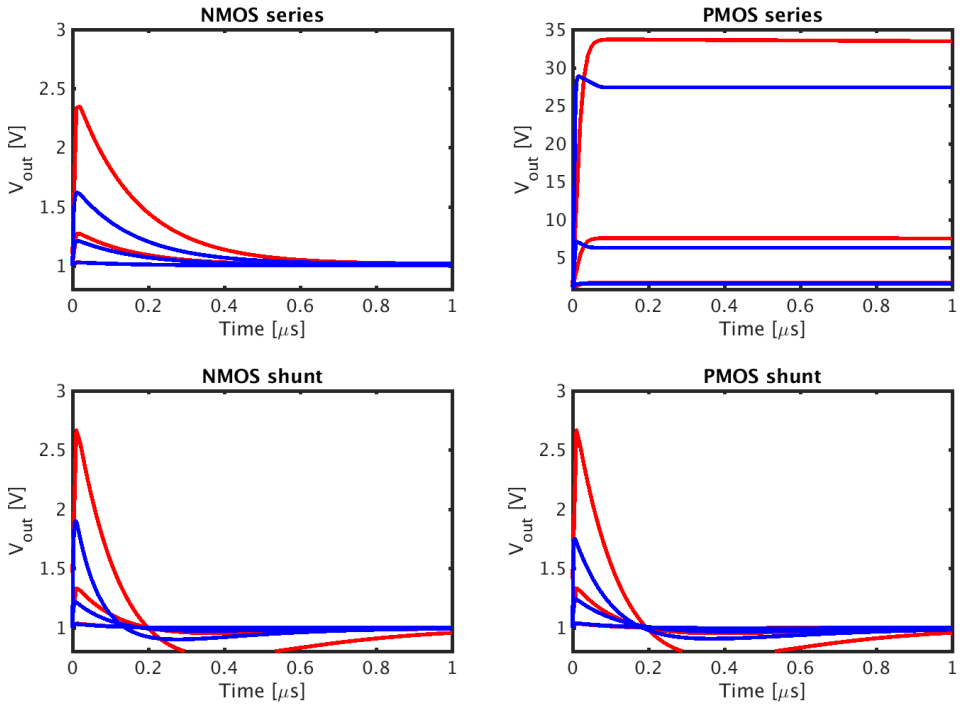

Figure 2.21: The simulated line transient response for supply steps of 1V, 10V and 50V. The response of the transistor models (blue) is compared to the Laplace transform of the output impedance of the model (red).

It can be seen that the equations match quite well with the simulated model. The simulations start to deviate at voltage steps above 10V due to large signal behavior.

2.1.9 Gain-Bandwidth Product

The open loop approach disregards the influence of the VRL. However the choice of topology does have an effect on the maximum Gain-Bandwidth (GBW) that can be

achieved in the VRL. In the following subsections, the Gain-Bandwidth capabilities of the topologies will be investigated.

Description

The GBW is mainly dependent on the parasitic capacitances within the VRL and the transconductances of the transistors. A large GBW results in a fast loop response to disturbances with high suppression.

Comparison

An estimate for the maximum attainable bandwidth of the loop can be made using the Loopgain-Poles product (LP product) [10]. The LP product is defined as:

$$LP_n = (1 - L_{DC}) \prod_{i=1}^{n} |p_i| \tag{2.57}$$

Where n is the number of poles in the loop and L_{DC} is the DC loop gain. The maximum attainable UGF is given by:

$$\omega_{n,max} = \sqrt[n]{LP_n} = \sqrt[n]{(1 - L_{DC}) \prod_{i=1}^{n} |p_i|} \tag{2.58}$$

NMOS series The two largest capacitances that influence the loop in the NMOS series topology are C_{DEC1} and C_{OUT} (figure 2.22). To calculate the equation for the loop gain, the loop is broken at the input of the feedback network. The loop gain is now calculated as:

$$A(s)\beta_v = \frac{v_{out}}{v_x} = -\frac{Gm_{TA} g_{m1} \beta}{(G_{TA} + sC_{DEC1})(g_{o1} + G_{CS} + G_{\beta_v,in} + g_{m1} + sC_{OUT})} \tag{2.59}$$

The pole at the output node can be considered as a non-dominant pole. The maximum attainable UGF as indicated by the LP-product is given by:

$$\omega_{max} = (1 + \frac{Gm_{TA} g_{m1} \beta}{G_{TA}(g_{o1} + G_{CS} + G_{\beta_v,in} + g_{m1})}) \frac{G_{TA}}{C_{DEC1}} \tag{2.60}$$

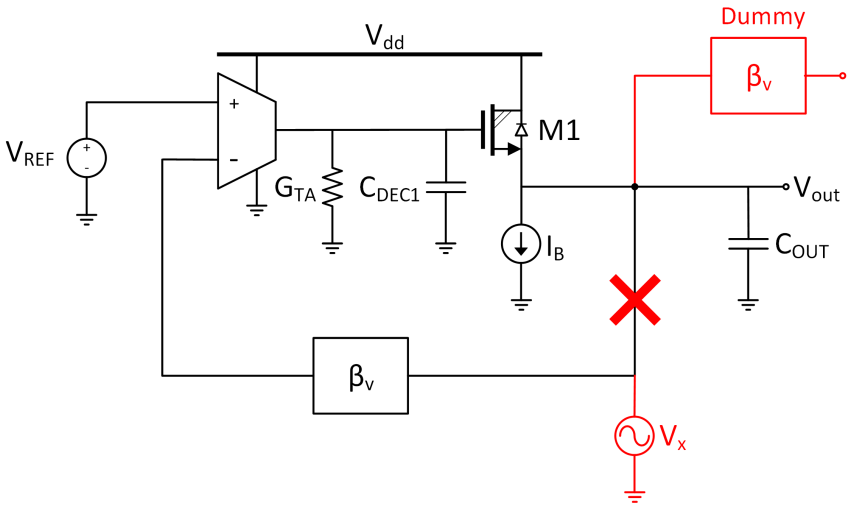

Figure 2.22: Schematic for determining the loop transfer function of the NMOS series regulator.

PMOS series The three largest capacitances that influence the loop in the PMOS series topology are C_{DEC1}, C_{GD1}, and C_{OUT} (figure 2.23). To calculate the equation for the loop gain, the loop is broken at the input of the feedback network. The poles are first approximated without the influence of C_{GD1}. The poles of the simplified system are given by:

$$\begin{aligned} p_1 &= -\frac{G_{TA}}{C_{DEC1}} \\ p_2 &= -\frac{g_{o1} + G_{CS} + G_{\beta_v,in}}{C_{OUT}} \end{aligned} \tag{2.61}$$

The maximum UGF as indicated by the LP-product is given by:

$$\omega_{n,max} = \sqrt{(1 + \frac{Gm_{TA}\beta g_{m1}}{G_{TA}})(\frac{G_{TA}}{C_{DEC1}})(\frac{g_{o1} + G_{CS} + G_{\beta_v,in}}{C_{OUT}})} \tag{2.62}$$

If $p_1 > p_2$, C_{GD1} will be subdued to the Miller effect and will have a substantial impact on the frequency behavior of the loop. The local feedback through C_{GD1} causes p_1 and p_2 to split. The splitting of the poles will lower the LP-product by [10]:

$$\frac{LP_{after}}{LP_{before}} = \frac{C_{DEC1}C_{OUT}}{C_{DEC1}C_{OUT} + C_{GD1}(C_{DEC1} + C_{OUT})} \tag{2.63}$$

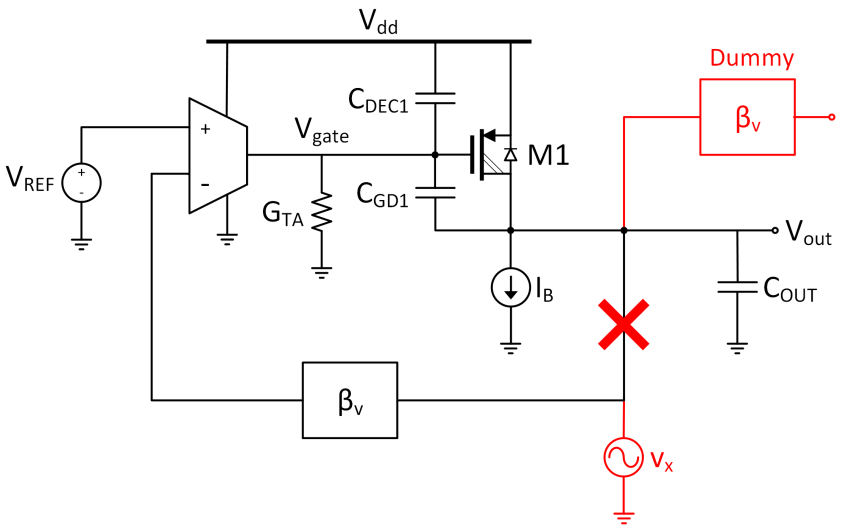

Figure 2.23: Schematic for determining the loop transfer function of the PMOS series regulator.

NMOS shunt The two capacitances that influence the loop in the NMOS shunt topology are C_{DEC2}, and C_{OUT} (figure 2.24). To calculate the equation for the loop gain, the loop is broken at the input of the feedback network. The poles are first approximated without the influence of C_{DEC2}. The poles of the simplified system are given by:

$$\begin{aligned} p_1 &= -\frac{G_{TA}}{C_{GS2}} \\ p_2 &= -\frac{g_{o2} + G_{CS} + G_{\beta_v,in}}{C_{OUT}} \end{aligned} \tag{2.64}$$

The maximum UGF as indicated by the LP-product is given by:

$$\omega_{n,max} = \sqrt{(1 + \frac{Gm_{TA}\beta g_{m2}}{G_{TA}})(\frac{G_{TA}}{C_{GS2}})(\frac{g_{o2} + G_{CS} + G_{\beta_v,in}}{C_{OUT}})} \tag{2.65}$$

If $p_1 > p_2$, C_{DEC2} will be subdued to the Miller effect and will have a substantial impact on the frequency behavior of the loop. The local feedback through C_{DEC2} causes p_1 and p_2 to split. The splitting of the poles will lower the LP-product by [10]:

$$\frac{LP_{after}}{LP_{before}} = \frac{C_{GS2}C_{OUT}}{C_{GS2}C_{OUT} + C_{DEC2}(C_{GS2} + C_{OUT})} \tag{2.66}$$

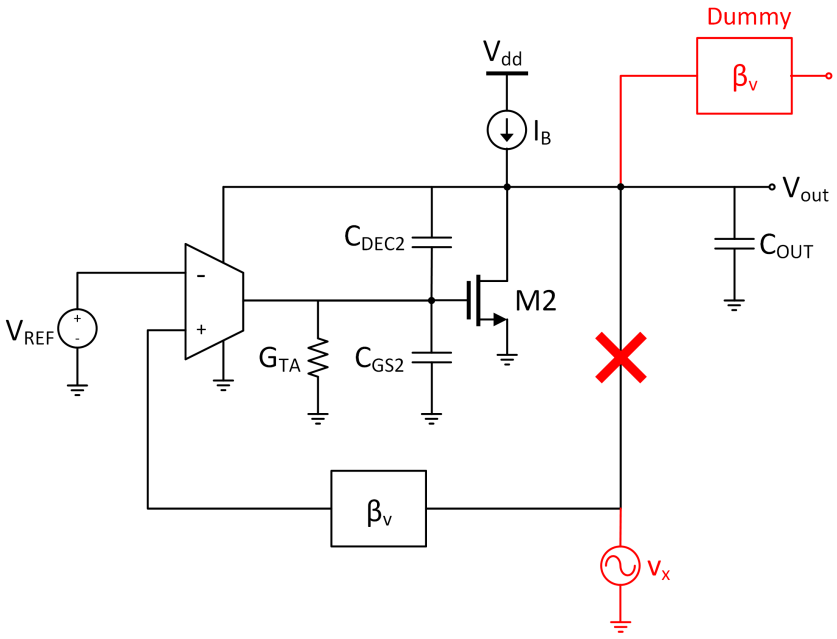

Figure 2.24: Schematic for determining the loop transfer function of the NMOS shunt regulator.

PMOS shunt The two largest capacitances that influence the loop in the PMOS shunt topology are C_{DEC2} and C_{OUT} (figure 2.25). To calculate the equation for the loop gain, the loop is broken at the input of the feedback network. The loop gain is now calculated as:

$$A(s)\beta_v = \frac{v_{out}}{v_x} = -\frac{Gm_{TA}g_{m2}\beta}{(G_{TA}+sC_{DEC2})(g_{o2}+G_{CS}+G_{\beta_v,in}+g_{m2}+sC_{OUT})} \tag{2.67}$$

The pole at the output node can be considered as a non-dominant pole. The maximum UGF as indicated by the LP-product is given by:

$$\omega_{max} = (1+\frac{Gm_{TA}g_{m2}\beta}{G_{TA}(g_{o2}+G_{CS}+G_{\beta_v,in}+g_{m2})})\frac{G_{TA}}{C_{DEC2}} \tag{2.68}$$

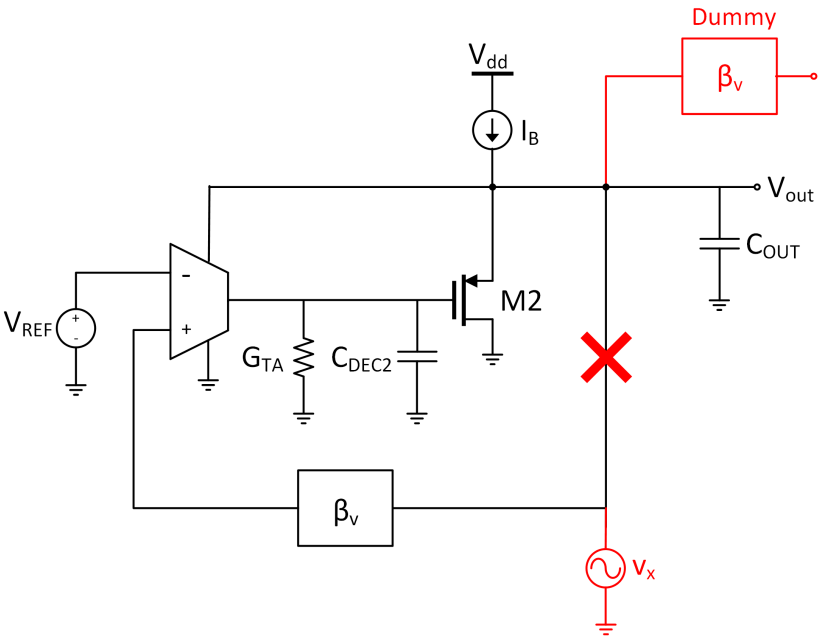

Figure 2.25: Schematic for determining the loop transfer function of the PMOS shunt regulator.

2.1.10 Area

In ISR designs where C_{OUT} is integrated, this capacitance is often the largest component. The main purpose of C_{OUT} is to supply load current for transient loads that are faster than the regulation loop. Only if the loop can be made fast enough to supply these transient load currents, significant area might be saved by reducing C_{OUT}. Although substantially smaller, the output MOS transistor is still quite large as it needs to dissipate a lot of power. The shunt topologies require larger output stage transistors as both current source I_B and the output transistor need to be able to handle the maximum amount of I_L.

2.2 Overall comparison

The topologies are compared by evaluating the performance parameters that were discussed in section 2. The results are shown in table 2.4.

As the focus of research in this thesis is mainly on EMI performance, the emission and PSR parameters are of most importance. In most literature, the series regulator is preferred over the shunt regulator due to its benefits in power efficiency. Although a very good PSR performance can be achieved using a NMOS series topology, it will not perform as well on emission as a shunt topology. If one would choose to use the shunt topology, a few downsides have to be faced:

1. Poor power efficiency
2. Limited current output range
3. Small increase in area

	Shunt		Series	
	NMOS	PMOS	NMOS	PMOS
PSR	+	+	++	- -
Emission	+	++	- -	-
Drop-out voltage	++	++	-	++
Power efficiency	-	-	+	+
Load regulation	-	+	++	-
Line regulation	-	+	++	-
Load transient	-	+	++	-
Line transient	-	+	++	-
Bandwidth	-	++	+	- -
Area	-	- -	+ +	+

Table 2.4: Comparison between the four regulator topologies, using the performance parameters.

2.3 ISR in the KMA3xx family

2.3.1 Description

The digital regulator that is used in the KMA3xx angular sensors is used as a reference design for performance. The topology is shown in figure 2.26. Component values are shown in table 2.5.

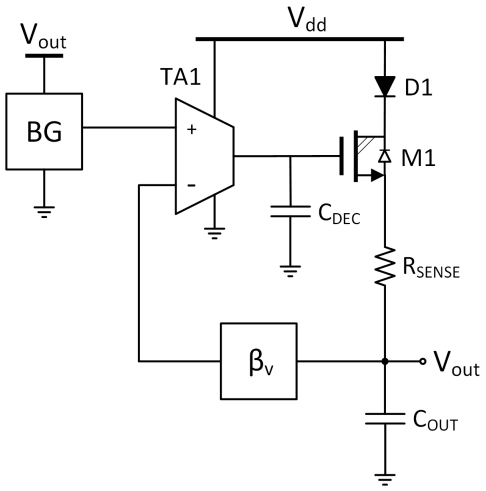

Figure 2.26: Architecture of the KMA3xx NMOS series regulator.

R_{sense} is placed in the load current path for testability. As a side effect, R_{sense} has significant impact on the EMC performance at high frequencies.

D1 is needed to protect M1 from a large inrush current in case the supply pins are reverse connected. In the NMOS series topology, it has no significant impact on the drop-out voltage.

The area of the toplevel components in figure 2.26 is shown in table 2.6.

It can be seen that most area in the design is consumed by the bandgap reference.

Circuit parameter	Value
C_{DEC1}	25.31pF
C_{OUT}	73.5pF
R_{SENSE}	53Ω
$(W/L)_1$	960
V_{BG}	900mV
β_v	0.5
R_{TA}	763MΩ
A_{DC}	87.6dB

Table 2.5: Component values for the KMA3xx ISR as shown in figure 2.26.

System block	Area (μm^2)	Area (%)
BG	56939.7	68.9
C_{OUT}*	6715.6	8.1
β_v	6630.7	8.0
M1	6408.2	7.8
TA1	4218.3	5.1
D1	1682.6	2.0
R_{SENSE}	62.2	0.1
C_{DEC}*	0	0

Table 2.6: Area of the toplevel components of the KMA3xx NMOS series regulator. *: The area consumed by MIM capacitors is excluded.

Chapter 3

Design of the ISR

In this chapter, a new topology will be proposed based on the knowledge that was acquired in the previous chapter. The chapter is divided in a section that describes the ISR on system level and a section that describes the ISR on circuit level. At the end of the system level section, all the circuit blocks are defined along with the specifications they should meet. These specifications are then used in the circuit level section, while designing the individual circuit blocks.

3.1 System design

With the performance parameters of table 2.4 in mind, a topology based on a shunt regulator is proposed. The shunt regulator is chosen due to its capability to attain good performance on both PSR and emission.

3.1.1 Concept

A lot of disadvantages of the shunt regulator topologies are caused by the fact that the bias current of the output stage (I_Q) is dependent on the load current (I_L). A second regulation loop is proposed in order to keep I_Q constant (figure 3.1).

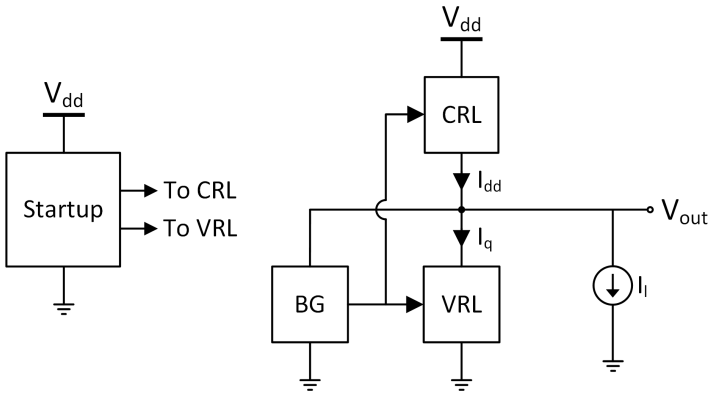

Figure 3.1: Proposed dual loop topology.

This loop is named the Current Regulation Loop (CRL). By reducing the dependency of I_Q on I_L, a stable biasing for the Voltage Regulation Loop (VRL) is provided. The CRL improves the power efficiency with respect to the regular shunt regulator topologies, as the amount of current drawn from the supply adapts to I_L.

A single bandgap reference circuit provides references for both the CRL and the VRL. It is supplied by V_{out} to improve the PSR at low frequencies.

A startup circuit is required to ensure a proper start up when the bandgap reference has not started yet.

3.1.2 Current regulation loop

The CRL is implemented by using a classical feedback approach (figure 3.2).

The feedback current ($I_q\beta_i$) is compared to a reference current (I_{REF}). The resulting error current (I_e) is amplified by current amplifier D(s) and fed back to the input through feedback network β_i. β_i must have a low input impedance so that I_Q will not be dependent on the load resistance (R_L). Also, the DC contribution of the CRL to V_{OUT} ($I_Q * R_{\beta_i,in}$) must be kept to a minimum. V_{out} should be mainly determined by the VRL.

Assuming $R_{\beta_i,in} \ll R_l$, I_q is effectively regulated to:

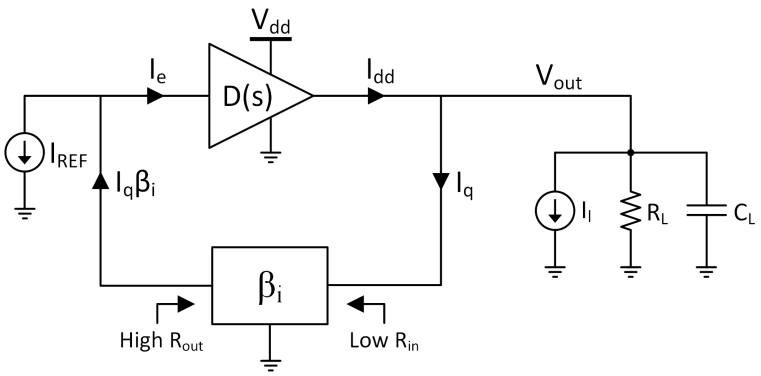

Figure 3.2: The CRL regulates I_Q to a fixed value.

$$I_q = \frac{I_{REF}}{\beta_i}\frac{D(s)\beta_i}{1+D(s)\beta_i} - \frac{I_l}{1+D(s)\beta_i} \tag{3.1}$$

For an infinite DC loop gain, I_Q is independent of I_L.

$$\begin{aligned} I_Q &= \frac{I_{REF}}{\beta_i}\frac{D_{DC}\beta_i}{1+D_{DC}\beta_i} - \frac{I_L}{1+D_{DC}\beta_i} \\ &\approx \frac{I_{REF}}{\beta_i} \end{aligned} \tag{3.2}$$

D(s) delivers the current to the load and must be supplied directly from V_{dd}. By definition, a dependency between i_{dd} and i_l will result in emission. This dependency can be found by solving the KCL equation at the output node of the circuit. It is assumed that $I_l \gg \frac{V_{out}}{R_L}$.

$$\begin{aligned} i_{dd} &= i_l + i_q \\ &= i_l - \frac{i_{dd}}{D(s)\beta_i} \end{aligned} \tag{3.3}$$

The emission is given by:

$$Emission = \frac{i_{dd}}{i_l} = \frac{D(s)\beta_i}{1+D(s)\beta_i} \tag{3.4}$$

When $D(s)\beta_i \gg 1$, the emission is close to 0dB. After the UGF of the loop gain, the emission starts to decrease with $D(s)\beta_i$. In order to improve the emission performance, the UGF of the loop gain must be reduced. This can be done be performing filtering inside the loop. As an on-chip capacitor consumes a lot of silicon area, the filtering is best performed on a high impedance node. In this way a relatively small capacitor can be used.

Loop specifications

As seen in equation 3.2, I_Q is ideally regulated to $\frac{I_{REF}}{\beta_i}$. In reality, there will be a current error due to a finite DC loop gain. The normalized current error is given by:

$$\epsilon_{I_Q} = \frac{I_Q - \frac{I_{REF}}{\beta_i}}{\frac{I_{REF}}{\beta_i}} \tag{3.5}$$

Another expression for ϵ_{I_Q} is found when substituting 3.2 in 3.5:

$$\begin{aligned} \epsilon_{I_Q} &= \frac{\frac{I_{REF}}{\beta_i}\frac{D_{DC}\beta_i}{1+D_{DC}\beta_i} - \frac{I_L}{1+D_{DC}\beta_i} - \frac{I_{REF}}{\beta_i}}{\frac{I_{REF}}{\beta_i}} \\ &= -\frac{1}{1+D_{DC}\beta_i} - \frac{\beta_i}{I_{REF}}\frac{I_L}{1+D_{DC}\beta_i} \\ &\approx -\frac{1}{1+D_{DC}\beta_i} - \frac{\lambda}{(1-\lambda)(1+D_{DC}\beta_i)} \end{aligned} \tag{3.6}$$

Where λ is the current efficiency described in chapter 2. The equation shows the distinction between a constant error due to a finite DC loop gain and an error due to I_L. The expected value for I_L in this application is 1-10mA. To achieve a minimum current efficiency of approximately 90%, I_Q is set to 100μA. In order to minimize ϵ_{I_Q} to 1%, a DC loop gain of 80dB or more is required.

As explained in section 1.2, in this application emission performance will start to play a role for frequencies above 5MHz. A CRL with an UGF of 100kHz will allow more then a decade for the emission to roll-of. As can be seen from equation 3.4, the emission performance will benefit from a steep roll-off after the UGF. To ensure stability, the second pole is placed just after the UGF.

The requirements result in the loop gain as shown in figure 3.3.

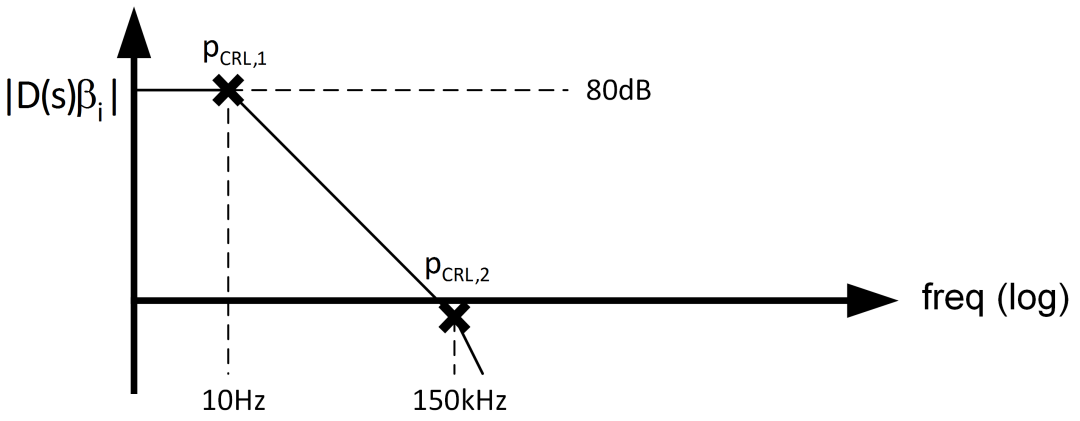

Figure 3.3: Desired loop gain for the CRL.

3.1.3 Voltage regulation loop

The VRL has the purpose of regulating the output voltage to the desired level (figure 3.4). As the CRL already provides a biasing independent of I_L and V_{DD}, the VRL does not necessarily need a high DC loop gain. Instead a large bandwidth is preferred to enhance the high frequency performance.

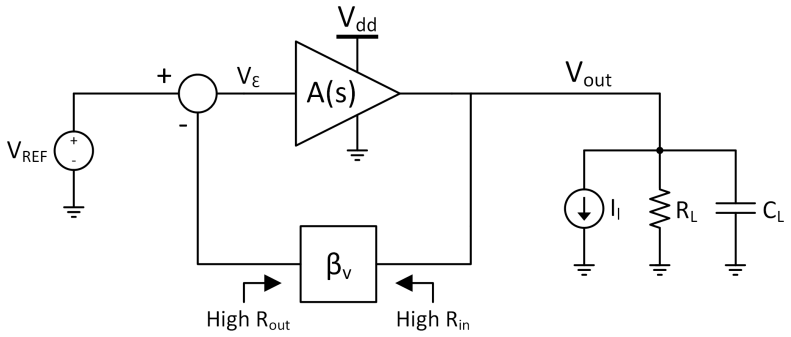

Figure 3.4: The VRL regulates V_{out} to a fixed value.

The DC output voltage is regulated to:

$$\begin{aligned} V_{OUT} &= \frac{V_{REF}}{\beta_v}\frac{A_{DC}\beta_v}{1+A_{DC}\beta_v} \\ &\approx \frac{V_{REF}}{\beta_v} \end{aligned} \tag{3.7}$$

Loop specification

V_{OUT} is ideally regulated to $\frac{V_{REF}}{\beta_v}$. In reality, there will be a voltage error due to a finite $A_{DC}\beta_v$. The normalized voltage error is given by:

$$\epsilon_{V_{OUT}} = \frac{V_{OUT} - \frac{V_{REF}}{\beta_v}}{\frac{V_{REF}}{\beta_v}} \tag{3.8}$$

Another expression for $\epsilon_{V_{OUT}}$ is found when substituting 3.7 in 3.8:

$$\begin{aligned} \epsilon_{V_{OUT}} &= \frac{\frac{V_{REF}}{\beta_v}\frac{A_{DC}\beta_v}{1+A_{DC}\beta_v} - \frac{V_{REF}}{\beta_v}}{\frac{V_{REF}}{\beta_v}} \\ &= -\frac{1}{1+A_{DC}\beta_v} \end{aligned} \tag{3.9}$$

The equation only shows a constant error due to the finite DC loop gain. In this work an accuracy of 99% is considered to be sufficient, requiring a DC loop gain of 40dB or higher. This requirement results in the desired loop gain shown in figure 3.5. As a large bandwidth is desired, $p_{VRL,1}$ and $p_{VRL,2}$ will be located at the highest frequency possible while maintaining stability.

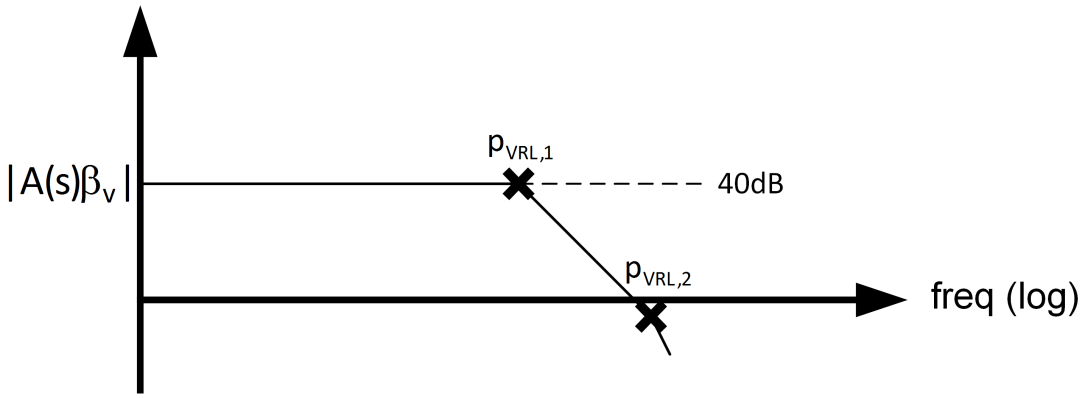

Figure 3.5: Desired loop gain for the VRL.

3.1.4 Regulating loops interaction

In the previous sections, the behavior of both loops was discussed separately. However it was not discussed how these loops can be combined in a single system. Figure 3.6 shows the output stage of the dual loop system on transistor level.

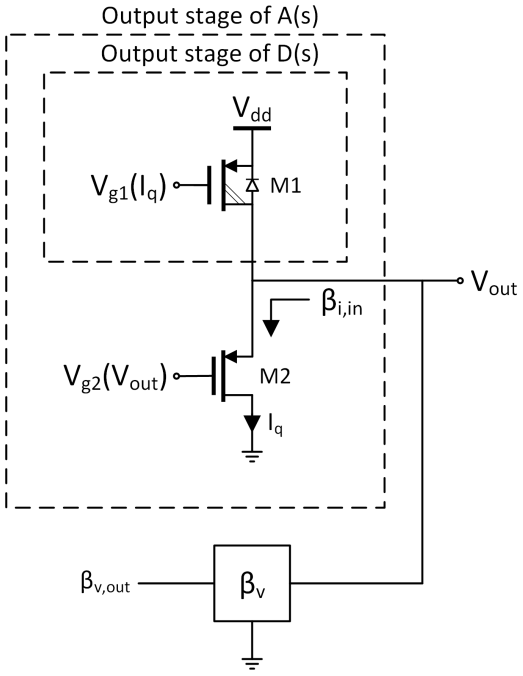

Figure 3.6: Output stages of D(s) and A(s) in a single system.

It can be seen that M1 belongs to the output stage of both D(s) and A(s). As discussed in section 3.1.2, β_i requires a low input impedance. For this reason, M2 is implemented as a PMOS transistor. This results in a regulator topology with the same type of output transistors as in the PMOS shunt topology.

The behavior of one feedback loop may be altered by the other. The consequences of the interaction between the two loops are analyzed in the following subsections.

Effect of the Voltage Regulation Loop on the Current Regulation Loop

The VRL tries to keep the output voltage at a constant value by regulating the current through M2 (figure 3.6). As a result, the output impedance looking into M2 is reduced by the loop gain of the VRL. This impedance is equal to the input impedance of $\beta_{i,in}$.

$$Z_{\beta_i,in}(s) = \frac{Z_{out,sf}(s)}{1 + A(s)\beta_v} \tag{3.10}$$

Where $Z_{out,sf}$ is the output impedance of the source follower stage. As I_Q is preferably small to maintain a good power efficiency, $Z_{out,sf}$ can be substantially large for a source follower. As C_L is also large, the pole at the output is chosen to be the second dominant pole in the CRL ($p_{CRL,2}$, from section 3.1.2). $p_{CRL,2}$ is located at:

$$p_{CRL,2} = -\frac{1}{s|Z_{\beta_i,in}|C_L} \tag{3.11}$$

The dominant pole in the VRL is also at the output of the regulator. $p_{VRL,1}$ is located at:

$$p_{VRL,1} = -\frac{1}{s|Z_{out,sf}|C_L} \tag{3.12}$$

Figure 3.7 visualizes the locations of $p_{CRL,2}$ and $p_{VRL,1}$ as the intersect of $|Z_{\beta_i,in}|$ and C_L, and $|Z_{out,sf}|$ and C_L respectively.

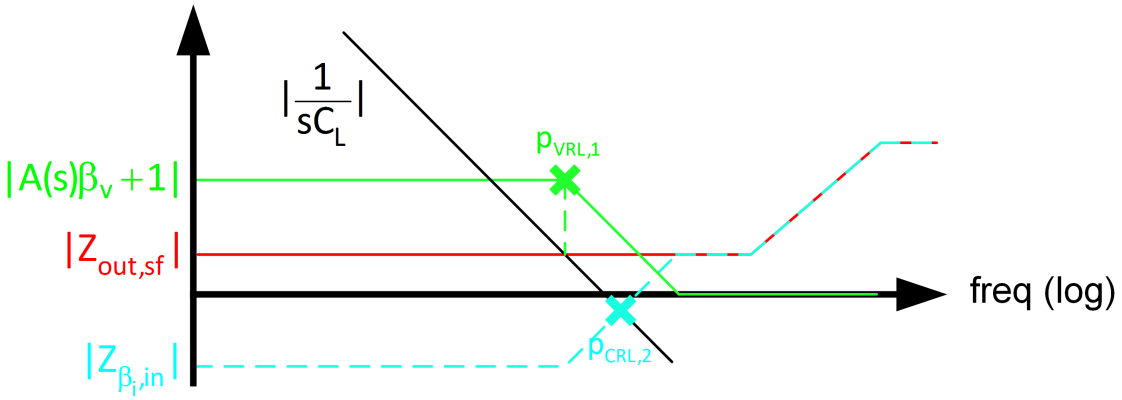

Figure 3.7: Derivation of the locations of $p_{CRL,2}$ and $p_{VRL,1}$ using a visual approach.

The VRL shifts $p_{CRL,2}$ to a higher frequency as it decreases $Z_{\beta,in}$ (see equation 3.11). This confirmed in figure 3.7. When the VRL is designed for a gain of 40dB, $p_{CRL,2}$ is shifted up one decade.

Effect of the Current Regulation Loop on the Voltage Regulation Loop

To investigate the effect of the CRL on the VRL, the output stage of the VRL is examined with the CRL modeled by a variable current source with a finite output conductance (figure 3.8).

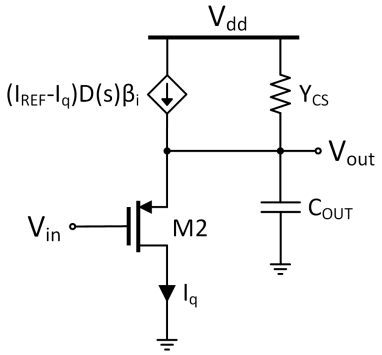

Figure 3.8: Output stage of the VRL.

The small signal voltage gain of the output stage is given by:

$$\begin{aligned} A_v(s) &= \frac{v_{out}}{v_{in}} \\ &= \frac{G_{m,sc}}{Y_{out}} \end{aligned} \tag{3.13}$$

Where $G_{m,sc}$ is the transconductance of the circuit while the output is shorted. Figure 3.9 shows the small signal equivalent circuit to calculate $G_{m,sc}$.

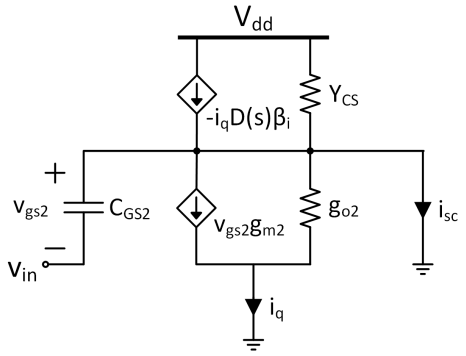

Figure 3.9: Circuit to calculate $G_{m,sc}$.

$$\begin{aligned} i_{sc} &= v_{in} s C_{GS2} + [-i_q D(s)\beta_i] - v_{gs2} g_{m2} \\ &= v_{in}\{g_{m2}[1 + D(s)\beta_i] + sC_{GS2}\} \end{aligned} \tag{3.14}$$

$G_{m,sc}$ is given by:

$$G_{m,sc} = \frac{i_{sc}}{v_{in}} = g_{m2}[1 + D(s)\beta_i] + sC_{GS2} \tag{3.15}$$

Figure 3.10 shows the small signal equivalent circuit to calculate Y_{OUT}.

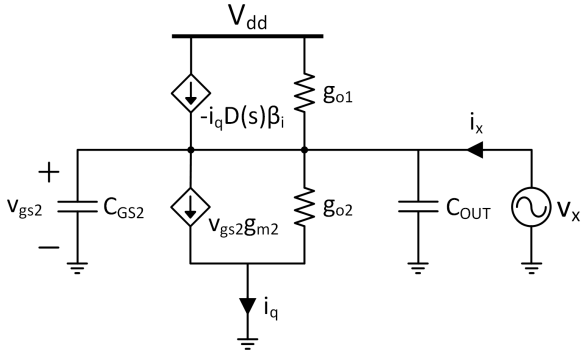

Figure 3.10: Circuit to calculate Y_{OUT}.

$$\begin{aligned} i_x &= i_q[1 + D(s)\beta_i] + v_x[g_{o1} + s(C_{GS2} + C_{OUT})] \\ &= v_x\{(g_{m2} + g_{o2})[1 + D(s)\beta_i] + Y_{CS} + s(C_{GS2} + C_{OUT})]\} \end{aligned} \tag{3.16}$$

Y_{out} is given by:

$$Y_{out} = \frac{i_x}{v_x} = (g_{m2} + g_{o2})[1 + D(s)\beta_i] + Y_{CS} + s(C_{GS2} + C_{OUT}) \tag{3.17}$$

Substituting 3.15 and 3.17 into 3.13 results in an expression for A_v:

$$A_v(s) = \frac{g_{m2}[1 + D(s)\beta_i] + sC_{GS2}}{(g_{m2} + g_{o2})[1 + D(s)\beta_i] + g_{o1} + s(C_{GS2} + C_{OUT})} \tag{3.18}$$

It can be seen that for $D(s)\beta_i \ll 1$, the gain is equal to a source follower stage [4]. When $D(s)\beta_i$ is large, g_{o1} does not degrade the gain of the source follower. In other words the CRL improves the finite impedance of the dependent current source.

3.1.5 Performance parameters

In the following section, the performance parameters that were introduced in chapter 2 are analyzed for the dual loop regulator. It was mentioned in subsection 3.1.4 that the type of transistors in the output stage is the same as in the PMOS shunt topology. Therefore the performance parameters will show a lot of similarities to this topology. References to the earlier analysis of the PMOS shunt topology will be made when applicable, instead of re-doing the analysis.

PSR

Due to the identical output stage architecture, the PSR_{OL} equation that was derived for the PMOS shunt topology in section 2.1.1 is also valid for the dual loop regulator.

At lower frequencies, the PSR is improved by both the VRL and the CRL. As the bandgap circuit will be supplied from V_{out}, its influence on the PSR is neglible. The PSR is given by:

$$PSR = PSR_{OL}[1 + A(s)\beta_v][1 + D(s)\beta_i] \tag{3.19}$$

Emission

For the same reason as with the PSR, the em_{OL} equation that was derived for the PMOS shunt topology in section 2.1.2 is also valid for the dual loop regulator.

At lower frequencies, the emission is kept close to 0dB by the CRL. The emission performance will start to improve beyond the UGF of the CRL. The emission is given by:

$$Emission(s) = \frac{Y_q[1 + A(s)\beta_v]D(s)\beta_i + Y_{dd}}{Y_q[1 + A(s)\beta_v][1 + D(s)\beta_i] + Y_{dd}} \tag{3.20}$$

The equation shows that the emission starts to decrease after the UGF of the CRL. After the UGF of the VRL, the emission is only determined by the ratio of open loop conductances Y_{dd} and Y_q (em_{OL}).

Minimum drop-out voltage

The minimum drop-out voltage of the dual loop regulator is expected to be slightly smaller than the minimum drop-out voltage of the PMOS shunt topology. This can be explained by the current margin that must be taken in the bias current source of the PMOS shunt topology. This margin results in a higher maximum bias current and consequently in a higher maximum V_{DSSAT}.

In this application, just like in the KMA3xx regulator, a diode in the current path is required to prevent a large current flow in case of a reversed connection of the IC supply pins (see section 2.3). This diode will increase the total dropout voltage to V_{DSSAT}+V_{DIODE}, which is equal to the minimum drop-out voltage of the KMA3xx ISR. In other applications, where the diode is not necessary, the dual loop regulator benefits from its low minimum drop-out voltage.

Power efficiency

As discussed in chapter 2, the power efficiency is determined by the ratio of the power delivered to the load and the total power that is drawn from the supply. To improve the power efficiency of the regulator, the amount of current that does not reach the load

must be minimized. Figure 3.11 shows the currents in the regulator that determine the power efficiency. I_{AUX1} and I_{AUX2} are the current required by the HV and LV auxiliary circuits. The auxiliary blocks contain the TA's, the bandgap reference and the start-up circuits.

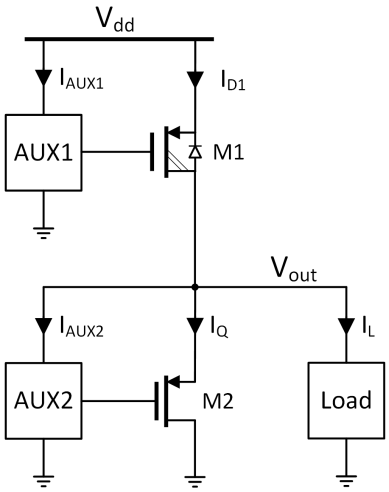

Figure 3.11: Currents that determine the power efficiency of the dual loop regulator.

The power efficiency can now be expressed in these currents:

$$\eta = \frac{P_L}{P_{DD}} = \frac{V_{OUT} I_L}{V_{DD}(I_{D1} + I_{AUX1})} = (1 - \frac{V_{DO}}{V_{DD}}) \frac{I_L}{(I_L + I_Q + I_{AUX1} + I_{AUX2})} \quad (3.21)$$

In order to improve η, the sum of I_Q, I_{AUX1}, and I_{AUX2}, must be kept to a minimum.

The minimum value for I_Q is determined by the magnitude of the maximum load and line steps for which the regulator must be robust. This will be explained in more detail in section 3.1.5. In this work I_Q was chosen to be 100μA.

The magnitude of I_{AUX1} is determined by the circuits in the CRL and the startup circuit. Both currents will be small during operation as the CRL is designed to be slow and the startup circuit will be off. Most likely, $I_Q \gg I_{AUX1}$, and so the extra hardware required for the CRL does not significantly degrade the power efficiency.

The power efficiency of the topology will largely depend on the value chosen for I_Q. As the VRL is designed for high speed, I_{AUX2} may also play a role. In any way, the power efficiency is improved substantially when compared to a regular shunt regulator. Recall from chapter 2 that I_Q in a regular shunt regulator was given by:

$$\begin{aligned} I_Q &= I_B - I_L \\ &> I_{L,max} - I_L \end{aligned} \quad (3.22)$$

I_Q had to be designed for the worst-case load condition. During low load conditions, a lot of current is wasted. Especially for IC's that have a varying current consumption, e.g. due to the switching between different operational modes, the dual loop regulator shows a huge improvement in power efficiency.

Load regulation

Figure 3.12 shows the output stage of the dual loop regulator, while affected by to a static variation in I_L.

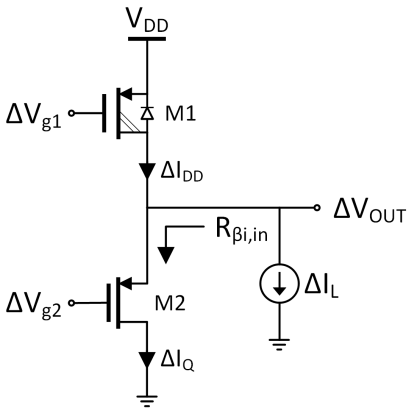

Figure 3.12: Output stage of the dual loop ISR affected by a static change in the I_L.

The static change in the output voltage can be expressed as:

$$\Delta V_{OUT} = \Delta I_Q R_{\beta_i,in} \tag{3.23}$$

The ΔI_Q due to a ΔI_L is given by:

$$\Delta I_Q = -\frac{\Delta I_L}{1 + D_{DC}\beta_i} \tag{3.24}$$

The impedance looking into M2 was given in subsection 3.1.4. The resistance is given by:

$$\begin{aligned} R_{\beta_i,in} &= \frac{R_{sf,out}}{1 + A_{DC}\beta_v} \\ &= \frac{1}{(1 + A_{DC}\beta_v)(g_{m2} + g_{o2})} \end{aligned} \tag{3.25}$$

Substituting 3.24 and 3.25 into 3.23 results in an expression for the load regulation:

$$\frac{\Delta V_{OUT}}{\Delta I_L} = \frac{1}{(1 + A_{DC}\beta_v)(1 + D_{DC}\beta_i)(g_{m2} + g_{o2})} \tag{3.26}$$

The equation shows that the two loops simultaneously improve the load regulation.

Line regulation

Figure 3.12 shows the output stage of the dual loop regulator, while affected by a static variation in V_{DD}.

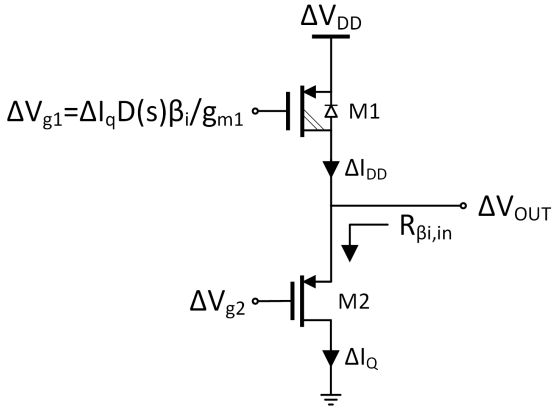

Figure 3.13: Output stage of the dual loop ISR affected by a static change in the supply voltage.

The static change in the output voltage can be expressed as:

$$\Delta V_{OUT} = \Delta I_Q R_{\beta_i,in} \tag{3.27}$$

ΔI_Q can be expressed as a function of ΔV_{DD} and ΔV_{OUT}.

$$\begin{aligned} \Delta I_Q &= \Delta I_{DD} \\ &= (\Delta V_{DD} - \frac{\Delta I_Q D_{DC} \beta_i}{g_{m1}}) g_{m1} + (\Delta V_{DD} - \Delta V_{OUT}) g_{o1} \\ &= \frac{\Delta V_{DD}(g_{m1} + g_{o1}) - \Delta V_{OUT} g_{o1}}{1 + D_{DC}\beta_i} \end{aligned} \tag{3.28}$$

Substituting 3.25 and 3.28 into 3.27 results in an expression for the line regulation:

$$\begin{aligned} \Delta V_{OUT} &= \frac{\Delta V_{DD}(g_{m1} + g_{o1}) - \Delta V_{OUT} g_{o1}}{(1 + D_{DC}\beta_i)(1 + A_{DC}\beta_v)(g_{m2} + g_{o2})} \\ \frac{\Delta V_{OUT}}{\Delta V_{DD}} &\approx \frac{g_{m1} + g_{o1}}{(1 + A_{DC}\beta_v)(1 + D_{DC}\beta_i)(g_{m2} + g_{o2})} \end{aligned} \tag{3.29}$$

The equation shows that the two loops simultaneously improve the line regulation.

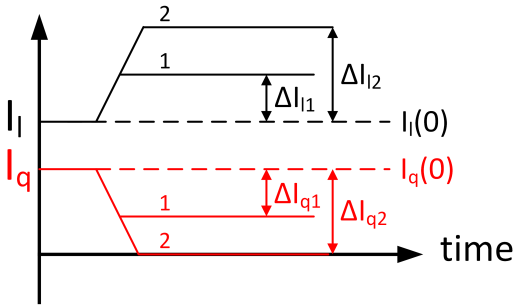

Figure 3.14: Two positive load steps that result in entirely different types of transient behavior.

Load Transient

During operation, it is desirable to always keep M2 in strong inversion. A positive load step above a certain magnitude can cause M2 to enter the sub-threshold region. Figure 3.14 shows this situation in more detail.

Two different load steps are defined:

1. $\Delta I_{l1} < I_q(0)$
   The change in load current is directly drawn from I_q, and so $\Delta I_{l1} = \Delta I_{q1}$. As then $I_q(0) > \Delta I_{q1}$, some bias current remains available to keep M2 in strong inversion. The circuit behaves as expected from to the small signal approximation.

2. $\Delta I_{l2} > I_q(0)$ The change in load current can not be fully drawn from I_q, and so $\Delta I_{l2} > \Delta I_{q2}$. I_q will drop to 0A causing M2 to enter the sub-threshold region. The extra current required by the load, $\Delta I_{l2} - \Delta I_{q2}$, will be provided by C_{OUT}, causing the output voltage to drop.

Figure 3.15 shows the system response to a load step belonging to the first category.

When t<0, the system is in a steady state; $I_{dd} = I_l + I_q$ and the output voltage is at its nominal value.
At t=0, I_l steps up with ΔI_{l1}. The VRL will respond and after $t' + \tau_{VRL,1}$ the difference in V_{out} will converge to:

$$\Delta V_{out1} = \frac{\Delta I_{l1}}{(1 + A_v\beta_v)(g_{m2} + g_{o2})} \tag{3.30}$$

The CRL will slowly adjust I_{dd} to regulate I_q to its defined value. After $\tau_{CRL,1}$ the difference in V_{out} will converge to:

$$\Delta V_{out2} = \frac{\Delta I_{l1}}{(1 + A_v\beta_v)(1 + D_i\beta_i)(g_{m2} + g_{o2}} \tag{3.31}$$

Figure 3.16 shows the system response to a load step belonging to the second category.

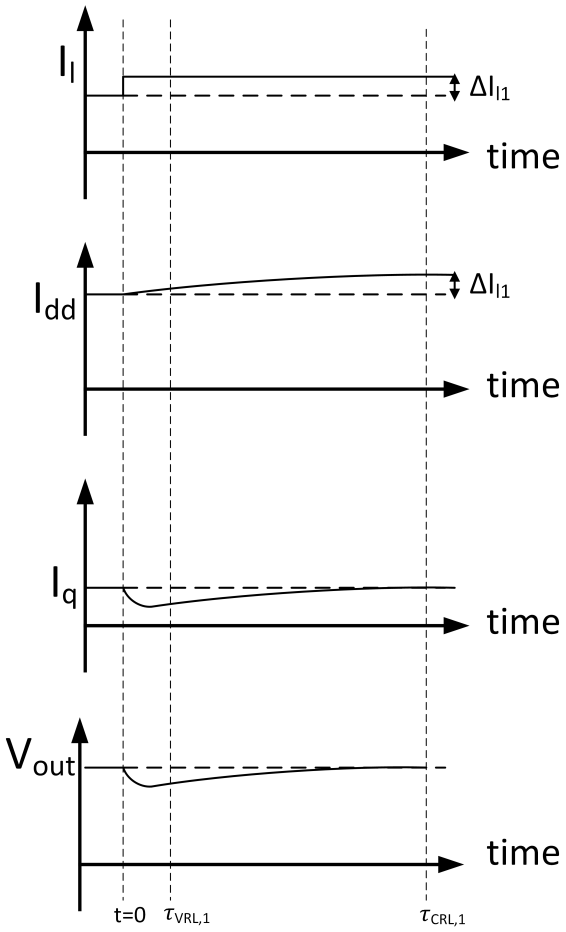

Figure 3.15: Load transient response for load steps where $\Delta I_{l1} < I_q(0)$.

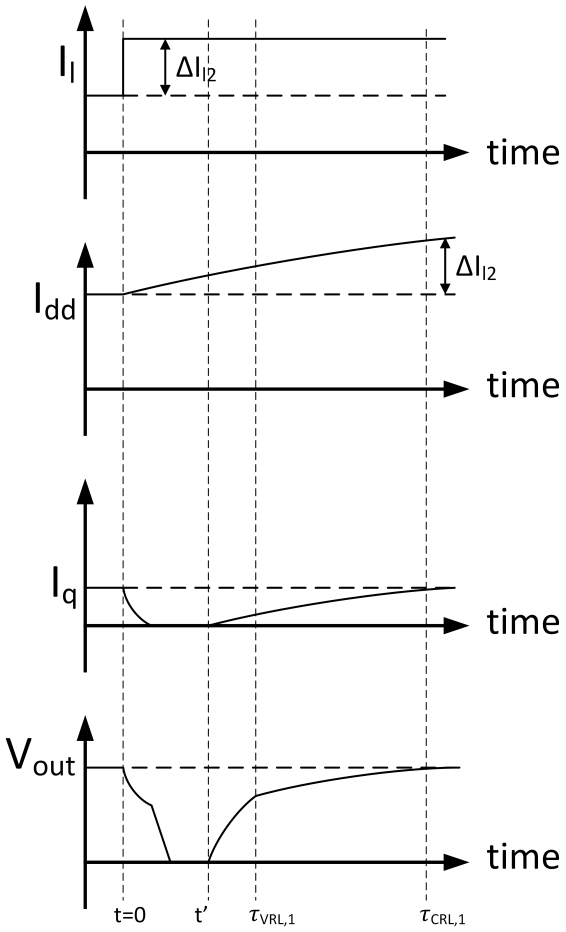

Figure 3.16: Load transient response for load steps where $\Delta I_{l2} > I_q(0)$.

As $\Delta I_{l2} > I_q(0)$, I_q will drop to zero after the loadstep. At this moment the VRL is broken and the output can be considered floating. The difference between ΔI_{l2} and $I_q(0)$ will be drawn from C_{OUT}. V_{out} will drop with a slope of:

$$\frac{\delta V_{out}}{\delta t} = \frac{I_q(0) - \Delta I_{l2}(t)}{C_{OUT}} \tag{3.32}$$

The CRL will slowly increase i_{dd}. At the point where $I_q > 0$, the VRL becomes active again. V_{out} is regulated to ΔV_{out1} (equation 3.30). The CRL will slowly adjust I_{dd} further until the error in V_{out} is given by ΔV_{out2} (equation 3.31).

Line transient

The line transient behavior can be divided in two similar situations as was done during the analysis of the load transient behavior. A line transient will cause a change in I_{dd} (figure 3.17).

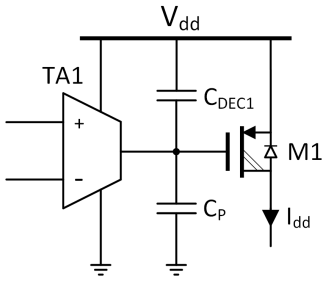

Figure 3.17: Line transient behavior of the dual loop ISR.

As the output impedance of TA1 is generally quite high, C_P will result in a non-zero gate-source voltage for medium to high frequencies. The resulting current flow is given by:

$$\Delta I_{dd} = \Delta V_{dd} \frac{C_P}{C_{DEC1} + C_P} g_{m1} \tag{3.33}$$

A negative line step above a certain magnitude can cause M2 to enter the sub-threshold region. Two different line steps are defined:

1. ΔV_{dd1}, where $\Delta I_{dd1} < I_q(0)$

   The change in I_{dd} is directly drawn from I_q, and so $\Delta I_{dd1} = \Delta I_{q1}$. As then $I_q(0) > \Delta I_{q1}$, some bias current remains so that M2 is kept in strong inversion. The circuit behaves as expected according to the small signal approximation.

2. ΔV_{dd2}, where $\Delta I_{dd2} > I_q(0)$

   The change in I_{dd} can not be fully drawn from I_q, and so $\Delta I_{l2} > \Delta I_{q2}$. I_q will drop to 0A, causing M2 to enter the sub-threshold region. The extra current required by the load, $\Delta I_{dd2} - \Delta I_{q2}$, will be provided by the output capacitor causing the output voltage to drop.

Figure 3.18 shows the system response to a line step belonging to the first category.

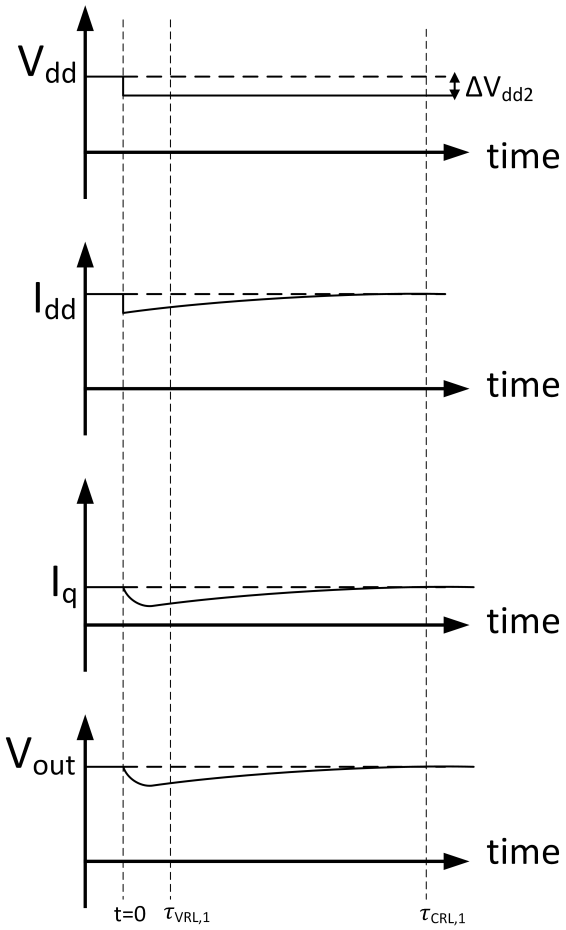

Figure 3.18: Line transient response for line steps where $\Delta I_{dd2} < I_q(0)$.

When t<0, the system is in a relaxed state; $I_{dd} = I_l + I_q$ and the output voltage is at its nominal value.

At t=0, V_{dd} steps down with ΔV_{dd1} resulting in a drop in I_{dd}, ΔI_{dd1}. The VRL will respond and after $t' + \tau_{VRL,1}$ the difference in V_{out} will converge to:

$$\Delta V_{out1} = \frac{\Delta I_{l1}}{(1 + A_v\beta_v)(g_{m2} + g_{o2})} \tag{3.34}$$

The CRL will slowly adjust I_{dd} to regulate I_q to its defined value. After $\tau_{CRL,1}$ the difference in V_{out} will converge to:

$$\Delta V_{out2} = \frac{\Delta I_{l1}}{(1 + A_v\beta_v)(1 + D_i\beta_i)(g_{m2} + g_{o2})} \tag{3.35}$$

Figure 3.19 shows the system response to a load step belonging to the second category.

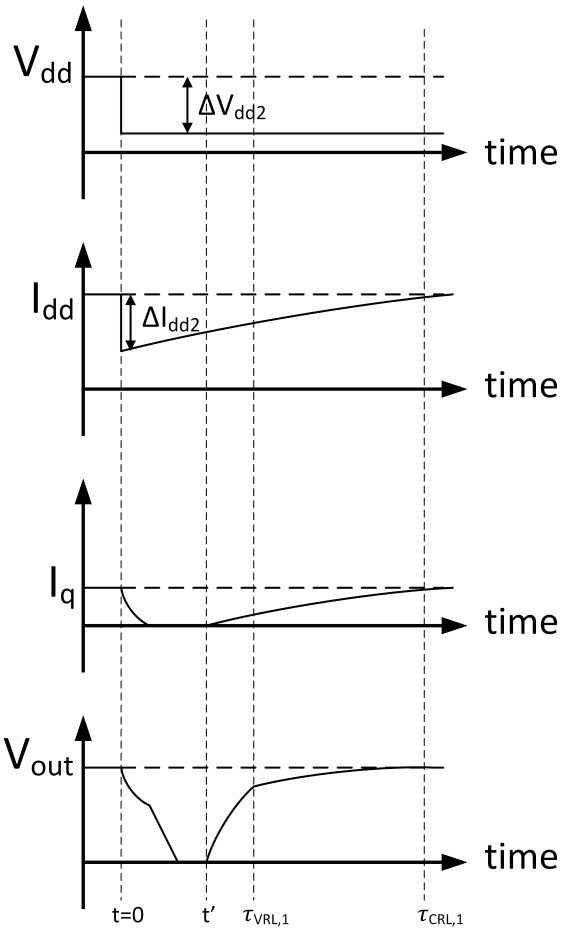

Figure 3.19: Line transient response for line steps where $\Delta I_{dd2} > I_q(0)$.

As $\Delta I_{dd2} > I_q(0)$, I_q will drop to zero after the line step. At this moment the VRL is broken and the output can be considered floating. The difference between ΔI_{dd2} and $I_q(0)$ will be drawn from C_{OUT}. V_{out} will drop with a slope of:

$$\frac{\delta V_{out}}{\delta t} = \frac{I_q(0) - \Delta I_{dd2}(t)}{C_{OUT}} \tag{3.36}$$

The CRL will slowly increase i_{dd}. At the point where $I_q > 0$, the VRL becomes active again. V_{out} is regulated to ΔV_{out1} (equation 3.34). The CRL will slowly adjust I_{dd} further until the error in V_{out} is given by ΔV_{out2} (equation 3.35).

Gain-Bandwidth Product

In the topologies from chapter 2, all output stage transistors were required to handle the maximum expected load current, $I_{L,max}$. Large transistors have to be used to handle this current, resulting in large parasitic capacitances. These capacitances limit the GBW of the regulation loop.

In the dual loop design, the output stage transistor only needs to handle I_Q, and can therefore be kept relatively small. Furthermore, the entire VRL can be implemented in the LV domain, keeping the capacitance inside the loop to a minimum. The dominant pole of the VRL is at the output of the regulator, and is located at high frequencies due to the source follower output stage.

Area

In section 2.3, it was shown that the bandgap reference consumes the most area in the KMA3xx design. Therefore it is expected that the influence on the total area in the design will be relatively small. The dual loop regulator will however be slightly larger due to a couple of reasons:

1. The MOS transistor carrying I_L is implemented as a HVPMOS. Due to the lower conductivity in p-type material, the PMOS needs to be bigger in order to handle the same amount of current for equal overdrive.
2. A large C_{DEC1} is required to avoid coupling from the supply to the output.
3. The CRL requires an extra reference voltage and TA.

3.1.6 System overview

Figure 3.20 shows the functional architecture of the total DL ISR.

Several options for the implementation of D(s) and β_i were analyzed. A β_i of unity was chosen to reduce the influence of mismatch on I_Q. D(s) is implemented by a small sense resistor in combination with a low transconductance amplifier. This was found to be the

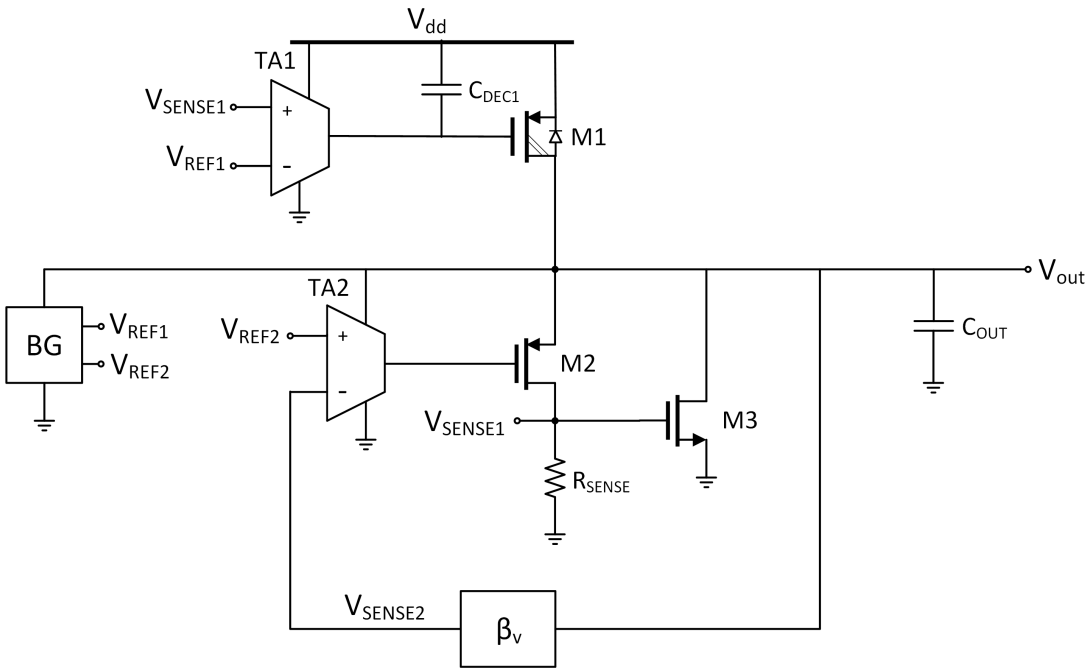

Figure 3.20: Functional architecture of the DL ISR

best option to reach a low UGF in the CRL. The difficulty in reaching a low UGF is in the fact that g_{m1} is large and only a small capacitor can be used for on-chip integration.

In order to reach the required system performance, specifications for all components will be determined in this section.

Transconductance amplifiers

Table 3.1 shows the specifications for both transconductance amplifiers.

	G_m	V_{in}		V_{out}		R_{OUT}	**PSR**	$V_{off,in}$
		min	**max**	**min**	**max**			
TA1	500nS	-0.5V	0.1V	0.2V	20V	$>$500MΩ	-	10mV
TA2	4mS	-0.1V	0.9V	0.2V	1.8V	-	20dB	10mV

Table 3.1: Specifications of the CMOS14 A-BCD9 process.

As TA1 is supplied directly by V_{dd}, it must be implemented in the HV domain. The voltage at the positive input (V_{SENSE1}) is the product of I_q and R_{SENSE}. As I_q may vary a lot due to high frequency load variations, a small R_{SENSE} is chosen (1kΩ) to keep M2 in saturation and to reduce the required dynamic input range of TA1. In order to bias I_Q to 100μA, V_{SENSE1} is regulated to 100mV. A maximum input referred offset of 10mV will be allowed, limiting the resulting error in I_Q to 10%.

TA2 is supplied by the output voltage and may be implemented in the LV domain. As TA2 has a finite PSR, $PSR * V_{out}$ is seen at the gate of M2. This effectively increases

the impedance looking into M2, $Z_{\beta_{i,in}}$. In order to keep $Z_{\beta_{i,in}}$ low, the PSR of TA2 should be at least 20dB.

Feedback network

Table 3.2 shows the specifications of the feedback network.

	Gain	$V_{in,max}$	R_{in}	$V_{noise,out}$
β_v	0.5	1.95V	1.8M	200nV/$\sqrt{Hz}$

Table 3.2: System specifications of the feedback network.

The bandgap reference of the KMA3xx family will be re-used in this design, resulting in a fixed bandgap voltage of 900mV. In order to regulate V_{out} to 1.8V, the feedback network should have a gain of 0.5.

Output stage transistors

The output transistors are sized such that the maximum expected power dissipation can be handled over the entire temperature range (-40°C to 210°C). The requirements for the output stage transistors are given in table 3.3.

	$I_{DS,max}$	$V_{DS,min}$	$V_{DS,max}$
M1	10mA	800mV	20V
M2	500μA	1.3V	1.95V

Table 3.3: System specifications of the output stage transistors.

Capacitances

The type and size for the two main capacitances in the circuit must be determined. The requirements for the capacitances are given in table 3.4.

	Value	$V_{AB,max}$	$I_{leak,max}$
C_{DEC1}	30pF	3.3V	1nA
C_{OUT}	140pF	1.95V	10μA

Table 3.4: System specifications of the capacitances.

3.1.7 Start-up behavior

To ensure proper start-up, the ISR must be forced to the desired operational state. Other stable states where the ISR might converge to pose a threat to the reliability of the ISR and must be made unstable. Figure 3.21 again shows the total system of the dual loop ISR.

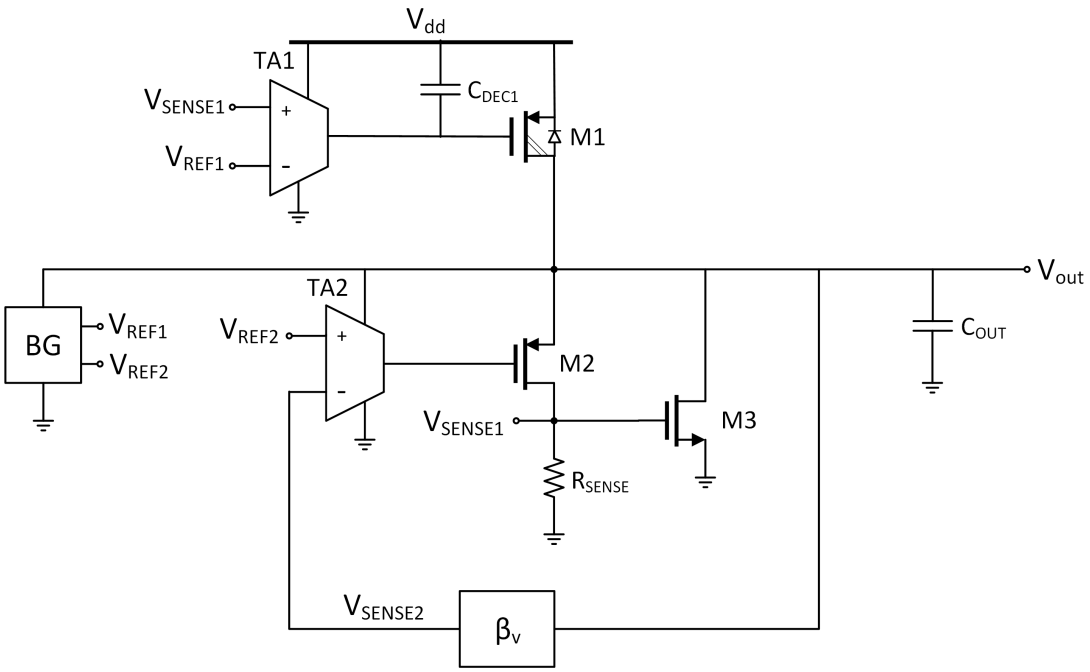

Figure 3.21: Total dual loop ISR.

Initially, when V_{dd} is applied, the gate of M1 will follow and no current will flow through M1. V_{out} will remain low and so the bandgap circuit will not start. Without voltage and current references, TA1 will not operate and the circuit will remain in this state.

In order to start the regulator, V_{out} must be kept stable at a voltage large enough to start the bandgap reference. After the bandgap reference has started, the circuit should converge to the desired functional state. The start-up circuitry should have no negative effects on the performance of the regulator during functional mode.

3.2 Circuit design

In this section, the circuit implementations for the system level blocks are presented. A justification will be given for certain design choices during the implementation process.

3.2.1 TA1

As the TA is specified to have a relatively low transconductance, several techniques were examined [9] to reduce the transconductance of the TA. These techniques are:

1. Current Division (CD)
2. Source Degeneration (SD)
3. Floating Gate input pair (FG)
4. Bulk Driven input pair (BD)

Without diving into the concepts of the different techniques, the findings from [9] are presented. Table 3.5 shows the performance of these techniques compared to a reference TA. The reference TA simply uses a very low bias current (2nA) to achieve a low conductance. In our application, such a solution is not reliable due to high temperature leakage.

Parameter design	**Ref.**	**SD+CD**	**FG+CD**	**BD+CD**
G_{M0} (nS)	11.6	11.55	11.51	11.24
Linearity@1% HD_3, 1 Hz (mVpp)	162	240	330	900
Input referred noise (μ Vrms)	12.04	17.29	26.03	70.3
Signal to Noise ratio (SNR)(dB)	73.5	73.9	73.0	73.1
Max Common Mode input (V)	0.18	0.2	1.5	1.6
Bias I_{ss} (nA)	2	100	200	500
Supply $V_{DD} = \|V_{SS}\|$ (V)	1.35	1.35	1.35	1.35
Power (μW)	0.0162	1.35	1.62	4.05
Total area (mm^2)	1.44	0.21	4.65	0.22
Inversion level of driver transistor i_f	10	15	17	31
Normalized power	1	83.3	100	250
Normalized area	6.71	1.00	21.61	1.01

Table 3.5: Performance comparison between different techniques for implementing extremely low transconductances. These simulation values have been presented in [9].

SD+CD is chosen as the preferred technique, mainly due to its possibility to operate under a low common mode input voltage. Other advantages like low noise, relatively small total area, low power and low noise are additional benefits. The technique is less exotic than a floating gate or bulk driven solution making it more reliable in an existing process.

Architecture

Figure 3.22 shows the final architecture of TA1. A differential PMOS input pair with a thick gate oxide is chosen as it can handle low common mode input voltages and has a low transconductance. M3 and M4 are biased in the linear region and act as source degeneration resistors. They are chosen over poly-silicon resistors due to a higher resistance over area ratio.

The effective transconductance of the source degenerated stage is given by:

$$G_{m,eff} = \frac{g_m}{1 + g_m R_{deg}} \tag{3.37}$$

Where R_{deg} is the effective resistance over M3 and M4. The value of R_{deg} is dependent on the W/L ratio of M3 and M4 and the voltage drop across D1.

The differential input voltage at which the output current will saturate is approximately given by:

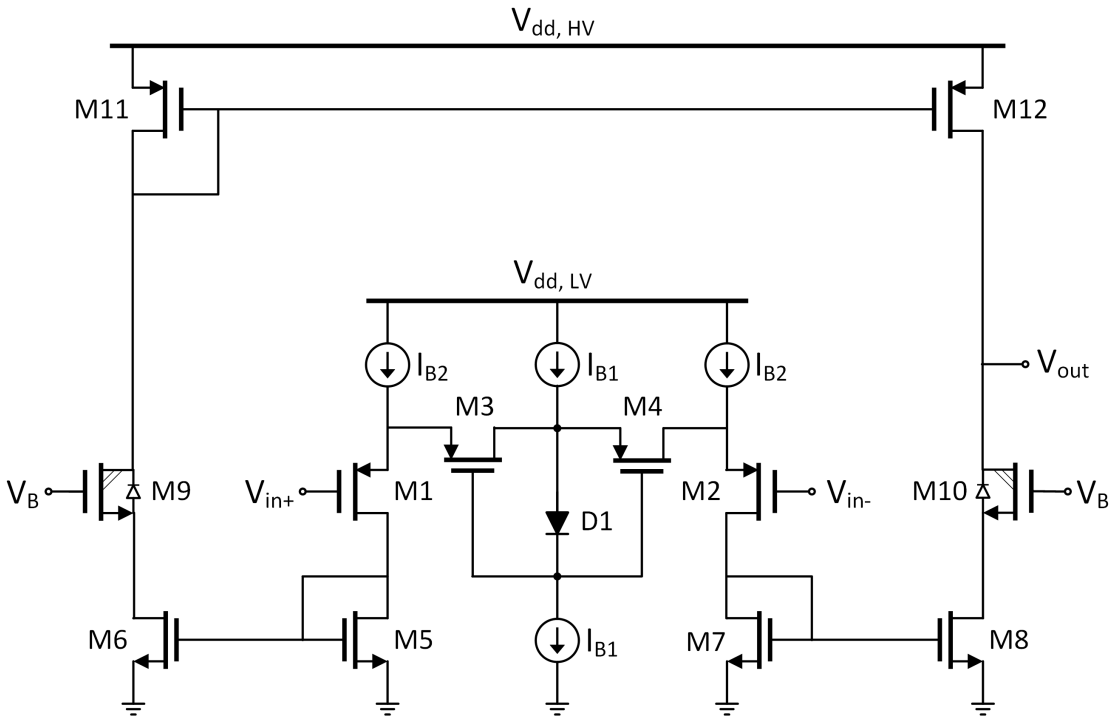

Figure 3.22: Architecture of TA1.

$$V_{in,max} \approx I_{B2} R_{deg} \tag{3.38}$$

Within the input range, $-V_{in,max} < V_{in} < V_{in,max}$, M3 and M4 must operate in the linear region. Figure 3.23 shows the linear biased PMOS transistors with voltage source V_x across them.

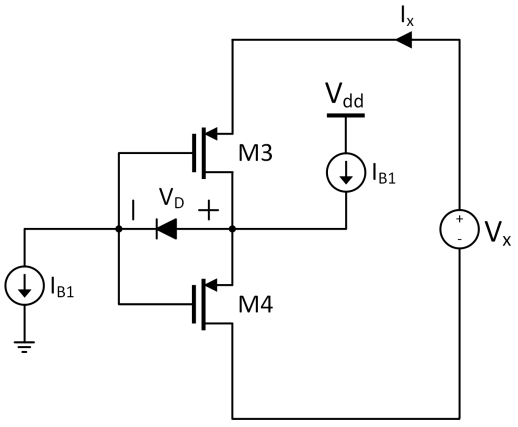

Figure 3.23: Two PMOS transistors biased in the linear region.

M3 is in the linear region, as long as:

$$V_D > |V_{TH3}| \tag{3.39}$$

As the gates of M3 and M4 are connected and $V_x > V_{sd4}$, it holds that $V_{sg3} > V_{sg4}$. Because the currents through M3 and M4 must be equal, M3 is forced deep into the linear region.

For small values of V_x, M4 is in the linear region. At the point where M4 goes into saturation, the current through M4 is given by:

$$\begin{aligned} I_{D4} &= \frac{k_4}{2}(V_D - |V_{TH4}|)^2 \\ &= \frac{k_4 I_{B1}}{k_D} \end{aligned} \tag{3.40}$$

Where: $k_x = \mu_x C_{ox}(W/L)_x$. It is assumed that D1 is implemented as a MOS diode.

So as long as $I_{D4} < \frac{k_4 I_{B1}}{k_D}$, M4 is in the linear region. In order words, for $I_{B2} < \frac{k_4 I_{B1}}{k_D}$ both M3 and M4 remain in the linear region over the entire current range of the amplifier.

Sizing

If the inputs of the TA would be shorted, the output current would be nonzero due to transistor mismatch. Transferring this current back to the input results in a relatively large voltage offset, as the TA is designed for a low g_m.

The offset can be reduced by minimizing the absolute value of this mismatch current. This was done by keeping I_{B2} small; in the sub micro range. Also M5-M8, M11, and M12, are chosen to be large transistors with a small W/L ratio. This reduces the current mismatch due to size and V_{TH} variations.

Transistor	W/L	Gate Oxide
M1,M2	8/10	7.2nm
M3,M4	0.768/24	2.9nm
M5,M6,M7,M8	6/40	2.9nm
M9,M10	6/1	7.2nm
M11,M12	6/20	7.2nm
D1	0.768/15	2.9nm

Table 3.6: Sizing of the transistors in TA1.

3.2.2 TA2

TA2 is supplied by the output voltage of the ISR, thus it can be implemented using fast LV transistors. The main challenge in the design is obtaining a high bandwidth while keeping the VRL stable.

Architecture

To increase the LP product of the TA, a two stage amplifier is proposed (figure 3.24). In order to reach the specification for the PSR, a standard differential PMOS topology was chosen cascaded by a NMOS gain stage. Current sources I_{B1} and I_{B2} isolate the supply from the output voltage.

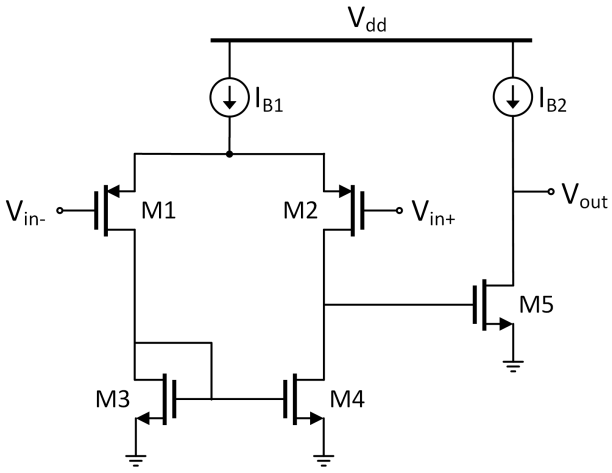

Figure 3.24: Architecture of TA2.

Sizing

As described in section 3.1.3, the internal poles of the TA should be non-dominant in the VRL. Small transistors and large biasing currents were chosen in order to keep the internal poles at high frequencies.

Transistor	W/L	Gate Oxide
M1,M2	0.786/0.16	2.9nm
M3,M4	0.786/0.16	2.9nm
M5	3.5/0.16	2.9nm

Table 3.7: Sizing of the transistors in TA2.

3.2.3 Feedback network

The feedback network has the output voltage of the regulator as its input and the negative input voltage of TA2 as its output. It is in the LV domain. A phantom zero [10] was realized in the feedback network for frequency compensation of the VRL.

Architecture

Figure 3.25 shows the feedback network of the VRL. The ratio of R_1 and R_2 determines the DC gain of the network. C_1, C_2, and R_{PHZ}, are used for frequency compensation.

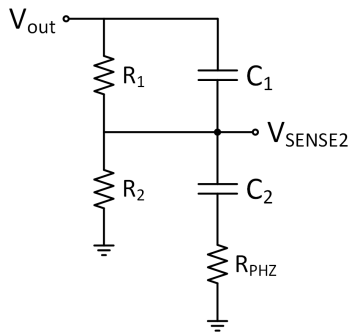

Figure 3.25: Architecture of TA2.

The resistances are implemented as n+ poly-silicon resistors placed in a nwell. This type of resistor was chosen for its high precision, reasonable sheet resistance and low sensitivity to temperature.

The capacitances are implemented with Metal-Insulator-Metal (MIM) capacitors for high precision. The capacitors have a maximum leakage current of 10nA/cm^2. The resulting offset in the gain of the feedback network can be considered to be negligible.

Sizing

The sizing of the resistors is a trade-off between noise and power consumption. As V_{out} is a low ohmic node, the total thermal noise at the input of TA2 is equal to the thermal noise of R_1 and R_2 in parallel.

$$v_{noise,TA2} = \sqrt{4kT(R1||R2)} \tag{3.41}$$

The noise can be translated to the output of the regulator by multiplying it with the closed loop gain.

$$\begin{aligned} v_{noise,out} &= v_{noise,TA2}\frac{A_v(s)}{1+A_v(s)\beta_v} \\ &\approx \frac{\sqrt{4kT(R1||R2)}}{\beta_v} \end{aligned} \tag{3.42}$$

Component	W/L	Value
R_1,R_2	0.32/2425	500kΩ
R_{PHZ}	0.32/48.50	20kΩ
C_1,C_2	20/40	1.03pF

Table 3.8: Component sizes of β_v

The noise referred to the output of the regulator with the component values from table 3.8), is given by:

$$v_{noise,out} \approx 163.3nV/\sqrt{Hz} \tag{3.43}$$

The static current consumption equals:

$$i_{static} = \frac{V_{out}}{R_1 + R_2} = 1.8\mu A \tag{3.44}$$

The frequency at which the phantom zero occurs is given by:

$$\begin{aligned} z_{PH} &= \frac{1}{2\pi R_{PHZ} C_2} \\ &= 7.7MHz \end{aligned} \tag{3.45}$$

3.2.4 Bandgap and current references

The bandgap voltage and current references of the KMA3xx family will be re-used in the current design. Therefore, minimum design effort is put in this circuit. However, minor adjustments had to be made to fulfill the needs of the new design.

Original circuit

The bandgap reference in the KMA3xx is mainly designed for a constant output voltage over a very large temperature range (-40°C to 210°). Figure 3.26 shows the architecture of the bandgap circuit.

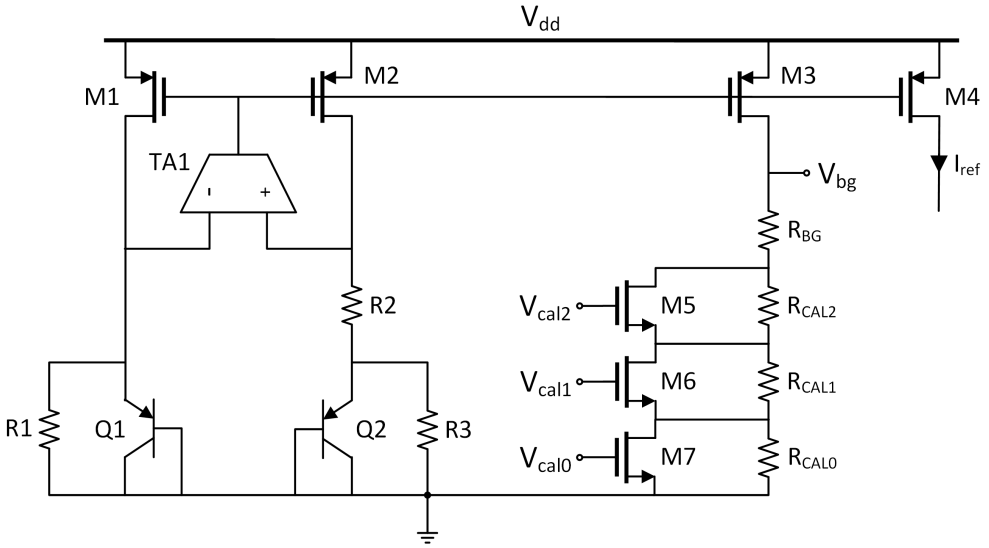

Figure 3.26: Architecture of the bandgap reference from the KMA3xx family.

The bandgap reference circuit can be calibrated by setting the $V_{cal,x}$ bits. For circuit readability, only 3 out of 5 bits are shown in this figure.

Adjustments

The core architecture of the bandgap reference is left untouched. Extra current references were added by placing transistors in parallel to M4. These transistors add parasitic capacitance to the output node of TA1. Care must be taken to not substantially increase the start-up time of the circuit.

3.2.5 Output stage MOS transistors

The sizing of the output stage MOS transistors is based on the maximum drain current, I_D, and minimum V_{DS}, $V_{DS,min}$. The transistors should stay in saturation over the entire temperature range.

	M1			**M2**		
Type	PMOS60V			PMOS		
Width	3000μm			8μm		
Length	2μm			0.32μm		
$V_{DS,min}$	700mV			1.1V		
	I_D			I_D		
	1mA	5mA	10mA	10μA	100μA	500μA
T [°C]	$V_{DS,SAT}[mV]$			$V_{DS,SAT}[mV]$		
-40	153.2	288.4	397.1	124.5	261.5	577.3
25	176.5	340.6	471.9	140.9	295.0	636.8
210	5.6	14.1	19.7	195.7	423.5	896.9
	$g_m[mS]$			$g_m[mS]$		
-40	10.2	24.1	33.4	169.6	591.3	1123
25	30.6	20.7	28.9	148.1	540.0	1030
210	5.6	14.1	19.7	98.8	395.7	807.7
	$g_o[\mu S]$			$g_o[\mu S]$		
-40	8.5	50.4	128.3	0.6	3.4	15.1
25	8.7	56.1	163.7	0.5	3.3	15.4
210	9.4	95.2	796.4	0.4	3.1	18.9

Table 3.9: Saturation voltage and important small signal parameters for the output stage transistors over the required temperature and current range.

3.2.6 Capacitors

The capacitors play a crucial role in the EMC behavior of the regulator. Table 3.10 shows the properties of different types of capacitors that are available in the process.

The MIM capacitor does not consume area in the active layer, as it is implemented in the top metal layer. Therefore, even though MIM capacitors have a lower capacitance per area value, it is still an attractive option. MIM capacitors are also very linear, have a high precision, and can withstand high voltages before breaking down. There are still some reliability problems with MIM capacitors in the current process. The capacitors

Capacitance type	Density	$V_{breakdown}$	Linearity	I_{leak}
Metal-Insulator-Metal	1.25fF/μm^2	12V	Good	10nA/cm^2
Gate Oxide 1	9.2fF/μm^2	1.95V	Bad	-
Gate Oxide 2	4.6fF/μm^2	3.6V	Bad	-

Table 3.10: Properties of various capacitor types available in the A-BCD9 process.

show a varying leakage current and may breakdown at a lower voltage then specified. Voltage stress during testing is required to ensure the integrity of the MIM capacitor.

Gate Oxide (GO) capacitances are implemented in the active area and have a high capacitance per area value as the gate oxide is extremely thin. The thin oxide is vulnerable to strong electric fields and so the breakdown voltage is relatively small.

Decoupling capacitance A large C_{DEC1} is beneficial for both emission and PSR at higher frequencies as it compensates the effect of $C_{GD1,ov}$. As TA1 has a low transconductance, a current error at the output of TA1 will translate to a large offset voltage at its input. The use of a MIM capacitor is excluded due to its finite leakage current. A GO2 capacitor is chosen as its breakdown voltage is equal to the gate source breakdown voltage of M1.

Output capacitance The output capacitance was kept equal to the capacitance of the KMA3xx regulator; A parallel combination of MIM and GO1 capacitance. The GO1 capacitance has a breakdown voltage of 1.95V so care must be taken to not exceed this voltage during start-up. The total capacitance at the output is 140pF.

3.2.7 Start-up circuit

The proposed solution is to use a start-up current to pull down the gate of M1 through D1 (figure 3.27). C_{DEC1} is discharged until $I_{D3} = I_{dd}\frac{(W/L)_3}{(W/L)_1} = I_{STARTUP}$. M4 ensures that V_{out} remains at V_{gs3}, enabling the bandgap reference to start. After the start of the bandgap reference, the circuit will converge to the required state. The start-up time is approximately 40μs. The performance during functional mode is untouched by the start-up circuitry.

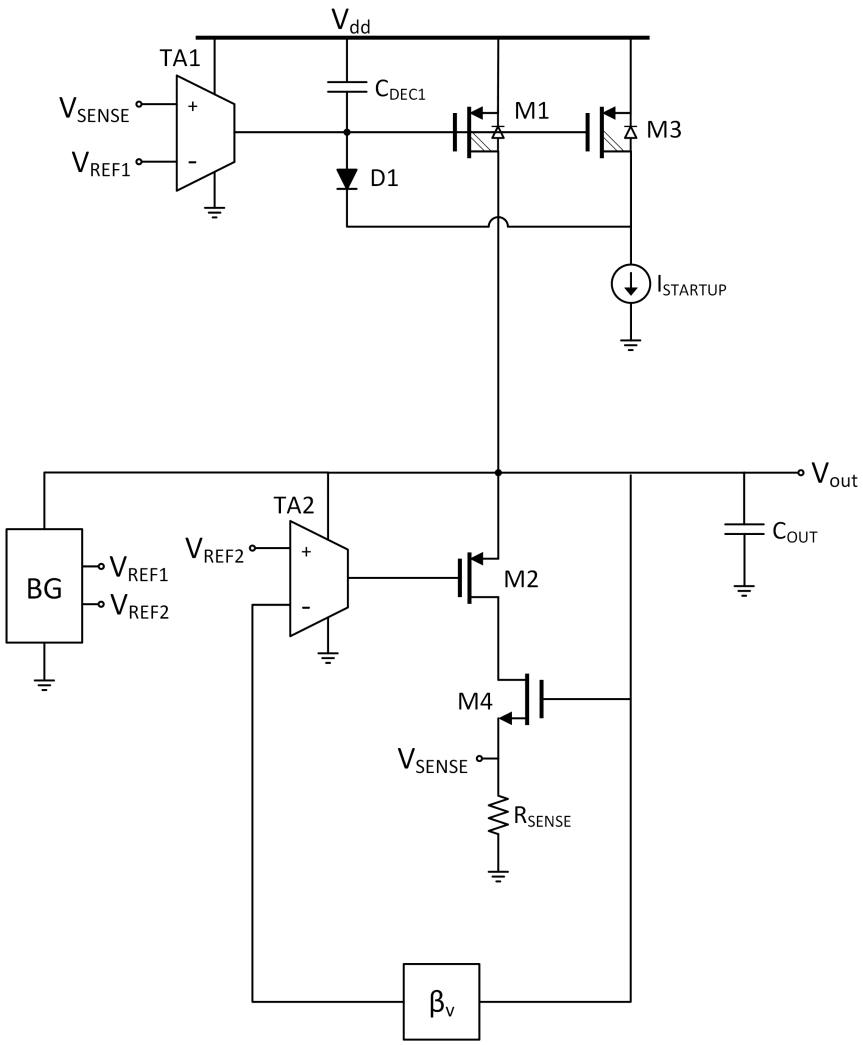

Figure 3.27: Proposed solution for a fast, well controlled start-up.

Chapter 4

Simulations

This chapter presents the simulation results of the dual loop ISR. The performance is then compared to the KMA3xx ISR.

4.1 Loop simulations

In order to have a stable ISR, both the CRL and the VRL should have the desired behavior. The loop gains of the CRL and the VRL should approximate the shapes that were specified in section 3.1. The phase margin of both loops must be above 70°over all conditions. Loop analysis was done by using the stability analysis virtuoso. This enables analysis without having to cut the loop.

4.1.1 Current regulation loop

Figure 4.1 shows the loop gain and phase of the CRL. The gain is mainly dependent on temperature and I_L.

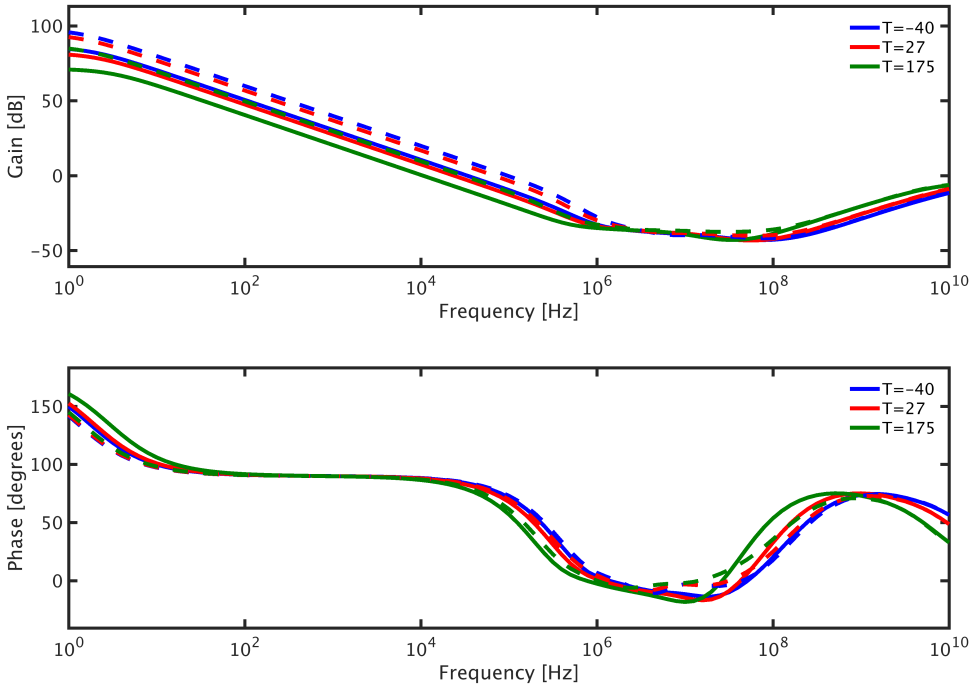

Figure 4.1: Gain and phase curves of the CRL with $C_L = 100pF$. The solid lines show the performance when $I_L = 1mA$, while dotted lines show the performance for $I_L = 10mA$.

Table 4.1 shows the phase margins of the CRL for different values of C_L. The phase margin is above 70°for all corners as long as $C_L < 1nF$.

C_L	**1pF**		**100pF**		**1nF**	
I_L	1mA	10mA	1mA	10mA	1mA	10mA
T [°C]	Phase Margin		Phase Margin		Phase Margin	
-40	83.8	73.7	83.7	73.6	83.4	72.6
27	84.6	76.2	84.6	76.1	84.3	75.3
175	86.4	81.1	86.3	81.0	86.1	80.5

Table 4.1: Phase margin of the CRL for different temperatures, C_L and I_L.

TA1

Figure 4.2 shows the transconductance of TA1. The dominant internal pole of TA1 is located at approximately 1MHz. This pole is the second dominant pole in the CRL, $p_{CRL,2}$. In subsection 3.1.2 this pole was ideally placed at 500kHz. In order to meet the stability criteria during high loading conditions, the pole had to be shifted to a higher frequency.

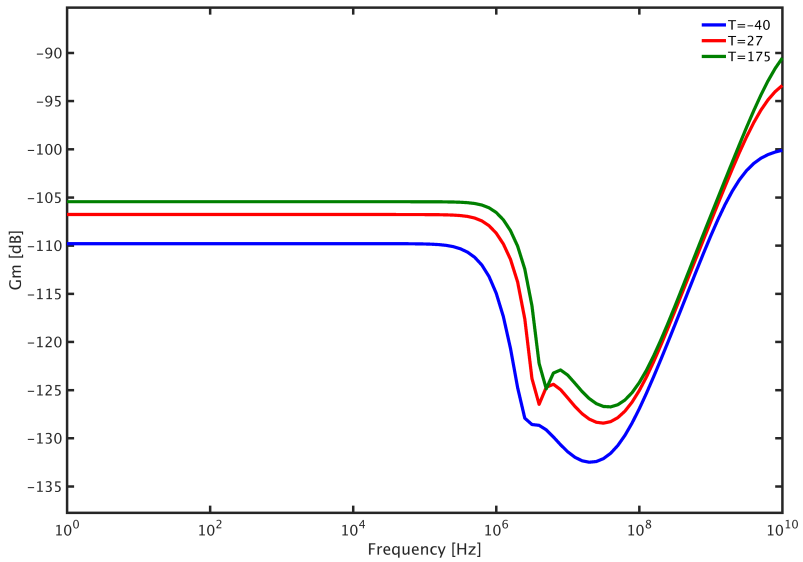

Figure 4.2: Transconductance of TA1.

Figure 4.3 shows the V-I relation of TA1 over the specified input range. It can be seen that the TA is highly linear due to the source degeneration.

Figure 4.4 shows the PSR of TA1 for different load capacitors. The load capacitance is assumed to be connected from the output of the amplifier to V_{dd}. Note that on system level, the PSR of the ISR improves when the PSR of TA1 is closer to 0dB.

The input referred offset is mostly determined by transistor mismatch and thus statistical simulations must be done. Figure 4.5 shows the test setup for the offset.

I_{off} is measured while the input terminals are shorted. V_{off} is then calculated by dividing I_{off} by the nominal transconductance of TA1. Figure 4.6 shows the probability density function of V_{off} after Monte Carlo simulation. Global process variations and mismatch are both taken into account.

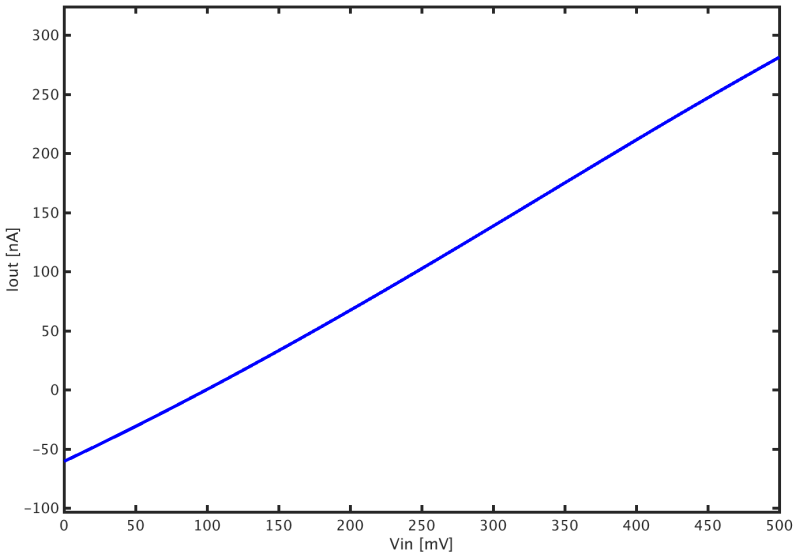

Figure 4.3: V-I curve of TA1.

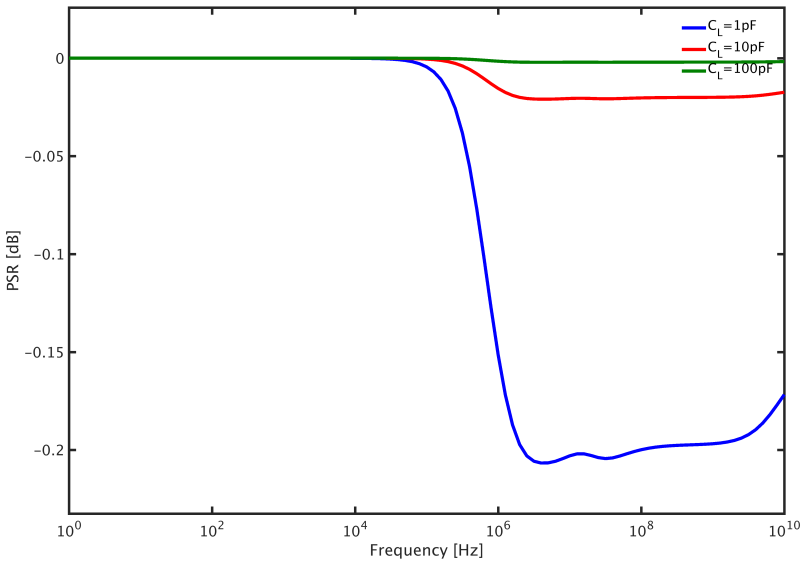

Figure 4.4: PSR of TA1 for different output capacitances.

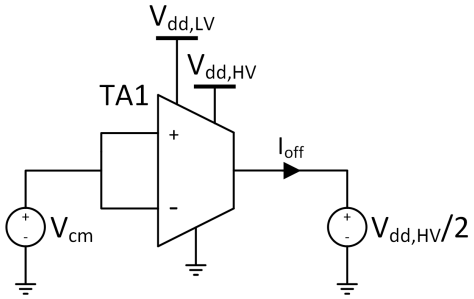

Figure 4.5: Simulation setup to measure the input referred offset of TA1.

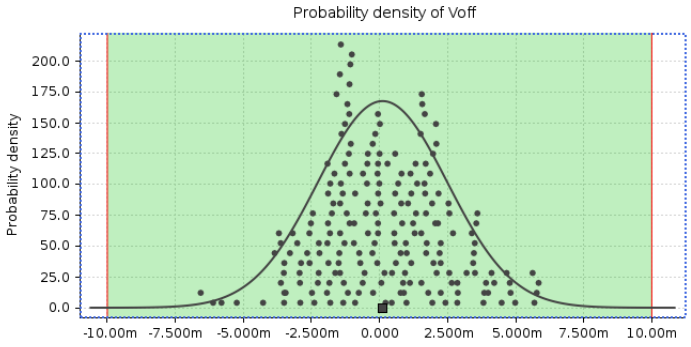

Figure 4.6: Statistical analysis of V_{off} of TA1 through Monte Carlo simulation.

The 3σ boundaries are located at -7.03mV and 7.25mV and so the specification is met. It is likely that the bandgap voltage connected to the negative terminal of TA1, V_{REF1}, will be calibrated. In this case the calibration can be used to compensate for V_{off}.

4.1.2 Voltage regulation loop

Figure 4.7 shows the loop gain and phase of the VRL. The gain is mainly dependent on temperature. I_L only has effect in the mid frequency band (10kHz to 10MHz).

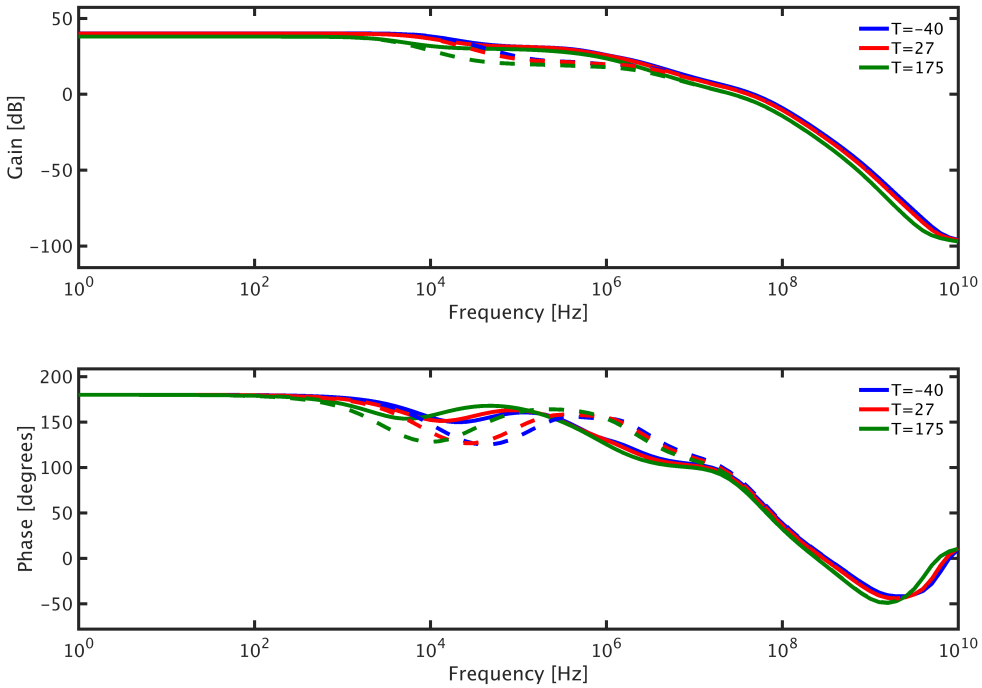

Figure 4.7: Gain and phase of the VRL with $C_L = 100pF$. The solid lines show the performance when $I_L = 1mA$, while dotted lines show the performance for $I_L = 10mA$.

It can be seen that a pole and zero pair is found around the UGF of the CRL. This effect was explained in subsection 3.1.4. A high value for I_L drives these pair apart causing a

gain reduction in the mid frequency range. A large C_{DEC1} will improve the pole zero cancellation and restore the gain.

Table 4.2 shows the phase margins of the VRL for different values of C_L. It was found that the phase margin is above 70°for all corners as long as $C_L > 50pF$.

C_L	**1pF**		**100pF**		**1nF**	
I_L	1mA	10mA	1mA	10mA	1mA	10mA
T [°C]	Phase Margin		Phase Margin		Phase Margin	
-40	56.3	59.0	85.0	87.5	96.7	100.2
27	59.2	62.1	87.7	90.5	95.5	99.1
175	73.2	77.5	94.7	99.1	93.2	98.3

Table 4.2: Phase margin of the VRL for different temperatures, C_L and I_L.

TA2

Figure 4.8 shows the transconductance of TA2. The dominant pole in the transconductance of TA2 is located at approximately 300MHz.

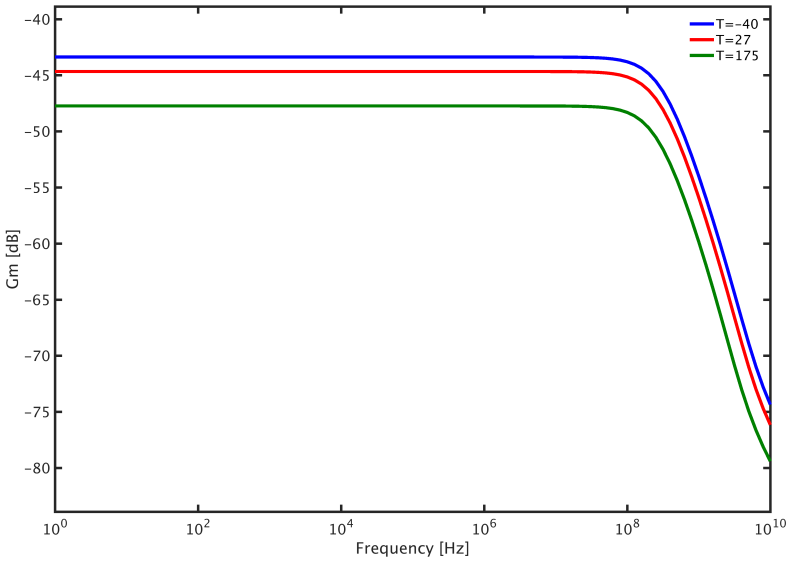

Figure 4.8: Transconductance of TA2.

Figure 4.3 shows the V-I relation of TA2 over the specified input range. It can be seen that the TA is quite non-linear due to the common drain output stage.

Figure 4.10 shows the PSR of TA2 for different load capacitors. The load capacitance is assumed to be connected from the output of the amplifier to ground. The PSR of TA2 only influences the PSR on system level at frequencies lower than $p_{VRL,1}$. For this reason it was chosen not to use a decoupling capacitor at the output of TA2.

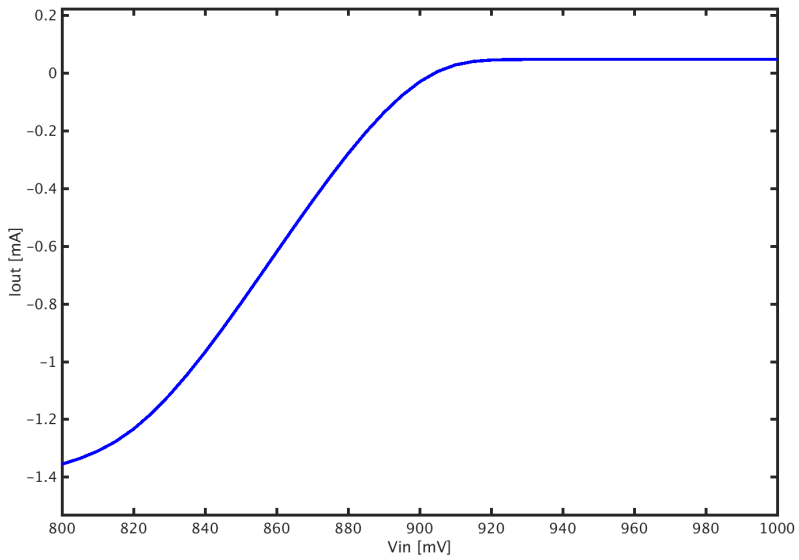

Figure 4.9: V-I curve of TA2.

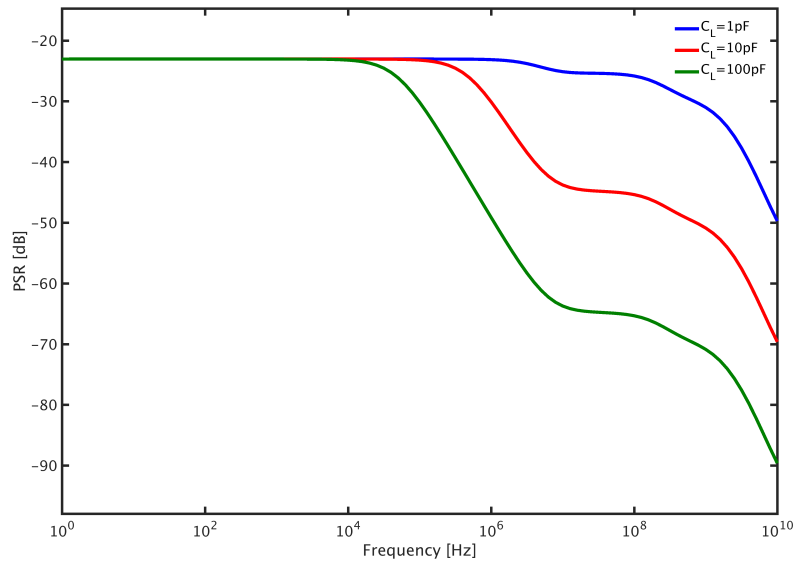

Figure 4.10: PSR of TA2 for different output capacitances.

4.2 Performance parameters

The performance of the dual loop ISR and the KMA3xx is compared by use of the performance parameters that were defined in chapter 2.

4.2.1 Power supply rejection

Figure 4.11 shows the PSR of the Dual Loop ISR and the KMA3xx ISR. The PSR is mainly dependent on temperature and I_L.

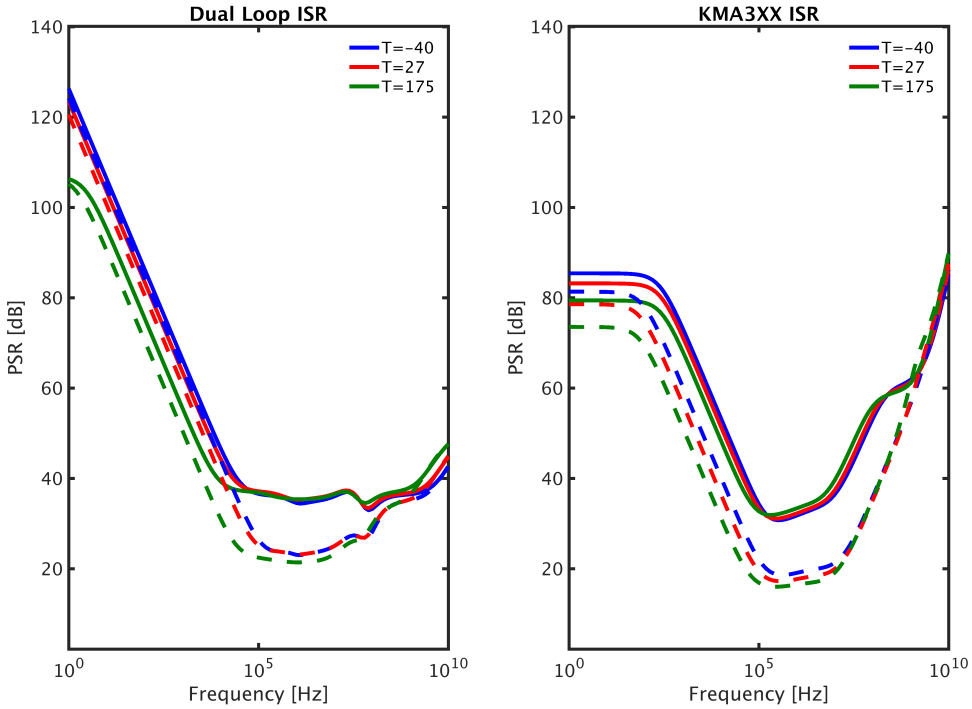

Figure 4.11: PSR comparison for the dual loop ISR and the KMA3xx ISR. The solid lines show the performance when $I_L = 1mA$, while dotted lines show the performance for $I_L = 10mA$.

It can be seen that the minimum value of the dual loop ISR lies about 6dB above the minimum value of the KMA3xx ISR. At high frequencies, the KMA3xx outperforms the dual loop ISR due the use of a HVNMOS instead of a HVPMOS.

4.2.2 Emission

Figure 4.12 shows the emission of the Dual Loop ISR and the KMA3xx ISR. The emission is mainly dependent on temperature and I_L.

For frequencies higher than 1MHz, the emission in the dual loop ISR has dropped -22dB to -30dB. The KMA3xx ISR reaches this amount of suppression at frequencies beyond 500MHz.

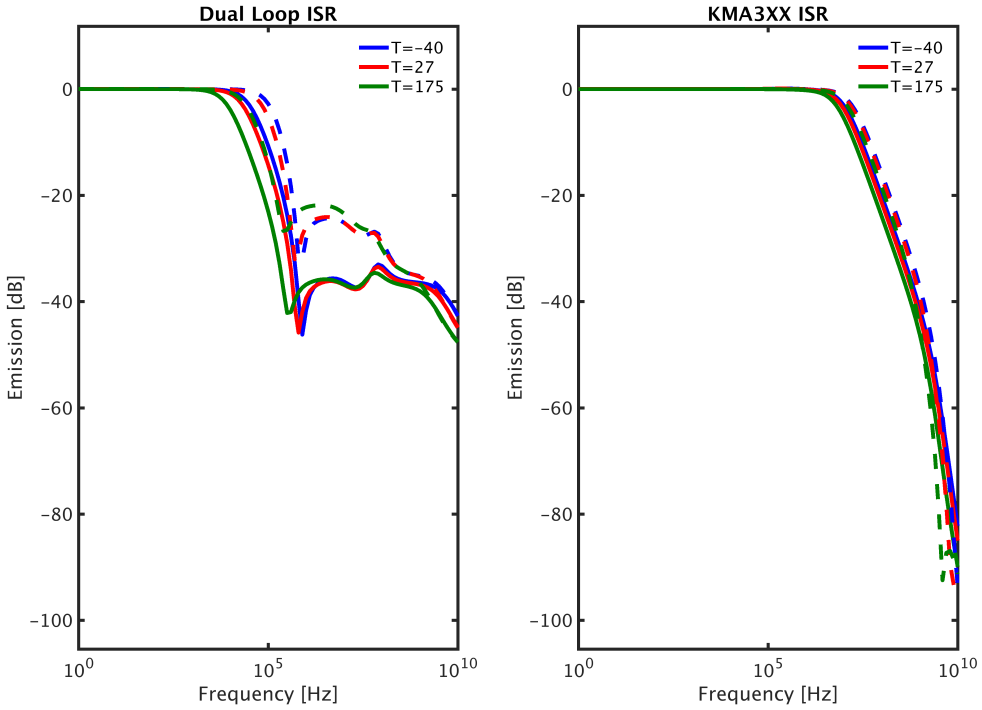

Figure 4.12: Emission comparison between the dual loop ISR and the KMA3xx ISR. The solid lines show the performance when $I_L = 1mA$, while dotted lines show the performance for $I_L = 10mA$.

4.2.3 Line regulation

Figure 4.13 shows the line regulation of the Dual Loop ISR.

As ΔV_{dd} rises from 0 to 40V and back, V_{out} drops about $11\mu V$. The behavior shows hysteresis in the circuit. The source of this hysteresis could not be found. The line regulation can be approximated by:

$$\frac{\Delta V_{OUT}}{\Delta V_{DD}} \approx -137.2dB \tag{4.1}$$

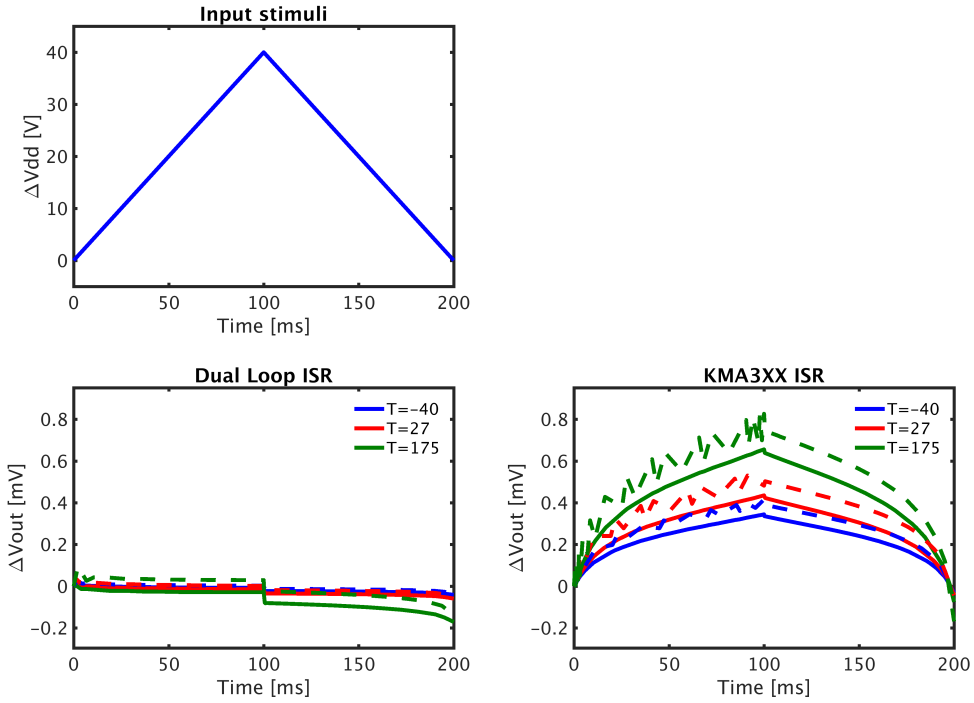

Figure 4.13: Line regulation comparison between the Dual Loop ISR and the KMA3xx ISR. The solid lines show the performance when $I_L = 1mA$, while dotted lines show the performance for $I_L = 10mA$.

4.2.4 Load regulation

Figure 4.14 shows the load regulation of the dual loop ISR.

As I_L rises from 1mA to 11mA and back, V_{out} drops about 11.5mV and returns to its initial value. The behavior is highly linear. The load regulation can be approximated by:

$$\frac{\Delta V_{OUT}}{\Delta I_L} \approx 1.15\Omega \tag{4.2}$$

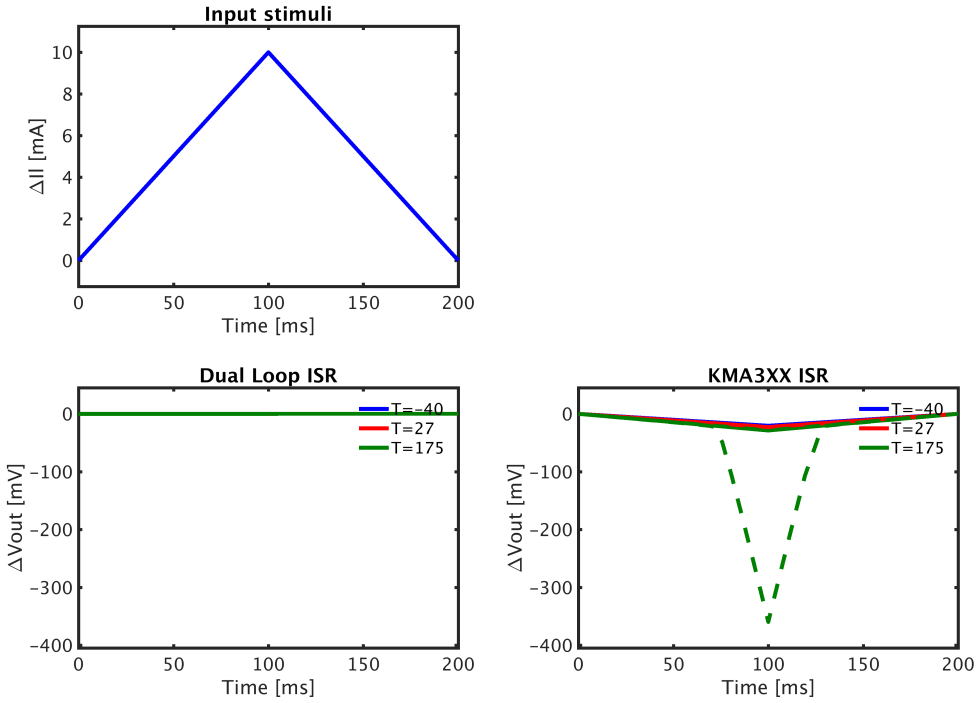

Figure 4.14: Load regulation comparison between the Dual Loop ISR and the KMA3xx ISR. The solid lines show the performance when $I_L = 1mA$, while dotted lines show the performance for $I_L = 10mA$.

4.2.5 Line transient

Figure 4.15 shows the line transient plots of the dual loop ISR and the KMA3xx ISR. The line transient is shown for different values of I_L.

The input voltage step has a magnitude of 100mV and a rise time of 1ns. It can be seen that the dual loop regulator performs better than the KMA3xx during a positive line step but worse during a negative line step. This is due to the non-linearity in the transconductance of M2 (g_{m2}).

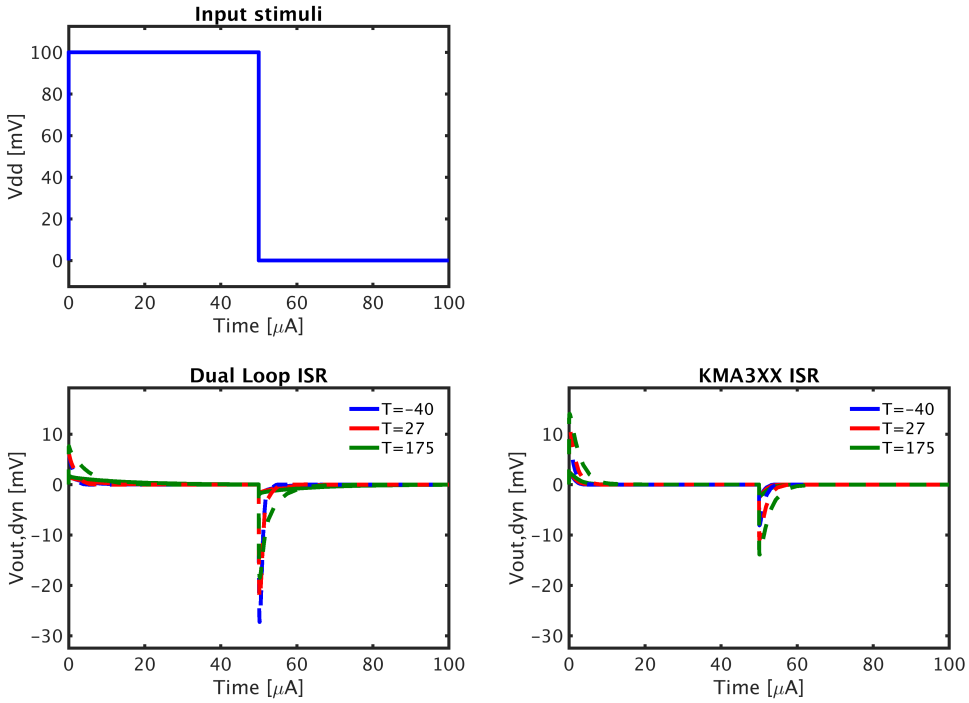

Figure 4.15: Line transient comparison between the Dual Loop ISR and the KMA3xx ISR. The solid lines show the performance when $I_L = 1mA$, while dotted lines show the performance for $I_L = 10mA$.

4.2.6 Load transient

Figure 4.16 shows the load transient of the dual loop ISR and the KMA3xx ISR. The load transient is shown for different values of I_L.

The load current step has a magnitude of 50μA and a rise time of 1ns. Due to the fast VRL of the dual loop ISR, the magnitude of the load step response is smaller than that of the KMA3xx. However, as the gain of the VRL of the KMA3xx ISR is a lot larger, it reaches higher load suppression at the output. The dual loop ISR is slower in reaching a high amount of suppression as this is done by the slow CRL.

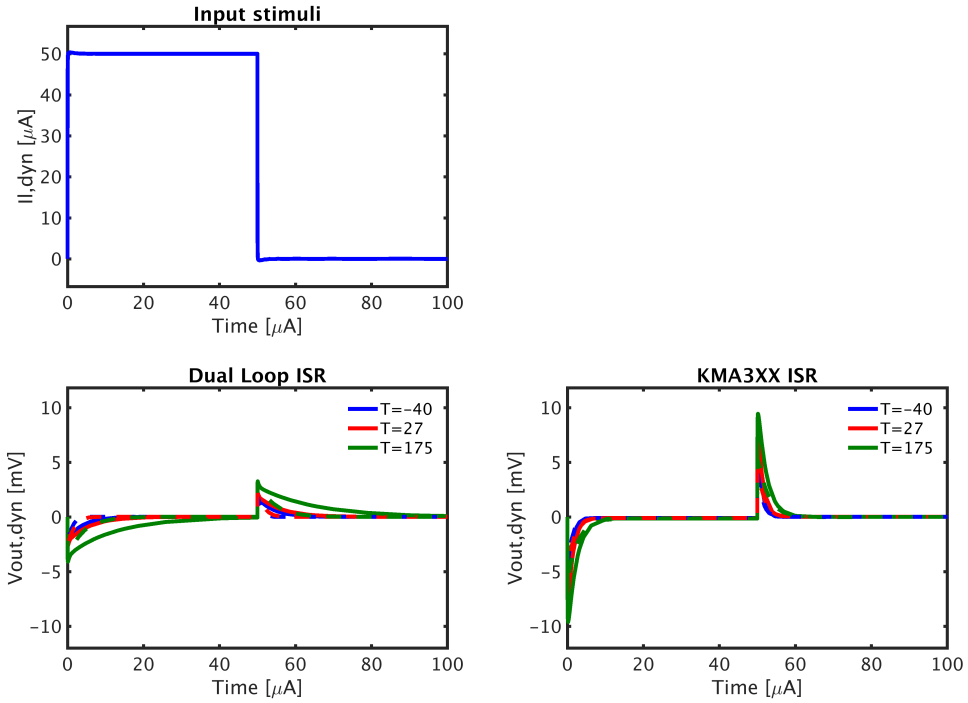

Figure 4.16: Load transient comparison between the Dual Loop ISR and the KMA3xx ISR. The solid lines show the performance when $I_L = 1mA$, while dotted lines show the performance for $I_L = 10mA$.

4.3 Realistic transient load

In order to test the ISR under realistic circumstances, simulations were done using an existing IP block as a load. The digital block that causes most electromagnetic interference in the KMA3xx design was chosen; the hardmacro.

The hardmacro runs at a clock frequency of 25MHz. At the rising clock edge, a large current is drawn from the supply to charge a number of nodes to V_{dd}. Figure 4.17 shows the load transient response of the dual loop ISR and the KMA3xx ISR.

It can be seen that the magnitude of i_{dd} approximately halved with respect to the KMA3xx ISR. The output impendance of the dual loop regulator is also smaller due to the larger bandwidth of the VRL.

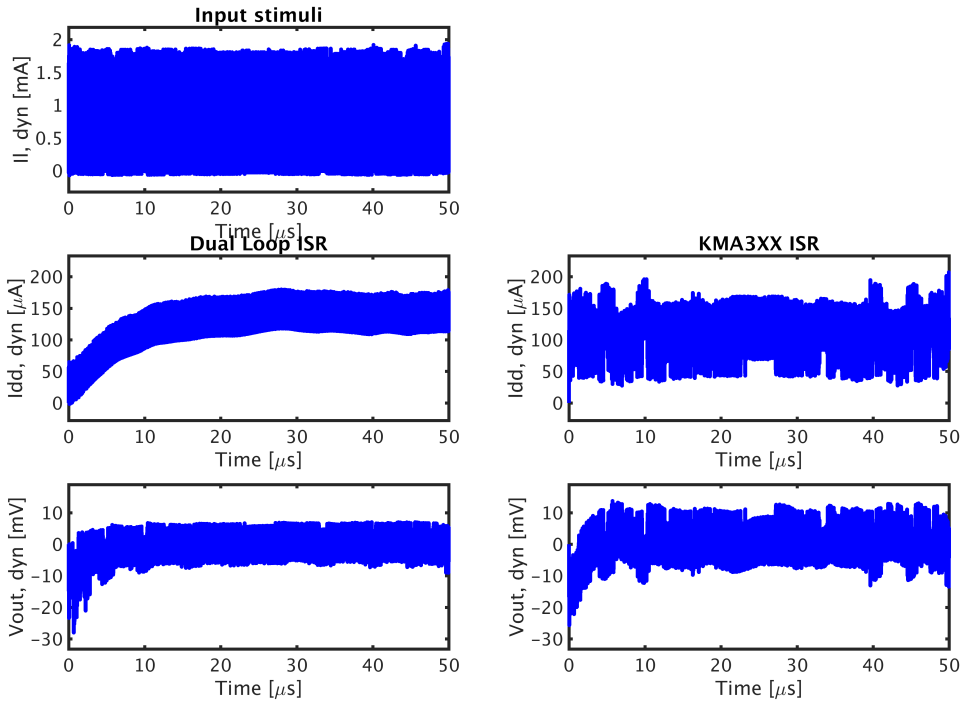

Figure 4.17: Realistic load comparison between the Dual Loop ISR and the KMA3xx ISR.

Chapter 5

Conclusion

The final chapter concludes the outcome of the research that was done. The contribution to science is described and options for further investigation are given.

5.1 Contribution to science

A performance comparison between different regulator output stages, with focus on EMC performance, was done. Based on this comparison, a new ISR architecture was proposed: the dual loop ISR. The proposed ISR has a conventional shunt VRL for EMC performance. A second loop controls the supply current. This loop eliminates the main weakness of a regular shunt regulator; Power efficiency.

The consequences of having a dual loop system were analyzed. With the proposed output stage using two PMOS transistors, the loop interaction is kept to a minimum. Stability is ensured by meeting Nyquist stability criteria for both loops.

Circuit simulations show an improvement in EMC performance and speed over the existing ISR.

5.2 Future activities

The design will be implemented on a NXP test chip along with other designs. Layouts of the individual circuit blocks have been made but the toplevel design will depend on the location of the ISR and the test structure of the test chip.

5.3 Recommendations for further study

As the dual loop ISR has a low minimum drop-out voltage, it is interesting to investigate the option to cascade the ISR with a NMOS series ISR to further increase EMC performance. Such a solution would also allow to implement either the series NMOS ISR or the dual loop ISR in the LV domain which will improve the performance even more.

Appendix A

Matlab scripts

Script to calculate PSR_{OL}

PSROL.m

```
%PSROL.m plots the open-loop PSR derived from the equations (blue) and the
%simulated models (red) for all four regulator topologies.

topology=1; %1=NMOS Series, 2=PMOS Series, 3=NMOS Shunt, 4=PMOS Shunt

for topology=1:4

if topology==1

M=csvread('~/Images/PSR_OL_NMOS_Series2.csv',1,0);
freq=M(:,1);
value=M(:,2);
plottitle='NMOS series';

%Set the small signal values found from DC simulation
gm1=34.9e-3;
go1=3.4e-6;
Gcs=1e-6;
Gtau=1e-6;
Gtad=1e-6;
Cdec1=10e-12;
Cout=100e-12;
Cdb1=190.8e-15;
Cgd1=569e-15;
Cgs1=3.6e-12;

s=tf('s');

N1=Cout*(Cdec1+Cgd1+Cgs1)-Cgs1*Cgs1;
N2=(Gtau+Gtad)*Cout+gm1*(Cdec1+Cgd1+Cgs1)-gm1*Cgs1;
```

```
N3=gm1*(Gtau+Gtad);
D1=Cgd1*Cgs1+Cdb1*(Cdec1+Cgd1+Cgs1);
D2=gm1*Cgd1+Gtau*Cgs1+(Gtad+Gtau)*Cdb1+go1*(Cdec1+Cgd1+Cgs1);
D3=gm1*Gtau+go1*(Gtau+Gtad);

H=(N1*s^2+N2*s+N3)/(D1*s^2+D2*s+D3);
[mag,phase,wout]=bode(H,1,1e12);
mag=squeeze(mag);
wout=squeeze(wout);
fout=wout/(2*pi);

elseif topology==2

M=csvread('~/Images/PSR_OL_PMOS_Series2.csv',1,0);
freq=M(:,1);
value=M(:,2);
plottitle='PMOS series';

%Set the small signal values found from DC simulation
gm1=28.5e-3;
go1=3.6e-6;
Gcs=1e-6;
Gtau=1e-6;
Gtad=1e-6;
Cdec1=18.5e-12;
Cout=100e-12;
Cdb1=384e-15;
Cgd1=1.1e-12;
Cgs1=0;

s=tf('s');
N1=Cdec1*Cgd1+Cout*(Cdec1+Cgd1);
N2=(Gtau+Gtad)*Cout+gm1*Cgd1+(go1+Gcs)*(Cdec1+Cgd1);
N3=(go1+Gcs)*(Gtau+Gtad);
D1=Cgd1*Cdec1+Cdb1*(Cdec1+Cgd1);
D2=gm1*Cgd1+Gtau*Cgd1+(Gtau+Gtad)*Cdb1;
D3=gm1*Gtad;

H=(N1*s^2+N2*s+N3)/(D1*s^2+D2*s+D3);
[mag,phase,wout]=bode(H,1,1e12);
mag=squeeze(mag);
wout=squeeze(wout);
fout=wout/(2*pi);

elseif topology==3

M=csvread('~/Images/PSR_OL_NMOS_Shunt2.csv',1,0);
freq=M(:,1);
```

```
value=M(:,2);
plottitle='NMOS shunt';

%Set the small signal values found from DC simulation
gm1=28.5e-3;
gm2=32.7e-3;
gm3=91.3e-6;
go1=6.9e-6;
go2=1.4e-3;
Gtau=1e-6;
Gtad=1e-6;
Cdec1=18.6e-12;
Cdec2=1e-12;
Cout=100e-12;
Cdb1=384e-15;
Cgd1=1.4e-12;
Cgs2=0;

s=tf('s');
Ydda=s*Cgd1*(gm3+s*Cdec1)/(gm3+s*(Cgd1+Cdec1))
Yddb=(s*Cgd1*gm1)/(gm3+s*(Cgd1+Cdec1))+go1+s*Cdb1
Yqa=((Gtau+s*Cdec2)*(Gtad+s*Cgs2))/(Gtau+Gtad+s*(Cdec2+Cgs2))
Yqb=(gm2*(Gtau+s*Cdec2))/(Gtau+Gtad+s*(Cdec2+Cgs2))+go2+s*Cout

H=(Ydda+Yddb+Yqa+Yqb)/(Ydda+Yddb);
[mag,phase,wout]=bode(H,1,1e12);
mag=squeeze(mag);
wout=squeeze(wout);
fout=wout/(2*pi);

elseif topology==4

M=csvread('~/Images/PSR_OL_PMOS_Shunt2.csv',1,0);
freq=M(:,1);
value=M(:,2);
plottitle='PMOS shunt';

%Set the small signal values found from DC simulation
gm1=38.4e-3;
gm2=31.4e-3;
gm3=91.3e-6;
go1=6.9e-6;
go2=1.2e-3;
Gtau=1e-6;
Gtad=1e-6;
Cdec1=18.6e-12;
Cdec2=1e-12;
Cout=100e-12;
```

```
Cdb1=384e-15;
Cgd1=1.2e-12;
Cgs2=0e-15;

s=tf('s');
Ydda=s*Cgd1*(gm3+s*Cdec1)/(gm3+s*(Cgd1+Cdec1));
Yddb=(s*Cgd1*gm1)/(gm3+s*(Cgd1+Cdec1))+go1+s*Cdb1;
Yqa=((Gtau+s*Cgs2)*(Gtad+s*Cdec2))/(Gtau+Gtad+s*(Cdec2+Cgs2));
Yqb=(gm2*(Gtad+s*Cdec2))/(Gtau+Gtad+s*(Cdec2+Cgs2))+go2+s*Cout;

H=(Ydda+Yddb+Yqa+Yqb)/(Ydda+Yddb);
[mag,phase,wout]=bode(H,1,1e12);
mag=squeeze(mag);
wout=squeeze(wout);
fout=wout/(2*pi);

end

%Make subplot
subplot(2,2,topology)
semilogx(freq,value,'LineWidth',4,'color','red')
axis([1 1e10 -80 80])
ax=gca;
ax.LineWidth = 3;
ax.FontSize = 18;
ax.XMinorTick = 'off';
title(plottitle)
xlabel('Frequency [Hz]')
ylabel('PSR_OL [dB]')
hold on
loglog(fout,20*log10(mag),'LineWidth',4,'color','blue')

end
```

Script to calculate EM_{OL}

EMOL.m

```
%EMOL.m plots the open-loop Emission derived from the equations (blue) and the
%simulated models (red) for all four regulator topologies.

topology=1; %1=NMOS Series, 2=PMOS Series, 3=NMOS Shunt, 4=PMOS Shunt

plottitle='NMOS series','PMOS series','NMOS shunt','PMOS shunt';

%Load csv files from simulation
M1=csvread('~/Images/EM_OL_NMOS_Series2.csv',1,0);
M2=csvread('~/Images/EM_OL_PMOS_Series2.csv',1,0);
M3=csvread('~/Images/EM_OL_NMOS_Shunt2.csv',1,0);
M4=csvread('~/Images/EM_OL_PMOS_Shunt2.csv',1,0);
M=M1,M2,M3,M4;

for topology=1:4

if topology==1

%Set the small signal values found from DC simulation
gm1=34.9e-3;
go1=3.4e-6;
Gcs=1e-6;
Gtau=1e-6;
Gtad=1e-6;
Cdec1=10e-12;
Cout=100e-12;
Cdb1=190.8e-15;
Cgd1=569e-15;
Cgs1=3.6e-12;

s=tf('s');

Ydda=s*Cgs1*(Gtau+s*Cgd1)/(Gtau+Gtad+s*(Cgd1+Cdec1+Cgs1));
Yddb=gm1*(Gtau+Gtad+s*(Cgd1+Cdec1))/(Gtau+Gtad+s*(Cdec1+Cgd1+Cgs1))+go1+s*Cdb1;
Yqa=(s*Cgs1*(Gtad+s*Cdec1))/(Gtau+Gtad+s*(Cdec1+Cgd1+Cgs1));
Yqb=Gcs+s*Cout;

H=(Ydda+Yddb)/(Ydda+Yddb+Yqa+Yqb);
[mag,phase,wout]=bode(H,1,1e12);
mag=squeeze(mag);
wout=squeeze(wout);
fout=wout/(2*pi);

elseif topology==2
```

```
gm1=28.5e-3;
go1=3.6e-6;
Gcs=1e-6;
Gtau=1e-6;
Gtad=1e-6;
Cdec1=18.5e-12;
Cout=100e-12;
Cdb1=384e-15;
Cgd1=1.1e-12;
Cgs1=0;

s=tf('s');

%Set the small signal values found from DC simulation
Ydda=(s*Cgd1*(Gtau+s*Cdec1))/(Gtau+Gtad+s*(Cdec1+Cgd1));
Yddb=gm1*(s*Cgd1)/(Gtau+Gtad+s*(Cdec1+Cgd1))+go1+s*Cdb1;
Yqa=(s*Cgd1*Gtad)/(Gtau+Gtad+s*(Cdec1+Cgd1));
Yqb=Gcs+s*Cout;

H=(Ydda+Yddb)/(Ydda+Yddb+Yqa+Yqb);
[mag,phase,wout]=bode(H,1,1e12);
mag=squeeze(mag);
wout=squeeze(wout);
fout=wout/(2*pi);

elseif topology==3

%Set the small signal values found from DC simulation
gm1=28.5e-3;
gm2=32.7e-3;
gm3=91.3e-6;
go1=6.9e-6;
go2=1.4e-3;
Gtau=1e-6;
Gtad=1e-6;
Cdec1=18.6e-12;
Cdec2=1e-12;
Cout=100e-12;
Cdb1=384e-15;
Cgd1=1.4e-12;
Cgs2=0;

s=tf('s');
Ydda=s*Cgd1*(gm3+s*Cdec1)/(gm3+s*(Cgd1+Cdec1))
Yddb=(s*Cgd1*gm1)/(gm3+s*(Cgd1+Cdec1))+go1+s*Cdb1
Yqa=((Gtau+s*Cdec2)*(Gtad+s*Cgs2))/(Gtau+Gtad+s*(Cdec2+Cgs2))
Yqb=(gm2*(Gtau+s*Cdec2))/(Gtau+Gtad+s*(Cdec2+Cgs2))+go2+s*Cout
```

```
H=(Ydda+Yddb)/(Ydda+Yddb+Yqa+Yqb);
[mag,phase,wout]=bode(H,1,1e12);
mag=squeeze(mag);
wout=squeeze(wout);
fout=wout/(2*pi);

elseif topology==4

%Set the small signal values found from DC simulation
gm1=38.4e-3;
gm2=31.4e-3;
gm3=91.3e-6;
go1=6.9e-6;
go2=1.2e-3;
Gtau=1e-6;
Gtad=1e-6;
Cdec1=18.6e-12;
Cdec2=1e-12;
Cout=100e-12;
Cdb1=384e-15;
Cgd1=1.2e-12;
Cgs2=0e-15;

s=tf('s');
Ydda=s*Cgd1*(gm3+s*Cdec1)/(gm3+s*(Cgd1+Cdec1));
Yddb=(s*Cgd1*gm1)/(gm3+s*(Cgd1+Cdec1))+go1+s*Cdb1;
Yqa=((Gtau+s*Cgs2)*(Gtad+s*Cdec2))/(Gtau+Gtad+s*(Cdec2+Cgs2));
Yqb=(gm2*(Gtad+s*Cdec2))/(Gtau+Gtad+s*(Cdec2+Cgs2))+go2+s*Cout;

H=(Ydda+Yddb)/(Ydda+Yddb+Yqa+Yqb);
[mag,phase,wout]=bode(H,1,1e12);
mag=squeeze(mag);
wout=squeeze(wout);
fout=wout/(2*pi);
end

freq=Mtopology(:,1);
value=Mtopology(:,2);

%Set the current subplot window
subplot(2,2,topology)

%Plot simulated curve for current topology
semilogx(freq,value,'LineWidth',4,'color','red')

%Set plot properties
axis([1 1e10 -80 5])
```

```
ax=gca;
ax.LineWidth = 3;
ax.FontSize = 18;
ax.XMinorTick = 'off';
title(plottitletopology)
xlabel('Frequency [Hz]')
ylabel('Emission_OL [dB]')
hold on

%Plot equation curve for current topology in the same subplot window
loglog(fout,20*log10(mag),'LineWidth',4,'color','blue')
end
```

Appendix B

Transistor models

NMOS series model

PMOS series model

NMOS shunt model

PMOS shunt model

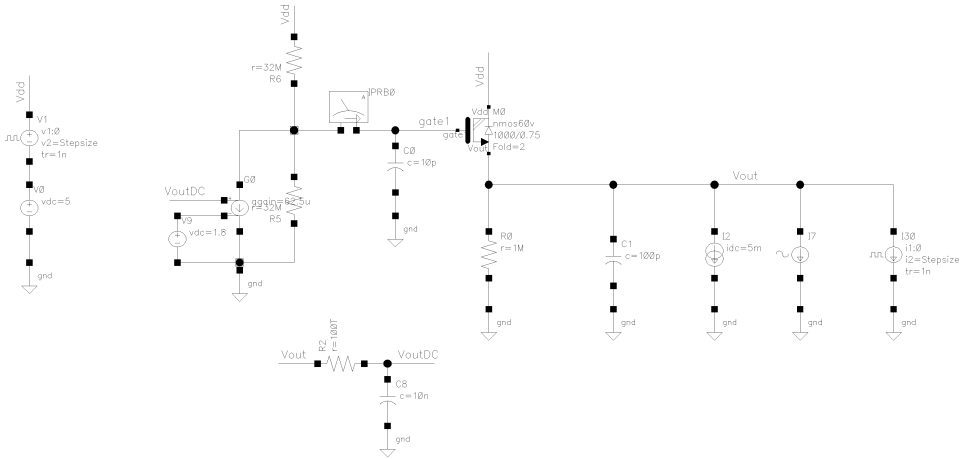

Figure B.1: Open loop model of the NMOS series topology.

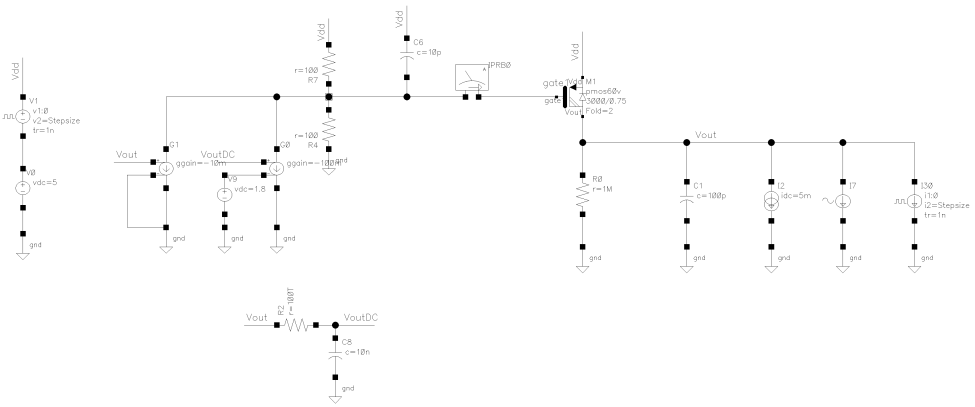

Figure B.2: Open loop model of the PMOS series topology.

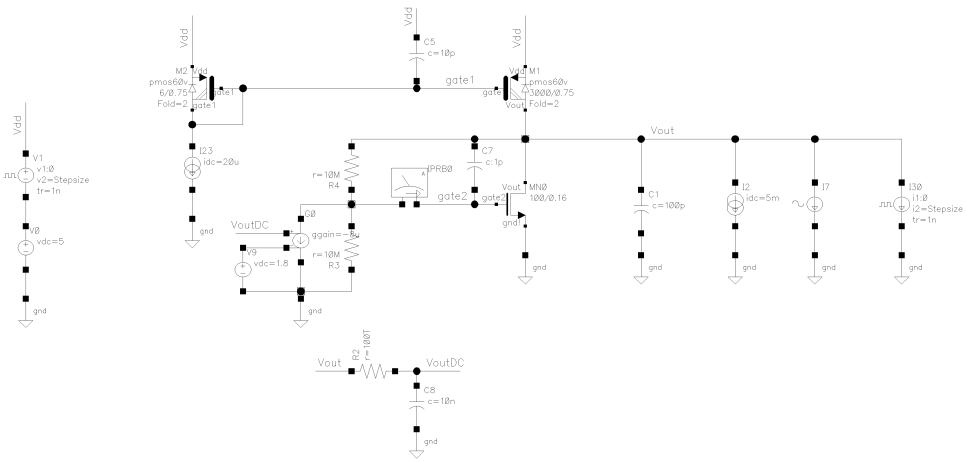

Figure B.3: Open loop model of the NMOS shunt topology.

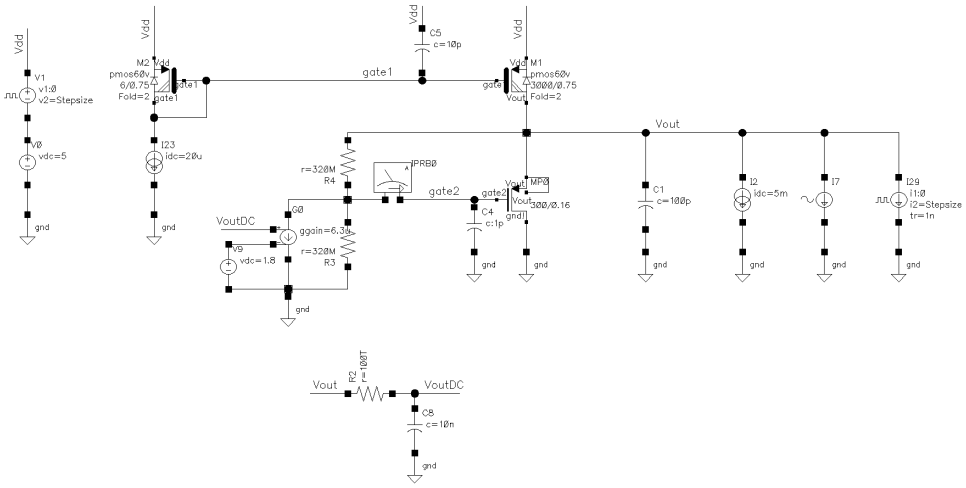

Figure B.4: Open loop model of the PMOS shunt topology.

Appendix C

Dual loop project files

Toplevel schematic

TA1 schematic

TA2 schematic

β_v schematic

ISR testbench

Toplevel layout

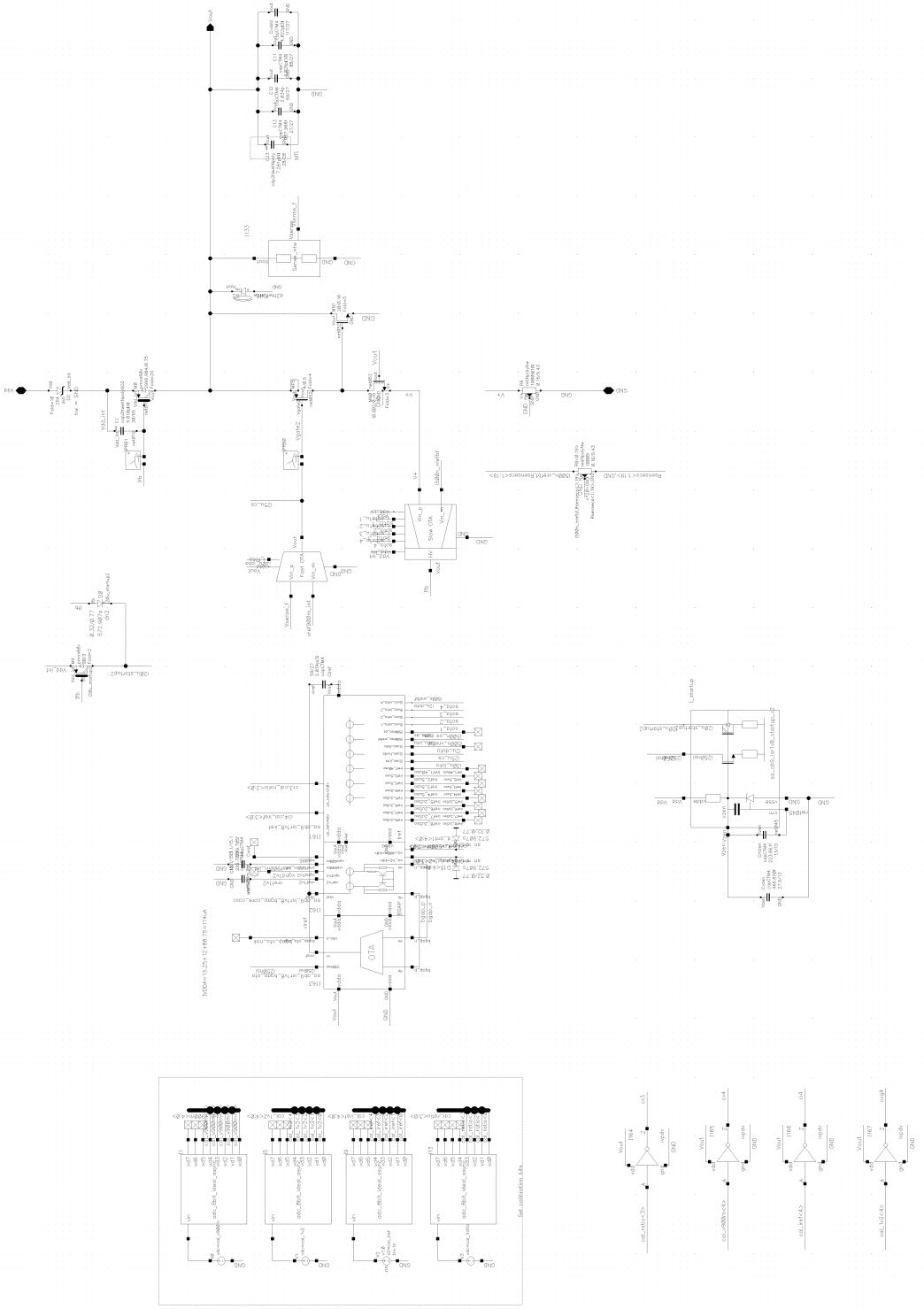

Figure C.1: Toplevel schematic of the Dual loop ISR.

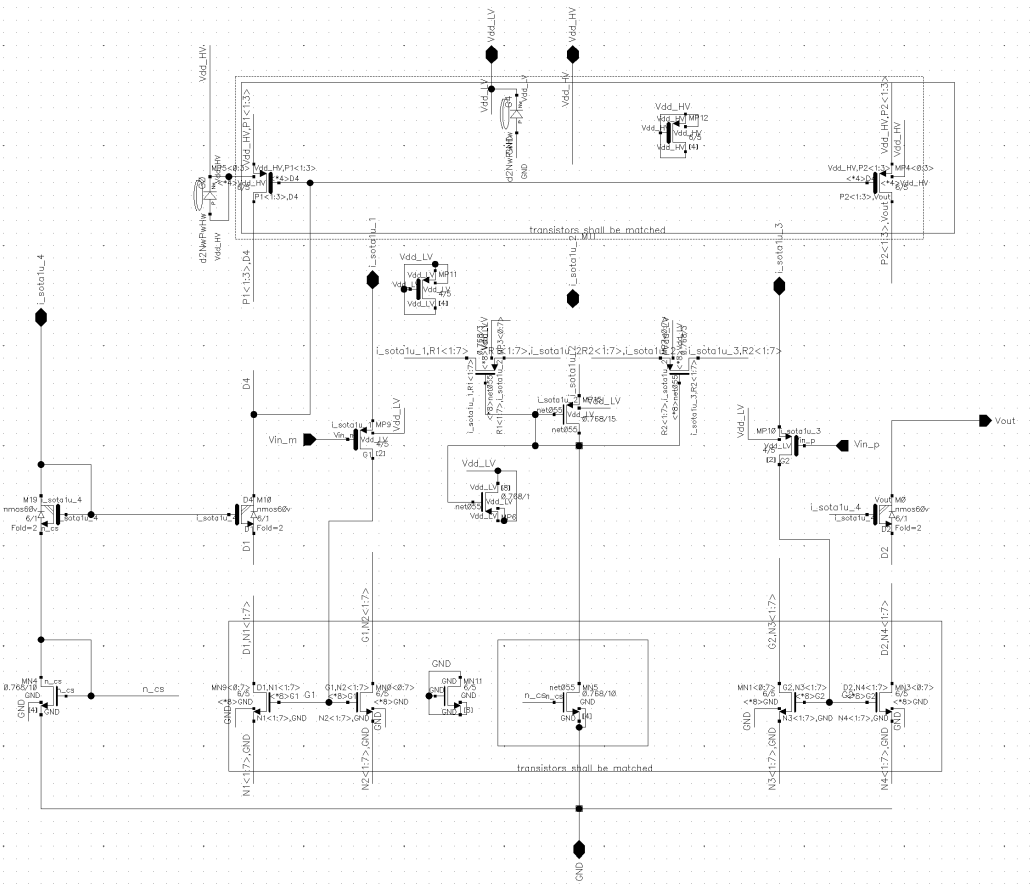

Figure C.2: Schematic of the TA1 circuit block.

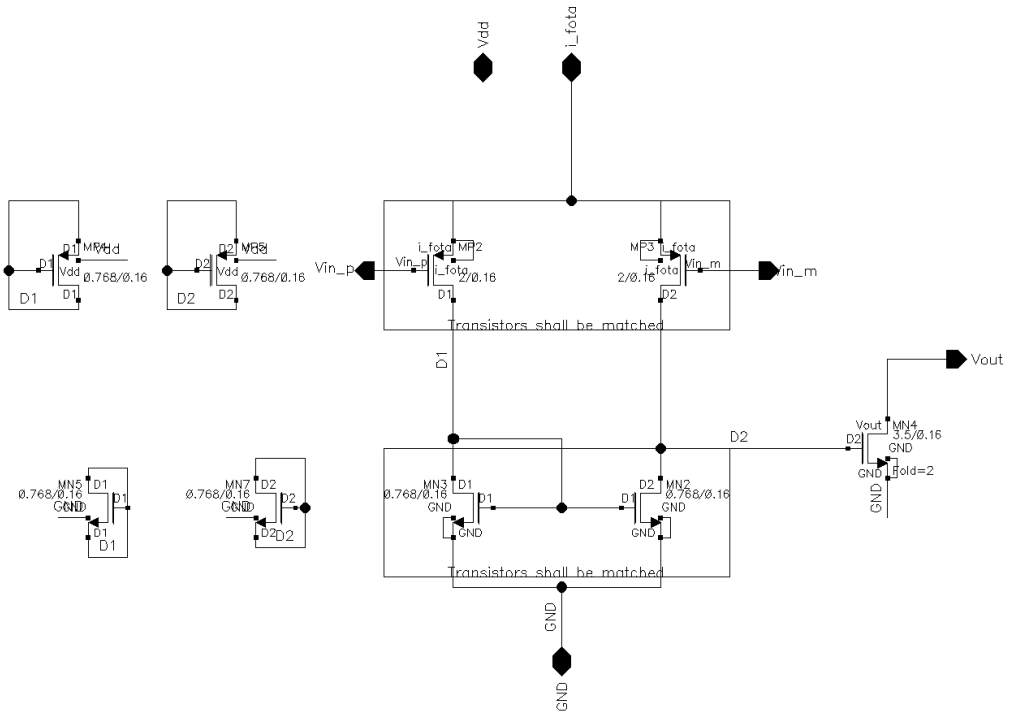

Figure C.3: Schematic of the TA2 circuit block.

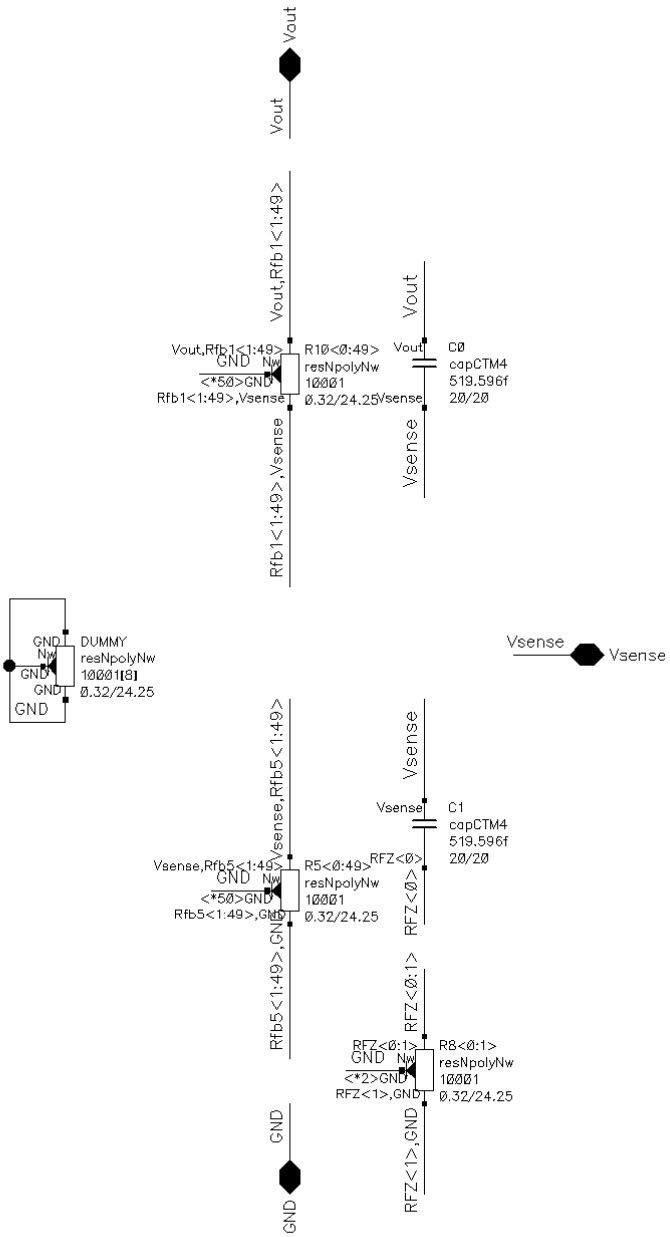

Figure C.4: Schematic of the β_v circuit block.

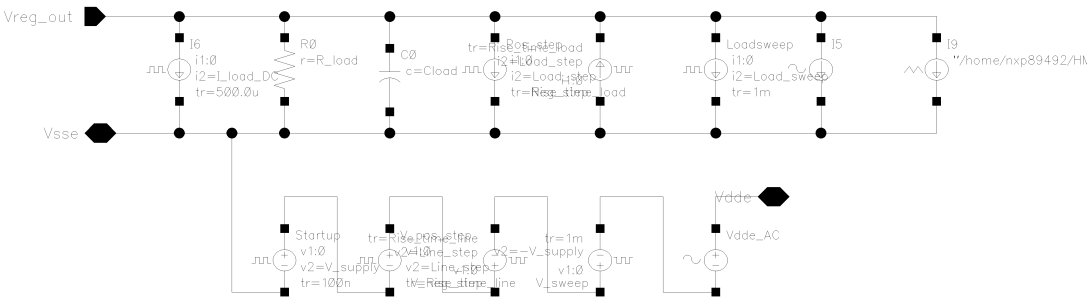

Figure C.5: ISR testbench.

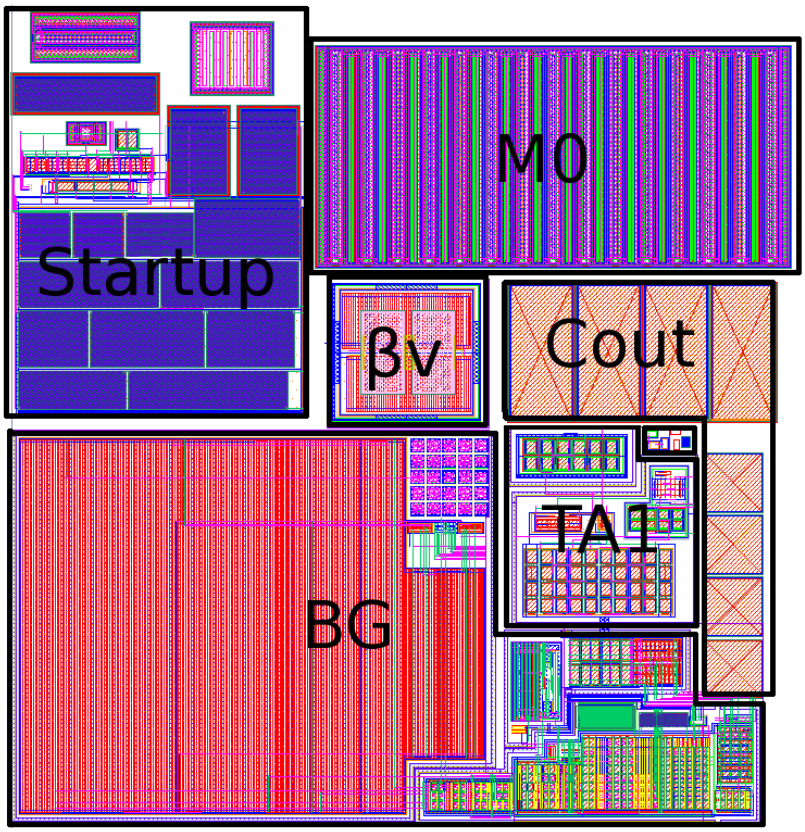

Figure C.6: Toplevel layout of the Dual loop ISR.

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