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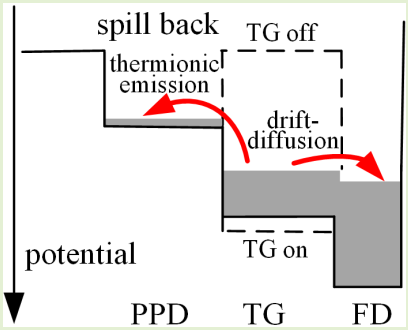
Analysis and Modeling of Spill Back Effect in High Illumination CMOS Image Sensors

Jiangtao Xu, *Member, IEEE*, Ruishuo Wang, Liqiang Han, and Zhiyuan Gao, *Member, IEEE*

***Abstract*—To improve charge transfer efficiency (*CTE*) and eliminate image lag, the impact of spill back effect on image lag is studied in CMOS image sensors (CISs), particularly in high illumination condition. By establishing a mathematical model based on the thermionic emission and drift-diffusion theory, the physical mechanism of spill back effect is described. This model shows that a lower transfer gate (TG) operating voltage and a higher reset voltage of Floating Diffusion (FD) node would mitigate spill back effect. In a 0.18μm CMOS process, by setting that the gate voltage of transfer transistor and the reset voltage of FD is 2.8 V and 3.8 V respectively, *CTE* of the proposed pixel is increased to 100%. The theoretical analysis and TCAD simulation results can explain spill back effect and offer a reference for designing a high *CTE* pixel in high illumination CISs.**



***Index Terms*—CMOS image sensors (CISs), charge transfer, image lag, spill back.**

I. Introduction

THE CMOS image sensors (CISs) based on Pinned Photodiode (PPD) are widely developed especially in consumer electronics, medical, security and industrial applications. Because they have various advantages, including low power consumption, low cost and high level of integration [1]–[3]. Meanwhile, the charge transfer performance is an important property for CISs. It must be noted that the photo-generated electrons in PPD should be transferred into FD completely. After TG is OFF, the charges left in PPD will deteriorate the linearity and the latter frame image quality due to image lag [4].

The main reason for image lag is the presence of potential pocket or barrier under TG. By an additional implantation, the Lateral Drift-Field Photodetector is formed, which would introduce an electrostatic potential gradient in the photoactive area during charge transfer process. Thus, a high charge transfer speed and low image lag CIS structure is proposed in [5]. In [6], a non-uniform doped transfer transistor channel is present for an optimized electrical potential distribution along the transfer path from the PPD to the FD. To deal with the image lag problem in a large photodiode pixel, "W" shaped PPD is proposed in [7]. A lag-free (CIS) with Constant Residue Reset (CRR) operation is presented in [8]. It totally eliminates image lag effect irrelevant to the channel doping profile variation of transfer transistor.

The spill back effect is another source of image lag. Especially, for high illumination applications, it becomes more possible to hold charges under TG before TG is turned OFF, which could result in signal charges spill back to PPD on the process of TG closure. Modelling the relationship between spill back effect and pixel design parameters is important for high *CTE* CISs. Considering the research related to spill back effect, the TG channel doping profile and pixel layout geometrical parameters strongly affect image lag. Introducing a step under the TG in the potential diagram can achieve a high *CTE* [9]. Other studies have been investigated about charge transfer process. But it's unexplored that the operating voltage of TG and the reset voltage of FD have an impact on spill back effect, eventually leading to image lag.

In order to better learn how to improve *CTE* and minimize spill back effect, the influence of operation condition on the spill back is further studied in this paper. Operating voltage of TG and the reset voltage of FD adjust the signal values, at which spill back occurs. Thanks to theoretical analysis and TCAD simulation, on the condition of no potential pocket or barrier along the charge transfer path, the influence

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J. Xu and R. Wang are with the School of Microelectronics, Tianjin University, Tianjin 300072, China, and also with the Tianjin Key Laboratory of Imaging and Sensing Microelectronic Technology, Tianjin University, Tianjin 300072, China (e-mail: xujiangtao@tju.edu.cn; wruishuo@tju.edu.cn).

L. Han is with the Electronic Instrumentation Laboratory, Delft University of Technology, 2628CD Delft, The Netherlands (e-mail: l.han-1@tudelft.nl).

Z. Gao is with the School of Computer, Guangdong University of Technology, Guangdong 510006, China (e-mail: flyuphigher@outlook.com).

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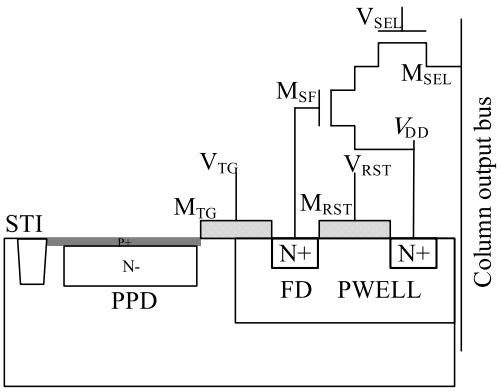

Fig. 1. Typical pixel structure of the 4T PPD CIS.

of different operating voltages of TG and the reset voltage of FD on image lag linked to spill back effect are shown in this paper.

The pixel structure and operating principle are described in Section II. A mathematical model of the spill back effect is presented in Section III. The TCAD simulation results about pixel design influence on the spill back effect and image lag are shown in Section IV. A conclusion is given in Section V.

II. 4T-Pixel Operating Principle and Spill Back Effect

A typical 4T PPD CIS pixel is shown in Fig.1 [10]. The incident photons are converted into electrons in PPD region. Before transferring electrons, the reset transistor M_{RS} is turned on to reset the FD node. The reset voltage value is read out by turning on the select transistor M_{SEL} for CDS. When TG is on, all the photo-generated electrons will, ideally, be transferred into FD node. Again by turning on the M_{SEL}, reading out the signal voltage value is needed.

Spill back effect occurs when signal charges are present under TG before TG being turned "OFF". When TG is switched from "ON" to "OFF", some charges under TG would flow into FD, others would spill back to PPD, which leads to image lag. The charge transfer performance is often represented by *CTE*

$$CTE = \frac{N_{transfer}}{N_{all}} \times 100\% \tag{1}$$

In (1), N_{transfer} and N_{all} are the number of charges transferred from PPD to FD and photo-generated charges in PPD respectively.

III. Mathematical Model and Analysis

A. The Principle of Charge Conservation

In order to further understand the spill back effect, the principle of charge conservation is used to discuss the influence of spill back on charge transfer process.

Fig.2 shows the equivalent circuit of the MOS structure, in which C_{ox} and C_{s} is the capacitance of oxide and space charge region, respectively. Moreover, V_{TG} is the TG voltage and V_{s} is the surface potential, and d_0 is the thickness of the oxide.

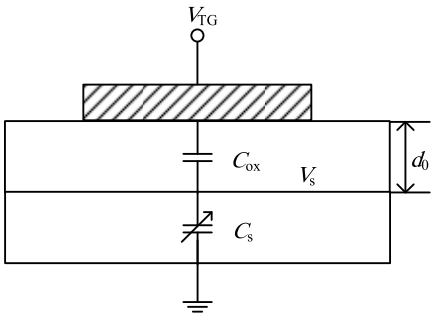

Fig. 2. The equivalent circuit model of the MOS structure [11].

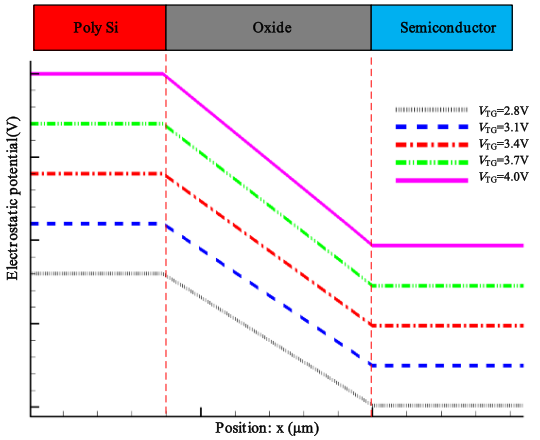

Fig. 3. The simulation result of MOS electrostatic potential.

According to $Q = CV$, the variation of charges ΔQ_1 on the poly Si surface is obtained for different TG voltage as follows:

$$\Delta Q_1 = C_{ox}\left[(V_{TG2} - V_{s2}) - (V_{TG1} - V_{s1})\right] \tag{2}$$

For the upper plate of the capacitor C_{s}, the variation of charges Q_2 is obtained:

$$\Delta Q_2 = \int_{V_{s1}}^{V_{s2}} C_s(V_s)dV_s \tag{3}$$

It has always been in strong inversion state under TG on the process of changing from V_{s1} to V_{s2}, so C_{s} is simplified as a constant and the following equation is obtained.

$$\Delta Q_2 = \int_{V_{s1}}^{V_{s2}} C_s dV_s = C_s\left(V_{s2} - V_{s1}\right) \tag{4}$$

Notice that (4) is not valid if the TG voltage is too low to make it in inversion state.

Due to the law of charge conversation, the amount of charges Q_{s} on the Si surface is fixed for different TG voltages:

$$\Delta Q_s = -\Delta Q_1 + \Delta Q_2 = 0 \tag{5}$$

Substituting (2) and (4) into (5) to get the following equation:

$$V_{s2} - V_{s1} = \frac{C_{ox}}{C_{ox} + C_s}\left(V_{TG2} - V_{TG1}\right) = \alpha\left(V_{TG2} - V_{TG1}\right) \tag{6}$$

where the coefficient α is the ratio of TG voltage to the surface potential in strong inversion region, and its value is:

$$\alpha = \frac{C_{ox}}{C_{ox} + C_s} \tag{7}$$

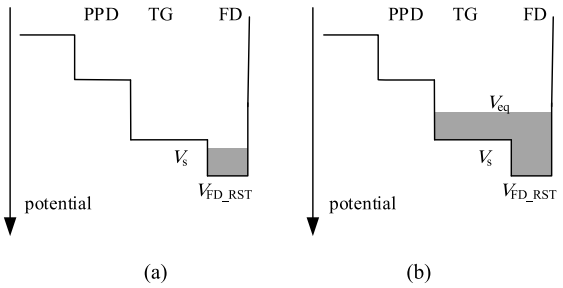

Fig. 4. Potential diagram of the charge transfer path before TG is switched OFF in low illumination (a) and in high illumination (b).

Fig.3 shows the electrostatic potential simulation result of MOS structure on transfer transistor. The simplified relationship $V_s = \alpha V_{TG}$ is valid.

Fig.4 shows the potential diagram of charge transfer path when TG is ON. It's assumed that V_{FD_RST} is the reset voltage of FD node. In high illumination, the electrons in FD region would overflow into TG channel. In Fig.4 (a) and (b), the channel region under TG gradually transforms from the depletion state in the low illumination condition to the inversion state in the high illumination condition. In Fig.4 (b), V_{eq} is the electrostatic potential of TG channel and FD after N_{all} signal charges are transferred from PPD.

According to the law of charge conversation, the following equation is obtained:

$$C_{ox}(V_s - V_{eq}) + C_{FD}(V_{FD\_RST} - V_{eq}) = qN_{all} \quad (8)$$

$$qN_{e0} = C_{ox}(V_s - V_{eq}) \quad (9)$$

where N_{e0} is the initial amount of channel charges after N_{all} signal charges are transferred from PPD, C_{FD} is the capacitance of FD respectively. Due to high doping concentration of FD region, the variation of C_{FD} with the number of electrons or voltage is very small. Therefore, in this model, C_{FD} is regarded as a constant independent of the number of electrons or voltage of FD.

From (8) and (9), the amount of initial charges N_{e0} in channel is written as:

$$N_{e0} = \frac{C_{ox}}{q(C_{ox} + C_{FD})}\left(qN_{all} - C_{FD}(V_{FD\_RST} - V_s)\right) \quad (10)$$

Substituting (10) with (8)

$$N_{e0} = \frac{C_{ox}}{q(C_{ox} + C_{FD})}\left(qN_{all} - C_{FD}\left(V_{FD\_RST} - \alpha V_{TG}\right)\right) \quad (11)$$

B. The Theory of Thermionic Emission and Drift-diffusion

To explain the influence mechanism of spill back effect, the thermionic emission [12] and drift-diffusion theory are adopted to obtain a mathematical model.

Fig.5 shows the energy band diagram from PPD to FD node when TG is switched from ON to OFF state, where E_C, E_f and E_V is the energy levels of the conduction band, Fermi level, and valence band, respectively. The voltage of TG begins to drop when $t = 0$. Then, we assume that the charges stored

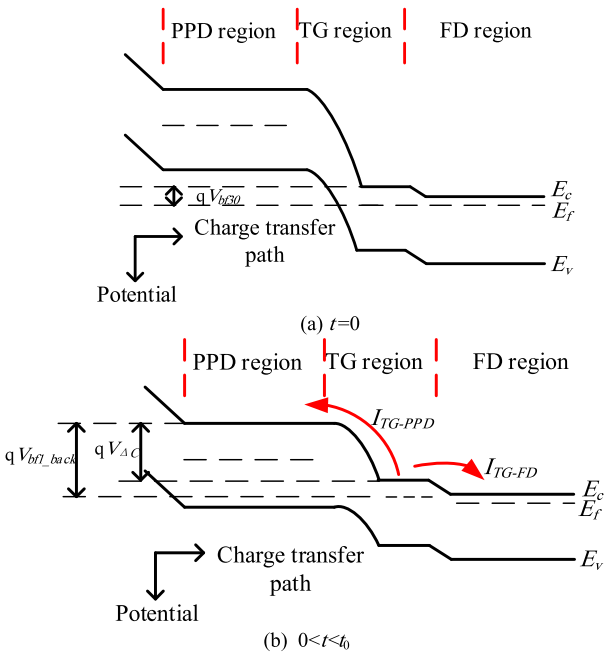

Fig. 5. Energy band diagram when TG is from ON to OFF.

in channel completely spill back to PPD or flow into FD when $t = t_0$.

In a very fast TG voltage drop process, the spill back process can be simplified. With a high potential barrier, the thermionic emission current from TG channel to PPD nearly equals to zero when TG is ON. Thus, a completely empty PPD in the initial condition, leads to that the current from PPD to TG is neglected during TG is switched from ON to OFF. According to the thermionic emission theory, the emission current from TG channel to PPD is:

$$I_{TG-PPD} = \frac{\mathrm{d}Q}{\mathrm{d}t} = I_{0PPD}\exp\left(\frac{-\mathrm{q}V_{bf1\_back}}{\mathrm{k}T}\right) \quad (12)$$

$$I_{0PPD} = \mathrm{A} \cdot S_{APPD} \cdot T^2 \quad (13)$$

where V_{bf1_back} is the potential barrier height from TG channel region to PPD region, A is the Richardson constant [10], S_{APPD} is the area of the cross section on the charge transfer path at the connection of TG and PPD, T is the absolute temperature.

In the condition of thermal equilibrium, the electron concentration n_e in the channel is obtained as follows:

$$\frac{N_e}{V_{ch}} = n_e = \mathrm{N_C}\exp\left(-\frac{E_c - E_f}{kT}\right) = \mathrm{N_C}\exp\left(\frac{\mathrm{q}V_{\Delta C} - \mathrm{q}V_{bf1\_back}}{\mathrm{k}T}\right) \quad (14)$$

where V_{ch} is the volume of channel under TG, N_C is the conduction band effective density of states, $V_{\Delta C}$ is the difference of conduction band between PPD and channel region. From (14), the potential height on the path of charge transfer from TG channel to PPD is:

$$V_{bf1\_back} = V_{\Delta C} - \frac{kT}{\mathrm{q}} \times \ln\left(\frac{N_e}{N_C V_{ch}}\right) \quad (15)$$

On the condition of strong inversion state, it's assumed that the energy difference of conduction band in channel equals to

the change of surface potential in the given TG voltage fall time due to capacitive coupling.

$$V_{\Delta C} = V_{\Delta C0} - \alpha a t \tag{16}$$

where a is the fall rate of gate voltage.

$$a = \frac{V_{TG\_HIGH} - V_{TG\_LOW}}{t_{fall}} \tag{17}$$

where $V_{\mathrm{TG\_HIGH}}$ and $V_{\mathrm{TG\_LOW}}$ are the high and low levels of the TG voltage, respectively. The t_{fall} is the fall time, during which TG voltage changes from $V_{\mathrm{TG\_HIGH}}$ to $V_{\mathrm{TG\_LOW}}$.

From (12)-(17), the current from TG channel to PPD can be derived:

$$I_{TG-PPD} = \frac{N_e I_{0PPD}}{N_c V_{ch}} \exp\left(\frac{-q V_{\Delta C0} + q\alpha a t}{kT}\right) \tag{18}$$

Also, according to the drift-diffusion model, the current density from TG channel to FD node is:

$$J_{TG-FD} = n_e q \mu_n \xi + q D_n \nabla(\Delta n) \tag{19}$$

where μ_{n} is the mobility of electrons, ξ is the electric field on the charge transfer path at the connection of TG and FD, and D_{n} is the diffusion coefficient of electrons.

From Einstein's relation, the following equation is established.

$$\frac{D_n}{\mu_n} = \frac{kT}{q} \tag{20}$$

From (19) and (20), the current from TG channel to FD can be derived:

$$I_{TG-FD} = S_{TG-FD} n q \mu_n \nabla \phi_n \tag{21}$$

where $S_{\mathrm{TG-FD}}$ is the cross-sectional area between TG channel and FD, and ϕ_n is the electron quasi-Fermi potential.

From (14), the energy difference (E_c-E_f) is obtained:

$$E_c - E_f = kT \ln \frac{V_{ch} N_c}{N_e} \tag{22}$$

The variation of ϕ_n is caused by the change of TG voltage and energy difference (E_{c}-E_{f}) in FD node. The change of TG voltage equals to ($\alpha a t$). According to (22), the change of energy difference (E_{c}-E_{f}) in FD node can be obtained:

$$\Delta(E_c - E_f) = kT \ln \frac{V_{ch} N_c}{N_{e0}} - kT \ln \frac{V_{ch} N_c}{N_e} = -kT \ln \frac{N_{e0}}{N_e} \tag{23}$$

Therefore, $\nabla \phi_n$ can be written as:

$$\nabla \phi_n = \frac{1}{d_{TG-FD}} \left(\alpha a t - \frac{kT}{q} \ln \frac{N_{e0}}{N_e}\right) \tag{24}$$

Using $dQ = -q dN_e$, the following equation is obtained:

$$(I_{TG-PPD} + I_{TG-FD})\, dt = dQ = -q dN_e \tag{25}$$

For an electron transfer process, the barrier heights and the amount of electrons in the TG channel are fixed values. From (18)-(25), the integral function can be obtained:

$$\int_0^{t_i} \left[\frac{I_{0PPD} N_e}{N_C V_{ch}} \exp\left(\frac{-q V_{\Delta C0}}{kT} + \frac{q\alpha a t}{kT}\right) + \frac{S_{TG-FD} q \mu_n N_e}{V_{ch} d_{TG-FD}} \left(\alpha a t - kT \ln \frac{N_{e0}}{N_e}\right)\right] dt_i = -q \int_{N_e}^{N_e - 1} dN_e \tag{26}$$

where N_{e} is the number of electrons in the TG channel in a certain t, N_{e0} is the initial number of electrons in the TG channel and t_{i} is the time interval in which an electron is transferred from TG channel.

By (26), the time interval t_{i} is calculated as follows:

$$1 = N_e \left(\frac{I_{0PPD}}{q N_C V_{ch}} \exp\left(\frac{-q(V_{\Delta C0} - \alpha a t)}{kT}\right) + \frac{N_e S_{TG-FD} \mu_n}{V_{ch} d_{TG-FD}} \left(\alpha a t - kT \ln \frac{N_{e0}}{N_e}\right)\right) t_i \tag{27}$$

Substituting (18) into $q dN_i = dQ_i = I_{TG-PPD} dt_i$, we can derive the number of electrons N_{i} that spill back to PPD from time t to time $(t + t_{\mathrm{i}})$:

$$N_i = \frac{N_e I_{0PPD}}{q N_C V_{ch}} \exp\left(\frac{-q V_{\Delta C0}}{kT}\right) \exp\left(\frac{q\alpha a t}{kT}\right) t_i \tag{28}$$

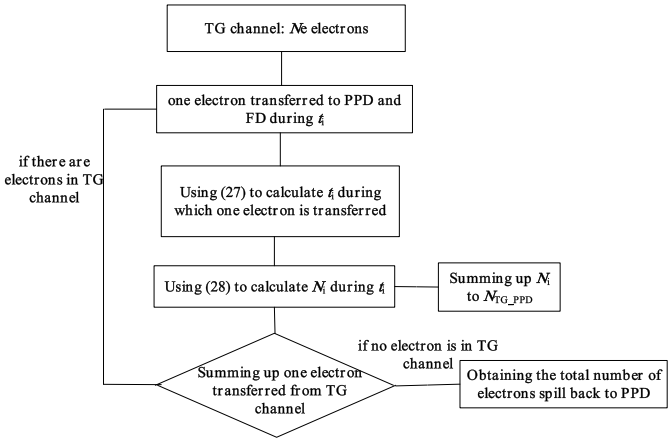

Fig. 6. Simulation procedure based on the thermionic emission and drift-diffusion theory.

Fig.6 shows the simulation procedure to obtain the number of electrons spill back to PPD from TG channel. An instance is demonstrated below based on the above mathematical analysis. TABLE I lists parameters of the mathematical model. The low bias voltage of V_{TG} and V_{RST} is 0 V. Also, the reset voltage of FD node is 3.5 V. In order to analyse the influence of $V_{\mathrm{TG_HIGH}}$and $V_{\mathrm{FD\_RST}}$ on *CTE*, the value of $V_{\mathrm{TG\_HIGH}}$ is changed from 2.8 V to 4.0 V, and $V_{\mathrm{FD\_RST}}$ changes from 2.6 V to 4.0 V.

Fig.7 (a) shows the relationship between TG high gate voltage and the number of electrons spill back to PPD. As$V_{\mathrm{TG_HIGH}}$ increases, the amount of charges stored in the channel under TG is increasing, which means a higher $N_{\mathrm{TG\_PPD}}$. From Fig.7 (a), it can also be noted that a stronger illumination would make more signal charges hold in channel and spill back to PPD region. Fig.7 (b) shows the function

TABLE I
PARAMETERS OF THE MATHEMATICAL MODEL

parameters	value
C_{ox}	3.4 fF
C_s	1.25 fF
C_{FD}	1.5 fF
S_{APPD}	0.12 μm^2
$S_{TG\text{-}FD}$	0.01 μm^2
V_{ch}	0.3 μm^3
t_{fall}	1.0 ns
$V_{\Delta C0}$	0.8 V
V_{bf30}	0.3 V

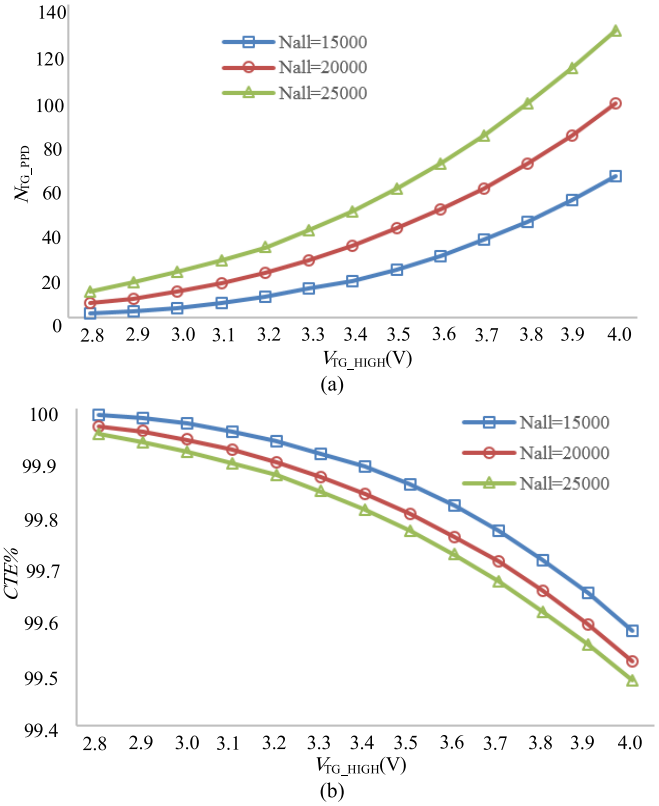

Fig. 7. (a) N_{TG_PPD} versus V_{TG_HIGH} and (b) *CTE* versus V_{TG_HIGH}.

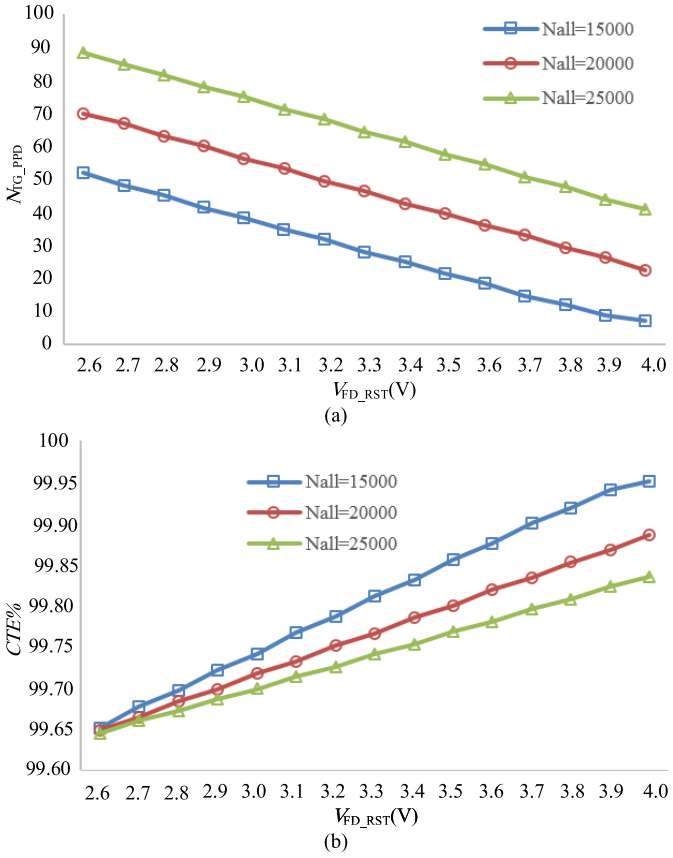

Fig. 8. (a) N_{TG_PPD} versus $V_{FD_RST}$and (b) *CTE* versus V_{FD_RST}.

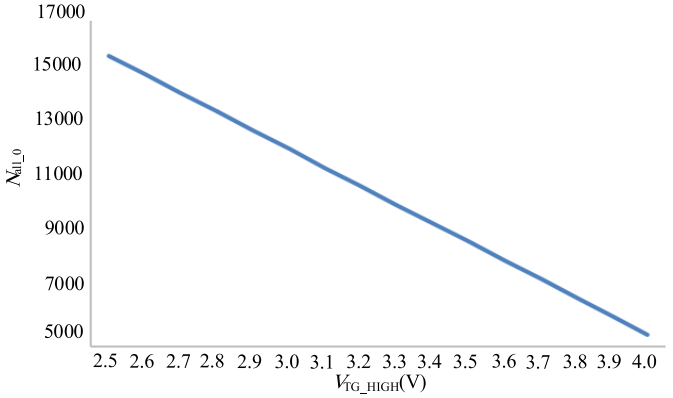

Fig. 9. The relationship between N_{all_0} and V_{TG_HIGH}.

between *CTE* and V_{TG_HIGH}. Thus, in order to obtain a better charge transfer performance, it's expected to adopt a lower gate voltage on the condition of no potential barrier or pocket along the path of charge transfer.

Fig.8 (a) displays the relationship between N_{TG_PPD} andV_{FD_RST}, in which TG voltage V_{TG_HIGH} is 3.5 V. Indeed, the number of charges spill back to PPD decreases linearly with the increase of V_{FD_RST}. It happens because a higher V_{FD_RST} would make a greater charge capacity of FD node. Then there are fewer signal charges stored in channel, resulting in fewer charges spill back to PPD. It's showed that the higher V_{FD_RST} the lower *CTE* in Fig.8 (b). Thus, charge transfer performance in PPD CIS is improved by raising the reset voltage of FD node.

In this paper, the simulated*CTE* is ranged from 99.5% to 100%. 99.5% *CTE* is the worst case in this simulation. The number of photo-generated charges in PPD is 15000. 99.5% *CTE* also means 75 electrons spill back to PPD after charge transfer phase. Actually, the electrons spill back to PPD are a kind of image lag under a certain condition, which has relationship with photo-generated charges in PPD, reset voltage of FD node and TG voltage.

By (8), the signal value is acquired at which, the spill back effect occurs.

$$N_{all\_0} = \frac{C_{FD}\left(V_{FD\_RST} - \alpha V_{TG}\right)}{q} \tag{29}$$

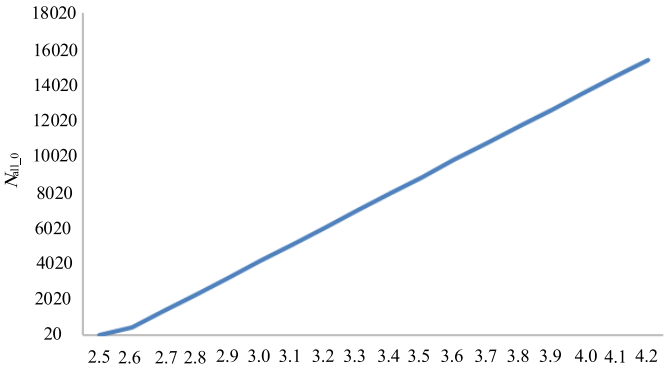

Fig. 10. The relationship between N_{all_0} and V_{FD_RST}.

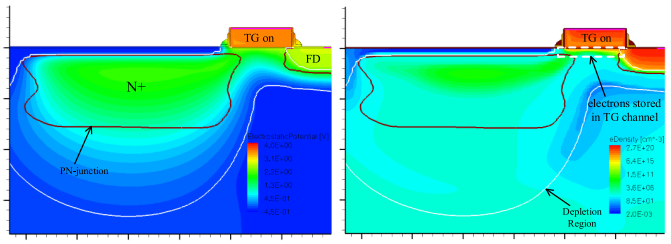

Fig. 11. The potential diagram and electron density when TG is ON.

where N_{all_0} is the signal value at which, electrons begin to appear in the TG channel. Then, electrons stored in TG channel would spill back to PPD during TG is switched from ON to OFF.

When V_{FD_RST} equals to 3.5 V, the relationship between N_{all_0} and $V_{TG_HIGH}$is showed in Fig.9. It can be seen that a higher V_{TG_HIGH} would make the surface potential of TG channel greater. Thus, a fewer photo-generated electrons transferred from PPD to FD could lead to overflow from FD into TG channel. When V_{TG_HIGH} equals to 3.5 V, Fig.10 shows the relationship between N_{all_0} with the reset voltage of FD node. More signal electrons could be held in FD node with a higher voltage differences between TG surface potential and the reset voltage of FD node.

As a conclusion of this part, a lower TG voltage and a higher reset voltage of FD node would bring a weaker spill back effect and means that a stronger illumination could lead to the occurrence of spill back effect. In [13], thanks to dedicated, flexible test chip (CREAPYX) investigations on V_{TG_HIGH} and V_{FD_RST} were obtained. When V_{TG_HIGH} decreases spill back effect occurs for higher signals, which means that a lower V_{TG_HIGH} yields better pixel performances. A higher V_{FD_RST} allows to push back spill back effect to a higher signal value. In [14], by the TCAD simulation, when V_{TG_HIGH} is equal to 3.0 V, the charges spill back to PPD are fewer than those when V_{TG_HIGH} reaches 3.3 V. Furthermore, it is also accessible to observe the spill back effect from the mean–variance curves by testing results. On the condition of a higher V_{TG_HIGH} than 3.0 V, the linearity of digital response will be an issue when the signal level is close to full well capacity. In other words, the simulation results of mathematical model are consistence with the conclusion in [13] and [14].

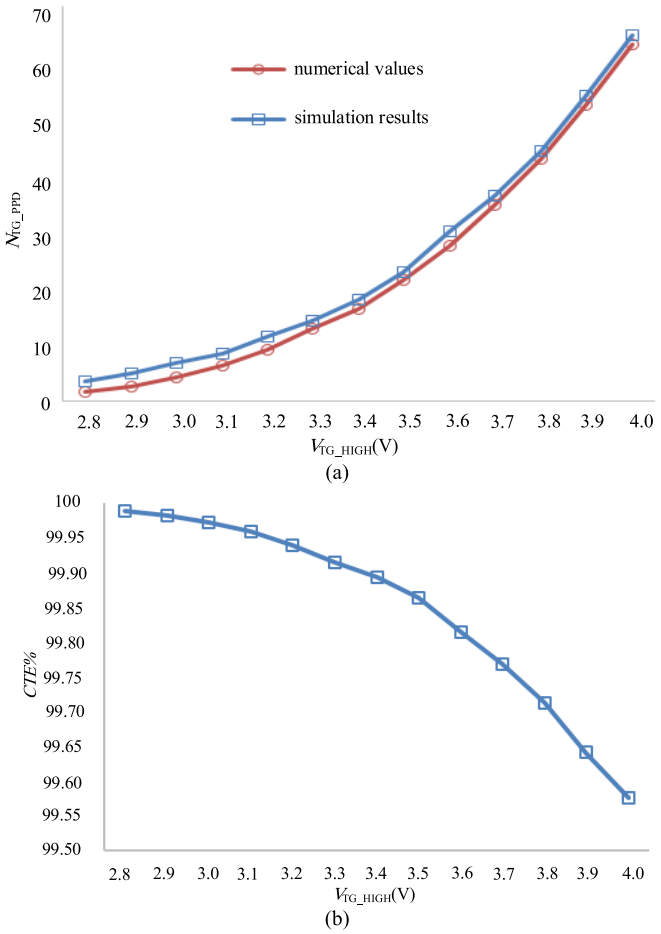

Fig. 12. (a) N_{TG_PPD} as a function of V_{TG_HIGH} by TCAD simulation and mathematical calculation and (b) *CTE* as a function of V_{TG_HIGH} by TCAD simulation.

IV. TCAD Simulations

For verifying the proposed model in section III, a transient simulation is performed by TCAD. In this part, the CIS PPD 4T pixels are designed and simulated by a 0.18 μm CIS technology. The length of PPD, TG and FD is 2.0 μm, 0.6 μm and 1.0 μm respectively. Fig.11 shows the potential distribution and electron density from PPD to FD at the end of charge transfer process by TCAD simulation. The amount of electrons stored in TG channel and spill back to PPD is affected strongly by TG voltage and reset voltage of FD node. The influence of V_{TG_HIGH} and V_{FD_RST} on spill back effect is simulated by TCAD as follows.

A. Influence of V_{TG_HIGH}

Influence of V_{TG_HIGH} on spill back effect is showed in this part. In this simulation process, the low voltage of TG and reset transistor is 0 V. Then, N_{all} is 15000. The number of charges spill back to PPD and *CTE* as a function of V_{TG_HIGH} are showed in Fig.12 (a) and (b), in which it's also depicted that N_{TG_PPD} is strongly affected by V_{TG_HIGH}. It's confirmed that *CTE* decreases with V_{TG_HIGH} increasing. The comparison of *CTE* between simulation and numerical values is also shown in Fig.12 (a). It can be seen from the comparison that the

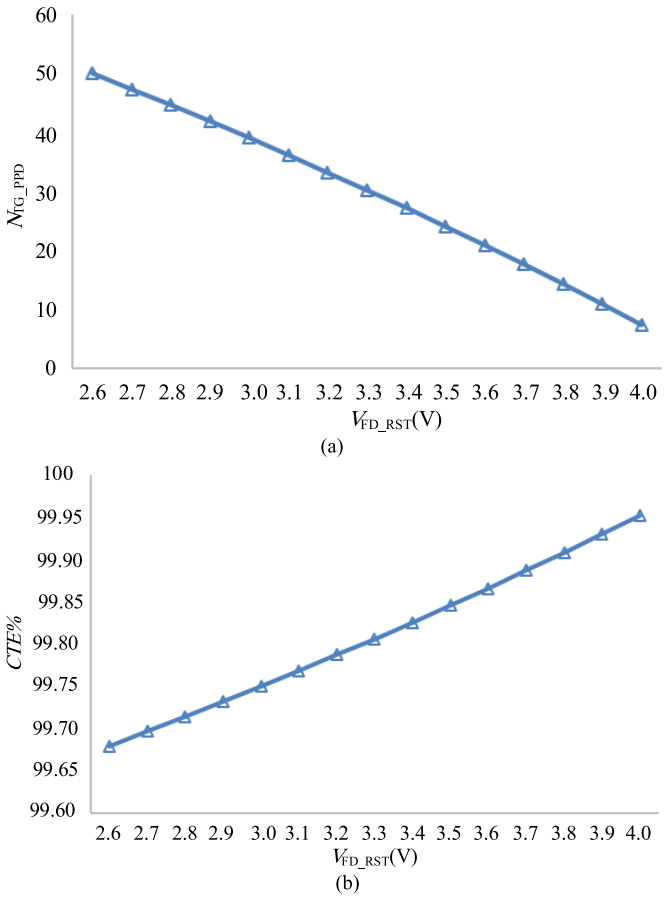

Fig. 13. (a) N_{TG_PPD} as a function of V_{FD_RST} and (b) *CTE* as a function of V_{FD_RST}.

simulation results are in agreement with those of mathematical calculation in section III.

B. Influence of V_{FD_RST}

This part mainly describes the influence of V_{FD_RST} on spill back effect. As showed in Fig.13, with the same signal, the higher the V_{FD_RST} value is, the fewer charges will be stored in the channel under TG. Moreover, the number of charges spill back to PPD would decrease, bringing about a higher *CTE*. In addition, N_{TG_PPD}decrease linearly with V_{FD_RST}, which is consistent with the mathematical model simulation results.

V. Conclusion

To improve *CTE* and alleviate spill back effect, the influence of several pixel operation parameters on spill back effect is studied for a high illumination CIS application. Under the circumstance of no potential barrier or pocket along the path of charge transfer, a lower V_{TG_HIGH} or a higher V_{FD_RST} mitigates spill back effect, contributing to better charge transfer performance. Meanwhile, a lower TG operating voltage and a higher reset voltage of FD node are expected to push spill back effect to higher signal charges. By setting that the gate voltage of TG and the reset voltage of FD is 2.8 V and 3.8 V respectively, the spill back effect of the proposed pixel is completely eliminated. As a result, the proposed mathematical model could explain the physical mechanism of spill back effect. The method to alleviate spill back effect and improve *CTE* is proved to be useful by TCAD simulation.

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Jiangtao Xu (M'02) received the B.E. degree from Tianjin University in 2001, the M.S. and Ph.D. degrees from the School of Electronic Information and Engineering, Tianjin University, in 2004 and 2007, respectively. From 2007 to 2010, he was a Lecturer with the School of Electronic Information Engineering. Since 2010, he has been an Associate Professor with the School of Microelectronics. His research interests are in CMOS image sensor chip and systems, power management circuits, and digital image signal processing circuits.

Ruishuo Wang received the B.E. degree from the School of Microelectronics, Tianjin University, Tianjin, China, in 2017, where she is currently pursuing the M.S. degree in microelectronics and solid electronics. Her research interest focuses on the high CTE pixel in CMOS image sensor.

Liqiang Han received the M.S. and Ph.D. degrees from the School of Electronic Information and Engineering, Tianjin University, Tianjin, China, in 2012 and 2016, respectively. From July 2016 to March 2018, he held a postdoctoral position at Tianjin Universit. Since April 2018, he holds a postdoctoral position at the Electronic Instrumentation Laboratory, Delft University of Technology. His research interests focus on the global shutter/high QE pixel and low-noise CMOS image sensors.

Zhiyuan Gao (M'15) received the B.E. and Ph.D. degrees from the School of Electronic Information Engineering, Tianjin University, Tianjin, China, in 2010 and 2015, respectively. From July 2015 to September 2017, he held a postdoctoral position at Tianjin University. Since September 2017, he holds a postdoctoral position at the Guangdong University of Technology, Guangzhou, China. His research interests span the area of CMOS image sensor pixel, wide dynamic range, and bionic CIS.