Novel method of alignment to buried cavities in cavity-SOI wafers for advanced MEMS devices

Mountain, Christopher ; Kluba, Marta; Bergers, Lambert; Snijder, Jaap; Dekker, Ronald

DOI
10.1016/j.mne.2019.100043

Publication date
2019

Document Version
Final published version

Published in
Micro and Nano Engineering

Micro and Nano Engineering 5 (2019) 100043

Contents lists available at ScienceDirect

Micro and Nano Engineering

journal homepage: www.journals.elsevier.com/micro-and-nano-engineering

Research paper

Novel method of alignment to buried cavities in cavity-SOI wafers for advanced MEMS devices

Christopher Mountain[a,1], Marta Kluba[b,1], Lambert Bergers[c,e,*,1], Jaap Snijder[d], Ronald Dekker[b,e]

[a] Dept. of Bioengineering, The University of Sheffield, England, United Kingdom
[b] Dept. of Microelectronics, Delft University of Technology, the Netherlands
[c] Dept. Mechanical Engineering, Eindhoven University of Technology, the Netherlands
[d] Philips Innovation Services, Eindhoven, the Netherlands
[e] Philips Research, Eindhoven, the Netherlands

ARTICLE INFO

Keywords:
C-SOI
Cavity-SOI
MEMS
Lithography
Alignment
Alignment marker
Wafer stepper

ABSTRACT

Accurate alignment between the cavities in cavity-SOI (c-SOI) wafers and lithography on the wafer surface is essential to advanced MEMS production. Existing alignment methods are well defined, but often require specialized equipment or costly software packages available only in professional manufacturing environments. It would be beneficial for the microfabrication world to be able to utilize standard alignment techniques and tools that are easily available also in smaller MEMS fabrication units and especially the majority of research facilities. Therefore, we demonstrate a feasible method for c-SOI wafer alignment using an ASML PAS5500/100 wafer stepper with standard software configuration by relocating ASML alignment markers towards wafer's edges and utilizing a terracing process to reveal them for alignment. Moreover, we characterize the magnitude and behavior of image offset errors that are introduced using this method. The offset error is found to be inversely proportional to the value of the coordinate in each axis, resulting in images being shifted towards the center of the wafer. The measured offset errors are < 160 nm, and are suitable for most applications. To further minimize these errors we propose a simple model or database of the offsets. We conclude that this alternative alignment method is feasible for a number of MEMS applications, and could promote increased integration of c-SOI technology into advanced MEMS production.

1. Introduction

Cavity-SOI (c-SOI) wafers are an emerging form of advanced substrates used in MEMS processing, which feature cavities below the buried oxide (BOX) layer. In most cases, cavities are etched into a silicon handle wafer, on top of which a silicon wafer is bonded and thinned to produce a device layer, such that MEMS can be fabricated over the cavities [1–4]. These cavities are used to simplify manufacturing [5] or can be integrated into the active, passive or structural elements of the MEMS device [6,7], see Fig. 1. Integration of CMOS and MEMS with cavities has been successful, as demonstrated by commercial availability of pressure sensors and accelerometers in smartphone and automotive applications [7–9]. The realization involves alignment of CMOS wafer to MEMS wafer with either having a cavity, while the alignment and bonding is achieved with industrial wafer alignment tools as the final step [8,10,11]. The utilization of c-SOI substrates can further increase the complexity of 3D devices that can be made, while maintaining compatibility with CMOS processing. Therefore, c-SOI substrates are increasingly used in various microfabrication applications [1–4,7,12]. For correct integration, lithography on the device layer must precisely correspond to the cavities hidden beneath it. Currently the alignment of the device layer to the cavities is still challenging. Overcoming this challenge would push forward the development of devices, that require advanced silicon structures such as next-generation CMOS-MEMS/NEMS [7,13,14], novel and highly integrated biomedical MEMS for implantables [15–19], smart drug delivery [20], catheter-based instruments [21,22], minimally invasive surgery [23,24] and fundamental cell/tissue biology [25–27]. Therefore, an effective and accurate method of aligning these two layers is essential.

Different methods to achieve such alignment are available. In one method, aligned wafer bonding relies on infrared imaging to view

* Corresponding author at: Dept. Mechanical Engineering, Eindhoven University of Technology, the Netherlands.
E-mail addresses: cmountain1@sheffield.ac.uk (C. Mountain), M.M.Kluba@tudelft.nl (M. Kluba), l.i.j.c.bergers@tue.nl (L. Bergers), R.Dekker@tudelft.nl (R. Dekker).
[1] Contributed equally to this work.

https://doi.org/10.1016/j.mne.2019.100043
Received 24 April 2019; Received in revised form 6 August 2019; Accepted 19 August 2019

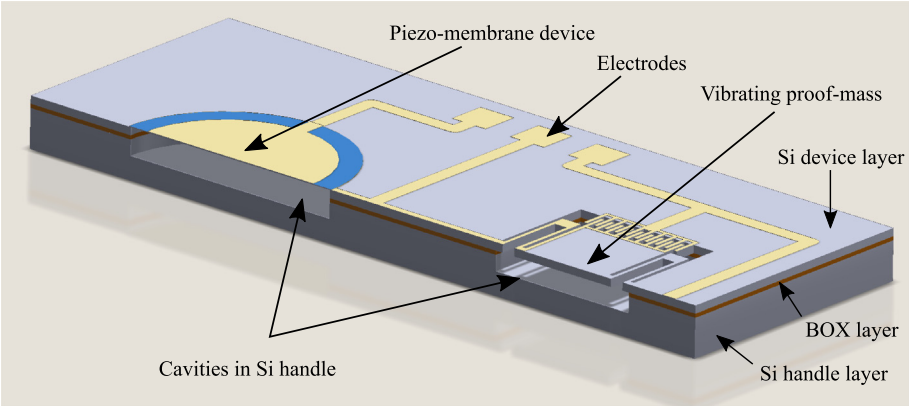

Fig. 1. Example cross-section of a C-SOI device showing pre-fabricated cavities inside the handle layer, used for advanced MEMS production.

buried structures and align them to a pre-fabricated device layer that is bonded on top [10,28] with sub-μm accuracy [29]. However, this method requires specialized equipment, which is not widely accessible, and specialized alignment markers [10,28,29]. An alternative approach is to place alignment markers on the back-side of the wafer, to which the cavities and top devices are both aligned [10,30]. This method however does not yield sub-μm accuracy [10,30] and is infeasible for wafer bonding due to front-side contamination when patterning markers on the back-side. Therefore, it is necessary to define a process whereby alignment to a pre-fabricated c-SOI wafer can be achieved using non-specific front-side alignment markers.

To this end, a new method is presented using processes commonly used in microfabrication facilities, e.g. a wafer stepper (ASML PAS5500/100) and dry etching, without expensive software- or hardware modifications. This wafer stepper detects markers on the substrate, which are simple diffraction gratings, by illuminating them with a 633 nm laser and tracking the diffracted beam with a photodiode system. An alignment feedback loop positions the wafer such that the markers provide optimal diffracted signal [31]. This alignment method is suitable for thin film 2D microfabrication, but needs to be extended to allow for true 3D microfabrication. To do so, we propose a method that involves patterning ASML alignment markers on the front-side of the handle wafer beneath the BOX layer. These alignment markers are to be detected through/below the top device layer and subsequently used to pattern new alignment markers on top of the device layer. The new markers would serve for further lithography of the device layer. The challenge is to detect the alignment markers with the alignment system, and to achieve sub-μm alignment of the top surface, on the device layer, to the pattern below the BOX on the handle layer. The alignment is analyzed through the measurement of offsets of the patterned alignment markers.

2. Detection of alignment markers

The PAS5500 wafer stepper detects markers on the substrate, using a 633 nm laser alignment system. The marker position is subsequently measured using laser interferometry with an accuracy of ~0.08 μm, allowing computation of the wafer's position relative to the stepper's projection optics [31]. Previous work has shown that certain alignment markers buried beneath the silicon device layer can be viewed with visible wavelengths provided the layer is suitably thin, e.g. 80 nm [32]. However, much thicker device layers, up to 80 μm for some novel MEMS applications [16], may inhibit optical detection of the markers. Modeling the attenuation of the diffraction signal suggests strong signal drop, falling below the detection limit of the wafer stepper. Proof-of-concept experiments for this scenario would be informative, but are impractical in this work, as they require manufacturing tools for producing the actual SOI wafer with alignment markers in the handle layer.

For these reasons, an alternative method is devised, involving relocation of the markers to the wafer edge, in order to take advantage of a 'terracing' process, common for SOI wafers. This process removes silicon from the edge of the device layer during SOI manufacturing by beveling. Non-standard positioning of the alignment markers to within 4 mm of the wafer edge places them in the terraced region (see Fig. 2A), thus revealing the markers for optical detection after beveling.

Several problems are anticipated with this process, such as edge effects during lithography, where exposure is performed on or near the edge bead, possibly resulting in dosage variations leading to imperfect marker exposure. Furthermore, the wafer edge can be exposed to debris and contamination during handling that cause micromasking effects during etching. Moreover, variability in dry etching at the wafer's edge could cause problems, because the diffraction intensity is optimal for a certain alignment marker depth. Furthermore, subsequent lithography

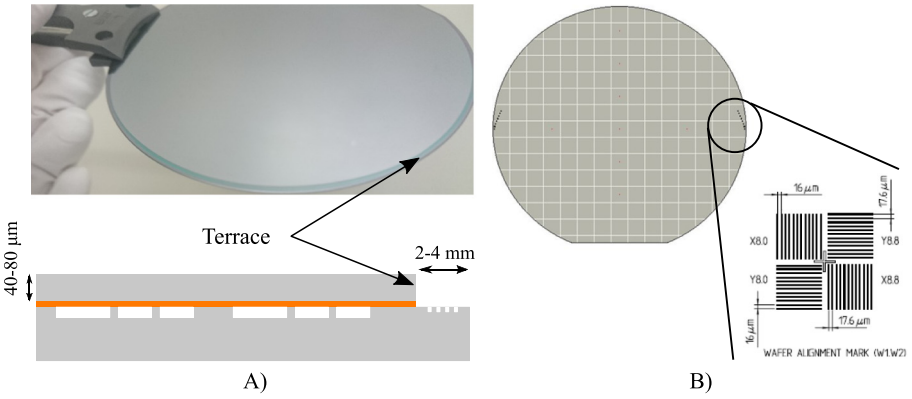

Fig. 2. (A) The c-SOI wafers are produced with a 2–4 mm terrace, where the device layer is removed down to the BOX on the handle wafer around the rim of the substrate. (B) A schematic showing the non-standard positioning of alignment markers used for detection experiments on standard 6-in. silicon wafers. The markers are positioned close enough to the wafer edge that 'terracing' reveals them for optical detection.

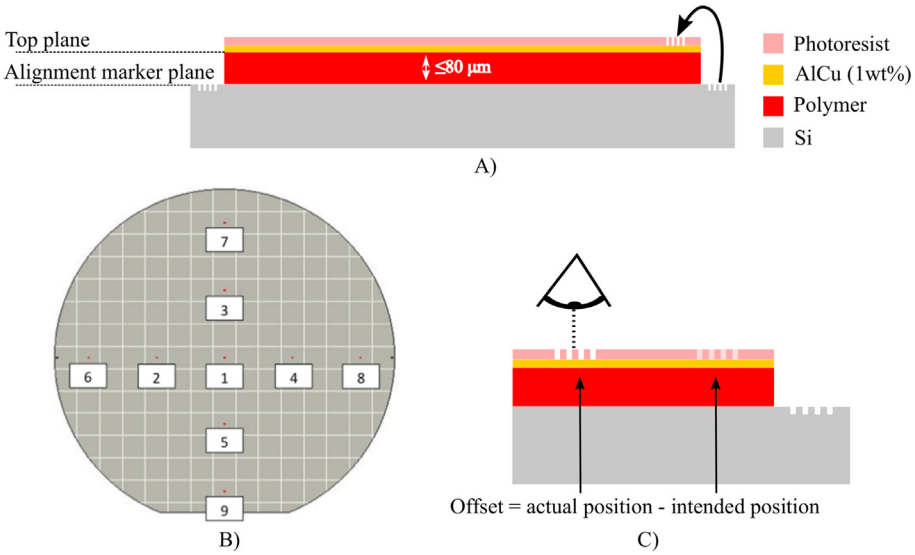

Fig. 3. (A) Cross-section showing the layers fabricated to create a geometric simulation of the proposed terraced wafer. (B) Alignment markers were fabricated at 9 locations (red dots) on the wafer surface plane. (C) The offset was calculated by measuring the markers' positions (C). (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

of c-SOI could leave resist on the alignment markers, effecting their reflectivity. Therefore, the key parameters to control and measure are the locations of the markers, specifically, their proximity to the wafer edge, and their subsequent detectability in the wafer stepper.

Five silicon wafers (6 in. diameter, 675 µm thick, < 100 > orientation) were spin coated with 1300 nm of HPR504 positive photoresist, which was exposed with the alignment marker pattern in the wafer stepper. Each wafer featured eight pairs of markers placed at intervals in the range of 0.8 mm–4 mm from the wafer edge (see Fig. 2B); 0.8 mm being the minimum optical clearance required on all sides of a marker, and 4 mm being the limit of the available terracing process. Following resist development, for two wafers the markers were dry etched in silicon (SPTS Pegasus DRIE etching tool) with a target depth of 140 nm (~0.25*wavelength of diffraction laser), after which the resist of these two wafers was stripped in oxygen plasma. The etched depth was measured with stylus profilometry (Dektak XT, 2.5 µm tip) on one wafer to quantify edge effects. The wafers were then re-inserted into the wafer stepper, with a special program to locate, focus and align to each respective pair of markers. The three wafers with markers-in-resist served to mimic lithography conditions in subsequent device layer patterning, when spin coated resist can reduce reflectivity of alignment markers. The two wafers with markers-in-silicon served as a control of maximum reflectivity.

No edge effects were visible after spin coating. Following exposure and etching, it was found that markers nearest to the wafer's edge were over-etched by up to 14 nm over the target depth of 140 nm (see online Supplementary Fig. S1), possibly due to higher concentrations of etchant species in this region. Marker depths approached the target depth as distance from the wafer edge increased. Subsequent re-insertion into the stepper resulted in successful location and alignment of all specimens. Furthermore, analysis of the signal quality from each marker, a relative metric computed by the stepper, showed no significant variation with respect to distance from the wafer's edge (see online Supplementary Fig. S2). The signal quality *SQ* was constant with the position of alignment markers. It was high (SQ = ~85%) for silicon surfaces and adequate (SQ = ~35%) for silicon wafers on which the markers were patterned in resist. Offset in focus for the resist-coated wafers served as worst alignment condition and showed no significant change of SQ either. This indicates that the alignment system is robust to edge effects on the markers and the surface reflectivity. Furthermore, the marker over-etch had no negative effect on the quality of the signal returned and alignment was successful with all tested markers. However, to avoid edge effects, the optimal position of alignment markers should be as far from the edge as possible while maintaining a distance of 0.8 mm from the terrace edge. This is to avoid obstruction of the light beam by the terrace.

3. Multi-height alignment on thick device layers

The second technical challenge arises from the fact that the alignment markers lie at a different height to the wafer's top surface. Alignment markers are placed at the surface of the handle layer of the c-SOI, while processing occurs on the surface of the device layer. When aligning wafers, the wafer stepper initially levels the wafer by detecting its surface and vertically translating the stage to ensure the surface lies within the focal range, specified as ± 25 µm for this wafer stepper [25,26]. For c-SOI wafers with thick device layers, device thickness > 50 µm, the focusing would be out of specification. Therefore, we investigate problems introduced by height difference of up to 80 µm between the top surface plane and the plane of the alignment markers. Anticipated problems include failure to align, out-of-focus exposure of patterns on the top plane and position errors in those patterns. Therefore, the key parameters to measure are the ability of the stepper to align to the markers, as well as the offset of patterns exposed at the surface of the device layer.

The method devised to test this involved creating proof-of-concept wafers that geometrically simulate the c-SOI wafer having a thick device layer. A terrace was created, which mimicked the device layer, while alignment markers in the silicon substrate simulated the alignment markers of the cavity pattern in the handle layer. Coating the terrace with positive photoresist allowed exposure of new features on top to characterize the key parameters. These features were again alignment markers, because the wafer stepper has built-in metrology to measure their position. The offset was then determined as the difference between the target position and actual measured position of each marker.

The fabrication of the proof-of-concept wafers commenced with lithography and etching of alignment markers on silicon monitor wafers at 1.2 mm from the wafer edge (see Fig. 3A). Two approaches were considered to simulate the device layer using thick polymeric layers. On one set of wafers, AZ40XT photoresist was spin coated to an average thickness of 30.0 µm (SD = 0.2 µm), followed by a 5 mm edge bead removal to create a terrace in the resist, and finally a hard bake according to manufacturer specifications. On the other wafers, 80 µm thick self-adhesive polyimide foil was manually applied, then selectively cut and peeled around the wafer edge to create the terrace. These approaches provided effective methods of quickly simulating thick device layers without encountering difficulties involved in wafer bonding.

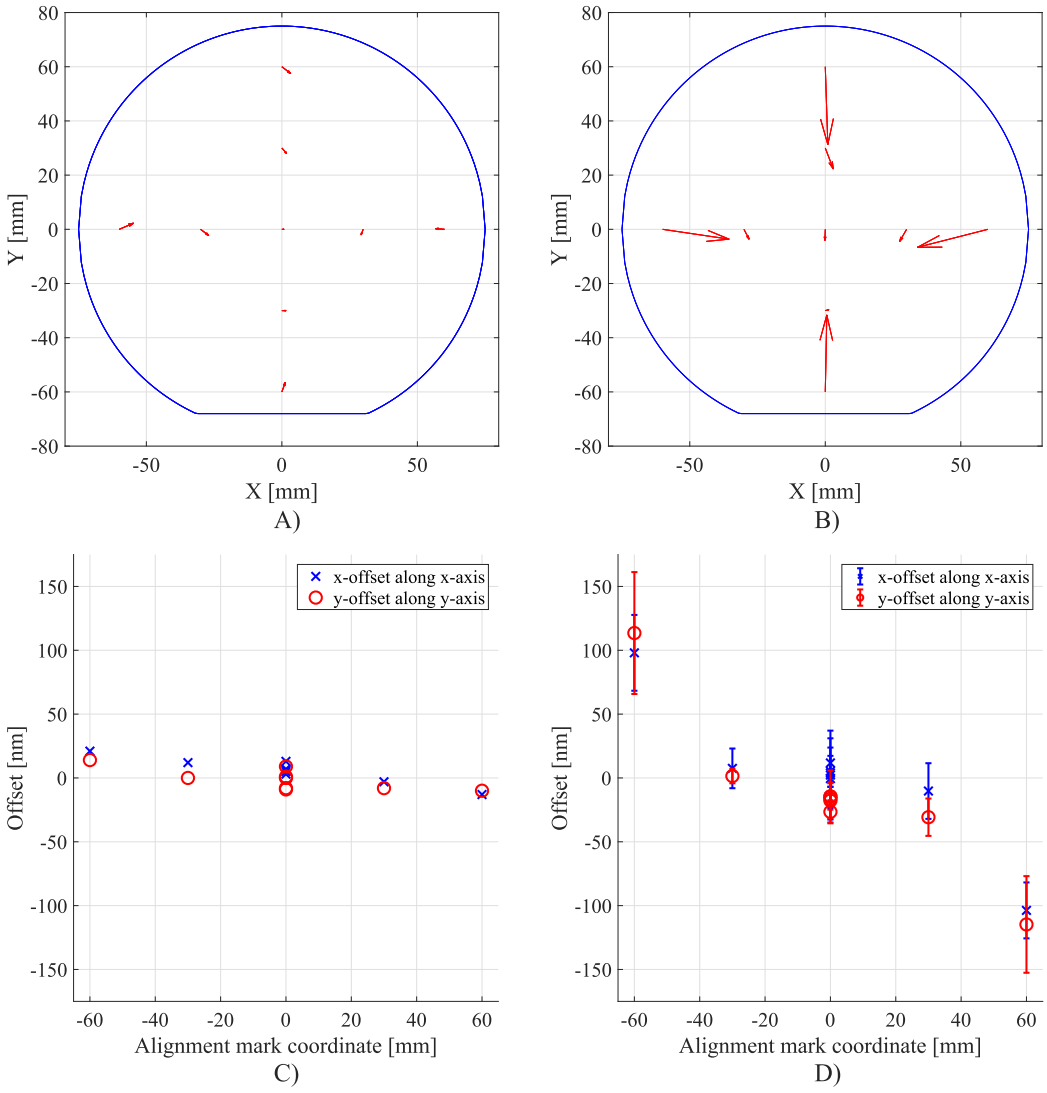

Fig. 4. Vector plots of offsets across the wafer reveal that the offsets are towards the center of the wafer with an amplitude of < 25 nm for the control wafer (A) and < 160 nm for wafers with an 80 µm device layer (B). Plotting the x- and y- components as function of the x-axis value and y-axis value respectively shows an inverse correlation, but with large spread for both the control wafer (C) and the wafer with 80 µm device layers (D). Error bars indicate 1σ standard deviation.

Each simulant device layer was sputter coated with 100 nm of Al(1 wt %)Cu for optical opacity, to ensure that this plane would be detected as the wafer surface during the leveling operation in the stepper. As a control situation, a control wafer was made without the device layer or metal to benchmark the offset error in case of regular lithography. All wafers were then spin-coated with 1300 nm of HPR504 positive resist, with a 5 mm edge bead removal to remove any resist covering the alignment markers in the silicon substrate. The wafers were aligned in the wafer stepper using these markers and 9 new markers in the resist at the top surface plane in a range of locations (see Fig. 3B). These markers were developed in the resist, but not etched. The wafers were re-placed in the stepper, which aligned to the markers in the silicon and measured the coordinates of the surface markers. The offset vector was then calculated as the difference between measured and target position (see Fig. 3C).

The wafer stepper successfully detects and aligns to markers at both 30 µm and 80 µm below the surface plane of the wafer. Subsequently, the wafer stepper successfully exposes new markers in focus at the wafer surface and detects these markers post-development. Analysis of the amplitude of the offset shows that it increases from an average of 14 ± 5 nm for a reference wafer to an average of 62 ± 8 nm for the 80 µm device layer (see online Supplementary Fig. S3). However, per wafer the spread in offset is large, with standard deviations up to 60 nm. A detailed analysis per wafer reveals that the offset amplitude increases with radial position of the marker (see online Supplementary Fig. S4). For the control wafer, the offset amplitude increases from a few nm to < 25 nm with increasing radial position from center (0 mm) to the edge (60 mm). For the 80 µm thick device layers the offset amplitude increases from 20 nm to nearly 160 nm with increasing radial position. The dependence of offset amplitude on layer thickness and radial position could be due to wafer-stage positioning inaccuracies (specified at 0.08 µm) or projection inaccuracies resulting from non-flatness of the thick-polymeric layer. Nonetheless, this offset for thick device layers only increases by a factor of 2 compared to the wafer stage positioning accuracy or by a factor of 5 when compared to the control wafer. This performance is better than conventional back side alignment (2–3 µm offset) and at par with commercial state-of-the-art wafer-bonding systems (< 0.5 µm) [10]. This would be sufficiently small for many MEMS applications, while enabling compatibility with CMOS applications, where offsets < 0.5 µm are required.

Reduction of the offset error, especially for devices patterned at large radial positions, might be possible by determining possible systemic errors. A model might be derived from an analysis of the components of the offset as a function of the radial location. This analysis

reveals that the offsets, both for control wafer and for wafers with 80 um terrace, are in the direction of the wafer center, see Fig. 4A,B. The x and y components of the offset appear to be inversely proportional with respectively the x and y axis of the wafer, see Fig. 4C,D. Correcting a projection by subtracting an average offset of a certain radial position would be most practical. The spread in offset is large across the wafer compared to the average offset for radii < 30 mm. Thus, for images with coordinates < |30| mm correcting a projection with the average offset will not necessarily improve the alignment. However, for images with coordinates |60| mm radius, the spread in the offset component is much smaller than the average, so correcting a projection with this average will improve the alignment. Alternatively, to fully minimize the offset, a database could be setup for each wafer in which the offset per image is stored for subsequent lithography steps. Hence, these two methods could be applied to further reduce offsets if necessary.

4. Conclusions

This work developed an easily accessible and cost-efficient process for alignment of patterns on thick device layers to cavity patterns in handle layers of pre-fabricated cavity SOI wafers. The process was implemented for an ASML PAS5500-stepper and does not involve any special lithography or alignment equipment. The process involves patterning alignment markers to the wafer edge of the handle layer and utilizing a wafer-edge terracing process to reveal them after bonding the SOI wafer. The standard alignment system of the employed wafer stepper successfully detected these markers. Subsequent successful patterning of secondary alignment markers on wafers with different device layer thicknesses, mimicked using polymeric layers of 30 µm and 80 µm thickness, demonstrated the feasibility of this approach. Quantification of the offset due to out-of-plane alignment and image projection revealed an increase in offset amplitude from < 25 nm for control wafers to < 160 nm for wafers with 80 µm thick device layers. The offsets are towards the center of the wafer and are largest for radial positions bigger than 30 mm. Although the offsets are small enough for most MEMS applications, correction of offsets could be possible. This could be achieved by determining the average offset at large radii, or by storing all offset values in a per-wafer database, and correcting image projections with these values.

This novel alignment process is feasible with standard cleanroom equipment, while providing alignment performance at par with state-of-the-art wafer bonding technologies. c-SOI wafers could be sourced from commercial SOI suppliers that offer c-SOI products, and then be further processed in-house. In-house, the presented alignment process may be incorporated into CMOS, MEMS and NEMS technologies. This could enable the development of advanced thick cavity-based MEMS devices, potentially leading to novel, highly integrated, and more cost-effective (bio) microsystems and microdevices.

Supplementary data to this article can be found online at https://doi.org/10.1016/j.mne.2019.100043.

Acknowledgements

The authors would like to extensively acknowledge Okmetic Oy (Vantaa, Finland). This work is part of the POSITION-II Project funded by the ECSEL Joint Undertaking under grant number Ecsel-783132-Position-II-2017-IA (www.position-2.eu).

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

References

[1] C. Liu, J. Froemel, J. Chen, T. Tsukamoto, S. Tanaka, Laterally vibrating MEMS resonant vacuum sensor based on cavity-SOI process for evaluation of wide range of sealed cavity pressure, Microsyst. Technol. 1 (2018), https://doi.org/10.1007/s00542-018-3984-1.
[2] Y. Zhang, C. Yang, F. Meng, G. Liu, C. Gao, Y. Hao, A monolithic integration multifunctional MEMS sensor based on cavity SOI wafer, IEEE SENSORS 2014 Proc, IEEE, 2014, pp. 1952–1955, , https://doi.org/10.1109/ICSENS.2014.6985414.
[3] G. Wu, D. Xu, B. Xiong, Y. Wang, A high-performance bulk mode single crystal silicon microresonator based on a cavity-SOI wafer, J. Micromech. Microeng. 22 (2012) 025020, , https://doi.org/10.1088/0960-1317/22/2/025020.
[4] J. Xu, X. Zhang, S.N. Fernando, K.T. Chai, Y. Gu, AlN-on-SOI platform-based micromachined hydrophone, Appl. Phys. Lett. 109 (2016) 032902, , https://doi.org/10.1063/1.4959078.
[5] O. Oy, SOI Wafers, https://www.okmetic.com/products/product-portfolio/soi-wafers, (2018) , Accessed date: 20 December 2018.
[6] A.S. Ergun, G.G. Yaralioglu, O. Oralkan, B.T. Khuri-Yakub, MEMS/NEMS techniques and applications, in: C.T. Leondes (Ed.), MEMS/NEMS, Springer US, Boston, MA, 2006, pp. 553–615, , https://doi.org/10.1007/0-387-25786-1_16.
[7] A.C. Fischer, F. Forsberg, M. Lapisa, S.J. Bleiker, G. Stemme, N. Roxhed, F. Niklaus, Integrating MEMS and ICs, Microsyst. Nanoeng. 1 (2015) 15005, , https://doi.org/10.1038/micronano.2015.5.
[8] D.R. Sparks, W.J. Baney, S.E. Staller, D.W. Chilcott, J.W. Siekkinen, Method for making an All-silicon capacitive pressure sensor, US5706565A, https://patents.google.com/patent/US5706565, (1998).
[9] D.R. Sparks, S.R. Zarabadi, J.D. Johnson, Q. Jiang, M. Chia, O. Larsen, W. Higdon, P. Castillo-Borelley, A CMOS integrated surface micromachined angular rate sensor: its automotive applications, Proc. Int. Solid State Sensors Actuators Conf. (Transducers '97), IEEE, 1997, pp. 851–854, , https://doi.org/10.1109/SENSOR.1997.635235.
[10] T. Plach, B. Rebhan, V. Dragoi, T. Wagenleitner, M. Wimplinger, P. Lindner, (Invited) High accuracy aligned wafer bonding for wafer-level integration, ECS Trans. 86 (2018) 145–158, https://doi.org/10.1149/08605.0145ecst.
[11] S.S. Nasiri, A.F.J. Flannery, Method of fabrication of Al/Ge bonding in a wafer packaging environment and a product produced therefrom, US 9,533,880 B2, 2017. https://patents.google.com/patent/US9533880B2/en.
[12] H. Luoto, K. Henttinen, T. Suni, J. Dekker, J. Mäkinen, A. Torkkeli, MEMS on cavity-SOI wafers, Solid. State. Electron. 51 (2007) 328–332, https://doi.org/10.1016/j.sse.2007.01.007.
[13] H. Qu, CMOS MEMS fabrication technologies and devices, Micromachines 7 (2016) 14, https://doi.org/10.3390/mi7010014.
[14] L.G. Villanueva, J. Bausells, J. Brugger, Grand challenge in N/MEMS, Front. Mech. Eng. 1 (2016), https://doi.org/10.3389/fmech.2015.00015.
[15] G. Yang, Implantable Sensors and Systems, Springer International Publishing, Cham, Switzerland, 2018, https://doi.org/10.1007/978-3-319-69748-2.
[16] M. Kluba, B. Morana, A. Savov, H. van Zeijl, G. Pandraud, R. Dekker, Wafer-scale integration for semi-flexible neural implant miniaturization, Proceedings 2 (2018) 941, https://doi.org/10.3390/proceedings2130941.
[17] J.P. Seymour, F. Wu, K.D. Wise, E. Yoon, State-of-the-art MEMS and microsystem tools for brain research, Microsyst. Nanoeng. 3 (2017) 16066, , https://doi.org/10.1038/micronano.2016.66.
[18] E.Y. Chow, S.P. Sanghani, V. Ramesh, Emerging research in wireless and MEMS for medical applications, Wirel. MEMS Networks Appl, Elsevier, 2017, pp. 153–175, , https://doi.org/10.1016/B978-0-08-100449-4.00007-5.
[19] Y. Xu, X. Hu, S. Kundu, A. Nag, N. Afsarimanesh, S. Sapra, S.C. Mukhopadhyay, T. Han, Silicon-based sensors for biomedical applications: a review, Sensors 19 (2019) 2908, https://doi.org/10.3390/s19132908.
[20] H. Zhang, J.K. Jackson, M. Chiao, Microfabricated drug delivery devices: design, fabrication, and applications, Adv. Funct. Mater. 27 (2017) 1703606, , https://doi.org/10.1002/adfm.201703606.
[21] S.P. Lee, L.E. Klinker, L. Ptaszek, J. Work, C. Liu, F. Quivara, C. Webb, C. Dagdeviren, J.A. Wright, J.N. Ruskin, M. Slepian, Y. Huang, M. Mansour, J.A. Rogers, R. Ghaffari, Catheter-based systems with integrated stretchable sensors and conductors in cardiac electrophysiology, Proc. IEEE 103 (2015) 682–689, https://doi.org/10.1109/JPROC.2015.2401596.
[22] B. Mimoun, V. Henneken, A. van der Horst, R. Dekker, Flex-to-rigid (F2R): a generic platform for the fabrication and assembly of flexible sensors for minimally invasive instruments, IEEE Sensors J. 13 (2013) 3873–3882, https://doi.org/10.1109/JSEN.2013.2252613.
[23] J. Gafford, T. Ranzani, S. Russo, A. Degirmenci, S. Kesner, R. Howe, R. Wood, C. Walsh, Toward medical devices with integrated mechanisms, sensors, and actuators via printed-circuit MEMS, J. Med. Device 11 (2017) 011007, , https://doi.org/10.1115/1.4035375.
[24] V. Sonetha, P. Agarwal, S. Doshi, R. Kumar, B. Mehta, Microelectromechanical systems in medicine, J. Med. Biol. Eng. 37 (2017) 580–601, https://doi.org/10.1007/s40846-017-0265-x.
[25] F. Zheng, F. Fu, Y. Cheng, C. Wang, Y. Zhao, Z. Gu, Organ-on-a-chip systems: microengineering to biomimic living systems, Small (2016) 1–30, https://doi.org/10.1002/smll.201503208.
[26] B. Tian, S. Xu, J.A. Rogers, S. Cestellos-Blanco, P. Yang, J.L. Carvalho-de-Souza, F. Bezanilla, J. Liu, Z. Bao, M. Hjort, Y. Cao, N. Melosh, G. Lanzani, F. Benfenati, G. Galli, F. Gygi, R. Kautz, A.A. Gorodetsky, S.S. Kim, T.K. Lu, P. Anikeeva, M. Cifra, O. Krivosudský, D. Havelka, Y. Jiang, Roadmap on semiconductor–cell biointerfaces, Phys. Biol. 15 (2018) 031002, , https://doi.org/10.1088/1478-3975/aa9f34.

[27] P. Pan, W. Wang, C. Ru, Y. Sun, X. Liu, MEMS-based platforms for mechanical manipulation and characterization of cells, J. Micromech. Microeng. 27 (2017) 123003, , https://doi.org/10.1088/1361-6439/aa8f1d.
[28] R.W. Bower, M.S. Ismail, US005485919A, 1993. doi:US005485919A.
[29] C. Wang, T. Suga, Nanoprecision aligned wafer direct bonding and its outlook, 2011 12th Int. Conf. Electron. Packag. Technol. High Density Packag, IEEE, 2011, pp. 1–4, , https://doi.org/10.1109/ICEPT.2011.6066807.
[30] ASML, Recent Advancements in Double Sided Alignment and Back-side Alignment, https://staticwww.asml.com/doclib/misc/asml_20070323_04_SA_Tech._Symp._presentation_3DAlign_v2.pdf, (2007) (accessed December 20, 2018).
[31] L. Fuller, S. Bolster, Introduction to ASML PAS 5500 Wafer Alignment and Exposure, https://people.rit.edu/lffeee/Lithography-ASML.pdf, (2019) (accessed December 21, 2018, n.d.).
[32] T.M. Chung, B. Olbrechts, U. Södervall, S. Bengtsson, D. Flandre, J.-P. Raskin, Planar double-gate SOI MOS devices: fabrication by wafer bonding over pre-patterned cavities and electrical characterization, Solid. State. Electron. 51 (2007) 231–238, https://doi.org/10.1016/j.sse.2007.01.017.