Spiral inductor modeling for RFIC using RLCK model order reduction

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Abstract.

Accurate and reliable models for integrated spiral inductors are required at design time of integrated circuits dedicated for RF applications. Electromagnetic solvers require long simulation times, especially taking into account advanced technology improvements like thick metal layers, substrate effects, etc. VeloceRF is a tool dedicated to analyse and model integrated spiral inductors. It is integrated into the design environment. Intelligent model order reduction needs to be used on the parasitics generated by VeloceRF in order to speed up the simulation times by another order of magnitude. This paper is about the successful application of VeloceRF and Jivaro on a WLAN power amplifier testcase.

I. Introduction

RFICs are becoming more complex, packing several functions and supporting multiple frequency bands and wireless standards. Modeling inductance in its intended (e.g. spiral) and parasitic forms is crucial for successful design. This is uniquely handled by Helic's VeloceRF™ tool, which rapidly models inductance across the chip and produces RLCK netlists. Netlist size and appropriateness for simulation is of concern, particularly for large-scale designs dominated by interconnect parasitics and mutual inductances. Fortunately, edXact's Jivaro™ tool can now dramatically reduce large netlists arising from RLCk extraction, slashing simulation time with minimal sacrifices in accuracy. In this paper we demonstrate how VeloceRF and Jivaro can be ideally combined in a fast, efficient and accurate RFIC design flow. A real-life circuit design is showcased.

II. Design of Multi-Turn Inductors

The on-growing trend towards high-frequency wireless products and the increasing frequencies of operation have pushed integrated inductor research at the highest levels over the past two decades. Today's state of the art wireless analog circuitry relies heavily on efficient inductor design accompanied by models that are reliable over a very wide range of frequencies. Inductors offer enhanced reliability and efficiency in the circuits where they are employed while allowing higher levels of integration through the replacement of some of today's off-chip components.

Low-noise amplifiers (LNA's) utilize integrated inductors to achieve input-impedance matching without deteriorating noise performance. When used as loads, inductors improve the gain capability of the amplifier while reducing its power consumption. Other RF circuits that incorporate inductors and transformers are voltage-controlled oscillators (VCO's), power amplifiers (PA's). The quality factor of the on-chip inductor affects significantly the behavior of such circuits; hence, the design of such passive devices remains of major importance.

Silicon technologies present a challenge in efficient inductor integration as the semi-conducting nature of the substrate is the cause of reduced inductor performance and the source of high-order electromagnetic effects that are difficult to isolate, quantify and model.

Accurate and reliable models are required at design time and only a systematic, analytical approach of the inductor behaviour can produce robust equivalent and scalable predictive models.

Electromagnetic (EM) solvers can be used to model inductive devices sufficiently. However, they require long simulation times that make the design process prohibitively lengthy. Technology advancements such as the The inclusion of thick Au or Cu metal layers, the use of multilayer substrates and additional device features such as patterned ground shields [1] make things worse as simulation times and required computer resources increase in a geometric manner. Also, the complexity of designs nowadays demands the modeling of mutual inductance effects which are global and if predicted accurately can be put in good use by the design. As a result, the simulation space is not limited to a single inductive component, but may include several inductors and transformers interacting with each other and/or other neighboring passive components. Given the iterative nature of the design process, EM tools are rendered inefficient for rapid and flexible RF design.

VeloceRF™ is an EM tool that is seamlessly integrated in the RF design flow and analyses and models accurately inductive components like multi-turn inductors and interconnects in a very fast manner, allowing flexible and very rapid design. The latest state-of–the art inductor designs like stacked-via inductors with polysilicon shields are dealt with by VeloceRF™ without the burden of long simulations times. In a more generic manner, VeloceRF™ can be employed to model mutual inductance effects between inductive devices and other critical parts of a chip and validate their influence on the design specification during the design process. VeloceRF outputs a distributed lumped element RLCk netlist and/or scattering parameters.

III. Model Order Reduction for RLCK

On-chip inductive effects are becoming increasingly important with the advances in process technology and especially with higher frequencies of operation [2-3]. Many commercial and proprietary extraction tools like Star RCXT (Synopsys), XCalibre (Mentor Graphics) or Assura (Cadence) model inductive, capacitive and ohmic effects by using RLCK circuits. These parasitic components together with the designed circuitry are then analyzed using spice or fast-spice simulators.

The typical data volume of those parasitic components significantly degrades the performance of the simulators, with respect to run-time and memory consumption. Over more than the last decade a lot of energy has been spent on MOR (model order reduction), which aim at replacing the parasitics model by an equivalent model of smaller model order.

This attempt usually has to trade-off between accuracy of the reduced model (and the result as a whole) and the speedup of the simulation process.

AWE (asymptotic waveform evaluation) was one of the first methods proposed based on matching moments in the complex frequency domain [4]. This was extended [5] to moment expansions at several points in the complex plane. Main problems arise with ill-conditioned matrices for the moments, which was attempted to be resolved by PVL [6], introduced in 1994. An alternative to the Lanczos process (PVL) was introduced with Arnoldi [7], later congruence transformation [8]. Main advantage of the congruence techniques is preservation of passivity. A very popular example of congruence transformation is PRIMA [11]. It can also guarantee stability.

Unfortunately, those methods are too general and complicated for ultra large scale integrated circuits. Moreover, additional capabilities are important for EDA software: exploitation of hierarchy.

Recently, realizable reduction was addressed for RC circuits [10] by preserving the Elmore delay time constant. The approach is attractive, since it works locally and generates guaranteed stable and passive circuits. This approach is very powerful, however strongly limited to simple interconnect

structures. RC ladders, fingered structures, or heavily cross-coupled nets cannot be reduced with sufficient reduction.

Often, very simplistic approaches can be found in today's EDA tools, that simply filter small or large values by setting thresholds. Those approaches can be very effective with respect to reduction, however, they fail completely with respect to accuracy or stability.

Especially in high-frequency circuits with signals below minus 60dBm, accuracy of the reduced order model is hard to achieve with acceptable effort. Moreover, purely RC parasitics circuits can be seen as low pass filters and simplifying approaches are easily at hand. RLCK circuits are completely different, since their behavior in frequency domain is much more complex than for RC circuits and the problems with stability and passivity are a real concern.

JIVARO is a suite of tools dedicated to model order reduction. It contains the most advanced algorithms that are chosen intelligently depending on the kind of circuit and the simulations carried out. It is the first set of tools, that consequently exploit both structural algorithms like [10] and purely mathematical ones [2-9, 11], combined with circuit partitioning and data range equilibration. The support of hierarchy is ensured, which is a very important feature as stated before.

Multi-Turn Inductor Netlist

We first investigate the effects of netlist reduction on a single, multi-turn, differential octagonal spiral inductor (Figure 1). The inductor under test has five turns and a diameter of 317 μm. A netlist model for the spiral was produced using VeloceRF. The tool's modeler produces distributed lumped-element models for inductors, employing several R, L, C and k elements.

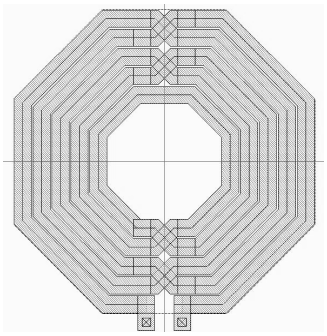

Figure 1.Multi-turn inductor layout view

The original netlist produced by VeloceRF was reduced using the Jivaro netlist reduction tool, following two alternatives for the reduction bandwidth: 15 and 3 GHz. The 15-GHz model is presumably more accurate, as it includes more elements. The reduction in terms of netlist elements is presented in **Error! Reference source not found.**.

To calculate inductance (L) and quality factor (Q) AC analysis was performed. The results are plotted in Figure 2. It is obvious that the 15-GHz reduced model tracks excellently the distributed VeloceRF model across the entire frequency range (DC-20 GHz). The 3-GHz reduced model is also quite accurate, missing only the self-resonance frequency of the spiral by a small margin. Arguably, even the 3-GHz model is fit for simulations at frequencies below resonance.

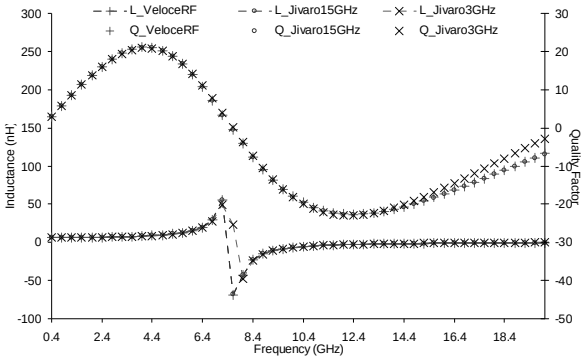

Figure 2: Inductance and quality factor using unreduced and reduced netlists

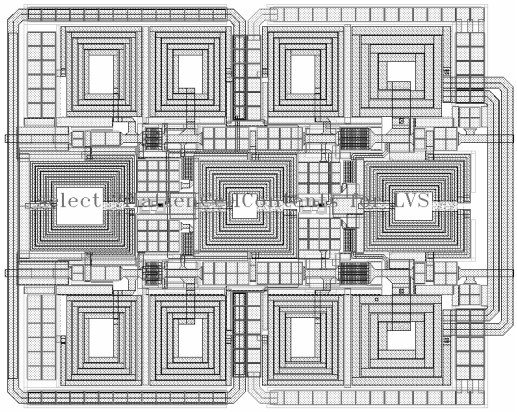

Figure 3: PA layout

Table I

	VeloceRF unreduced netlist	Jivaro reduction (15GHz)	Jivaro reduction (3GHz)
Total # of lines	1982	913	377
		-53.94%	-80.98%
Total # of k's	1324	423	15
		-68.05%	-98.87%
Total # of L's	60	31	6
		-48.33%	-90.00%
Total # of R's	181	152	127
		-16.02%	-29.83%
Total # of C's	332	280	202
		-15.66%	-39.16%

IV. WLAN Power Amplifier testcase

To assess the effects of netlist reduction on the simulation of a demanding RF circuit, the case of a WLAN PA (frequency range: 2.4 - 2.5 GHz) is investigated. The layout of the complete PA is shown in Figure 3. Several high-Q inductors are used for input, output and inter-stage matching. To minimize die size the spirals are packed closely, while their magnetic interaction is used constructively for optimizing the gain characteristics of the amplifier. This is made possible by VeloceRF's capability to extract full distributed mutual inductances, along with the netlists for each spiral. Additionally, the interface in VeloceRF automatically merges the inductance netlist with the output of the layout extraction tool, so a netlist becomes available for the complete circuit, including the RLCk model for the inductors, all mutual inductances and all interconnect parasitics (RC).

The resulting netlist is understandably quite large, so Jivaro reduction comes in handy. The reduction engine was applied, again with 15 and 3 GHz bandwidth settings, and the unreduced and reduced netlists were used for simulating the key performance metrics of the PA: S-parameter response and output harmonics. Table I summarizes the reduction results in terms of netlist size and simulation time savings. The S-parameter curves of the PA for the three different netlists are displayed in Figure 4. The harmonic analysis results are tabulated in Table II.

The 15-GHz reduced model tracks very well the linear gain and return loss characteristics of the unreduced model, as well as the non-linear harmonic results (maximum deviation is 0.15 dB), while it reduces simulation time by as much 65%.

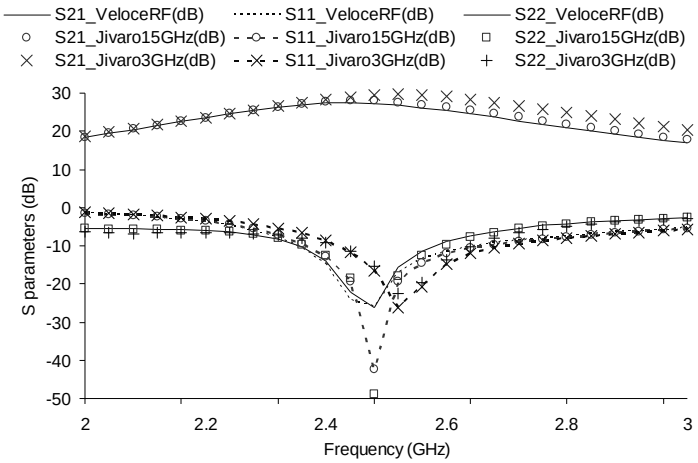

Figure 4: The S-parameter response of the PA for the three different RLCk netlists

The 3-GHz model brings even more drastic savings in analysis time, while it exhibits deviations in frequency response only above 2.5 GHz, and tracks the harmonic output fairly well up to the third harmonic tone. Therefore, even the 3-GHz model is useful for fast analysis, if signoff accuracy is not needed.

Table I

	VeloceRF unreduced netlist	Jivaro reduction (15GHz)	Jivaro reduction (3GHz)
Total # of lines	76903	50176	29673
		-34.75%	-61.42%
Total # of k's	23676	14768	1596
		-37.62%	-93.26%
Total # of L's	285	205	57
		-28.07%	-80.00%
Total # of R's	27756	22430	22281
		-19.19%	-19.73%
Total # of C's	25353	10896	2782
		-57.02%	-89.03%
SP analysis time (sec)	280.82	117.68	40.6
		-58.09%	-85.54%
Harmonic analysis time (sec)	693.44	241.31	122.28
		-65.20%	-82.37%

Table II

harmonic tone (GHz)	VeloceRF unreduced netlist, dBm	Jivaro reduction (15GHz), dBm	Jivaro reduction (3GHz), dBm
2.45	15.08	15.08	15.06
4.9	-55.77	-55.73	-56.11
7.35	-49.70	-49.69	-49.51
9.8	-84.73	-84.58	-78.51
12.25	-71.10	-71.09	-70.96
14.7	-102.39	-102.35	-99.26

V. Conclusions

Inductance model netlists produced by VeloceRF are efficiently reduced by Jivaro, to bring significant savings in simulation times, for linear and non-linear analyses. Excellent model fit for spiral inductors is demonstrated. In the case of a complex RF PA circuit with several cross-coupled inductors and parasitics, reduction slashes netlist size and simulation time by as much as 85%, with minor deviations in S-parameter results and less than 0.15 dB deviations in non-linear harmonic output. Dramatic improvements and savings are demonstrated for RFIC design flows, since now complex inductance effects can be accurately modeled with speed and ease, enabling the verification of complete chips within reasonable times.

About VeloceRF

Helic's VeloceRF™ is the leading EDA tool for spiral inductor synthesis, inductance modeling and verification, adopted by several renowned semiconductor companies worldwide. For additional information please visit Helic online at www.helic.com or contact veloceRF_sales@helic.com.

About Jivaro

Edxact's Jivaro™ is the leading standalone netlist reduction engine for parasitic netlists, containing lumped RLCK elements. Jivaro™ is available for analog, RF, mixed-signal and digital netlists. It

has successfully been evaluated by major semiconductor companies. For additional information please visit Edxact online at www.edxact.com or contact info@edxact.com.

VI. References

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