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Singh, Gagan Deep; Nemati, Hossein Mashad; Alavi, Morteza S.; de Vreede, Leonardus Cornelis Nicolaas

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An Inverted Doherty Power Amplifier Insensitive to Load Variation With an Embedded Impedance Sensor in Its Output Power-Combining Network

Gagan Deep Singh, *Graduate Student Member, IEEE*, Hossein Mashad Nemati, Morteza S. Alavi, *Member, IEEE*, and Leonardus Cornelis Nicolaas de Vreede, *Senior Member, IEEE*

***Abstract*— This article presents an inverted Doherty power amplifier (IDPA) made load insensitive up to 2:1 voltage standing wave ratio (VSWR) across its fractional bandwidth with a very compact wideband impedance sensor embedded in its output power-combining network (OPCN). To correct for load variation, a low-loss tunable resonator (TR) is used to ensure ohmic loads to the main and peaking stages at the center frequency of operation. At off-center frequencies, TR is used to present an ohmic load for the main stage, while a digitally adjustable phase shifter is used to (re)align the main and peaking stage's current summation in the OPCN. For ohmic load deviations, the main and peaking stage supply voltages and input drives are adjusted to maintain the ideal Doherty's output power and efficiency profile related to nominal 50 Ω loading across the bandwidth. To implement the control of the formerly mentioned technique, a wideband impedance sensor is proposed, which uses the orthogonality of incident and reflected waves and requires only four peak detectors. As proof of principle, a prototype 850–950-MHz IDPA featuring the proposed correction technique, the impedance sensor, and the control loop has been implemented as a printed circuit board (PCB) demonstrator. Measurement results show that the IDPA can maintain constant output power with a tolerance of only ±0.2 dB while improving the drain efficiency and linearity across the entire fractional bandwidth (11%) for a VSWR range of 2:1.**

***Index Terms*— DC–DC power converters, impedance sensor, inverted Doherty power amplifier (IDPA), load-insensitive power amplifiers (PAs), tunable phase shifter, tunable resonators (TRs).**

I. Introduction

THE ever-growing demand for higher data rates is being met through the increased use of spectrally efficient signals, larger modulation bandwidths, higher operating frequencies, and interference reduction techniques such as beam steering. This combination of techniques enforces stringent performance requirements on radio frequency (RF) power amplifiers (PAs) which need to amplify signals with large peak-to-average power ratio (PAPR), video bandwidth, RF bandwidth, and be tolerant to changing voltage standing wave ratio (VSWR) conditions in handsets from the antenna input impedance variation due to hand effect [1] or in base stations, from the undesired mutual coupling in the multiantenna beam steering structures [2], [3]. The Doherty PA (DPA) is a popular choice to satisfy most of these requirements [4], [5], since it can efficiently amplify signals with large video bandwidth and PAPR; moreover, its high bandwidth operation is not limited by the need for a fast, as well efficient dc modulator as required in the envelope tracking architecture [6]. However, conventional DPAs can be used only over a narrow RF bandwidth. Therefore, inverted DPA (IDPA) topologies offering higher RF bandwidths have gained popularity [7], [8], [9], [10]. Unfortunately, DPAs are very sensitive to changing VSWR conditions [11], [12]. Various techniques exist in the literature to overcome the VSWR sensitivity of the DPA/PA. These can be broadly classified into five groups.

The first and most traditional technique is using an isolator to break the reciprocity of the network, thereby isolating the DPA from the load and presenting a constant impedance to the DPA. However, isolators are bulky, expensive, and need a third port termination to dissipate the reflected power from load mismatch. They also have a magnetic field around them, posing integration challenges. Recent works have demonstrated magnetic-free isolators, but have higher insertion loss [13], [14]. Second, in theory, a tunable matching network (TMN) can correct for changing VSWR conditions and omits any reflection losses [15], [16], [17], [18], [19], [20]. However, a successful low-loss TMN realization relies heavily on the availability of tunable components with extremely high-Q, high-tuning range, and breakdown voltage [21]. Therefore, practical TMNs have high insertion losses [15], [16], [17], [18], [19], [20]. To reduce the insertion loss of TMN, a hybrid approach of using an adjustable supply voltage and input drive in combination with a low-loss tunable resonator (TR) was proposed in [21] for a class-B PA and in [22] for a DPA, but only across a narrow RF bandwidth. Third, a balanced configuration can function as an isolator, but does this correctly only in power back-off conditions, as its branch PAs still see (opposite) changing loading conditions [23], [24]. Fourth, reconfigurable DPAs have recently received considerable interest,

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Gagan Deep Singh, Morteza S. Alavi, and Leonardus Cornelis Nicolaas de Vreede are with the Department of Microelectronics, Delft University of Technology, 2628 CD Delft, The Netherlands (e-mail: g.d.singh@tudelft.nl; S.M.Alavi@tudelft.nl; l.c.n.devreede@tudelft.nl).

Hossein Mashad Nemati was with Huawei Technologies Sweden AB, 412 50 Gothenburg, Sweden. He is now with Infineon Technologies AG, 81726 Munich, Germany (e-mail: hossein.nemati@infineon.com).

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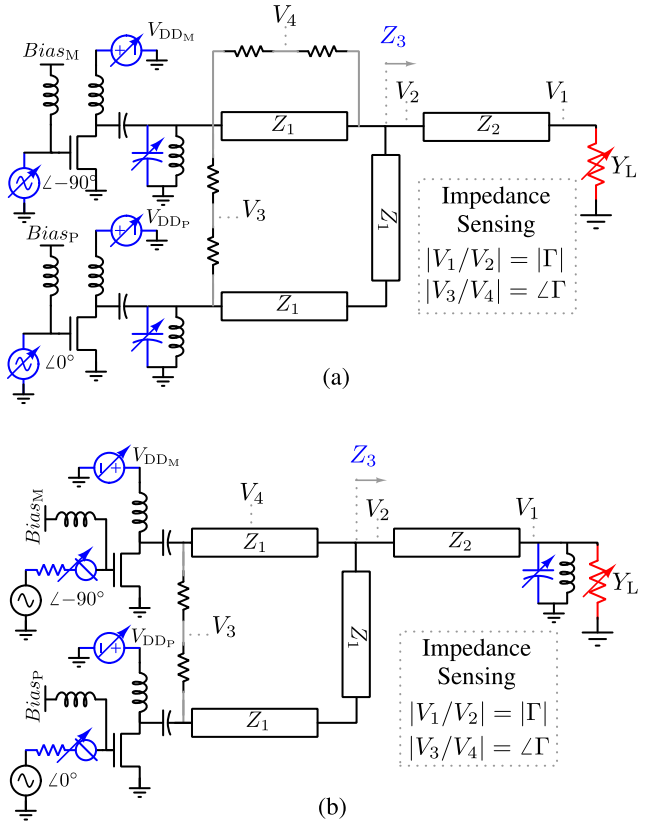

Fig. 1. Proposed (a) load-insensitive IDPA with the wideband impedance sensor embedded into its output power-combining network. The voltage ratios $|V_1/V_2|$ and $|V_3/V_4|$ point to $|\Gamma|$ and $\angle\Gamma$, respectively, and (b) finally implemented circuit with digitally tunable input amplitude and phase.

namely, transconductance (g_m) and phase adjustments (tunable phase shifter) of the carrier and peaking amplifiers [25]. A reconfigurable series/parallel switchable Doherty [26], [27]. Furthermore, to enhance the performance of this concept, a switchable series/parallel Doherty using a coupler with complex impedance termination at the isolation port and adjustable gate bias is proposed in [28]. Switching between a balanced PA and DPA configuration using a silicon-on-insulator (SOI)-based single-pole-double-throw (SPDT) switch [29] and multiport active load-pull [30]. These techniques do not fully restore the DPA performance from the impact of the applied load mismatch but rather try to "soften" the consequences of this load mismatch. Fifth, concepts based on the use of digital predistortion (DPD). Namely, it is known that the load sensitivity of a DPA will affect its output power, causing (large) variations in the direction of the main beam, its nulls, and side lobes levels when applied in a beamforming antenna array [31]. Correcting this change requires a complex crossover DPD [32], which increases the overall power consumption. For example, it was shown in [33] that the DPD-related power consumption can exceed the overall PA power consumption, even when handling two antennas.

Furthermore, an output impedance sensor is needed to effectively apply the formerly mentioned techniques, e.g., TMN, reconfigurable DPA, and complex DPD. Various active and passive sensing methods exist in the literate [21]. The active method typically uses a coupler to extract the reflected signal due to load mismatch and uses mixer-based amplitude and phase detection [18], [34], [35]. However, the insertion loss of the coupler cascaded in the RF path tends to increase both the loss and size [36]. Moreover, active impedance detection methods are more complicated when working with high bandwidth modulated TX signals [21]. Passive magnitude-only detection methods do not require any knowledge of the signal content and can handle very large modulation bandwidths. However, typically, they have a large footprint and need extensive calibration and computation to determine the effective PA loading [37], [38]. Moreover, to reduce the footprint, works have focused on directly embedding the impedance sensing into the PA output matching network (OMN) [38], [39]. A multiport reflectometry theory can be applied to an arbitrary linear network and, therefore, to the existing OMN of a PA [36]. However, having many ports in the OMN introduces extra loss. Furthermore, these earlier proposed embedded impedance sensing techniques are narrowband in nature.

In contrast, this article proposes a wideband DPA load correction technique demonstrated using an IDPA with embedded wideband load-mismatch sensing in its output power-combining network (OPCN) (see Fig. 1). It can act on the (slow, milli/micro-second) load changes caused by the hand effect or beam steering. It builds on the techniques proposed in [21], [22], and [40]. This work uses a low-loss TR from [21] and load-insensitive DPA concept from [22], [40] and extends them to wideband operation. The most important contributions of this work compared with the prior state-of-the-art [21], [22], [28], [40] are as given below.

1) A low-loss TR facilitating low-Q impedance matching across VSWR and frequency has been integrated into a wideband inverted Doherty power combiner to present ohmic loading conditions to the main stage under all the conditions.
2) An embedded tunable phase shifter in the input allows realignment of the main and peaking stage currents across VSWR and frequency, lowering the requirements on the capacitance-tuning range and Q-factor of the TR even further.
3) A novel, wideband impedance sensor (using only four peak detectors) facilitating cointegration in the inverted Doherty OPCN.

The proposed DPA combination provides so far, unseen functionality. Namely, a standalone DPA that delivers constant output power over the full VSWR $\leq$ 2 range and IDPA bandwidth, while simultaneously improving drain efficiency and linearity. The realized demonstrator features a single RF input and single external supply and has embedded mismatch VSWR detection. As such, it allows the use of an unaltered 50 Ω DPD correction set for any load within the 2:1 VSWR (0°–360°) circle. Furthermore, the phase control is also helpful in accommodating the relatively large changes in the output capacitance [41] of the PA stages when adjusting their supply voltages.

The outline of this article is as follows. In Section II, the wideband load-insensitive IDPA topology is proposed. In Section III, the wideband impedance sensor embedded in the OPCN of the IDPA is introduced. Section IV gives the

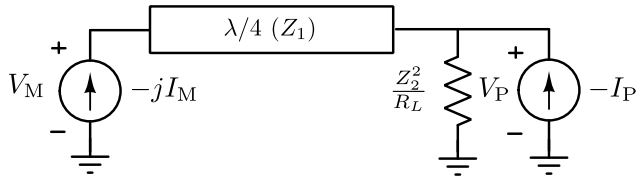

Fig. 2. IDPA circuit [see Fig. 1(a)] modeled as an ideal DPA circuit for the center frequency of operation.

printed circuit board (PCB) prototype design details. Section V provides the measurement results. The article is concluded with a discussion of the achieved performance in Section VI.

II. Wideband Load-Insensitive IDPA

In this section, the IDPA performance is analyzed, and it is shown that the proposed technique can recover the IDPA performance from load mismatch over its entire fractional operation bandwidth. To analyze the proposed circuit of Fig. 1, the main and peaking stages are modeled as ideal current sources. At its center frequency, the circuit in Fig. 1 can be reduced to the configuration shown in Fig. 2. Using the transmission line ABCD parameters [42] and the circuit shown in Fig. 2, the following matrix is found

$$\begin{bmatrix} V_{\rm M} \\ -jI_{\rm M} \end{bmatrix} = \begin{bmatrix} 0 & jZ_1 \\ j(1/Z_1) & 0 \end{bmatrix} \begin{bmatrix} V_{\rm P} \\ I_{\rm P} + V_{\rm P}[R_{\rm L}/(Z_2)^2] \end{bmatrix}. \quad (1)$$

Using (1), the voltages across the main and peaking PA stages for ohmic loading conditions are found to be

$$V_{\rm P} = -Z_1 I_{\rm M}\ (a), \quad V_{\rm M} = -jZ_1\left(I_{\rm M}\frac{Z_1 R_{\rm L}}{Z_2^2} - I_{\rm P}\right)\ (b). \quad (2)$$

From (2a) and (2b) and the topology shown in Fig. 2, it can be observed that for the center frequency, the circuit is basically equivalent to [22], [40], but includes an extra impedance inversion due to transmission line (Z_2). To make the DPA insensitive to load variation at its center frequency of operation, the procedure in [22], [40] needs only minor adjustments. Namely, the required supply voltages ($V_{\rm DD_M,R_L}$, $V_{\rm DD_P,R_L}$) and current drives ($I_{\rm M,R_L}$, $I_{\rm P,R_L}$) needed to handle an arbitrary load ($R_{\rm L}$) can be found by keeping the main and peak PA output powers constant ($P_{\rm out_M} = 0.5V_{\rm M}I_{\rm M}$) in power back-off ($I_{\rm P} = 0$) and at peak power conditions. Using (2a) and (2b), and expressing these quantities in terms of the nominal loading condition ($R_{\rm L_{opt}}$) with voltages ($V_{\rm DD_M}$, $V_{\rm DD_P}$) and currents ($I_{\rm M}$, $I_{\rm P}$), yields

$$V_{\rm DD_M,R_L} = V_{\rm DD_M}\sqrt{\frac{R_{\rm L}}{R_{\rm L_{opt}}}}\ (a), \quad I_{\rm M,R_L} = I_{\rm M}\sqrt{\frac{R_{\rm L_{opt}}}{R_{\rm L}}}\ (b) \quad (3)$$

$$V_{\rm DD_P,R_L} = V_{\rm DD_P}\sqrt{\frac{R_{\rm L_{opt}}}{R_{\rm L}}}\ (a), \quad I_{\rm P,R_L} = I_{\rm P}\sqrt{\frac{R_{\rm L}}{R_{\rm L_{opt}}}}\ (b). \quad (4)$$

The output power and drain efficiency can be determined using (1) and (2) to obtain the loading impedance of the main ($Z_{\rm M}$) and peaking ($Z_{\rm P}$) stage and substituting them in (5)–(7) where $I_{\rm Mfund,R_L}$ and $I_{\rm Pfund,R_L}$ are the amplitudes of the fundamental components of $I_{\rm M,R_L}$ and $I_{\rm P,R_L}$, respectively,

$$P_{\rm out} = \frac{1}{2}I^2_{\rm Mfund,R_L}{\rm Re}(Z_{\rm M}) + \frac{1}{2}I^2_{\rm Pfund,R_L}{\rm Re}(Z_{\rm P}) \quad (5)$$

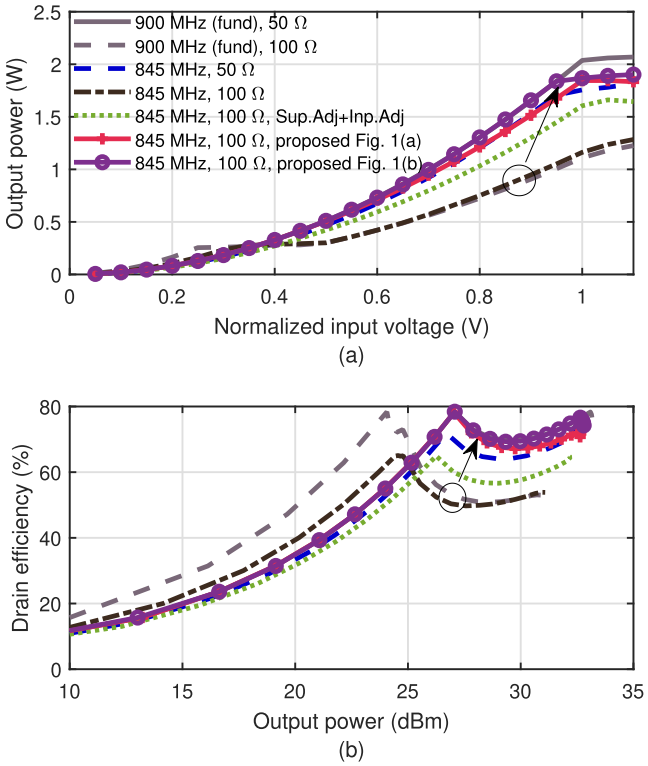

Fig. 3. Simulated inverted Doherty (a) output power in watts and (b) drain efficiency, assuming ideal class-B operation across bandwidth and impedance mismatch, for four cases. 1) IDPA operated at its center frequency of 900 MHz and load set to its nominal value of 50 Ω, 2) load mismatched to 100 Ω at 900 MHz, 3) load mismatched to 100 Ω at 845 MHz with input drive and supply adjustment for the main and peaking stage, and 4) load mismatched to 100 Ω at 845 MHz with input drive and supply adjustment along with TR/TMN matching to the ohmic line.

while the overall dc power consumption can be calculated using the (average) dc currents of the main and peak devices. For ideal class-B operation (rectified current sine wave), these can be written in terms of their fundamental amplitude and supply voltages (6) allowing the calculation of the efficiency (7)

$$P_{\rm dc} = \frac{2}{\pi}(I_{\rm Mfund,R_L}V_{\rm DD_M,R_L} + I_{\rm Pfund,R_L}V_{\rm DD_P,R_L}) \quad (6)$$

$$\eta_{\rm drain}(\%) = \frac{P_{\rm out}}{P_{\rm dc}}100. \quad (7)$$

To verify the former principle of operation, the IDPA schematic of Fig. 1(a) is used with the following nominal circuit parameters; $V_{\rm DD_M} = 6.4$ V, $V_{\rm DD_P} = 6.4$ V, and $g_{\rm m} = 0.64$ S, and the transmission line impedances are set to $Z_1 = 20\ \Omega$ and $Z_2 = (25Z_1)^{0.5}$. The transmission line Z_2 acts only as a prematch, converting the external (nominal) 50 Ω load into Z_3, which needs to be $Z_1/2$ (representing the conventional symmetrical Doherty matching conditions). Furthermore, all the harmonics are short-circuited (ideal class-B operation). Using these settings, the IDPA performances is tested for the 50-Ω nominal loading condition across its fractional bandwidth, which is defined in this work by the frequencies at which the output power drops by 1 dB, and was found to be ≈22% centered around 900-MHz frequency. The simulated IDPA performances with ideal components

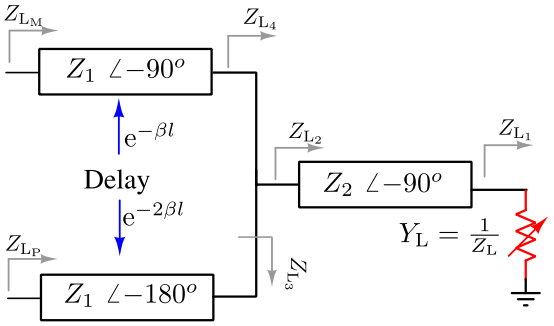

Fig. 4. IDPA OPCN (see Fig. 1) used to formulate the compensating shunt susceptance and relative phase between main and peaking stages as a function of frequency.

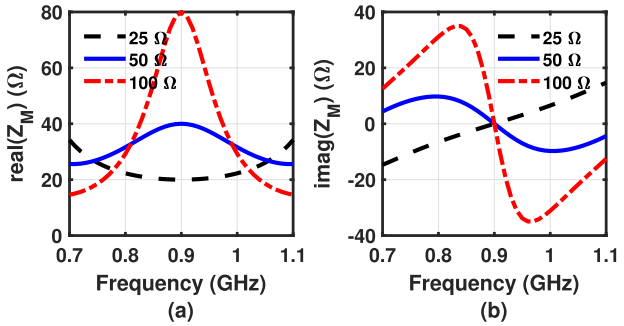

Fig. 5. Impedance offered to the main stage versus frequency. (a) Real part and (b) imaginary part in power back-off.

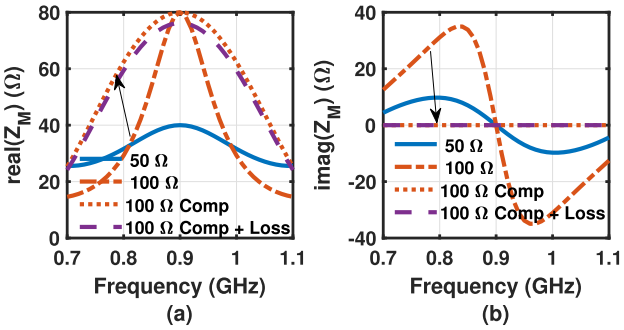

Fig. 6. Impedance offered to the main stage versus frequency. (a) Real part and (b) imaginary part after matching (100 Ω load) to the ohmic line using a TR/TMN with and without loss (see Fig. 1).

for its nominal loading $R_{L_{opt}}$, in terms of output power and drain efficiency at 900 MHz (solid gray line) and 845 MHz (dashed blue line), are shown in Fig. 3. Next, at its design center frequency (900 MHz), the IDPA is subjected to ohmic mismatch ($R_L = 100\ \Omega$), yielding a performance degradation (see Fig. 3(a) and (b), dashed gray line). Using (3) and (4), it is possible to recover and approach the ideal Doherty characteristics by adjusting the supply voltage and input drive of the DPA branches in a mirrored fashion (solid gray line). For complex loads, it is also possible to recover the performance, by first compensating for the reactance/susceptance part using a low-loss TR/TMN [22] [see Fig. 1(a)]. Next, the remaining ohmic (mismatch) can be handled again by adjustment of the supplies and input drive levels using (3) and (4). However, these techniques work only over a narrow frequency band. Moving away from the design frequency even at ohmic loads, the IDPA power-combining network will present non-ohmic loading conditions to its PA branches. This is verified in simulation by subjecting the IDPA operating at 845 MHz to a mismatched load of 100 Ω. This is shown in Fig. 3 (dashed-dotted black line). It can be observed that both the IDPA output power and drain efficiency degrade considerably. The supply and input drive adjustment technique using (3) and (4) is applied to recover the performance. It can be seen that it only partially recovers the performance (dotted green line). The complex impedance seen by the main stage ($Z_{L_M}(f)$) as a function of frequency in power back-off (peak stage turned off) can be derived as follows:

$$Z_{L_M}(f) = Z_1 \frac{Z_{L_4}(f) + jZ_1 \tan\left(\frac{\pi}{2} f/f_0\right)}{Z_1 + jZ_{L_4}(f)\tan\left(\frac{\pi}{2} f/f_0\right)} \tag{8}$$

where $Z_{L_4}(f) = Z_{L_2}(f)||Z_{L_3}(f)$, $Z_{L_3}(f) = -jZ_1\cot(\pi f/f_0)$, and $Z_{L_2}(f)$ in (9) is a function of Z_L

$$Z_{L_2}(f) = Z_2 \frac{Z_L + jZ_2 \tan\left(\frac{\pi}{2} f/f_0\right)}{Z_2 + jZ_L \tan\left(\frac{\pi}{2} f/f_0\right)}. \tag{9}$$

The theoretical/simulated impedance profile of the main stage across frequency as provided by the output power combiner in deep-power back-off is shown in Fig. 5. It can be observed that the main stage impedance is ohmic only at the center frequency (f_0) of operation. This is especially the case when dealing with a higher load impedance (e.g., 100 Ω).

The main stage sees a varying, highly complex load versus frequency in this case. To also handle this condition, we propose to compensate for the complex loading across the main stage using a low-loss TR [see Fig. 1(a)]. The required susceptance (B_{M_X}) to be compensated across frequency at the main stage [see Fig. 1(a)] can be determined using the impedance presented to the main stage $Z_{L_M}(f)$ [see Fig. 4]

$$B_{M_x}(f) = -\mathrm{Im}\left[\frac{1}{Z_{L_M}(f)}\right]. \tag{10}$$

By doing this (using a loss-less TR), an ohmic loading impedance can be maintained at the main stage (for e.g., 100 Ω load) as shown in Fig. 6(a) and (b). The impact of losses in the TR (assuming a tunable capacitor with a quality factor of 20) is also shown (dashed purple line). The required supply voltages and current drives can be found by substituting $R_L = \{[1]/\mathrm{Re}[1/Z_{L_M}(f)]\}$ in (3) and (4). Moreover, low-loss TR can also be used at the peaking stage to compensate for the reactive loading [see Fig. 1(a)]. Consequently, it is possible using the proposed technique to recover the IDPA performance across the fractional bandwidth of interest. This is verified using the simulation results shown in Fig. 3. It can be seen that for the 845-MHz frequency of operation, the proposed technique not only follows the 50-Ω loading output power of the IDPA for the mismatched 100-Ω loading case but also improves the efficiency (>15% compared with the technique in [22] and [40]) in the power back-off. However, having multiple tunable components in the output power-combining stage also increases the losses in practical implementations due

to their finite quality factor. To reduce the number of tunable components required, the circuit in Fig. 1(b) is proposed, which has the TR placed at the Z_L port. This placement lowers the currents flowing in the OPCN under (highly) reactive VSWR loading conditions, as such lowering the losses. The required susceptance $B_{M_X}(f)$ in this configuration can be found by equating the imaginary component of $Z_{L_M}(f)$ to be zero, i.e., $\mathrm{Im}[Z_{L_M}(f)] = 0$ and solving for $B_{M_X}(f)$. The required supply voltages and current drives can be found again by substituting $R_L = \{[1]/\mathrm{Re}[1/Z_{L_M}(f)]\}$ in (3) and (4). Note that in this analysis, we have assumed the TR to be lossless. When the TR has losses, this can be modeled as an extra shunt conductance in parallel to R_L, so effectively lowering its value.

Moreover, the transmission lines in the path of the main and peaking stages provide a frequency-dependent delay. This delay needs to be compensated by the adjustable phase shifter for perfect in-phase current-combining of main $[I_M \exp(-j\phi_M)]$ and peaking $[I_P \exp(-j\phi_P)]$ stage current vectors. The following frequency-dependent phase relationship can be derived using the circuit in Fig. 4, when accounting for the transmission line frequency-dependent phase delay

$$\phi_M - \phi_P = -\frac{\pi}{2}\frac{f}{f_0}. \tag{11}$$

Moreover, it can be summarized that the TR is used to present ohmic loads to the main and peaking stages at the center frequency of operation. At off-center frequency, TR is used to present an ohmic load for the main stage while the digitally adjustable phase shifter is used to (re)align the main and peaking stage's current summation in the OPCN [e.g., see Fig. 1(b)]. Using this technique, the lowest loss from a TR/TMN in practical circuit implementation can be achieved. For practical implementations, a lookup table (LUT) can be created that stores the required TR capacitance value, the relative phases between the main and peaking stages, and also their supply voltages with input drive profile for the expected range of load impedance's (Z_L) and operational frequency (f). The impedance sensor voltage ratios can provide the link to the load impedance and as such replace them. The details of the impedance sensor are explained in Section III. Furthermore, LUT can be adjusted to account for the parasitics in a practical implementation.

III. Wideband Impedance Sensor

Sensing the load accurately with minimal overhead is key to implementing the proposed wideband load-insensitive IDPA operation. This section introduces a wideband impedance sensor, which can be embedded in the OPCN of an IDPA. The complex varying load impedance ($Z_L = R_L + jX_L$) requires two independent equations to determine its real (R_L) and imaginary parts (X_L). The proposed impedance sensor (see Fig. 7) uses the orthogonality of the incident and reflected waves. Only four voltages need to be sensed using peak detectors and resistance-based voltage-combining networks (see Fig. 7). Equivalent capacitive or inductive voltage-combining networks can also replace the resistance-based networks. The organization of this section is as follows. First, we demonstrate the concept at the center frequency. Second, the proposed concept is extended to wideband operation by analyzing the sensor–voltage relations for a given operating frequency. As such, the theoretical peak detector voltage ratios for an applied load will be derived for both the center-frequency and wideband cases. To simplify the analysis, the following assumptions have been made.

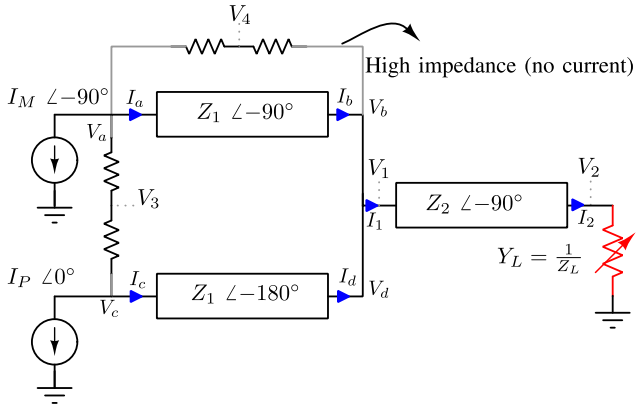

Fig. 7. Schematic of the wideband impedance sensor to analyze the dependence of voltage ratios $|V_1/V_2|$ and $|V_3/V_4|$ on Z_L and operating frequency.

1) The OPCN of an IDPA [43] is restricted to the three transmissions line configuration as shown in Fig. 7.
2) It is assumed that the peak stage is in its OFF-state, and as such, it does not provide any RF output current ($I_P = 0$).
3) The resistance-based combining network has a very high impedance, so any current flowing through it is ignored.

A. Center-Frequency Operation

$$\begin{bmatrix} V_x \\ I_x \end{bmatrix} = \begin{bmatrix} \cos(\beta l) & \mathrm{j}Z_{xy}\sin(\beta l) \\ \mathrm{j}(1/Z_{xy})\sin(\beta l) & \cos(\beta l) \end{bmatrix} \begin{bmatrix} V_y \\ I_y \end{bmatrix}. \tag{12}$$

For the center-frequency (0.9 GHz) operation, when only the main PA is active, using the schematic in Fig. 7 and the ABCD matrix for a lossless transmission line [42], (12) with $\beta l = \pi/2$, we can find the expression for the voltages V_1, V_2, V_3, and V_4. Taking the subsequent ratios of V_1/V_2 and V_3/V_4, the following equations are derived

$$\frac{V_1}{V_2} = -\mathrm{j}\frac{Z_L}{Z_2} \tag{13}$$

$$\frac{V_3}{V_4} = \frac{Z_L + \mathrm{j}Z_2^2/Z_1}{Z_L - \mathrm{j}Z_2^2/Z_1}. \tag{14}$$

Substituting ($Z_L = R_L + jX_L$) in (13) and (14) and taking the magnitude, we get

$$\left|\frac{V_1}{V_2}\right| = \frac{\sqrt{R_L^2 + X_L^2}}{Z_2} \tag{15}$$

$$\left|\frac{V_3}{V_4}\right| = \frac{\sqrt{R_L^2 + (X_L + Z_2^2/Z_1)^2}}{\sqrt{R_L^2 + (X_L - Z_2^2/Z_1)^2}}. \tag{16}$$

From (15) and (16), it can be observed that the ratio $|V_1/V_2|$ is sensitive to both R_L and X_L, i.e., $|\Gamma|$, whereas

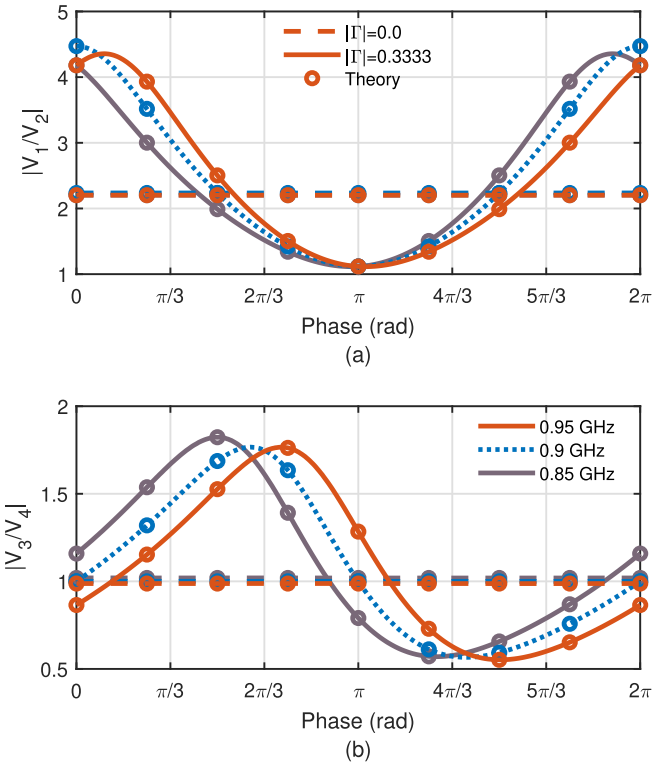

Fig. 8. Theoretical (circles) and simulated (solid and dotted lines) voltages' ratio at three operational frequencies 0.85, 0.9 (center frequency), and 0.95 GHz. (a) $|V_1/V_2|$ pointing to $|\Gamma|$ and (b) $|V_3/V_4|$ pointing to $\angle\Gamma$ for $|\Gamma|$ of 0.0 (dashed line) and 0.3333 (solid and dotted lines) as a function of the phase of Γ.

$|V_3/V_4|$ is only sensitive to X_L, i.e., $\angle\Gamma$. The $|V_3/V_4|$ ratio becomes unity when $X_L = 0$, for any value of R_L (due to the orthogonal relation between Z_L and jZ_2^2/Z_1). The theoretical and simulated (using the schematic in Fig. 7) magnitudes of these voltage ratios are plotted in Fig. 8 for $|\Gamma|$ set to {0.00, 0.33} with $\angle\Gamma$ swept from 0° to 360°, with the transmission lines impedance set to $Z_1 = 1/Y_1 = 20\ \Omega$ and $Z_2 = 1/Y_2 = (25Z_1)^{0.5}$. It can be seen that when the IDPA is matched to the load, i.e., 50 Ω ($|\Gamma| = 0$). The voltage ratios $|V_1/V_2|$ [see Fig. 8(a)] and $|V_3/V_4|$ [see Fig. 8(b)] are constant across all the phase angles. The voltage ratio $|V_1/V_2|$ settles at 2.24 while $|V_3/V_4|$ settles at 1.00. It can be observed from (13) and (14) that $|V_1/V_2|$ is dependent on transmission line impedance Z_2, while $|V_3/V_4|$ ratio is independent of the transmission line impedance since $Z_2 = (25Z_1)^{0.5}$. Using (13) and (14), it can be concluded that by only sensing the magnitude of these four voltages and taking their ratios ($|V_1/V_2|$, $|V_3/V_4|$), the magnitude and phase of the applied load reflection coefficient can be determined.

B. Wideband Operation

Also, in the wideband analysis, the OPCN transmission line model in Fig. 7 is used together with the transmission line ABCD matrix [42] (12). Furthermore, in this case βl is formulated as $0.5\pi(f/f_0)$ and $\pi(f/f_0)$ for transmission line lengths of $\lambda/4$ and $\lambda/2$, respectively. Consequently, we can determine the voltages V_1–V_4 and subsequently the voltage ratios of interest: V_1/V_2 and V_3/V_4 yielding

$$\frac{V_1}{V_2} = \frac{1}{\cos\left(\frac{\pi}{2}\frac{f}{f_0}\right) + jY_L Z_2 \sin\left(\frac{\pi}{2}\frac{f}{f_0}\right)}. \tag{17}$$

When $f = f_0$, i.e., at the center frequency of operation, (17) and (18), as shown at the bottom of the next page, can be reduced to (15) and (16), and therefore, as explained in Section III-A the voltage ratios ($|V_1/V_2|$ and $|V_3/V_4|$) point to $|\Gamma|$ and $\angle\Gamma$, respectively. The theoretical and simulated magnitudes of these voltage ratios ($|V_1/V_2|$ and $|V_3/V_4|$) at three operational frequencies 0.85 GHz, 0.9 GHz, and 0.95 GHz are shown in Fig. 8(a) and (b), for $|\Gamma|$ set to {0.00, 0.33} with $\angle\Gamma$ swept from 0° to 360°. It can be observed that the voltage ratio pattern at the off-center frequency closely resembles the voltage ratio pattern at the center frequency. Furthermore, it can be concluded that using (17) and (18), only sensing the magnitude of these four voltages and taking their ratios ($|V_1/V_2|$, $|V_3/V_4|$), and using the operation frequency (f/f_0) information along with the designed OPCN impedance $Z_1 = 1/Y_1$. The magnitude and phase of the applied load ($Z_L = 1/Y_L$) can be determined.

IV. Design Details

To demonstrate the concepts described in Sections II and III, a prototype IDPA with a digital control loop has been designed (see Fig. 9). The digital control loop algorithm is implemented in MATLAB. Fig. 9 shows the complete implementation schematic of the proposed wideband load-insensitive IDPA. It comprises the Doherty transistor output stages, the inverted Doherty power-combining network with a cointegrated orthogonal summation-based impedance sensor, and a parallel output resonator with a tunable capacitor. Rogers RO4350B with 0.508-mm thickness is chosen as the PCB substrate. The input power splitter with phase control, digitally controlled attenuators, and voltage-controllable dc–dc converters are implemented on external PCBs. In this work, based on the available technologies, we have optimized our design on the VSWR $\leq$ 2 range to avoid too severe performance tradeoffs (available quality factor and power handling of the TR, as well as the voltage/current headroom of the active devices in the output stages), facilitating the demonstration of a clear IDPA performance improvement over the targeted VSWR range.

A. Inverted Doherty PA

Commercial packaged laterally-diffused metal-oxide semiconductor (LDMOS) devices (AFIC901N [48]) are used to implement the main and peaking devices. This choice is made to respect later on the voltage/RF-power limitations of commercially available switch capacitor banks. The inputs of these devices are impedance matched to 50 Ω. The resulting Doherty configuration achieves an output power of 32 dBm from a 6.4-V supply and has an optimum load impedance ($R_{L_{opt}}$) close to 25 Ω. An additional $\lambda/4$ transmission line transfers this impedance level to 50 Ω. The output capacitance of the devices is resonated out using the dc-feed inductor.

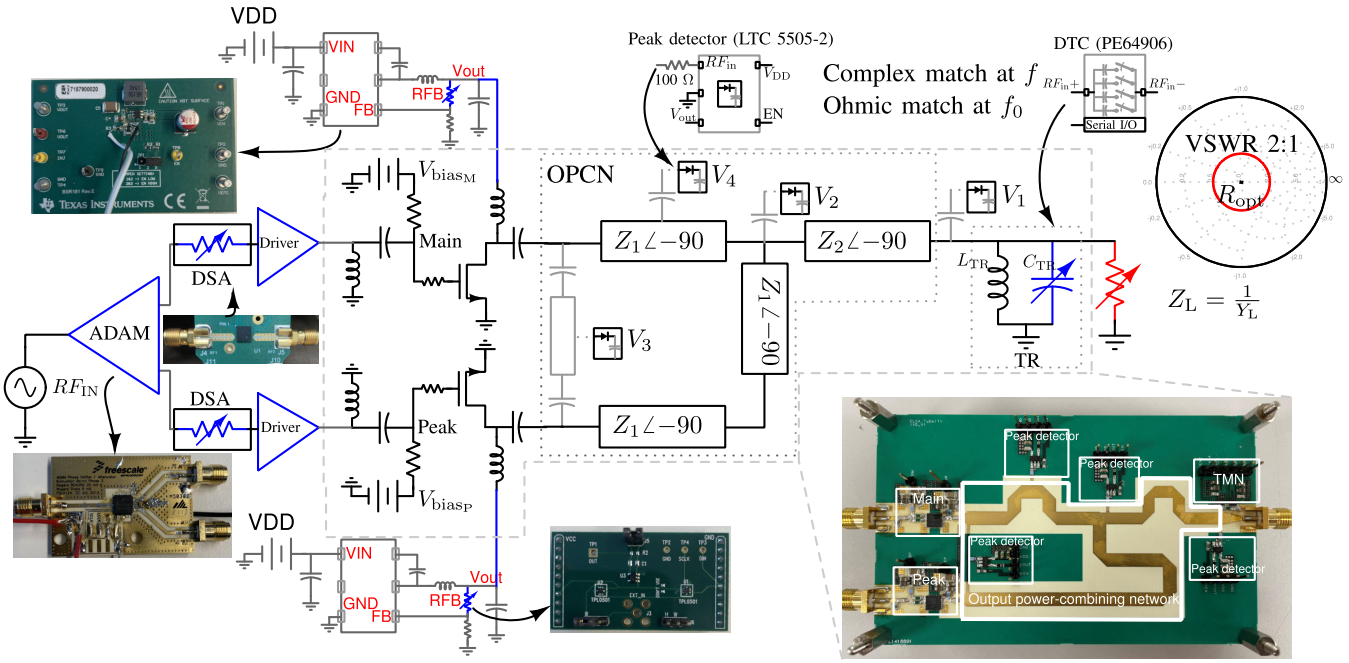

Fig. 9. Schematic of the proposed wideband load-insensitive inverted Doherty PA. The input signal splitter is implemented using ADAM ([44]). Fine-level control of the input signal is implemented through a DSA ([45]). The adjustable supplies are implemented as dc–dc buck converters [46], in which the feedback resistor that sets the supply voltage has been replaced by a digitally programmable potentiometer [47]. The voltage ratios ($|V_1/V_2|$ and $|V_3/V_4|$) are used to sense the presented load impedance to the PA. The TR/TMN cancels the complex part of the load at the fundamental.

B. Wideband Impedance Sensor

The impedance sensor voltages V_1, V_2, and V_4 are extracted using capacitive coupling at the indicated points of the 90° transmission lines (see Fig. 7 and 9). The sensing voltage V_3 is obtained by capacitive coupling of the main and peaking stage output nodes and combining them using a transmission line (see Fig. 9). The coupling capacitors are implemented using an interdigitated finger structure on the PCB, as shown in Fig. 9. They are sized to provide a coupling factor of −30 dB. The RF peak detectors for measuring the rms voltages are from analog devices, i.e., LTC5505-2. They provide a dynamic range of 40 dB [49].

C. Tunable Shunt Resonator

For a 2:1 VSWR circle, the maximum required capacitance of the parallel resonator to cover the operational band from 850–950 MHz in this design is 5.96 pF. Consequently, the required inductor (L_{TR}) value at 900 MHz is found to be 5.25 nH. The switched capacitor banks from pSemi were selected to implement the tunable capacitor. PE64906 [50] offers a $C_{min} = 0.8$ pF and $C_{max} = 5.4$ pF at 900 MHz with a step size of 119 fF (estimated from the datasheet plots [50]), yielding an effective capacitance tuning range of 4.6 pF. The maximum voltage and RF power for these components are 30 V and 34 dBm, respectively. Two of these banks are connected in parallel to cover the entire capacitance range of 5.96 pF. Furthermore, a 0603DC high-Q inductor from coil craft was selected to implement the resonant inductor (L_{TR}).

D. Input Splitter and Digital Step Attenuator

To achieve the required two independently controllable RF inputs for the main and peak stage in the proposed load-insensitive inverted Doherty PA, a wideband advanced Doherty alignment module (ADAM) [44] is used. It contains a 90° coupler, followed by a digitally selectable phase shifter in its output (7° LSB step with 49° maximum range), and step attenuators (0.5 dB LSB step with 7.5 dB maximum range). For finer amplitude control in steps of 0.25 dB, a digital step attenuator (DSA [45]) from pSemi is added directly after the ADAM module.

E. DC–DC Converter

TI dc–dc buck converters (LMR54410) [46] in combination with a digitally tunable feedback resistor (TPL0501) [47] were used to control the supply voltage of the IDPA branches statically. Note that these dc–dc converters can be relatively slow since they do not need to track the envelope of the modulated RF signal, allowing high-efficiency operation.

$$\frac{V_3}{V_4} = \frac{\frac{V_2}{V_1}\left[\cos\left(\frac{\pi}{2}\frac{f}{f_0}\right)+\cos\left(\pi\frac{f}{f_0}\right)\right]+\mathrm{j}Z_1\sin\left(\frac{\pi}{2}\frac{f}{f_0}\right)\left[\mathrm{j}Y_2\sin\left(\frac{\pi}{2}\frac{f}{f_0}\right)+Y_L\cos\left(\frac{\pi}{2}\frac{f}{f_0}\right)+\mathrm{j}Y_1\frac{V_2}{V_1}\tan\left(\pi\frac{f}{f_0}\right)\right]+\frac{V_2}{V_1}\tan\left(\pi\frac{f}{f_0}\right)\sin\left(\pi\frac{f}{f_0}\right)}{\frac{V_2}{V_1}\left[1+\cos\left(\frac{\pi}{2}\frac{f}{f_0}\right)\right]+\mathrm{j}Z_1\sin\left(\frac{\pi}{2}\frac{f}{f_0}\right)\left[\mathrm{j}Y_2\sin\left(\frac{\pi}{2}\frac{f}{f_0}\right)+Y_L\cos\left(\frac{\pi}{2}\frac{f}{f_0}\right)+\mathrm{j}Y_1\frac{V_2}{V_1}\tan\left(\pi\frac{f}{f_0}\right)\right]}. \quad (18)$$

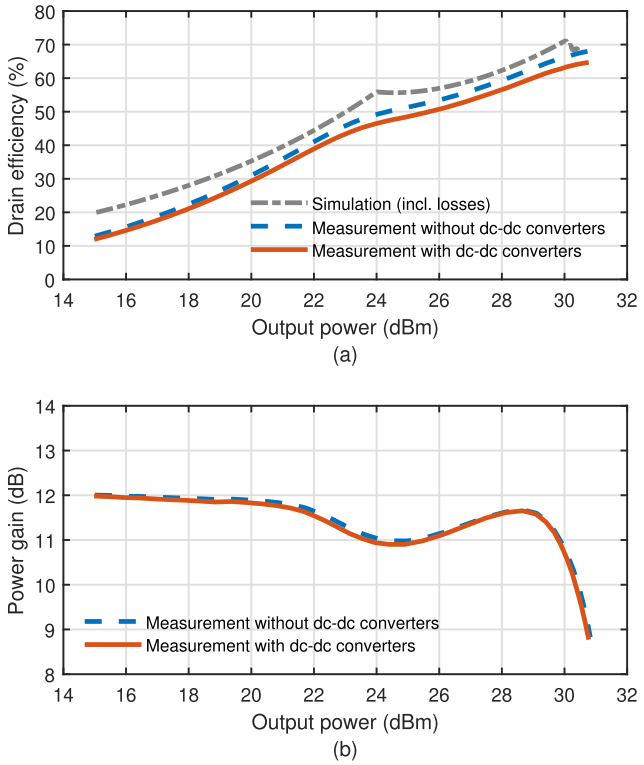

Fig. 10. Measured inverted Doherty results at the designed center frequency of 900 MHz versus output power (red color). (a) Drain efficiency and (b) power gain. Also, the measured and simulated (inclusive losses) efficiency performance of the IDPA without the dc–dc converter is included for reference.

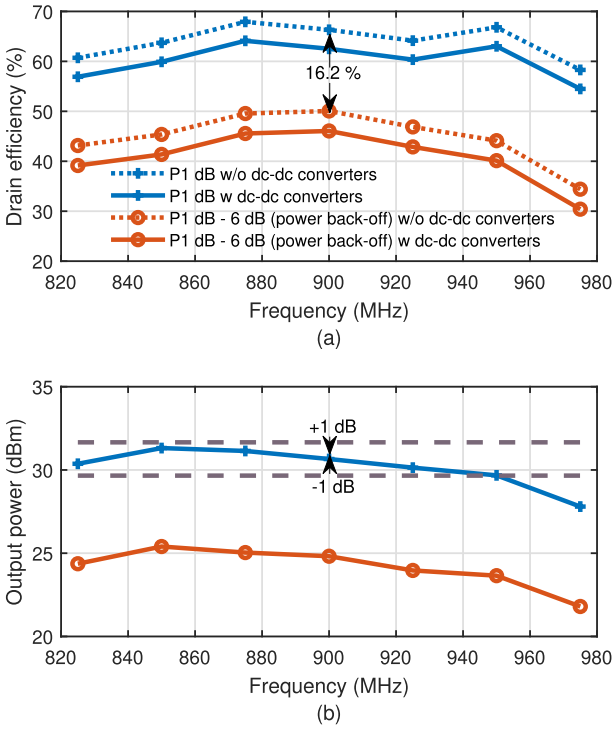

Fig. 11. Inverted Doherty performance versus frequency. (a) Drain efficiency with and without the dc–dc converters at 1-dB output power compression and 6-dB power back-off from the 1-dB output power compression. (b) 1- and 6 dB-back-off output power, also shown are the ±1-dB variation lines from 900-MHz center frequency.

V. Measurement

This section presents the measurement results of the implemented IDPA with an embedded wideband impedance sensing network.

A. Inverted Doherty PA

The main stage of the IDPA is biased in the class-AB mode with a quiescent current (I_{D_M}) of 28 mA. While the peaking stage is biased in the class-C mode with a quiescent current (I_{D_P}) of 0 mA. Both the stages use $V_{DD} = 6.4$ V in the $R_L = 50\ \Omega$ loading condition.

1) Center Frequency: The performance of the IDPA at its design frequency is shown in Fig. 10. It can be seen that the IDPA without the dc–dc converters has a power gain of 12 dB [see Fig. 10(b)] and delivers a peak output power of 30.95 dBm [see Fig. 10(a)] with a 68.1% drain efficiency when matched to its nominal 50-Ω load. At the center frequency, the drain efficiency at the 1-dB compression and 6-dB power back-off points is 66.5% and 50.3%, respectively (not including the impact of the dc–dc converters). The 16.2% efficiency degradation at 6-dB power back-off can be attributed to the output losses of the LDMOS output stage devices [51] and the shunt inductor used to resonate out their output capacitance, the losses from the embedded impedance sensor (≈0.075 dB) and the TR losses (≈0.44 dB). These losses can be represented by equivalent shunt resistances of, 150, 2870, and 468 Ω, respectively, at the output of the main LDMOS stage. This yields (including the impedance transformation of the OPCN) an effective parasitic shunt loading resistance of ≈120 Ω. The related analytical equations are given in Appendix. We have simulated the impact of these losses on the drain efficiency [see Fig. 10(a)], correlating well with the measured efficiency curve. However, when including the power dc–dc converters, the output power and drain efficiency are slightly reduced to 30.9 dBm and 63.7%, respectively. In this case, the dc–dc converters down-convert a 7.7-V supply to 6.4 V in the 50-Ω loading case. Note that all the further measurement results include the power consumption of the dc–dc converters.

2) Wide-Bandwidth Operation: The IDPA performance across frequency is shown in Fig. 11. The measurement results show that the fabricated IDPA has a 1-dB power bandwidth of 100 MHz around a 900-MHz center frequency [see Fig. 11(b)]. Translating to a fractional bandwidth of ≈11.1 %. This lower bandwidth, compared with the ≈22% in Section II, is caused by the inclusion of the output capacitance of the LDMOS devices and the added TR. At the 1-dB compression, the drain efficiency is more than 60% over the entire fractional bandwidth, while the 6-dB power back-off drain efficiency remains more than 40%. The measured IDPA drain efficiency and power gain over the fractional bandwidth (i.e., 850–950 MHz) are shown in Fig. 12(a) and (b), respectively.

B. Embedded Impedance sensor

1) Center Frequency: Fig. 13(a) and (b) shows comparison of the actual measurement and idealized simulation results of voltage ratios $|V_1/V_2|$ and $|V_3/V_4|$ of the proposed embedded

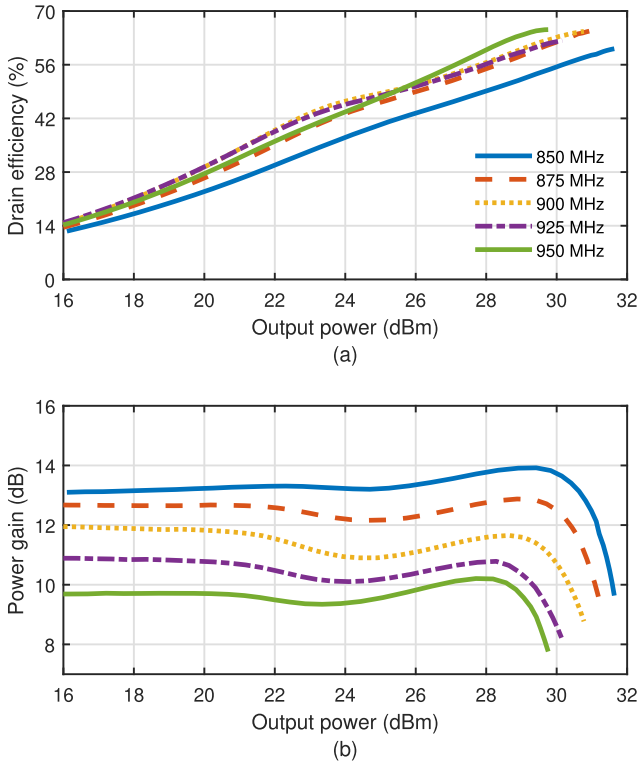

Fig. 12. Inverted Doherty PA 1-dB power bandwidth performance versus output power. (a) Drain efficiency and (b) power gain.

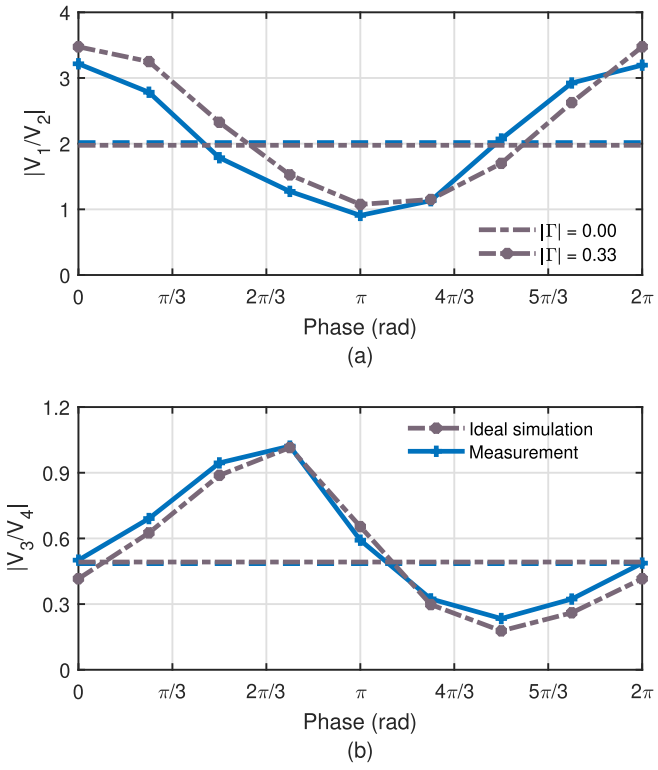

Fig. 13. Embedded impedance sensor idealized simulation and measurement results of the IDPA when operating at 900 MHz with 22-dBm output power. The voltage ratios versus phase ($\angle\Gamma$) (a) $|V_1/V_2|$ and (b) $|V_3/V_4|$.

impedance detector at 900 MHz. $|\Gamma|$ is set to 0.00 and 0.33, while the phase angles are swept from 0° to 360° in steps of 45°. The measurement results show excellent agreement

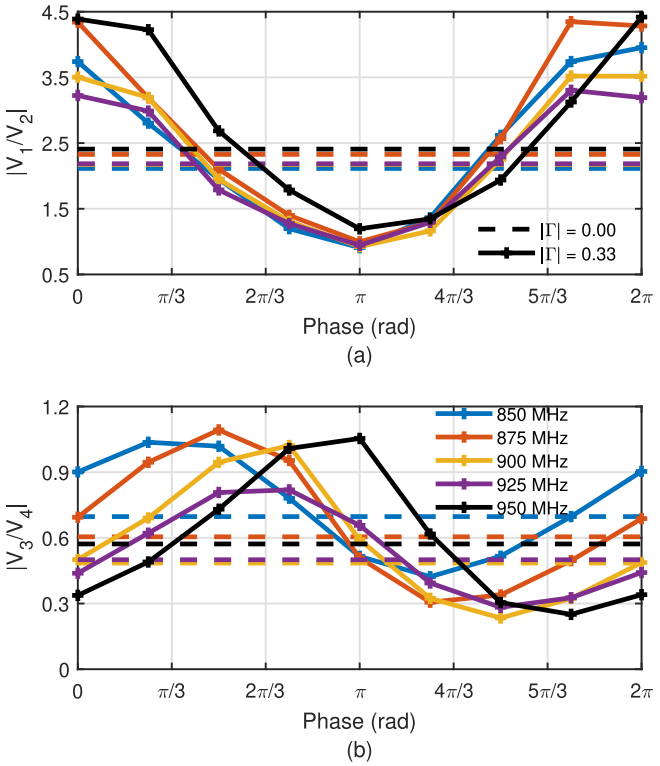

Fig. 14. Measurement results of the wideband embedded impedance sensor from 850–950 MHz. The voltage ratios versus phase ($\angle\Gamma$) (a) $|V_1/V_2|$ and (b) $|V_3/V_4|$.

with the idealized simulation results. The phase crossover points of the $|V_3/V_4|$ ratio is aligned with respect to the theory. However, there is a slight misalignment in the phase crossover points of the $|V_1/V_2|$ ratio at 90° and 270°. The deviations between the measurement and idealized simulated results can be traced back to gain variation in the peak detectors, component tolerances, and PCB parasitics.

2) Wide-Bandwidth Operation: Fig. 14(a) and (b) shows the measurement results of voltage ratios $|V_1/V_2|$ and $|V_3/V_4|$ of the proposed embedded impedance sensor from 850–950 MHz. $|\Gamma|$ is set to 0.00 and 0.33, while the phase angles are swept from 0° to 360° in steps of 45°. It can be observed that the voltage ratio pattern resembles the center frequency voltage ratio pattern (see Section III). Therefore, these voltage ratios can determine loading impedance across a wider bandwidth.

C. IDPA Performance Under 2:1 VSWR

To implement the proposed technique, an LUT-based control algorithm is implemented in MATLAB to restore the 50-Ω IDPA performance within specified ±0.2 dB tolerance in the output power. The LUT takes three (3) inputs $\{|V_1/V_2|, |V_3/V_4|, \text{and } f\}$ and provides seven control variables $\{V_{DD_M}, V_{DD_P}, \phi_M, \phi_P, \text{DSA}_M, \text{DSA}_P, \text{and } C_{TR}\}$ as output. These control variables act on the main and peaking stages, adjusting; supply voltages $\{V_{DD_M}, V_{DD_P}\}$, relative phases, $\{\phi_M, \phi_P\}$, input amplitudes $\{\text{DSA}_M, \text{DSA}_P\}$, and capacitance value (C_{TR}) of TR to present an ohmic impedance to the main stage. The initial values of the control variables $\{V_{DD_M}, V_{DD_P}, \phi_M, \phi_P, \text{DSA}_M, \text{DSA}_P, C_{TR}\}$ were generated using the equations as

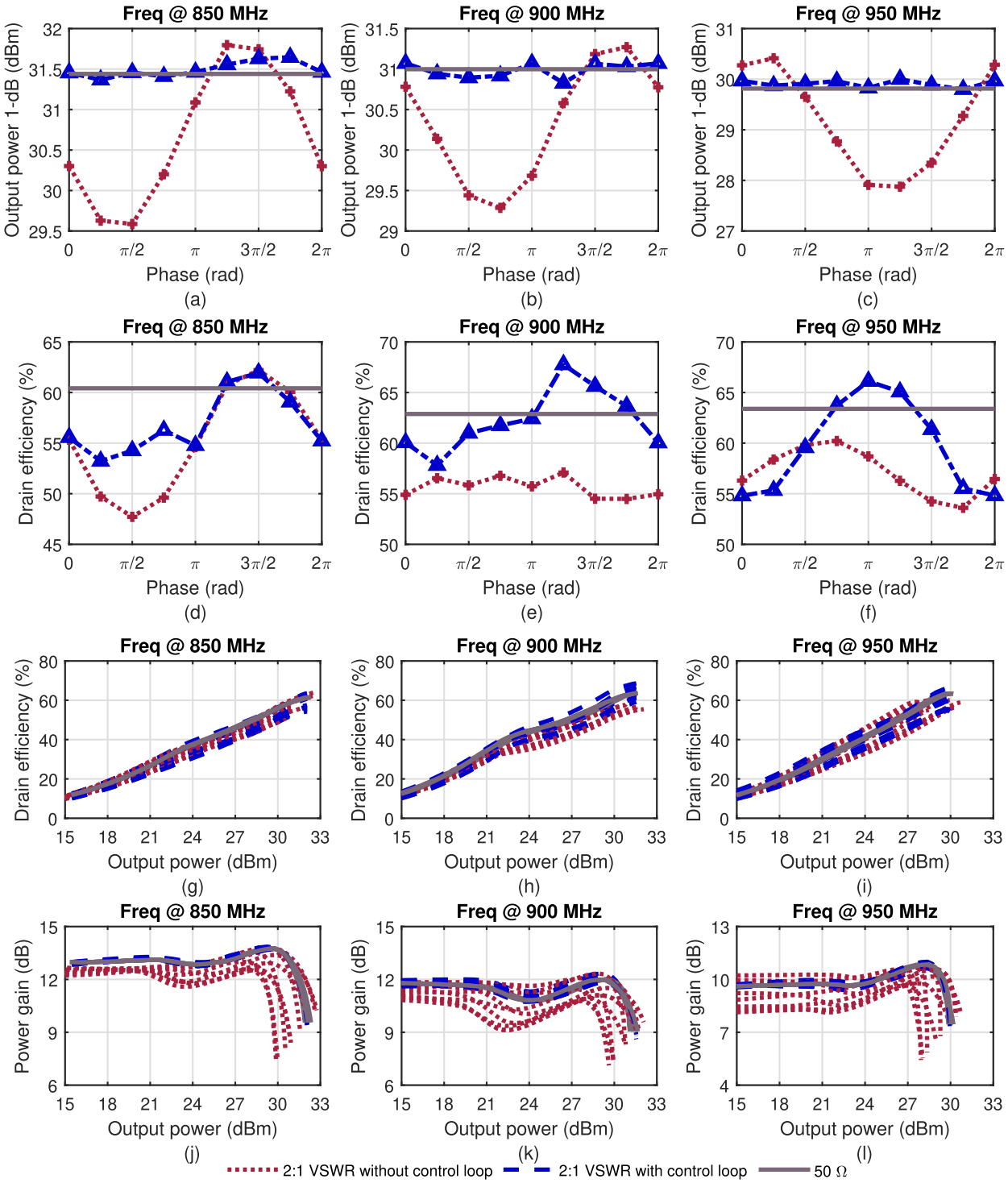

Fig. 15. IDPA performance at the operation frequencies 850, 900, and 950 MHz as such covering the entire fractional bandwidth of the PA. At these frequencies, the IDPA is subjected to the following loading conditions. First, 50 Ω; second, on a 2:1 VSWR circle with 45° phase steps without the control loop activated; and third, with the control loop active on a 2:1 VSWR with 45° phase steps. (a)–(c) IDPA output power versus phase ($\angle\Gamma$). (d)–(f) Drain efficiency for a given phase ($\angle\Gamma$). (g)–(i) Drain efficiency versus output power. (j)–(l) Power gain versus output power.

formulated in Section II for Fig. 1(b). Next, they were mapped to the input variables $\{|V_1/V_2|, |V_3/V_4|$, and $f\}$ using the equations as formulated in Section III for Fig. 7. Finally, these values were slightly adjusted to accommodate the impact of parasitics and PCB tolerances. The objective of the control loop algorithm for the single-tone operation is to maximize the drain efficiency while tracking the output power and power gain profile within the set tolerance limit. Whereas for the modulated signals, the objective of the control algorithm is to keep the average output power constant (i.e., within the tolerance bound) while improving the drain efficiency and linearity simultaneously.

1) Single-Tone: The IDPA performance at the operating frequencies 850, 900, and 950 MHz is presented in Fig. 15

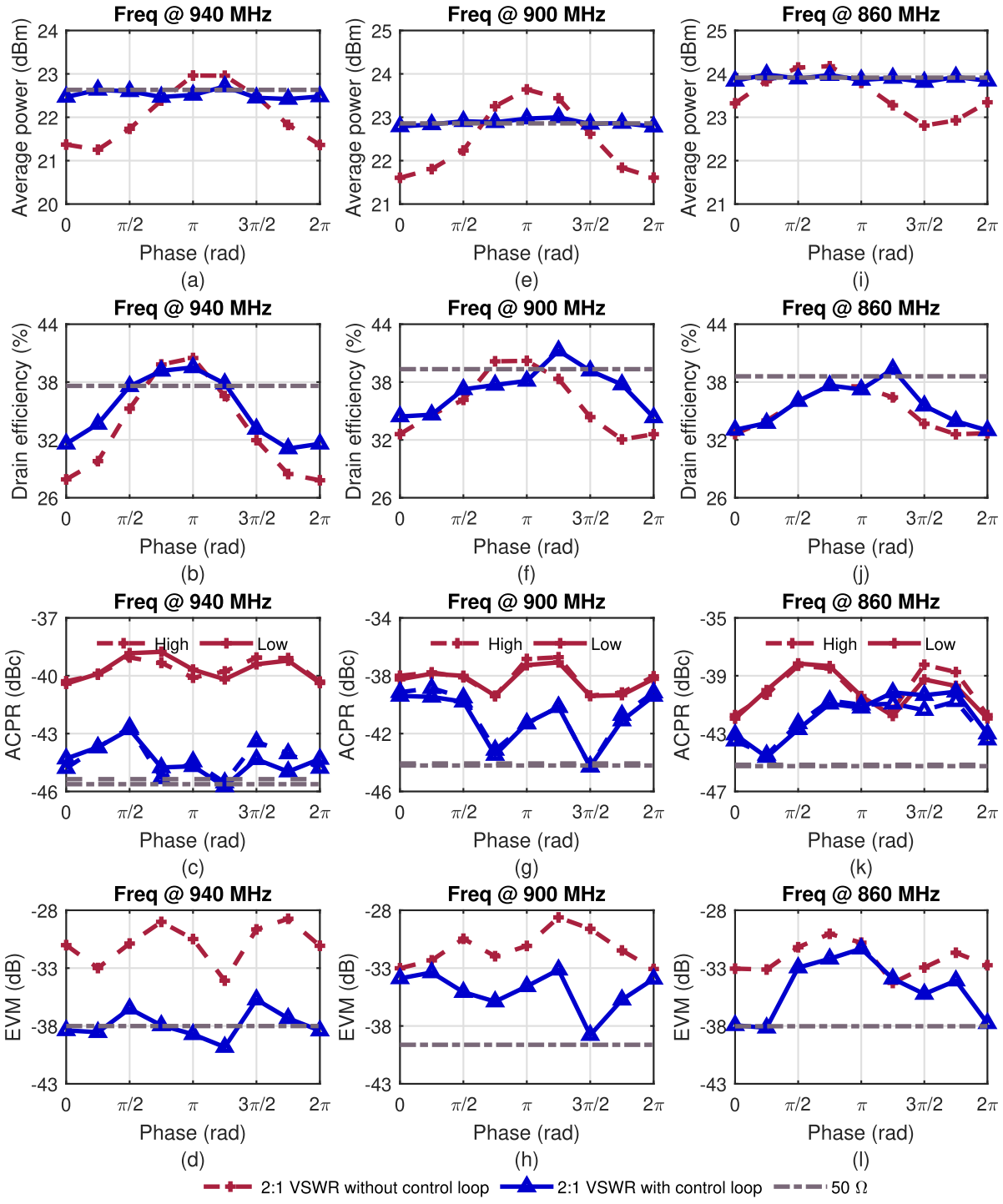

Fig. 16. IDPA performance when driven by a modulated signal (64-QAM 2 MHz) at the operating frequencies 940, 900, and 860 MHz as such covering the entire fractional bandwidth of the PA. At these frequencies, the IDPA is subjected to the following loading conditions. First, 50 Ω; second, on a 2:1 VSWR circle with 45° phase steps without the control loop activated; and third, with the control loop active on a 2:1 VSWR with 45° phase steps. (a)–(c) IDPA output power. (d)–(f) Drain efficiency. (g)–(i) Drain efficiency. (j)–(l) Power gain.

for the entire fractional bandwidth (≈11%) of the IDPA. Furthermore, the IDPA is subjected to three loading conditions, i.e., first, 50 Ω, second, on a 2:1 VSWR circle with 45° phase steps without the control loop, and third, with activated control loop on a 2:1 VSWR circle using 45° phase steps. The measurement results of these loading conditions are as follows: Fig. 15(a)–(c) shows the IDPA 1-dB compression output power versus loading phase angle ($\angle\Gamma$) at the frequencies 850, 900, and 950 MHz, respectively. Similarly, Fig. 15(d)–(f) shows the drain efficiency. Whereas Fig. 15(g)–(i) shows the drain efficiency versus output power at the frequencies 850, 900, and 950 MHz respectively. Similarly, Fig. 15(j)–(l) shows the power gain versus output power. From the above results, we can conclude that the proposed technique with the control loop meets the objective of maintaining constant output power within the tolerance band of ±0.2 dB while tracking the power

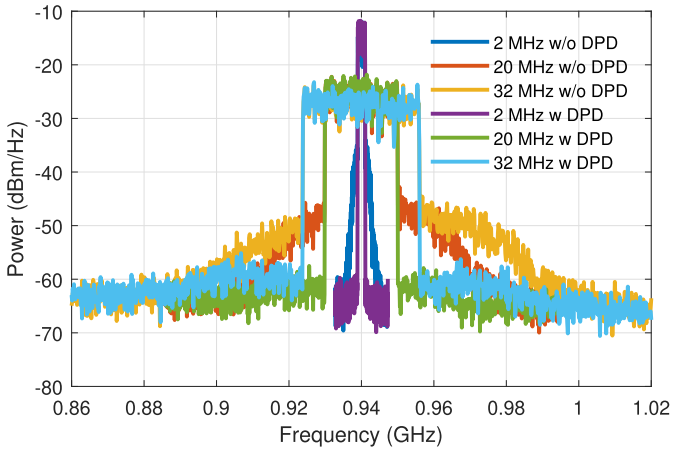

Fig. 17. Measured power spectral density on the 50-Ω load with and without the DPD from 2 to 32-MHz video bandwidth with the IDPA operating at 940-MHz carrier frequency.

gain profile of the IDPA across frequencies. Moreover, this objective is met while improving or at least maintaining the efficiency performance of the IDPA across different loading conditions.

2) Modulated Signal: The measured IDPA performance when driven by modulated signals at the operating frequencies 940, 900, and 860 MHz and for the load trajectory (45° phase steps) on the 2:1 VSWR circle, with and without the control loop activated, is shown in Fig. 16. Also provided is the performance of the IDPA when matched to a 50-Ω load for comparison. For these measurements, a 64-QAM 2 MHz modulated signal is used. First, a simple static AM-AM and AM-PM, an LUT-based DPD was performed for the IDPA when connected to a 50-Ω load. This resulted in a set of predistorted drive signals for the main and peaking devices, which remain unaltered in the following VSWR measurements. At 940-MHz operational frequency, the IDPA output power, drain efficiency, adjacent channel power ratio (ACPR), and error vector magnitude (EVM) are as shown in Fig. 16(a)–(d), respectively. It can be seen that the proposed method can track the 50-Ω loading performance of the IDPA on a 2:1 VSWR circle within a tolerance of ±0.2 dB, while simultaneously improving the drain efficiency and the linearity performance. Similarly, at 900 and 860 MHz with activated control loop, the nominal IDPA 50-Ω load performance can be approximated when operated on the 2:1 VSWR circle within a tolerance of ±0.2 dB while improving the drain efficiency, and linearity performance; see Fig. 16(e)–(h) and (i)–(l), respectively.

The IDPA is also tested with a 50-Ω trained predistorted modulated 64-QAM signals having higher video bandwidths, and the power spectral density with and without the DPD for 50-Ω matched load is shown in Fig. 17. The linearity improvement of the EVM and ACPR on the 2:1 VSWR circle in steps of 45° from 2–32-MHz video bandwidth for the IDPA operating at 940-MHz carrier frequency is also given in Fig. 18(a) and (b). In these experiments, the IDPA output power across bandwidth is kept constant within ±0.2 dB of its nominal 50-Ω performance. It can be observed that

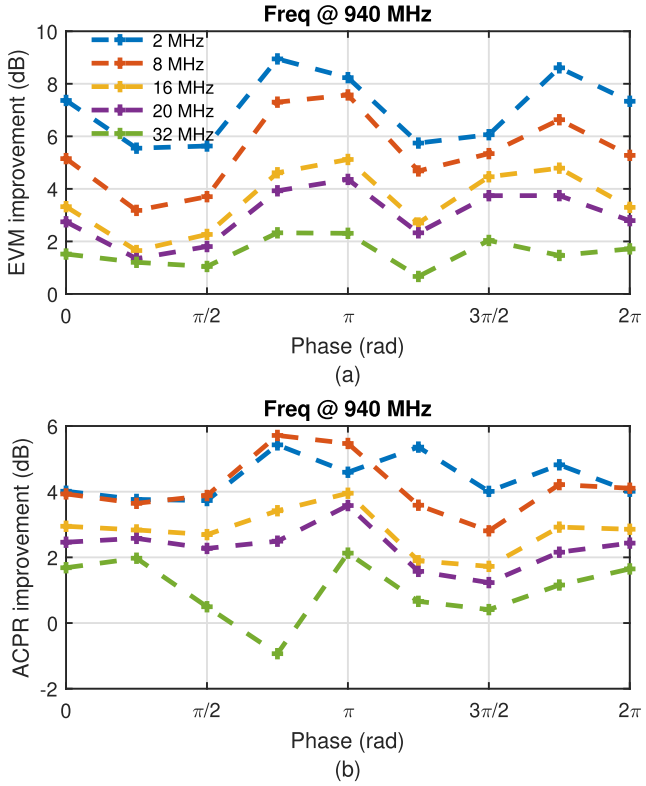

Fig. 18. Measured linearity improvement (a) EVM and (b) ACPR on the 2:1 VSWR circle with phase steps of 45° across 2–32-MHz video bandwidth with IDPA operating at 940-MHz carrier frequency (IDPA output power across bandwidth was kept constant within ±0.2-dB tolerance of 50-Ω nominal loading).

the proposed technique is effective even across wide video bandwidth signals.

From the measurement results, it can be concluded that when activated, the VSWR control loop can recover the IDPA performance in terms of output power and gain with a variation of less than ±0.2 dB across the entire fractional bandwidth of the IDPA. However, it suffers from decreased efficiency for some of the phase points. This degradation can be linked to two causes. First, the phase points where the active devices need to handle larger currents yield higher I^2R losses [21]. Second, the LDMOS device has a sizeable nonlinear output capacitance; changing the supply voltage yields a change in the output capacitance, causing reactive loads. Even though this can be adjusted in the TR, adding capacitance incurs extra losses. Moreover, for the cases where R_L is well above (>) 50 Ω, the insertion loss of the shunt resonator is higher, which also negatively impacts the efficiency [21].

Table I, provides a comparison with the state-of-the-art load-insensitive Doherty PAs. Switching between the Doherty-balanced [29] configuration is capable of providing higher output power when compared with the balanced-only configuration. However, this is achieved at the expense of degraded efficiency and EVM. Reconfigurable DPAs [25], [28] are much more resilient than the balanced configuration, yet the performance degradation is much higher when compared with their 50-Ω performance. Moreover, when compared with [22], which does not include the power consumption

TABLE I
COMPARISON WITH THE STATE-OF-THE-ART LOAD-INSENSITIVE DOHERTY PAS

Comparison	**This work**						[22] EUMC-2022		[28] TMTT-2021		[29] TMTT-2020		[25] TMTT-2015	
Technique	**Supply + TR/TMN**						Supply + TMN		QB-DPA ‡		Doherty-Balanced ‡		Re-configurable-DPA	
Freq (GHz)	**0.85-0.95**						0.9		3.5		3.5		3.6	
Fractional BW	**11 % (1 dB P_{out} variation)**						NR		NR		NR		NR	
Impedance Sensor	**Wideband & embedded**						Narrowband & external		No		No		No	
CW signal	**1-tone CW**						1-tone CW		1-tone CW		1-tone CW		1-tone CW	
Freq (GHz)	**0.85**		**0.9**		**0.95**		0.9		3.5		3.5		3.6	
Z_{L}	**50 Ω**	**2:1**	**50 Ω**	**2:1**	**50 Ω**	**2:1**	50 Ω	2:1	50 Ω	2:1	50 Ω	2:1	50 Ω	2:1
$P_{\text{out}_{1\text{dB}}}$ (dBm)	**31.5**	**31.5 ± 0.2**	**30.9**	**30.9 ± 0.2**	**29.9**	**29.9 ± 0.2**	32.3	32.3[0.4,-0.2]	40.7	38.8-40.4	41.9‡‡	NR	27.1‡‡	NR
DE (%)	**60.5**†	**53.3-62**†	**63.5**†	**57.8-67.2**†	**63.4**†	**55-66.1**†	61	48-59	68.4	51-59	70‡‡	NR	30.9‡‡	NR
Freq (GHz)	**0.94**						0.9		3.5		3.5		3.6	
Modulated signal	**64-QAM 2 MHz**		**64-QAM 20 MHz**		**64-QAM 32 MHz**		64-QAM 4 MHz		64-QAM 20 MHz		LTE 10 MHz		16-QAM 1 MHz	
DPD (static)	Yes						Yes		No		No		No	
PAPR	**7.3**						7.3		NR		8.4		5.4	
P_{out} (dBm)	**22.7**	**22.7 ± 0.2**	**22.7**	**22.7 ± 0.2**	**22.6**	**22.6 ± 0.2**	24.4	24.4 ± 0.1	35	33-34.2	34.5	32.5-35.1	21.9	20-20.8
DE_{avg} (%)	**37.6**†	**31.6-39.5**†	**37.7**†	**31.5-39.5**†	**37.3**†	**31.1-39.2**†	41	34-39	45	32.5-42.5	42.4	22-39	18.2	NR
P_{out} variation (dB)	**NA**	**± 0.2**	**NA**	**± 0.2**	**NA**	**± 0.2**	NA	± 0.1	NA	1.2	NA	2.6	NA	0.8
ACLR (dBc)	**-45.6**	**< -42.7**	**-36.2**	**< -34.4**	**-33.6**	**< -32.1**	-46.9	< -39.3	-41.0	NR	-37.0	NR	-35.3	< -30.3
EVM (dB)	**-38.0**	**<-35.8**	**-31.9**	**<-28.8**	**-28.6**	**<-25.2**	-40.9	< -32.3	-36.6	< -27.9	-32.5	<-26.0	-28.2	< -25.0

‡ results are estimated from plots; NR = Not reported; NA = Not applicable; † Including dc-dc converter's power consumption; ‡‡ saturated performance;

of dc–dc converters, the proposed technique works over a wider bandwidth, and furthermore, this work presents for the first time an embedded wideband impedance sensor, input amplitude, and phase adjustment for the main and peaking stages. The proposed technique achieves the best state-of-the-art performance in terms of constant linear output power with a variation of only ±0.2 dB, over the 2:1 VSWR circle across the fractional bandwidth of 11%. Furthermore, with a 50-Ω trained predistorted 64-QAM signals, the demonstrator meets the −33 dBc ACLR for the handset [19] on the 2:1 VSWR circle for upto 20-MHz video bandwidth while delivering the 50-Ω load power and improving efficiency.

VI. CONCLUSION

This article has demonstrated a wideband load-insensitive inverted Doherty PA with built-in wideband impedance sensing capability and controlling circuitry. The DPA is insensitive to load variation by tuning the input drive level and supply voltage of the main and peaking stages and adjusting its TR. As a result, it was shown, both in theory and experiments, that we can always recover the ideal Doherty operation for any load mismatch across the fractional bandwidth. The prototype DPA and LUT-based control algorithm recovered from all the load variations on a 2:1 VSWR circle. It could reduce the gain and output power variation to less than ±0.2 dB (driven by a complex modulated signal), when compared with the 50-Ω reference case, while improving the efficiency and linearity simultaneously. This allows using a simple LUT DPD, which can remain unaltered over the entire 2:1 VSWR circle. To the best of the author's knowledge, achieving all the functionalities within a single DPA design has not been reported before (see Table I), making the proposed load-insensitive IDPA with an embedded impedance sensor an interesting candidate for VSWR-tolerant mobile handset and beam steering base station applications.

APPENDIX

The impact of losses in the power-combining network originating from the active devices (R_{D}), tunable resonator (R_{TR}), and peak detectors (R_{PK}) on the back-off efficiency of the main PA can be derived using the following assumptions.

1) The knee effect ($R_{\text{on}} = 0$) of the device can be neglected.
2) The device output network can be modeled as lossy output admittance/impedance with compensated susceptance/reactance.
3) The losses of the distributed peak detectors can be combined into a single equivalent loss resistor (R_{PK}) in parallel to the load.

Using the schematic in Fig. 1(b), and incorporating the losses. The IDPA back-off efficiency expression assuming class-B operation for the main PA can be derived as follows:

$$\eta_{\text{M,back-off}} = \alpha\frac{\pi}{4} \tag{19}$$

in which α is

$$\alpha = [1]\Bigg/\left[1 + \frac{R_{\text{L}}}{R_{\text{TR}}} + \frac{R_{\text{L}}}{R_{\text{PK}}} + \frac{Z_1^2 R_{\text{L}}}{Z_2^2 R_{\text{D}_\text{M}}} + \frac{Z_1^2}{R_{\text{D}_\text{M}} R_{\text{D}_\text{P}}}\left(1 + \frac{R_{\text{L}}}{R_{\text{TR}}} + \frac{R_{\text{L}}}{R_{\text{PK}}}\right)\right] \tag{20}$$

and R_{D_M}, R_{D_P}, R_{TR}, and R_{PK} represent the equivalent losses originating from the main device, peak device, TR, and peak detectors, respectively.

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Gagan Deep Singh (Graduate Student Member, IEEE) was born in Wander Jatana, Punjab, India, in 1992. He received the B.E. degree in electronics and communication engineering from Visvesvaraya Technological University (VTU), Belgavi, Karnataka, India, in 2014, and the M.Tech. degree in RF and photonics from the Indian Institute of Technology (IIT) Guwahati, Guwahati, Assam, India, in 2018. He is currently pursuing the Ph.D. degree with the Delft University of Technology, Delft, The Netherlands.

He worked as a Software Engineer with L&T Infotech, Pune, Maharashtra, India, from 2014 to 2016, and as a Technologist at Tata Steel, Jamshedpur, Jharkhand, India, from 2018 to 2019. His research interests include analog and radio frequency (RF) integrated circuits, specializing in load-insensitive and switch-mode class-E power amplifiers.

Hossein Mashad Nemati received the B.Sc. degree in telecommunication engineering from the Amirkabir University of Technology, Tehran, Iran, in 2004, and the M.Sc. and Ph.D. degrees in microwave electronics from the Chalmers University of Technology, Gothenburg, Sweden, in 2006 and 2010, respectively.

He is currently a Senior Project Manager at Infineon Technologies AG, Munich, Germany. His research background and interest cover a wide range of applications within telecom and automotive industries, including transmitter circuits and architectures, digital predistortion, MIMO antenna systems, automotive radars, radar signal processing and tracking, multimodality sensor fusion algorithm, and perception system for autonomous driving applications.

Dr. Nemati was a recipient of the 2008 Outstanding Achievement Award and the 2010 First-Place Award of the Student High-Efficiency Power Amplifier Design Competition of the IEEE Microwave Theory and Techniques Society (IEEE MTT-S) International Microwave Symposium (IMS).

Morteza S. Alavi (Member, IEEE) received the B.S.E.E. degree from the Iran University of Science and Technology, Tehran, Iran, in 2003, the M.S.E.E. degree from the University of Tehran, Tehran, in 2006, and the Ph.D. degree in electrical engineering from the Delft University of Technology (TU-Delft), Delft, The Netherlands, in 2014.

He was a Co-Founder and the CEO at DitIQ B.V., Delft, a local company developing energy-efficient, wideband wireless transmitters for the next generation of the cellular network. Since September 2016, he has been with the Electronic Circuits and Architectures (ELCA) Research Group, TU-Delft, where he is currently a tenured Assistant Professor. He has coauthored *Radio Frequency Digital-to-Analog Converter* (Elsevier, 2016). His main research interests include designing high-frequency and high-speed wireless/cellular communication and sensor systems, as well as in the field of wireline transceivers.

Dr. Alavi was a recipient of the Best Paper Award at the 2011 IEEE International Symposium on Radio Frequency Integrated Technology (RFIT). He received the Best Student Paper Award (Second Place) at the 2013 Radio Frequency Integrated Circuits (RFIC) Symposium. His Ph.D. student also won the Best Student Paper Award (First Place) at the 2017 RFIC Symposium in Honolulu, HI, USA. His research group recently received the 2021 Institute of Semiconductor Engineers (ISE) President Best Paper Award of the International SoC Design Conference (ISOCC). One of his Ph.D. students also received the Platinum Award (first place) of the 2021 Huawei Student Design Content.

Leonardus Cornelis Nicolaas de Vreede (Senior Member, IEEE) received the Ph.D. degree (cum laude) from the Delft University of Technology, Delft, The Netherlands, in 1996.

In 1996, he was appointed as an assistant professor at the Delft University of Technology working on the nonlinear distortion behavior of active devices. In 1999 and 2015, he was appointed, respectively, Associate and a Full Professor at the Delft University of Technology, where he become responsible for the Electronic Research Laboratory (ERL/ELCA). During that period, he worked on solutions for improved linearity and RF performance at the device, circuit, and system levels. He is the Co-Founder/Advisor of Anteverta-mw, Eindhoven, The Netherlands, a company specialized in RF device characterization. He has (co)authored more than 120 IEEE-refereed conference and journal papers and holds several patents. His current interests include RF measurement systems, RF technology optimization, and (digital-intensive) energy-efficient/wideband circuit/system concepts for wireless applications.

Dr. de Vreede was a (co)recipient of the IEEE Microwave Prize in 2008, the Mentor of the Else Kooi Prize awarded for his Ph.D. work in 2010, and the Mentor of the Dow Energy Dissertation Prize Awarded for his Ph.D. work in 2011. He was a recipient of the TUD Entrepreneurial Scientist Award 2015. He has (co)guided several students that won (best) paper awards at the: IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM), Program for Research on Integrated Systems and Circuits (PRORISC), IEEE Symposium on Gallium Arsenide Integrated Circuit (GaAs IC), IEEE European Solid-State Device Research Conference (ESSDERC), IMS, RFIT, and RFIC.