

A Highly Selective Receiver With Programmable Zeros and Second-Order TIA

Montazerolghaem, Mohammad Ali; de Vreede, Leo C.N.; Babaie, Masoud

10.1109/JSSC.2023.3335921

Publication date

Document Version Final published version

Published in IEEE Journal of Solid-State Circuits

Citation (APA)

Montazerolghaem, M. A., de Vreede, L. C. N., & Babaie, M. (2023). A Highly Selective Receiver With Programmable Zeros and Second-Order TIA. *IEEE Journal of Solid-State Circuits*, *59*(6), 1668-1683. https://doi.org/10.1109/JSSC.2023.3335921

Important note

To cite this publication, please use the final published version (if applicable). Please check the document version above.

Other than for strictly personal use, it is not permitted to download, forward or distribute the text or part of it, without the consent of the author(s) and/or copyright holder(s), unless the work is under an open content license such as Creative Commons.

Takedown policy

Please contact us and provide details if you believe this document breaches copyrights. We will remove access to the work immediately and investigate your claim.

Green Open Access added to TU Delft Institutional Repository 'You share, we take care!' - Taverne project

https://www.openaccess.nl/en/you-share-we-take-care

Otherwise as indicated in the copyright section: the publisher is the copyright holder of this work and the author uses the Dutch legislation to make this work public.

A Highly Selective Receiver With Programmable Zeros and Second-Order TIA

Mohammad Ali Montazerolghaem[®], *Member, IEEE*, Leo C. N. de Vreede[®], *Senior Member, IEEE*, and Masoud Babaie[®], *Senior Member, IEEE*

Abstract—This article presents a wideband blocker tolerant receiver (RX) for fifth-generation (5G) user equipment applications. Two programmable zeros around the channel bandwidth are introduced to sufficiently suppress the close-in blockers of 5G applications. Since the effect of zeros gradually diminishes at larger out-of-band offset frequencies, an auxiliary currentsinking path is also introduced to reduce the RX input impedance at far-out offset frequencies. Moreover, a simple second-order transimpedance amplifier (TIA) is adopted to enhance the proposed RX selectivity. The utilized TIA synthesizes two complex conjugate poles to achieve a flat gain response and -40 dB/dec roll-off. A 40-nm CMOS RX prototype occupies 1.15 mm² and consumes 84-140 mW from a 1.3-V supply voltage over the 0.5-3-GHz operating frequency range. The RX achieves a 160-MHz RF bandwidth, 2.6-4.2-dB noise figure, a −0.3-dBm blocker 1-dB compression point (B1dB), and an out-of-band third-order intercept point (IIP3) of 22.5 dBm. As a test case, using the 3GPP standard, a -15-dBm continuous wave (CW) close-in out-of-band blocker located at 85-MHz offset from the passband edges is applied to the RX. Thanks to the receiver's high selectivity, the RX achieves 100% throughput while detecting 100-MS/s quadrature phase shift keying (QPSK) signal with 16 dB higher power than the reference sensitivity.

Index Terms—Current-mode receiver, fifth-generation (5G) user equipment applications, N-path filters, out-of-band linearity, programmable zeros, surface acoustic wave (SAW)-less receiver, second-order transimpedance amplifier (TIA).

I. INTRODUCTION

RECENTLY, the fifth generation (5G) of mobile communications has been introduced for sub-6-GHz and mmWave frequency bands. Although 5G new radios at mmWave bands can offer a higher maximum data rate, they suffer from high path loss, limiting their applications only to short-range communication. Hence, 5G sub-6-GHz radios gained more attention for long-range communication despite the congested sub-6-GHz spectrum. However, compared with the fourth-generation (4G) sub-6-GHz radios, the design of receivers (RXs) for 5G user equipment confronts new challenges. First, the RX's maximum RF bandwidth (BW_{RF}) is

Manuscript received 17 August 2023; revised 6 November 2023; accepted 16 November 2023. Date of publication 11 December 2023; date of current version 29 May 2024. This article was approved by Associate Editor Yunzhi Dong. This work was supported in part by the Nederlandse Organisatie voor Wetenschappelijk Onderzoek (NWO)/Ampleon Partnership Program under Project 16336 and in part by the Netherlands Organisation for Scientific Research under Project 17303. (Corresponding author: Mohammad Ali Montazerolghaem.)

The authors are with the Department of Microelectronics, Delft University of Technology, 2628 CD Delft, The Netherlands (e-mail: m.a. montazerolghaem-1@tudelft.nl).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/JSSC.2023.3335921.

Digital Object Identifier 10.1109/JSSC.2023.3335921

expanded from 20 to 100 MHz, increasing the design complexity of the baseband amplifiers. Second, despite increasing the BW_{RF}, the offset frequency (f_{OS}) of the close-in out-of-band blocker from the passband edge remains the same (i.e., at 85 MHz) due to the congested sub-6-GHz spectrum. Such a small f_{OS}/BW_{RF} (i.e., 0.85) requires sharp filtering to handle the -15-dBm continuous wave (CW) out-of-band blocker in a 5G time division duplex (TDD) test case. Finally, a sub-3-dB noise figure (NF) is desired to improve the signal-to-noise ratio (SNR) and adopt higher order modulation schemes to enhance the data rate and achieve the maximum communication range [1], [2].

Mixer-first RXs are popular for their far-out out-of-band linearity performance and simplicity, making them an appealing candidate for 5G user equipment applications. Usually, mixer-first RXs require large switches to achieve decent NF and linearity performance, and consequently, they suffer from high local oscillator (LO) leakage to the RX RF input. Moreover, most prior art mixer-first RXs [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14] only offer first-order filtering, making them prone to close-in blockers. Several attempts have been made to improve the selectivity of the mixer-first RXs [15], [16], [17], [18], [19]. For example, [15] and [16] introduced a positive feedback technique to achieve a second-order filtering response, and [17], [18], and [19] proposed a third-order TIA to improve further the selectivity of the mixer-first RXs. Although [15] achieves decent NF and linearity, its gain is low, requiring an analog-to-digital converter (ADC) with high dynamic range. To relax the ADC requirements, its gain needs to be increased; but in this case, its reported selectivity may not be enough to suppress the close-in blockers of the 5G applications. Moreover, [16], [17], [18], and [19] could not simultaneously achieve sharp filtering and sub-3-dB NF.

Alternatively, a low-noise transconductance amplifier (LNTA) can be placed before the passive mixers to achieve a lower NF in wideband RXs. However, the out-of-band blockers appear at the LNTA input without any attenuation, thus significantly degrading the RX linearity. Hence, different flavors of N-path filters [20], [21], [22], [23] have recently been used to enhance the selectivity and linearity of the LNTA-based RXs. In [24] and [25], an N-path filter is placed at the LNTA input to filter out the out-of-band blockers before entering the RX. However, since the RX input impedance at out-of-band offset frequencies is limited to the switches' on-resistance ($R_{\rm ON}$), large switches must be used to provide enough filtering for the large blockers, thus increasing the LO

0018-9200 © 2023 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See https://www.ieee.org/publications/rights/index.html for more information.

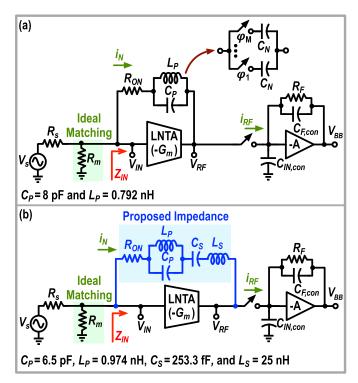


Fig. 1. (a) Conventional LNTA-based RX architecture with the equivalent model of the N-path notch filter in its feedback. (b) Proposed impedance in the feedback of the LNTA. Note that for simplicity, in these conceptual diagrams, an explicit shunt resistor, R_m , is used for the input matching.

buffers' dynamic power consumption and the LO leakage to the RX input port. Moreover, the large parasitic capacitance of the N-path filter switches at the RX input reduces the RX maximum operating frequency and bandwidth.

In order to alleviate those issues, as shown in Fig. 1(a), [26], [27], [28], [29], [30], [31], [32], [33], [34], [35], [36], [37], [38], and [39] placed an N-path notch filter in the LNTA's feedback to reduce the switches' sizes by benefiting from the Miller effect. Around the operating frequency, the N-path notch filter exploits high impedance, and the LNTA converts the input voltage to an RF current. Then, as the offset frequency deviates from the passband edges toward the outof-band frequencies, the N-path notch filter impedance drops with a -20-dB/dec slope to reach its final value, i.e., R_{ON} . Hence, at far-out offset frequencies, a feed-forward current flows from the input of the LNTA to its output through the N-path notch filter; and as shown in Fig. 2(a), if $G_m R_{ON} = 1$ $(G_m$ is the LNTA's transconductance), a null appears in the transfer function of the LNTA voltage gain (G_{LNTA}) [36]. Moreover, the Miller effect of the N-path notch filter is seen at the RX input, and thus, RF filtering is also achieved at the RX input transfer function (G_{IN}) , improving the RX out-ofband linearity performance [see Fig. 2(b)]. Interestingly, the RX input impedance is inversely proportional to G_m at outof-band offset frequencies, and increasing G_m improves the out-of-band linearity and NF simultaneously. However, as can be inferred from Fig. 2, due to the first-order filtering of the N-path notch filter, $G_{\rm IN}$ and $G_{\rm LNTA}$ reach their minimum values at very large offset frequencies, i.e., $f_{OS}/BW_{RF} \gg 0.85$. The amount of attenuation at low offset frequencies is limited at both LNTA input and output, making the RX prone to the

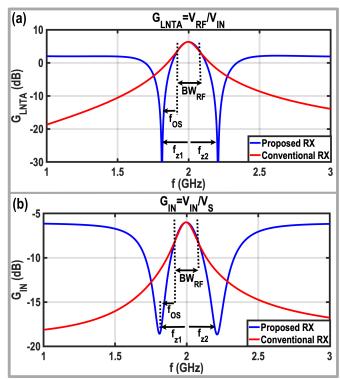


Fig. 2. Comparison between the simulated (a) G_{LNTA} and (b) G_{IN} of the conventional LNTA-based architecture and the proposed RX. Note that LNTA, mixers, and TIAs are implemented using ideal elements, and the notch filters are realized by RLC components with $R_{ON} = 7.7 \Omega$.

close-in blockers of 5G applications. A straightforward solution for this issue is significantly increasing the order of the N-path notch filter to achieve the required filtering. However, this comes at the cost of much higher power consumption and circuit complexity [18], [38]. Another way to improve the linearity performance of the LNTA-based RX is by adopting a quantized RF front end [40]. However, this technique requires performing complex calibration to improve the out-of-band linearity, and the operating frequency is limited due to the parasitic capacitors of the multiple low-noise amplifiers (LNAs) at the RX input. Hence, despite all the mentioned benefits of prior art structures, additional techniques are required to *efficiently* handle the close-in blockers and avoid RX desensitization.

To improve those limitations, we introduce two programmable zeros and an auxiliary current-sinking path in the LNTA feedback to suppress close-in and far-out blockers, respectively. Moreover, a second-order transimpedance amplifier (TIA) with complex-conjugate poles is also adopted to improve out-of-band linearity further and achieve a flat in-band gain response. This article is the extended version of [41], providing a more detailed analysis and explanation of the proposed RX. Moreover, to improve the linearity performance and selectivity of the RX, passive mixers and programmable zeros are trimmed in a respin prototype. This article is organized as follows: Sections II and III describe the evolution and implementation of the RX RF front end and second-order TIA, respectively. Section IV presents the RX circuit implementation. Section V elaborates on the RX noise analysis. The measurement results are shown in Section VI, and Section VII concludes this article.

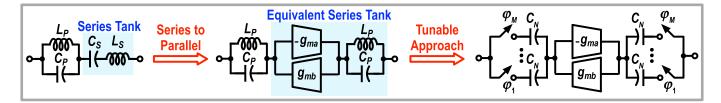


Fig. 3. Evolution of implementing the proposed impedance using two N-path notch filters and a gyrator.

II. EVOLUTION OF THE PROGRAMMABLE ZEROS

Although conventional LNTA-based RXs have nulls in $G_{\rm LNTA}$ at far-out offset frequencies, they do not provide enough attenuation for the close-in blockers. Note that these nulls appear at offset frequencies where the impedance of the notch filter approaches zero. Consequently, if one shifts the short impedance of the notch filter toward the frequencies of the close-in blockers, $G_{\rm IN}$ and $G_{\rm LNTA}$ will reach their minimum possible values at those frequencies, thus suppressing the close-in blockers sufficiently before entering the RX and baseband amplifiers. Hence, as depicted in Fig. 1(b), by adding a series tank (L_S and C_S) to the existing parallel tank (L_P and C_P), we introduce two zeros to the LNTA's feedback impedance. Note that the series and parallel tanks have the same resonant frequency, i.e., $f_{\rm LO} = \omega_{\rm LO}/(2\pi)$.

Due to the presence of the parallel tank, the proposed impedance shows high impedance inside the desired band. Consequently, as depicted in Fig. 2, the LNTA acts as a transconductance stage and no significant difference between the in-band responses of $G_{\rm IN}$ and $G_{\rm LNTA}$ of the conventional and proposed RXs is observed. However, as calculated in the Appendix, the proposed impedance offers two zeros around the operating band. The relative zeros frequencies from $f_{\rm LO}$ are given by

$$f_{z1,2} \approx \mp \frac{f_{\text{LO}}}{2} \sqrt{\frac{C_S}{C_P}}.$$
 (1)

Intuitively, for frequencies below f_{LO} , the parallel tank becomes inductive, and the series tank becomes capacitive; thus, their series combination creates a zero at a frequency close to but lower than f_{LO} (f_{z1}). Similarly, for frequencies above f_{LO} , a zero (f_{z2}) is realized since the parallel and series tanks become capacitive and inductive, respectively. As can be gathered from the simulation results in Fig. 2(a), the locations of G_{LNTA} nulls in the proposed RX are moved to the close vicinity of the operating band, thus greatly attenuating close-in blockers at the LNTA's output and avoiding RX desensitization. Moreover, at close-in blocker offset frequencies, the proposed RX offers around 5 dB better rejection at the RX input compared to the conventional RXs, as shown in Fig. 2(b). Beyond the zeros frequencies, the performance of the proposed RF front end degrades; its solution will be discussed in Section II-C.

A. Implementation of the Programmable Zeros

To achieve programmable zeros with wideband operation, the resonators must be replaced with tunable filters. To do

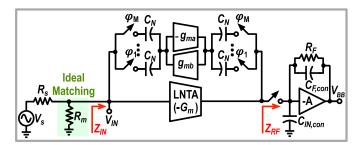


Fig. 4. Preliminary block diagram of the proposed RX, where the proposed programmable filter is placed in the LNTA's feedback.

so, as shown in Fig. 3, the series tank is firstly replaced with its counterpart, i.e., a parallel tank in series with a gyrator consisting of a feedforward (g_{ma}) and a feedback (g_{mb}) transconductance [42]. Here, we decided to have the same component values for both resulting parallel tanks to be convenient in the final implementation and achieve a symmetric schematic for the proposed filter. Considering the gyrator's impedance inversion characteristics, we have

$$C_S = g_{\text{ma}}g_{\text{mb}}L_P = \frac{g_{\text{ma}}g_{\text{mb}}}{C_P \ \omega_{\text{LO}}^2} \tag{2}$$

and

$$L_S = \frac{C_P}{g_{\text{ma}}g_{\text{mb}}}. (3)$$

By substituting the equivalent value of C_S from (2) into (1), the zeros frequencies in this implantation may be approximated by

$$f_{z1,2} = \mp \frac{1}{4\pi C_P} \sqrt{g_{\text{ma}} g_{\text{mb}}}.$$
 (4)

Interestingly, the zeros frequencies can be tuned by $g_{\text{ma}}g_{\text{mb}}$ and C_P . Finally, to obtain a programmable network, each parallel tank is easily replaced with an N-path notch filter, as shown in Fig. 3. The unit capacitor of each N-path notch filter, C_N , can be estimated by

$$C_N = \frac{2}{M} \operatorname{sinc}^2 \left(\frac{1}{M}\right) \times C_P \tag{5}$$

where M is the number of LO phases in the N-path notch filter [43].

B. RX Bandwidth and Input Impedance at Zeros Frequencies

Fig. 4 shows the RX preliminary schematic, where the proposed programmable filter is placed in the LNTA's feedback. The RX input impedance can be approximated by

$$Z_{\rm IN}(\omega) \approx \frac{1 + g_{\rm ma}g_{\rm mb}Z_N(Z_N + Z_{\rm RF})}{g_{\rm ma}(Z_N + Z_{\rm RF}) + G_m Z_{\rm RF}} \times \frac{1}{g_{\rm mb}}$$
 (6)

where Z_{RF} is the load impedance of the LNTA seen from the RF port of passive mixers, and Z_N is the equivalent impedance of the identical N-path notch filters, given by

$$Z_N = R_{\rm ON} + \frac{j\omega L_P}{1 - \omega^2 L_P C_P}. (7)$$

In current-mode RXs, Z_{RF} is designed to be low enough in order to sink the RF current of the LNTA. Consequently, by considering $Z_N \gg Z_{RF}$ and assuming $g_{\rm ma}g_{\rm mb}Z_N^2 \gg 1$, $Z_{\rm IN}$ around the zeros frequencies can be approximated by

$$Z_{\rm IN}(\omega \approx \omega_{z1,2}) \approx R_{\rm ON} + \frac{j}{\sqrt{g_{\rm ma}g_{\rm mb}}}.$$
 (8)

As can be gathered from (4) and (8), enhancing $g_{\text{ma}}g_{\text{mb}}$ increases the zeros frequencies, and at the same time, reduces the RX input impedance around the implemented zeros.

As the next step, the RX 3-dB bandwidth is estimated using the input transfer function of the RX

$$G_{\rm IN} = \frac{1}{2} \times \frac{Z_{\rm IN}}{Z_{\rm IN} + \frac{R_s}{2}}.$$
 (9)

Assuming $Z_N \gg Z_{\rm RF}$ around the operating frequency, the 3-dB bandwidth can be calculated by setting $|G_{\rm IN}(f_{\rm LO}) \pm f_{\rm 3dB})| = |G_{\rm IN}(f_{\rm LO})|/\sqrt{2}$

$$f_{3dB} = \frac{2}{2\pi C_P R_S \times \left(1 + \sqrt{1 + \frac{16}{g_{\text{mag}} g_{\text{mb}} R_S^2}}\right)}.$$
 (10)

Here, f_{3dB} is BW_{RF}/2. Interestingly, increasing $g_{ma}g_{mb}$ enhances the 3-dB bandwidth, and a larger C_P is required to keep the desired bandwidth constant.

C. Improving Far-Out Out-of-Band Linearity

Unfortunately, the proposed impedance becomes an open circuit at the far-out out-of-band frequencies, and the RF filtering at the RX input diminishes at those offset frequencies, as can be gathered from Fig. 2. Hence, far-out blockers create a high voltage swing at the RX input, deteriorating the RX linearity performance. To resolve this issue, as shown in Fig. 5(a), an auxiliary N-path notch filter is added from the antenna to the output port of the gyrator. Its bandwidth is intentionally chosen $2 \times$ larger than that of the main notch filter such that this extra path acts as an open circuit for the desired band and the close-in blockers, thus keeping the RX response at those frequencies intact. At far-out offset frequencies, all N-path notch filters exhibit low impedance, and the auxiliary N-path notch filter shorts the input of the gyrator to its output. Therefore, the gyrator's impedance inversion operation vanishes, and the effect of zeros in $G_{\rm IN}$ and $G_{\rm LNTA}$ is diminished. At far-out frequencies, as shown in Fig. 5(b), the RX front end is simplified to three transconductances $(-G_m, -g_{ma}, \text{ and } g_{mb})$ with low-ohmic resistive shunt feedback, thus approximately reducing the RX input resistance to $1/(G_m + g_{ma} - g_{mb})$.

D. Design Guide for the RX RF Front End

In this section, we develop a design guide for estimating the components of the RX RF front end (i.e., G_m , g_{ma} , g_{mb} , and C_N) to satisfy the 5G user equipment specifications,

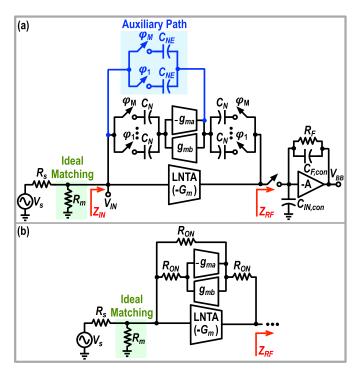


Fig. 5. (a) Block diagram of the RX front end. An auxiliary N-path filter is added to reduce the RX input impedance at far-out frequencies; (b) The equivalent model of the proposed RX architecture at far-out offset frequencies.

i.e., the desired bandwidth and required blocker input 1-dB compression point (B1dB). In this analysis, without loss of generality, the loss of the N-path notch filters is neglected, and the input matching is accomplished by a shunt resistor at the RX input (see Fig. 5).

The first step is to estimate the values of $g_{\rm ma}$, $g_{\rm mb}$, and C_N based on the 3-dB bandwidth and the location of the zeros set by the 3GPP standard. Here, we define a parameter, χ , for relating the zeros frequencies to the 3-dB bandwidth

$$\chi = \mp \frac{f_{z1,2}}{f_{3dB}}.$$
 (11)

Equivalently, (11) leads to $f_{OS} = (\chi - 1) f_{3dB}$. Note that χ is always larger than one since the frequencies of the zeros must lie outside the RX 3-dB bandwidth. By assuming $f_{LO} \gg \chi f_{3dB}$, and substituting (11) into (4), the 3-dB bandwidth of the RX can be approximated as

$$f_{3\text{dB}} = \frac{\sqrt{g_{\text{ma}}g_{\text{mb}}}}{4\pi \chi C_P}.$$
 (12)

The RX 3-dB bandwidth can be calculated using (12) and (10). Therefore, by equating (10) and (12), we have

$$\sqrt{g_{\text{ma}}g_{\text{mb}}} = \frac{2(\chi^2 - 1)}{\chi R_S}.$$
 (13)

Choosing χ fixes the value of $\sqrt{g_{\rm ma}g_{\rm mb}}$, and accordingly, via (8), the RX input impedance at zeros' frequencies. Moreover, increasing the zeros' frequency offset from the passband edges (i.e., larger χ) leads to larger $g_{\rm ma}g_{\rm mb}$, and thus, higher power consumption in the gyrator.

Based on the 3GPP standard, the location of the close-in blocker is 85 MHz from the 3-dB bandwidth edge, and BW_{RF}

is 100 MHz. However, in this work, we target BW_{RF} = 200 MHz, resulting in $\chi = 185/100 = 1.85$. Despite that, we choose $\chi = 1.5$ to place zeros closer to passband edges, thus reducing power consumption. This results in $\sqrt{g_{\rm ma}g_{\rm mb}} = 33.3$ mS, and $Z_{\rm IN}(\omega_{z1,2}) = 30~\Omega$. Moreover, to guarantee the gyrator's stability, one should set $g_{\rm ma} \geq 4 \times g_{\rm mb}$, leading to $g_{\rm ma} = 72$ mS and $g_{\rm mb} = 16$ mS.

On the other hand, by substituting $\sqrt{g_{\text{ma}}g_{\text{mb}}}$ from (13) into (10), C_P can be estimated by

$$C_{P} = \frac{2}{2\pi f_{3dB} R_{S} \times \left(1 + \sqrt{1 + \left(\frac{2\chi}{\chi^{2} - 1}\right)^{2}}\right)}.$$
 (14)

Accordingly, C_N is determined using (5) and (14). Considering $f_{3\text{dB}} = 100 \, \text{MHz}$, C_P and C_N are approximated to be 17.7 and 4.2 pF, respectively. Since the auxiliary N-path notch filter should have more bandwidth than the main notch filter, the auxiliary path unit capacitor, C_{NE} , is chosen $\approx 2 \times \text{smaller}$ than C_N .

The design guide finishes with G_m estimation. At far-out frequencies, the LNTA's input voltage can be calculated by

$$V_{\rm IN} = \frac{V_{s,B}}{1 + (G_m + g_{\rm ma} - g_{\rm mb})R_s}$$
(15)

where $V_{s,B}$ is the maximum blocker voltage, approximated by $\sqrt{8R_s \times 10^{B\,1d\,B/10}}$. In order to tolerate the blocker, the RX input voltage must be below the LNTA's input 1-dB compression voltage ($V_{\rm Blk}$). Consequently

$$G_m \ge \frac{1}{R_s} \left(\frac{\sqrt{8R_s \times 10^{\frac{B1dB}{10}}}}{V_{\text{Blk}}} - 1 \right) + g_{\text{mb}} - g_{\text{ma}}.$$
 (16)

Based on the 3GPP standard, the required B1dB is -15 dBm; however, we target 0-dBm B1dB at far-out offset frequencies. Considering a simulated $V_{\rm Blk}$ of 0.14 V, G_m should be larger than 16 mS to tolerate the aimed blocker power. However, the calculated G_m based on the linearity spec does not satisfy the NF requirement [see (38) in Section V], and we choose $G_m = 130$ mS to achieve sub-3 dB NF.

Fig. 6 illustrates the simulation results of the proposed structure in Cadence. In this simulation, the calculated components' values from the design guide are used. The simulated BW_{RF} is around 170 MHz, and the location of the zeros is 70 MHz from the passband edges, indicating that the presented design guide provides a sufficiently accurate initial estimation for the circuit parameters of the proposed RX RF front end. As can be gathered from the simulated results in Figs. 2 and 6, although the depth of $G_{\rm IN}$ nulls is almost maintained, the amount of G_{LNTA} rejection at the zero frequencies is reduced in the active realization of the proposed feedback network compared to its passive implementation. Due to the active implementation of the series inductor, the feed-forward current does not flow from the LNTA input to its output, thus lowering the nulls' depth. Consequently, the active implementation of the feedback network brings programmability for the null locations and operating RX frequency but at the cost of a lower G_{LNTA} rejection at zeros' frequencies.

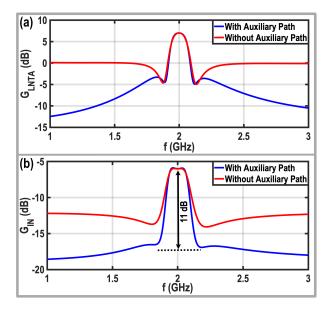


Fig. 6. Circuit level simulation results of (a) $G_{\rm LNTA}$ and (b) $G_{\rm IN}$ for the proposed structure shown in Fig. 5, using the components' values calculated in the design guide.

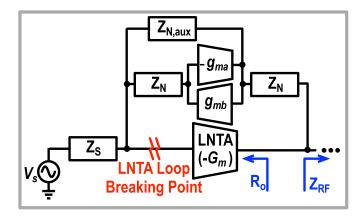


Fig. 7. The simplified model of the RX front end for the stability analysis.

E. Loop Stability of the RX RF Front End

To ensure that the proposed feedback impedance does not sacrifice the RX stability, this section investigates the loop gain (LG) of the RX front end at in-band and out-of-band frequencies by using the simplified model in Fig. 7 and breaking the loop at the LNTA's input. Since the bandwidth of the auxiliary path is higher than that of the main N-path notch filters, the LG at in-band and close-in out-of-band frequencies can be approximated by

$$LG_{IB} = G_m(Z_{RF} \parallel R_o) \times \frac{Z_S}{Z_S + Z_N}$$
$$\times \frac{g_{mb}(Z_N + Z_S)}{1 + g_{ma}g_{mb}Z_N(Z_N + Z_S)}$$
(17)

where R_o is the LNTA's output resistance, and Z_S is the antenna impedance with an ideal value of 50 Ω . Since $Z_S \ll Z_N$ and $Z_{RF} \ll R_o$ at in-band and close-in out-of-band frequencies, (17) can be simplified to

$$LG_{IB} = \frac{G_m}{g_{ma}} \times \frac{Z_S}{Z_N} \times \frac{Z_{RF}}{Z_N}.$$
 (18)

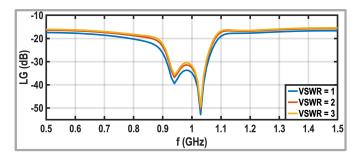


Fig. 8. Simulated LG of the RX front end for different VSWR values.

Since both Z_S and Z_{RF} are much smaller than Z_N , LG_{IB} is much smaller than 1 around the operating frequency, ensuring the stability of the RX front end. Interestingly, enhancing g_{ma} improves the stability and reduces the RX input impedance around the implemented zeros but pushes zeros frequencies toward higher out-of-band frequencies. However, at out-of-band frequencies, the value of Z_N reduces, increasing the LG of the LNTA feedback network.

At far-out offset frequencies, the auxiliary N-path notch filter exhibits low impedance and eradicates the gyrator effect on the receiver operation. Therefore, the LG at far-out out-ofband frequencies can be estimated by

$$LG_{OOB} = G_m Z_{RF} \times \frac{Z_S}{Z_S + Z_{RF} + Z_N + Z_{N,aux}}.$$
 (19)

Since $Z_S > Z_N + Z_{N,aux} + Z_{RF}$ at far-out out-of-band frequencies, (19) can be simplified to

$$LG_{OOB} = G_m Z_{RF}.$$
 (20)

Hence, the combination of mixers' on-resistance and TIAs' input impedance must stay low enough at far-out out-of-band frequencies to guarantee the RX front-end stability.

The loop stability of the proposed RF front end is simulated in Cadence using "pstb." Fig. 8 illustrates the simulated LG for three different voltage standing wave ratios (VSWRs). To consider the worst case, the LG is simulated when the angle of the reflection coefficient is zeros ($\theta=0$), and hence, the antenna impedance is 100 and 150 Ω for VSWR = 2 and 3, respectively. For all the VSWRs, LG is below 0 dB with enough margin, confirming the RX front-end stability.

III. SECOND-ORDER TIA

The conventional TIA, shown in Fig. 5, offers a first-order filtering roll-off. However, since the RF front end merely offers 11-dB rejection at the RX input for close-in blockers, they may still create a large voltage swing at the conventional TIA output, and desensitize the RX line-up, especially when a large TIA feedback resistance (R_F) is required to reduce the NF contribution of the subsequent stages. Consequently, a second-order TIA is desired to handle the close-in blockers of 5G applications. Unlike the conventional TIA, the second-order TIA also has complex conjugate poles and features a flat in-band gain response.

Here, as depicted in Fig. 9(a), we remove C_F from the conventional TIA feedback and replace it with a load capacitor (C_L) at the TIA output to achieve second-order filtering. R_F

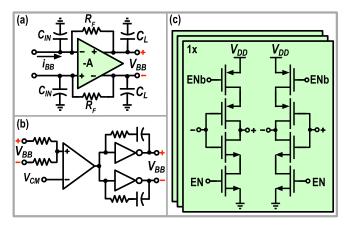


Fig. 9. Schematics of (a) second-order TIA, (b) its CMFB circuit, and (c) utilized TIA amplifier.

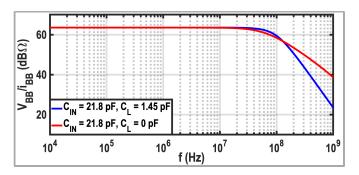


Fig. 10. Simulated TIA transfer function with/without C_L .

remains in the feedback of the TIA to convert down-converted current to a baseband voltage. The transfer function of the TIA can be derived as

$$\frac{V_{\rm BB}}{i_{\rm BB}} \approx \frac{-R_F}{s^2 C_{\rm IN} C_L \frac{R_F}{g_{\rm mt}} + s \left(\frac{C_{\rm IN}}{g_{\rm mt}} + \frac{C_L}{g_{\rm mt}} + \frac{C_{\rm IN}}{g_{\rm mt}} \frac{R_F}{r_{\rm ot}}\right) + 1}$$
(21)

where $V_{\rm BB}$ and $i_{\rm BB}$ are the TIA's output voltage and input current, respectively [see Fig. 9(a)]. Moreover, $g_{\rm mt}$ and $r_{\rm ot}$ are the transconductance and output resistance of the TIA amplifier. As can be inferred from (21), the transfer function of the TIA is a second-order low-pass filter with a damping ratio (ζ) and natural frequency (ω_n) of

$$\zeta = \frac{1}{2} \frac{1}{\sqrt{g_{\text{mt}} R_F}} \times \left(\sqrt{\frac{C_{\text{IN}}}{C_L}} \left(1 + \frac{R_F}{r_{\text{ot}}} \right) + \sqrt{\frac{C_L}{C_{\text{IN}}}} \right)$$
(22)

$$\omega_n = \sqrt{\frac{g_{\rm mt}}{C_{\rm IN}R_FC_L}}. (23)$$

Usually, ζ is set to $\sqrt{2}/2$ to achieve a Butterworth low-pass filter and reach the maximum bandwidth. In this way, the 3-dB bandwidth of the TIA is ω_n . As illustrated in Fig. 10, adding C_L improves the filtering response of the TIA to a second-order response. Moreover, two complex conjugate poles of the second-order TIA enhance the 3-dB bandwidth, and a flat gain response is also achieved.

It is instructive to investigate the trade-off between TIA's 3-dB bandwidth and power consumption. At first glance, as can be inferred from (23), the most power-efficient way to increase the TIA's 3-dB bandwidth by a factor of β is to reduce

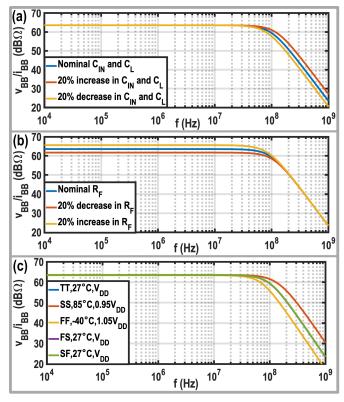


Fig. 11. The deviations of the frequency response of the second-order TIA against (a) $\pm 20\%$ variations of $C_{\rm IN}$ and C_L , (b) $\pm 20\%$ R_F variations, and (c) only $g_{\rm mt}$ and $r_{\rm ot}$ changes over PVT variations.

 $C_{\rm IN}$ and C_L by the same factor. However, one of the main roles of the TIA input capacitor is absorbing the out-of-band blocker currents. Since the location of the close-in blocker remains almost constant from the passband edges for different channel bandwidths in 3GPP standard [1], by an aggressive $C_{\rm IN}$ reduction, the TIA amplifier has to absorb a significant portion of the out-of-band blocker currents instead of $C_{\rm IN}$, thus degrading the RX out-of-band linearity performance. In other words, the linearity performance of the RX is sacrificed for the sake of power consumption. To alleviate this issue, the value of $g_{\rm mt}$ should be increased accordingly to maintain the RX linearity performance. Hence, to increase the 3-dB bandwidth of the TIA by the factor of β , it is wise to reduce $C_{\rm IN}$ and C_L by $\beta^{2/3}$, and simultaneously increase the value of $g_{\rm mt}$, and therefore, the TIA's power consumption should be increased by $\beta^{2/3}$.

A. TIA Performance Over PVT Variations

Since the damping ratio and natural frequency of the second-order TIA are related to the values of resistors, capacitors, and amplifier's transconductance and output resistance, this section investigates the sensitivity of the TIA frequency response over process, voltage, and temperature (PVT) variations.

The TIA's damping ratio is related to the ratio of $C_{\rm IN}$ to C_L [see (22)] and, consequently, remains almost constant with capacitor changes over PVT variations. However, as shown in Fig. 11(a), the TIA's 3-dB bandwidth is inversely proportional to the absolute values of $C_{\rm IN}$ and C_L and changes by $\approx \pm 20\%$ due to the expected $\pm 20\%$ capacitor deviation over PVT variations. On the other hand, as can be gathered

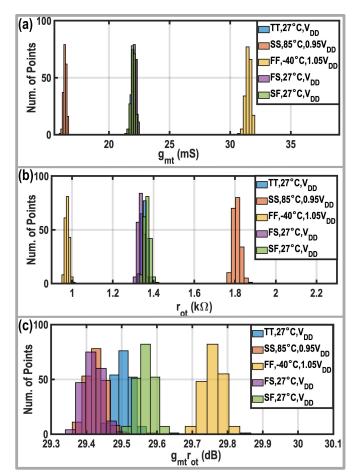


Fig. 12. Fluctuation of (a) $g_{\rm mt}$, (b) $r_{\rm ot}$, and (c) $g_{\rm mt} \times r_{\rm ot}$ over PVT variations using Monte Carlo simulations.

from (21) and simulation results in Fig. 11(b), the foreseen $\pm 20\%$ R_F variations change the transimpedance gain and 3-dB bandwidth of the second-order TIA significantly (i.e., $\pm 20\%$ and $\mp 10\%$, respectively), but its impacts on the damping ratio is negligible (i.e., $\approx \pm 1\%$).

Next, $g_{\rm mt}$ and $r_{\rm ot}$ fluctuations can also affect the TIA performance. Interestingly, the intrinsic gain $(g_{\rm mt} \times r_{\rm ot})$ of a single-stage inverter-based amplifier used in this design is almost constant over PVT variations, as can be gathered from Monte Carlo simulations in Fig. 12 (maximum 0.5-dB gain variation is observed). Hence, we can model $g_{\rm mt}$ and $r_{\rm ot}$ over PVT variations by

$$g_{\rm mt} = (1 + \alpha)g_{\rm mtTT} \tag{24}$$

$$r_{\rm ot} = \frac{r_{\rm otTT}}{(1+\alpha)} \tag{25}$$

where α is a process-dependent scaling factor; g_{mtT} and r_{otTT} are, respectively, the nominal values of the amplifier's transconductance and output resistance at the typical–typical process corner. By replacing (24) and (25) into (22) and assuming that $C_{\text{IN}} \gg C_L$, the damping ratio of the TIA can be rewritten as

$$\zeta \approx \frac{1}{2} \frac{1}{\sqrt{g_{\text{mtTT}} R_F}} \sqrt{\frac{C_{\text{IN}}}{C_L}} \left(1 + \frac{R_F}{r_{\text{otTT}}} + \frac{\alpha}{2} \left(\frac{R_F}{r_{\text{otTT}}} - 1 \right) \right). \tag{26}$$

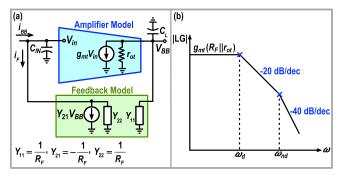


Fig. 13. (a) Feedback model with Y parameters for the second-order TIA. (b) Bode plot of the TIA amplifier LG.

Therefore, by choosing $r_{\text{otTT}} \approx R_F$, the sensitivity of the damping ratio to the g_{mt} and r_{ot} variations is vastly reduced. However, as shown in Fig. 11(c), the 3-dB bandwidth of the TIA is still sensitive to g_{mt} variations.

Considering the presented analysis, the damping ratio of the second-order TIA is almost insensitive to PVT variations. However, the 3-dB bandwidth and RX gain are PVT-sensitive and require calibrations. In practice, $g_{\rm mt}$ value is mainly determined based on noise requirement and can be stabilized over PVT variations using g_m -constant techniques. Then, R_F is tuned to adjust the RX gain. Finally, while maintaining $C_{\rm IN}$ to C_L ratio to keep the damping ratio constant, $C_{\rm IN}$ and C_L values are adjusted to get the desired 3-dB bandwidth.

B. Stability Analysis of the TIA's Amplifier

As mentioned earlier, C_F is removed from the TIA amplifier feedback to implement a second-order TIA. However, in conventional TIAs, C_F creates a zero improving the stability of the TIA amplifier [45]. Hence, it is instructive to analyze the effect of the adopted technique on the TIA amplifier stability. In order to do so, the same method presented in [46] is utilized to calculate the TIA amplifier's LG. Since the feedback type of the TIA amplifier is voltage-to-current, the Y matrix is employed to calculate the loading effect of the feedback impedance, as shown in Fig. 13(a). Consequently, the LG can be calculated by

$$LG = \frac{g_{\text{mt}}(R_F \parallel r_{\text{ot}})}{(1 + sC_{\text{IN}}R_F)(1 + sC_L(R_F \parallel r_{\text{ot}}))}.$$
 (27)

As illustrated in Fig. 13(b) and can be gathered from (27), the LG of the TIA amplifier has two poles. The dominant pole of LG is $1/(C_{\rm IN}R_F)$, and the nondominant pole of LG is $1/(C_L(R_F \parallel r_{\rm ot}))$. The phase margin of the TIA amplifier should be better than 45° to ensure its stability. Hence, the nondominant pole of LG should be larger than the unity-gain bandwidth (ω_u) of the TIA amplifier

$$\omega_{\rm nd} \ge \omega_u \Longrightarrow \frac{C_{\rm IN}}{C_L} \ge \frac{g_{\rm mt}(R_F \parallel r_{\rm ot})^2}{R_F}.$$
 (28)

Consequently, to ensure the stability of the TIA's amplifier, C_{IN} must be chosen much larger than C_L .

Fig. 14 shows the simulated magnitude and phase response of the LG of the TIA's amplifier using the "stb" analysis in Cadence. Since the TIA employs a single-stage amplifier,

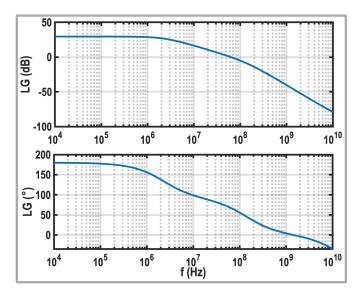


Fig. 14. Simulated magnitude and phase response of the TIA's LG.

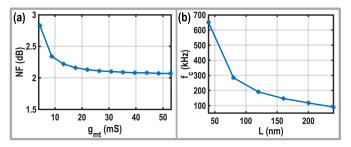


Fig. 15. (a) Simulated RX NF versus $g_{\rm mt}$. (b) Simulated flicker noise corner of the TIA amplifier versus the channel length of its input transistors.

the adopted method does not cause any stability issues, and a phase margin of 69° is obtained. It is worth mentioning that in applications with high in-band linearity requirements, a multistage amplifier is required, and any internal pole of the multistage amplifier should be considerably higher than ω_u to ensure the amplifier stability.

One may notice that the TIA can be stabilized even by choosing $1/(C_L(R_F \parallel r_{\rm ot}))$ as the dominant pole and wonder if this choice would result in a better performance. However, in this case, the TIA output would be shorted to ground at far-out out-of-band frequencies since C_L must be much larger than $C_{\rm IN}$ to ensure TIA's stability. Consequently, the input impedance of the TIA increases from $1/g_{\rm mt} + R_F/(g_{\rm mt}r_{\rm ot})$ to R_F at those frequencies, degrading the RX out-of-band linearity and sacrificing the stability of the RX front end, as can be gathered from (20) in Section II-E.

C. Design Guide for the Second-Order TIA

In this section, we develop a design guide for estimating the components (i.e., R_F , $g_{\rm mt}$, $r_{\rm ot}$, $C_{\rm IN}$, and C_L) of the second-order TIA based on the noise requirement, 3-dB bandwidth, and stability of the TIA amplifier. First, the R_F value is chosen based on the RX required gain. Then, the value of $g_{\rm mt}$ is determined such that the TIAs' noise has a negligible effect on the NF. Based on the simulated NF of the proposed RX versus $g_{\rm mt}$ in Fig. 15(a), $g_{\rm mt}$ larger than 17.5 mS is needed to limit its NF penalty to ≈ 0.1 dB. Later, in Section V, we will

develop a closed-form equation for the RX NF so that the required $g_{\rm mt}$ value can also be estimated analytically.

In the next step, as can be gathered from Fig. 15(b), the channel length (L_t) of the input transistors of the inverter-based amplifier is chosen 240 nm to achieve a flicker noise corner of ~100 kHz, much smaller than the RX 3-dB bandwidth. By knowing $g_{\rm mt}$ and L_t , the output resistance of the inverter-based amplifier can be easily determined. Finally, by considering a simulated $r_{\rm ot}$ of 1.5 k Ω , and assuming $C_{\rm IN} \gg C_L$ due to stability issues, $C_{\rm IN}$ and C_L can be estimated using damping factor (22) and natural frequency (23) equations

$$C_{\rm IN} = \frac{2\zeta g_{\rm mt}}{\omega_n \left(1 + \frac{R_F}{r_{\rm ot}}\right)} \tag{29}$$

$$C_L = \frac{\left(1 + \frac{R_F}{r_{\text{ot}}}\right)}{2R_F \zeta \omega_n}.\tag{30}$$

Considering $\zeta = \sqrt{2}/2$, $\omega_n = 2\pi \times 100$ MHz, and $R_F=1.6\,\mathrm{k}\Omega$, the calculated values of C_{IN} and C_L are 21.8 and 1.45 pF, respectively. All the circuit parameters calculated in the design guide are then used to simulate the filter transfer function. As shown in Fig. 10, the simulated 3-dB bandwidth and filtering roll-off of the designed TIA are, respectively, 88 MHz and -38 dB/dec, confirming the validity of the developed design guide.

D. TIA Selectivity and Area Tradeoff

Although the adopted second-order TIA has two complex conjugate poles and offers better selectivity than conventional first-order TIA, it is instructive to compare the total value of their required capacitors to realize the same 3-dB bandwidth. The 3-dB bandwidth of the conventional TIA, illustrated in Fig. 5(a), can be calculated by

$$f_{3dB} = \frac{1}{2\pi \left(C_{F,con} R_F + C_{IN,con} \left(\frac{1}{g_{mt}} + \frac{R_F}{1 + g_{mt} r_{ot}} \right) \right)}.$$
 (31)

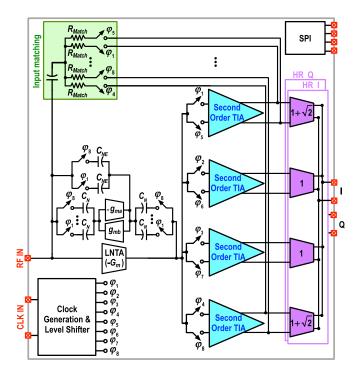
One can choose $C_{IN,conv} = 0$ and set the 3-dB bandwidth by $C_{F,con}R_F$ to minimize the required capacitor. However, in this way, the TIA amplifier should absorb all the out-ofband blocker current, increasing the TIA's power consumption. As a compromise between the power consumption and area, the poles created by $C_{F,\mathrm{conv}}$ and $C_{\mathrm{IN},\mathrm{conv}}$ should contribute equally to the 3-dB bandwidth. Hence

$$C_{F,\text{conv}} = \frac{1}{4\pi f_{\text{2dR}} R_F} \tag{32}$$

$$C_{F,\text{conv}} = \frac{1}{4\pi f_{3\text{dB}} R_F}$$

$$C_{\text{IN,conv}} = \frac{g_{\text{mt}} r_{\text{ot}}}{4\pi f_{3\text{dB}} (R_F + r_{\text{ot}})}.$$
(32)

Considering the same parameters used in the second-order TIA design, $R_F = 1.6 k\Omega$, $f_{3dB} = 100$ MHz, $g_{mt} = 20$ mS, and $g_{\rm mt}r_{\rm ot}=30$, $C_{F,\rm conv}$ and $C_{\rm IN,conv}$ become 0.5 and 7.7 pF, respectively. As estimated in Section III-C, the total required capacitor of the adopted second-order TIA is 23.25 pF, thus demanding 2.75× larger capacitance than the conventional TIA. However, since the value of the TIA capacitors for the 5G channels with large bandwidths is relatively small, they do not occupy a large chip area, and it is wise to use second-order



Block diagram of the proposed RX.

TIAs to achieve higher selectivity. For the 5G low channel bandwidth, the location of the close-in blocker from passband edges remains constant, and even a more area-efficient firstorder TIA can provide sufficient blocker attenuation due to the higher ratio of the blocker offset frequency to the channel bandwidth. Consequently, for future implementation of 5G RXs with programmable channel bandwidths, switchable load (C_L) and feedback (C_F) capacitors must be placed to achieve area efficiency and selectivity simultaneously. In low (high) bandwidths, $C_F(C_L)$ and $C_L(C_F)$ banks would, respectively, be turned on and off to realize first-order (second) filtering.

IV. CIRCUIT IMPLEMENTATION

Fig. 16 shows the entire RX block diagram, in which eight-phase passive mixers are used to down-convert the RF current of the LNTA. Then, the second-order TIAs convert the downconverted RF current to baseband voltages. Similar to [47] and as shown in Fig. 9(b), a common-mode feedback (CMFB) circuit sets the dc operating point of the TIAs' outputs around mid-rail voltage. Harmonic rejection (HR) is implemented by combining the weighted TIAs' outputs to generate in-phase (I) and quadrature (Q) baseband signals. Therefore, the third and fifth harmonic of the LO will be rejected, improving the NF and linearity of the RX. The $50\,\Omega$ matching is implemented by up-converting baseband voltages at TIAs' outputs, combining the upconverted signals through the matching resistors (R_{Match}), and applying the resulting signal back to the RX input [48], [49], [50]. In this way, thanks to the RX voltage gain, the matching resistors become significantly large and negligibly contribute to the RX NF. Since the voltage gain from the antenna to the TIA output has a positive sign, a-1 multiplication is required in the translational network to guarantee negative feedback. The -1 multiplication is easily implemented by applying

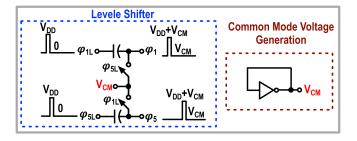


Fig. 17. Schematics of the implemented level shifter for biasing the LOs.

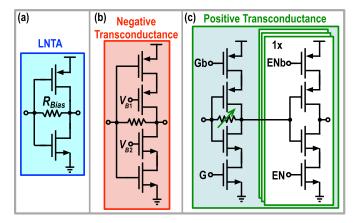


Fig. 18. Schematics of the implemented (a) LNTA, (b) positive, and (c) negative transconductance of the gyrator.

out-of-phase LO clocks to the associated down-converting and up-converting passive mixers of each TIA.

NMOS transistors are used to implement the passive mixers. The drains of those devices are biased at $V_{CM} \approx V_{DD}/2$ since they are connected to the input and output of the LNTA. Hence, as shown in Fig. 17, level shifters are used to shift the LO levels from 0- V_{DD} to V_{CM} - V_{DD} + V_{CM} . V_{CM} is generated inside the chip using an inverter with shorted input and output. Unlike the RX implemented in our previous work [41], the bulks of NMOS transistors are biased to V_{CM} in the respin prototype to improve the RX linearity performance. As shown in 18(a), the LNTA is implemented using inverter-based amplifiers with shunt resistive feedback to bias the transistors in saturation. Despite the simplicity of the inverter-based LNTA, G_m , the power consumption, and the input-referred noise voltage of the LNTA are sensitive to the PVT variations. In a future implementation, a constant- g_m biasing technique can be adopted to resolve this issue.

In the gyrator-based implementation of an active inductor, an undesired equivalent series resistance exists, which is inversely related to the voltage gain of the feedforward transconductance (g_{ma}) [51]. Hence, the feedforward transconductance is implemented with a cascode inverter-based amplifier to reduce the undesired series resistance of the gyrator. However, in the first implementation of the proposed RX [41], a common gate amplifier was used to implement the feedback transconductance (g_{mb}). The input impedance of the feedback transconductance can be approximated by $1/g_{mb}$, which loads the feedforward transconductance, reducing its gain. Thus, the series resistance increases, degrading

the selectivity of the proposed RX. To solve this issue, in the respin prototype, two series amplifiers are adopted to implement the feedback transconductance, as illustrated in Fig. 18(c). For measurement purposes, different components of the TIA (the amplifier, C_L , and $C_{\rm IN}$) and gyrator ($g_{\rm ma}$ and $g_{\rm mb}$) are tunable and can be programmed through a serial peripheral interface (SPI).

Since this design employs a supply voltage higher than the 40-nm nominal voltage (i.e., 1.3 V, rather than 1.1 V), time-dependent dielectric breakdown (TDDB) and hot carrier injection (HCI) [52], [53], as two main failure mechanisms in CMOS circuits, are considered here to investigate the RX reliability. The HCI degradation occurs when the drain current and drain-source voltage (V_{DS}) of a transistor are large simultaneously. The maximum V_{DS} of all transistors in the LNTA and TIAs' amplifiers is $0.5V_{DD} = 0.65 \text{ V}$, which is much less than the standard voltage of thin-oxide transistors. Moreover, the transistors in the LO buffers do not conduct any current when their $V_{\rm DS}$ is 1.3 V. Consequently, the proposed RX is not vulnerable to HCI. On the other hand, the thickness of gate-oxide for 40-nm transistors is ~2.5 nm, and based on analysis in [53] and [54] and the reliability rules of the process design kit, they can withstand a maximum gate-drain and gate-source voltage of 1.6 V without facing a gate-oxide breakdown in ten years.

V. Noise Analysis

Fig. 19 shows the simplified noise model of the proposed RX, in which the gyrator noise is modeled with two current sources at its input and output, i.e., $i_{n,\text{gmb}}^2 = 4kT\gamma g_{\text{mb}}$ and $i_{n,\text{gma}}^2 = 4kT\gamma g_{\text{ma}}$, where γ is the average thermal noise excess factor of NMOS and PMOS transistors used in gyrators feedforward and feedback transconductors. By taking the same procedure presented in [3], [47], and [55], the noise factor of the proposed RX can be approximated by

$$F = \left(1 + \frac{\gamma}{G_{m}R_{s}} + \frac{R_{s}}{R_{\text{Bias}}} + \frac{R_{s}}{R_{\text{Match}}} + \left(\frac{R_{S}}{Z_{N}}\right)^{2} \times \frac{\gamma}{g_{\text{ma}}R_{S}} \left(1 + \frac{1}{g_{\text{mb}}^{2}Z_{N}^{2}}\right) + \frac{1}{A_{v}^{2}} \times \left(\frac{R_{o}}{Z_{N}}\right)^{2} \times \frac{\gamma}{g_{\text{mb}}R_{S}} \left(1 + \frac{1}{g_{\text{ma}}^{2}Z_{N}^{2}}\right) + \frac{1}{A_{v}^{2}} \times \left(\frac{R_{\text{SW}}}{R_{S}} + \frac{M \times R_{S}}{R_{F}}\right) \times \frac{1}{\text{sinc}^{2}\left(\frac{1}{M}\right)} + \frac{1}{A_{v}^{2}} \frac{\rho v_{n,A}^{2}}{4kTR_{S}} \times \left(\frac{R_{o} + R_{\text{SW}}}{\rho R_{F}} + \frac{R_{o} + R_{\text{SW}} + Z_{\text{eq}}}{Z_{\text{eq}}}\right)^{2}.$$
(34)

Here, $R_{\rm SW}$ is the on-resistance of the down-converting passive mixers, $R_{\rm Bias}$ is the shunt bias resistor of the LNTA, A_v is the voltage gain from the antenna to the LNTA's output $(A_v = G_m R_o/2)$, $v_{n,A}$ is the input-referred noise voltage of the TIA amplifier, and ${\rm sinc}^2(1/M)$ accounts for the loss of passive mixers. Moreover, ρ and $Z_{\rm eq}$ are given by

$$\rho = \frac{1}{M} \operatorname{sinc}^2 \left(\frac{1}{M} \right) \tag{35}$$

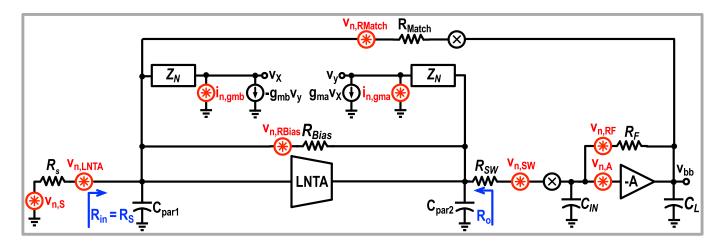


Fig. 19. Simplified model of the proposed RX for NF calculation.

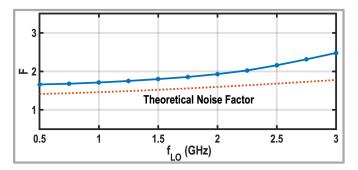


Fig. 20. Simulated noise factor of the proposed RX realized with real devices versus the LO frequency.

$$Z_{\rm eq} = Z_{\rm sh} \parallel \frac{1}{j\omega_{\rm BB} \times \frac{C_{\rm IN}}{\rho}} \tag{36}$$

$$Z_{\rm sh} = \frac{M\rho}{1 - M\rho} (R_o + R_{\rm SW}). \tag{37}$$

At the low in-band offset frequencies, the N-path notch filter exploits high impedance (i.e., $Z_N \gg R_s$, R_o), and the gyrator noise does not degrade the noise factor. Assuming that R_F and R_{Match} are large enough, (34) at low in-band offset frequencies can be simplified to

$$F = \left(1 + \frac{\gamma}{G_m R_s} + \frac{R_s}{R_{\text{Bias}}} + \frac{1}{A_v^2} \times \left(\frac{R_{\text{SW}}}{R_S}\right) + \frac{M \times R_S}{R_F} + \frac{v_{n,A}^2}{M \times 4kTR_S}\right) \times \frac{1}{\text{sinc}^2(\frac{1}{M})}.$$
 (38)

Considering $G_m=130$ mS, $\gamma=1$, $R_o=60$ Ω , $R_{\rm Bias}=400$ Ω , M=8, $R_{\rm SW}=10$ Ω , $R_F=1.6$ $k\Omega$, and $g_{\rm mt}=20$ mS, the theoretical noise factor is 1.41. As illustrated in Fig. 20, the simulated noise factor of the RX realized with real devices is 1.66 at low LO frequency, which is 0.25 higher than the ideal case, since the noise of gate and bulk resistors is not modeled in our analysis. The parasitic capacitors at the input and output of the LNTA reduce A_v at high LO frequencies, increasing the noise contribution of passive mixers, TIA feedback resistors, and TIA amplifiers, as predicted by (34) and confirmed by the noise factor simulation results in Fig. 20.

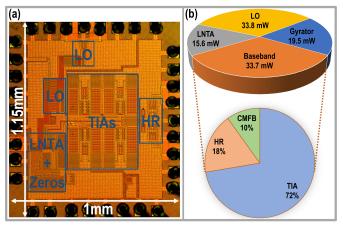


Fig. 21. (a) Die micrograph of the proposed RX. (b) Power consumption breakdown at 1.5-GHz LO frequency.

Consequently, the noise factor degrades to 2.47 at 3-GHz LO frequency.

VI. EXPERIMENTAL RESULTS

The proposed RX was fabricated in TSMC 40-nm bulk CMOS technology. As shown in Fig. 21(a), the RX occupies $1 \times 1.15 \text{ mm}^2$ with a core area of 0.5 mm^2 . The chip consumes 84–140 mW from a 1.3-V supply voltage over the 0.5–3-GHz operating frequency. The power consumption breakdown at 1.5-GHz LO frequency is also depicted in Fig. 21(b).

Fig. 22(a) and (b) shows the RX gain and in-band S_{11} versus the operating frequency when the auxiliary path is enabled. The RX gain is 37.2 dB at 0.5-GHz LO frequency and decreases to 34.6 dB at 3-GHz LO frequency. Due to the higher parasitic capacitance of the N-path notch filters, the measured BW_{RF} is 160 MHz. The input matching of the proposed RX is better than -8 dB over the 3-dB bandwidth and for the entire operating frequency. Fig. 22(c) shows the RX input impedance on the Smith chart for 1.5-GHz LO frequency when the auxiliary path is active. The input impedance is around 50 Ω across the 3-dB bandwidth (highlighted in red). Then, the input impedance reaches $\approx 10 \Omega$ at far-out out-of-band offset frequencies.

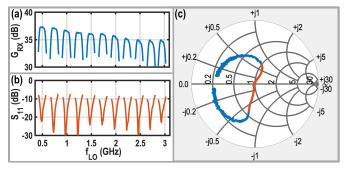


Fig. 22. Measured (a) G_{RX} , (b) in-band S_{11} , and (c) Smith chart view of the measured S_{11} at $f_{\rm LO}=1.5$ GHz.

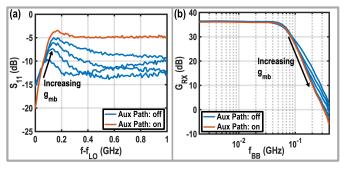


Fig. 23. Effect of the programmable zeros on (a) S_{11} and (b) G_{RX} at $f_{\rm LO}=1.5$ GHz.

The zeros' effect on the RX input impedance is investigated in Fig. 23(a) by turning off the auxiliary path and sweeping the value of $g_{\rm mb}$ at $f_{\rm LO}=1.5$ GHz. As mentioned earlier and predicted by (4) and (8), enhancing $g_{\rm mb}$ increases the zeros frequencies and reduces the input impedance of the proposed RX at the location of the zeros. Hence, measured S_{11} approaches ≈ -5 dB for the highest $g_{\rm mb}$, and the zero frequency is increased from $f_{\rm OS}\approx 10$ MHz ($\chi=1.125$) to $f_{\rm OS}\approx 100$ MHz ($\chi=2.25$) by moving from the lowest $g_{\rm mb}$ setting to the highest one. Moreover, enabling the auxiliary path increases S_{11} to above -5 dB beyond the zero frequency, as it reduces the RX input impedance at far-out offset frequencies.

The effect of the programmable zeros on the RX gain is shown in Fig. 23(b). Enhancing g_{mb} increases the zeros frequencies, offering \approx 4.6-dB better rejection for the close-in blockers. The auxiliary path also improves the out-of-band rejection of the RX by at least \approx 2 dB at far-out offset frequencies. Note that the auxiliary path has a negligible effect on the RX 3-dB bandwidth. For the rest of the measurements, the auxiliary path is enabled, and g_{mb} is set to its maximum value.

As can be deduced by (22) and Fig. 24(a), enhancing C_L reduces the damping factor and realizes two complex poles and a flat in-band gain in the transfer function of the RX gain. Moreover, as can be inferred from (23) and Fig. 24(b), the 3-dB bandwidth of the TIA can be controlled by $g_{\rm mt}$ while keeping the passive components of the TIA constant. The RX BW_{RF} can be tuned from 119 to 168 MHz by increasing $g_{\rm mt}$, while the value of ζ remains almost constant. For the rest of the measurements, $g_{\rm mt}$ is adjusted to its nominal value, and the C_L tuning word is set to achieve a second-order Butterworth response with a 160-MHz bandwidth.

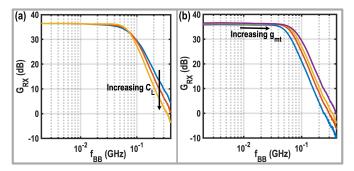


Fig. 24. (a) Improving the RX selectivity by adjusting the value of C_L at $f_{\rm LO} = 1.5$ GHz. (b) Enhancing the 3-dB bandwidth of the RX by increasing $g_{\rm mt}$ at $f_{\rm LO} = 1.5$ GHz.

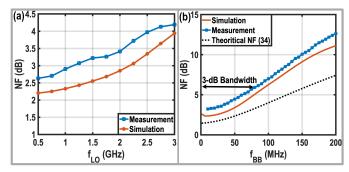


Fig. 25. (a) Measured NF versus the LO frequency. (b) Measured NF versus the baseband frequency at $f_{LO} = 1.5$ GHz.

Fig. 25(a) and (b) depicts the measured NF versus the LO frequency and the baseband frequency. NF is 2.6 dB at the minimum LO frequency and increases to 4.2 dB at the maximum operating frequency. At the RX passband edges, the impedance of the N-path notch filters and the TIA input capacitor is reduced. Hence, as can be gathered from (34), the noise contribution of the gyrator noise and the TIA amplifier increases at the 3-dB bandwidth edge. Consequently, as shown in Fig. 25(b), the NF degrades by 2.7 dB at the RX passband edges.

As illustrated in Fig. 26(a), the worst measured LO leakage is -90.9 dBm at the minimum LO frequency and reaches -63 dBm at the maximum LO frequency. As discussed in [26] and [56], the parasitic capacitors of the passive mixers and the LNTA's delay shift the center frequency of the RX gain toward the lower side of the LO frequency. This is a drawback of channel selection at the RF front end. Fig. 26(b) shows the frequency shift of the RX gain (f_{shift}) normalized to BW_{RF}, in which the worst frequency shift is 14% of the BW_{RF}. Consequently, in future implementations, a polyphase N-path notch filter [26] should be adopted in the auxiliary path to alleviate this issue. Simulation results show that this well-known technique can bring back the center frequency of the RX gain to f_{LO} , without affecting the zeros frequencies.

After showing the wideband operation of the proposed RX, the LO frequency is fixed at 1.5 GHz, and the rest of the measurements are carried out. The RX small-signal linearity measurements are depicted in Fig. 27. For third-order intercept point (IIP3) measurement, the tones are located at $f_1 = f_{LO} + \Delta f$ and $f_2 = f_{LO} + 2\Delta f - 5$ MHz. Moreover, the locations of the two tones are $f_1 = f_{LO} + \Delta f$ and $f_2 = f_{LO} + \Delta f$ or the second-order intercept point

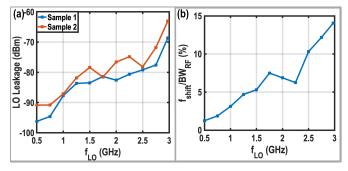


Fig. 26. Measured (a) LO leakage for two samples and (b) frequency shift of the proposed RX normalized to BW_{RF} versus the LO frequency.

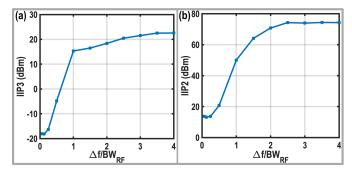


Fig. 27. Measured (a) IIP3 and (b) IIP2 versus the offset frequency (Δf) normalized to BW_{RF} at $f_{\rm LO}=1.5$ GHz.

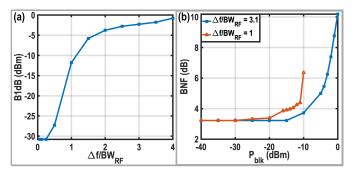


Fig. 28. Measured (a) B1dB versus the blocker offset frequency and (b) blocker NF versus the blocker power at $f_{LO} = 1.5$ GHz.

(IIP2) measurements. The RX in-band IIP3 is -18 dBm, and thanks to the RX sharp filtering, it improves to 15.3 dBm when $\Delta f/\mathrm{BW_{RF}}$ is 1. The out-of-band IIP3 of the proposed RX reaches 22.5 dBm at far-out offset frequencies. The measured in-band IIP2 is 13.4 dBm, and it reaches 74.3 dBm at far-out out-of-band offset frequencies.

A small signal at $f_{\rm sig}=f_{\rm LO}+5$ MHz is accompanied by a large blocker located at $f_{\rm blk}=f_{\rm LO}+\Delta f$ for the B1dB measurements. As shown in Fig. 28(a), the RX in-band B1dB is -30.8 dBm and improves to -11.8 dBm when $\Delta f/{\rm BW_{RF}}$ is 1. The out-of-band B1dB of the RX is -0.3 dBm. The RX NF is plotted versus the blocker power located at $\Delta f/{\rm BW_{RF}}=1$ and $\Delta f/{\rm BW_{RF}}=3.1$ in Fig. 28(b). A -10-dBm blocker located at $\Delta f/{\rm BW_{RF}}=1$ increases the NF to 6.3 dB, and a 0-dBm blocker placed at $\Delta f/{\rm BW_{RF}}=3.1$ degrades the NF to 10.2 dB.

The performance of the RX is also investigated based on the 3GPP requirements for user equipment applications. The first test is reference sensitivity, and to do so, a 100-MS/s quadrature phase shift keying (QPSK) signal with -86.7-dBm

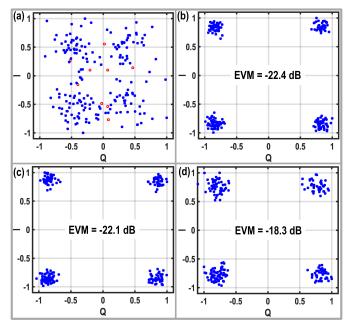


Fig. 29. (a) Measured constellation at reference sensitivity. Measured constellation in the presence of (b) -44-dBm blocker located at 15-MHz offset, (c) -30-dBm blocker at 60-MHz offset frequency, and (d) -15-dBm blocker at 85-MHz offset frequency, while signal power is 16 dB higher than the reference sensitivity level.

power is applied to the proposed RX. In this case, the throughput of the RX should be better than 95%. Fig. 29(a) shows the constellation of the received signal. The throughput of the RX is 95.5%. Note that red squares denote the missing symbols in Fig. 29(a).

The out-of-band blocking test of the user equipment application is divided into three ranges. In the first range, a -44-dBm CW blocker is located between 15- and 60-MHz offset from the 3-dB bandwidth edge. In the second range, the blocker is located between 60- and 85-MHz offset and its power increases to -30 dBm. The last range is the most difficult blocking scenario in which a -15-dBm CW blocker is present at 85-MHz offset frequency. Based on the 3GPP standard, the power of the desired signal in all the above-mentioned tests should be increased by $9 + 10\log_{10}(BW_{RF}/20)$ dB compared with the reference sensitivity power level [1]. Since the bandwidth of the desired signal is 100 MS/s, its power is increased by 16 dB. As can be gathered from the constellation diagrams in Fig. 29(b)-(d), all the symbols are received correctly, and the measured error vector magnitude (EVM) is always better than -18.3 dB. Hence, the proposed RX successfully passes all out-of-band blocking tests defined in the 3GPP standard for the TDD mode.

High-order modulation schemes are used in 5G applications to increase the data rate and spectral efficiency. Hence, the performance of the proposed RX is also investigated for the QAM-64 signal. A 100-MS/s QAM-64 signal with -60 dBm is applied to the RX. Fig. 30(a) shows the measured constellation in which the EVM is -29 dB. Moreover, to test the large signal performance of the RX, a -5-dBm blocker is combined with the desired signal and applied to the RX input. As shown in Fig. 30(b), the measured EVM only degrades by 1.9 dB and reaches -27.1 dB.

	This Work	This Work	Murphy	Hedayati	Musayev	Wang	Razavi	Kim	Guo
	Respin Prototype	ISSCC 2021 [41]	JSSC 2012 [47]		JSSC 2019 [58]			OJSSC 2022 [40]	RFIC 2023 [59]
Technology	40nm CMOS	40 nm CMOS	40nm CMOS	40nm CMOS	65nm CMOS	45nm SOI	28nm	65nm CMOS	65nm CMOS
f _{RF} (GHz)	0.5 - 3.0	0.4 - 3.2	0.09 - 2.7	0.1 – 2.8	0.7 – 1.4	0.2 – 2	0.4 – 6	1.6 – 2.2	1 – 3
Gain (dB)	37	36	72	50	36.8	40	54	23.2	40
NF (dB)	2.6 – 4.2	2.7 – 3.6	1.9	1.8	1.9	2.1 - 2.5	2.1†/4.42§	2.5	2.2
BW _{RF} (MHz)	160	160	6	10	30	20	0.2 - 160	80	850
LO Leakage (dBm)	-94 – -66	-8669	-65	-82	NA	-94 – -79	NA	NA	NA
In-band Flatness	Yes	Yes	No	No	No	No	No	No	Yes
Out-of-band IIP3	16.5	10	13.5	5	1	14	3\$	26.1	8
(dBm)	$\Delta f/BW_{RF} = 1.5$	$\Delta f/BW_{RF} = 1.5$	$\Delta f/BW_{RF} = 3.3$	$\Delta f/BW_{RF} = 5$		$\Delta f/BW_{RF} = 5$	$\Delta f/BW_{RF} = 12.5$	$\Delta f/BW_{RF} = 1.5$	$\Delta f/BW_{RF} = 2.5$
B1dB (dBm)	-2.7	-5	-2	NA	-8.5	NA	NA	0.5	NA
	$\Delta f/BW_{RF} = 2.5$	$\Delta f/BW_{RF} = 2.5$	$\Delta f/BW_{RF} = 13.3$	INA					INA
Out-of-band IIP2	64	50	55	50	35	60	20\$	71	NA
(dBm)	$\Delta f/BW_{RF} = 1.5$	$\Delta f/BW_{RF} = 1.5$	$\Delta f/BW_{RF} = 3.3$	$\Delta f/BW_{RF} = 5$		$\Delta f/BW_{RF} = 5$	$\Delta f/BW_{RF} = 12.5$	$\Delta f/BW_{RF} = 2.5$	INA
0 dBm BNF (dB)	10.2	8.4	4.1	14	6.6	6.7	5.2 [†] /7.4 [§]	5.9	3.6
	$\Delta f/BW_{RF} = 3.1$	$\Delta f/BW_{RF} = 3.1$	$\Delta f/BW_{RF} = 13.3$	$\Delta f/BW_{RF} = 5$		$\Delta f/BW_{RF} = 4$			$\Delta f/BW_{RF} = 1.5$
EVM wo/wi blocker	-29 / -27.1&	-26.4 / -25.5 [£]	NA	NA	NA	NA	-25.3¢ / NA	NA	NA
Supply (V)	1.3	1.3/1.2	1.3	1.1	0.8/1/1.2	1.2	1	0.4/1.2/2.5	1.2
Active Area (mm²)	0.5	0.6	1.2	0.8	0.25	1.05	1.9	0.33	0.5
Power (mW)	72.8 + 22.5 mW/GHz	58.5 + 17.6 mW/GHz	35.1 – 78	27 – 40	14 + 37.2 mW/GHz	68 – 95	23 – 49	6.5 + 18.5 mW/GHz	44 + 14 mW/GHz

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART RXS

& 100 MS/s -60 dBm QAM-64 with -5 dBm blocker, £ 143 MS/s -60 dBm QAM-64 with -8 dBm blocker, † Low noise mode, § Harmonic Reject, \$ Highest bandwidth, ¢ 80 MS/s -57 dBm QAM-64

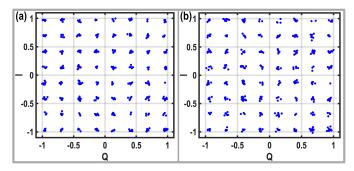


Fig. 30. Measured constellation of 100-MS/s -60-dBm QAM-64 signal: (a) without blocker and (b) with -5-dBm blocker located at $\Delta f/\omega_{3\text{dB}}=3.1$.

Table I summarizes the measured performance of the proposed RX and benchmarks it with state-of-the-art LNTA-based RXs. The proposed RX shows a competitive NF compared with state-of-the-art LNTA-based RXs [33], [36], [40], [41], [47], [57], [58], [59]. Moreover, at the cost of higher power consumption, the fabricated prototype outperforms other LNTA-based RXs in terms of linearity except [40]. However, [40] has a relatively narrow operating frequency range, uses several supply voltages, and requires a complex calibration procedure to reach the reported linearity performance. Moreover, this work is the only RX that reports EVM while facing a large CW blocker.

VII. CONCLUSION

This article demonstrates a wideband RX in 40-nm bulk CMOS technology for 5G TDD user equipment applications. The proposed programmable zeros and the adopted second-order TIA increase the selectivity of the proposed RX and satisfy the 5G stringent linearity requirements for close-in blockers. Moreover, an auxiliary path is introduced to sink the blocker current, improving the far-out linearity performance

of the proposed RX. Two design guides are provided to determine the components' values of the proposed RX RF front end and the second-order TIA. The proposed RX could successfully satisfy the requirements of the 5G TDD user equipment application for reference sensitivity and out-of-band blocking tests.

APPENDIX

This appendix accurately calculates the frequencies of the implemented zeros. The proposed LNTA feedback impedance, Z_F , is calculated as follows:

$$Z_F = \frac{s^4 C_S L_S C_P L_P + s^2 (C_S L_S + C_P L_P + C_S L_P) + 1}{s C_S (s^2 C_P L_P + 1)}.$$
(39)

Hence, the zeros frequencies can be derived as

$$f_{1,2}^2 = f_{LO}^2 \times \left(1 + \frac{1}{2} \omega_{LO}^2 C_S L_P \left(1 \mp \sqrt{1 + \frac{4}{\omega_{LO}^2 C_S L_P}} \right) \right)$$
(40)

and assuming that $\omega_{LO}^2 C_S L_P \ll 1$, (40) can be simplified as follows:

$$f_{1,2} = f_{LO}\sqrt{1 \mp \omega_{LO}\sqrt{C_S L_P}} = f_{LO}\sqrt{1 \mp \sqrt{\frac{C_S}{C_P}}}.$$
 (41)

Finally, considering $C_S/C_P \ll 1$, (41) can be recalculated as follows:

$$f_{1,2} = f_{LO} \mp \frac{f_{LO}}{2} \sqrt{\frac{C_S}{C_P}} = f_{LO} \mp f_{z1,2}.$$
 (42)

ACKNOWLEDGMENT

imec-Leuven is acknowledged for handling the tape-out. The authors would like to thank Atef Akhnoukh and Zu-Yao Chang for their strong support during the design, fabrication, and measurement. They would also like to thank Zhong Gao and Sajad Golabi for their technical discussions. They would also like to thank Mohsen Mortazavi and Yiyu Shen for their help during the measurements.

REFERENCES

- [1] User Equipment (UE) Radio Transmission and Reception, document TS 38.101-1 V16.8.0, 3GPP, EUTR Access, Jun. 2021.
- [2] User Equipment (UE) Radio Transmission and Reception, document TS 36.101 V17.3.0, EUTR Access, 3GPP, Sep. 2021.
- [3] C. Andrews and A. C. Molnar, "A passive mixer-first receiver with digitally controlled and widely tunable RF interface," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2696–2708, Dec. 2010.
- [4] C. Andrews, L. Diamente, D. Yang, B. Johnson, and A. Molnar, "A wideband receiver with resonant multi-phase LO and current reuse harmonic rejection baseband," *IEEE J. Solid-State Circuits*, vol. 48, no. 5, pp. 1188–1198, May 2013.
- [5] D. H. Mahrof, E. A. M. Klumperink, Z. Ru, M. S. O. Alink, and B. Nauta, "Cancellation of OpAmp virtual ground imperfections by a negative conductance applied to improve RF receiver linearity," *IEEE J. Solid-State Circuits*, vol. 49, no. 5, pp. 1112–1124, May 2014.
- [6] A. Nejdel, M. Abdulaziz, M. Törmänen, and H. Sjöland, "A positive feedback passive mixer-first receiver front-end," in *Proc. IEEE Radio* Freq. Integr. Circuits Symp. (RFIC), May 2015, pp. 79–82.
- [7] H. Westerveld, E. Klumperink, and B. Nauta, "A cross-coupled switch-RC mixer-first technique achieving +41 dBm out-of-band IIP3," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, May 2016, pp. 246–249.
- [8] Y.-C. Lien, E. A. M. Klumperink, B. Tenbroek, J. Strange, and B. Nauta, "High-linearity bottom-plate mixing technique with switch sharing for N-path filters/mixers," *IEEE J. Solid-State Circuits*, vol. 54, no. 2, pp. 323–335, Feb. 2019.
- [9] V. K. Purushothaman, E. A. M. Klumperink, B. T. Clavera, and B. Nauta, "A fully passive RF front end with 13-dB gain exploiting implicit capacitive stacking in a bottom-plate N-path filter/mixer," *IEEE J. Solid-State Circuits*, vol. 55, no. 5, pp. 1139–1150, May 2020.
- [10] E. Zolkov and E. Cohen, "A mixer-first receiver with enhanced matching bandwidth by using baseband reactance-canceling LNA," *IEEE Solid-State Circuits Lett.*, vol. 4, pp. 109–112, 2021.
- [11] A. N. Bhat, R. A. R. van der Zee, and B. Nauta, "A baseband-matching-resistor noise-canceling receiver with a three-stage inverter-only OpAmp for high in-band IIP3 and wide IF applications," *IEEE J. Solid-State Circuits*, vol. 56, no. 7, pp. 1994–2006, Jul. 2021.
- [12] V. K. Purushothaman, E. A. M. Klumperink, R. Plompen, and B. Nauta, "Low-power high-linearity mixer-first receiver using implicit capacitive stacking with 3× voltage gain," *IEEE J. Solid-State Circuits*, vol. 57, no. 1, pp. 245–259, Jan. 2022.
- [13] B. Guo, H. Wang, Y. Wang, K. Li, L. Li, and W. Zhou, "A mixer-first receiver frontend with resistive-feedback baseband achieving 200 MHz IF bandwidth in 65 nm CMOS," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2022, pp. 31–34.
- [14] S. Araei, S. Mohin, and N. Reiskarimian, "An interferer-tolerant harmonic-resilient receiver with > 10 dBm 3rd-harmonic blocker P1dB for 5G NR applications," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, USA, Feb. 2023, pp. 18–20.
- [15] Y.-C. Lien, E. A. M. Klumperink, B. Tenbroek, J. Strange, and B. Nauta, "Enhanced-selectivity high-linearity low-noise mixer-first receiver with complex pole pair due to capacitive positive feedback," *IEEE J. Solid-State Circuits*, vol. 53, no. 5, pp. 1348–1360, May 2018.
- [16] S. Krishnamurthy and A. M. Niknejad, "Design and analysis of enhanced mixer-first receivers achieving 40-dB/decade RF selectivity," *IEEE J. Solid-State Circuits*, vol. 55, no. 5, pp. 1165–1176, May 2020.
- [17] G. Pini, D. Manstretta, and R. Castello, "Analysis and design of a 260-MHz RF bandwidth +22-dBm OOB-IIP3 mixer-first receiver with third-order current-mode filtering TIA," *IEEE J. Solid-State Circuits*, vol. 55, no. 7, pp. 1819–1829, Jul. 2020.
- [18] S. Krishnamurthy and A. M. Niknejad, "Synthesis and design of enhanced N-path filters with 60-dB/decade RF selectivity," *IEEE Solid-State Circuits Lett.*, vol. 3, pp. 522–525, 2020.

- [19] S. Krishnamurthy and A. M. Niknejad, "An enhanced mixer-first receiver with distortion cancellation, achieving 80-dB/decade RF selectivity and +8-dBm B1dB for adjacent channel blockers," *IEEE Solid-State Circuits Lett.*, vol. 4, pp. 64–67, 2021.
- [20] A. Ghaffari, E. A. M. Klumperink, M. C. M. Soer, and B. Nauta, "Tunable high-Q N-path band-pass filters: Modeling and verification," *IEEE J. Solid-State Circuits*, vol. 46, no. 5, pp. 998–1010, May 2011.
- [21] C. Andrews and A. C. Molnar, "Implications of passive mixer transparency for impedance matching and noise figure in passive mixer-first receivers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 12, pp. 3092–3103, Dec. 2010.
- [22] A. Mirzaei, H. Darabi, J. C. Leete, and Y. Chang, "Analysis and optimization of direct-conversion receivers with 25% duty-cycle currentdriven passive mixers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 9, pp. 2353–2366, Sep. 2010.
- [23] A. Mirzaei, H. Darabi, and D. Murphy, "Architectural evolution of integrated M-phase high-Q bandpass filters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 1, pp. 52–65, Jan. 2012.
- [24] A. Mirzaei, H. Darabi, A. Yazdi, Z. Zhou, E. Chang, and P. Suri, "A 65 nm CMOS quad-band SAW-less receiver SoC for GSM/GPRS/EDGE," *IEEE J. Solid-State Circuits*, vol. 46, no. 4, pp. 950–964, Apr. 2011.
- [25] J. Borremans et al., "A 40 nm CMOS 0.4–6 GHz receiver resilient to out-of-band blockers," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1659–1671, Jul. 2011.
- [26] J. W. Park and B. Razavi, "Channel selection at RF using Miller band-pass filters," *IEEE J. Solid-State Circuits*, vol. 49, no. 12, pp. 3063–3078, Dec. 2014.
- [27] F. Lin, P.-I. Mak, and R. P. Martins, "An RF-to-BB-current-reuse wideband receiver with parallel N-path active/passive mixers and a single-MOS pole-zero LPF," *IEEE J. Solid-State Circuits*, vol. 49, no. 11, pp. 2547–2559, Nov. 2014.
- [28] C.-K. Luo, P. S. Gudem, and J. F. Buckwalter, "A 0.4–6-GHz 17-dBm B1dB 36-dBm IIP3 channel-selecting low-noise amplifier for SAW-less 3G/4G FDD diversity receivers," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 4, pp. 1110–1121, Apr. 2016.
- [29] L. Zhang, A. Natarajan, and H. Krishnaswamy, "Scalable spatial notch suppression in spatio-spectral-filtering MIMO receiver arrays for digital beamforming," *IEEE J. Solid-State Circuits*, vol. 51, no. 12, pp. 3152–3166, Dec. 2016.
- [30] G. Qi, P.-I. Mak, and R. P. Martins, "A 0.038-mm² SAW-less multiband transceiver using an N-path SC gain loop," *IEEE J. Solid-State Circuits*, vol. 52, no. 8, pp. 2055–2070, Aug. 2017.
- [31] G. Qi, B. van Liempd, P.-I. Mak, R. P. Martins, and J. Craninckx, "A SAW-less tunable RF front end for FDD and IBFD combining an electrical-balance duplexer and a switched-LC N-path LNA," *IEEE J. Solid-State Circuits*, vol. 53, no. 5, pp. 1431–1442, May 2018.
- [32] H. Wang, Z. Wang, and P. Heydari, "A wideband blocker-tolerant receiver with high-Q RF-input selectivity and <-80 dBm LO leakage," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2019, pp. 450–452.
- [33] H. Wang, Z. Wang, and P. Heydari, "An LO leakage suppression technique for blocker-tolerant wideband receivers with high-Q selectivity at RF input," *IEEE J. Solid-State Circuits*, vol. 56, no. 6, pp. 1682–1696, Jun. 2021
- [34] H. Razavi and B. Razavi, "A 0.4-6 GHz receiver for LTE and WiFi," in *Proc. Symp. VLSI Circuits*, Jun. 2021, pp. 1-2.
- [35] M. A. Montazerolghaem, L. C. N. de Vreede, and M. Babaie, "A 0.5–3 GHz receiver with a parallel preselect filter achieving 120 dB/dec channel selectivity and +28 dBm out-of-band IIP3," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Apr. 2022, pp. 11–12.
- [36] H. Razavi and B. Razavi, "A 0.4–6 GHz receiver for cellular and WiFi applications," *IEEE J. Solid-State Circuits*, vol. 57, no. 9, pp. 2640–2657, Sep. 2022.
- [37] M. A. Montazerolghaem, L. C. N. de Vreede, and M. Babaie, "A 300 MHz-BW, 27-to-38 dBm in-band OIP3 sub-7 GHz receiver for 5G local area base station applications," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, USA, Feb. 2023, pp. 292–294.
- [38] M. A. Montazerolghaem, L. C. N. de Vreede, and M. Babaie, "A highly linear receiver using parallel preselect filter for 5G microcell base station applications," *IEEE J. Solid-State Circuits*, vol. 58, no. 8, pp. 2157–2172, Aug. 2023.
- [39] Z. Lin, P.-I. Mak, and R. P. Martins, "Analysis and modeling of a gain-boosted N-path switched-capacitor bandpass filter," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 9, pp. 2560–2568, Sep. 2014.

- [40] J. Y. Kim and A. Liscidini, "A reconfigurable power-efficient quantized analog RF front-end with smart calibration," *IEEE Open J. Solid-State Circuits Soc.*, vol. 2, pp. 165–174, 2022.
- [41] M. A. Montazerolghaem, S. Pires, L. C. N. de Vreede, and M. Babaie, "A 3 dB-NF 160 MHz-RF-BW blocker-tolerant receiver with third-order filtering for 5G NR applications," in *IEEE Int. Solid-State Circuits Conf.* (ISSCC) Dig. Tech. Papers, Feb. 2021, pp. 98–100.
- [42] M. Darvishi, R. van der Zee, and B. Nauta, "Design of active N-path filters," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 2962–2976, Dec. 2013.
- [43] A. Ghaffari, E. A. M. Klumperink, and B. Nauta, "Tunable N-path notch filters for blocker suppression: Modeling and verification," *IEEE J. Solid-State Circuits*, vol. 48, no. 6, pp. 1370–1382, Jun. 2013.
- [44] I. Fabiano, M. Sosio, A. Liscidini, and R. Castello, "SAW-less analog front-end receivers for TDD and FDD," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3067–3079, Dec. 2013.
- [45] B. Razavi, "The transimpedance amplifier [a circuit for all seasons]," IEEE Solid State Circuits Mag., vol. 11, no. 1, pp. 10–97, Winter. 2019.
- [46] B. Razavi, Design of Analog CMOS Integrated Circuits. New York, NY, USA: McGraw-Hill, 2002.
- [47] D. Murphy et al., "A blocker-tolerant, noise-cancelling receiver suitable for wideband wireless applications," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 2943–2963, Dec. 2012.
- [48] X. He and H. Kundur, "A compact SAW-less multiband WCDMA/GPS receiver front-end with translational loop for input matching," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2011, pp. 372–374.
- [49] R. Chen and H. Hashemi, "A 0.5-to-3 GHz software-defined radio receiver using discrete-time RF signal processing," *IEEE J. Solid-State Circuits*, vol. 49, no. 5, pp. 1097–1111, May 2014.
- [50] R. Chen and H. Hashemi, "Reconfigurable receiver with radio-frequency current-mode complex signal processing supporting carrier aggregation," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 3032–3046, Dec. 2015.
- [51] B. Razavi, "The active inductor [a circuit for all seasons]," *IEEE Solid State Circuits Mag.*, vol. 12, no. 2, pp. 7–11, Spring 2020.
- [52] C.-M. Hung, R. B. Staszewski, N. Barton, M.-C. Lee, and D. Leipold, "A digitally controlled oscillator system for SAW-less transmitters in cellular handsets," *IEEE J. Solid-State Circuits*, vol. 41, no. 5, pp. 1160–1170, May 2006.
- [53] M. Babaie and R. B. Staszewski, "An ultra-low phase noise class-F 2 CMOS oscillator with 191 dBc/Hz FoM and long-term reliability," *IEEE J. Solid-State Circuits*, vol. 50, no. 3, pp. 679–692, Mar. 2015.
- [54] M. Babaie and R. B. Staszewski, "A study of RF oscillator reliability in nanoscale CMOS," in *Proc. Eur. Conf. Circuit Theory Design (ECCTD)*, Dresden, Germany, Sep. 2013, pp. 1–4.
- [55] D. Murphy, "Noise in large-signal, time-varying RF CMOS circuits: Theory and design," Ph.D. dissertation, Dept. Elect. Eng., Univ. California, Los Angeles, Los Angeles, CA, USA, 2012.
- [56] S. Pavan and E. Klumperink, "Analysis of the effect of source capacitance and inductance on N-path mixers and filters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 5, pp. 1469–1480, May 2018.
- [57] H. Hedayati, W. A. Lau, N. Kim, V. Aparin, and K. Entesari, "A 1.8 dB NF blocker-filtering noise-canceling wideband receiver with shared TIA in 40 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 50, no. 5, pp. 1148–1164, May 2015.
- [58] J. Musayev and A. Liscidini, "A quantized analog RF front end," *IEEE J. Solid-State Circuits*, vol. 54, no. 7, pp. 1929–1940, Jul. 2019.
- [59] B. Guo, H. Wang, L. Li, and W. Zhou, "A 65 nm CMOS current-mode receiver frontend with frequency-translational noise cancelation and 425 MHz IF bandwidth," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2023.



Mohammad Ali Montazerolghaem (Member, IEEE) received the B.Sc. degree in electrical engineering from the University of Isfahan, Isfahan, Iran, in 2012, and the M.Sc. degree in electrical engineering from the Amirkabir University of Technology, Tehran, Iran, in 2014. He is currently pursuing the Ph.D. degree with The Electronic Circuits and Architectures (ELCA) Research Group, Delft University of Technology, Delft, The Netherlands.

In 2022, he joined Renesas Electronics, 's-Hertogenbosch, The Netherlands, where he is currently a Senior RFIC Designer. His research interests include high-performance receivers for 5G cellular and base station applications.



Leo C. N. de Vreede (Senior Member, IEEE) received the Ph.D. degree (cum laude) from the Delft University of Technology, Delft, The Netherlands, in 1996.

In 1996, he was appointed as an Assistant Professor with the Delft University of Technology, working on the nonlinear distortion behavior of active devices. In 1999 and 2015, he was appointed, respectively, as an Associate Professor and a Full Professor where the Delft University of Technology, where he became responsible for the Electronic Research

Laboratory [ERL/The Electronic Circuits and Architectures (ELCA)]. During that period, he worked on solutions for improved linearity and RF performance at the device, circuit, and system levels. He is a Co-Founder/Advisor of Anteverta-mw B. V., Eindhoven, The Netherlands, a company that specializes in RF device characterization. He has authored or coauthored more than 150 IEEE-refereed conference papers and journal articles. He holds several patents. His current interests include RF measurement systems, RF technology optimization, and (digital-intensive) energy-efficient/wideband circuit/system concepts for wireless applications.

Dr. de Vreede was a recipient or co-recipient of the IEEE Microwave Prize in 2008, a Mentor of the Else Kooi Prize Awarded Ph.D. Work in 2010, and the Dow Energy Dissertation Prize Awarded Ph.D. Work in 2011. He was a recipient of the Technische Universiteit Delft (TUD) Entrepreneurial Scientist Award in 2015. He (co)guided several students who received the (Best) Paper Award from the Bipolar/BiCMOS Circuits and Technology Meeting (BCTM), the Program for Research on Integrated Systems and Circuits (PRORISC), the European Solid-State Circuits and Devices Conference (ESSDERC), the International Microwave Symposium (IMS), the Radio-Frequency Integration Technology (RFIT), and the Radio Frequency Integrated Circuits Symposium (RFIC).



Masoud Babaie (Senior Member, IEEE) received the B.Sc. degree (Hons.) from the Amirkabir University of Technology, Tehran, Iran, in 2004, the M.Sc. degree from the Sharif University of Technology, Tehran, in 2006, and the Ph.D. degree (cum laude) from the Delft University of Technology, Delft, The Netherlands, in 2016, all in electrical engineering.

From 2006 to 2011, he was with the Kavoshcom Research and Development Group, Tehran, where he was involved in designing wireless communication

systems. From 2014 to 2015, he was a Visiting Scholar Researcher with the Berkeley Wireless Research Center, Berkeley, CA, USA. In 2016, he joined the Delft University of Technology, where he is currently an Associate Professor. He has authored or coauthored one book, three book chapters, 11 patents, and more than 90 peer-reviewed technical articles. His research interests include RF/millimeter-wave integrated circuits and systems for wireless communications and cryogenic electronics for quantum computation.

Dr. Babaie was a co-recipient of the 2015–2016 IEEE Solid-State Circuits Society Pre-Doctoral Achievement Award, the 2019 IEEE International Solid-State Circuits Conference (ISSCC) Demonstration Session Certificate of Recognition, the 2020 IEEE ISSCC Jan Van Vessem Award for the Outstanding European Paper, the 2022 IEEE CICC Best Paper Award, and the 2023 IEEE IMS Best Student Paper Award (Second Place). He received the Veni Award from the Netherlands Organization for Scientific Research (NWO) in 2019. He is on the Technical Program Committee of the IEEE ISSCC. He also serves as the Co-Chair for the Emerging Computing Devices and Circuits Subcommittee of the IEEE European Solid-State Circuits Conference (ESSCIRC).