A 1.8-mW CMOS $\Sigma\Delta$ Modulator with Integrated Mixer for A/D Conversion of IF Signals

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***Abstract*—In this paper, the design of a continuous-time baseband sigma–delta ($\Sigma\Delta$) modulator with an integrated mixer for intermediate-frequency (IF) analog-to-digital conversion is presented. This highly linear IF $\Sigma\Delta$ modulator digitizes a GSM channel at intermediate frequencies up to 50 MHz. The sampling rate is not related to the input IF and is 13.0 MHz in this design. Power consumption is 1.8 mW from a 2.5-V supply. Measured dynamic range is 82 dB, and third-order intermodulation distortion is −84 dB for two −6-dBV IF input tones. Two modulators in quadrature configuration provide 200-kHz GSM bandwidth. Active area of a single IF $\Sigma\Delta$ modulator is 0.2 mm^2 in 0.35-μm CMOS.**

***Index Terms*—Analog–digital conversion, CMOS analog integrated circuits, continuous-time modulation, harmonic distortion, IF mixer, radio receivers, sigma–delta modulation.**

I. Introduction

INCREASING the level of integration in communication receivers is the subject of considerable research effort, as it involves reduction of complexity and cost. Integrating signal processing like narrow-band channel filtering, commonly performed by analog external filters, in the digital domain would be beneficial in the sense of both cost reduction and improvement of performance and accuracy. Realizing this higher level of integration introduces the challenge of pushing the analog-to-digital (A/D) converter performance towards higher resolution and higher frequencies.

Fig. 1 shows a block diagram of the traditional heterodyne receiver architecture. The desired channel is converted to baseband through several mixer stages and separated into in-phase (I) and quadrature (Q) components for image rejection. The I and Q signals are digitized by two baseband A/D converters. Alternatively, direct digitization of the channel at the intermediate frequency (IF) by a wide-band A/D converter [1] or a bandpass $\Sigma\Delta$ modulator [2]–[4] has become an important field of interest. Direct IF digitization with a wideband A/D converter has several advantages over baseband A/D conversion. Demodulation of I and Q components is done in the digital domain with perfect gain and phase matching. Also, IF A/D conversion is insensitive to dc offset and low frequency noise. An important disadvantage of a wide-band A/D converter is the high power consumption, as it provides high resolution in a large bandwidth. Also, dynamic range (DR) and linearity specifications are more difficult to meet at higher frequencies due to circuit nonidealities and parasitic effects. Using a bandpass $\Sigma\Delta$ modulator for IF digitizing is more efficient because high resolution is provided only in a small bandwidth at the IF. However, the oversampling of the IF, usually by a factor of four, and the need for a linear bandpass filter make the bandpass $\Sigma\Delta$ modulator rather power consuming in the case of a high IF. In [5], a receiver is presented that performs subsampling of the IF input signal in order to lower the sampling rate of the bandpass $\Sigma\Delta$ modulator.

Baseband $\Sigma\Delta$ modulation, performing high-resolution A/D conversion of baseband signals with relatively low bandwidths, is in particular suitable for use in communication applications like GSM receivers or AM/FM radio. An important property of a higher order baseband $\Sigma\Delta$ modulator is that it achieves high resolution at modest oversampling ratios [6] and low-power consumption. In this paper, the design of a baseband $\Sigma\Delta$ modulator with integrated mixer for IF digitization is presented (IF $\Sigma\Delta$ modulator). The mixer converts the IF input signal to baseband with high linearity, and the $\Sigma\Delta$ modulator performs the low-power, high-resolution A/D conversion. The mixer does not contribute to total power consumption. Moreover, the input IF and sampling frequency are not related, but can be chosen independently. This greatly extends the IF input range to frequencies measured up to 50 MHz, without affecting power consumption of the $\Sigma\Delta$ modulator.The dashed box in Fig. 1 shows the functional block diagram of the IF $\Sigma\Delta$ modulator. It replaces the IF mixer, anti-aliasing filter, and A/D converter. Two IF $\Sigma\Delta$ modulators are required for I and Q demodulation and I. The channel selection filter in front reduces dynamic range, linearity, and image rejection requirements for the modulators. Because of its multiple functions, the channel filter is a key element in the receiver architecture. An example filter response is shown in Fig. 2. The filter passes the desired channel band (200 kHz) and suppresses adjacent channels by 30 to 40 dB. In order to filter a 200-kHz channel bandwidth with high selectivity, external ceramic filters or surface-acoustic-wave (SAW) filters are used. As mentioned in the previous section, cost reduction of the receiver is achieved by a higher integration level. Therefore, on-chip integration of this external passive channel filter by means of active or digital filters is highly desired.

Section II describes the role of the channel filter in the receiver architecture. In Section III, the main system requirements are discussed. The design of the $\Sigma\Delta$ modulator with mixer is shown in Section IV. Important design aspects are highlighted in Section V. Measurement results are presented in Section VI, and conclusions are drawn in Section VII.

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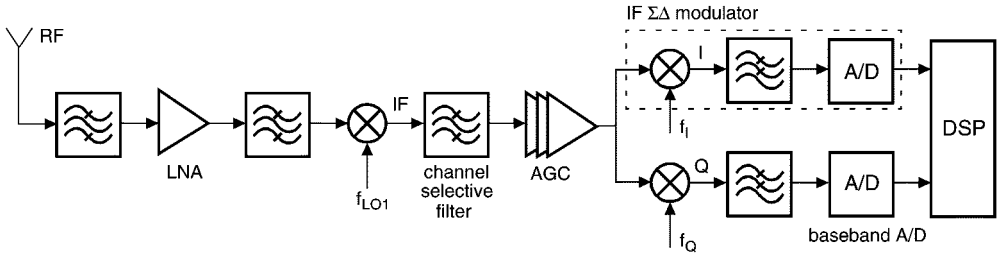


Fig. 1. Traditional heterodyne receiver architecture.

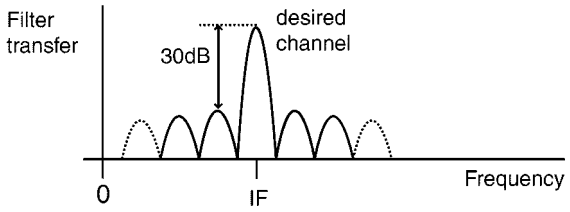


Fig. 2. Typical channel filter frequency response.

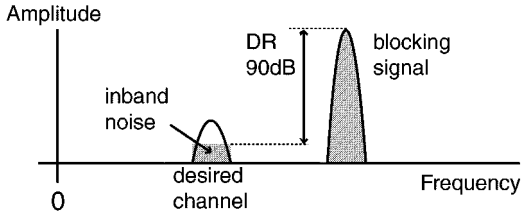


Fig. 3. Dynamic range requirement.

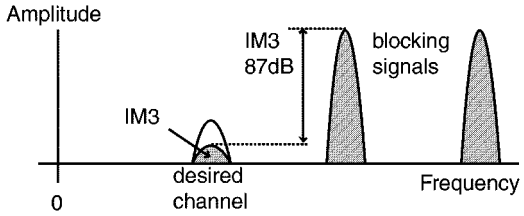


Fig. 4. Third-order intermodulation requirement.

II. Channel Filtering

An integrated higher order active filter can be designed by cascading several transconductance-C filter sections [7]. However, severe dynamic range, bandwidth, and linearity requirements apply to the active filter, as it has to handle the full unfiltered IF signal spectrum. A considerable amount of power will be needed for such a high-performance filter. Moreover, due to parasitics and process variations, only a limited quality factor is achievable. Special tuning techniques have been reported to push the quality factor to higher values [7], [8]. Still, the selectivity of an active filter is not sufficient yet for radio applications.

Alternatively, a digital filter can be designed with superb selectivity, linearity, and accuracy. However, without analog narrow-band filtering, the automatic gain control, mixer, and A/D converter must be capable of handling the full dynamic range and bandwidth of the received signal.

Thus, analog integration of the channel filter requires a high-performance active channel filter, while a high-performance A/D converter is required in case of digital integration of the channel filter. Because the feasibility of either analog or digital channel filter integration has not been shown yet, especially for low-power consumption, the traditional architecture of Fig. 1 with an external analog channel filter is still widely used in today's receivers. Great effort is made at optimizing the A/D converter for one or more of the specifications described above. The design in this paper has been optimized for large dynamic range, high linearity, and low-power consumption. In the next section, these requirements are discussed in more detail.

III. System Requirements

The design of the modulator in this paper was intended for use in GSM-based receivers. The specifications have been defined at the input of the channel filter.

A. Dynamic Range

The dynamic range requirement at the channel filter input has been indicated in Fig. 3. The minimum power of a desired GSM channel at the antenna of the receiver is specified to be −104 dBm. To have sufficiently low bit error rate, the required signal-to-(noise + distortion) ratio (SNDR) is 9 dB. This implies that power of total in-band noise and distortion should be as low as −113 dBm. Total power of the adjacent interference channels in the GSM band can be up to −23 dBm, resulting in a dynamic range of 90 dB.

B. Linearity

The linearity specification is also determined by out-of-band blocking power. Third-order intermodulation distortion (IM3) for two maximum blocking signals of −26 dBm should be 87 dB below the signal carriers (Fig. 4). This is required in order to meet the 9-dB SNDR at minimum input power of the desired channel. Thus, third-order intermodulation at the input of the channel filter should be not stronger than −87 dB.

C. Image Rejection

The image rejection requirement depends on the topology. In the zero-IF topology, the GSM channel is directly converted to dc. Image rejection requirements are relaxed because the desired channel and the image channel are essentially the same, and

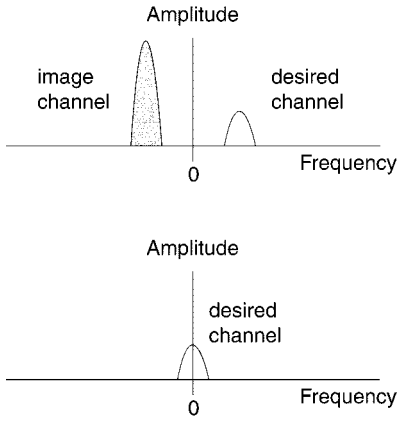


Fig. 5. (a) Low IF conversion. (b) Zero IF conversion.

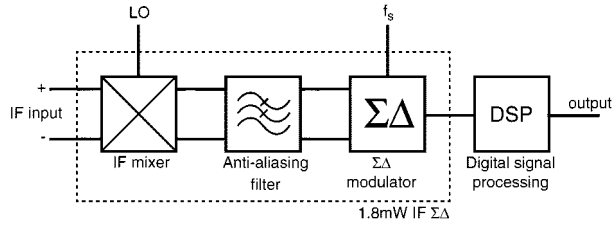


Fig. 6. A/D converter topology.

25 dB of image rejection is sufficient for many applications [9], [10]. Enough rejection of the image channel is obtained by I and Q demodulation. Consequently, zero IF conversion does not introduce the need for a filter for image rejection.

An alternative method is to convert the channel at IF to a low offset frequency (low-IF topology). In this case, the image channel and desired channel are not related, and the image signal can be much stronger than the desired signal (Fig. 5). Depending on the radio standard, this may result in a severe image rejection requirement in the order of 80 dB. This is achieved by a combination of channel filtering (30–40 dB) and I and Q demodulation (40 dB).

In the case of GSM application, there are guaranteed holes in the receive spectrum, and image rejection requirements are much reduced if such a hole is chosen as the image signal [9].

If the A/D converter reaches these requirements closely, channel filter specifications become more relaxed and a lower cost channel filter can be used. Obviously, there would be no need for an external channel filter if the A/D converter meets all requirements. In that case, channel filtering can be done in the digital domain.

IV. IF ΣΔ Modulator Design

A. Topology

The IF A/D converter topology is shown in Fig. 6 [11]. The IF input is in the 10–100-MHz range or up to a few hundreds of megahertz. The IF channel is converted down to baseband by the mixer and filtered by an anti-aliasing filter. A baseband A/D converter digitizes the low-frequency channel. In order for this topology to be widely applicable, the local oscillator (LO) frequency must be in the same input IF 10–100-MHz range.

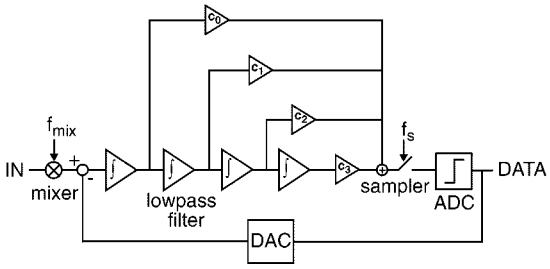


Fig. 7. IF ΣΔ modulator block diagram.

For portable applications, low-power consumption is mandatory. Therefore, the LO frequency should be independent of the ΣΔ sampling frequency f_s to avoid excessive values for the sampling frequency in case the input IF is high.

Fig. 7 shows the IF ΣΔ modulator block diagram. The mixer is placed at the input of the modulator, followed by a fourth-order low-pass anti-aliasing filter. The output of the filter is sampled at frequency f_s and digitized by a 1-bit comparator. The bitstream output of the comparator is fed back through digital-to-analog (D/A) conversion and subtracted from the analog mixer output. The feedback path forms the continuous-time baseband ΣΔ modulator loop. The feedforward paths in the loop filter are needed for high-frequency stability of the modulator [12].

This architecture has some important features. The mixing frequency and sampling frequency are not related and can be chosen independently. This is important for both flexibility and power consumption of the ΣΔ modulator in particular for receiver architectures with a high input IF. The local oscillator frequency is equal to the input IF, while the sampling frequency is determined by the dynamic range and bandwidth requirements of the baseband signal. The sampling frequency is set to the lowest possible value to minimize power consumption. The mixer does not contribute to the power consumption, as will be shown in the next section. Last, the loop filter of the ΣΔ modulator acts as an anti-aliasing filter as well.

B. Implementation

An RC integrator implementation is used for the first filter stage, which is an op-amp with integration capacitors C_i in negative feedback (Fig. 8) [13]. The input resistors $R_{\rm in}$ and D/A converter (DAC) feedback resistors $R_{\rm DAC}$ are connected to the input nodes of the op-amp and convert the input and DAC reference feedback voltages into currents. A passive mixer is implemented with two differential current switching pairs. The complementary clock phases φ_1 and φ_2 periodically couple and cross-couple the differential input current. Due to the mixing, the input signal amplitude is reduced by 4 dB. Highly linear mixing is achieved by placing the mixer at the op-amp virtual ground nodes. Then, the nonlinear channel resistance of a mixer switch is only modulated by a fraction of the input voltage. The DAC feedback resistors are connected to the output of the mixer therefore placing the mixer outside the ΣΔ loop. The error current flows into the integration capacitors and generates a voltage output. The output voltage of the first integrator is connected to the next filter stage with voltage input. The higher order filter stages are all transconductance-C integrators. The feedforward paths are implemented as transconductance amplifiers.

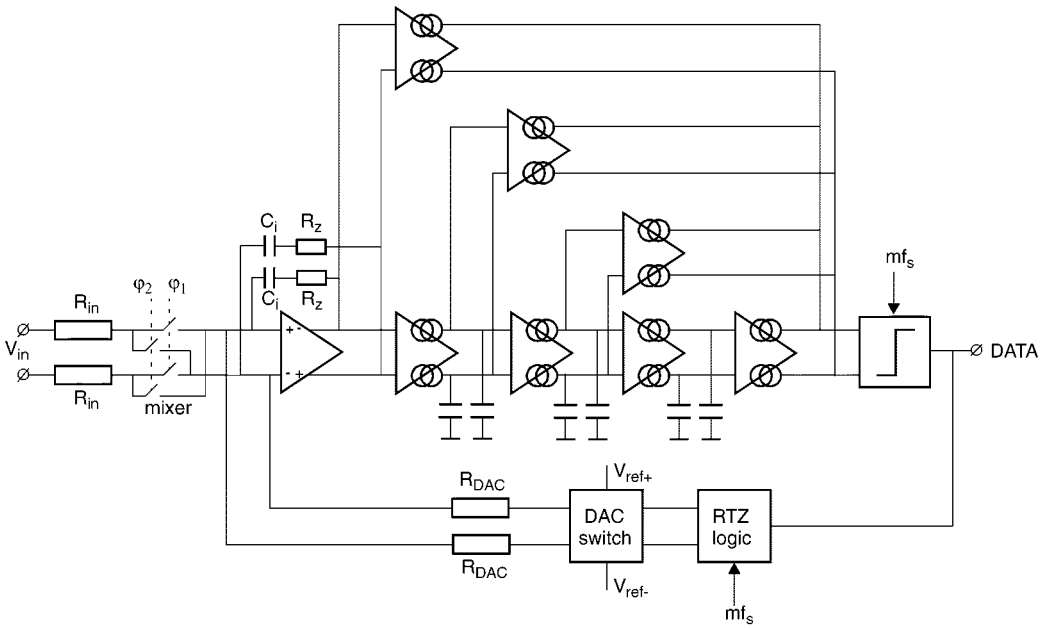


Fig. 8. Implementation of fourth-order ΣΔ modulator with mixer.

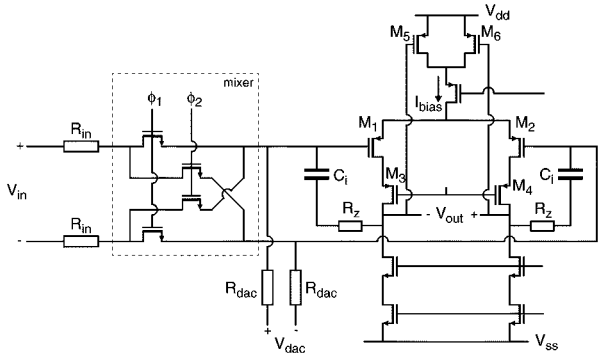


Fig. 9. Mixer and op-amp circuit.

The output current signals of the feedforward paths are connected together and fed into the current input of the comparator. The digital output of the comparator is fed into a one-bit D/A converter with a periodic return-to-zero interval in order to avoid intersymbol interference [14]. The D/A converter switches connect the feedback resistors to the positive or negative reference voltage. During the return-to-zero interval, the feedback resistors are connected to a zero reference voltage.

C. Input Stage Design

In this design, the first filter stage dominantly determines system noise and distortion performance. The design of the first stage is shown in Fig. 9. For speed reasons NMOS transistors have been used for implementation of the mixer. The ON-resistance of each switch is small relative to the input resistance. Therefore, the switches are modulated by a small fraction of the input voltage only. The input stage of the op-amp is a differential PMOS pair (M_1, M_2) with cascade transistors (M_3, M_4) to increase gain. The upper PMOS transistors (M_5, M_6) are biased in the linear region and the gates control the common-mode

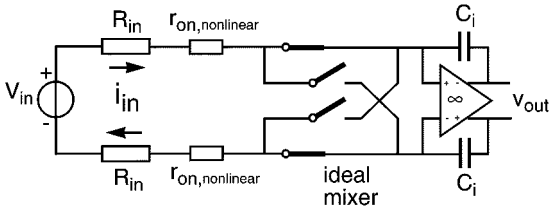


Fig. 10. Nonlinear mixer model.

output voltage of the op-amp. Small resistors R_z are placed in series with the integration capacitors to compensate for the right-half-plane zero of the integrator.

Noise performance of the input stage is dominantly determined by the thermal noise of the input and DAC resistors. Having finite gain, the input PMOS transistors M_1, M_2 produce harmonic distortion. These transistors are biased with relatively high currents (210 μA each) to achieve good linearity.

V. Performance Aspects

A. Mixer Nonlinearity

For first-order approximation of the nonlinear mixer behavior, the simple model of Fig. 10 has been used. If driven by perfect complementary clock phases, always one pair of switches is conducting and the mixer is simply modeled by two nonlinear switch ON-impedances $r_{\rm on}$ and four ideal switches. The current through a transistor operating in the linear region is given by [15]

$$I_D = \mu_n C_{\rm ox} \frac{W}{L} \left(v_{\rm gs} - V_T - \frac{v_{\rm ds}}{2} \right) v_{\rm ds} \qquad (1)$$

where μ_n is the mobility, $C_{\rm ox}$ the oxide capacitance, W and L the transistor dimensions, $v_{\rm gs}$ the gate-source voltage, V_T the

TABLE I
MIXER SWITCH DESIGN PARAMETERS

V_{in}	$3V_{pp}$
V_{GT}	0.5V
R_{on}	2kΩ
R_{in}	70kΩ
HD3	-94dB

threshold voltage, and $v_{\rm ds}$ the drain-source voltage. The conductance of the switch is calculated by differentiating (1)

$$\frac{\partial I_d}{\partial v_{\rm ds}} = \mu_n C_{\rm ox}\frac{W}{L}(v_{\rm gs} - V_T - v_{\rm ds}) = \frac{1}{r_{\rm on}}. \tag{2}$$

From Fig. 10, the input current through a switch is calculated

$$I_D = \frac{1}{R_{\rm in} + r_{\rm on}} \cdot \frac{V_{\rm in}}{2}. \tag{3}$$

It has been assumed that the input nodes of the op-amp are perfect virtual ground nodes. Substitution of (1) and (2) into (3) and Taylor series expansion yields an expression for the third-harmonic distortion HD3

$$\text{HD3} = \frac{3}{32} \cdot \left(\frac{V_{\rm in}}{v_{\rm gs} - V_T}\right)^2 \cdot \left(\frac{r_{\rm on}}{R_{\rm in}}\right)^3. \tag{4}$$

In this analysis, matching between the differential paths is considered to be perfect (no even-order harmonic distortion). From (4), it can be concluded that good linearity is achieved if the switches have low ON-impedance and a high overdrive voltage $(v_{\rm gs} - V_T)$. Table I shows some relevant parameters for the design in this paper. Substituting these parameters into (4) gives a first-order estimation of −94-dB HD3 produced by the mixer, which shows that high linearity is achievable with this architecture.

B. Op-Amp Nonlinearity

Distortion analysis of the first op-amp is more complicated, as it is introduced within the ΣΔ loop. In [16], an analysis is given to calculate distortion of the ΣΔ modulator due to nonlinearity of the first opamp. Third-harmonic distortion is estimated by (strong inversion)

$$\text{HD3} \approx \frac{V_{\rm gt} \cdot V_{\rm in}^2}{128(I_D \cdot R_{\rm in})^3} \cdot \left(1 + \frac{R_{\rm in}}{R_{\rm DAC}}\right) \tag{5}$$

where $V_{\rm gt}$ is the overdrive voltage $(v_{\rm gs} - V_T)$. It has been assumed that the impedance of a mixer switch is much smaller than the input resistance. A simple design strategy is derived from (5). The input transistors are biased in moderate inversion to have a low $V_{\rm gt}$. Furthermore, the values of the input resistors $R_{\rm in}$ and feedback resistors $R_{\rm DAC}$ are large (limited by thermal noise contribution). From (5), the biasing current I_d can be estimated for a certain distortion requirement. Table II shows the parameters used for this design. According to (5), third-harmonic distortion due to op-amp nonlinearity is expected to be below −100 dB.

TABLE II
DESIGN PARAMETERS OF THE INPUT FILTER STAGE

V_{dd}	2.5V
G_m	3.4mA/V
I_d	210μA
V_{in}	1.875V
R_{in}	70kΩ
R_{dac}	33kΩ
HD3	-105dB

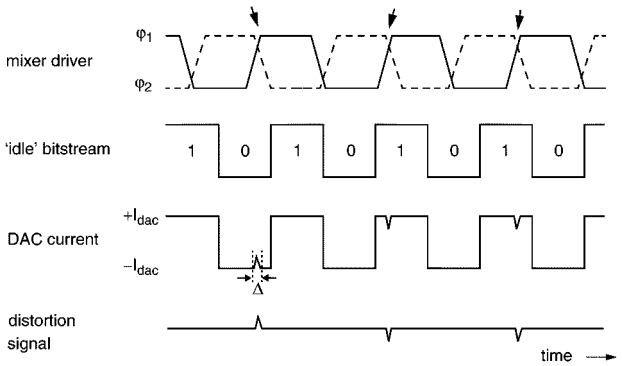


Fig. 11. Mixer LO overlapping clock driver (time domain).

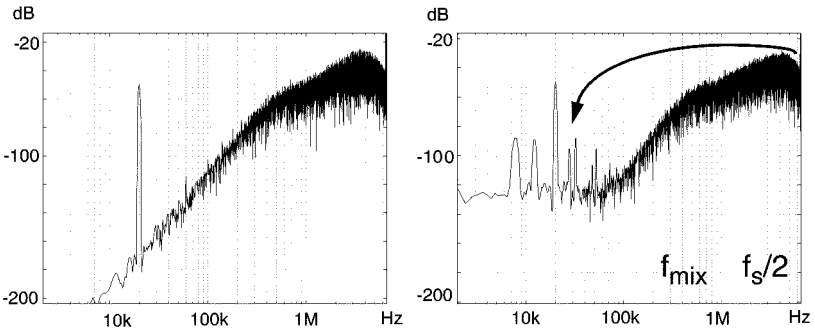
C. Mixer LO Driver

Another important aspect related to the performance is the local-oscillator clock scheme that drives the mixer. As mentioned earlier, the mixer is ideally driven by perfect complementary clock phases. A simple implementation providing complementary phases is a single inverter stage. However, due to the delay of the inverter, the output signal is slightly shifted in phase. As a consequence, both clock phases may be overlapping (high) for a short time interval. If both clock phases are high, all switches are conducting at the same time, and a low impedance path exists between the input nodes of the op-amp. Due to the short-circuit path, the differential feedback DAC current is distorted. This is shown in the time domain in Fig. 11 for the case where the LO frequency and sampling frequency are not equal.

The upper plot shows the mixer local oscillator with overlapping phases. Without an input signal present, the ΣΔ modulator produces an idle 1-0 bitstream pattern and the DAC feedback current toggles between the positive and negative reference values. At the moment of overlap, the DAC current is distorted and the frequency of this distortion signal equals

$$f_{\rm dist} = f_{\rm DAC} - f_{\rm LO} \tag{6}$$

being the difference between the frequency of the DAC feedback signal and the local oscillator. This effect has been verified by simulation. In simulation, the mixer is operating at half the sampling frequency (6.5 MHz), and a 6.52-MHz input signal is downconverted to 20 kHz. Fig. 12(a) shows the simulated bitstream spectrum when the mixer is driven by perfect complementary LO clock phases. Clearly, the fourth-order noise shaping is visible within the signal band. Fig. 12(b) shows the simulated spectrum if the mixer is driven by overlapping LO



(a) (b)

Fig. 12. Simulated bitstream spectrum of IF ΣΔ modulator with (a) ideal mixer and (b) overlapping clock phases.

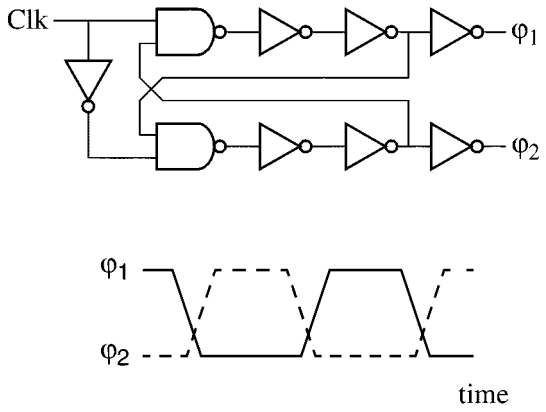


Fig. 13. Nonoverlapping clock generator.

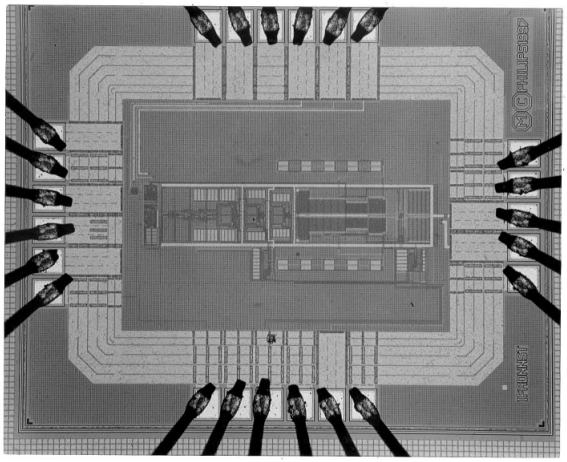


Fig. 14. Test chip micrograph.

clock phases. The in-band noise level has been raised and some discrete peaks can be observed. This is high-frequency quantization noise present in the bitstream spectrum at the LO frequency's leaking into baseband due to the nonideal mixing.

This effect of quantization noise "leakage" is much less severe if the local oscillator frequency is equal to the sampling frequency. Due to the noise-shaping characteristic, quantization noise power at the sampling frequency is very low. However, the most flexible way to solve the problem of leakage is the use of nonoverlapping LO clock phases. Fig. 13 shows a simple circuit that has been used to generate nonoverlapping clock phases.

VI. Experimental Results

The IF ΣΔ modulator has been realized in a 0.35-μm standard CMOS process. The chip micrograph is shown in Fig. 14. The active area is 0.2 mm^2. The resistors are implemented in polysilicon. The floating capacitors of the first integrator stage are metal-to-metal sandwich devices. Gate-oxide capacitors have been used for the other filter stages [12]. All measurements described below have been taken at 2.5-V supply voltage.

First, dynamic range of the ΣΔ modulator has been measured (mixer turned off). This was done by connecting one pair of the mixer switches to ground and the other pair to the supply voltage. A 10-kHz test signal has been applied to the input. Fig. 15 shows the measured SNDR of the output bitstream spectrum of the modulator for different input levels. The measured

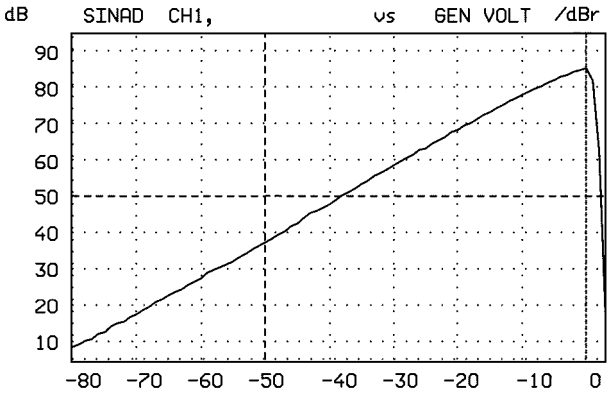


Fig. 15. Measured SNDR as function of applied input level (mixer off).

DR is 86 dB. At 0 dBFS (full-scale input is 1.3-V_{rms} differential), the SNDR is 84 dB. For signals larger than 0 dBFS, the system is stable but overloaded and the performance is degraded. The next measurements have been done with the mixer turned on. The resolution bandwidth of all measured spectra is 36 Hz. Fig. 16 shows the bitstream output spectrum from 0 to 100 kHz. A −28-dBFS, 13.02-MHz signal is applied to the input. The mixer is operating at 13.0 MHz and converts the input tone to 20 kHz. Due to the passive mixing of a sinusoidal input signal and the square LO waveform, the downconverted frequency component of interest $(f_{in} - f_{LO})$ is suppressed by

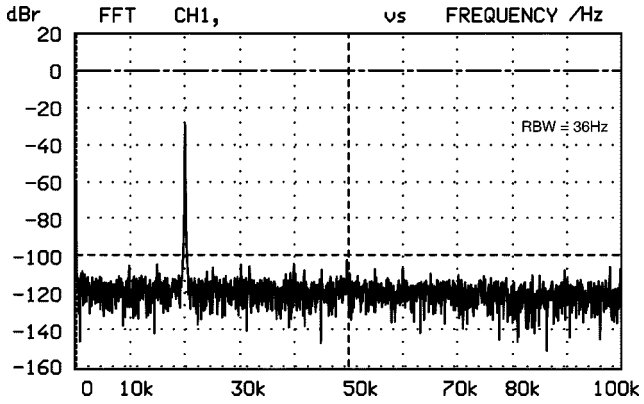


Fig. 16. Measured output spectrum.

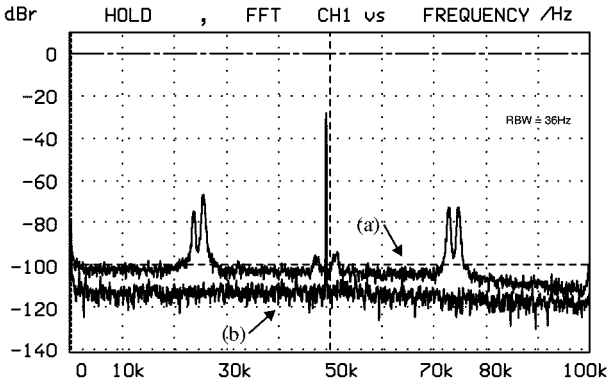


Fig. 17. Measured output spectrum of IF $\Sigma\Delta$ modulator with (a) overlapping LO clock phases and (b) non-overlapping clock phases.

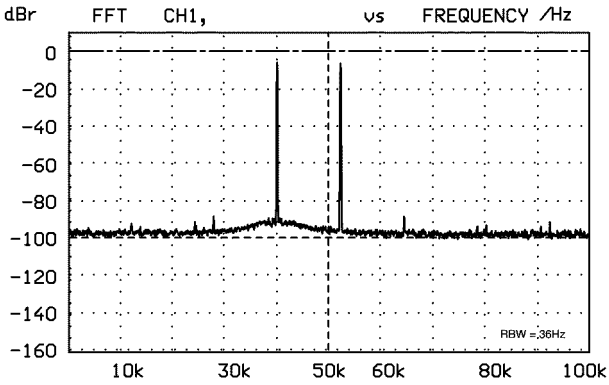


Fig. 18. Output spectrum for IP3 measurement.

TABLE III
OVERVIEW OF MEASURED PERFORMANCE

Technology	0.35μm CMOS (1PS 5AL)
Active area	$0.2mm^2$
Supply voltage	2.5V
Power consumption	1.8mW
Sampling frequency	13.0MHz
Bandwidth	100kHz
Input amplitude	$1.3V_{rms}$
Local oscillator frequency	0-50MHz
SNR	82dB
IM3	-84dB
IP3	+36dBV

4 dB. Therefore, the maximum input signal amplitude is 4 dB larger compared to the maximum input of the $\Sigma\Delta$ modulator without the mixer. In order to have the same maximum input amplitude, the DAC reference voltage of the IF $\Sigma\Delta$ modulator has been scaled down by 4 dB. The measured DR of the modulator with mixer is 82 dB. Fig. 17(a) shows the output spectrum with a -30-dBFS signal at 49 kHz originating from a 6.549-MHz input signal and the mixer operating at 6.5 MHz. The mixer is driven by overlapping clock phases. Some large discrete peaks can be observed as expected from simulation results. Fig. 17(b) shows the same measurement if the mixer is driven by nonoverlapping clock phases. The noise floor has dropped by more than 10 dB and the spectrum is flat without large discrete peaks. This experiment shows that nonoverlapping clock phases prevent significant leakage of quantization noise, which is present at the LO frequency, into baseband.

Linearity of the mixer and modulator was measured by applying two -6-dBV input tones at 13.040 and 13.052 MHz. The mixer operating at 13.0 MHz converts the input tones to 40 and 52 kHz, respectively. Fig. 18 shows the bitstream output spectrum. Third-order intermodulation distortion components can be found at 28 and 64 kHz and are 84-dB below the signal carriers. The third-order intercept point (IP3) is at $+36$ dBV. The noise that can be observed around the 40-kHz carrier is phase noise from the 13.040-MHz signal generator. Due to the limited dynamic range of the measurement equipment, the noise floor of Fig. 18 is higher than in the previous figures.

The mixer frequency can ranged from 0 to 50 MHz. The limitation was the external circuit that provided the nonoverlapping clock phases. This circuit was not integrated on chip for experimental purposes. Power consumption of a single IF $\Sigma\Delta$ modulator is 1.8 mW from a 2.5-V supply. Half of the power is consumed by the first filter stage, while power consumption of the mixer is negligible. The measured performance has been summarized in Table III.

VII. CONCLUSION

Research efforts pushing toward digital integration of the channel filter in radio receivers have introduced the need for high-performance A/D converters, operating at higher frequencies with a large dynamic range and high linearity. An integrated design of a $\Sigma\Delta$ modulator and an IF mixer for IF A/D conversion has been presented. The resulting IF $\Sigma\Delta$ modulator has some important features. The input IF can be chosen independently and can be much higher than the sampling frequency if necessary. This is different from a bandpass $\Sigma\Delta$ modulator that needs a sampling rate that is higher than the input IF.

Power consumption is low (1.8 mW) as a result of combining a passive mixer and a baseband continuous-time $\Sigma\Delta$ modulator. High linearity has been achieved, and the IP3 is measured to be $+36$ dBV. The chip as described in this paper is designed for use in GSM-based receivers and provides 100-kHz (single modulator) signal bandwidth at a 13.0-MHz sampling frequency. Two

IF ΣΔ modulators in quadrature configuration provide 82 dB of dynamic range in 200-kHz GSM bandwidth while consuming only 3.6 mW.

The linearity and dynamic range specifications of the measured prototype chip are closely reaching the GSM requirements before channel filtering. This implies that requirements for the channel filter in front of the A/D converter are relaxed. Pushing the A/D converter to even higher performance may result in on-chip digital integration of the channel filter in the future.

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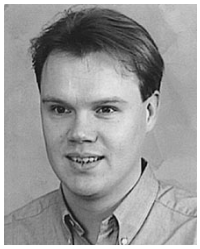

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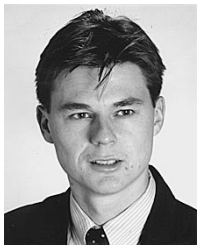

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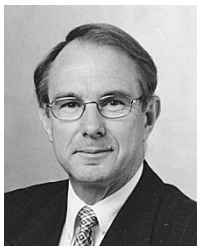

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