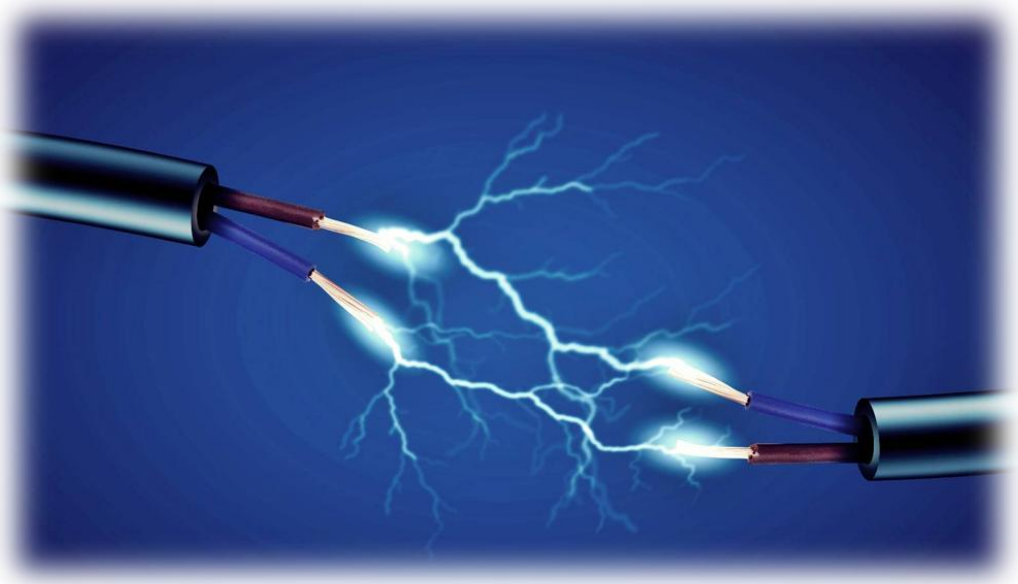
Control and Protection of VSC-based Multi-terminal DC Networks



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Control and Protection of VSC-based Multi-terminal DC Networks

THESIS

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by

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Abstract

The increasing global energy needs and the high integration of renewable energy generation have changed the requirements for the electricity grid. Countries are becoming unable to cover their energy demands with their own means and the need for power exchange between neighboring countries has increased. Consequently, power needs to be transmitted over longer distances and multi-terminal complex grids need to be created to facilitate the energy evolution.

Contrary to the existing AC grids, HVDC is an appealing alternative for future grids. VSC technology has been the focus of recent HVDC research due to its inherent advantages. However, the use of fully-controllable switches becomes a disadvantage in case of DC contingencies. Thus far, opening the AC breakers has been the only way to clear DC faults, by completely de-energising the system and interrupting the power transfer with significant economic and societal consequences. Other protection concepts include multi-level converters with full-bridge submodules, which are able to limit the fault current; and control methods which identify the faulty lines. However, DC switch breakers are necessary to isolate the faulty line from the network, allowing normal operation to be resumed.

The main contributions of this thesis are the comparison of different grid operating topologies under fault cases; and the impact analysis of different current limiting measures and control strategies on the developing DC fault currents. A four-terminal grid in radial configuration was simulated using Matlab/Simulink®, and the natural fault response of the stations in most common HVDC grid topologies was studied. Additionally, two selective fault detection methods are proposed, which take into account the current direction on DC lines and the rate of rise of the fault currents. Four DC breaker technologies were simulated for all analysed grid topologies, and compared on the basis of the total DC fault interruption time and their influence on the system post-fault coordination and operation restoration.

With the concepts analysed in this thesis, MTDC network system designers will be able to understand and tackle DC contingencies to facilitate an uninterruptible power flow between the different interconnected AC grids.

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List of Acronyms

Acronym	Description
AC	Alternating Current
CSC	Current-Source Converter
DC	Direct Current
EMF	Electro-Magnetic Field
GCT	Gate-Commutated Thyristor
GTO	Gate Turn-off Thyristor
HVAC	High Voltage Alternating Current
HVDC	High Voltage Direct Current
ICC	Inner Current Converter
IGBT	Insulated Gate Bipolar Transistor
KVL	Kirchhoff's Voltage Law
LCC	Line-Commutated Converter
LV	Low Voltage
MMC/M2C	Multi-Level Converter
MTDC	Multi-Terminal Direct Current
MV	Medium Voltage
PCC	Point of Common Coupling
PI	Proportional-Integral
PLL	Phase-Locked Loop
PTC	Positive Temperature Coefficient
PWM	Power Width Modulation
SVPWM	Space-Vector Pulse Width Modulation
SCR	Short-Circuit Ratio
THD	Total Harmonic Distortion
TIF	Telephone Influence Factor
UFS	Ultra Fast Switches
VCO	Voltage-Controlled Oscillator
VSC	Voltage-Source Converter

Chapter 1

Introduction

1.1 Motivation

The changes in the global energy status quo and the grid penetration of a constantly increasing amount of renewable energy sources have affected the shape of the electricity grid. The distance between consumption and generation has increased significantly and it is expected to increase even more in the coming years, upgrading the role of the transmission system to a critical factor for the future grid configuration [1]. This is additionally corroborated by the increasing energy exchange between countries.

Many countries with a traditional energy mix, based on various forms of coal or oil, are forced by international treaties, such as the Kyoto Protocol or the 20-20-20 goals in Europe, to reduce their energy dependence on fossil fuels and to introduce a more sustainable way to cover their energy needs. By creating energy pathways between countries and by interconnecting the national grids, sustainability goals can be achieved more easily and intermittency problems of renewable sources can be tackled. However, there are technological issues related to the transmission system that need to be resolved in order to materialize the vision of a transnational grid.

The traditional AC grid utilizes alternating voltage with a frequency of 50 or 60 Hz. Depending on the power that needs to be transmitted and the transmission distance, the level of the chosen AC voltage varies. For applications where high power needs to be transmitted over long distances, high-voltage alternating current (HVAC) is implemented. A main disadvantage resulting from HVAC is the high transmission losses and limited transmission distance. The resistance of AC cables is higher than for DC cables, due to the skin effect and proximity which cause higher losses [2]. Moreover, reactive power cannot be avoided when using alternating current and reactive power compensation is necessary, specially for long transmission distances, at different points of the AC lines. Consequently, the focus of the present research is turned to the DC transmission systems.

High-voltage DC (HVDC) was first commercially used in 1954 for the connection of the Gotland island to the mainland of Sweden. The development of high voltage components, as well as the inherent advantages of HVDC over HVAC have made it an appealing and economically viable transmission option for long distances.

The classic HVDC transmission systems are based on current source converters (CSC). These converters, also known as line commutated converters (LCC), make use of thyristor valves, which switch with the frequency of the AC grid. Their low switching frequency results in low converter switching losses, while the required filter size is high. Moreover, they are able to handle DC contingencies, as they do not allow the AC grid to feed the DC side fault, once the thyristors are blocked.

However, their main drawback is their low controllability, which is an inherent characteristic of thyristor valves, and the difficulties in creating a DC grid using this technology. As a natural consequence, research has recently focused on voltage-source converters (VSC) for the transmission applications [3].

VSC-HVDC converters utilize insulated gate bipolar transistors (IGBT), which are controlled with pulse width modulation (PWM) controllers. The use of fully controllable switches allows to independently control the converter active and reactive power, as well as DC voltage and AC voltage; the latter in case of connection to a weak AC grid. In this way, the power quality is enhanced and the realization of multi-terminal HVDC networks is theoretically easier, as low coordination among the VSCs is required. Due to the isolation of the DC network from the AC grid, the connection of AC grids with different operating frequencies can also be realized.

Although the use of VSC-HVDC converters seems to be more advantageous than the other technologies (HVAC, LCC-HVDC), its major drawback results from the use of IGBT valves. In case of a DC fault, the blocking of IGBTs does not prevent the AC grid from feeding the fault via the anti-parallel diodes of the switches. Except for the AC breakers, already in use for years in AC transmission systems, there was no commercially available DC breaker for the protection of DC systems, at the time this thesis was written. Consequently, the main focus of the HVDC industry, among other proposed protection schemes, is on the design of DC breakers, which will be able to isolate the fault as fast as possible and at the same time will exhibit the lowest possible power losses during normal operation. So far, ABB [4] and Alstom [5] have announced prototype DC breakers designed in their labs, but they are yet to be proof-tested in commercial use.

1.2 Research Questions

The key research questions this thesis addresses are:

- Which are the development stages of the DC fault currents?
- Which are the fault current contributions in different HVDC grid topologies?
- What is the maximum time a network has to isolate the fault, before the interconnected VSCs are damaged?
- By what means can different DC breaker technologies handle a fault?
- Which other measures need to be taken in order to achieve an early fault detection and isolation?

As already mentioned in section 1.1, the major problem of VSCs is their inability to isolate the AC side from the DC grid, in order to protect themselves and the network from the DC fault currents. Therefore, the first objective of this thesis is to identify the stages in which a DC fault develops and compare the fault current contributions for the most common HVDC grid configurations. By defining the DC fault stages, the time the VSC valves can survive an overcurrent and thus the time the protection measures have to act, before a converter damage occurs, can be determined. As a benchmark for the work, a radial configuration of four VSC stations is simulated using the Matlab/Simulink environment.

The second main goal of this thesis is to study the impact of different DC breaker technologies, proposed in literature, on the protection scheme of a VSC-HVDC network. For this purpose, two fault detection methods, used by the respective controllers of the DC breakers, were implemented. Moreover, the study focuses on other technological options that can be used alongside DC breakers to limit the peak fault currents and prevent a power transfer interruption.

1.3 Contributions

The major contribution of this thesis is the comparison of different grid operating topologies in terms of DC fault development, which seems to be lacking in the literature. The impact of the converter arrangement on the DC fault protection scheme is essential when designing an HVDC network. Therefore, the thesis investigates the system power transfer capability after a fault occurrence and the role of the DC grounding in the fault developing stages.

Another contribution is the impact analysis of different limiting reactor sizes on the developing DC fault currents. This study can aid system designers in selecting the DC reactor size, considering its effect to the normal operation of the system and the grid fault response.

Additionally, this thesis proposes two fast fault detection methods, based on the post-fault system characteristics, which are compared for all proposed grid configurations. These methods are implemented in the DC breaker controllers and aim at selectively isolating the faulty line and allowing the system an uninterrupted operation.

Finally, a comparison of different theoretical DC breaker models is made and the influence of the breaker technology is investigated on the system post-fault coordination and operation restoration for all analysed grid topologies. Different breaker technologies have different interruption times, influencing subsequently the system behaviour. Therefore the thesis studies the network pre- and post-fault state and evaluates the performance of the implemented protection methods.

1.4 Thesis Outline

To answer the research questions and meet the objectives, the thesis is structured as follows: Chapter 2 presents a typical VSC station layout and its main components. The equivalent model of the VSC is described and the converter controllers are analysed in detail. Finally,

an overview of operating topologies for multi-terminal HVDC networks is introduced and the Simulink cable models are compared for the simulation of the HVDC lines.

Chapter 3 presents the different DC fault types and a detailed theoretical analysis of fault development for a symmetric monopolar station. This analysis is succeeded by the presentation of a VSC average simulation model. The limitations of the average model on DC faults studying are discussed and a switched model is proposed as an alternative. This model is subsequently used for all simulations in this thesis. The chapter concludes with a summary and comparison of DC breaker technologies, proposed in literature.

Chapter 4 addresses other technologies and control methods employed for the protection of HVDC networks from DC contingencies. The first part of the chapter gives an overview of three-level VSC technologies and commercially available modular multi-level converters, which are the recent trend in HVDC systems. The working principles of these technologies are described and their DC fault response is analysed. The second part deals with a proposed control method, referred to as the Handshaking Method, which uses a combination of AC breakers and fast DC mechanical switches, for fast detecting and isolating the faulty line and restoring the system operation.

In Chapter 5, the bipolar grid configuration with metallic return is investigated based on its fault response. At first, different case studies are established for the evaluation of the system performance during normal operation and under fault circumstances. Then, the role of the fault location is studied and the contributions of the different system components to the fault current are monitored for each fault case. At a next stage, the effect of the different limiting reactor sizes on the fault current peak value and on its rate of rise is studied. Furthermore, two DC fault detection methods are developed and compared for each specific HVDC grid topology. Based on the topology, the best method is selected and implemented on the DC breaker controllers. Finally, different DC breaker models are simulated in combination with DC side limiting reactors, to investigate their effect on the system fault response.

Chapter 6 follows the principles of Chapter 5 and the determined DC fault cases are applied to four other possible HVDC grid topologies. Conclusions are drawn for the fault current contributions, the most appropriate selective fault detection method is indicated and the combination of DC breaker technology and limiting reactors, whenever needed, is analysed.

Chapter 7 concludes the thesis by answering the questions presented in section 1.2, , based on the performed research. In conclusion, future research recommendations are given.

A scheme of the thesis outline is presented in Figure 1.1.

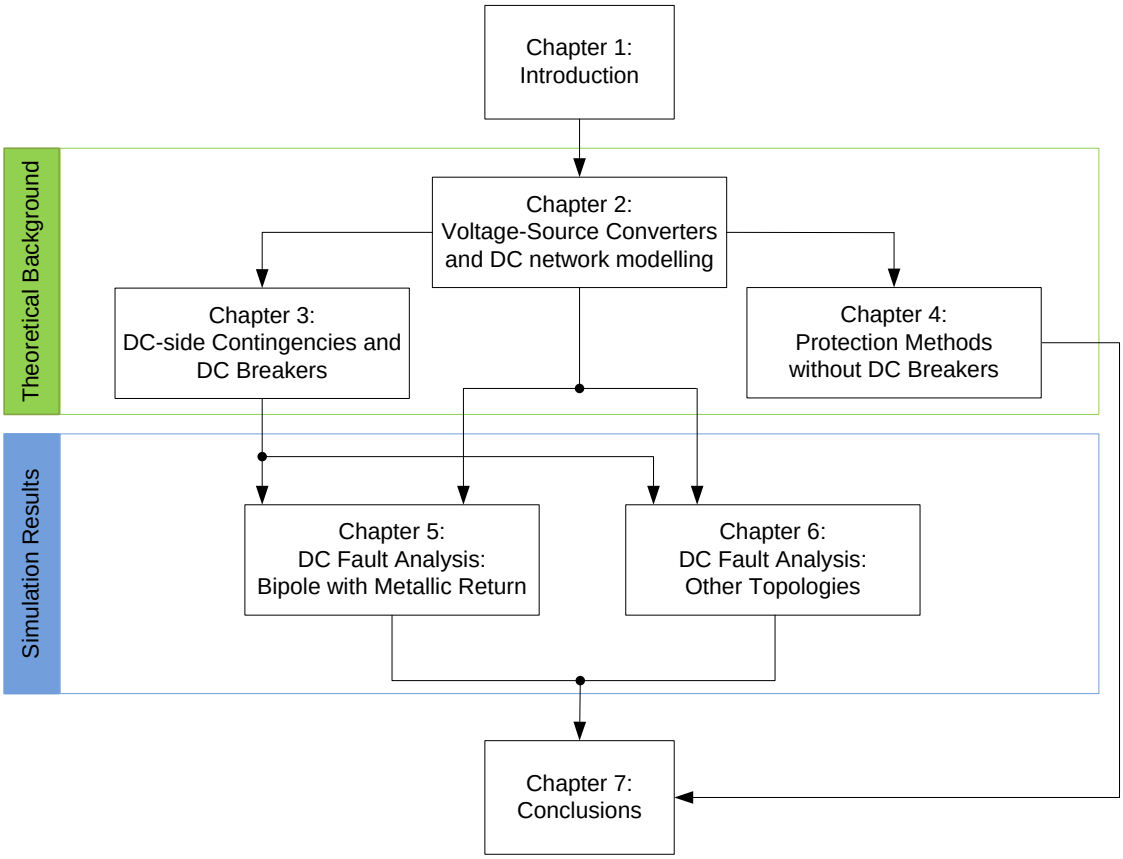


Figure 1.1: Thesis Outline

Chapter 2

Voltage-Source Converters and DC Network Modelling

The main objective of this chapter is to present the basic configuration of a voltage-source converter for high voltage DC transmission (VSC-HVDC) system. On the first part of the chapter, a short description of the main components and the parameters that have to be considered for modelling a typical VSC station are provided. Moreover, the basic control principles are illustrated and the related control equations are derived. The second part deals with multi-terminal HVDC networks. The main operating HVDC topologies used for point-to-point links are explained, compared and extended to fit the basic model of a multi-terminal DC network.

2.1 Introduction

Voltage-source converters were introduced for the first time to the HVDC transmission market in 1997 by ABB, for the experimental Hllsjn project in Sweden [6]. This link operated at 3 MW and $\pm$10 kV. After the successful test of the new HVDC transmission technology, the first commercial VSC installation was commissioned in 1999, for a system of 50 MW at a DC voltage of $\pm$80 kV, on the island of Gotland, in Sweden. Since then, the voltage and power ratings for VSC-HVDC applications have steadily increased, reaching nowadays a DC voltage level of $\pm$640 kV (bipolar) and a power capability of 2562 MVA.

A typical VSC-transmission system consists of an AC power transformer, AC filters, a phase reactor, the converter cabinet, which includes the switch valves, as well as one or two DC capacitors, DC harmonic filters and finally one or more DC cables and neutral point grounding depending on the configuration of the DC network. The layout of such a VSC-HVDC transmission system is depicted in Figure 2.1.

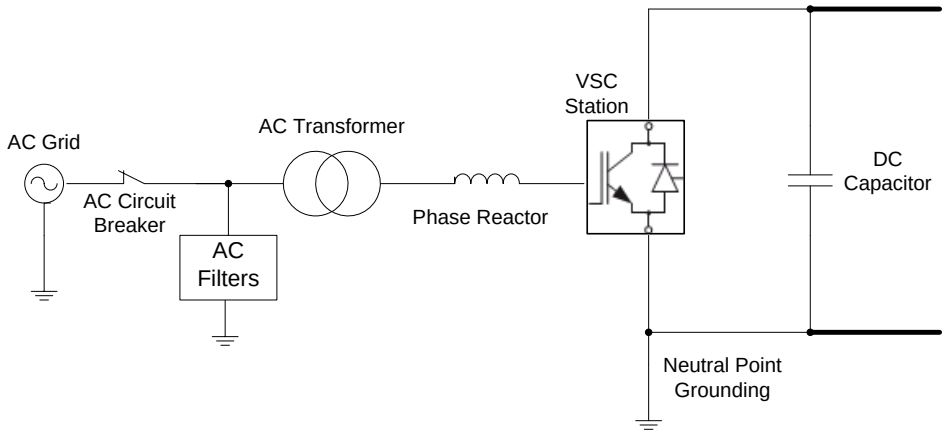


Figure 2.1: Single-line diagram of a VSC station

2.2 VSC-HVDC Components

The AC grid can be generally represented by three voltage sources 120^o phase shifted and series impedances. Whether an AC grid is characterized as weak or strong, is mostly dependent on its short-circuit ratio (SCR), which is defined as the ratio between its apparent power and the apparent power of the VSC connected to it, i.e. SCR=S_{AC}/S_{VSC}. The higher the SCR, the stronger is the grid and thus the less are the grid voltage perturbations due to the exchanged power with the VSC. Finally, it is important to determine the grid's XR-ratio, which is the ratio between the grid reactance and its resistance. This is an alternative way of expressing the grid's short-circuit angle and its value is usually high for HVAC networks, in which reactance prevails (inductive grid).

In a VSC-HVDC station AC breakers are necessary because [7; 8; 9]:

- They are able to disconnect the VSC from the AC grid in case of emergency or maintenance;
- They consist the only so far applicable way to clear DC faults, as VSCs lack the inherent ability of classical HVDC systems to deal with DC contingencies;
- They can connect the AC grid to the VSC link in order to charge the DC capacitors during the start-up phase of the system.

However, although the technology of the AC breakers is mature enough to provide an inexpensive solution, its use has a main disadvantage. The converter safety cannot solely depend on them, as in case of a DC fault, the whole converter is forced to shut down for several milliseconds. This is inefficient, as the power exchange is interrupted for long times due to their mechanical restrictions and thus new more delicate solutions were investigated and are described in the following chapters.

Finally, a bypass resistor is usually used to limit the maximum phase current during the energization of the system. The pre-insertion resistors can be connected in series with each

phase only for the start-up period. After the transient period is over, the resistors are bypassed to avoid extra losses and any effect on the control of the system. The resistors' value depends on the system parameters and needs to be determined for each specific application.

2.2.1 Transformer

A power transformer is used to change the voltage level of the grid to the appropriate level for the VSC station. The transformer can be an ordinary three-phase power transformer and mainly provides a galvanic isolation between the AC grid and the DC side, which is important in case of a fault in either of the connected sides. Moreover, a transformer with primary grounding is commonly used. In this way zero-sequence voltages can be blocked by the ungrounded transformer secondary.

The use of a usual two winding transformer is further supported by the fact that, the current in the transformer windings contains hardly any harmonics and therefore the respective losses are low [10].

However, the transformer is not only exposed to AC voltage stresses, which are generally low, but also to DC stresses. If the VSC configuration of Figure 2.2a is considered, the DC potential on the valve side winding of the transformer is $+V_{DC}/2$. However, if the DC side is grounded in the middle point of the DC link, as in Figure 2.2b, the DC potential, to which the secondary of the AC transformer is subjected, is zero [11]. Therefore, the DC stresses and consequently the transformer insulation level depend greatly on the grounding of the HVDC grid topology and will be further discussed in section 2.5.

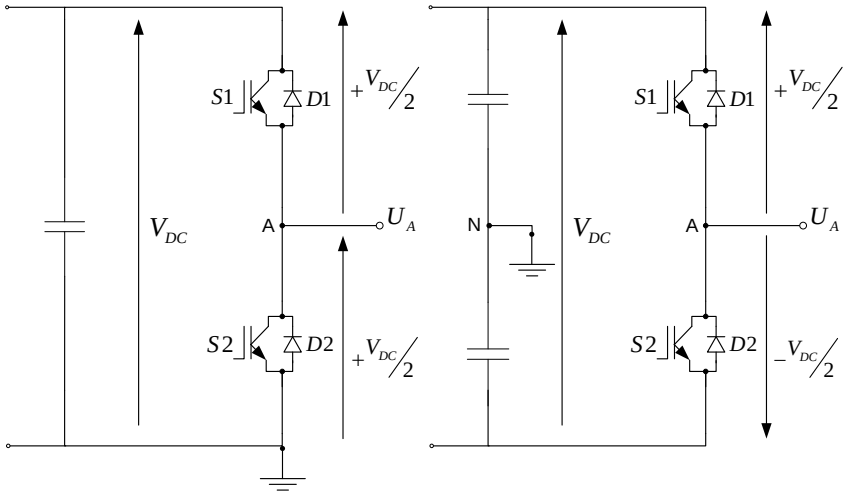


Figure 2.2: DC potential level of AC phase in case of (a) neutral point grounding (b) DC link middle-point grounding.

2.2.2 AC Filters

The main goal of the AC filters is to limit the harmonic content of the converter current and voltage, which can be detrimental for the whole system. The magnitude of the harmonic electromagnetic field (EMF) at the converter depends on the switching frequency, the DC voltage and the chosen PWM technique. In general, PWM moves the produced converter harmonics to the high-frequency spectrum, where they can be filtered more effectively. Consequently, the AC filters have to be designed as high-pass filters in order to cut those frequencies, which results in smaller AC filter sizes in VSC-HVDC compared to the classic HVDC (LCC). In this way the AC filters also protect the transformer from high frequency stresses, preventing harmonics from entering the AC grid. Since there is mainly high-frequency harmonic content the AC filters do not need to be more specifically tuned.

An important parameter, which most of the times is not specified, is the impedance of the grid to which the VSC is connected. However, the general requirements for the AC filters are [10]:

- Individual harmonic distortion:

$$D_h = \frac{U_h}{U_1} \approx 1\% \tag{2.1}$$

- Total harmonic distortion:

$$THD = \sqrt{\sum_h D_h^2} \approx 1.5 - 2.5\% \tag{2.2}$$

- Telephone influence factor:

$$TIF = \sqrt{\sum_h \left(5hf_1 C_{message(hf_1)} D_h\right)^2} \approx 40 - 50 \tag{2.3}$$

A typical filter size is between 10 to 30% of the VSC station's rated power.

2.2.3 Phase Reactor

The phase reactor, usually installed on the VSC-HVDC AC side, plays a multifaceted role for the converter. The phase reactor acts as a filter for the harmonic currents generated by the converter switching (low-pass filter). It prevents very fast changes in polarity that can be caused from the valves switching, while it limits short-circuit currents. An additional main purpose of the reactor is to permit independent and continuous control of active and reactive power, by controlling the voltage drop and the direction of the current flow across itself. A common size for the phase reactor is 0.15 pu [10].

2.2.4 Voltage Source Converter

A typical VSC uses fully-controllable switches, like gate turn-off thyristors (GTOs) or IGBTs, in contrast to the LCC, which makes use of line-commutated thyristor valves. Fully-controllable switches are preferred for high voltage applications with relatively high switching frequencies ($\sim$2 kHz). The switches are mostly controlled with PWM techniques to

reproduce a sinusoidal waveform on the AC side, which is filtered by the phase reactor and the AC filters. As a result, the harmonic content of the reproduced waveform is kept low. A two-level converter is the simplest topology that can be used to build a three-phase VSC. For this converter topology, six switch valves are used which contain several switches in series, depending on the voltage and the current ratings, and anti-parallel diodes to facilitate the bidirectional power flow of the converter. A typical layout of a two-level three-phase voltage-source converter is presented in Figure 2.3.

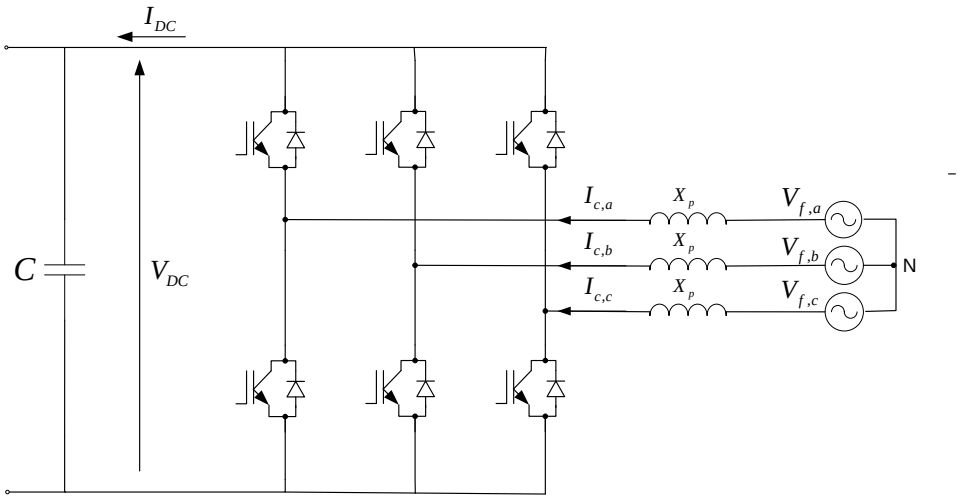


Figure 2.3: Two-level Three-phase Converter

The operating principle is simple; each of the phases is connected via the switches either to the positive or the negative pole of the DC grid. By controlling the width of the pulses via PWM techniques, a sinusoidal waveform is reproduced. As a consequence, the more the levels of switching valves that are connected in each of the arms of the converter, the lower the harmonic content of the AC waveform will be. A more detailed analysis of multi-level converters (M2C) and their behaviour during DC faults is provided in Chapter 4.

2.2.5 DC Capacitor

The DC capacitors on the DC side of the converter are most of the times placed inside the converter enclosure. The DC capacitor is used to maintain the DC side voltage at a specific level and within very close limits, thus acting as a voltage source. The primary purpose of the capacitor is to provide a low-inductance path for the turn-off current, to serve as energy storage and to reduce the harmonic ripple of the DC voltage.

However, the size of the capacitor influences the power flow control, the stiffness of the controllers and their bandwidth. In VSC-HVDC links, the DC capacitors consist the main inertia source and thus their size has to be carefully calculated, based not only on the steady-state operation, but basically based on the desired transient behaviour, e.g. during

faults or changes in operating power point, in order to avoid unwanted overvoltages at the converter valves.

The DC capacitor can also be divided into two capacitors connected to a neutral point, which can either be clamped to the neutral of the converter and grounded, or only grounded. In this way, the DC capacitor serves its goal as a path for the turn-off current to the ground. The DC capacitors' configuration depends on the DC grid topology, which is further discussed in section 2.5.

The DC capacitor can be characterized by a time constant τ. This constant represents the necessary time to fully charge the capacitor at the converter nominal power and is defined as the ratio of the energy stored in the capacitor, when rated voltage (V_{DC}) is applied to it, with respect to the converter's nominal apparent power S_n.

$$\tau = \frac{1}{2} C \frac{V_{DC}^2}{S_n} \tag{2.4}$$

If the mechanical analog of the DC capacitors in a VSC-HVDC link is considered, the time constant τ corresponds to the machine inertia constant H [sec]. More specifically, H is given by [12]:

$$H = \frac{W_k}{S_g} = \frac{1}{2} J \frac{\omega^2}{S_g} \tag{2.5}$$

where W_k [MVA·sec]is the kinetic energy stored in the rotating mass of the machine, S_g [MVA] is the generator rating, J is the moment of inertia [kg· m^2] and ω [rad/s] is the generator's angular speed.

The analogy of the two constants is backed up by the dimensional analysis of the equations. The mechanical analog of voltage [V] is velocity [m/s], while the respective analog of capacitor [F] is the mass [kg]. As a result, the kinetic energy in the rotating part of the generator is equivalent to the electrostatic energy stored in the capacitor.

Furthermore, the machine inertia constant H determines the response of the generator's angular speed to any changes in the input power. Equivalently, the capacitor's time constant determines the response of the DC voltage level to any power changes. Therefore, the DC capacitors play the role of the machine inertia in VSC-HVDC systems.

2.3 Equivalent Model

2.3.1 AC Side

The AC side of the VSC can be considered as a controlled voltage source, whose frequency, phase angle and amplitude can be independently controlled using PWM techniques. As a result this voltage source can be described by the equation:

$$\begin{aligned} V_C(t) &= \sqrt{2} V_C \sin(\omega t + \delta) + harmonics \\ V_C &= m_a \frac{V_{DC}}{2} \end{aligned} \tag{2.6}$$

where m_α is the PWM modulation index, ω is the angular frequency of the voltage fundamental component and δ is the phase angle between the AC grid and the converter fundamental voltage. The harmonics content of the converter voltage can be considered negligible, as it is filtered by the phase reactor and the AC filters, which were described in the previous sections. Therefore, the converter voltage can be assumed to be equal to the modulator reference voltage, as long as the PWM modulation index remains in the linear region ($m_\alpha \leq 1$). If space-vector modulation is considered, the upper limit for the modulation index linear region is 1.15 (or $\frac{2}{\sqrt{3}}$).

For the better understanding of the AC side operation, a single phase diagram is provided and further elaborated. In Figure 2.4 the AC grid is connected to the converter controlled voltage source through a series impedance. This impedance mainly consists of the transformer and phase reactor inductances, as their resistances can be safely neglected. In this case, the circuit is lossless.

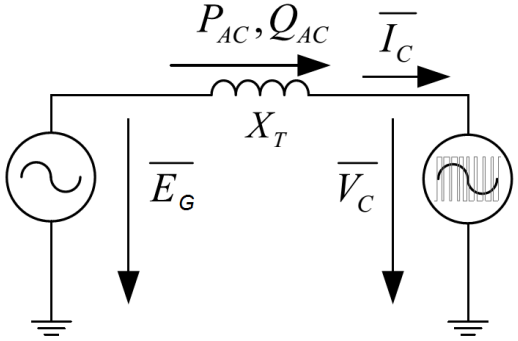


Figure 2.4: VSC-HVDC AC-side equivalent model

The grid voltage is assumed to have a null phase angle, i.e. $\bar{E}_G = E_G e^{j0}$, where E_G is the phase rms grid voltage. The converter voltage has a phase angle δ, $\bar{V}_C = V_C e^{j\delta}$, where V_C is the converter phase rms voltage. The per unit active power flow is given by the equation:

$$p_{AC} = \frac{e_G v_C}{x_T} \sin\delta \tag{2.7}$$

where e_G is the grid voltage in pu, v_C is the converter voltage in pu and x_T is the total per unit reactance.

The active power control can be accomplished by changing the converter voltage phase angle δ, while keeping all other parameters constant. This is done through PWM techniques, by controlling the switching of the valves. When $\delta > 0$, $p_{AC} > 0$, active power is being fed to the AC grid and the VSC acts as an inverter. When $\delta < 0$, $p_{AC} < 0$ and active power is delivered to the DC grid, thus VSC acts as a rectifier.

Accordingly, the pu reactive power flow is defined as :

$$q_{AC} = \frac{e_G}{x_T}(e_G - v_C \cos\delta) \tag{2.8}$$

If $e_G < v_C \cos\delta$ reactive power is being consumed by the AC grid, while if $e_G > v_C \cos\delta$ reactive power is produced by the AC grid. Consequently the reactive power can be controlled

by adjusting the amplitude of the converter voltage V_C, which is achieved through the modulation index. The influence of each of the aforementioned controls to each other can be neglected and hence the active and reactive power control can be considered independent. Based on this fact, the VSC can operate at all four quadrants of its P, Q diagram (see Figure 2.5). However, there are certain limitations imposed by the converter nominal specifications, namely:

- 1st limitation: The current is limited by the rated current of the converter valves. Therefore the apparent power that can be transmitted is limited and so is the radius of the P,Q circle.
- 2nd limitation: The direct voltage is limited by the overvoltage limit of the DC grid. The maximum DC voltage level influences the maximum converter voltage, which in turn influences the reactive power flow.
- 3rd limitation: The under-voltage limit is set by the main-circuit design. There is a certain minimum voltage that is required for the active power transmission.

In order to create the VSC capability diagram (P,Q) the active and reactive power flow equation need to be adjusted since $\cos\delta = (\frac{e_G^2}{x_T} + q_{AC})\frac{x_T}{e_G v_C}$ and $\sin\delta = p_{AC}\frac{x_T}{e_G v_C}$, using the identity $\cos^2\delta + \sin^2\delta = 1$, the equations are rearranged as follows:

$$\left(\left(\frac{e_G^2}{x_T} + q_{AC}\right)\frac{x_T}{e_G v_C}\right)^2 + \left(p_{AC}\frac{x_T}{e_G v_C}\right)^2 = 1 \Rightarrow p_{AC}^2 + \left(q_{AC} + \frac{e_G^2}{x_T}\right)^2 = \left(\frac{e_G v_C}{x_T}\right)^2 \quad (2.9)$$

This is an equation of a circle on the P, Q diagram, with centre $(0, -\frac{e_G^2}{x_T})$ and radius $\frac{e_G v_C}{x_T}$. The chord in the first circle determines the second limit. The resulting P, Q diagram of the VSC station is depicted in Figure 2.5.

2.3.2 DC Side

The DC side of a VSC station can be modelled as a controlled DC current source. If the converter is considered lossless, $P_{AC} = P_{DC}$, and thus, for a specific V_{DC} the direct current is given as:

$$I_{DC} = \frac{P_{DC}}{V_{DC}} \quad (2.10)$$

The losses in a VSC station are non-linear in nature and are basically influenced by the PWM switching frequency. Therefore, the losses and the converter efficiency have to be obtained at each operating point. An indication of the converter losses at full power is 1-2% [13; 14; 15]. The equivalent DC side for the average model is presented in Figure 2.6.

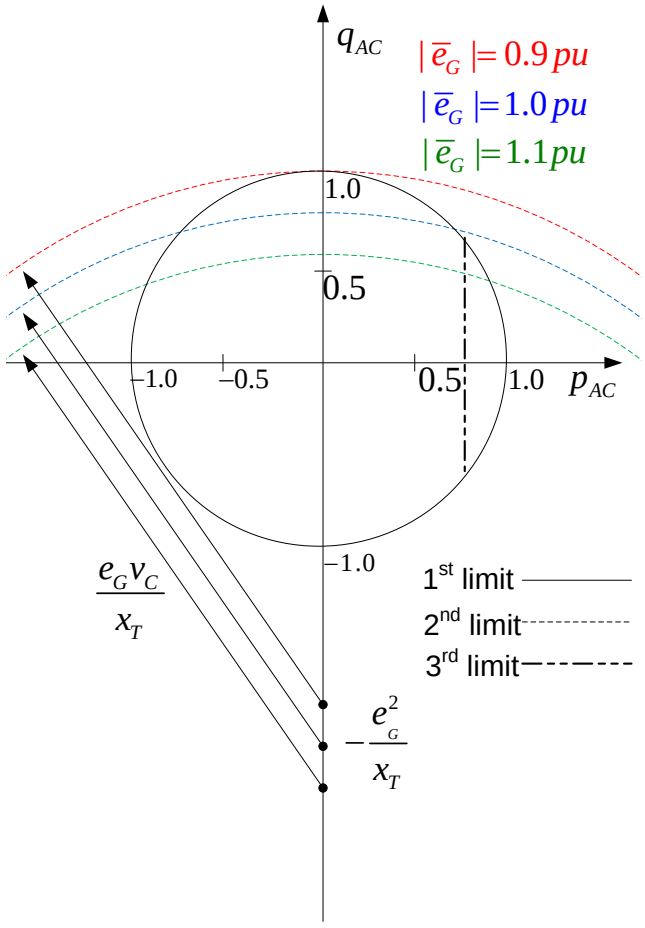


Figure 2.5: Active and reactive power transmission limitations of VSC-HVDC converters

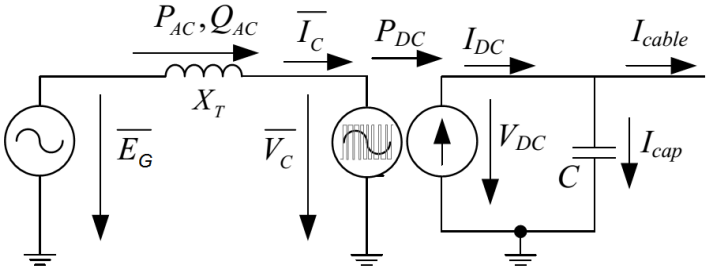


Figure 2.6: DC side equivalent model of a VSC-HVDC transmission system

2.4 Controllers

The main capability of a VSC is the independent control of active and reactive power flow. As mentioned in the previous section, by controlling the phase angle δ and the amplitude of the converter voltage, active and reactive power can be independently adjusted.

Reactive power control is possible through direct control and AC voltage control. In the direct reactive power control, reactive power is compared to a reference value. The PWM modulation index (m_α) is controlled to make the converter absorb or generate the necessary amount of reactive power.

In case of AC voltage control, the actual AC voltage level at the converter is compared to a reference value. If it needs to be lowered, the converter absorbs reactive power. On the contrary, if the AC voltage needs to be increased, the converter generates reactive power.

As far as real power is concerned, it can be controlled in three ways:

- directly;
- by controlling DC voltage level;
- by controlling AC frequency.

The direct active power control is accomplished through setting the phase angle of the fundamental frequency component of the VSC voltage.

In the DC networks active power flow should be balanced at all times. A possible unbalance in the active power causes rapid changes in the DC voltage level, which can be prevented by controlling it. Due to such unbalances, it is considered essential to use DC voltage control at least in one of the VSC stations in a two- or more terminal network. In this way, balanced active power flow can be ensured and the amount of real power needed to be fed or absorbed to sustain the required voltage level at the DC capacitors is always regulated.

In addition to the previous two control mechanisms, AC frequency control is necessary in case of VSC connection to a weak grid or passive loads. The control is achieved through changes in the frequency of the valve pulse firing sequence in PWM. By regulating the amount of active power exchanged with a weak grid, VSC can support the grid frequency, damping any frequency oscillations.

Another important VSC control is the AC current control that flows to/from the converter through the phase reactor. The inner current controller (ICC) regulates the current to a reference value, without exceeding the maximum current limitation of the converter. The reference values for the current are provided by the outer controllers and the role of the ICC is to evaluate the necessary voltage drop over the series reactance to produce the reference current.

The outer controllers consist of the all the previously discussed controllers used for active and reactive power control. However, the controller choice depends on the VSC network and on each project's specifications. Figure 2.7 shows the overview of a VSC system's control structure.

To facilitate the system's control, all the three-phase voltages and currents are transformed into the direct-quadrature coordinate system (dq). This transformation is called the

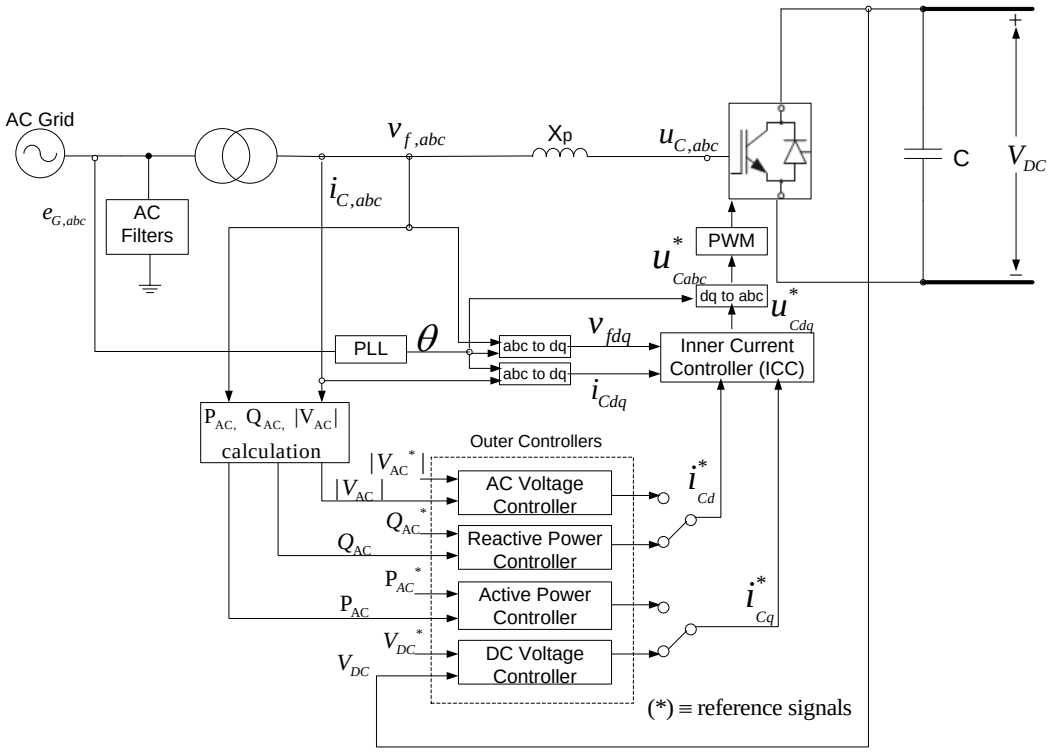


Figure 2.7: VSC controllers overview

Park Transformation.[1] The abc-frame is firstly transformed into the αβ-frame. The αβ-frame is the Cartesian coordinate system.

For control design and implementation purposes, it is more efficient to use functions of time instead of the amplitude and the phase of a space-phasor as system variables. Moreover, the control in αβ-frame reduces the number of required control loops from three to two. However, the controller signals have sinusoidal waveforms, which make control difficult. Compensators need to be of high order and control bandwidth has to be larger than the frequency of the reference signals to achieve zero steady-state error, therefore, the use of dq-frame control is preferred. In dq-frame the signals assume DC waveforms in steady-state and zero steady-state error can be achieved by including integral compensator terms [16].

However, in case the dq-frame representation is used, the new coordinate system needs to be synchronized with the AC network. This is achieved through a phase-locked loop control (PLL).

2.4.1 Phase-Locked Loop Control

The phase-locked loop (PLL) is accommodating the synchronization of the converter control with the line voltage [17]. The input of the PLL is the three-phase grid voltage, which

[1] see Appendix B

is usually measured at the AC filters. Its function is to align the grid voltage with one axis in the dq-frame. If the voltage is aligned with the q axis, e_{Gd}=0. If the d axis is preferred, e_{Gq}=0. Therefore, the PLL can calculate the grid's phase synchronous angle required for the dq transformations, via a closed-loop control, which is presented in the block diagram of Figure 2.8 [16].

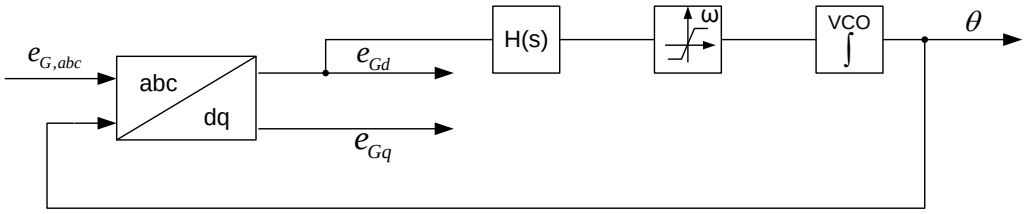


Figure 2.8: PLL controller

The three-phase voltage is transformed in the dq-frame. The d coordinate, e_{Gd}, is chosen to be regulated to zero in the steady state. A compensator H(s) is designed to ensure a zero steady-state error. The compensator's transfer function is determined on the basis of the required phase and gain margins, as well as the PLL's required bandwidth.

After acquiring the rotational speed of the dq frame ω, this value is limited by upper and lower limits to avoid large variations. Finally, a voltage-controlled oscillator (VCO) is used to integrate ω and thus, calculate the grid's phase synchronous angle (θ) and reset it to zero, as soon as it reaches 2π. This value is used for the new dq-transformation of the grid voltage, closing the control loop.

2.4.2 Inner Current Controller

The Inner Current Controller (ICC) evaluates the voltage drop across the phase reactor to produce the necessary AC current within the converter rating limits. Across the reactor the following equation applies:

$$v_f - u_C = R_p \cdot i_C + L_p \cdot \frac{d}{dt}(i_C) \tag{2.11}$$

where R_p is the phase reactor resistance, L_p is the phase reactor inductance, v_f is the voltage at the AC filter, at one end of the phase reactor and u_C is the converter voltage.
The above equation when transformed into dq-frame results in:

$$\begin{aligned} v_{fd} - u_{Cd} &= R_p \cdot i_{Cd} + L_p \cdot \frac{d}{dt}(i_{Cd}) - \omega L_p i_{Cq} \\ v_{fq} - u_{Cq} &= R_p \cdot i_{Cq} + L_p \cdot \frac{d}{dt}(i_{Cq}) + \omega L_p i_{Cd} \end{aligned} \tag{2.12}$$

The above equations, applicable for the phase reactor, take into account only the fundamental voltage of the VSC-HVDC. From the equations, it can also be derived that the ICC is used to get rid of the cross-coupling effects between the d and q axes. A block diagram

representing those equations is depicted in Figure 2.9. Following this method, the equations for all the individual parts of the VSC AC side circuit were derived and included in the averaged VSC station model.

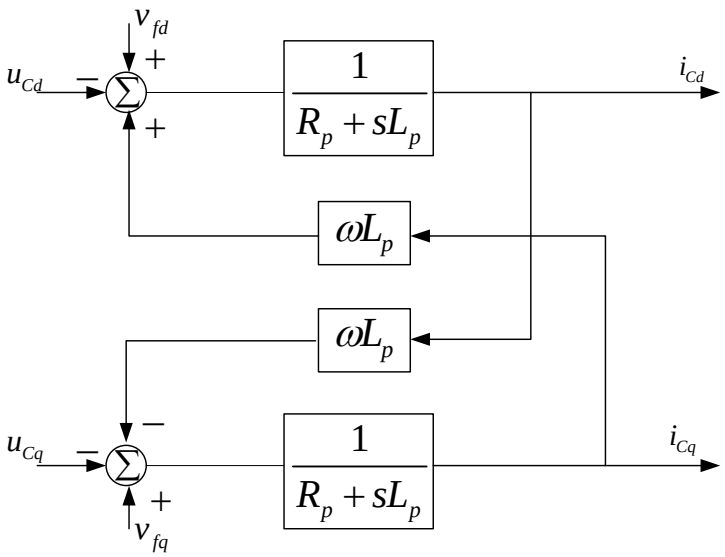


Figure 2.9: Phase Reactor block model

At the first stage, the current through the phase reactor is compared to a reference value provided by the outer controllers discussed in the next sections. A compensator (PI Controller) is used to transform this current error into a voltage error. This voltage error is subtracted by the converter voltage at that moment, creating a reference voltage value, which should be kept within the converter voltage rating. When the voltage error is nullified, the converter voltage has the desired level. Figure 2.10 presents a block diagram of the ICC.

2.4.3 Outer Controllers

This group of controllers can be divided into two main categories: the reactive power channel and the active power channel. The first group of controllers includes the reactive power controller and the AC voltage controller, while the latter consists of the active power controller and the DC voltage controller. The AC frequency controller was not implemented for further investigation, as it is only used when the VSC is connected to passive or isolated loads.

Not all of the controllers can be used simultaneously. Only one from each category (active/reactive power channel) can be used at a given time, depending on the network configuration and the system specifications. All of the implemented controllers employ a proportional-integral (PI) regulator to achieve zero steady-state error.

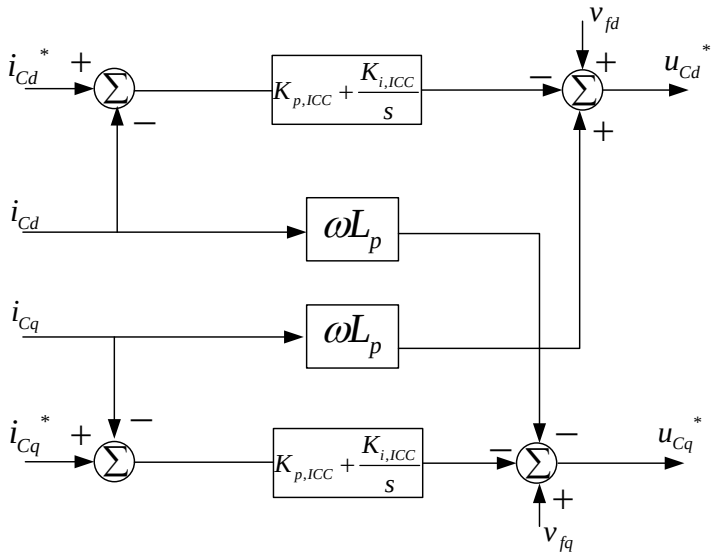


Figure 2.10: ICC controller

Active and Reactive power Controller

The instantaneous values of active and reactive power in three-phase abc-frame are given by [18; 19]:

$$\begin{aligned} p_{ac} &= u_a i_a + u_b i_b + u_c i_c \\ q_{ac} &= \frac{1}{\sqrt{3}}(u_{ab} i_c + u_{bc} i_a + u_{ca} i_a) \end{aligned} \tag{2.13}$$

If a Park transformation (Appendix B) that preserves the magnitude of the phase quantities is used, the above equations, when transformed into dq-frame, result in:

$$\begin{aligned} p_{ac} &= \frac{3}{2}(v_d i_d + v_q i_q) \\ q_{ac} &= \frac{3}{2}(v_q i_d - v_d i_q) \end{aligned} \tag{2.14}$$

Because of the PLL control, the q-axis of the dq-frame is aligned with the AC network voltage phasor, thus $e_d = 0$. As a result:

$$\begin{aligned} p_{ac} &= \frac{3}{2} v_q i_q \\ q_{ac} &= \frac{3}{2} v_q i_d \end{aligned} \tag{2.15}$$

Hence, from (2.14), it becomes apparent that active and reactive power can be independently controlled. The active power can be controlled through i_q, whereas the reactive power can be controlled through i_d. The reference dq currents calculated by the active and reactive power controllers need to be saturated before fed to the ICC. A current limiter is responsible to

maintain the current references within the converter's current ratings. Figure 2.11 depicts the block diagrams of the two implemented PI controllers, whose analytical equations are:

$$\begin{aligned} i_{Cq}^{*} &= (p_{ac}^{*} - p_{ac}) \cdot \left(K_{p,p} + \frac{K_{i,p}}{s} \right) \\ i_{Cd}^{*} &= (q_{ac}^{*} - q_{ac}) \cdot \left(K_{p,q} + \frac{K_{i,q}}{s} \right) \end{aligned} \tag{2.16}$$

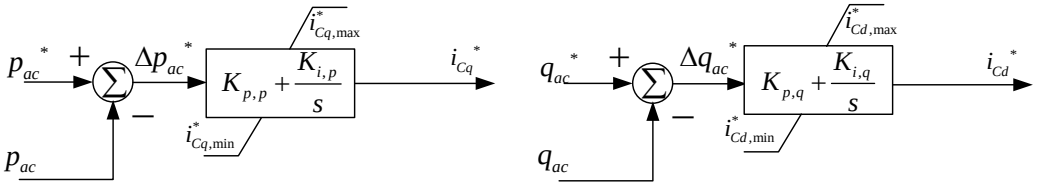


Figure 2.11: Active and reactive power controllers

DC Voltage Controller

The controller aims to keep the DC voltage at a certain level, adjusting the amount of active power that needs to be fed into or absorbed by the network, which is accomplished via i_q control. The controller could be working on the error of the DC voltage, however in that case, the closed-loop dynamics would depend on the operating point, since I_{DC} is inversely proportional to V_{DC}. To avoid non-linearity problems, the control is based instead on the energy W_C stored in the DC capacitor (C), which is proportional to V_{DC}^2, and is given by the equation:

$$W_c = \frac{1}{2} C V_{DC}^2 \tag{2.17}$$

In Figure 2.12 the block diagram of the controller is depicted, whose analytical expression is:

$$i_{Cq}^{*} = (W_c^{*} - W_c) \cdot \left(K_{p,DC} + \frac{K_{i,DC}}{s} \right) \tag{2.18}$$

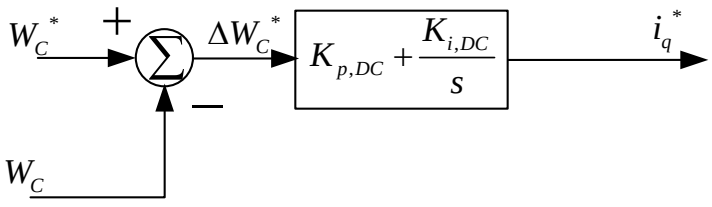


Figure 2.12: DC voltage controller

AC Voltage Controller

The purpose of this controller is to regulate the AC voltage at the point of common coupling (PCC), which in our analysis is located at the secondary of the AC transformer. By adjusting the i_{Cd}, the amount of reactive power flow to/from the converter is controlled so that the AC voltage level is kept at a reference value. This controller is depicted in Figure 2.13 and is described by:

$$i_{Cd}^{*} = (v_{PCC}^{*} - v_{PCC}) \cdot \left(K_{p,AC} + \frac{K_{i,AC}}{s} \right) \tag{2.19}$$

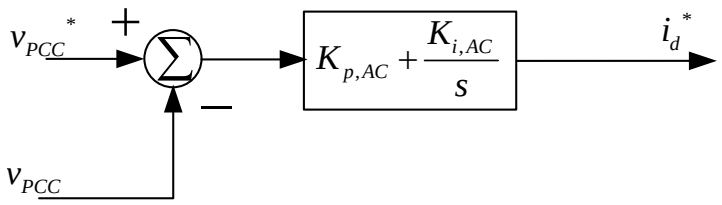


Figure 2.13: AC voltage controller

Bandwidth

When PWM techniques are used, it is important to select the switching and sampling frequencies carefully. The closed-loop bandwidth (a_c) should be at least 10 times lower than the angular sampling frequency (ω_s), while the angular switching frequency (ω_{sw}) should be at least lower than half the sampling frequency [20; 21], thus:

$$a_c \leq \frac{\omega_{sw}}{5} \leq \frac{\omega_s}{10} \tag{2.20}$$

In this thesis the switching frequency was selected at 2 kHz (12.56 krad/s) and therefore the maximum closed-loop bandwidth is a_c =2.5 krad/s, which is enough for damping purposes [22]. However, for sake of safety margin the control bandwidth was chosen to be 2 krad/s.

The outer controllers need to be sufficiently slower than the ICC to ensure control stability. Therefore, for the DC voltage outer controller, analysing its closed-loop transfer function, the proportional gain should be:

$$K_{p,DC} \leq \frac{1}{8} a_c C \leq a_{dc} C \Rightarrow a_{dc} \leq 0.125 a_c \tag{2.21}$$

Therefore, there is a relation between the ICC bandwidth (a_c) and the bandwidth of the DC voltage outer controller (a_{dc}). As several simplifications were made in (2.21), there is the need to keep an extra safe margin. Therefore it is advisable to choose $a_{dc} \leq 0.1 a_c$ [23]. Simplification included neglect of converter switching behaviour, PLL influence, cross-coupling of d and q axes etc. In this thesis $a_{dc} = 0.075 a_c$. As far as the integral gain is considered, to guarantee a sufficient gain to damp voltage oscillations:

$$\frac{K_{i,DC}}{K_{p,DC}} << \frac{a_c}{4}, \text{ if } \frac{K_{i,DC}}{K_{p,DC}} \leq \frac{a_c}{8} = a_{dc} \Rightarrow K_{i,DC} \leq a_{dc}^2 C \tag{2.22}$$

The dynamics of the reactive power channel depend on the impedance of the AC grid. Therefore, it can only be tuned via trial and error. However, the bandwidth should not exceed that of the DC voltage controller, a principle applicable for the active power controller as well. It is favored to first track the power variations in the network through the VSC station that controls the DC voltage level, maintaining it within limits. Thus, the bandwidth of the active power controller should be, at its maximum, the same as the respective value of the DC voltage controller.

To calculate the controller gains, it is possible to use dimensional analysis. The input and the output units of the controller are used to acquire the units of the controller gains. More specifically, the gains of the controllers are calculated in the SI and in pu based on the equations shown in Table 2.1.

Table 2.1: Controller gains

Controllers	k_p (pu)	K_p (-)	k_i (pu)	K_i (-)
ICC	$\alpha_{c_{pu}} \cdot L_p$	$\alpha_{c_{pu}} \cdot L_p \cdot \omega$	$\alpha_{c_{pu}} \cdot R_p$	$\alpha_{c_{pu}} \cdot R_p \cdot \omega$
P	$\alpha_{dc_{pu}} \cdot C_{dc_{pu}}$	$k_p \cdot I_{bc}/S_{bc}$	$\alpha^2_{dc_{pu}} \cdot C_{dc_{pu}}$	$k_i \cdot I_{bc} \cdot \omega/S_{bc}$
Q	$\alpha_{dc_{pu}} \cdot C_{dc_{pu}}$	$k_p \cdot I_{bc}/S_{bc}$	$\alpha^2_{dc_{pu}} \cdot C_{dc_{pu}}$	$k_i \cdot I_{bc} \cdot \omega/S_{bc}$
DC voltage	$\alpha_{dc_{pu}} \cdot C_{dc_{pu}}$	$k_p \cdot \frac{I_{bc}}{(1/2)CV^2_{dcr}}$	$\alpha^2_{dc_{pu}} \cdot C_{dc_{pu}}$	$k_i \cdot \frac{I_{bc} \cdot \omega}{(1/2)CV^2_{dcr}}$
AC voltage	$\alpha_{dc_{pu}} \cdot C_{dc_{pu}}$	$k_i \cdot \frac{I_{bc}}{V_{bc}}$	$\alpha^2_{dc_{pu}} \cdot C_{dc_{pu}}$	$k_i \cdot \frac{I_{bc} \cdot \omega}{V_{bc}}$

The quantities V_{bc}, I_{bc}, S_{bc} are the base AC voltage, AC current and power values of the converter respectively, while V_{dcr} is the voltage base of the DC grid.

2.4.4 Current Limiter

A current limiter is needed to maintain the current at the converter within limits. The reference current value provided by the outer controllers is compared to the maximum allowable current through the valves. If this value is exceeded, the magnitude of the current has to be limited. The magnitude of the current vector is given by:

$$|i^*| = \sqrt{i_d^{*2} + i_q^{*2}} \tag{2.23}$$

There are three limitation modes that can be applied, depending on the converter, which are summarized as follows:

1. d-axis priority: reactive power is prioritized to help voltage restoration. In this case d-axis current remains stable and q-axis current is reduced. This strategy is mostly applicable in case of weak grid connections.

2. q-axis priority: active power is considered more important and thus only d-axis current is limited, while q-axis current is preserved.

3. proportional limitation: both axes currents are decreased proportionally, i.e. power factor is maintained constant.

The aforementioned limitation modes are presented in Figure 2.14.

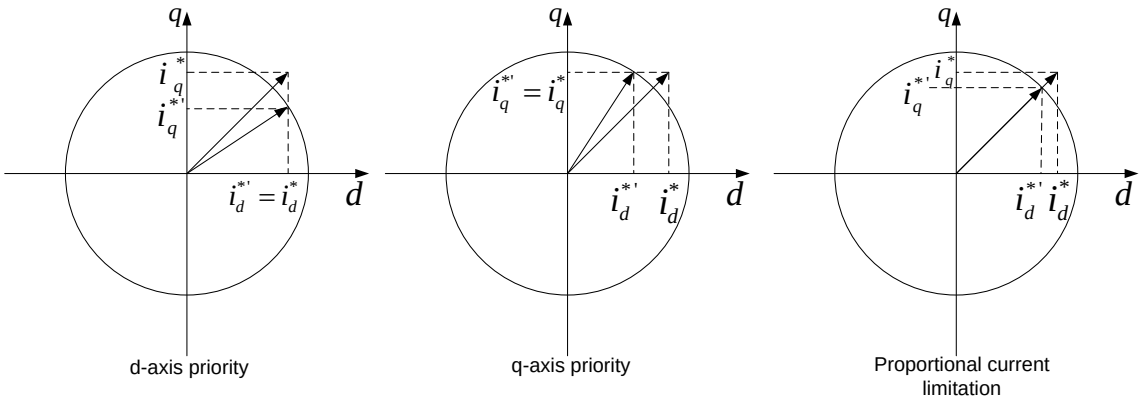


Figure 2.14: Current limiter modes of operation

2.5 HVDC Topologies

2.5.1 Introduction

HVDC links have been operating around the globe for more than half a century. The first commercial link was made in 1954 to connect the island of Gotland to the mainland of Sweden. Based on the classical LCC-station, most of those links are point-to-point, while only two multi-terminal LCC-HVDC systems exist with three hubs interconnected [10; 24]. The two multi-terminal HVDC links currently in operation are [25]:

- the Sardinia-Corsica-Italy (SACOI), interconnecting the two islands with the mainland of Italy;
- the Hydro Quebec - New England link in Canada.

One of the main advantages of VSC technology in comparison to the classical is its capability to easily facilitate large multi-terminal networks. This is possible, due to their high controllability and the low levels of interaction between the interconnected terminals. This feature is essential for the new era of HVDC transmission systems in an attempt to reinforce the existing AC infrastructure and effectively connect not only national grids with the available offshore wind supplement, but also interconnect countries, providing cost-effective and reliable solutions.

Therefore, the analysis of the operation of all the possible network topologies on a real multi-terminal network consisting of VSCs is essential not only for normal operation, but also for protection analysis, especially when it comes to DC contingencies. In this section an overview of the existing topologies with their respective advantages and disadvantages is provided. These topologies are simulated and further investigated in Chapters 5 and 6.

2.5.2 Operating Topologies

There are several possible converter arrangements in a HVDC transmission system, which can be divided, based on the number of converters used at each terminal, into monopole and bipole configurations.

Monopolar configuration uses only one pole, while the bipolar uses two poles with different polarities ($\pm V_{DC}/2$). These topologies can be further classified by the DC circuit characteristics, e.g. return path. It is important to stress that all the presented topologies can be extended to accommodate multi-terminal HVDC networks. Table 2.2 summarizes the most common operating topologies [26; 8].

Table 2.2: Operating HVDC configurations

	Number of converters	
	Monopole	Bipole
Return Path	Symmetric Ground Return Metallic Return	Ground Electrodes Metallic neutral

Monopolar HVDC configuration

In this topology only one converter is used at each end of the network. Because of this characteristic, this method is more cost effective, but also more prone to problems. The HVDC grid lacks DC fault redundancy, as all of the interconnected stations are affected by the high fault currents and no power can be exchanged. Unless selective DC protection methods are implemented, which are able to isolate the faulty HVDC line in time, the grid has to get de-energized before operation is restored.

There are mainly three types of monopolar configurations:

1. Symmetric monopole, which uses two fully insulated conductors for the positive and return pole of the DC grid.

2. The asymmetric with metallic return has two DC conductors between the terminals, one of which is also grounded.

3. The asymmetric with ground return has only one DC conductor connecting the terminals and the return is made through the ground. All connected terminals need to be grounded.

Symmetric Monopole Figure 2.15 depicts the symmetric monopole DC grid scheme. This configuration either uses no grounding on the DC side or the DC link capacitors are grounded in their middle point to fix the DC voltage. Therefore, in case of a DC pole-to-ground fault, the DC side is not fed by AC grid currents. Due to lack of DC grounding or the particular middle point grounding of the DC link, the coupling transformer is not

subjected to any DC voltage and thus it does not suffer from increased voltage stresses. Therefore, its design can be simple. Moreover, there is no DC current in the ground, which can raise environmental issues. However, its main disadvantage against the other monopolar topologies is that it requires two fully insulated conductors, which increases its cost.

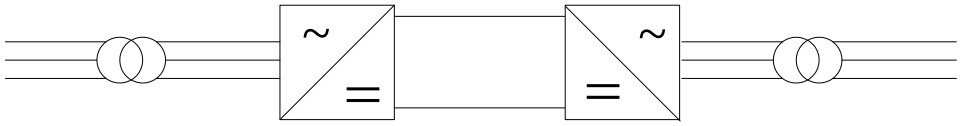


Figure 2.15: Symmetric Monopole

Asymmetric Monopole with Metallic Return The configuration, presented in Figure 2.16 has no DC ground current, as the return is made via the metallic conductor, while at the same time it requires only one fully insulated conductor and one less, reducing its cost. Moreover, it can easily facilitate the expansion of the network to bipolar, as the metallic return can be used as neutral connection. On the other hand, the DC voltage stress on the coupling transformer is high. The transformer lies at 0.5 pu DC voltage and thus, it needs to be designed for higher DC voltage stresses than the one in symmetric monopole.

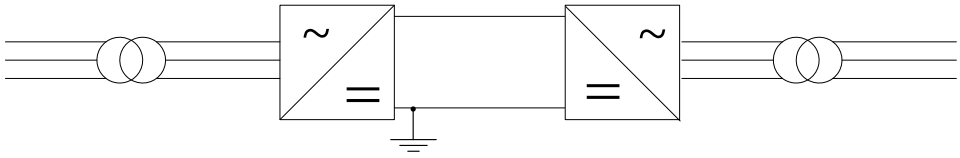


Figure 2.16: Asymmetric Monopole with metallic return

Asymmetric Monopole with Ground Return This topology has the advantage of very low cost, due to the presence of only one fully insulated conductor and the capability of expansion to bipolar if necessary. However, except for the disadvantages of asymmetric monopole with metallic return, it requires permission for introducing electrodes to the ground and for continuous operation with DC ground current. As a result it raises environmental concerns, because the direct currents can interact with metallic structures in its vicinity. Therefore, a more careful design is necessary.

Additionally, the coupling transformer insulation levels need to be high, due to the DC voltage stresses to which it is exposed. The DC voltage level, at which the secondary of the transformer lies, is the same as for the asymmetric monopole with ground return. Finally, in case of DC faults, the AC side continues to feed the fault with in-feed currents, due to the loop created by the grounds at different points of the grid. Figure 2.17 presents the discussed topology.

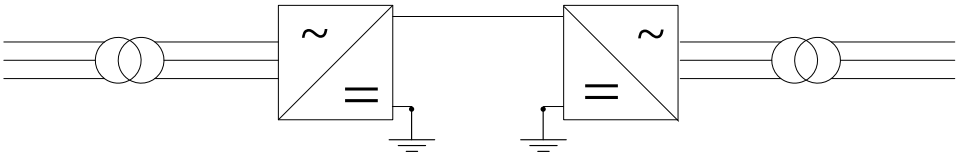


Figure 2.17: Asymmetric Monopole with ground return

Bipolar HVDC configuration

The bipolar configuration employs two converters at each terminal. On the AC side they are powered either by two different transformers, or by a transformer with two secondary windings. It is common to use Yg-d configuration for the positive pole converter and Yg-y for the negative pole converter or vice versa. The DC stresses on the transformers' secondary windings are high, as both of the transformers lie at 0.5 pu DC voltage. Therefore, special attention has to be paid to their insulation.

On the DC side, each of them controls half of the DC voltage ($\pm V_{DC}/2$). The current on each pole is roughly the same, with only small unbalances. The main advantage of the bipolar configuration is its redundancy, which can be even more than half the total station rating if overloading is possible, in case one converter suffers a fault. However, there are disadvantages for each of the available bipolar topologies.

Bipole with metallic neutral This configuration is shown in Figure 2.18. As long as the DC side has a ground at the neutral, the transformers need to be designed for high DC voltage stresses. This fact along with the use of more converters makes them a more costly alternative than the monopolar ones for the same power rating, however bipolar configurations can achieve double the power rating of monopolar links. Moreover, this bipolar configuration needs an extra low-voltage insulated neutral inductor, in comparison to the bipolar with ground return. There is also the possibility to use a fully insulated conductor and use it as spare in case of emergency, providing a more expensive solution.

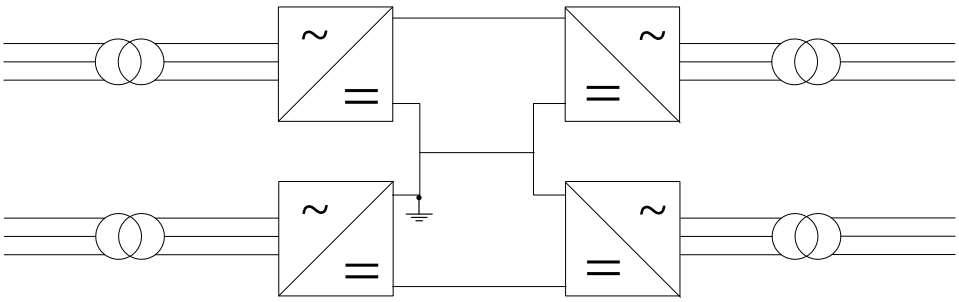


Figure 2.18: Bipole with metallic return

Bipole with ground return Except for the higher cost when compared to respective monopolar configurations, the bipolar configuration with ground return also raises environmental concerns, same with those of the asymmetric monopole with ground return. This HVDC topology is depicted in Figure 2.19.

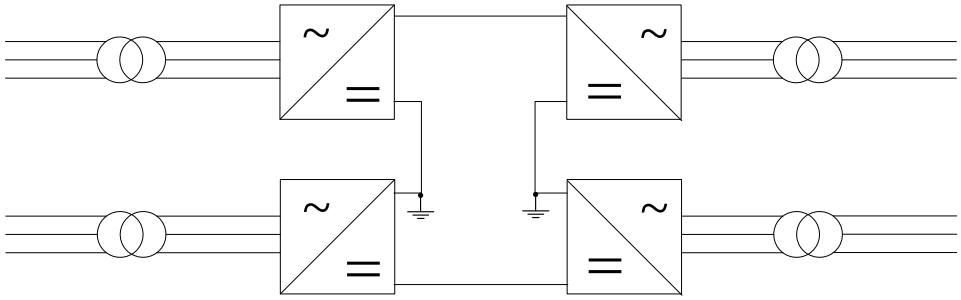


Figure 2.19: Bipole with ground return

2.5.3 Multi-terminal DC Network Model

There are several ways to model a multi-terminal DC network (MTDC), depending on the research objective. The focus of this thesis is to develop of a simulation model, which represents with as much detail as necessary the different DC grid configurations and analyzes the system response during DC faults.

Keeping this into account, a state-space model of a MTDC grid was not applicable. Such an average model is mostly useful in steady-state operation and cannot be easily used to represent different topologies and types of DC faults. Moreover, the application of a fault in different locations and the consequent need for fault location, line isolation and DC breaker implementation cannot be investigated. These limitations subsequently led to the development of a grid, making use of custom components provided by the Matlab/ Simulink®SimPowerSystems™library. Depending on the DC grid configuration, the grid schematic was subsequently changed. A scheme of a simple symmetric monopolar grid model is presented in Figure 2.20.

There are two ways to model HVDC lines, the pi-equivalent (π) section model and the distributed parameters model.

π-section line model

The pi-equivalent model consists of lumped RLC elements. In order to represent an HVDC transmission line, whose characteristics are uniformly distributed along its length, there is the possibility to cascade several identical pi-sections. Based on the frequency range that needs to be represented, the number of sections used can change. A representation of a pi-section model is given in Figure 2.21.

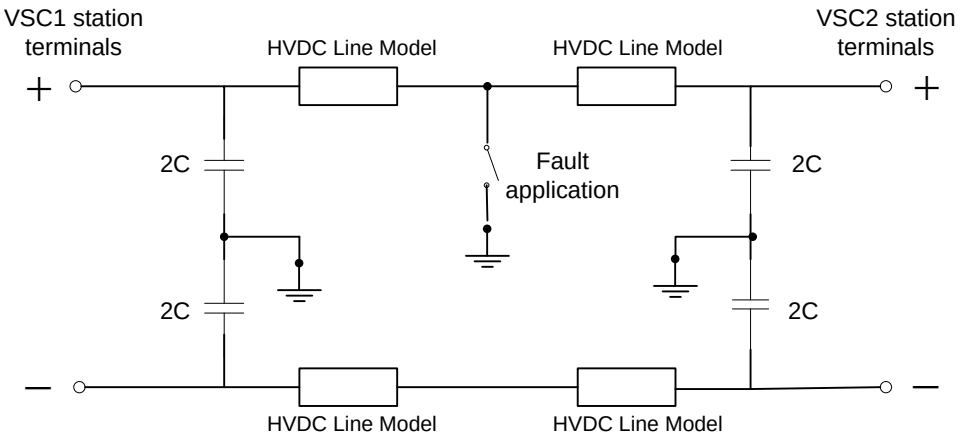


Figure 2.20: Matlab/Simulink simple grid model

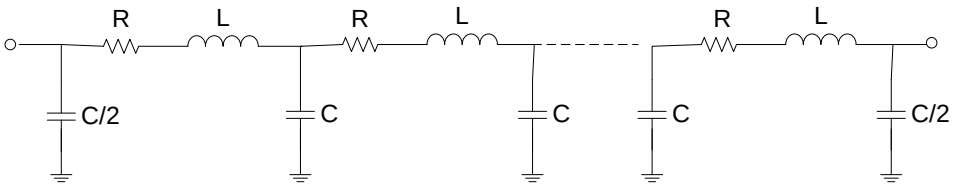


Figure 2.21: Pi-equivalent line section model

The series impedance and shunt admittance of one pi-section are given by the following equations [27; 28; 29]:

$$\frac{1}{Y_{series}} = (R' + j\omega L') \cdot l \cdot \frac{\sinh(\gamma \cdot l)}{\gamma \cdot l} \tag{2.24}$$

$$Y_{shunt/2} = (j\omega C'/2) \cdot l \frac{\tanh(\gamma \cdot l/2)}{\gamma \cdot l/2} \tag{2.25}$$

where R', L', C' are the line parameters per unit length, l is the length of the line or the section modeled and $\gamma = [(R' + j\omega L') \cdot j\omega C']^{1/2}$. From the equations, it becomes clear that this model is best suited for one frequency of interest and a specific length. If high transients need to be analysed the difference in performance with the distributed line model needs to be evaluated.

Distributed parameters model

This model assumes that inductance and capacitance of the line are uniformly distributed along the line, while the resistance is lumped. It is based on the Bergeron's travelling wave model, which produces constant surge impedance and is basically a single frequency model [29]. The surge impedance is given by the equation:

$$Z_c = \sqrt{\frac{L'}{C'}} \tag{2.26}$$

where L', C' are the per unit length parameters. In this model e+Zi, where e is the line voltage and i is the line current, enters one end of a lossless LC line end, travels with a phase velocity v and exits at the other end unchanged after time τ. Phase velocity and transport delay are equal to:

$$v = \frac{1}{\sqrt{L'C'}} \tag{2.27}$$

$$\tau = \frac{l}{v} \tag{2.28}$$

where l is the length of the line.
The resistance of the line is lumped at three places; R/4 at both ends of the line and R/2 in the middle. Taking this into account, the model is represented in Figure 2.22 .

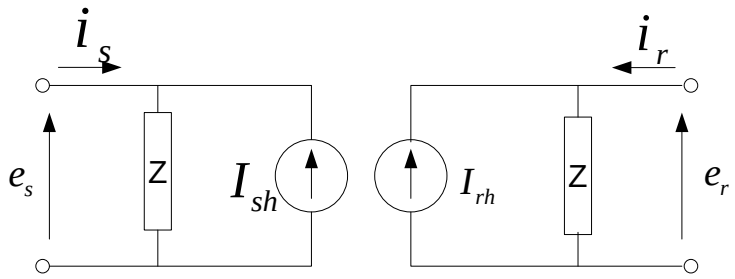


Figure 2.22: Distributed parameters line model

The following equations are derived when using the current injection method [29]:

$$\begin{aligned} I_{sh}(t) &= \left(\frac{1+h}{2}\right)\left(\frac{1+h}{Z}e_r(t-\tau) - hi_r(t-\tau)\right) + \left(\frac{1-h}{2}\right)\left(\frac{1+h}{Z}e_s(t-\tau) - hi_s(t-\tau)\right) \\ I_{rh}(t) &= \left(\frac{1+h}{2}\right)\left(\frac{1+h}{Z}e_s(t-\tau) - hi_s(t-\tau)\right) + \left(\frac{1-h}{2}\right)\left(\frac{1+h}{Z}e_r(t-\tau) - hi_r(t-\tau)\right) \end{aligned} \tag{2.29}$$

where

$$Z = Z_c + \frac{R'}{4}$$

$$h = \frac{Z_c - \frac{R'}{4}}{Z_c + \frac{R'}{4}}$$

$$\tau = l\sqrt{L'C'}$$

R', L', C' are line parameters per unit length and l is the total length of the line. It becomes apparent that this model can be used to better represent wave propagation phenomena and line end reflections more accurately than the pi-equivalent line model [27]. However, its increased complexity slows down the simulation time, so its use should be selected in face of a trade-off between accuracy and time needed.

2.6 Comparison of HVDC line models

A simple point-to-point asymmetric monopolar configuration with ground return (see Figure 2.17) is used to simulate and evaluate the investigated line models available in Matlab/Simulink®. The parameters of the simulated HVDC line are shown in Table 2.3.

Table 2.3: DC line parameters

DC line parameters	Unit	Value
Length (l)	km	100
Resistance (R)	Ω/km	0.0195
Inductance (L)	mH/km	0.2
Capacitance (C)	nF/km	220

The two available line models are compared in normal operation, as well as under faulty circumstances. Therefore, a fault is applied, through an ideal switch, in the middle of the line at 0.7 s.

Bode plots were made for the impedance of the distributed parameters line model and the pi-equivalent model with 1, 3 and 6 pi-sections. The results are presented in Figure 2.23.

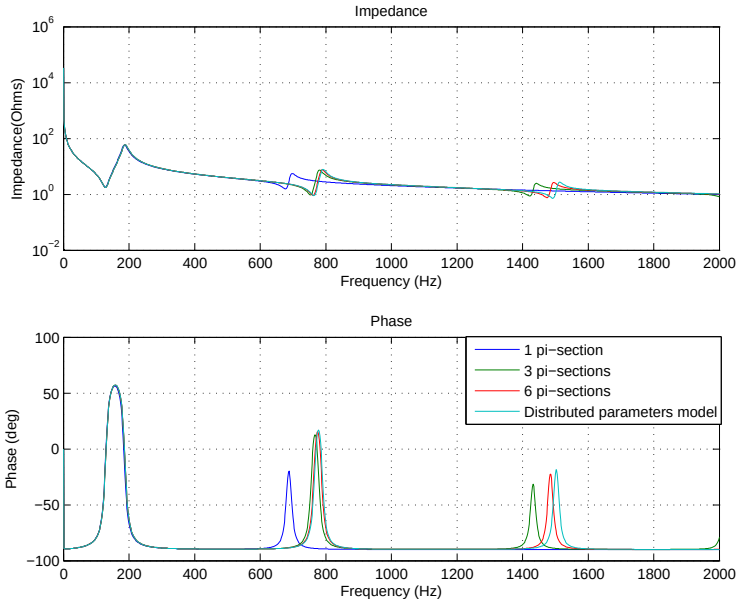


Figure 2.23: Impedance vs. Frequency relation for different line models

While the time domain response of the DC currents and voltages was found to be the same for all simulated line models, the main difference was observed in the frequency domain calculation of their impedance.

From Figure 2.23, it can be observed that the higher the number of the incorporated pi-sections, the more the pi-equivalent model approaches the distributed parameters line characteristic curve, especially for frequencies below 1 kHz.

In this study, the line models are used to simulate DC lines. Consequently the currents and voltages simulated are not periodical, except for the fault case, where the storage elements of the lines get discharged. Although the discharging current frequency depends on the energy storage elements of the DC lines, as well as the DC link capacitors and additional DC filters implemented, in general, the observed frequencies do not exceed a few hundred Hz.

Consequently, in the HVDC simulations the pi-equivalent model with six pi-sections is considered equivalent to the distributed parameters line model. In the fault simulations, presented in Chapter 5, the distributed parameters model was preferred to simulate the transport delay of the lines.

2.7 Summary

In the first part of Chapter 2, the general configuration of a VSC station was presented along with its main controllers. In the second part, the existing HVDC grid topologies were introduced. These topologies are simulated, in Chapters 5 and 6, for multi-terminal HVDC links and are compared based on their fault response. Finally, two different options for line modelling offered by the Matlab/ Simulink® SimPowerSystems™ library were described. After analysing the theoretical models and after calculating their impedance in the frequency domain, the distributed parameters line model was chosen over the pi-equivalent model for the HVDC line fault simulations, based on its travelling wave characteristics.

Chapter 3

DC-side Contingencies and DC Breakers

3.1 Introduction

One of the main obstacles MTDC VSC networks will have to deal with is grid protection [30]. Such transmission systems are vulnerable to DC faults and lack of adequate protection has proven to be a significant problem preventing MTDC systems from expansion [31].

Unlike AC faults, DC faults are almost always permanent and are caused by failure of cable insulation or damaged cable due to another source, e.g. ship anchors for undersea cables or fallen trees in case of overhead lines [9]. When a DC fault occurs, the current rises significantly and can damage the equipment close to it. Additionally in case of a multi-terminal network, all stations connected to the common DC terminal are vulnerable and the performance of the whole system is at stake [32].

In classical HVDC, thyristors have the capability to block the AC side from feeding the DC fault. More specifically, by turning them off, as soon as a DC fault is detected and the AC breakers are opened, in order to de-energize the system. However, this is not applicable in VSC HVDC networks.

A VSC converter comprises of IGBT modules with anti-parallel diodes, facilitating the two-way exchange of power. Therefore, in case of a DC fault, even if the IGBTs are switched off, a large fault current can still flow through the freewheeling diodes. In this case, use of AC breakers could protect the system, but at the same time complete de-energization of a multi-terminal system for a long time is not acceptable for HVDC grids [33; 34]. Consequently, several protection measures have been suggested in the literature, regarding design of DC breakers and control strategies for fast and reliable detection and isolation of faulty lines, and some prototype breakers have been designed (ABB, Alstom).

However, breaker use is not yet extensive and research is very active in the optimization of speed, on-state losses and DC opening capability.

In the present chapter, the types of DC faults are presented, along with an extensive theoretical analysis of the system reaction during a fault, in case no protection scheme is used. Moreover, a simulation model for the study of these faults is explained, while the limitations of the use of an average model are elaborated. In the last part, an overview of

the proposed DC breaker technologies and the way of integrating those into the simulation model is provided.

3.2 Types of DC Faults

Cable faults are more common than faults in other parts of the system [35]. This is due to the variety of conditions that can cause a DC fault. The most frequent reason is insulation deterioration or breakdown [35]. However, there are several others reasons that can lead to the same result, such as electrical stresses, environmental conditions, aging and physical damage [35]. The DC faults that are possible in a HVDC system can be categorized as [9; 19; 36]:

- Positive line to ground fault;
- Negative line to ground fault;
- Positive to negative line fault.

Since the system is in general symmetrical, negative line to ground fault can be considered a mirror of the positive line to ground fault. Therefore, in the remaining of this thesis only the line-to-line fault and positive line to ground fault are further investigated.

Faults on DC lines are, usually, line-to-ground faults [9; 30; 19]. A line-to-line fault happens when the two active conductors are connected either directly or through the ground. This occurs seldom, as it requires a severe damage of both HVDC line cables. Especially regarding submarine cables, where most of the cable problems are created by mechanical stresses, a short-circuit fault is very unlikely.

3.2.1 Line-to-ground fault

This type of fault occurs when one line (positive or negative pole) is short-circuited to the ground. This can happen due to the reasons already mentioned. Most commonly, broken insulation, due to environmental and mechanical fatigue, can allow a current path to ground. As the fault persists, it deteriorates the cable insulation and worsens the fault situation.

In case of submarine cables, ground faults can happen when ships anchor and cut one of the lines. In case of overhead lines, lightnings or construction works can result in a cut line falling to the ground [9]. In all of these cases the fault is permanent and the line needs to be completely isolated for the cable to be replaced.

3.2.2 Line-to-line fault

A line-to-line fault is less likely to occur than a line-to-ground fault. It is generally very unlikely, due to the distance between the lines, that an object falls and cuts both the positive and the negative line at the same time, resulting in a short-circuit through the ground. Especially in overhead lines, a lightning cannot cause a bipolar fault [19].

As far as undersea cables are considered, they are almost immune to such faults, as they are most often separated from each other, and are well protected by several layers of

insulation and conduit, which make less likely the occurrence of a simultaneous fault that would bring both conductors in touch [9]. The only case that a line-to-line fault is more probable is the occurrence of a switching fault or failure at the converter station, which could result in a short-circuit between the two poles.

3.2.3 DC fault probability

Overhead HVDC lines are reported to have a monopolar fault probability of 0.4 faults/100 km/year [37]. From these faults, only approximately 10% are permanent, with an estimated repair time of 24 hours. Permanent bipolar faults have almost the same risk as HVAC double circuit faults, namely 0.003 faults/100 km/year [37]. If the same 10% permanent-temporary faults rate is assumed, the total bipolar fault rate is 0.03 faults/100 km/year. This rate is 10 times less than monopolar faults [37].

Moreover, submarine cables have an even less probability of experiencing a fault, and especially a bipolar fault. More specifically, the main causes of submarine cables damage are anchors and fishing activity [38]. Between 2007 and 2010, many incidents were recorded, involving ships travelling with their anchors deployed for several miles, leading to multiple cable damage [38]. As a result, measures have been taken considering not only spacing of cables, but also cable burial (even more than 0.5 m) depending on seabed conditions and sea depth or even protection with mattresses or rock dumping, if the seabed conditions do not accommodate cable burial. Indicative is the rate of submarine cable faults around the Norwegian coast due to anchors, which is only 2-5$\cdot 10^{-4}$ faults/100 km/year [39].

3.3 DC Fault Analysis

In this section a more elaborate analysis is provided for both types of investigated faults. The theoretically expected VSC system behaviour is presented for a better understanding of the complete system reaction. The DC fault analysis is presented in the simulation results of Chapters 5 and 6.

For the analysis, it is assumed, based on circuit theory, that the DC cable fault is the same as a DC bus fault. In order to better understand the non-linear nature of the fault, it is divided into stages for each of which the respective equations are provided.

3.3.1 Line-to-ground fault

The line-to-ground fault analysis depends basically on the grounding of the DC system and the converter. This determines the loop that will be created between the fault ground and the rest of the system. The converter is usually grounded at the neutral point in a bipolar configuration.

Otherwise, in case of monopolar HVDC links, the return can be either through the ground, or via a grounded metallic return. In case of a symmetric monopole the only loop there can be is with the middle point of the DC-link. This is generally employed to reduce the imbalance between the positive and negative voltages and currents.

The loop formed between the grounding of the DC side and the AC side of the converter can be avoided, if an AC transformer is used after the AC filters with no grounding on its secondary winding, which provides galvanic isolation from the AC grid. In the following analysis, a transformer with a ground on its secondary is assumed.

Let us consider a positive line-to-ground fault. The only change in case of a negative line-to-ground fault will be the direction of the current and the active diodes that feed the fault [35]. Figure 3.1 depicts a positive pole-to-ground fault and only shows the VSC which is closer to the fault.

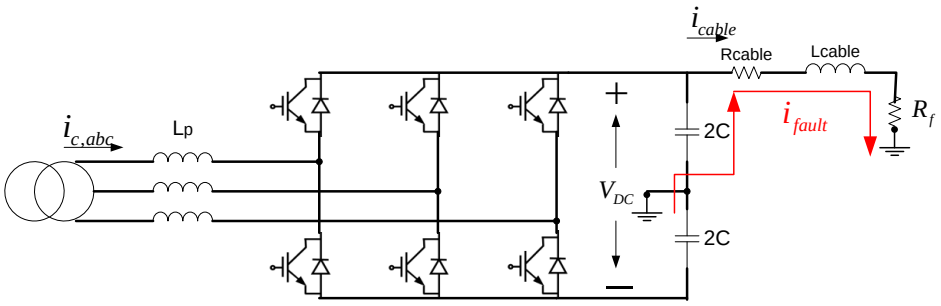


Figure 3.1: VSC with positive pole-to-ground fault

First Stage There is a loop formed between the fault ground and the middle point of the DC link. The circuit can be analyzed with equivalent circuits that show the different stages of fault development. It should also be noted that the fault resistance value plays a role in the oscillation damping. First of all, the positive pole capacitor gets discharged through the fault, contributing significantly to the fault peak current. This stage is a series RLC circuit with certain initial conditions, $v_C(t_0) = V_0$ and $i_{cable}(t_0) = I_0$. It can be assumed that the discharge takes place as a natural response, without the current contribution from the converter. Figure 3.2 presents the equivalent circuit.

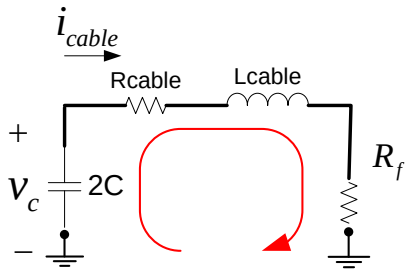


Figure 3.2: DC capacitor discharge stage

The second order RLC circuit is characterized by the following second order differential equation:

$$\frac{d^2v_c}{dt^2} + 2a\frac{dv_c}{dt} + \omega_0^2 v_c = 0 \tag{3.1}$$

where $a = \frac{R}{2L}$ and $\omega_0 = \sqrt{\frac{1}{LC}}$. In case of a ground fault the value of resistance R for the circuit becomes $R = R_{cable} + R_f$ and thus, $a = \frac{R_{cable}+R_f}{2L_{cable}}$ and $\omega_0 = \sqrt{\frac{1}{L_{cable}2C}}$. The solution of this equation depends on the relation between α and ω_0. Therefore, for a complete analysis the DC grid parameters are provided in Table 3.1.

Table 3.1: HVDC system parameters

Network Parameters	
Line Length	50 km
R_{cable}	0.975 Ω
L_{cable}	5.927 mH
C	75 μF
R_{fault}	7

Taking these values into account, $\alpha = 672.76 < 1060 = \omega_0$ and the discharge of the capacitor is an under-damped case. The solution of this case has a general form of:

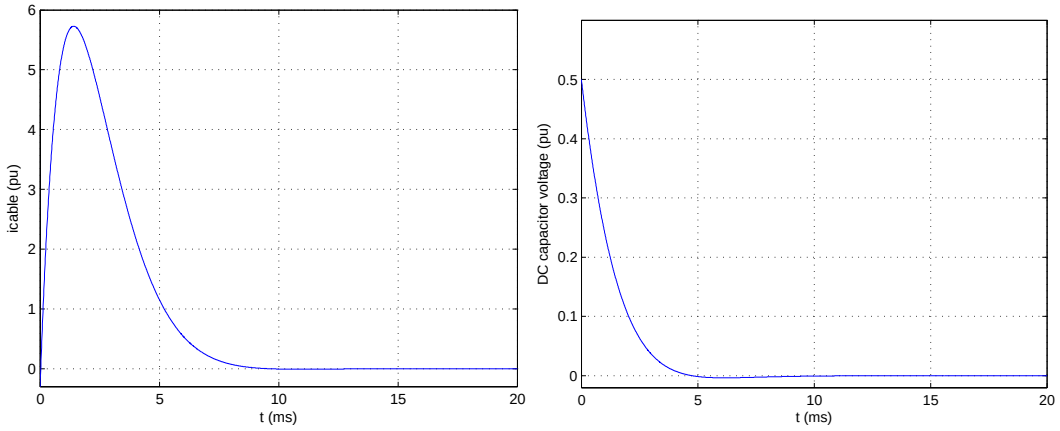
$$\begin{aligned} v_c(t) &= e^{-\alpha t}(B_1 \cos\omega_d t + B_2 \sin\omega_d t) \\ i_{cable}(t) &= 2Ca\omega_d e^{-\alpha t}(B_1 \sin\omega_d t - B_2 \cos\omega_d t) \end{aligned} \tag{3.2}$$

where $\omega_d = \sqrt{\omega_0^2 - \alpha^2}$. If $t_0 = 0$, $B_1 = V_0$ and $B_2 = -\frac{I_0}{2C\alpha\omega_d}$. The free response of the cable current and DC voltage is shown in Figure 3.3, assuming that $I_0 = -0.3pu$ and $V_0 = 0.5pu$.

Second Stage The second stage begins as soon as the voltage of the capacitor falls below any grid voltage. The IGBTs either lose control due to over-current or they are blocked for sake of protection. The capacitor voltage collapses and it is bypassed by the free-wheeling diodes of the converter. This is a forced response which can create a significant over-current that can damage the diodes and subsequently the VSC [40; 35; 9].

VSC-HVDC stations have very weak overload capability in contrast to classical HVDC and it is generally admitted that a VSC converter can handle up to 2 pu current for a limited time, i.e. only a few milliseconds [41; 42]. Figure 3.4 shows the grid current feeding stage. This stage does not have a linear response, while a continuous solution demands knowledge of the state variables of the previous diode conduction period as initial conditions. The system of state space equations that can best describe this phase is [35]:

$$\begin{pmatrix} \frac{dv_c}{dt} \\ \frac{di_{cable}}{dt} \\ \frac{di_c}{dt} \end{pmatrix} = \begin{pmatrix} 0 & -\frac{1}{2C} & \frac{1}{2C} \\ \frac{1}{L_{cable}} & -\frac{R_{cable}+R_f}{L_{cable}} & 0 \\ -\frac{1}{L_p} & 0 & 0 \end{pmatrix} \begin{pmatrix} v_c \\ i_{cable} \\ i_c \end{pmatrix} + \begin{pmatrix} 0 \\ 0 \\ 1/L_p \end{pmatrix} e_{G_{a,b,c}} \tag{3.3}$$



(a) Cable current (b) DC capacitor voltage

Figure 3.3: Free response of cable current and DC voltage for the first stage of pole-to-ground fault

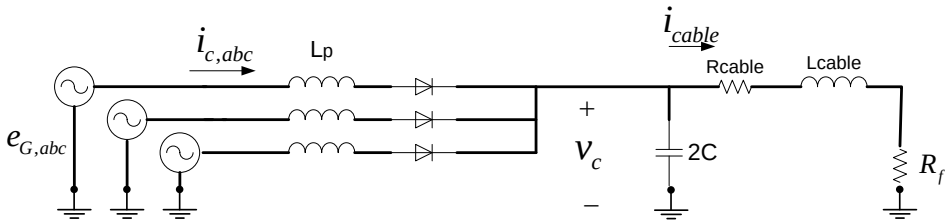


Figure 3.4: Grid current feeding stage

Third Stage Finally, the third stage includes the steady-state response in case no protection is used. The grid continues feeding the fault infinitely with equivalent impedance [35]:

$$Z = (R_f + R_{cable} + j\omega_s L_{cable}) || (1/j\omega_s 2C) + j\omega_s L_p = |Z| \angle \kappa \tag{3.4}$$

where ω_s is the synchronous angular frequency and L_p is the grid side inductance. The current through each diode is then given by:

$$i_{D1} = i_{c_{a,(>0)}} = \frac{e_G \angle \theta}{|Z| \angle \kappa} = \frac{e_G}{|Z|} \angle \theta - \kappa \tag{3.5}$$

where θ is the phase angle of the grid voltage.

The cable current is subsequently given by:

$$i_{cable} = i_{D1} + i_{D2} + i_{D3} \tag{3.6}$$

where D1, D2, D3 are the positive phase arm diodes.

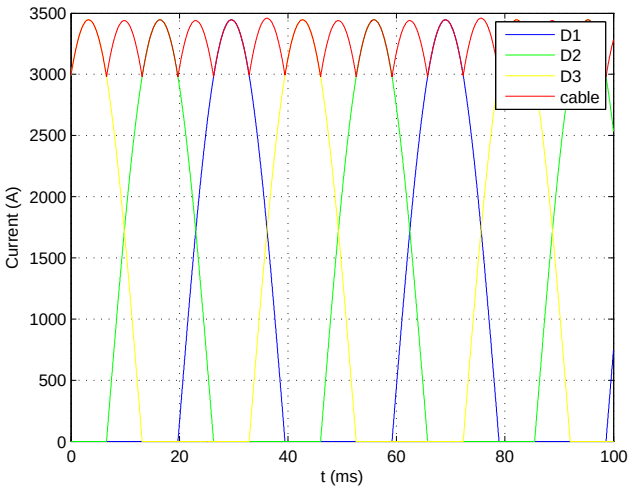


Figure 3.5: Diode and DC cable currents in steady-state stage

If a phase reactor value of 27 mH and a voltage amplitude of 120 kV are assumed, the diode currents and the DC cable current for the third stage, are shown in Figure 3.5.

The whole analysis referred to the faulty line. As far as the ”healthy” line capacitor is considered, while the other capacitor gets discharged almost to zero, depending on the value of the fault resistance, the former gets overcharged, carrying the whole nominal DC link voltage on its own, due to the DC voltage controller [43].

3.3.2 Line-to-line fault

This fault can occur in case the positive and the negative pole conductors touch each other, or are both short-circuited to the ground simultaneously. Even though it is very rare, all possible DC faults have to be considered. In this case the AC side is short-circuited via the free-wheeling diodes, even if the switches are blocked. The only solution is to isolate the DC line by means of breakers, either on the DC side, or on the AC side, to de-energize the system [43]. Figure 3.6 presents the equivalent circuit for line-to-line fault.

First Stage The first stage of the fault is the same as for the previously analysed DC fault type. The DC capacitor gets naturally discharged through an RLC circuit [35]. Based on the line parameters in Table 3.1, $\alpha < \omega_0$ and thus, the second order circuit has the same under-damped response as in the case of line-to-ground fault. Equations 3.1 to 3.2 apply in this case with resistance R only taking into account the line resistance; no fault resistance is present in short-circuit.

Second Stage During the second stage, the DC link voltage has dropped to zero and the cable inductance is discharged through the freewheel path. The current is given by the expression:

$$i_{cable} = I_0 e^{-(R_{cable}/L_{cable})t} \tag{3.7}$$

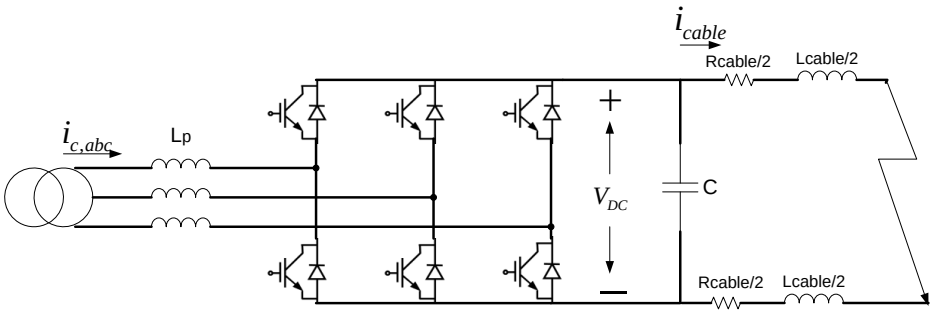


Figure 3.6: VSC line-to-line fault

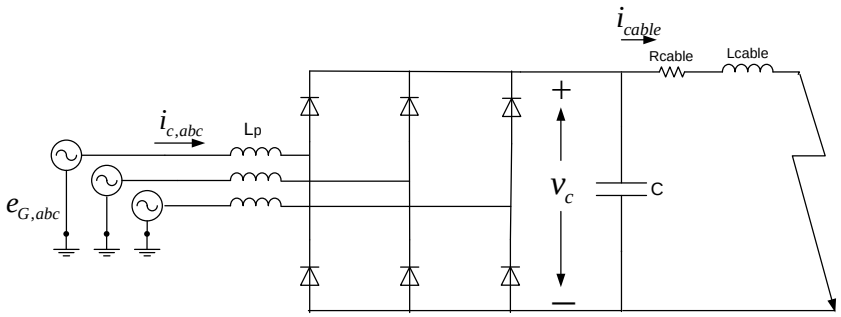


Figure 3.7: Diode free-wheel stage

where I_0 is the initial value of the current for this phase. The current through each of the diodes of the converter is equal to $i_{D1} = i_{cable}/3$. The equivalent circuitry that describes this stage is shown in Figure 3.7 and the cable current free response is presented in Figure 3.8,

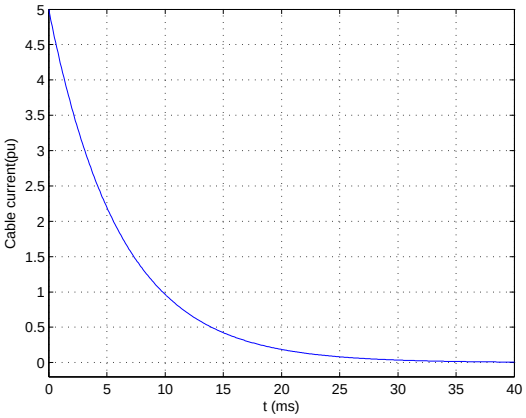


Figure 3.8: Free response of cable current in the second stage of short-circuit fault

assuming an initial value $I_0 = 5pu$. In this phase an over-current is created abruptly during the commutation through the diodes and it is able to damage the converter valves [35].

Third Stage Finally, the last stage includes a forced current source response. Figure 3.9 depicts the system during this phase. The VSC station functions as a current source, which feeds the fault. Finally the system reaches a steady state [35]. The grid phase voltage after the fault is:

$$e_{G,a} = E_G \sin(\omega_s t + \theta) \tag{3.8}$$

where E_G is the phase amplitude, θ is the phase angle and ω_s the synchronous angular frequency. The grid phase current is given by the expression:

$$i_{c,a} = I_c \sin(\omega_s t + \theta - \varphi) + I_0 e^{-\frac{R}{L}t} \tag{3.9}$$

where $L = L_{cable} + L_p$ and $\varphi = \arctan[\omega_s(L_p + L_{cable})/R]$. Therefore, for $t_0 = 0$, $I_0 = I_{c_0}\sin(\theta - \varphi_0) - I_c \sin(\theta - \varphi)$, where I_{c0} and φ_0 are the initial grid current amplitude and phase angle. (3.8) is transformed into:

$$i_{c,a} = I_c \sin(\omega_s t + \theta - \varphi) + [I_{c_0}\sin(\theta - \varphi_0) - I_c \sin(\theta - \varphi)]e^{-\frac{R}{L}t} \tag{3.10}$$

The VSC current, in this stage, has the same free response as the waveform of Figure 3.5 and is given by:

$$i_{VSC} = i_{c,a>0} + i_{c,b>0} + i_{c,c>0} \tag{3.11}$$

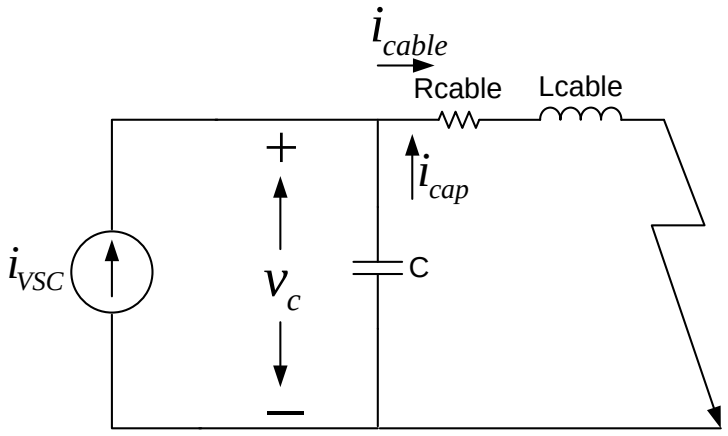


Figure 3.9: Grid current source stage

3.4 VSC Simulation Model

The simulation model of the DC lines for a MTDC grid was thoroughly described in Chapter 2. The distributed line model was finally preferred over the pi-equivalent model for the better representation of the fast transients during a fault. In this section the model of DC faults is dealt with. Whether a line-to-line fault is applied or a line-to-ground fault, the continuation of the model simulation has to be preserved. This means that the transition from one state to another has to account for the theoretical model and represent to a great extent the real reaction of a multi-terminal network. Therefore, two models for the complete VSC station were developed using Matlab/Simulink®and were compared in terms of fault simulation facilitation and faithful representation of a transient system response.

In both models the faults were applied by use of an ideal switch from the library of SimPowerSystems™, either connecting the desired point of the line to ground or to the respective point on the second DC line. By using two distributed line models for each line and changing their line length value, a fault can be easily applied at any distance from a VSC station. Furthermore, a fault resistance value has to be chosen carefully, as it can change significantly the transient response (oscillation damping) during a fault.

More specifically, the transient response of the system depends on the constants α and ω_0 of the second order differential (3.1). When a short-circuit is applied, the fault resistance is small and therefore on the DC side $R < 2\sqrt{L/C}$, which results in an oscillation of the circuit, whereas in case of a ground fault, fault resistance is usually significant and thus $R_f + R > 2\sqrt{L/C}$. This is a first order damped process, during which the DC link voltage does not fall to zero. As a result, no freewheel diode stage occurs, as described in the second stage of line-to-line fault, and the overcurrent can be limited [35].

When a short-circuit fault is applied the fault resistance is generally very small. Based on literature [30; 44; 45] in case of ground fault, the fault resistance was chosen to be 7Ω, which is the resistance at the peak current of a sparking connection in wet loamy sand and is based on the impulse behavior of concentrated grounds at high currents.

3.4.1 VSC Average Model

The average model of the VSC station makes use of equations, which describe the operation of the VSC fundamental component. As described in Chapter 2, during steady-state and under the assumption that the converter is lossless, the VSC can be represented on the DC side by a controlled current source. The value of the current is determined, taking into account the power that needs to be fed or absorbed and the DC link voltage at each moment. This can be seen in figure 2.5. However, this model is not any longer applicable in case of a fault.

As aforementioned, during a DC fault, there are several stages of system reaction. More specifically, after the initial discharge of the DC-link capacitor that corresponds to the faulty pole, the IGBTs are blocked for their protection and the converter acts as a bridge rectifier, with the current being transmitted via the freewheeling diodes.

The average model of a three-phase full-bridge rectifier can be roughly analyzed under the main assumption that the current on the DC side remains constant. If the phase reactor

inductance is neglected, the DC-side voltage average value can be obtained by considering one segment $-\frac{\pi}{6} < \omega t < \frac{\pi}{6}$. The instantaneous waveform v_d is given by the equation:

$$v_d = v_{ab} = \sqrt{2} V_{LL} \cos \omega t \tag{3.12}$$

for $-\frac{\pi}{6} < \omega t < \frac{\pi}{6}$ where V_{LL} is the line-to-line nominal voltage. The average DC voltage is therefore calculated as follows:

$$V_{do} = \frac{3}{\pi} \int_{-\frac{\pi}{6}}^{\frac{\pi}{6}} \sqrt{2} V_{LL} \cos \omega t d(\omega t) = \frac{3}{\pi} \sqrt{2} V_{LL} \simeq 1.35 V_{LL} \tag{3.13}$$

If we then consider the phase reactor inductance L_p on the AC-side, the commutation is no longer instantaneous. Figure 3.10 depicts the equivalent circuit for the commutation process and the voltage waveforms.

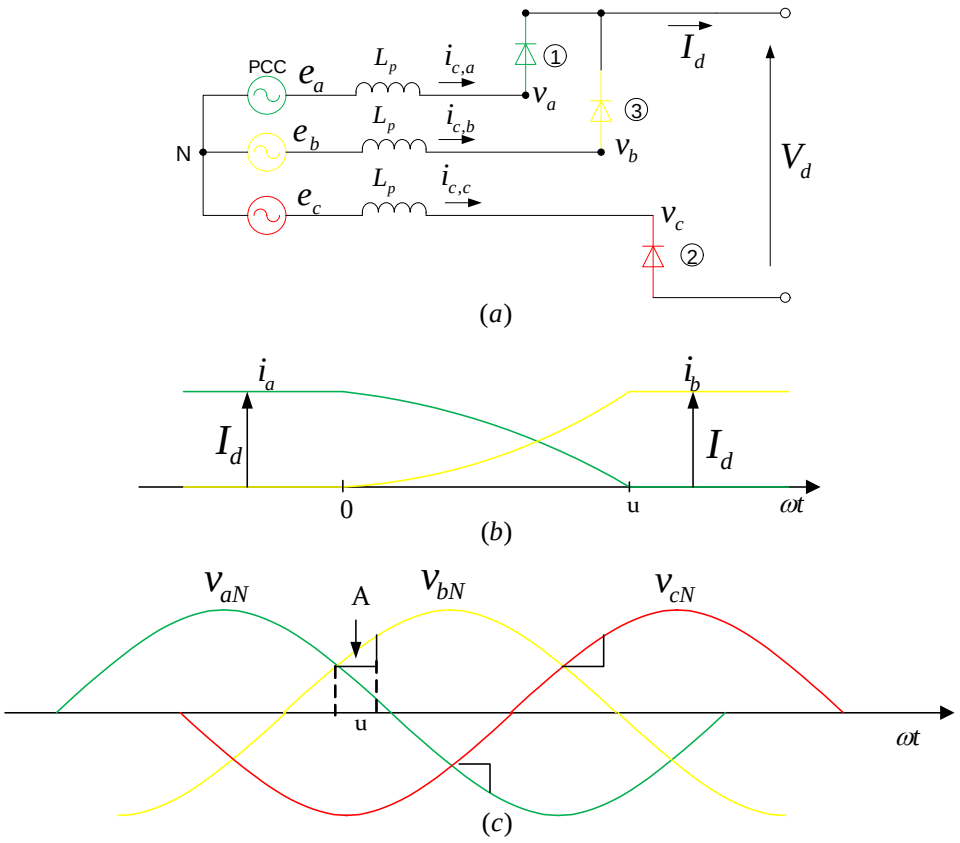


Figure 3.10: (a) Commutation equivalent circuit, (b) Current commutation, (c) Phase voltages during commutation

If the current is to be commutated from diode 1 to diode 3 at $t = 0$, the commutation only involves phases a and b and the commutation voltage is given by:

$$v_{comm} = e_a - e_b \tag{3.14}$$

Applying KVL to the a-b loop:

$$v_a = v_b \Rightarrow e_a - L_p \frac{di_1}{dt} = e_b - L_p \frac{di_3}{dt} \tag{3.15}$$

If we assume I_d constant and without ripple:

$$I_d = i_1 + i_3 \Rightarrow \frac{di_1}{dt} = -\frac{di_3}{dt} = \frac{di_u}{dt} \tag{3.16}$$

Substituting equation 3.15 into 3.14 it yields:

$$L_p \frac{di_u}{dt} = \frac{e_a - e_b}{2} \Rightarrow \omega L_p \int_0^{I_d} di_u = \int_0^{u} \frac{e_a - e_b}{2} d\omega t \tag{3.17}$$

The commutation voltage can be expressed as $v_{comm} = e_a - e_b = \sqrt{2} V_{LL} \sin \omega t$ and thus substituting into equation 3.16 gives:

$$\omega L_p I_d = \frac{\sqrt{2} V_{LL}(1 - \cos u)}{2} \Rightarrow \cos u = 1 - \frac{2\omega L_c I_d}{\sqrt{2} V_{LL}} \tag{3.18}$$

The voltage drop caused by the AC-side inductance is the area A, which is equal to $\omega L_p I_d$. This area is lost every 60^o , thus the average DC voltage is reduced by:

$$\Delta V_d = \frac{\omega L_p I_d}{\pi/3} \tag{3.19}$$

Consequently, the average DC voltage is:

$$V_d = V_{d0} - \Delta V_d = 1.35 V_{LL} - \frac{3}{\pi} \omega L_p I_d \tag{3.20}$$

where I_d is always considered positive, feeding the fault, and $V_{d,min} = 0$. Therefore:

$$I_d = i_{c,a(>0)} + i_{c,b(>0)} + i_{c,c(>0)} \tag{3.21}$$

Furthermore, the average model equations need to change, as soon as a fault is detected and continuation of the model must be preserved. When the IGBTs get blocked, all control loops are broken and control is lost.

The calculation path reaches the PCC (Point of Common Coupling), usually at the AC filters or at the secondary of the transformer, where the voltage (e_{pcc}) is monitored continuously. The output voltage of the converter is then calculated through (3.18) and fed to the DC side controlled voltage source. The q-coordinate of the phase reactor current, which determines the active power transfer, is made equal to the current I_d that is being fed to the

grid from the voltage source, thus creating a calculation loop. The d-coordinate is considered zero. Finally, the voltage at the input of the converter (v_c) is subsequently calculated by the equation:

$$e_{pcc} - i_c Z_p = v_c \tag{3.22}$$

where $Z_{p)}$ is the phase reactor impedance.

The equivalent average model of the VSC-HVDC transmission system after a fault, is depicted in Figure 3.11.

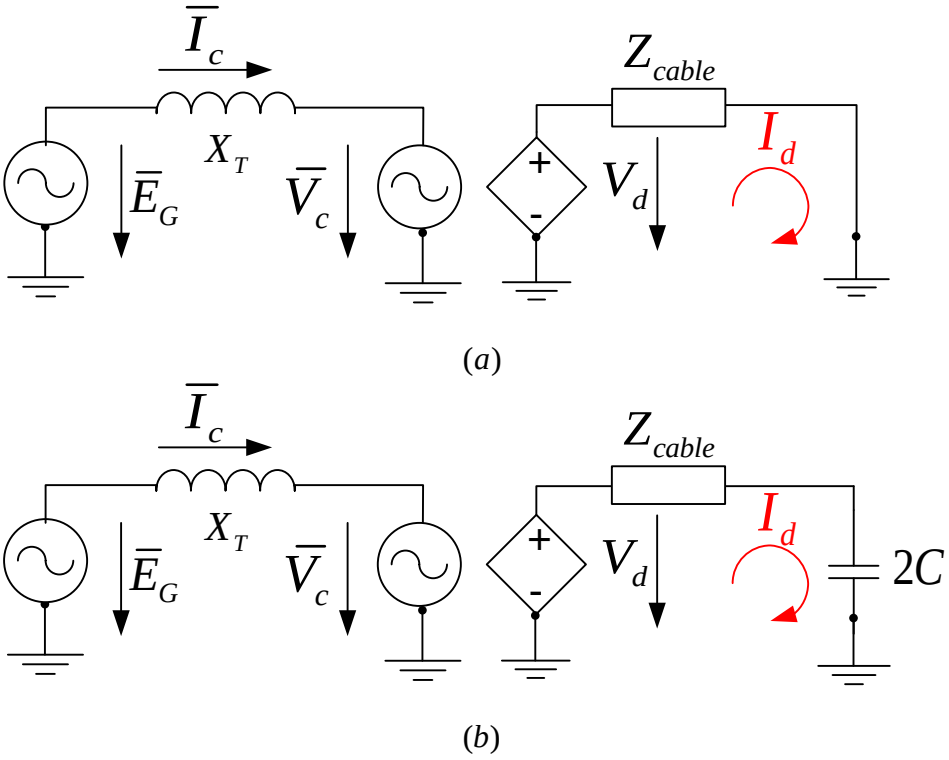


Figure 3.11: VSC-HVDC equivalent average circuit of a VSC in symmetric monopole configuration (a) after a line-to-line fault, (b) after a line-to-ground fault

Limitations There are certain limitations associated with this average model that need to be taken into account. First of all, the average model assumes that the DC side has either a constant voltage or a constant current with negligible ripple [46]. Therefore, the DC side is represented as voltage or current source. This can be applied only in case of normal operation and not during a fault, where transients take place. The equivalent circuits for the dynamic response of the VSC-HVDC system are seen in Figures 3.2- 3.9.

Secondly, the model assumes the DC line impedance is much smaller than the AC side one, for the ripple to be negligible [47]. In the simulated model this does not apply, as the DC side impedance is comparable to the AC supply lines impedance, thus making the response of the system more complex.

Moreover, there is the need for continuation. It is essential that the fault phase initializes correctly after switching from a controlled current source to a controlled voltage source VSC model on the DC side. On the DC side model switches are being implemented, that accommodate the shift between the controlled current source, used under normal operation and the controlled voltage source, which is employed during a fault. As the DC side model is only connected to the AC side by means of the DC fault current used in (3.18), the change of state for the AC side parameters is abrupt and results in unfiltered fluctuations.

Finally, the DC current at the converter output is not continuous during the period of commutation between the two controlled sources.

3.4.2 SimPowerSystems model

Taking the limitations of the average model into account, a simulation model is realized, making use of the SimPowerSystems library elements of Simulink. The VSC station is simulated as shown in figure 3.12.

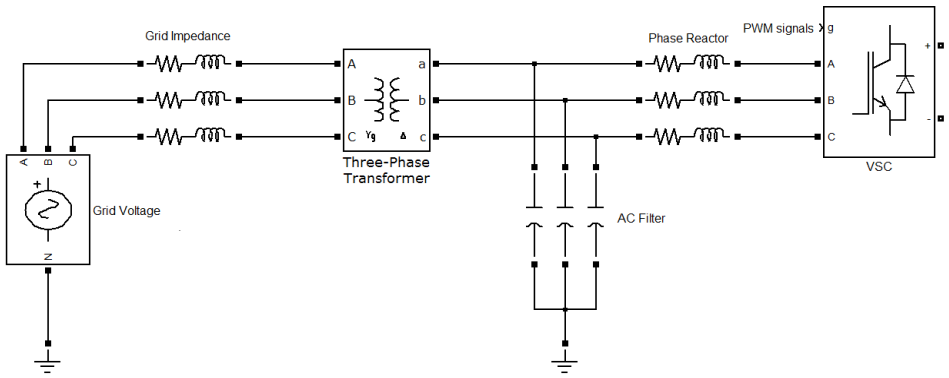


Figure 3.12: Matlab/Simulink VSC station model

The control system remains the same, following the principles presented in Chapter 2. Also here, PWM modulation is employed in order to drive the switches of the converter in normal operation, while in case of a fault the switches are blocked. Finally on the DC side, the average model controlled sources are replaced and the grid is instead directly connected to the output of the converter, thus providing a direct interaction between AC and DC side.

3.5 DC Breaker Technologies

The need for a high level protection of HVDC networks has led to the research and development of a variety of DC breaker models. Breakers provide a way to isolate faulty lines and to protect the connected equipment from HVDC line faults. Many parameters, such as on-state losses and time response for fault current interruption, have to be considered and compared, before a choice of technology is made. In this section an overview of high potential DC breaker technologies is provided, along with their most essential specifications, based on current research in this field.

3.5.1 Full Semiconductor / Solid State Breakers

Several topologies using solid-state switches have been proposed in the literature [30; 48; 49]. However, considering the device ratings, a large number of semiconductor switches has to be connected in series to withstand the maximum switching current and voltage. Figure 3.13 presents a topology of such a breaker.

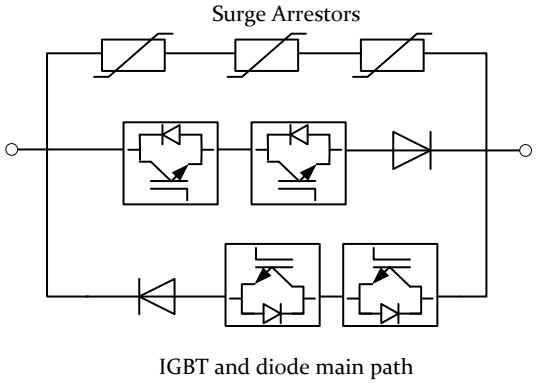


Figure 3.13: Solid-state breaker model

The DC breaker consists of three conduction paths. There are two main paths accommodating the bidirectional power flow, which have a number of switches connected in series and reverse conducting diodes. The number of switches depends on the voltage rating of the DC breaker. The diode is used to prevent DC current to flow through the anti-parallel diodes of the switches, when these are blocked. As a result, as soon as a fault is detected, the switches get blocked and the current commutates to the parallel connected varistors. The varistors prevent the fault current conduction and operate as energy sinks for the energy that the DC lines have stored during normal operation. Moreover, the surge voltage across the main path is suppressed to the clamping voltage of the surge arrestors [49].

Insulated gate bipolar transistors (IGBT), gate commutated turn-off (GCT) and gate turn-off are, at the moment, the preferred switches in solid-state breakers [30; 48]. Switching speed, which is essential for multi-terminal applications, is their main advantage. If detection time is kept short, the turn-off time and consequently the interruption time can be kept to a minimum value around 1ms [30].

Moreover, IGBTs have the inherent capability to limit the external current, during a short-circuit, which gives them an advantage over the other thyristor-type devices. However, the use of semiconductors in series introduces significant on-state losses to the system, while switching losses can be neglected. Considering this aspect of operation, IGBTs have three times higher conduction losses per switch than the other two types of switches [48]. Therefore, GTOs are preferred for such applications, also based on material costs. Solid-state breakers have only been tested so far for low (LV) and medium voltage (MV) DC grids [50; 30; 48], therefore as technology advances, device ratings increase and losses decrease, such breakers can provide a fast and reliable solution.

3.5.2 Hybrid Solid State Breakers with Mechanical Disconnector (Hybrid I)

This type of circuit breaker tries to compromise the switching speed with the on-state losses, by using two current paths for conduction and interruption. ABB proposed a modular hybrid IGBT DC breaker [51], which has a main path with one fast mechanical disconnector and a small number of semiconductor switches in series and the main breaker path, rated for full current and voltage breaking capability. The hybrid DC breaker is presented in Figure 3.14.

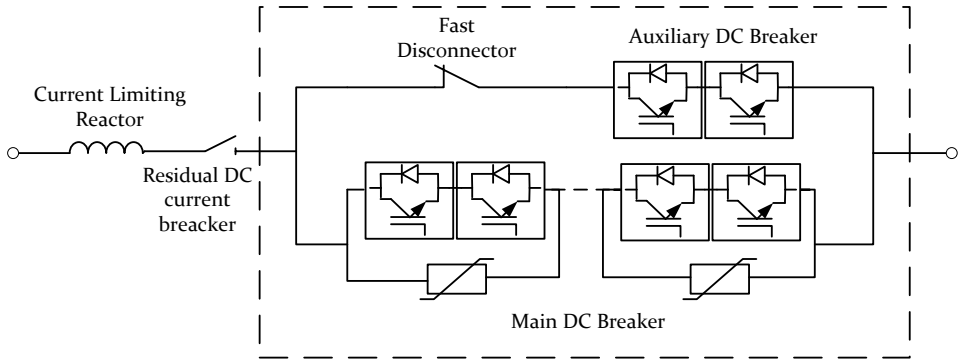


Figure 3.14: Hybrid solid state breaker model with mechanical disconnector

When a DC fault occurs, the auxiliary breaker on the main path commutates the current immediately to the main breaker path and the fast mechanical disconnector opens. Because the auxiliary breaker only needs to create a voltage high enough to commutate the current to the breaker path and because the disconnector isolates the breaker from the primary voltage, the auxiliary breaker is rated for lower voltage and current. Therefore, the forward voltage and subsequently its on-state losses are kept low during normal operation.

The interruption time is a bit higher than the full solid-state breaker because of the mechanical disconnector, however opening times of 2 ms are achievable if several mechanical switches are connected in series [51].

3.5.3 Hybrid Fault-Current Limiting Breaker (Hybrid II)

There have been many breaker topologies proposed that include the use of fast semiconductor switches and current-limiters or mechanical switches. Their main topology is shown in Figure 3.15.

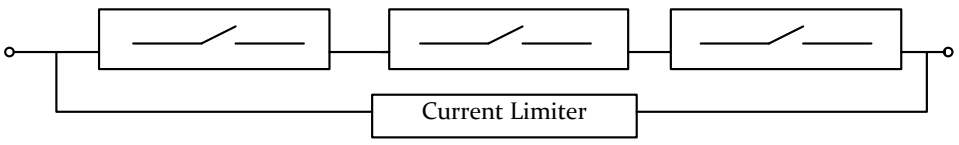


Figure 3.15: Hybrid fault-current limiting breaker general topology [48]

The current limiter path consists of an inductor and a capacitor in series or in parallel, acting as snubbers. As soon as a fault is detected, the switch is turned off and the current

is conducted through the reactive path. Due to the inductor, the current is limited below the short-circuit value and thus, the disturbance to the rest of the circuit is much lower than without the limiter.

As a result, simple mechanical switches can be used in series to isolate the line [48], although this can result to increased interruption times due to the total break time of common breakers (20ms) [52].

Because of the use of the inductor, overvoltages can occur till the fault current is successfully commutated. However, its presence is necessary to limit the current that goes to the capacitor directly after the switching [48].

There are also other hybrid topologies proposed in the literature, which make use of fast switches and are based on the same principle. One such topology is depicted in figure 3.16.

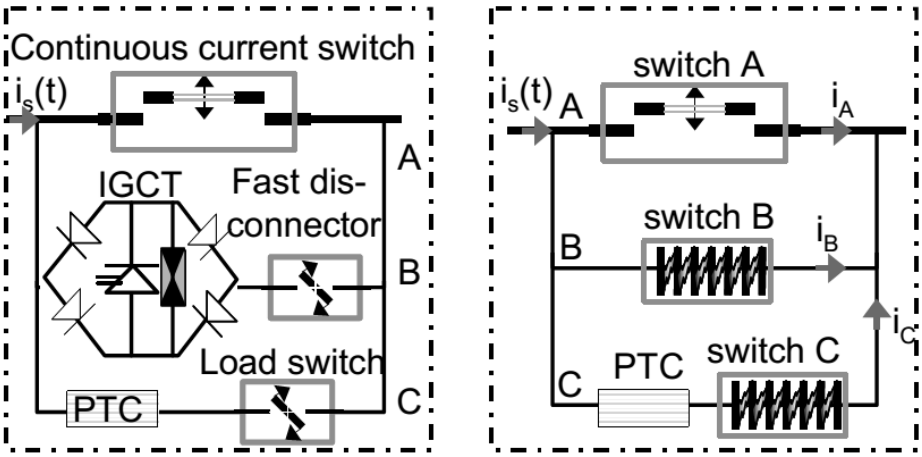


Figure 3.16: Other proposed hybrid breaker topologies [53; 54]

The concept shown in Figure 3.16 consists of three paths in parallel.

The first path consists of an ultra-fast switch, which opens within a few microseconds (μs) and commutates the current to the second commutation aid path.

The second one includes a four-diode bridge to accommodate bipolar fault current and GTOs, the number of which depends on the application, to help the commutation of the current to the last path, which operates as a current limiter. As soon as the current is zero on the second path a fast disconnecting switch is opened to isolate it.

Finally, the current limiter has a high positive temperature coefficient (PTC) resistor and a load switch, which can interrupt current at the first zero crossing.

In series with this limiting topology a mechanical breaker is inserted to meet the voltage-withstand requirements for a circuit breaker [54].

The topologies discussed in this paragraph have only been tested for MV networks and thus, an increase in current interrupting capability is necessary. Moreover, both bring along higher interruption times (5-30 ms) [30], due to the use of series mechanical breakers.

3.5.4 Active or Passive Resonance Breakers

These breakers have long been proposed for DC grids and are based on AC gas breakers (mostly SF_6). Figure 3.17 shows the basic topology of such a breaker.

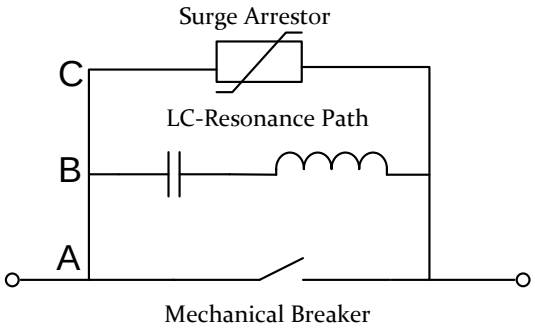


Figure 3.17: Resonance DC breaker

First of all, the breaker consists of three paths. The path that is used during normal operation comprises only a low-loss interrupter. As soon as a fault is detected, this switch opens, thus creating an arc. The arcing voltage is high and so resistors and an LC path are necessary to limit the commutation voltage.

The energy storage elements create an oscillating current through the main path interrupter, which depends on the frequency of the commutation circuit, as well as the parameters of the switch. When the oscillating current crosses zero, the switch is able to interrupt the current. The commutated current charges the capacitor C.

The surge arrestor used can limit the maximum voltage across the capacitor and as soon as this is reached the current is commutated to the energy absorbers, which dissipate the energy in the system and reduce the DC current to zero [55; 30; 56; 33].

Both active and passive resonance breakers have the same operating principle. However, passive resonance breakers have a limit for the maximum interruptible DC current, based on the voltage-current arc characteristics at high currents [57; 30]. More specifically, if the DC current surpasses the instability limit, $\left|\frac{di}{dt}\right| \geq 0$, the current through the interrupter has no zero crossings. In this case, a zero crossing has to be excited either through an external circuitry or through a precharged capacitor Cc, in the LC-commutation path, in series with another switch (Sc).

Once the switch Sc is closed, the precharged capacitor Cc gets discharged, a current is injected into the nominal path and consequently a counter current is induced [33]. In this way a zero crossing is created, enough for the switch to turn off.

Their main advantage is the low cost of the components and the low on-state losses. However, they are slower than the other technologies investigated and can only be used in combination with current limiters [30].

3.6 DC Breaker Comparison

A summary of the most important parameters of the DC breakers technologies, which were presented in the previous section, is given in Table 3.2.

For the implementation of the DC breakers in an HVDC network, they need to fulfil certain requirements. The most important are: the low total current interruption time, the low losses during normal operation and the ability to break high currents when subjected to high voltage stress.

As it can be seen from Table 3.2, none of the existing DC breaker technologies fulfils all the aforementioned requirements.

From the investigated circuits, only full solid-state breakers have a competitive breaking time of less than 1 ms, while the ABB proposed hybrid, has a combination of desired characteristics, with achievable times below 2 ms and very low on-state losses. However, it is not yet tested and operated at voltages above 120 kV. Therefore, more research is needed.

The main goal of this thesis is the study of the protection of MTDC networks and, on this basis, the most important parameter of the breaker technology is the total interruption time. Therefore, no focus is given to the individual transient response of each circuitry, but only interruption time is considered for the implementation of the different DC breaker simulation models.

The breaker is simulated as an ideal switch, which is controlled by an external controller. As soon as a fault is detected, a delay, corresponding to the total interruption time of each breaker topology, as provided in Table 3.2, is inserted. After this period, the switch is turned off.

For the simplification of the breaker model, several assumptions were made. First of all, it was assumed that the breaker technology does not influence the controller gains of the VSC station as, under normal circumstances, it does not change the characteristics of the DC line (RLC parameters). Moreover, all of the aforementioned breakers are included in the simulations, even though the hybrid solid state breakers with mechanical disconnector and the resonance breakers are yet only available for lower voltages than those simulated (640 kV).

Finally, the on-state losses, especially important for full solid-state breakers, were not taken into account during normal operation. It was assumed that the only losses in the grid are caused by the lines impedance.

Table 3.2: DC breaker technologies specifications

	Solid State Breakers	**Hybrid Solid State Breakers with Mech. Disconnector**	**Hybrid Fault-Current Limiting Breaker**	**Active or Passive Resonance CB**
Commutation time [ms]	0.1 switch	<0.2 switch ~0.25 disconnector	~0.1 switch <20 breaker 1-5 UFS	<20 breaker ~30 passive res. ~2 active res.
Energy absorption time [ms]	~1	~1	-	-
Total interruption time [ms]	<1	<2	<5-30	<60
Max rated voltage U_n [kV]	≤800	120 tested (up to 320 feasible)	AC-CB >500 UFS<12	≤550 available
Max breaking DC current [kA]	<5	9 tested (up to 16 expected)	~6-12 (estimated)	4 tested in operation (8 with active res.)
Expected power losses compared to a VSC station [%]	GCT ~30% GTO ~40%	<1% (few series switches)	negligible; only due to metallic contacts	negligible; only due to metallic contacts

3.7 Summary

The DC faults generally develop in three stages, as presented in section 2.3. During the first stage, the DC capacitors get discharged through the fault, whereas on the second stage the converter switches get blocked for their protection and the VSC acts as a diode bridge rectifier. In the final stage, there is a grid forced system response and the grid reaches a new steady state. This dynamic response of the system cannot be simulated using a VSC average model, due to several limitations. As a result, a SimPowerSystems®model can be developed instead.

To handle DC contingencies, several DC breaker prototypes have been proposed and tested in laboratory conditions. In this chapter, four DC breaker models were presented and compared, in section 3.5, based on their total interruption time and their on-state losses. Their main characteristics can be found in Table 3.2. The response of VSC-HVDC multi-terminal networks to DC faults, when using different DC breaker technologies, is further simulated and discussed in Chapters 5 and 6 for different HVDC grid topologies.

Chapter 4

Protection Methods without DC Breakers

4.1 Introduction

One of the main problems VSCs face when installed in MTDC networks, which inhibits their full exploitation, is the handling of DC faults. In Chapter 3 pole-to-ground and short-circuit fault cases were presented and theoretically analysed. From this analysis, it was concluded that the need for means to limit the initial fault currents and also for ways to isolate the faulty part of the system should be a research priority heading towards the realization of multi-terminal HVDC networks.

However, regular two-level VSCs cannot achieve the limitation of DC fault currents. Therefore, research should come up with different novel protection means. Based on the experience on the operation of AC grids, where AC faults can be isolated by means of robust AC breakers, research was focused on the realization of respective breakers that could handle DC contingencies. Although, this idea is easily applicable for AC applications, due to the natural zero-crossing of the current, it is difficult to be realized in cases where DC is used.

The DC breaker is required to be able to interrupt high currents that do not have a natural zero-crossing, to dissipate the high amount of energy that is stored in the inductors of the system and also withstand the voltage created at its terminals after the current interruption [33]. These requirements make DC breaker design a challenging research topic. First of all, fast switches with the aforementioned characteristics, which do not add high series power losses, are not available and need to be designed (Full semiconductor DC breakers). Secondly, the use of mechanical breakers inserts a high time delay which cannot be tolerated during DC faults, due to the high peak currents which will follow(Hybrid II DC breaker). Finally, the design of breakers to create artificial current zero-crossing (Resonant Breakers) is promising, however, not yet mature enough to achieve low interruption times [33].

Due to the aforementioned reasons, alternative methods to deal with DC faults are investigated. First, this chapter focuses on the idea of Multi-level Modular Converters (MMC) and its DC fault capability is presented and discussed. Next, another method for DC fault

handling, known as Handshaking Method, is presented, which makes use of a combination of fast mechanical DC switches and AC breakers.

4.2 Multilevel VSC

In Chapter 2 the two-level converter topology was presented (Figure 2.3). This VSC design, although simple in its control logic and structure, has disadvantages.

For HVDC applications each of the phase arms needs to be designed to withstand $V_{DC}/2$, which can be up to 320 kV, depending on the application. Consequently, several IGBTs need to be connected in series to match this rating. In the market, IGBTs are available with blocking voltage ratings up to 6.5 kV. Therefore, 50 IGBTs need to be connected in series in each of the six phase arms of the converter. This fact complicates the switching control, as the switching of all the IGBTs in one arm needs to take place simultaneously (within fraction of microseconds), otherwise there is severe stress on the IGBTs. At the same time, regarding their packaging, series connection of IGBTs structure-wise is not an easy task.

Moreover, two-level converters create rectangular waveforms of steep and high voltage steps, which require intensive filtering and smoothing to obtain sinusoidal voltage at the AC terminals, thus increasing the converter cost significantly [58]. Another important disadvantage of the two-level converter is the need for high switching frequency, which can be up to 2 kHz in order to reproduce the AC voltage output, resulting in high switching losses.

Finally, during every commutation, due to the two-level switching, a high voltage derivative du/dt is produced, which stresses not only the IGBTs, but also the phase inductor connected in series with the converter, creating high levels of electromagnetic interference (EMI) [59].

Due to these inherent disadvantages of two-level converters, a natural tendency arose to increase the number of steps from which the AC voltage output of the converter switches, to create a better sinusoidal waveform.

4.2.1 Three-Level Converter

The first step towards multi-level converters was to create three-level converters. The most important topologies of this technology are the multi-level diode clamping and the multi-level flying capacitor [60; 61].

Multi-level Diode Clamping In this topology diodes are utilized to clamp the AC voltage at zero, creating an additional switching step. To achieve this, the DC link capacitors are split into two arms, creating a middle point. The topology scheme is presented in Figure 4.1.

Two clamping diodes are used for each phase arm, which are connected to the DC link middle point at one end, while their other end is connected in the middle of the phase arm.

Working principle The switching logic of this topology is simple and can be summarized in Table 4.1, which shows the switching state of each of the phase IGBTs, needed to produce a specific voltage output [61].

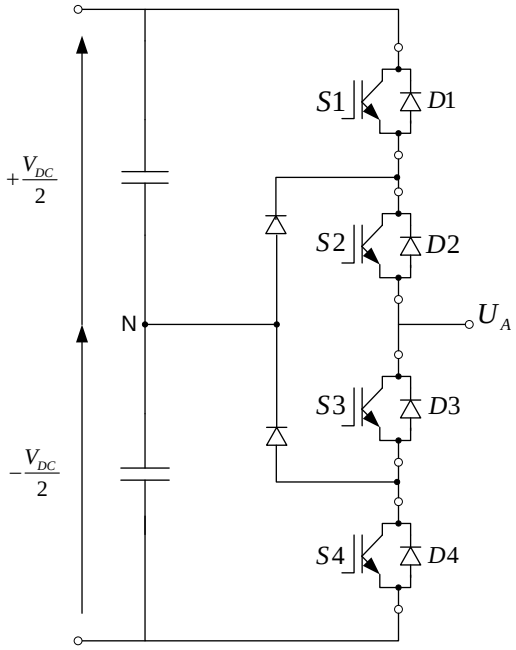


Figure 4.1: Three-level diode clamping converter

Table 4.1: Switching states for three-level diode clamping converter

	Switching States			
Voltage Level	S1	S2	S3	S4
$+V_{DC}/2$	on	on	off	off
0	off	on	on	off
$-V_{DC}/2$	off	off	on	on

When the upper phase arm switches are on and the lower arm switches off, the voltage at the point A, with respect to the DC link middle point, is $+V_{DC}/2$, whereas when the opposite occurs V_{AN}=$-V_{DC}/2$. For the intermediate voltage state to be created, S2 and S3 only need to be on, hence, $V_{AN} = 0$. As seen, the diode-clamp three-level VSC working principle is straightforward and thus is easily extensible to more levels.

Multi-level Flying Capacitor As the name suggests, this topology uses capacitors instead of clamping diodes. More specifically, in the three-level topology one capacitor is used, which connects the middle of the upper and lower phase arm. This capacitor is charged to $V_{DC}/2$, which, depending on the switches on-off state, can be connected in series to the phase to either add or subtract to the total output voltage. In this way an intermediate step of null voltage is added in the AC voltage generated output. Figure 4.2 presents an overview of the topology.

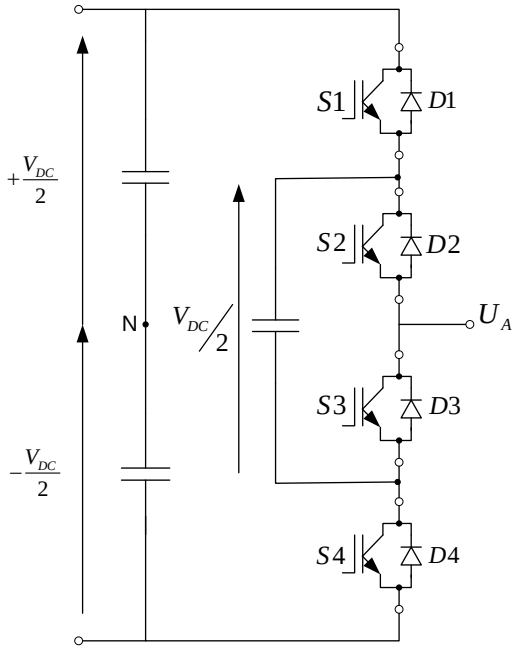


Figure 4.2: Three-level flying capacitor converter

Working principle In order to produce the necessary voltage states, only two of the phase leg switches need to be on at any time. In this case, the null voltage state is possible in two distinct switching combinations: if S1 and S3 (or S2 and S4) are on simultaneously then the flying capacitor is connected in series with the phase current and $V_{AN} = 0$.

The switching states needed to produce each voltage level are presented in Table 4.2 [61; 8].

Table 4.2: Switching states for three-level flying capacitor converter

	Switching States			
Voltage Level	S1	S2	S3	S4
$+V_{DC}/2$	on	off	on	off
0	off	on	on	off
	on	off	off	on
$-V_{DC}/2$	off	on	off	on

Discussion Both of the presented topologies have advantages when compared to the classical two-level converter, but their use also introduces some drawbacks.

The total number of IGBTs in the three-level converter for HVDC transmission is not necessarily higher than in two-level VSCs. The main difference is that each valve in a

three-level converter needs to withstand half the voltage when compared to the two-level case.

Moreover, both of the presented three-level concepts can be expanded to more levels, resulting in lower harmonic distortion of the AC voltage, lower switching losses, as well as lower filtering needs. The more levels introduced, the smaller capacitors needed on the DC link of smaller dimensions.

However, their cost is a main disadvantage. The diode clamping converter requires a high number of diodes, which not only increases cost, but at the same time the circuitry complexity. Additionally, diodes complicate the insulation and cooling design of the valves. Regarding the flying capacitor topology, more capacitors are necessary, which introduces dimensioning problems. These are some of the reasons why such converter topologies are difficult to be used in HVDC applications.

Finally, regarding DC fault handling, both topologies do not differ from the two-level converter, and are subjected to high fault currents in case of a DC fault.

4.3 Multi-level Modular Converters

In 2003, Professor Marquardt from the Technical University of Munich [62] proposed the concept of modular multi-level converters (MMC).

The proposed converter consists of three phase units. Each phase unit comprises two converter arms, each with a converter module and a converter reactor. Each converter module consists of numerous power modules connected in series, whose number depends on the application. Each power module contains two or four IGBTs as the switching elements, depending on the design (half bridge or full bridge), a DC storage capacitor and other valve firing electronics.

Unlike other VSC topologies, there is less difficulty in connecting modules in series with this converter topology. The converter number of levels can simply be increased by connecting more submodules in series. Hence, the submodules are the elementary building blocks of the MMC system.

The main advantage of this topology is the fact that since there are n-1 capacitors stacked, n-1 respective voltage levels are available to synthetize the desired n-level AC voltage. Therefore, the AC voltage created has an almost perfect sinusoidal shape and the filtering or smoothing needs are minimum. At the same time, the voltage derivative is very low, resulting in less stresses on the switches and on the phase reactor and less produced EMI.

Moreover, the more levels are introduced, the lower the switching frequency which results in less switching losses in the converter and increased overall system efficiency. On the other hand, more complex structures with more switching elements increase control complexity and introduce higher system costs.

Three companies currently offer HVDC modular multi-level converters: ABB, Alstom and Siemens. Next, an overview of the different commercially available technologies is given.

ABB HVDC LIGHT ABB introduced the concept of a cascaded two-level converter in 2010 [63]. The operating principle is the same as the modular multi-level converter, however a different name is used to stress that their solution of press-packed IGBTs, used for two-level converters, is extended to accommodate the increase of converter levels. More specifically, press-packed IGBTs are connected in series to form the converter phase arm. The valves are connected as shown in Figure 4.3.

From Figure 4.3 it can be seen that half-bridge modules, consisting of eight IGBTs in series per submodule pole and one capacitor are used as primary blocks. These are then connected in series to create each phase arm. Inside each submodule, ABB introduces series connection of devices also in the multi-level converter. In this way it supports the redundancy of the system and avoids system failure in case a single device experiences a problem. In case one switch fails, the rest in the same pack are able to share the slightly increased voltage and operation is continued without interruption. The IGBT that failed enters a short-circuit failure mode (SCFM), which means it can carry the load current until the next maintenance takes place [64].

Another important fact is that the switching frequency of each cell is approximately 150 Hz, which is only three times higher than the AC system fundamental frequency. The effective switching frequency per phase leg can be calculated by multiplying the cell switching frequency by the number of employed cells. As a result, the dynamic response of the converter is very good, while at the same time the overall losses are kept low, circa 1% [65].

Siemens HVDC PLUS Siemens was the first company to introduce the M2C technology for HVDC applications. Based on the original concept of Professor Marquardt [62], each converter arm operates as a controllable voltage source with as many voltage steps as the number of submodules. Each converter phase arm is built by submodules, which are identical, but controlled individually. The HVDC PLUS configuration is shown in Figure 4.4 [66].

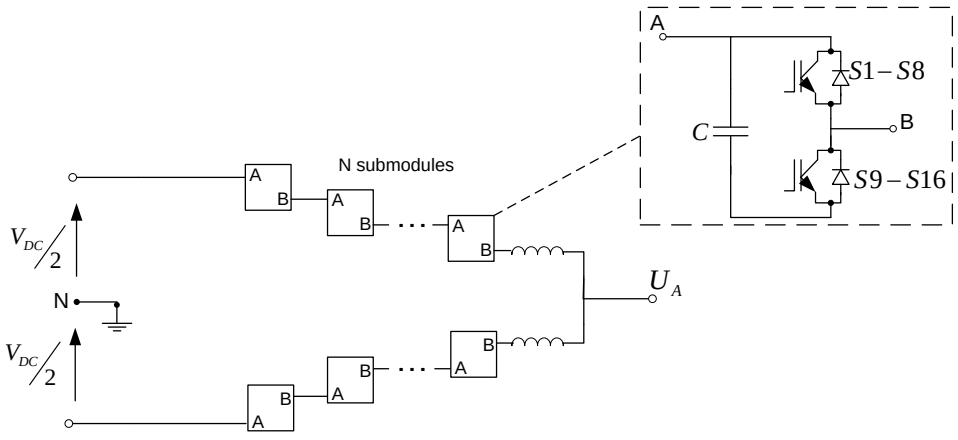


Figure 4.3: ABB HVDC LIGHT topology and half-bridge submodule

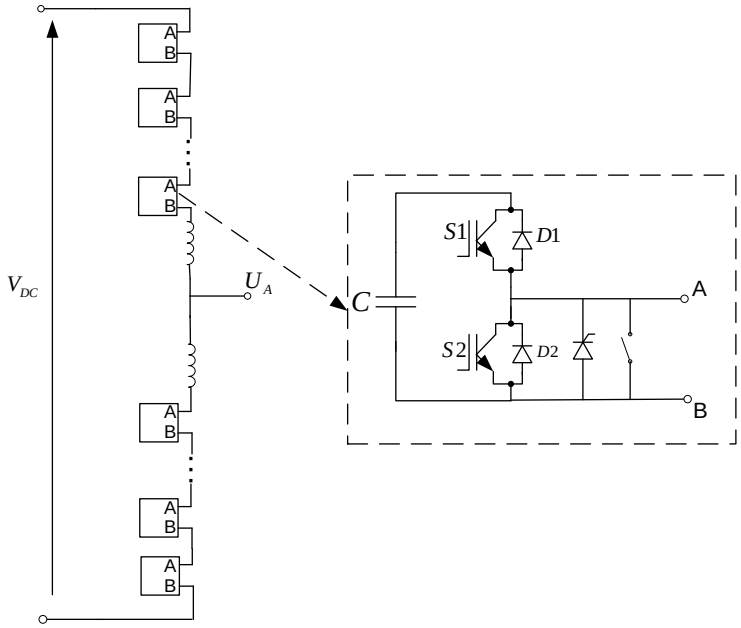


Figure 4.4: SIEMENS HVDC PLUS topology and half-bridge submodule

The power submodule contains an IGBT half bridge and a DC capacitor for energy storage. Depending on the way the submodule is switched, the capacitor is either bypassed or connected in series to the phase current. The switching states of half bridge modules will be further explained in section 4.3.1.

In case of a module failure, the system should be able to withstand the fault and not interrupt the energy transfer. Therefore, a high-speed bypass switch is implemented, which is turned on in case of an emergency reliably by-passing the module. In this way, operation is not interrupted and the excess voltage stress on the rest of the arm modules is equally distributed.

Moreover, equal voltage distribution is ensured through periodic control of the capacitor voltage on each module. When necessary, selective switching of power modules can be used to balance the voltages between the submodules.

Additionally, phase reactors are connected at each phase arm in order to reduce the fault currents and their rate of rise, in case of faults within or outside the converter, as well as to reduce balancing currents between the phase units.

Finally, each submodule has a press-pack thyristor, which is used in case of DC faults to protect the free-wheeling diodes of the switches till the AC breakers open. The response of half-bridge modules to DC faults is further explained in section 4.3.

Alstom HVDC MAXSINE Alstom has also developed a modular multi-level converter, known as HVDC MAXSINE. The operating principle is the same as the MMC, however, unlike the previous two solutions which use half-bridge modules in their converters, Alstom

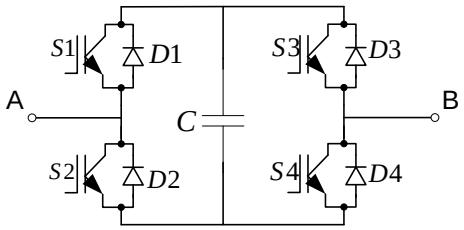


Figure 4.5: Alstom HVDC MAXSINE full-bridge submodule

has developed full-bridge modules, mainly driven by the need to provide a solution for the DC fault handling problem. In Figure 4.5. the general scheme of HVDC MAXSINE is given.

As with Siemens HVDC Plus, connecting a number of submodules in series, creates the multilevel circuit. The number of series connected submodules depends on the application.

The submodule, shown in Figure 4.5, contains full-bridge IGBTs as switching element (cooled by water heat sinks) and the DC capacitor (oil free design). In case a submodule fails, a mechanical switch is used to short-circuit and successfully provide uninterrupted energy transfer.

However, the use of full-bridge modules increases the number of semiconductor switches used in the design, thereby resulting in higher cost as well as higher losses (1.3-1.4%) than the half-bridge modules [67]. In order to overcome this problem, Alstom has proposed a hybrid topology, which is presented in Figure 4.6 [67; 68].

This hybrid series connected converter tries to combine the advantages of half-bridge modules (low harmonic distortion and low losses) with the DC fault response of full-bridge modules. Series connected IGBTs are arranged to form the converter and they are used as director switches. The full-bridge modules are then switched in a way to produce the desired AC voltage waveform which meets the requirements of the grid. The full-bridge IGBTs are switched at the frequency of the AC supply, but also at near zero voltage, which decreases significantly the switching losses. More specifically, the positive cycle of the sinusoidal waveform is constructed by the upper arm whereas the negative cycle is produced by the lower arm. At the same time, the converter is still very responsive to faults and it has the capability of blocking the DC fault current [69].

Finally, in VSC-HVDC transmission links there is not usually the need to invert the DC voltage of the converter. However, Alstom claims that by using the hybrid MMC topology with full-bridges it is possible to reverse the voltage on the DC-side of the VSC, making it easier to operate this converter alongside LCC-HVDC [70].

4.3.1 Half-bridge modules

In this section the operating principle of half-bridge modules is explained and the DC fault response of the system is discussed.

A multi-level converter is generally switched in the way presented in Figure 4.7. In this figure a 8-level converter is shown. Each submodule has two operating states, in which

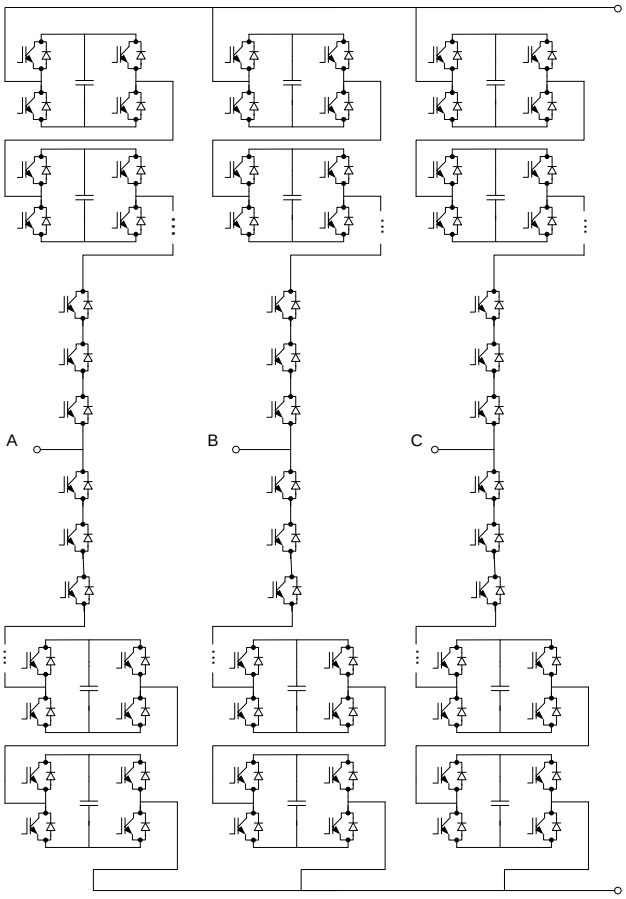


Figure 4.6: Alstom hybrid series connected topology

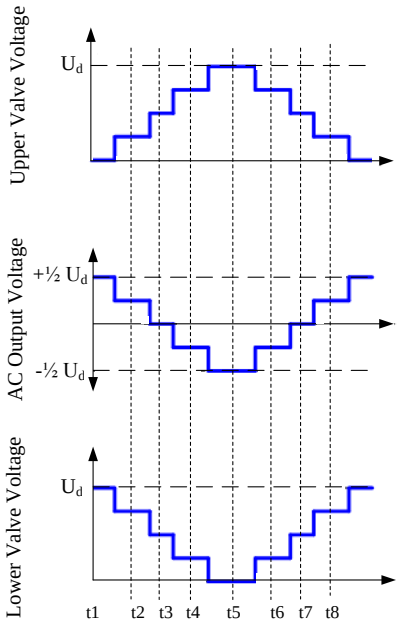
either the DC capacitor is connected in series to the AC current or it is bypassed. Therefore, it can be simply simulated by a two-state switch. In this way, each phase leg can be assumed to work as an independent controllable voltage source.

Based on this principle, more voltage levels can be created by cascading submodules, resulting in an almost perfect sinusoidal AC voltage waveform that needs little filtering or smoothing.

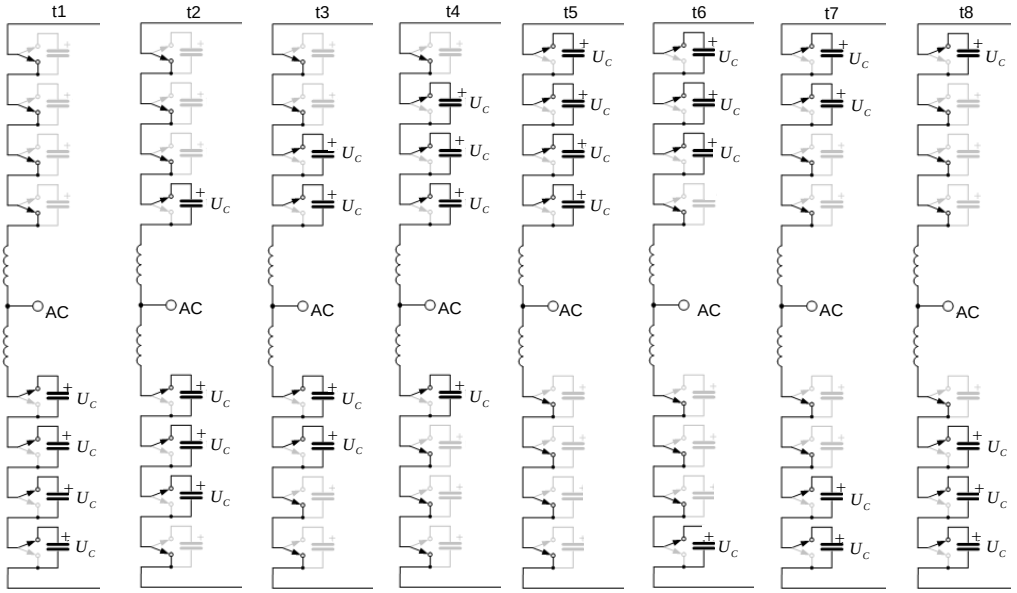
More specifically, based on the current direction and the IGBTs switching states, the following situations can be distinguished [71]:

- *S1 and S2 are off*: This state occurs during the initial start-up of the system and in case of a fault. The current flows through the anti-parallel diode D2 and the submodules are by-passed in case AC current flows to the DC grid. If current is coming from the positive pole of the DC grid, the submodule capacitor is connected in series and is thus charged.

- *S1 on and S2 off*: Depending on the current direction, the capacitor is either getting



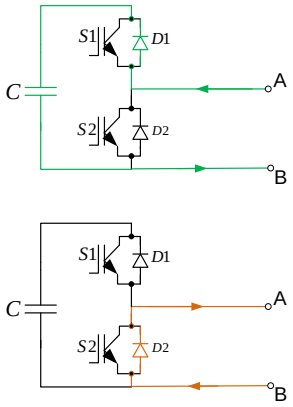
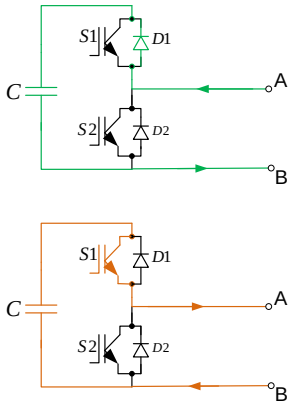
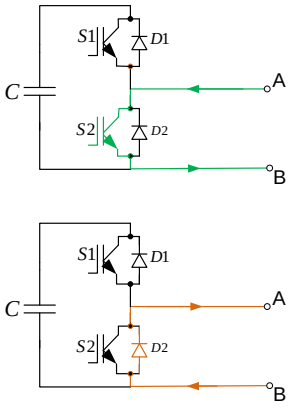
(a)



(b)

Figure 4.7: a) Voltage waveforms, b) 8-level converter switching states

Table 4.3: States and Current Paths in a half-bridge submodule

S1 & S2 Off	S1 On	S2 On
		

charged through D1 or discharged through S1.

- *S1 off and S2 on*: In this case, irrespective of the current direction, the submodule gets by-passed, either through S2 or D2 and thus the capacitor state remains unchanged.

The aforementioned situations are displayed in Table 4.3. The green line represents the current flow from the AC grid to the DC network and the orange one represents current flowing in the opposite direction.

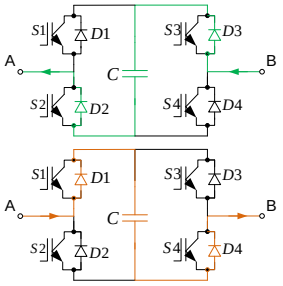
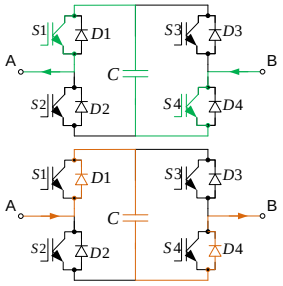
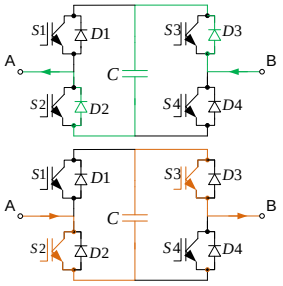
In general, in case of a DC fault, the converter arms cannot block the fault current. As soon as a fault is detected, the IGBTs are blocked for their protection, but the anti-parallel freewheeling diodes still provide a path for the AC current to the DC grid, thus feeding the fault (current path through D2 in Table 4.3).

The fault generally develops in three stages, as shown in Chapter 3. The first stage takes place between the moment the fault occurs and the moment the IGBTs get blocked. Because of its brief duration and the high inductances connected in series (AC reactor and smoothing reactor of phase arm) the AC currents can be assumed to remain constant during the first stage [72]. As soon as the fault occurs, each phase arm inductor is subjected to a voltage $V_{DC}/2$.

After the IGBTs are blocked, the fault current start flowing through the anti-parallel diodes. The arm inductors are opposed to the increase of the current and they exhibit a voltage of $-V_{DC}/2$, thus decreasing the circulating current. This cannot happen in the two-level converter, as there are no phase arm inductors, but only smoothing reactors on the AC side [72].

As soon as the circulating current drops to zero, the current infeed from the AC grid increases and the converter is transformed into a three-phase half wave rectifier (see Figure 3.3). As a result, the duration of this stage mainly depends on the size of the inductors, as they determine the rate of current change.

Table 4.4: States and Current Paths in a full-bridge submodule

All switches Off	S1 On & S4 On	S2 On & S3 On
		

Afterwards, the fault current can only flow through the diodes of the upper arm of the converter and this consists the third stage of fault development.

To provide an alternative path for the fault current Siemens implemented a parallel-connected thyristor, which reduces the load stress on the switch diodes, as these diodes generally have low capability of withstanding high surge currents. In case of a fault, a press-pack thyristor, with higher surge current withstanding capacity, connected in parallel is fired [72]. As a result, most of the fault current flows through the thyristor, protecting the diode until the AC breaker opens.

Taking the fault stages into consideration, the thyristor firing time is an important variable that defines the maximum current the diode will experience during a fault. If the thyristor is fired before the circulating current becomes zero (third stage), the diode peak current will be lower. The exact values are difficult to be determined, as they depend greatly on the network parameters. The state space equations describing the second stage can be found in the pole-to-ground fault analysis in Chapter 3 (see equation (3.4)).

In conclusion, the phase arm reactors play an important role in reducing the fault currents and their respective rate of rise. Moreover, the use of a thyristor or a fast mechanical switch in parallel to the submodules is essential for their protection when subjected to DC faults. However, these measures can only provide a limited time protection to the converters till the AC breakers are activated. There is no means of blocking the DC fault current through half-bridge modules and therefore other isolation measures need to be implemented.

4.3.2 Full-bridge modules

In contrary to half-bridge modules, the utilization of full-bridge modules can be a solution to the DC fault handling issue in multi-terminal DC networks.

Full-bridge switches can only be switched in pairs. Depending on the functioning switch pair, the current direction states are depicted in Table 4.4, where the green line represents the current flow from the AC grid to the DC network and the orange one represents current flowing in the opposite direction [61].

In case of a fault, the H-bridge cells have the capability of suppressing the fault current [73]. Initially, a surge current is allowed to flow through the IGBTs and feed the DC fault. However, as soon as the IGBTs are blocked, there is only one available current path through the series and reverse connected DC capacitors of the submodules. Moreover, the DC capacitors cannot get discharged through the fault, due to the configuration of the submodules. The total capacitor voltage of a phase leg is equal to the pole-to-pole DC voltage. As a result, the fault current can be limited and there is no need to trip the AC breakers [67]. In such case, a DC breaker with low current rating can be used to isolate the faulty line. Nevertheless, in case of a DC fault in a MTDC network, even with full-bridge modular multi-level converters, it is still necessary to isolate the faulty line to regain normal operation.

During a short-circuit fault, the fault current follows the path depicted in Figure 4.8, via the antiparallel diodes and through the submodule DC capacitors.

Based on this operating principle, other hybrid topologies have been proposed, e.g. the use of cascaded H-bridge cells in series on the AC side of the converter along with the use of half-bridge modules on the converter phase legs [74].

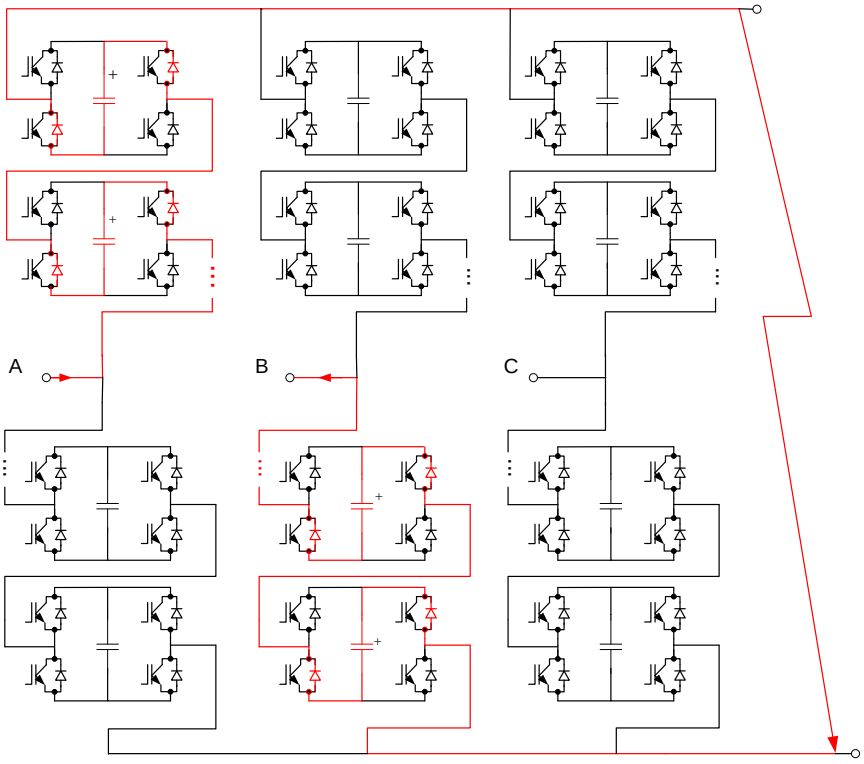


Figure 4.8: Alstom full-bridge modular converter fault response

4.4 AC Breakers

Modular multi-level converters consisting of full-bridge submodules are the only known VSC technology that has the capability of suppressing the high currents generated in case of a dc fault and thus protect the converter. However, all other known VSC topologies need either AC or DC breakers in order to isolate the fault.

The AC breakers take a long time, up to 100 ms, before they open. In the meanwhile, other protection measures for the converter free-wheeling diodes, such as parallel thyistors or fast mechanical switches, are required in order to avoid a converter failure.

As soon as the AC breakers open, the AC current infeed to the DC grid stops and the system gets de-energized. However, in order to achieve a complete system de-energization, all of the interconnected HVDC stations will need to activate the AC breakers. A restoration of the DC network requires the isolation of the faulty line and a new start-up process.

This situation is not admissible for a multi-terminal system. It is a costly option and requires the complete isolation of all interconnected stations, thus resulting in demanding situations for the AC grids (e.g. high power shortage or even blackout).

To restore the system operation in as minimum time as possible, methods of locating the fault need to be developed along with means to isolate the faulty line as soon as it is identified.

To date, several methods were developed to quickly locate a DC fault in a multi-terminal system. The most important of these is the wavelet method [75]. In this method different kinds of DC faults can be diagnosed based on the frequency content of the faults, which are extracted using wavelet decomposition [32]. The wavelet energy is then calculated for all the positive and negative DC lines and compared to a database of energy values describing a fault case, so that the faulty line can be distinguished [75; 32]. For further localization of the fault, the travelling wave method can be used [75]. This is based on the travelling wave propagation speed of a lossless line which is equal to:

$$v = \frac{1}{\sqrt{L'C'}} \tag{4.1}$$

where L',C' are the per unit length parameters of the line. Considering this value and the time it takes for the fault generated wave to reach a discontinuity (a station terminal), the precise location of the fault can be determined [76].

Apart from these advanced methods, a simpler control strategy, which makes use of a combination of fast mechanical DC switches and AC breakers in order to isolate a faulty line and quickly restore the system, known as the Handshaking Method, is presented in the following section.

4.4.1 Handshaking Method

The Handshaking Method to protect multi-terminal DC networks was first proposed in 2003 as an alternative cheaper method of fault isolation compared to the expensive and the, then not yet available, DC breakers [77]. This method can be applied to all grid interconnections

and only uses local measurements at each station terminals. It is thus assumed that no communication means are necessary, which reduces implementation costs.

The method is based on the use of conventional fast DC switches at both ends of a line, and the use of AC breakers required for isolating the AC grid. To present the method, a simple meshed three-terminal network is used [77; 78]. The implemented network is shown in Figure 4.9.

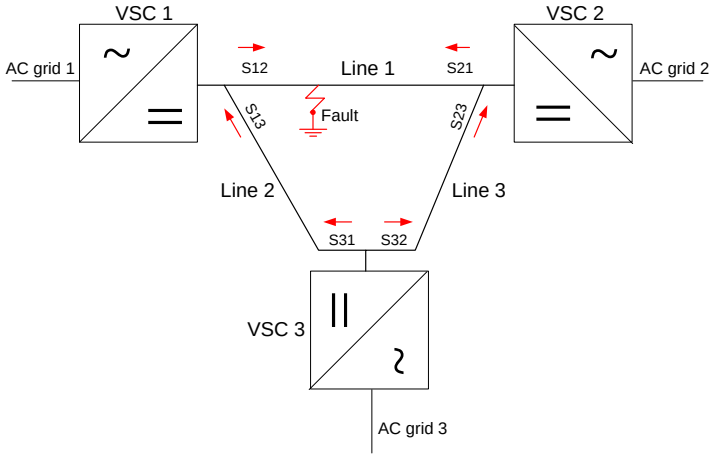


Figure 4.9: Three-terminal meshed network for implementation of the Handshaking Method

The 'Handshaking Method' implementation can be divided into 4 main steps [78]:

Step 1: Selection of Potential Faulty Line Each converter monitors the current and voltage at its terminals with a specific sampling frequency. The identification of the potential faulty line is based on the difference between the pre-fault and the post-fault measurements at each station.

When a fault occurs, the currents from each station are redirected towards the fault point. Based on this observation, visible in Figure 4.9, the selection of the DC switches that need to be opened will be determined.

As soon as a fault is detected, the IGBTs of the stations are blocked for their protection and a signal is given to the AC breakers to open. The opening times of the breakers differ, however a time of 100 ms can be assumed to be representative [78].

Based on the comparison of the VSC measurements, each of them needs to select a DC mechanical switch to switch off, which corresponds to the potential faulty line. In general, the selection principle is that the DC switch at each converter terminals which carries the largest positive current (exiting the converter) is selected to be opened. In this case, VSC1 and VSC2 had a positive and a negative current measured at the lines to which they are connected. Consequently, S12 and S21 meet the opening criteria, as they were the switches carrying a positive current after the fault occurence.

Regarding VSC3, both currents through switches S31 and S32 are positive. Therefore, the selection of the switch to open needs to be based on extra criteria. The line which meets

at least one of the following requirements is selected:

1. The line, in which the incremental current change (Δi) first exceeds a threshold value, before the IGBTs are blocked. The current change is given by the equation:

$$\Delta i_{kix} = i_{kix}(t) - i_{kix0} \tag{4.2}$$

where the subscript k refers to the number of the line; i refers to the VSC number and x refers to the positive or negative pole; i_{kix0} is the local average of $i_{kix}(t)$.

2. The line, in which the incremental change of active power (Δp) first exceeds a threshold value and has a negative sign. If a pole-to-pole fault occurs, Δp is defined as:

$$\Delta p_{ki} = \Delta v_{DCi} \cdot \Delta i_{ki} \tag{4.3}$$

where Δv_{DCi} is the incremental change in the DC voltage at station i, and Δi_{ki} is the incremental change of current and is equal to $\Delta i_{ki} = 0.5 \cdot (\Delta i_{kip} + \Delta i_{kin})$; i_{kip} is the current flowing on the positive pole and i_{kin} is the one flowing on the negative pole of line k from/to VSCi.

3. In case of a pole-to-ground fault, p_0 is checked, if it exceeds a certain value. p_0 is calculated via the formula:

$$p_{0ki} = 0.5 \cdot v_{divi} \cdot (i_{kip} - i_{kin}) \tag{4.4}$$

where $v_{divi} = 0.5 \cdot (v_{pi} - v_{ni})$ is the DC voltage divergence at VSCi.

Based on these criteria, VSC3 can either select S31 or S32 for opening and subsequently identify line 2 or line 3 as the potentially faulty one. In the specific case study, S31 was selected.

As soon as the AC breakers open, the fault currents are extinguished from the grid. The network gets de-energized and the next step of the method takes place.

Step 2: Opening of Potential Faulty Lines DC Mechanical Switches In this step the fast DC switches, which were selected previously, are switched off. As soon as the current and voltage on each line has dropped to zero the DC switches are able to open. As a result, in the present case study, the selected switches were S12, S21 and S31. Through this process, line 1 is isolated as both switches at its ends were opened. In all the rest of the lines, only one switch was opened. This can be attributed to the fact that during a fault there is only one line in which the currents have opposite directions at its ends and this is the faulty one. The opening of the fast DC switches is shown in Figure 4.10.

Step 3: Re-charging of DC Capacitors After the opening of the fast DC switches, the AC breakers are ordered to reclose. This is assumed to take the same time as the opening process; approximately 100 ms. As soon as the AC breakers have closed, the DC link capacitors start getting charged. The converter IGBTs remain blocked, thus the converter acts as a three-phase full-bridge diode rectifier charging the DC link up to the peak phase-to-phase value of the AC converter side.

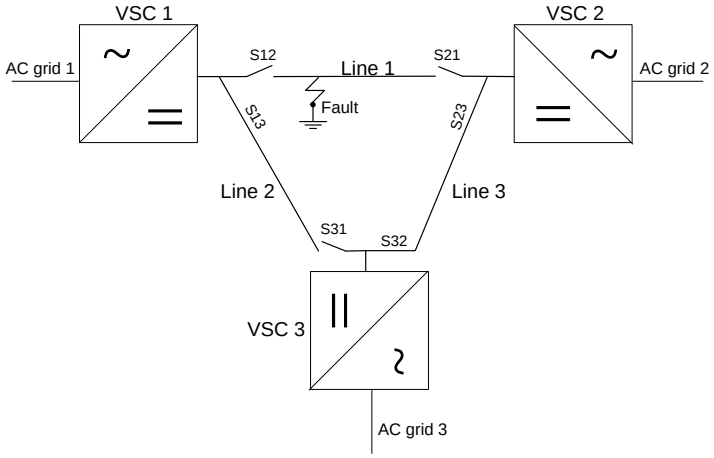


Figure 4.10: Opening of the selected fast DC switches

Step 4: Re-closing of DC Switches As soon as the DC voltage is restored, the DC fast switches are able to reclose only if the voltage of the DC line voltage at the switch is close to the DC voltage at the VSC terminals. In this case, S31 is able to reclose, as line 2 is connected to VSC1 through the closed DC switch S13. However, S12 and S21 remain opened, because only the VSC terminals have a high DC voltage, as the line is disconnected and has already been discharged by the fault. After the successful isolation of the faulty line, the VSCs are ready to be deblocked and the system can be restored to normal operation. The reclosing of S31 for restoring the system operation is presented in Figure 4.11.

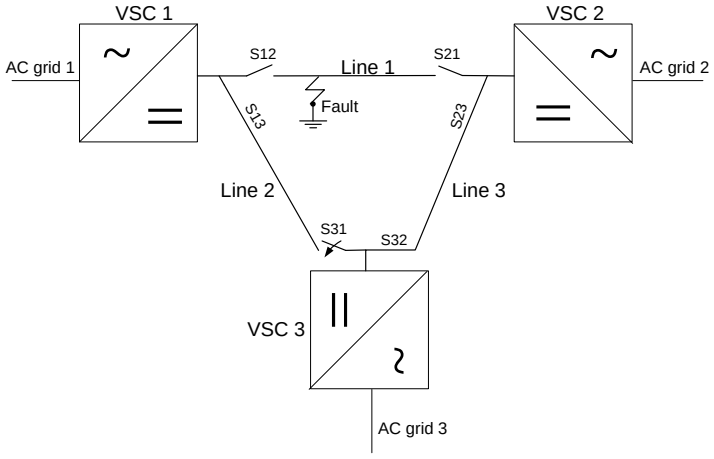


Figure 4.11: Reclosing of fast DC switches

4.5 Conclusions

The multi-level converters provide high AC voltage quality, reducing the station filtering and smoothing needs. However, MMC configurations which use half-bridge submodules cannot handle the high DC fault currents. Their response does not differ from the two-level converters, analysed in Chapter 3, and thus, AC breakers and/or DC breakers are required to isolate the fault and restore normal oreration. However, full-bridge modules introduced by Alstom have the capability to suppress the DC fault current and even drive it to zero, by connecting opposing DC voltages, via the submodules DC capacitors, in series with the fault current. Therefore, DC breakers with lower current ratings can be used to isolate the faulty line and the AC breakers tripping can be avoided.

The 'Handshaking Method' provides an alternative solution to fast location and isolation of a faulty line, as well as fast restoration of a multi-terminal network, without the use of expensive DC breakers. The only equipment required are AC breakers, which are already installed in the system and only two fast DC switches per DC line on the multi-terminal network.

The control is performed simultaneously at all the VSCs and the time needed does not change with the size of the network. As a result, the main time constraint in the method is posed by the AC breakers and the fault detection schemes presented.

Another advantage of this method is the fact that other fault detection and location methods can be applied without changes in the overall strategy. Moreover, there is the possibility, in a large network, to use DC breakers to separate the system in different independent parts to decrease the impact of a possible fault.

Finally, the criteria that are applied throughout the implementation method (faulty line selection criteria, reclosing of fast DC switches), as well as the fact that no communication means are necessary, increase the method reliability and allow the system successful restoration.

Chapter 5

DC Fault Analysis: Bipole with Metallic Return

5.1 Introduction

In Chapter 2, the main VSC controllers and the basic HVDC grid operating topologies were introduced, while in Chapter 3 the VSC-HVDC system response to DC faults was presented and four main DC breaker models, proposed in literature, were discussed. In this chapter, a simulation model to evaluate the performance of a four-terminal HVDC network under DC fault conditions was designed and implemented in Matlab/Simulink, using the VSC-HVDC models introduced in the previous chapters. This chapter presents the simulation results for the bipolar HVDC topology with metallic return, based on which the design characteristics of the DC grid are discussed and validated.

The main focus of this chapter is the positive line-to-ground fault response of a bipolar topology with metallic return. Based on the probabilities of DC faults presented in Chapter 3, pole-to-ground faults are more common than line-to-line faults, especially for submarine DC cables, and thus, they are the focus of this thesis. In order to deal with the fault, several aspects are considered. Limiting reactors are introduced at the end of each DC line to limit the increase rate of the fault current and provide additional time to the controllers to detect the fault before the converters experience the peak current.

Moreover, an overview of the used fault detection methods is presented along with a description of their operating principle. A distinction is also made between primary protection schemes and back-up methods for the sake of completeness. In case there is a problem, e.g. with the communications, the back-up protection schemes are activated to detect the fault. However, both elements have disadvantages and contradictory characteristics.

Therefore, a performance evaluation and comparison of all the proposed schemes is made, while the interruption times of theoretical DC breakers are also included in the investigation due to their importance for the coordination of the system. The whole analysis is carried out for a positive line-to-ground fault, considering negative line-to-ground fault to be symmetrical.

5.2 Network Configuration

Among the possible multi-terminal HVDC grid topologies presented in Chapter 2, the bipolar configuration with metallic return appears to be the most promising and representative. The main advantage of the bipolar topology is its capability to transfer half of the station power in case of a line-to-ground fault. The transferred power can be even more, if the station has an overload capability. Therefore, the stations continue to be connected and there is no need for a complete shut down and restoration of the system. Moreover, in case ground or subsea current return is prohibited, metallic neutral complies with the respective regulations.

Additionally, simulation results can be easily extended to the monopolar configuration with metallic return, as well as the bipolar and the monopolar with ground return, due to the system symmetry. Thus, in this section a positive line-to-ground fault is simulated in a four-terminal grid with bipolar station configuration and metallic neutral. The simulated network and the overview of the AC side of one HVDC station are presented in Figure 5.1.

5.2.1 System Parameters

The AC side voltage level was chosen to be 380 kV, which is the most representative high voltage level in Europe [79]. The selection of the VSC station and the DC grid voltage level was made based on a market survey. The lowest DC grid bipole voltage level that can accommodate station power up to 1200 MVA is ±320 kV, with rated current of 1881 A. The available station modules are presented in Table 5.1 [26], whereas the network parameters are summarized in Table 5.2. Based on the given system base values, the station components, as well as the DC link capacitors were calculated and cables were selected.

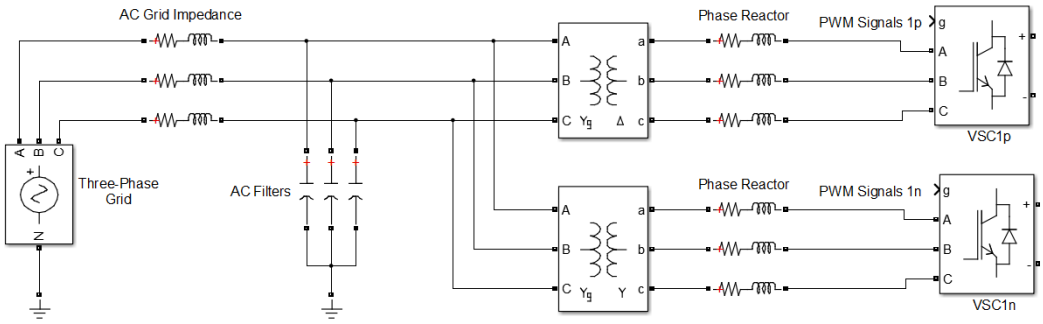
Table 5.1: ABB HVDC Light Module Ratings [26]

DC Voltage Level (kV)	±80			±150			±320			±640		
Base Power (MVA)	106	209	319	200	393	600	427	839	1281	667	1311	2001

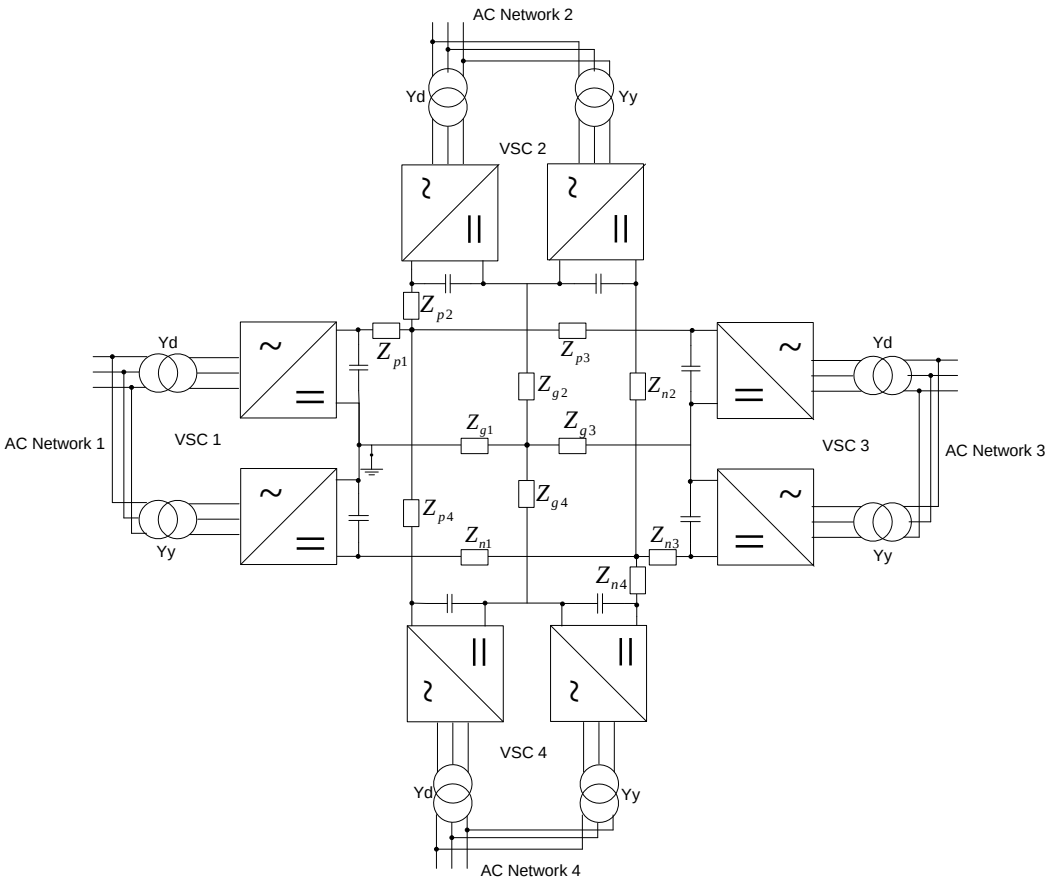
Table 5.2: Network Parameters

Models	Rated Power (GVA)	Impedance (pu)	Rated Voltage (kV)
AC Network 1	10	0.001+0.1j	380
AC Network 2	10	0.001+0.1j	380
AC Network 3	10	0.001+0.1j	380
AC Network 4	10	0.001+0.1j	380
VSC	1.2	-	AC Side: 150 DC Side: 320
Transformer	1.2	0.1+0.001j	Primary: 380 Secondary: 150

As mentioned in Chapter 2 (see section 2.2), a bypass resistor is used during start-up to avoid overcurrent in the AC and DC capacitors at the connected stations. During start-up the AC filter capacitors and the DC link are charged. To ensure that the VSC current



(a) Four-terminal HVDC bipolar network



(b) Bipolar station

Figure 5.1: Bipolar configuration with metallic return

does not exceed 1 pu, a series resistor is connected for 10 ms. The size of the resistor is equal to converter AC-side base impedance, namely 37.5 Ω for the present case study. Another option to limit the power through the station during the start-up phase is to charge the DC link first through the aforementioned resistor, via another line, completely bypassing the VSC station. As soon as the voltage level of the DC link has reached its rated value, the resistor is bypassed, the additional line is disconnected, and the converter station is connected in series with the rest of the system.

The AC filters are sized based on the converter station rated power. A typical filter size is 20% of the station rated power [26]. Therefore, in case of a bipolar configuration the station consists of two VSCs connected in parallel on the AC side, each of which is rated for half the station power. In this case, the station power rating is 1.2 GVA and each converter is rated for 0.6 GVA. The filter capacitor size is thus calculated as:

$$0.2 \cdot Q_{phase} = \omega C V_{f,phase-rms}^2 \Rightarrow C = \frac{0.2 \cdot Q_{phase}}{\omega V_{f,phase-rms}^2} \Rightarrow C = \frac{0.2 \cdot (1.2e9/3)}{314 \cdot (220e3)^2} = 5.26uF \quad (5.1)$$

In series to the AC filters, two transformers are connected in parallel to form the bipolar station. The transformer rating is selected based on the converter rating. In the present case study, two transformers 380 kV/150 kV were selected.

The two voltage levels are typical values for the high voltage grid, based on the ENTSOE Interconnected Network Grid Map [79]. The transformers are not only galvanically isolating the converter itself from the AC grid, but they also generate a phase shift. The bipolar converter bridges (6-pulse) are connected in series on the DC side, thus making a 12-pulse circuit. The 3-phase systems leading to the converters need to have a 30^o phase shift, to cancel out the 6-pulse harmonics. This is achieved by using one transformer in star-grounded delta configuration (Yg-d) and one transformer in star-grounded star connection (Yg-y).

The transformer impedance is particularly important for the VSC control, as it adds to the value of the phase reactor. A typical short-circuit voltage of a converter reactor is 15% [10]. The short-circuit voltage (U_k) of a reactor is given by the equation [80]:

$$U_k = \frac{100 \cdot \sqrt{3} \cdot I_{rms} \cdot X}{U_{3-phase,rms}}\% = 100 \cdot \frac{X}{Z_{base}}\% \quad (5.2)$$

where I_{rms} is the rated continuous current of the coil, $U_{3\text{-phase,rms}}$ is the rated voltage of the network, X is the reactance of the reactor and Z_{base} is the system base impedance.

Considering (5.2), the total reactance should be 0.15 pu. If the transformer is considered to have an equivalent impedance of 0.0005+0.05j pu, the phase reactor is selected to be 0.001+0.1j pu. The parasitic resistance is considered to be 1% of the phase reactance.

The PWM switching in the converters introduces a voltage ripple on the DC side voltage. Therefore, capacitors are required to reduce the ripple and provide a steady voltage to the HVDC grid. The bigger the capacitor size, the smaller the ripple will be, the smaller the current through it and thus the longer its lifetime. However, the capacitor size cannot be too high, as this results in higher cost, space demand and also increased network inertia. One of the main advantages of the VSC technology is the ability to fast control the power exchange between the terminals and the DC voltage level. A smaller capacitor makes fast

changes easier. Therefore, a trade-off has to be made between the voltage ripple, the control stiffness and the lifetime of the capacitor.

The time constant of the DC capacitor (τ) is the time it takes to fully charge the capacitor (C_{dc}) from zero to nominal voltage with the converter providing active power equal to the rated apparent power S_{VSC}. It is given by the following equation:

$$\tau = \frac{0.5 C_{dc} V_{dc}^2}{S_{VSC}} \tag{5.3}$$

where S_{VSC} is the nominal apparent power of the converter and V_{dc} is the nominal DC voltage level.

In order to satisfy both criteria, the time constant τ is typically chosen to be less than 10 ms [81], while a voltage ripple 5-10% is acceptable [82]. In the bipolar topology, each capacitor is chosen to have a time constant of 8.5 ms, thus C=100 μF, resulting in a peak-to-peak ripple percentage of 1%, as estimated from the simulations (see Figure 5.3(c)).

Regarding the DC network, suitable cables have to be selected. In the simulations 100 km lines were considered between the four terminals. The stations are connected in radial configuration and have a distance of 50 km from the middle point of the DC grid. The submarine cables are chosen, based on the bipole station rated power, the voltage level of the DC grid and the rated current [10; 8]. The DC grid parameters are given in Table 5.3.

Table 5.3: DC grid parameters

DC grid parameters	**Unit**	**Value**
VSC station rated power (S_{VSC})	MVA	1200
DC grid voltage level (V_{dc})	kV	$\pm$320
Rated current (I_{dc})	A	2062
Conductor area (A)	mm^2	2200
Resistance (R)	Ω/km	0.0195
Inductance (L)	mH/km	0.2
Capacitance (C)	nF/km	220

5.2.2 Control performance in normal operation

After selecting the system parameters, the system performance under normal operation has to be tested. In the simulations, VSC1 is used to control the DC voltage level while the remaining three stations are controlling their active power (Figure 5.1). In Table 5.4 the order of events implemented in the simulations is presented. The negative sign (-) denotes the station is feeding power to the DC grid and the positive sign (+) denotes that the station is absorbing power. The station power is equally distributed between its converters.

Figure 5.2 and Figure 5.3 show the simulation result for VSC1. The most important features which reflect the control performance of the VSCs are the DC voltage, the active power, the reactive power and the AC current through the converter. The simulation results for the remaining converters are given in the Appendix A.1.

Table 5.4: Order of events in bipolar converters for simulation of normal operation

Time (s)	0.5	0.8	1.2
VSC 2 Power (pu)	-0.30	+0.20	+0.40
VSC 3 Power (pu)	+0.30	-0.15	-0.30
VSC 4 Power (pu)	+0.40	-0.25	-0.05

Figure 5.2(a) shows the active power change for the positive pole converter VSC1p. It can be seen that there is a peak-to-peak ripple of 0.3 pu, which results from the switching behaviour of IGBTs in the simulation. However, the mean value follows the reference power steps within 1 ms. The measurement for the converter AC active power is taken on the secondary of the converter. As a result, the ripple is high in comparison to the grid side AC active power peak-to-peak ripple, which has been smoothed out by the AC filters and is measured to be 0.15 pu. The pu grid active power is shown in Figure 5.2(e). It has to be noted that the grid active power is higher than double the controlled active power of each pole converter to account for the losses in the station. The power measurements are taken with respect to the pole converter base power.

The reactive power mean value is controlled at zero at all times (Figure 5.2(c)). However the peak-to-peak ripple increases the higher the active power the VSC is handling. As the power the station needs to feed to the grid is increasing, the capacitors are also participating in this exchange. As a result the AC reactive power needs to compensate, thus depicting a heavy ripple (0.4 pu peak-to-peak), if measured on the secondary of the AC transformers. The effect of the AC filters reduces the peak-to-peak ripple to 0.2 pu on the AC grid side, as shown in Figure 5.2(f).

However, the reactive power is only controlled to zero on the phase reactors. As a result, the measured reactive power on the grid side is equal to the reactive power produced by the AC filters. The AC filter capacitors were sized to provide 0.2 pu reactive power compensation for the station VSC1. Therefore, the measured reactive power is equal to 0.4 pu of the VSC1p rated power (S_{VSC1p}=S_{VSC1}/2).

The current follows the active power steps. More specifically, the current q-component is controlled similarly to the active power(Figure 5.3(a)) and comparing to the reference signals, it can be concluded that the control is precise and fast.

The AC current does not exceed the VSC ratings at any point of the simulation. During start-up there is an instantaneous overcurrent resulting from the active power transferred to charge the DC link capacitors. This could be avoided, in case the DC link capacitors were pre-charged before the VSC was connected.

A solution to this can be to charge them in the same way as the AC filter capacitors, by connecting them in series with a resistor. As soon as the capacitors are fully charged, the VSC is connected and the series resistor is bypassed. In the present case study, the focus is not on the start-up procedure and therefore further details are not included.

The DC link voltage control can be seen in Figure 5.3(c). The voltage reaches 1 pu from zero in 200 ms (i.e. 10 AC network cycles). During start-up there is an overvoltage of 15%

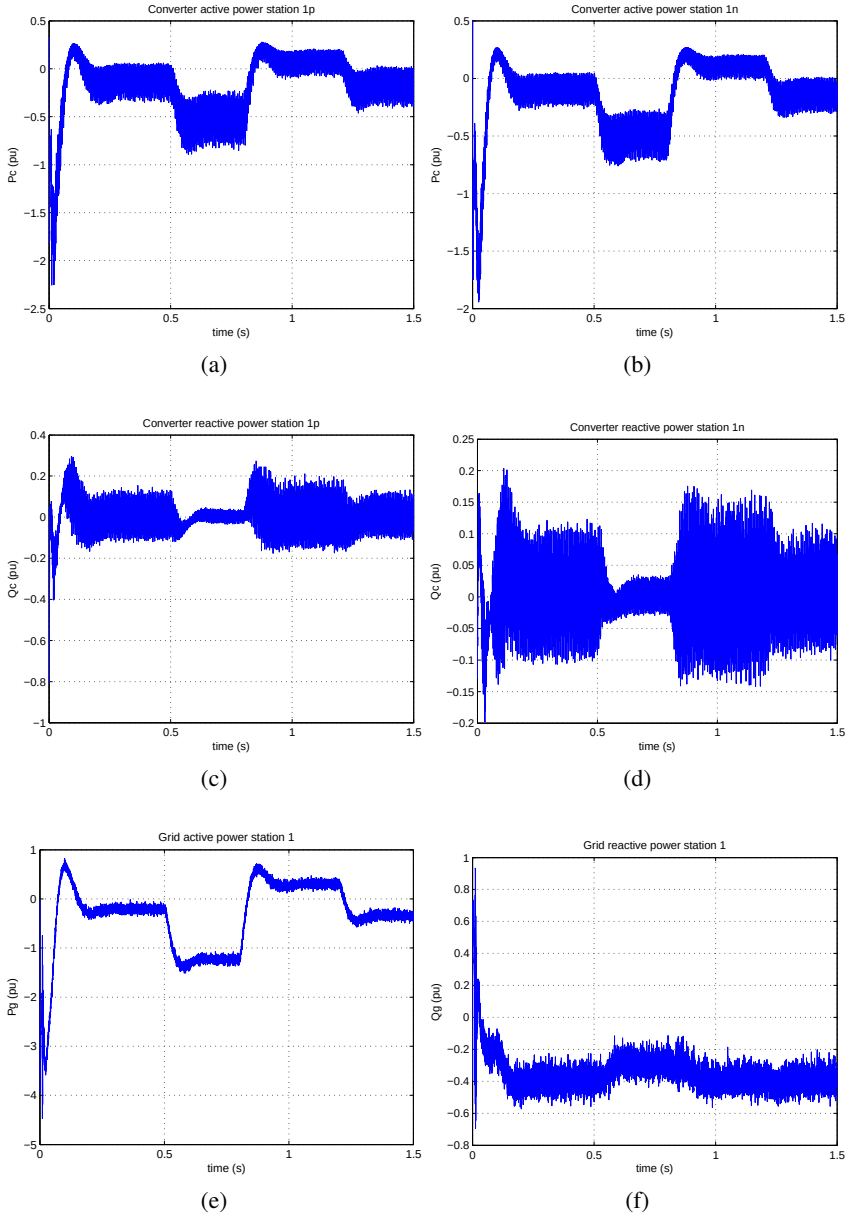


Figure 5.2: VSC1 Active and reactive power in normal operation

peak for less than 100 ms. When a negative active power step is imposed to the VSC in charge of DC voltage control, the voltage depicts a small dip, depending on the size of the step. In case a positive step occurs, there is a small overvoltage. Both transient situations are restored within 200 ms.

The same remarks apply for the other VSC stations as well, which are presented in the Appendix A.1. Ultimately, in terms of control, the bipolar configuration appears to operate

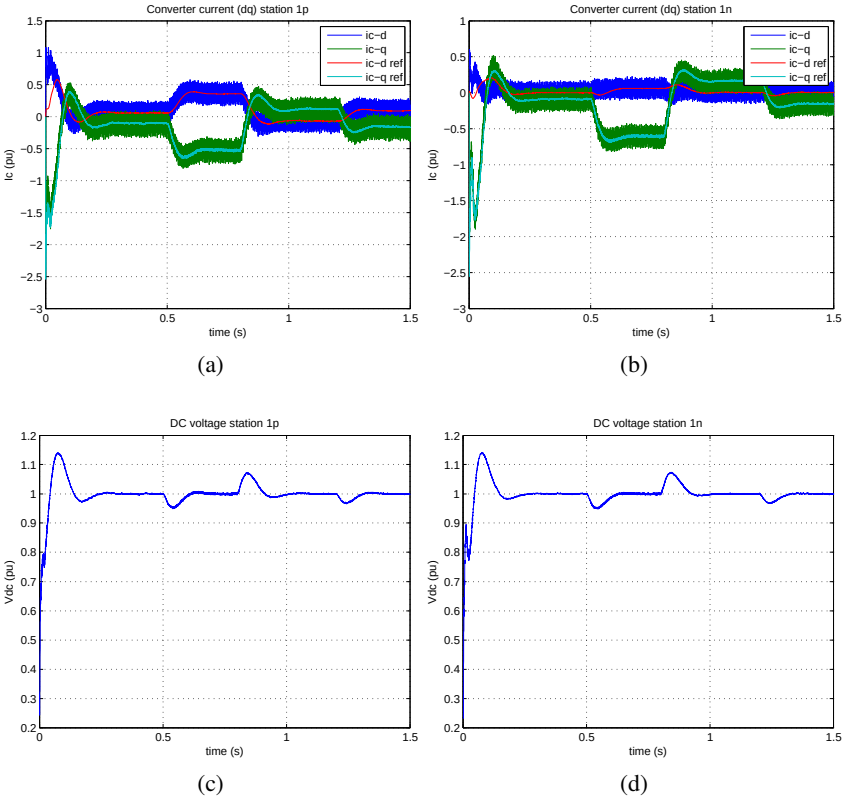


Figure 5.3: VSC1 AC current (dq) and DC voltage in normal operation

well under normal operation. However, its performance has to be further evaluated under contingency circumstances.

5.3 Fault detection methods

The inability of a VSC to break the current during DC faults is one of the major drawbacks in comparison to the classic CSC-HVDC.

As already discussed in Chapter 3, during a DC fault, the IGBTs need to be blocked for their protection. However, the antiparallel diodes of the IGBT modules continue to provide a path for the fault current through the converter station. Therefore, there is need for protection measures against DC contingencies. This section provides a description of the fault detection methods used during the simulations.

The main objective of a fault detection scheme is to reliably detect as fast as possible a DC fault case. In many cases, the same detection methods can also be tuned to deal with AC faults; however, this is out of the scope of this thesis. As soon as a fault is detected, signals have to be transmitted to the IGBTs drivers to block their operation for the sake of

their protection. The same signals are also given to the controllers of the DC breakers to open the circuit and isolate the faulty line.

In reality more than one detection methods has to be implemented in order to satisfy the redundancy requirement for an HVDC network. In case one mechanism fails there has to be an alternative protection scheme for the protection of the costly VSC stations and the security of the grid.

The fault detection methods can be divided into two main categories:

1. The converter protection (overcurrent)
2. The selective DC fault detection methods

5.3.1 Overcurrent Protection

This scheme is intended to protect the converter IGBT valves from overcurrent and its operation principle is straightforward. Based on the current ratings of the IGBTs, and the maximum capability rating of the VSC, a threshold is value is selected for the current. As soon as the AC-side current exceeds the threshold, a signal is generated that blocks the IGBTs.

The IGBT current is calculated as $I_{IGBT} = \sqrt{2}I_n$, where I_n is the rated AC current [83]. For the selection of an appropriate threshold, values were taken from the literature and the industrial catalogues. For example, Infineon provides IGBT modules for HVDC applications. Two of their IGBTs - rated for 4.5kV and 6.5kV - are presented in Table 5.5. The findings of the study are summarized in Table 5.6.

Based on Table 5.6 the lowest value was chosen as a threshold for the overcurrent protection, namely 1.8 pu. In this way, the protection is faster and accounts for an additional 20% overcurrent margin. As soon as this value is surpassed, the IGBTs are blocked.

Table 5.5: Infineon IGBT modules specifications

Component	**V_{CES} (V)**	**I_{Cnom} (A)**	**I_{CRM} (A)**	**Ipeak (p.u.)**
Infineon IGBT modules FZ1200R45KL3_B5	4500	1200	2400	2
Infineon IGBT modules FZ750R65KE3	6500	750	1500	2

(V_{CES}: Collector-Emitter Voltage, I_{Cnom}: Collector Nominal Current, I_{CRM}: Repetitive Peak Collector Current)

Table 5.6: Maximum overcurrent ratings of IGBTs

Literature	**Overcurrent capability (p.u.)**	**Time (ms)**
Protection of VSC-Multi-Terminal HVDC against DC Faults [36]	1.8	0
Short-Circuit and Ground Fault Analysis and Location in VSC-Based DC Network Cables [35]	2	0
Locating and Isolating DC Faults in Multi-Terminal DC Systems [78]	2	few ms
Market		
Infineon IGBT modules FZ1200R45KL3_B5	2	1
Infineon IGBT modules FZ750R65KE3	2	1

This IGBT protective method is based on local measurements at each station and is implemented in all the simulation cases enhancing the redundancy of the system.

5.3.2 Selective DC fault detection methods

These methods are based on the grid reaction in case a fault occurs. They are called selective, as their principle is to distinguish the faulty line from the rest of the network based on the line characteristics. More specifically, the described schemes were developed based on the simulation of the grid performance during a line-to-ground fault and are primarily determined to drive the DC breakers controllers. The two methods that will be further described are:

1. The current direction detection
2. The current derivative detection

Method 1: Current direction detection

This method, as its name states, is based on the fault current direction on the lines. In Figure 5.4, only the positive pole of the bipolar topology is depicted in case a fault occurs on the line connecting VSC2 to the middle node of the radial configuration. The direction of the currents from the converter stations is depicted with red arrows.

In case of a DC fault, control is lost at the stations. The IGBTs are blocked and all converters act like diode bridge rectifiers, feeding the fault. As seen in Figure 5.4, the line that experiences the fault has a different current direction at the point it is connected to the VSC station and at the central node of the grid. Thus, in case of a fault, the currents at the terminals of the faulty line have opposite directions. Taking this into account and assuming that at the central node of the connection a measurement station will exist, whenever different current directions are detected, a fault signal is generated blocking the IGBTs and triggering possible DC breakers.

In order to avoid any false signal resulting from oscillations in the grid, a current threshold of 2 pu is used. If both currents at the ends of the cable have a magnitude higher than 2 pu and at the same time they are moving in opposite directions, then a fault signal is generated.

Current measurements at both ends of each line are necessary for the realization of this scheme. As this method is not based on local station measurements and coordination between measuring devices is needed, fast communication lines are essential for its realization. Because of its dependence on communication lines, the main drawback of this mechanism is that it can fail in case of communication loss.

In order to estimate the detection delay, the propagation time of a signal has to be taken into account. Assuming copper wires, the signal propagation speed is $2.25 \cdot 10^8$m/s [84]. For a distance of 50 km between the central node and the VSC station for this case, the transmission delay is 0.22 ms without taking into account the data packet size in bits and the bit rate of the line (bit/s). In case of wireless connection, signals travel with the speed of light ($3 \cdot 10^8$ m/s) making the delay equal to approximately 0.17 ms. However, it has to

be considered, that the transmission bandwidth changes with the connection type used, thus changing the data transmission delay. The general equation for the data transmission delay is [85]:

$$t = \frac{P(bits)}{R(bps)} + \frac{l(m)}{v(m/s)}$$

where P is the data packet size in bits, R is the data transmission rate in bps, l is the distance the data have to travel in meters and v is the propagation speed (m/s).

Method 2: Current derivative detection

During a fault, DC link capacitors closer to the fault are the station components that first get discharged contributing the most to the fault current, as will be later shown in the simulation results. Because of the large change in the current of the faulty line, the current derivative is higher for the faulty line than for the rest of the network. When a current derivative limit is trespassed, a fault signal is generated. The drawback of this method is the need of a high sampling rate of the DC line current.

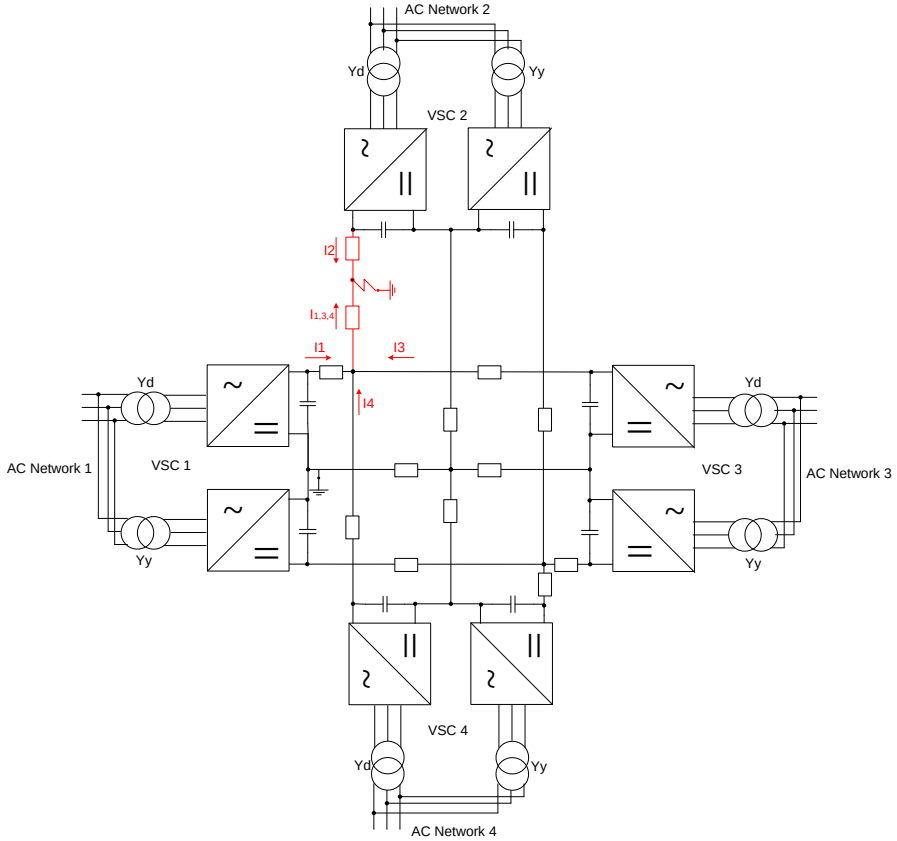


Figure 5.4: Positive line-to-ground fault in a radial network (red: the fault currents)

However, it was observed that this current derivative threshold value can also be exceeded in the time period that follows the opening of the faulty line DC breakers. The current is oscillating until a new steady-state is reached, resulting often in high values of current derivative. Therefore, another requirement has to be included as part of this method to tackle the secondary oscillations.

It was observed that during a fault, the current derivative has a steeper slope than any of the secondary oscillation. Therefore, the second requirement can be expressed as follows:

- If the current derivative at one station exceeds a first threshold value, then a fault case is identified in the system, but no action is yet taken. This first threshold is exceeded at all the positive pole converters, while at the same time, a timer is triggered.
- A second threshold is selected, as previously mentioned, based on the peak current derivative observed at each station. The highest peak normally corresponds to the faulty-line VSC. If this second threshold is exceeded within a certain time from the triggering of the timer, the fault is identified. In any other case, it is a secondary oscillation and there is no need to break the line, unless the protection measures are triggered.

For the implementation of this selective method, the line currents and their derivatives during a fault are simulated beforehand. Based on the simulation results, the first and second current derivative threshold values are determined, as well as the time within which the second threshold is exceeded by the faulty line current derivative. The current derivative thresholds have to be evaluated based on the system parameters and are different for different topologies. The threshold values depend greatly on the cables and the DC link capacitor size. This detection method is prone to noise sources and thus a certain safety limit has to be considered during the control design. The main advantage of this method is its detection speed.

The method strategy is better depicted in Figure 5.5.

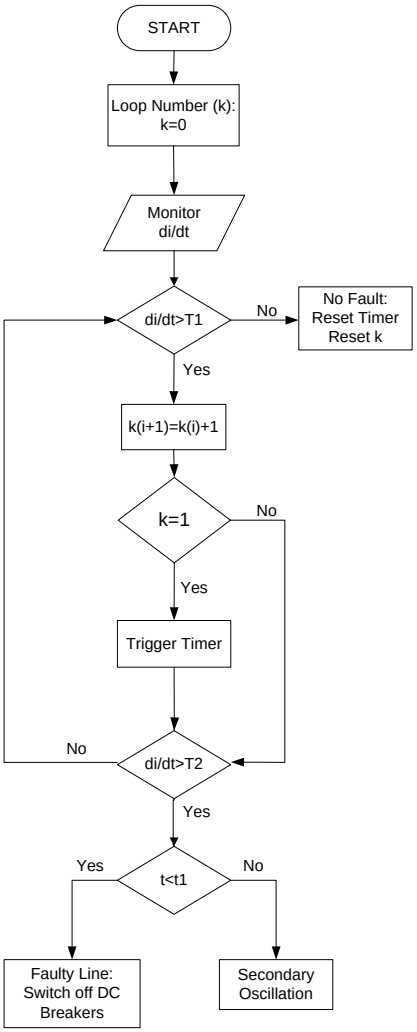


Figure 5.5: Flowchart of current derivative fault detection method

5.4 Pole-to-ground fault without protection

Before applying further protection schemes to the HVDC grid, it is important to understand the way it behaves naturally during a fault. For this purpose no selective detection schemes are implemented. Overcurrent protection of the converters is used in order to block the IGBTs, as would happen in case of a DC fault. The purpose of the simulations is to determine the contributions of the different DC grid components to the fault current and examine the effect of the distance between the fault point and the VSC station connected to the faulty line.

A positive line-to-ground fault is applied on the line connecting VSC2 to the grid central node. For the simulations in this section the same model as in the normal operation is used. Additionally the valve protections are implemented. The fault resistance used is 7 Ω, which

Table 5.7: Order of events in bipolar converters for simulation of line-to-ground fault

Time (s)	P_{VSC2}(pu)	P_{VSC3}(pu)	P_{VSC4}(pu)
0.5	-0.3	0.3	0.4
0.7	Fault	0.3	0.4

corresponds to the resistance of wet loamy sand at peak current [30]. Three different fault point cases are considered: the distances between the fault point and VSC2 simulated are:

1. Case 1: 1 km;
2. Case 2: 25 km;
3. Case 3: 49 km.

The case studies can be seen in the single line diagram of Figure 5.6. In all the simulations the currents at the lines, the capacitors, the converters and the fault point are monitored. The simulations are run for 1 s and the order of events is presented in Table 5.7. Moreover, it is assumed that the power references of the VSC stations do not change before and after the fault.

For each of the cases the AC side and DC side parameters of every VSC need to be studied. As soon as a fault happens, the DC link voltage starts decreasing, while the DC current from each station reaches a peak. In Figure 5.7 the voltage of the DC link at each station is depicted for case 1.

After the fault occurrence, the voltage of the VSC closer to the ground of the DC grid decreases, in less than 3 ms, to 0.5 pu. The other stations, which are in greater distance from the ground point, fall to 0.5 pu in 5 ms.

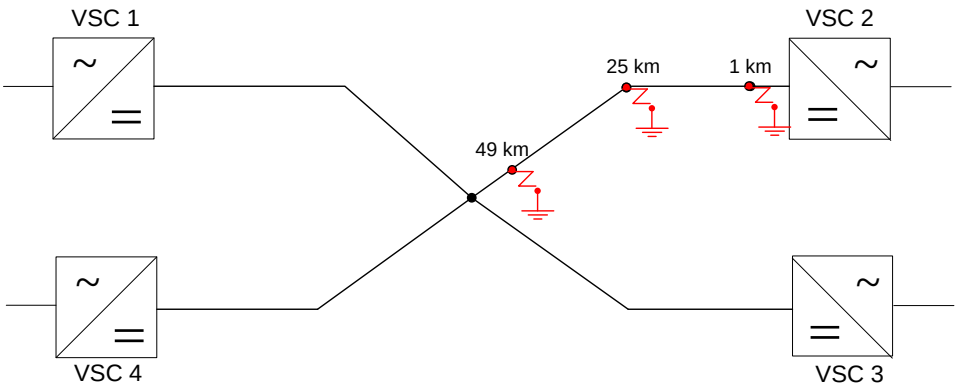
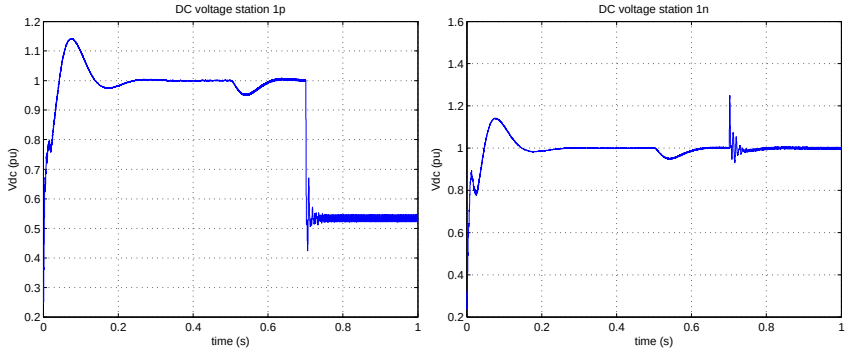


Figure 5.6: Positive line-to-ground fault cases based on distance from VSC2 Case 1: 1km, Case 2: 25km, Case 3: 49km



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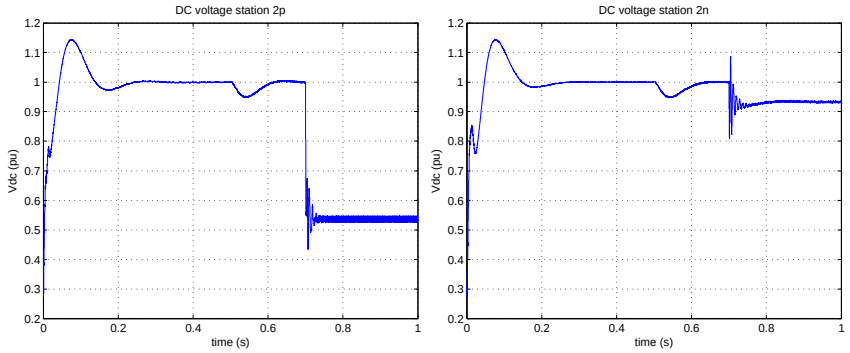

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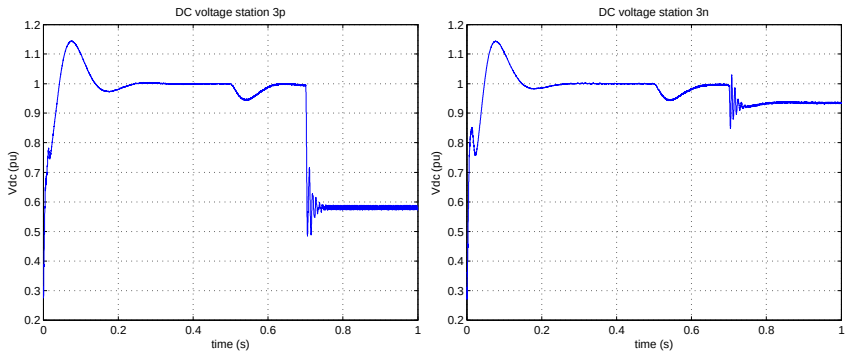

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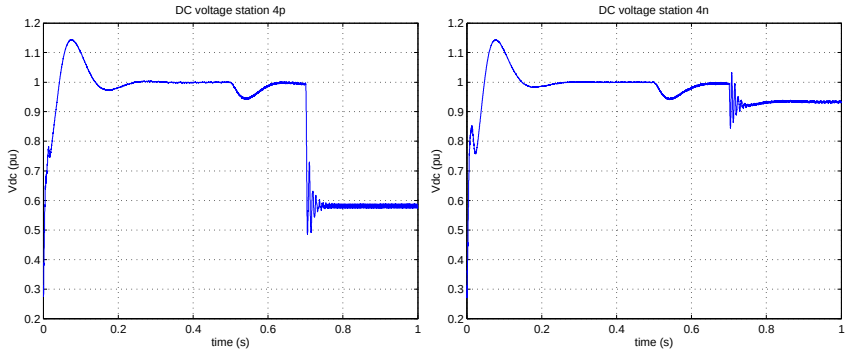


(g)

(h)

Figure 5.7: DC Voltage fault case1

At this point it has to be stressed that the new steady state level of the DC link voltage level depends greatly on the fault resistance. Based on the literature, this was chosen to be 7 Ω, which corresponds to the resistance of wet loamy sand soil type [30]. In case other types of soil are present this can change significantly, however, its value cannot be neglected for the case of a line-to-ground fault.

In Figure 5.7 it can be seen that the new steady state value differs for the different stations, as VSC2 is closer to the fault point, while VSC1 is closer to the ground point of the network. As a result these two stations have a new voltage value, determined by the fault resistance. If the steady state fault current (Figure 5.11(a)) is taken into account, it can be verified that the voltage is:

$$V_f = R_f \cdot I_f = 7\Omega \cdot (12pu \cdot 1875A) = 157.5kV = 0.492pu \tag{5.5}$$

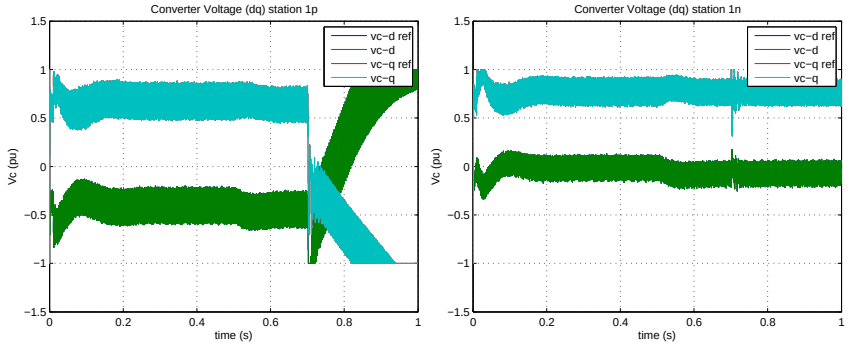
As the DC currents increase, the DC voltage drop in the lines increases as well, since all the positive pole converters are feeding the fault and fault currents are circulating in the DC grid, from the VSCs through the fault resistance. As the fault point voltage level is fixed due to the fault resistance in the new HVDC network steady-state, the voltage level at the VSCs is higher the bigger the total impedance until the fault. As a result, there is a bigger voltage drop in the lines connecting VSC3 and VSC4 with the fault point than in the lines connecting VSC1 and VSC2, which are closer to the fault.

Because of the neutral metallic connection between the stations, there is fault current circulating in the neutral. This current (Ineutral) has a direction from the grounding point of the neutral of VSC1 to the grid central node, where it is split into converter components (Ineutral2, Ineutral3, Ineutral4). The neutral currents can be seen in Figure 5.9. The rest of the fault current goes to VSC1 (Ineutral1). This high current is responsible for the losses in the neutral line and accounts for the voltage drop at the DC link of the negative pole VSCs (see Figure 5.7). As VSC1 is controlling the DC grid voltage, its value is fixed. For the rest of the converters there is a drop ΔV=0.05 pu (5%).

In Figure 5.8(c) the AC current of VSC1p is depicted for the fault case 1. The AC current of the other stations can be found in Appendix A.2. There is a big difference between the current contribution of VSC1 and VSC2 in comparison to the other two converters. From the study of the figures it becomes apparent that the role of the DC grounding determines to a great extent the response of the individual converters.

The negative pole converters do not experience big transients during the fault. Only VSC1n experiences an overcurrent due to the high value of the fault current circulating through the common grounding it shares with the respective VSC1 positive pole converter. However, this is not enough to trigger any fault signal at the converter and block the IGBTs.

At the moment of the fault, the control of the IGBTs is lost. The voltage at the AC side (Figure 5.8(a)) of the converter increases to reach the value of the DC link voltage and the current no longer follows the reference values. The current reference is not controlled and it shows how much the current would need to be in case the IGBTs were still working, to achieve the wanted power level. The change in the direction of the current of VSC3 and VSC4, depicted in Appendix A.2. is due to the fault. Before the fault, they were both controlled to absorb power from the DC grid, whereas as soon as a fault occurs, the currents change direction to feed the fault.



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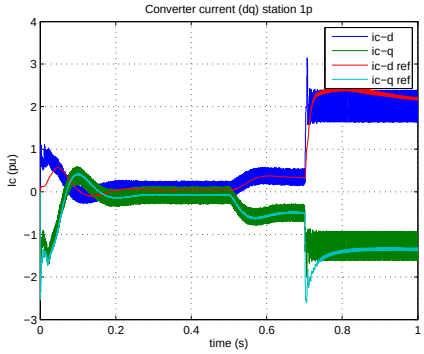

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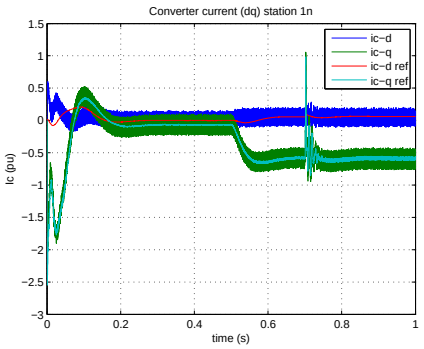

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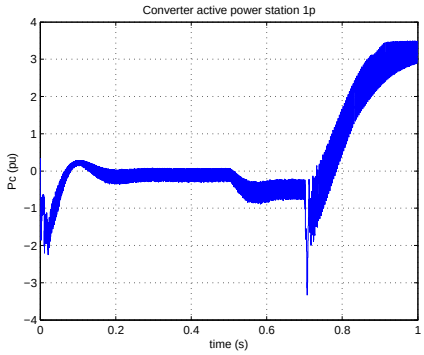

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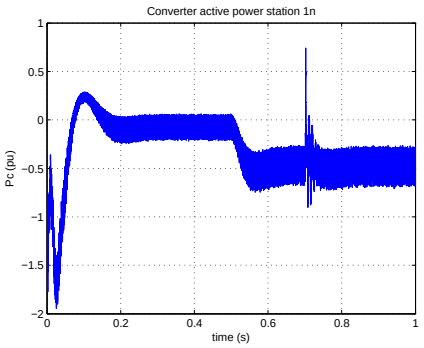

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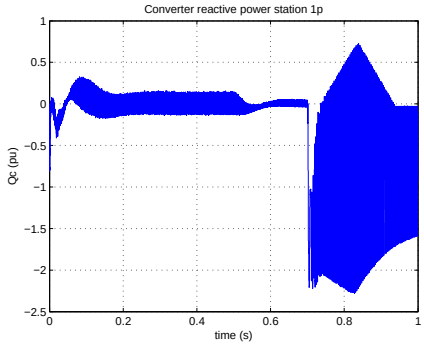

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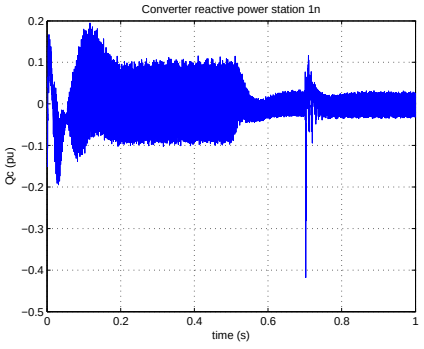


(h)

Figure 5.8: VSC1 AC characteristics fault case 1

As shown in Figure 5.4, all currents change direction, feeding the fault. Because of this change in the current and voltage signals, the active power changes as well and its value is given by:

$$p_{ac} = \frac{3}{2}(v_d i_d + v_q i_q) \tag{5.6}$$

As expected, no change in the active power exchanged with the grid occurs for the VSCs controlling the negative pole line. A big change occurs for the reactive power exchanged with the grid. Due to the blocking action of the IGBTs the reactive power is no longer zero on the AC side, but experiences a big oscillation mainly due to the direct connection of the AC side on the capacitor at the output of the diode bridge. This influences the power factor of the system and therefore the fault needs to be isolated as soon as possible. For the negative pole VSCs, the reactive power continues to be controlled at zero, as is the normal operation case. The peak-to-peak ripple is high due to the fact that the measurements are made on the secondary of the AC transformer. The grid power is smoothed out by the AC filters and is shown for the three fault cases in Appendix A.2.

The remarks made for case 1 can be extended to all three fault cases, as no big differences are observed. The simulated DC voltage, AC voltage, AC current, active and reactive power for each of the converters are presented for Case 2 and 3 in the Appendix A.2 (from Figure A.13 to Figure A.23). It is important to mention that depending on the fault point, the

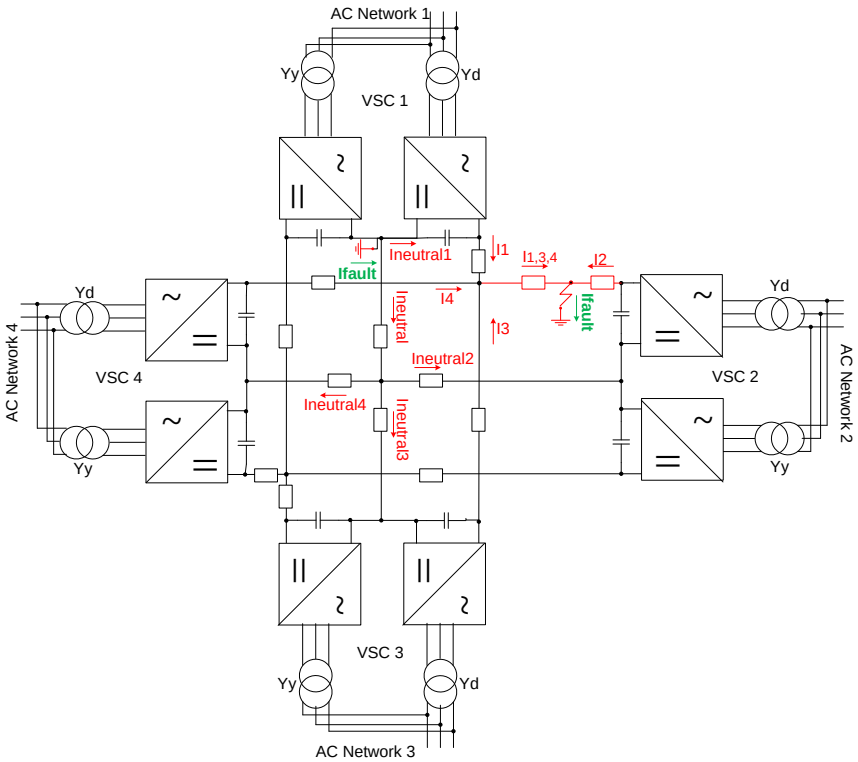


Figure 5.9: Fault and neutral currents circulating on the positive pole VSCs

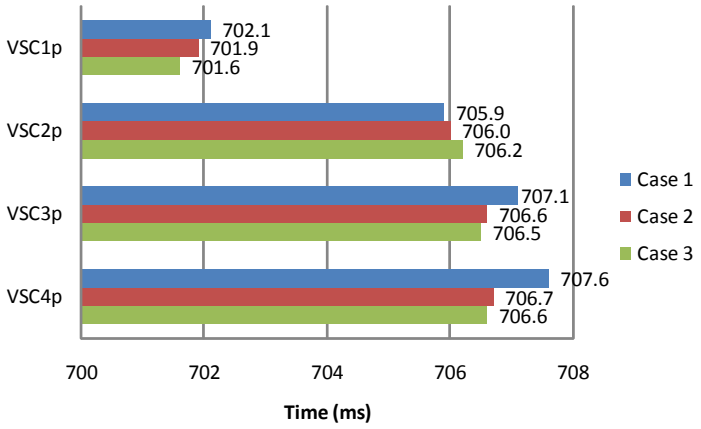


Figure 5.10: Fault signals positive pole VSCs for the three different fault cases

distance from each converter changes and thus the DC link voltage level slightly changes, accounting for the voltage drop on the DC lines.

Figure 5.10 compares the fault signals, generated from the overcurrent protection controllers, for all the VSCs for the different cases. In every case the first VSC that experiences a high overcurrent, thus blocking its IGBTs first, corresponds to the station to which the grounding of the HVDC network is directly connected, i.e. VSC1. From the simulations emerged that the negative poles do not experience any overcurrent that would generate a fault signal.

5.4.1 Fault current contributions

In this section the contributions of the different network components to the fault current are presented and compared based on the line-to-ground fault scenarios presented in Figure 5.6.

Figure 5.11 shows that in case no clearance action is taken, fault currents develop in two phases. There is a transient period and a steady-state period, as discussed in Chapter 3, section 3.3. The transient period lasts for circa 15 to 20 ms. The initial peak of the fault current is marked with an ellipse and is shown in more detail in Figure 5.12 for each of the studied cases.

For case 1, initially the DC link capacitor closer to the fault is discharged, reaching a peak current of 8 pu before dropping to zero. It is important to mention that the contribution from the discharge of the DC line, which experiences the fault is also significant and reaches a peak of 4 pu. After the discharge of the network energy storage elements of the network (i.e. cable inductance and capacitance, DC link capacitors), the fault is mostly fed from the converter stations depending, as mentioned in the previous section, on the total impedance until the fault. Therefore, station 1 and station 2 contribute the most during the steady-state period.

In case 2, the transient phase contributions change. As the distance between the fault

and the VSC2 DC link capacitor increases, the capacitor peak is delayed and only occurs after 0.4 ms. The initial peak of the fault current is therefore coming from the discharge of the faulty line. The steady-state response remains the same and the contributions follow the same principle as described for case 1.

Finally, in case 3, as the fault point is closer to the middle node of the network, the fault current is initially fed only from the contributions of the discharging DC lines. The steady-state response of the system remains the same. The percentages of the contributions of the different components is given in Appendix A.2.

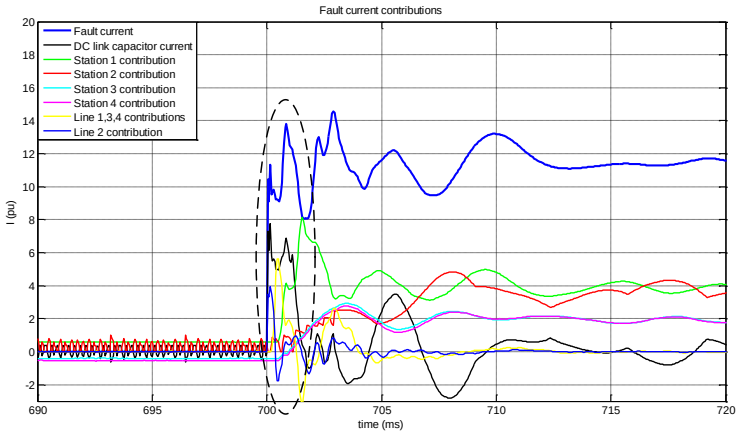
5.4.2 Preliminary Conclusions

From the previous analysis it can be concluded that the most important issue regarding the response of a network during a DC fault is the grounding of the DC side. This influences significantly the DC link voltage level for each converter and the contributions of the VSC currents to the DC fault during the steady-state. From the comparison of the case studies, the closer the fault point to the middle point, the more difficult it is for the system to detect and isolate only the faulty line.

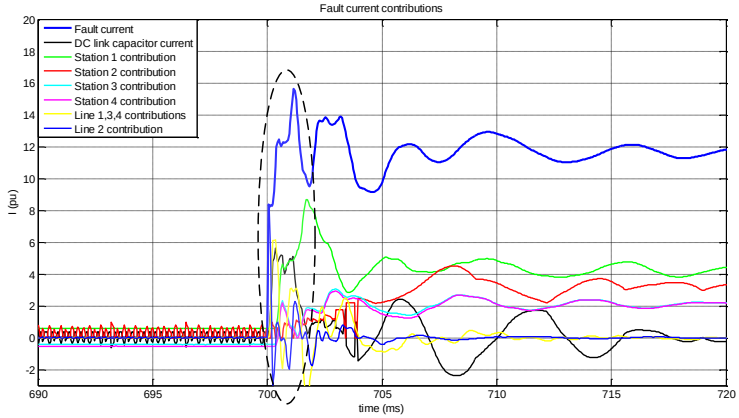
The goal of the safety measures that will be investigated is to act as fast as possible to protect the VSC connected to the faulty line and isolate this from the rest of the system before the fault current influences the other stations. In case 3, the fault is detected from VSC1, VSC3 and VSC4 sooner than in the other two cases, while at the same time the peak fault current reaches a value of 18 pu during the transient period. As a result, this case is considered to be the worst case scenario and will be further investigated.

Moreover, depending on the ground of the system, the time each VSC needs to detect the fault differs and this needs to be considered in the design of fault detection selective methods. The transient characteristics of a VSC at the moment a fault occurs are used to determine threshold values, based on which the faulty line is detected and can, therefore, be isolated with use of DC breakers, thus ensuring the safe operation of the rest of the network.

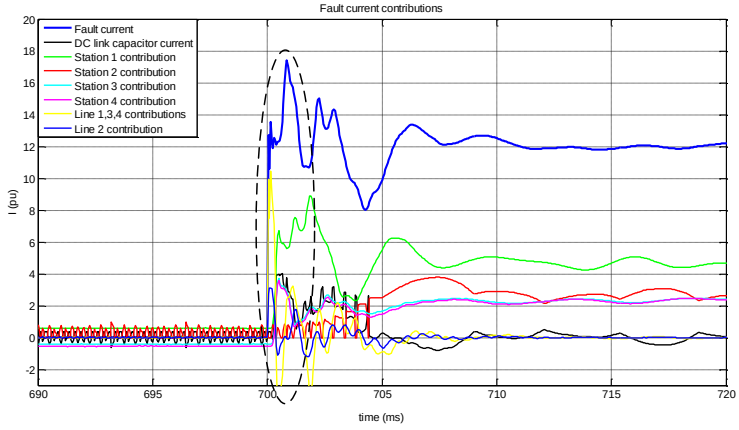
Finally, it was seen from Figure 5.10 that as soon as a fault occurs there is limited time left for the system to detect the fault and isolate the line, namely 1ms. In order to limit the peak current, delay its occurrence and allow for a bigger period for the system detection and isolation measures to act, before all the VSCs are influenced, limiting reactors are used.



(a) Case 1

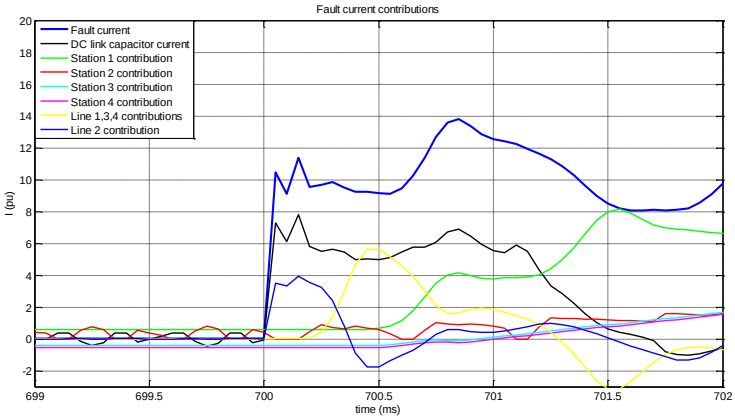


(b) Case 2

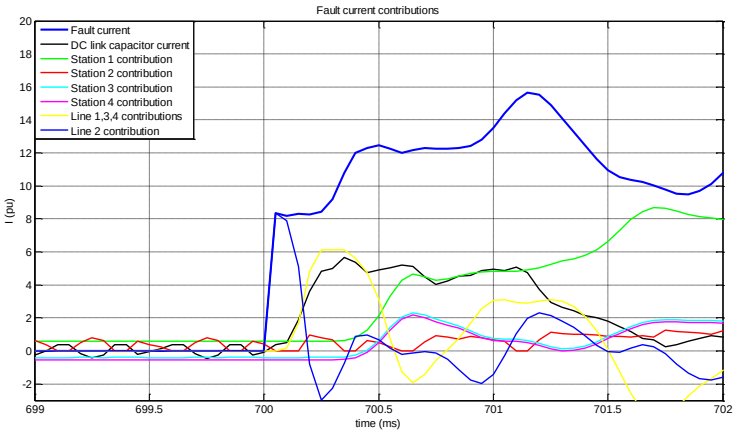


(c) Case 3

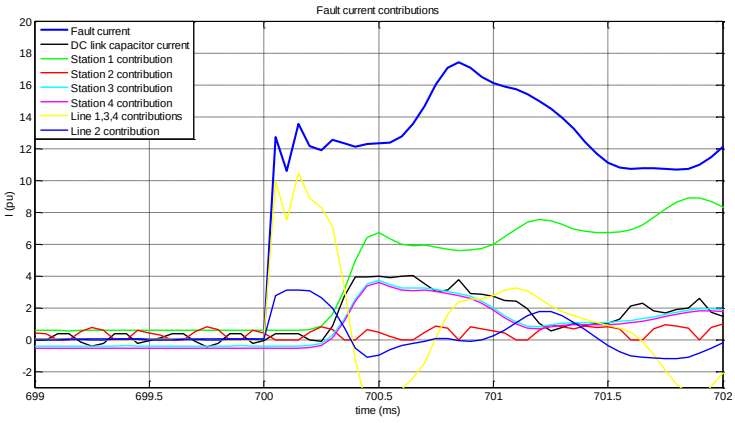
Figure 5.11: Fault current contributions in the different case studies



(a) Zoom-in Case 1



(b) Zoom-in Case 2



(c) Zoom-in Case 3

Figure 5.12: Fault current contributions in the first 2 ms from fault occurrence

5.5 Pole-to-ground fault with limiting reactors

In order to evaluate the influence of limiting reactors in the system a sensitivity analysis is carried out. Five limiting reactor values are chosen in the range from 1 mH to 200 mH and their respective influence in the system is compared. These limiting reactors are connected between the DC link and the DC line on both the positive and the negative pole, as shown in Figure 5.13.

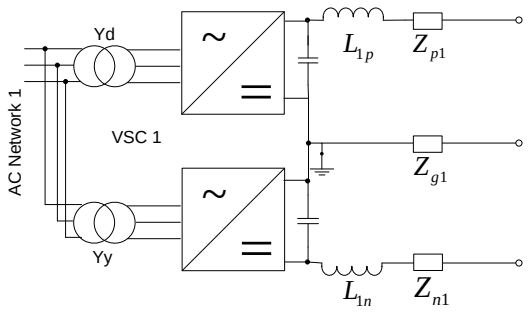


Figure 5.13: Limiting reactors on the DC network

The influence of the limiting reactors size in the total fault current is shown in Figure 5.14. When an inductor of 1 mH is used, the total fault current measured at the fault point accounts for 17.2 pu, dropping to 13.5 pu with use of 200 mH inductance.

In Figure 5.15 the correlation between the peak fault current at the station at the point of connection with the HVDC network with the inductor size is presented. The inductor size appears to influence the peak current at station 1 the most, bringing it down from 8.58 pu to 4.63 pu with use of 200 mH inductor. Station 2 also experiences a higher fault current with a peak at 4.45 pu with 1 mH inductor and, as the inductor increases, it falls to 3.1 pu.

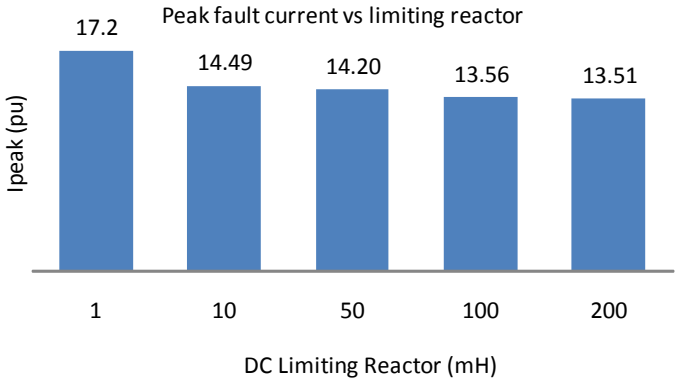


Figure 5.14: Peak fault current for different limiting reactor sizes for bipolar topology with metallic return

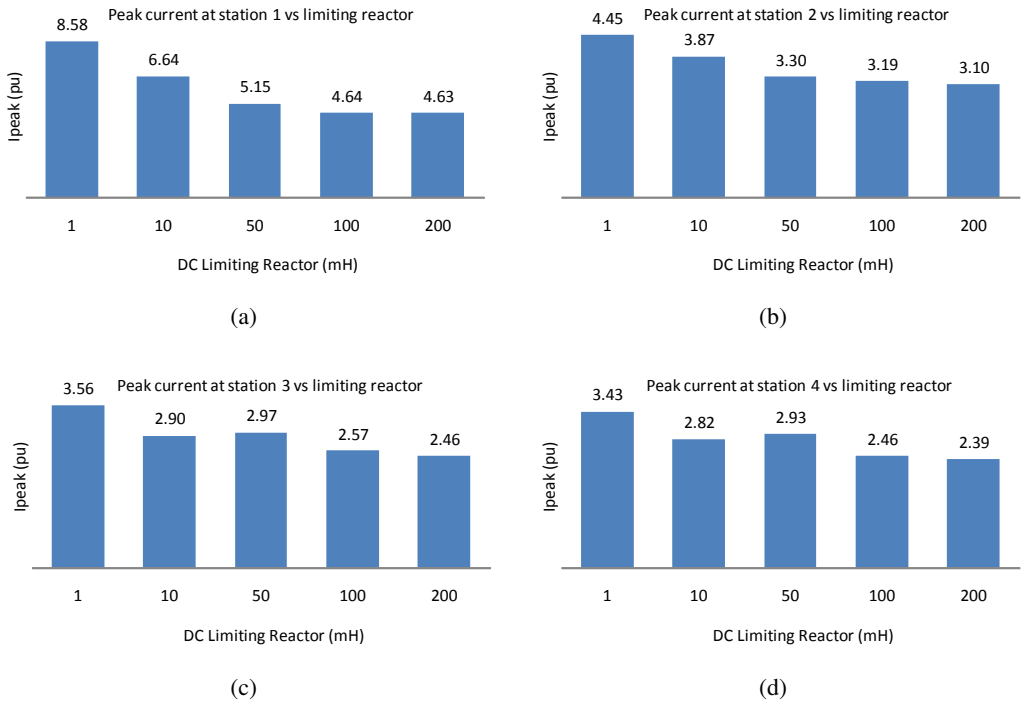


Figure 5.15: Peak current at positive line for different limiting reactor sizes for bipolar topology with metallic return (measurement after limiting reactor)

Stations 3 and 4 have almost the same behaviour. From the graphs, it can be seen that as the inductor size further increases the difference in peak current value is becoming lower, showing a strong diminishing return trend between 100 mH and 200 mH.

It has to be noted that as the inductor size increases, it not only decreases the rate of increase of the current, but it also increases the resistance of the network during the transient phase, thus limiting the peak value of the current on each line. However, the influence of the inductor size on the AC side current, which also needs to be investigated, is presented in Figure 5.16. From Figure 5.16, no pattern seems to be followed based on the limiting reactor size. The values differ by 0.2 pu for all the station, while VSC1 has a bigger value difference between the two extreme cases, namely 0.5 pu. The impact of the inductor size is not as strong as on the DC side and therefore no safe conclusion can be drawn.

More important than the effect of the limiting reactor size on the AC current is the way it influences the peak current occurrence and more specifically the time it takes for the over-current protection to be triggered. As it can be seen from Figure 5.17, the higher the value of the inductor the slower is the fault detection for each of the affected VSCs. For VSC1, making use of different inductor sizes, the time it takes for the AC current to surpass the 2 pu threshold of the IGBTs increases by almost 4 ms. A time difference of 2 to 3 ms was estimated for the remaining VSCs. This increase might seem small, but in case of protection measures every millisecond matters.

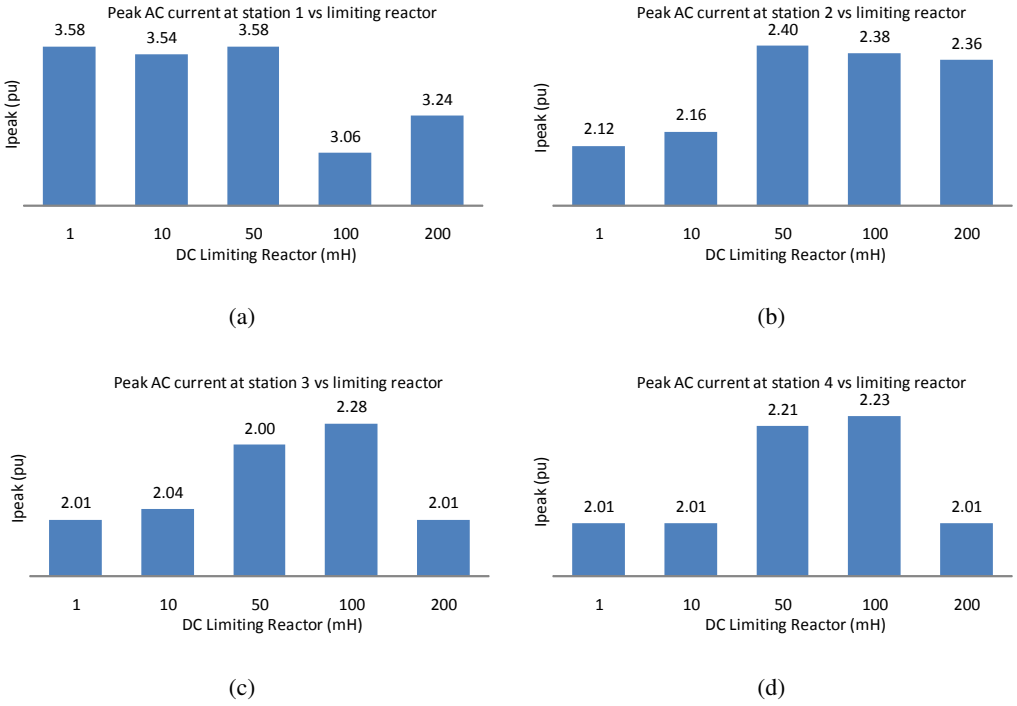


Figure 5.16: Peak AC current for different limiting reactor sizes for bipolar topology with metallic return

The time at which the fault detection signal is generated for the different reactor sizes is given in Table 5.8. The values in Table 5.8 need to be taken into account when testing different DC breaker models. In order for the network to be able to operate without interruption, even in case of a DC fault, the selective detection methods need to detect and, in cooperation with the DC breakers, to isolate only the faulty line within the times provided in Table 5.8.

Hence, big inductors can be used to lower the rate of rise of the fault current and, therefore, shift its occurrence for some milliseconds and also limit the peak DC current at each station. On the other hand, from the simulations, it was seen that the use of high inductance values needs to be balanced by the VSCs controllers, as higher values increase the stiffness of the network and thus do not allow fast current changes, which are important for power flow control.

Therefore, when deciding the inductor size, there is a trade-off between the rise rate of the fault current - which accommodates better handling of fault cases - and the normal operation time response of the system, which needs to be as fast as possible to fulfil the needs of a multi-terminal network.

For the aforementioned reasons, only 50-mH, 100-mH and 200-mH inductors, will be further compared for the fault cases with use of DC breakers, to investigate their effect on the selective protection measures and the coordination of the grid.

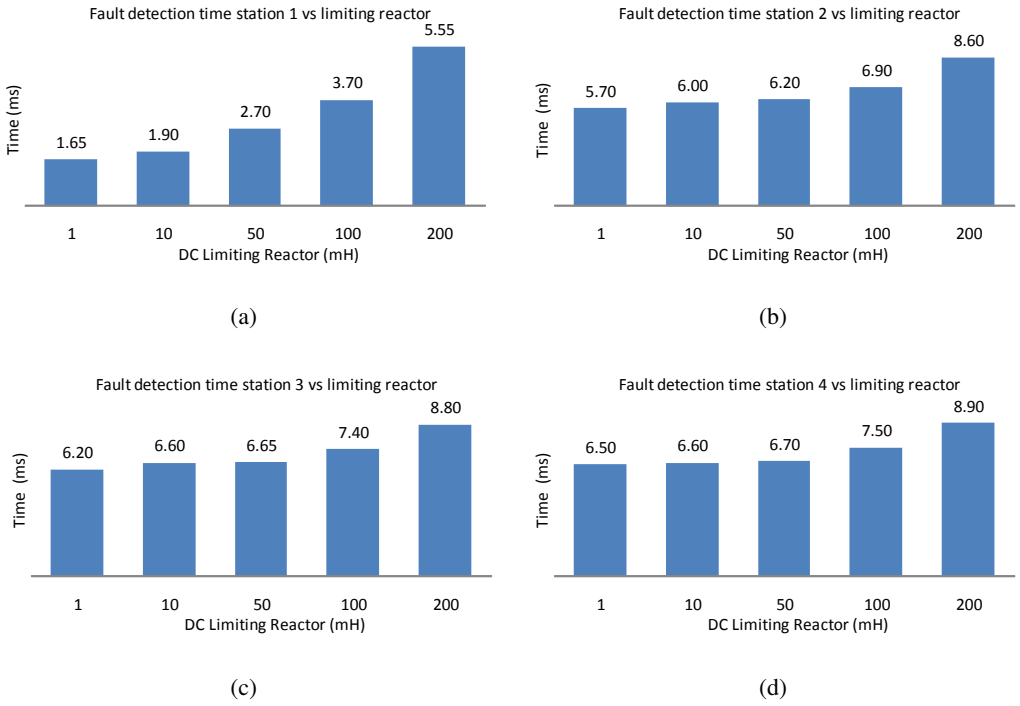


Figure 5.17: Fault signals for each positive pole VSC with use of different limiting reactor sizes for bipolar topology with metallic return

Table 5.8: Fault signal detection times from the moment of fault occurrence for different reactor sizes for bipolar topology with metallic return

	Time (ms)			
Reactor size (mH)	**VSC 1p**	**VSC 2p**	**VSC 3p**	**VSC 4p**
1	1.65	5.70	6.20	6.50
10	1.90	6.00	6.60	6.60
50	2.70	6.20	6.65	6.70
100	3.70	6.90	7.40	7.50
200	5.55	8.60	8.80	8.90

5.6 Pole-to-ground fault with DC breakers

In this section DC breakers are simulated in the bipolar configuration. They are modelled as ideal switches with a time delay based on the theoretical analysis made in Chapter 3 for four DC breaker models. The simulation model used for the study of DC breakers is shown in Figure 5.18. The total interruption times used for the DC breakers simulations are summarized in Table 5.9.

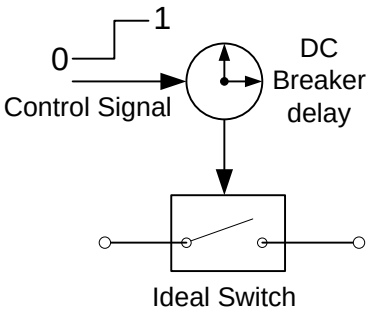


Figure 5.18: DC breaker model

Table 5.9: DC breakers total interruption time

	DC breaker technologies			
	Solid State Breakers	Hybrid I	Hybrid II	Resonance
Maximum total interruption time (ms)	1	2	30	60

DC breakers are added at both ends of each line, in order to accommodate a possible isolation of the faulty line. To avoid overvoltage on the DC link after the VSC is isolated, at the moment the respective DC breakers open, the VSC is blocked, in case it hasn't already been blocked.

At this point, it can be noted that a system response during a fault depends greatly on the pre-fault condition of each VSC. More specifically, the time a VSC needs to understand a change in the system and respond depends primarily on the travel time of the line. If a fault occurs, the DC link voltage drops and the station reacts by increasing the current it feeds to the DC grid. As a result, the time between the fault occurrence and the point at which an overcurrent is detected at the IGBTs of the converter leading to its blocking, depends on the travel delay of the line, as well as on the control speed and the current slope permissible through the IGBTs. The higher the power the VSC is handling at the point the fault occurs, the higher its current and thus the less time it has before an overcurrent state is reached. More specifically, the total fault detection time is:

$$t_{detection} = \tau_{line} + t_{control} + t_{(I_0 \rightarrow 2pu)} \tag{5.7}$$

where τ_{line} is the line transport delay from the fault point, $t_{control}$ is the controller delay and $t_{(I_0 \rightarrow 2pu)}$ is the time the converter current needs to surpass the overcurrent threshold of 2 pu. The latter variable depends on the IGBTs permissible current slope.

In the performed simulations, it was assumed that the power references of the VSC stations, at the post-fault stage, maintain their value as it was before the fault occurrence. Consequently, in case a converter is isolated after the fault, the others need to compensate for the power it was either absorbing or feeding from and to the grid at the pre-fault stage. If the power balance is not correct, thus the sum of the active power levels is not right, there

is the danger that the VSC responsible for voltage control experiences an overcurrent after the fault has been cleared, due to its tentative to meet the power requirements set by the grid power balance.

As a result this is taken into account when deciding the power references for the case studies used for the fault simulations for all the topologies. The order of events for the case studies is presented in Table 5.7.

Before proceeding to the fault simulations, a selective fault detection method, on which the controller of the breaker is based, needs to be selected. In order to compare the two selective fault detection methods (current direction and current derivative method) and choose the best option for the topology, they are both simulated along with a full semiconductor breaker with total interruption time 1 ms and an inductor size of 50 mH. The fault detection method is selected based on two criteria:

1. The detection selectivity;

2. The detection speed (from fault occurrence).

The detection selectivity determines the capability of the method to distinguish the faulty line from the others and therefore disconnect it successfully from the rest of the network. On the other hand, the speed accounts for the time it takes for the method to generate a trigger signal for the breakers to open. These parameters will determine which fault detection method will be used for every grid topology that will be simulated.

Moreover, a successful isolation of a line occurs when two criteria are fulfilled, namely:

1. All the converters are not damaged;

2. All the converters that are not attached to the faulty line continue to work normally after the faulty line isolation.

5.6.1 Current derivative fault detection

As expected, when a fault occurs the negative pole converters do not experience any overcurrent or huge voltage sag that would generate a fault signal, and therefore they continue working properly.

However, VSC1n, whose neutral is directly grounded, appears to be affected more than the rest of the negative pole converters, mainly due to the high initial neutral current returning from the fault point, creating a bigger voltage oscillation at the negative pole DC link capacitor. The negative pole converters AC characteristics and DC voltage are shown in Appendix A.3.

Considering the positive poles, it is difficult to establish a threshold value for the current derivative, in order to distinguish which is the faulty line, mainly due to the position of the DC-side grounding. Because of the presence of only one grounding in the DC network, the station at which the neutral is directly grounded experiences a high current derivative along with the VSC connected to the faulty line.

Table 5.10: Current derivative peak values for each VSC

Station	**di/dt peak (kA/ms)**
VSC 1p	6.14
VSC 2p	6.12
VSC 3p	5.8
VSC 4p	5.8

More specifically in order to determine a current derivative threshold value, simulations were run without the use of DC breakers. The maximum values of each station's current derivative at the moment of the fault are summarized in Table 5.10.

Apparently, VSC3 and VSC4 are the ones with the lowest current derivative peak values and thus can be distinguished from the rest of the positive pole converters. However, their current derivative is only 5.8% lower than the respective peak value of VSC1, making it difficult to distinguish the stations in reality. Moreover, there is no definite threshold to distinguish VSC2 from VSC1. As a result, for the bipolar topology with metallic return the current derivative fault detection method cannot operate properly and does not fulfil its selectivity requirement. The time it takes for each station to detect a higher current derivative than the threshold value is given in Table 5.11.

Table 5.11: Time from fault at which current derivative threshold is surpassed

Station	**Time(ms)**
VSC 1p	0.5
VSC 2p	0.4
VSC 3p	-
VSC 4p	-

As soon as the fault signal is generated (0.4-0.5 ms), the DC breakers are triggered. After 1 ms, the DC breakers of line 1 and line 2 are switched off and the respective converters are isolated from the rest of the network.

The DC voltage in VSC1 and VSC2 begins to drop, up to the point where it becomes equal to the AC side phase-to-phase peak voltage, namely 212 kV or 0.66 pu. The VSCs DC voltage is shown in Figure 5.19.

From this moment on, the grid does not have a VSC controlling the DC voltage level. VSC3p and VSC4p do not experience an overcurrent, neither the current derivative peak surpasses the determined threshold. As a result, they remain connected, maintaining the power reference values they had before the fault occurrence. Both VSCs were controlled to absorb power from the DC grid. However, as both VSC1p and VSC2p, that used to provide power to the other two converters, are now disconnected, there is no other power source. Therefore, both converters, in their attempt to keep their power reference steady, absorb power from the DC link and the energy storage elements of the lines, until the DC

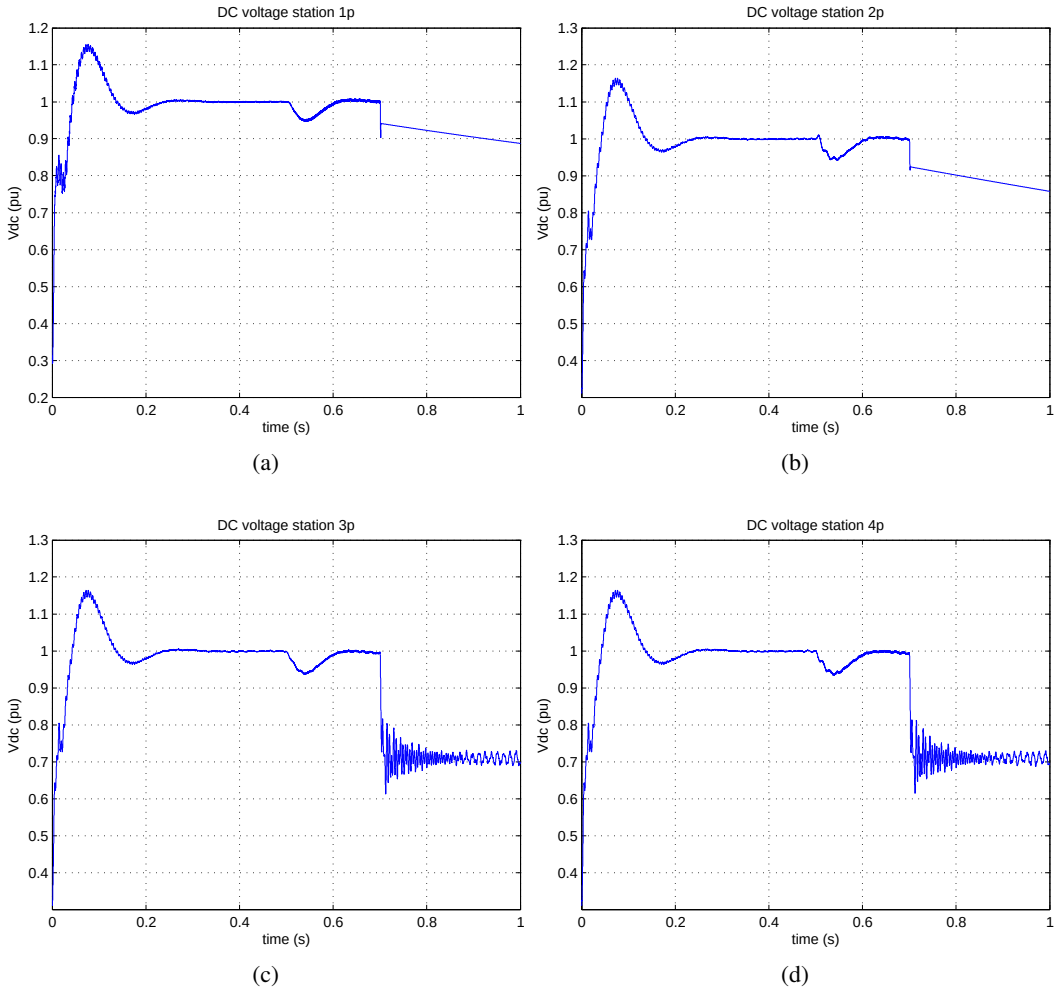


Figure 5.19: Positive pole VSCs DC voltage level for fault case with use of current derivative fault detection method

voltage drops to 0.73 pu. At this point, the AC current becomes zero and there is no more power exchange, as seen in Figure 5.21(c),(d). The current reference increases, as p_{ac} drops to zero and the difference $p^*_{ac} - p_{ac}$ becomes equal to the reference active power p^*_{ac}. The voltage value is imposed by the AC transformer configuration. As there is no direct ground on the secondary of the transformer, the DC capacitors do not get completely discharged through the converter IGBTs into the AC grid. In case there is a ground, e.g. the secondary winding has a star-grounded configuration, the current is circulating through the ground of the winding and the ground of the station neutral, bypassing the VSC. In this case, the DC link voltage drops to zero.

The VSC3p AC voltage is depicted in Figure 5.20. The new post-fault steady-state AC voltage has a peak of 1.1 pu. The balance between the AC voltage and the DC link voltage

occurs at the maximum linear region value of the modulation index, which is 1.15 for the space-vector pulse width modulation (SVPWM).
More specifically:

$$\frac{\hat{V}_{ac}}{\frac{V_{DC}}{2}} \leq 1.15 \Rightarrow \frac{1.1 \cdot 122.5}{\frac{0.73 \cdot 320}{2}} = 1.15 \tag{5.8}$$

where $\hat{V}_{ac}$ is the amplitude of the AC converter phase voltage.

Based on these observations, it can be concluded that, as the choice of grounding point is crucial, it should not be installed at a VSC station that controls the DC network voltage. If this is the case, in case of inability to trace the faulty line, the network will not operate properly after the affected lines are isolated, as the DC voltage level is no longer controlled. As a result, there are mainly two proposed solutions.

One of them is to ground the neutral of a station that controls power or ground the DC grid in any other location, so as to keep the DC voltage control safe. A second solution is to have more than one station in a multi-terminal network, controlling the voltage, in case one is affected by a fault. This would provide more reliability and redundancy to the network. However, in this case market issues arise and particular schemes need to be followed, concerning the power sharing [7].

In general, the fault tends to develop as shown in Figure 5.11. The absolute fault current contributions change, based on the limiting reactor size that is used for every case study. On the other hand, the AC side behavior of the terminals remains unchanged and the station reactions to a fault are independent of the DC breaker technology that is used. The only characteristics factor that changes is the time at which the station is disconnected from the

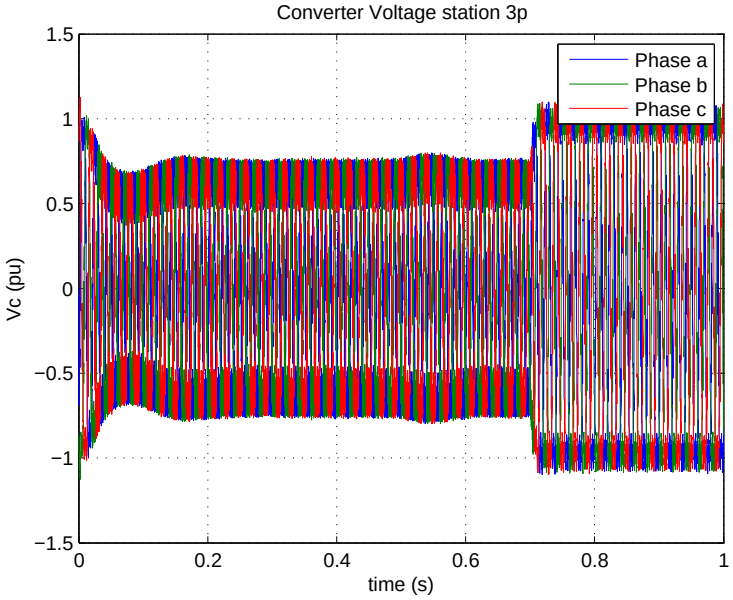


Figure 5.20: VSC3p AC voltage for fault case with use of current derivative fault detection method

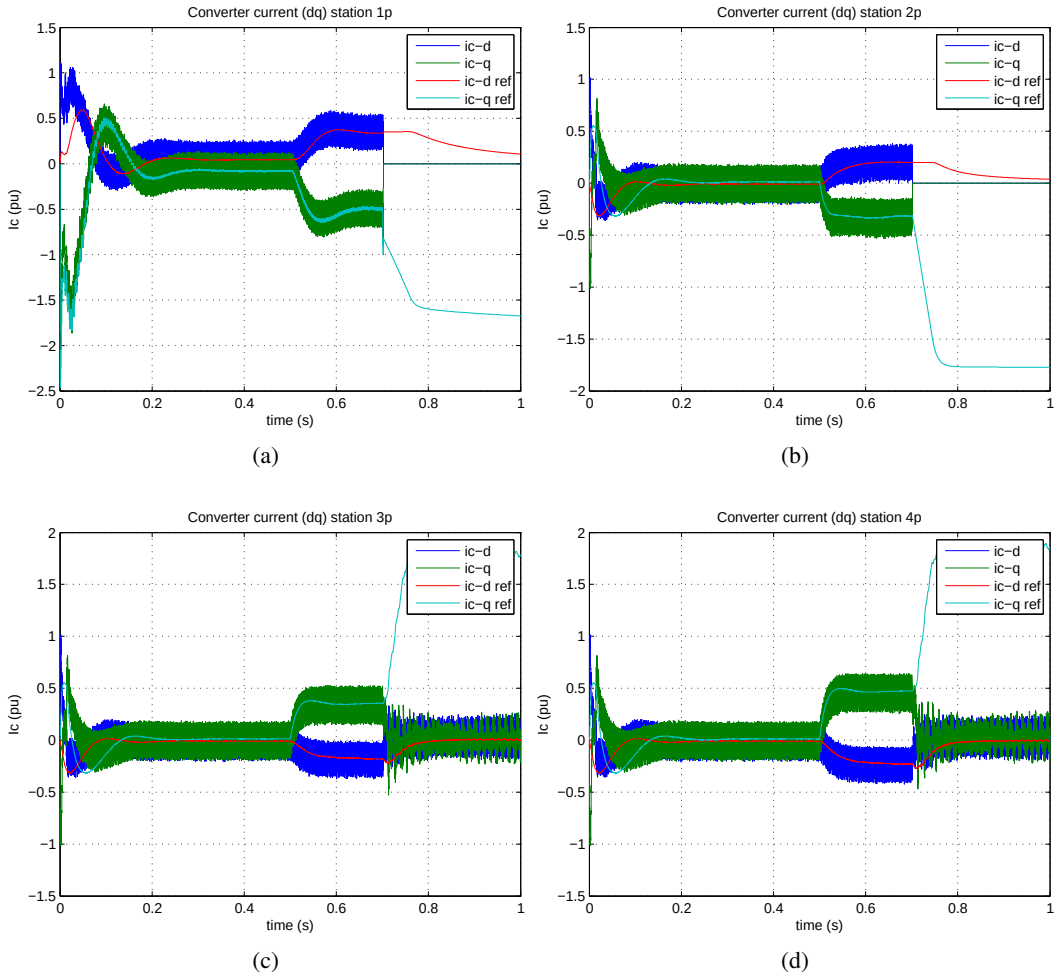


Figure 5.21: Positive pole VSCs AC current (dq) for fault case with use of current derivative fault detection method

grid. As a result, the converters AC-side characteristics will only be presented once for each investigated grid topology.

5.6.2 Current direction fault detection

This fault detection method appears to work better than the previous one for the bipolar topology with metallic return. The faulty line is distinguished within 0.6 ms from the rest of the grid, based on the current direction at its ends and 1.6 ms after the fault has occurred the line is isolated, due to the full semiconductor DC breakers, which have a total interruption time of 1 ms.

However, despite the faulty line isolation, an overcurrent occurs at station VSC 1, 2.7 ms after the fault occurrence. For the specific limiting reactor size, shown in Table 5.8, an

overcurrent is expected if the fault is not isolated, which is not the case in this simulation.

This can be explained, if the travelling wave properties are considered. As seen in Chapter 2, every line is characterized by its phase velocity and transport delay. To put it simply, the line's transport delay is the time required by one end of the line to realize a change at the other end. This delay mainly depends on the line capacitance and inductance and is calculated as:

$$\tau = \frac{l}{v} = l\sqrt{L'C'} \tag{5.9}$$

where τ is the transport delay, l is the length of the line and L', C' are the line parameters per unit length.

For the line connecting VSC1 to the central node, it has a length of 50 km and the per unit length parameters are given in Table 5.3. When calculating the total line inductance, the lumped inductance of the limiting reactor also needs to be taken into consideration. Therefore, the transport delay of this line is calculated as:

$$\tau = l\sqrt{L'C'} = 50km\sqrt{\left(\left(\frac{100mH}{50km}\right) + 0.2\frac{mH}{km}\right) \cdot 220\frac{nF}{km}} = 1.1ms \tag{5.10}$$

It can be seen that VSC1 realizes that the fault is isolated only after 1.1 ms, which results in a total 2.7 ms from the fault occurrence. The overcurrent occurs right at the moment the fault isolation is identified by VSC1. This affects not only the converter but the whole grid as well, as the IGBTs get blocked for their protection and a switch-off signal for the DC breakers is triggered.

This could have been avoided if a larger inductor was used, which would limit the rate of rise of the current and therefore provide sufficient time for the VSC 1 to adjust to the new steady state. The individual time delays are presented in Table 5.12.

Table 5.12: Total time necessary for VSC1 to realise the fault isolation with use of full semiconductor DC breakers and current direction fault detection method

Fault detection time (ms)	DC breaker interruption time (ms)	Line transport delay (ms)	Total time (ms)
0.6	1	1.1	2.7

Selective fault detection method conclusion

As aforementioned, the selection of the fault detection method is based on speed and selectivity. The results of the simulations can be summarized in Table 5.13.

Although in terms of detection time, both achieved similar times (0.4 and 0.6 ms), the faulty line cannot be distinguished based on the current derivative monitored at each station DC link. Consequently, the current direction fault detection method is more suitable for the bipolar configuration with metallic return and will be further investigated for the rest of the DC breaker technologies.

Table 5.13: Comparison of selective fault detection methods

	Speed	Selectivity
di/dt	+	-
Idc direction	+	+

5.6.3 Full Semiconductor DC Breakers (t_{open} = 1 ms)

In the previous simulation, it was concluded that the 50 mH limiting reactor was not enough to protect VSC1 from reaching overcurrent state after the faulty line had been isolated. Therefore 100 mH inductor size is chosen to reduce the current rate of rise.

The fault is detected 0.6 ms after the fault occurrence by VSC2p only. The faulty line 2 is isolated in 1.6 ms. Taking the line transport delay into account, the faulty line isolation gets realized by VSC1 a total time of 2.7 ms after the fault occurrence. This time is 1 ms smaller than the time needed for an overcurrent to occur at VSC1p (see Table 5.8).

Therefore, the faulty line is successfully isolated and the rest of the network remains connected and continues working properly. The only difference that is observed is the increased active power VSC1p has to inject, as it also needs to compensate for the loss of converter 2p, which was also injecting power to the DC network at the pre-fault stage.

The simulations result become more clear in Figure 5.22 and Figure 5.23. In these figures the DC voltage and the AC current of the positive pole converters are presented. The negative pole converter characteristics are shown in Appendix A.4. Although the DC voltage level has a dip as soon as a fault occurs, it recovers after the faulty line is isolated and continues to be controlled at the nominal level. The oscillations are the result of the transient situation during a fault. A discharge of the energy storage elements of the DC grid takes place in the beginning of the fault. After the fault is isolated, these components need to get charged again to reach a new steady-state. The oscillations are, therefore, the result of this discharge and recharge process. The same oscillations are observed for the AC current shown in Figure 5.23.

5.6.4 DC Breaker Hybrid I (t_{open} = 2 ms)

In this section the second fastest DC breaker is simulated. The only parameter that is of interest in this study is the total interruption time of the breaker. It has been mentioned in Chapter 3 that the total interaction time of this technology is 2 ms, as claimed by ABB. In the simulations, it is assumed that the DC breaker does not change the RLC parameters of the network. Therefore, it can be assumed that the limiting reactor in the hybrid breaker is the same as the one already being used (100 mH).

From the simulations, the same findings as in the case study for the fully semiconductor breaker with a 50 mH limiting reactor were derived. More specifically, although the faulty line is interrupted within 2.6 ms, VSC1p exhibits an overcurrent at 3.7 ms (Table 5.8). This issue can be attributed to the 1.1 ms transport delay of line 1. The individual time delays are shown in Table 5.14.

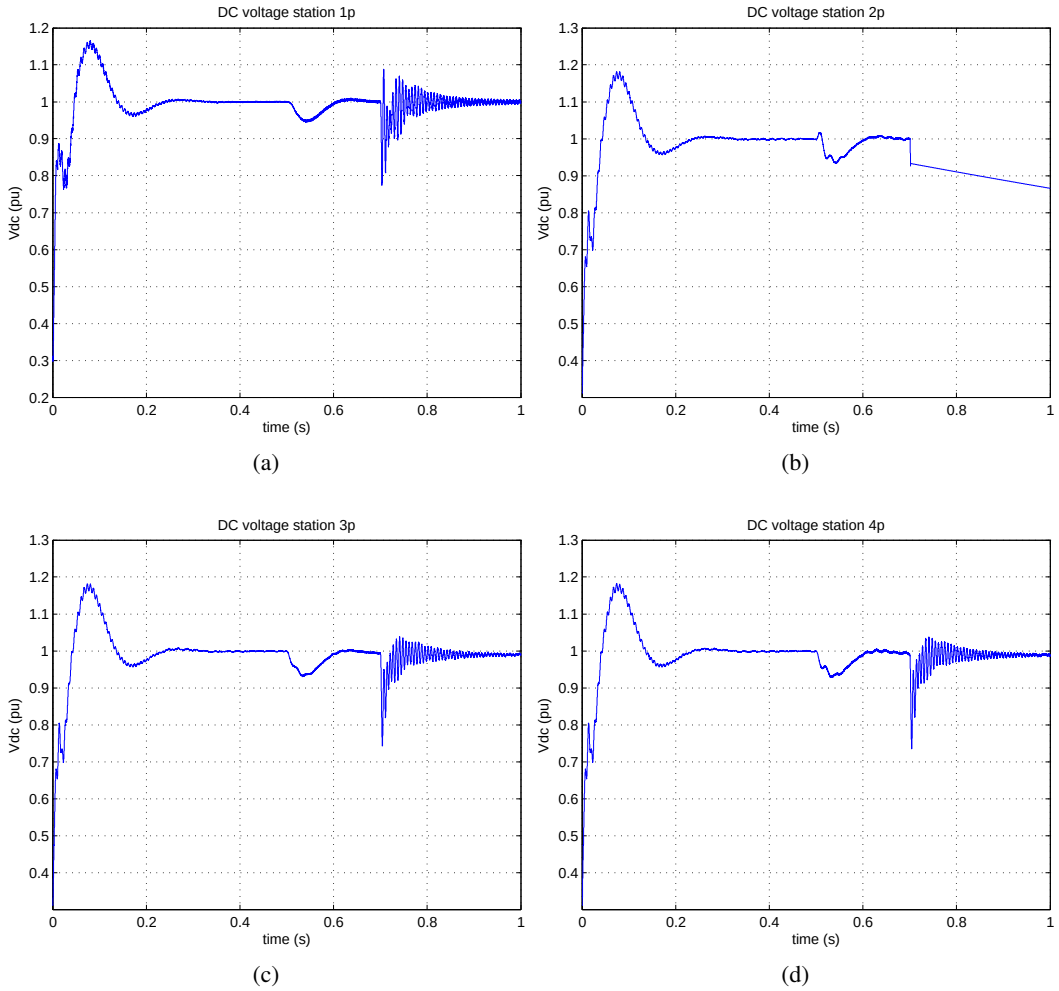


Figure 5.22: Positive pole VSCs DC voltage level for fault case with use of current direction fault detection method and full semiconductor DC breakers

For the specific case, this could be prevented by using a bigger limiting inductor, i.e. 200 mH, however, there are cost issues and control issues that need to be considered as well, when designing a DC network. A cost-benefit analysis in this case would be proposed, but remains out of the scope of this thesis.

Although the VSC station is blocked, it remains safe, as the fault has already been isolated and therefore the station remains in the safe current region, without contributing any excess current to the fault. The respective line is isolated after an additional time of 2 ms from the overcurrent detection.

As long as the converter is not damaged, its operation can be resumed, after the station is disconnected, by opening the AC breakers. The total opening and re-closing time of the AC breakers, depends on their technology, but can be assumed to be approximately 200 ms

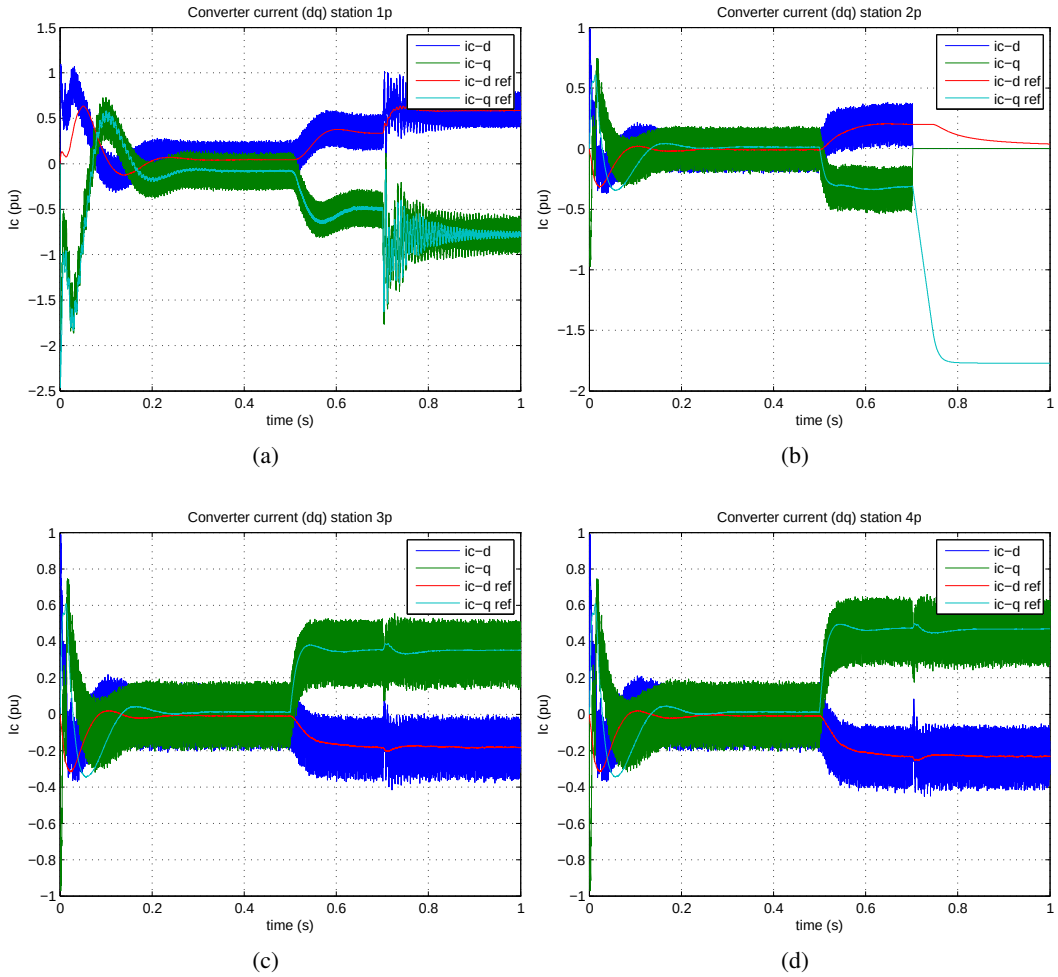


Figure 5.23: Positive pole VSCs AC current (dq) for fault case with use of current direction fault detection method and full semiconductor DC breakers

[78]. It has to be noted that the converter AC breakers need to be placed after the AC filters, in order to prevent operation disruption of the negative pole converter.

Table 5.14: Total time necessary for VSC1 to realise the fault isolation with use of Hybrid I DC breakers and current direction fault detection method

Fault detection time (ms)	DC breaker interruption time (ms)	Line transport delay (ms)	Total time (ms)
0.6	2	1.1	3.7

5.6.5 Hybrid II (t_{open} = 30 ms) and Resonance DC Breakers (t_{open} = 60 ms)

The second investigated hybrid DC breaker has a total interruption time, which is basically determined by the mechanical breaker switching times. The worst case is simulated, namely an interruption time of 30 ms.

The fault gets identified by VSC2p 0.6 ms after its application and the DC breakers are triggered. The rest of the stations experience an overcurrent at different points in time (see Table 5.8).

The time from the blocking of the IGBTs until the DC breakers are opened is 30 ms. The converter valves cannot handle the overcurrent for more than 1 ms, as it was specified in Table 5.6. As a result, the converters are damaged before the fault is isolated from the DC grid. This represents a huge economic impact and, therefore, such a design cannot be permitted. It is, however, for the completeness sake included in the study.

Assuming hypothetically that the converters have the capability to handle the overcurrent for such a long time, 37.5 ms after the fault all the positive pole DC breakers are switched off and the network needs to be disconnected by opening the AC breakers in order to safely resume operation.

The same conclusions can be drawn for resonant DC breakers, which have a even higher total interruption time of circa 60 ms. Currently, there are no available methods e.g. limiting reactors, through which these technologies can be applied successfully for DC fault handling in HVDC networks with bipolar configuration with metallic return.

5.7 Conclusions

The previous analysis was made under the assumption that the DC breaker topology does not influence the characteristics of the grid and thus does not affect the development of the fault (e.g. line currents). The only parameter that changes the fault characteristics is the size of the limiting reactors used on the DC side. This affects the peak fault current and the rate of rise of the station fault contribution, therefore changing the time it takes for each VSC to realize there is a DC fault in the network.

Taking these assumptions into account, it was found that the closer the fault is at the central node of the radially configured multi-terminal grid, the less time the VSCs have to react. However, for the bipolar configuration with metallic return, the most critical parameter that affects the station response to the fault is the point of grounding.

The VSC which has its neutral directly grounded experiences high current derivatives the moment the fault occurs. As a result, the current derivative selective method cannot be used for the bipolar topology with metallic return, as its sensitivity depends greatly on the grounding location. Consequently, the current direction fault detection method was chosen as most appropriate.

Concerning the fault current development, this can be divided into two stages, a transient that last approximately 20 ms and a steady state stage. During the transient, the fault current is mostly a result of the discharge of the energy storage elements of the grid. During the steady-state stage, these contributions are almost zero and the fault current is a result of the AC grids, which continue feeding the fault.

Another general issue that was observed, during the simulations, is that the VSC responsible for the DC voltage control is the first to experience an over-current on the AC side and thus the first that has its IGBTs blocked. This can be attributed to the fact that this station has the responsibility to provide for any excess power need in the grid, as it is not actively controlling its active power.

The second station affected is the one closest to the network ground. This is expected, as the positive pole-to-neutral short-circuit is first experienced in this station. The rest of the stations that control active power are the last to develop overcurrents, even if the point at which the fault occurs is closer to them. Among those stations, the fault is first detected at the station which injects active power into the DC network at the pre-fault stage, as, otherwise, the current direction needs first to change, which accounts for a few tenths of milliseconds, before feeding the fault.

Finally, the simulations confirm the theoretical expectations that the Hybrid II and the resonant breakers are not yet mature enough to handle DC contingencies for this kind of grid topology. The other two breaker technologies can be used, but only in combination with large limiting reactors. The semiconductor breakers need at least 100 mH reactors, while the Hybrid I DC breakers at least 200 mH.

Chapter 6

DC Fault Analysis: Other Grid Topologies

6.1 Introduction

In Chapter 5, the pole-to-ground fault for the bipolar HVDC grid topology with metallic return was simulated and discussed. The same methodology is followed in the present chapter for four other multi-terminal topologies and a comparison is made, based on their performance during a fault. The workflow of the used methodology is presented in Figure 6.1. The different components fault current contributions are studied, as well as the effect of the DC breaker technology on the system and the coordination of the VSC stations are evaluated.

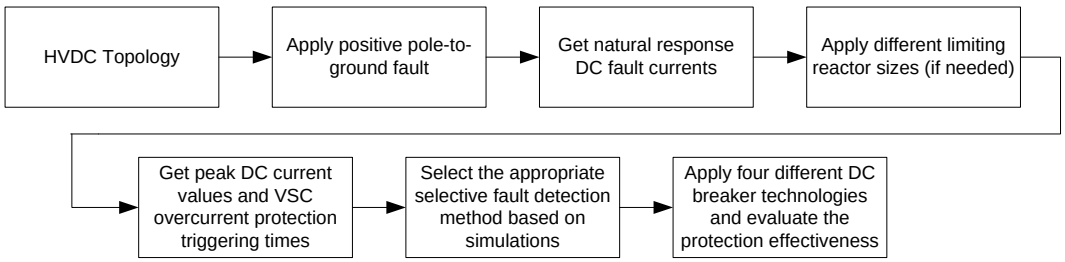


Figure 6.1: Workflow of the methodology used in the topologies study

6.2 Bipole with ground return

In this section the bipolar HVDC network configuration with ground return is investigated. A figure of the simulated DC network is shown in Figure 6.2.

This topology differs from the previous one as all the station neutrals are directly grounded and, in case of unbalances, the poles return current flows through the ground. Under normal circumstances, the ground current is almost zero, however, in fault cases, there is a high current flowing through the ground, which is prohibited by some countries regulations [86] and can interact with human, animal or marine life, telecommunication networks and

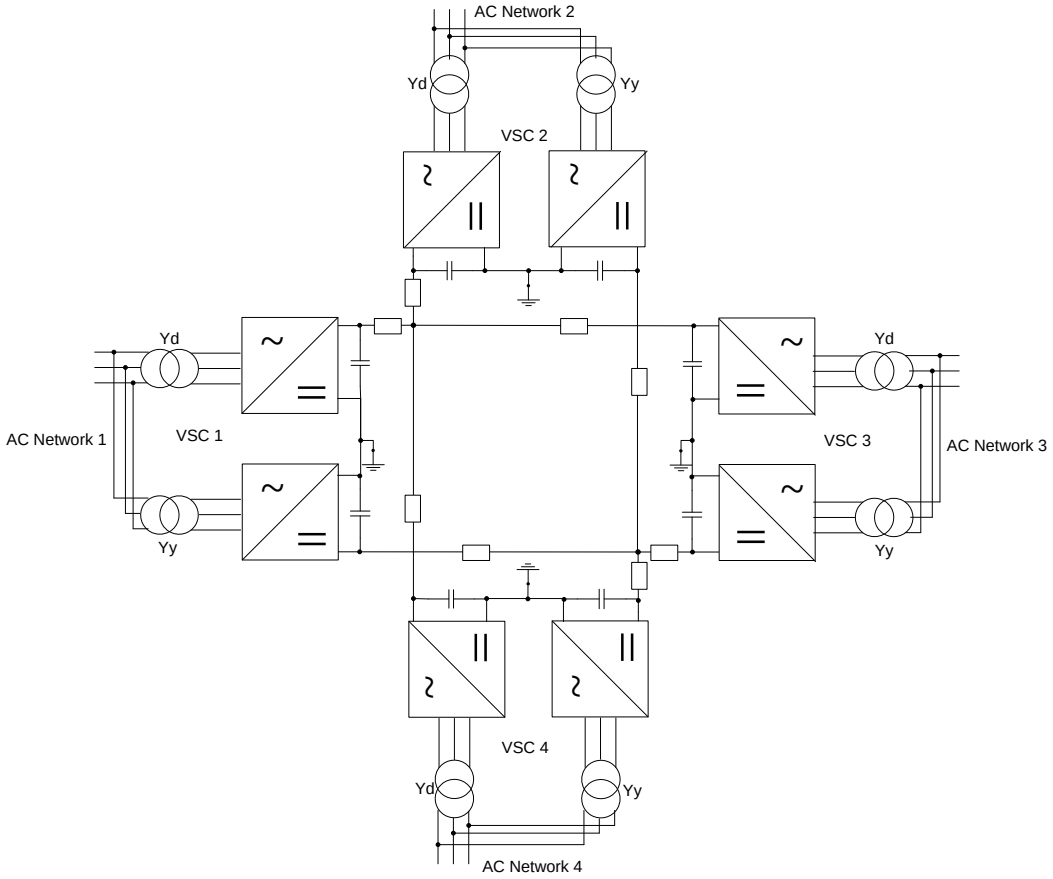


Figure 6.2: Bipolar DC network with ground return

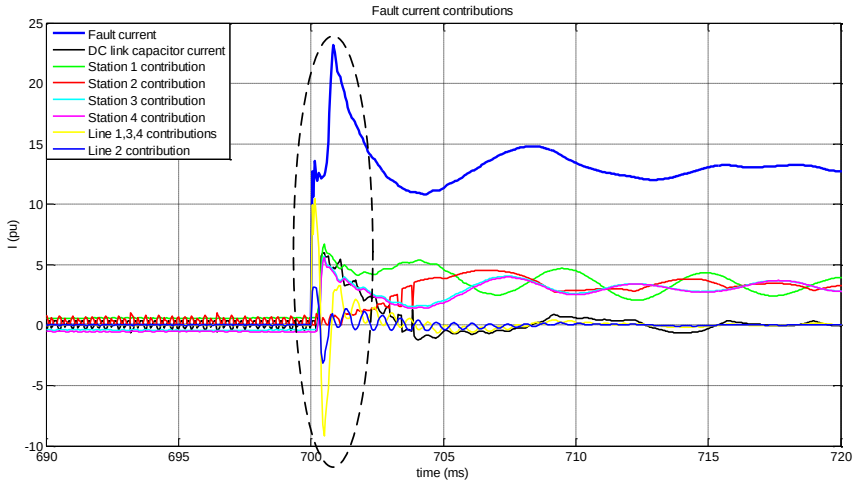
buried metallic structures [87]. Consequently, such a topology is not usually favored. Nevertheless, in case DC breakers are implemented, the fault can be isolated quickly enough to prevent unwanted effects to the environment.

A positive pole-to-ground fault is studied for this topology and the fault characteristics are described. All the AC and DC system parameters are the same as for the bipolar topology with metallic return, to provide a fair comparison between the studied topologies. The time order of events is the same as described before in Table 5.7.

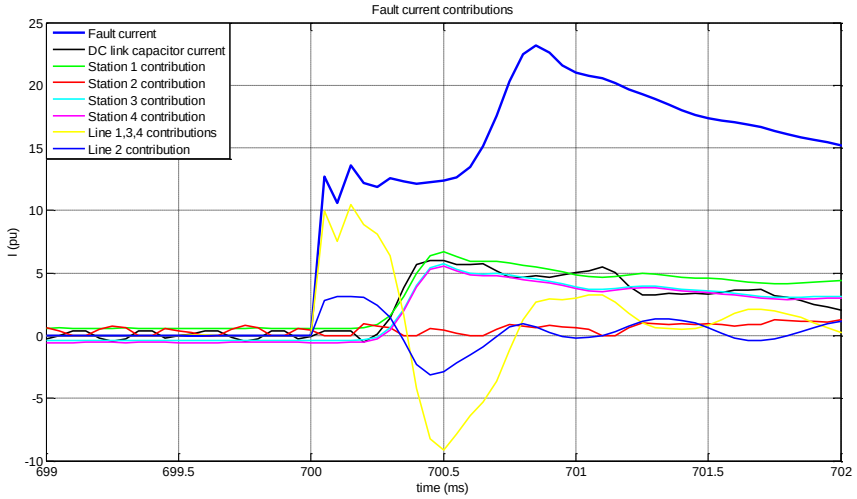
6.2.1 Fault current contributions

The positive pole-to-ground fault is applied at 49 km from station VSC2 on line 2. The fault current contributions, in case no fault clearance takes place, from the different network sources are presented in Figure 6.3.

From Figure 6.3 it can be seen that the transient period is circa 20 ms. The initial peak of the fault current comes from the discharge of the energy storage elements of the lines and the limiting reactors. Only 0.3 ms after the fault, the contributions from the DC link



(a) Fault currents



(b) Zoom-in view

Figure 6.3: Fault current contributions

capacitors and the stations become predominant. Finally during the steady-state, all the stations seem to be equally contributing to the fault with currents from 3 to 3.5 pu, which add up to a total of 12.5 pu current at the point of the fault.

Compared with the fault current contributions for case 3 (fault at 49 km) in the bipolar configuration with metallic return (Figure 5.11(c)), the initial fault current peaks are the same, i.e. circa 12 pu. However, the second peak 0.9 ms after the fault, is higher in case of ground return, reaching 23 pu in comparison to 18.8 pu with metallic return.

This difference can be attributed to the impedance of the metallic return cable. In case of a ground return, the impedance from the VSCs to the fault is lower than in case of a metallic return. In the bipolar topology with metallic return, the VSC responsible for voltage control (VSC1), whose neutral was directly grounded, was contributing the most from the beginning of the fault and the currents from the rest of the stations were increasing with a delay, never exceeding 5 pu. In case of a ground return, all station neutrals are directly grounded, and thus, all VSCs respond faster and more uniformly to the fault.

6.2.2 Positive pole-to-ground fault application with limiting reactors

In case of a fault in a bipolar HVDC network with ground return, the station currents increase above their ratings limit within 0.4 ms from the time of fault occurence, as observed in Figure 6.3(b). Therefore, the effect of limiting reactors on the fault current needs to be evaluated. Five limiting reactor values in the range from 1 mH to 200 mH are compared, as done for the bipolar topology with metallic return.

In Figure 6.4 it can be observed that, for VSC1p and VSC2p, the drop in the peak current with higher inductance values is almost 3 pu. For VSC3p and VSC4p this is estimated at 2 pu.

As mentioned for the bipolar topology with metallic return, the VSC responsible for DC voltage control is the first to experience an overcurrent during a fault, due to its response to provide first any excess need of power in the grid. The second station that gets affected is the one attached to the faulty line and, afterwards, the remaining ones that control power follow. Therefore, it is logical that the initial overcurrent experienced during a fault is higher for VSC1p and VSC2p and, thus, the effect of the reactor is higher at these two stations.

The influence in the total fault current is shown in Figure 6.5. If a 1 mH inductor is used, the peak fault current reaches 22.81 pu, whereas it only gets up to 13.5 pu if a 200 mH inductance is applied.

The limiting reactor size influences the peak current occurrence significantly. In Table 6.1 the effect of the different limiting reactors on the time it takes for each VSC to experience an overcurrent and for the IGBTs protection to be triggered is presented. This effect is also depicted in Figure 6.6. The negative pole converters do not experience any overcurrent, and thus, the protection measures are not triggered.

If compared with the respective values from Table 5.8, the time it takes for the converters to experience an overcurrent is less, as their neutral are directly grounded in case of a ground return. The lack of return path impedance in the neutral line can be a reason for this time difference.

6.2.3 Positive pole-to-ground fault application with DC breakers

In this section DC breakers are simulated in the bipolar configuration with ground return. The selection of the fault detection method that will be used, is based on simulations in a grid with 50 mH limiting reactors and full semiconductor DC breakers.

Current direction fault detection simulation

Firstly, the current direction fault detection method, which was used for the bipolar topology with metallic return is simulated.

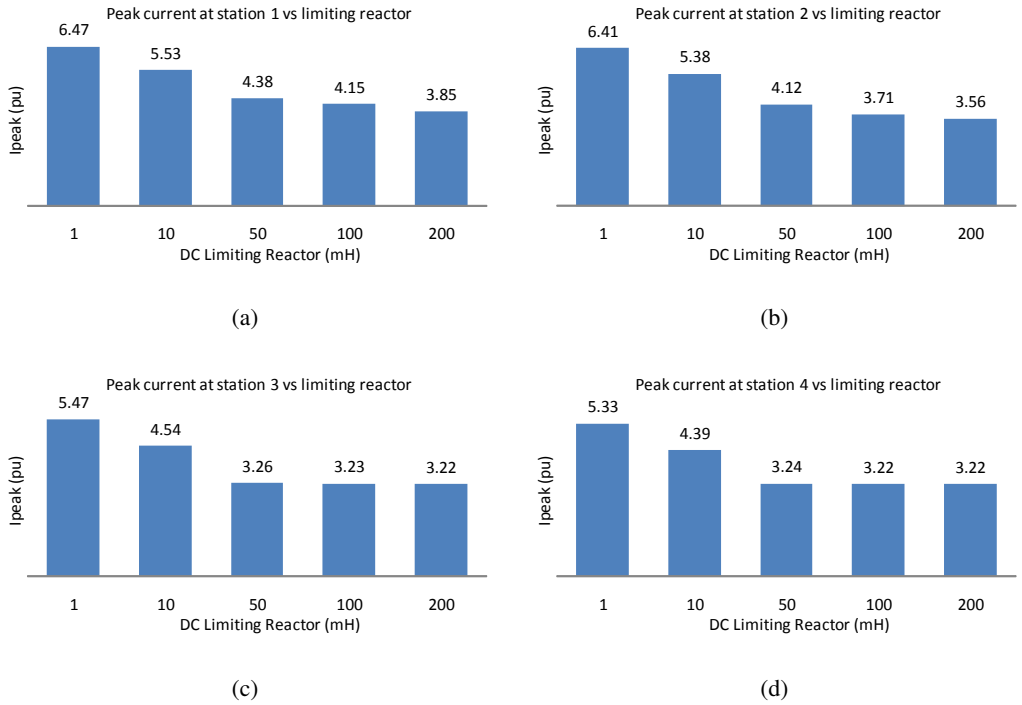


Figure 6.4: Peak current at positive line for different limiting reactor sizes for bipolar topology with ground return (measurement after limiting reactor)

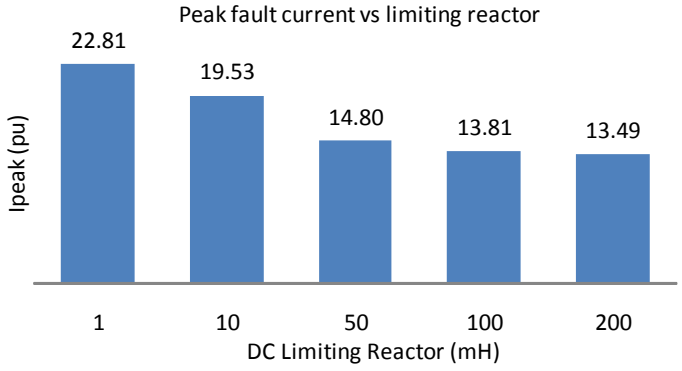


Figure 6.5: Peak fault current for different limiting reactor sizes for bipolar topology with ground return

Table 6.1: Fault signal detection times from the moment of fault occurrence for different reactor sizes for bipolar topology with ground return

	Time (ms)			
Reactor size (mH)	**VSC 1p**	**VSC 2p**	**VSC 3p**	**VSC 4p**
1	1.8	3.8	4.6	4.8
10	2.0	3.8	4.8	4.8
50	2.7	4.8	5.5	5.6
100	3.5	6.1	6.4	6.5
200	5.5	7.6	8.1	8.1

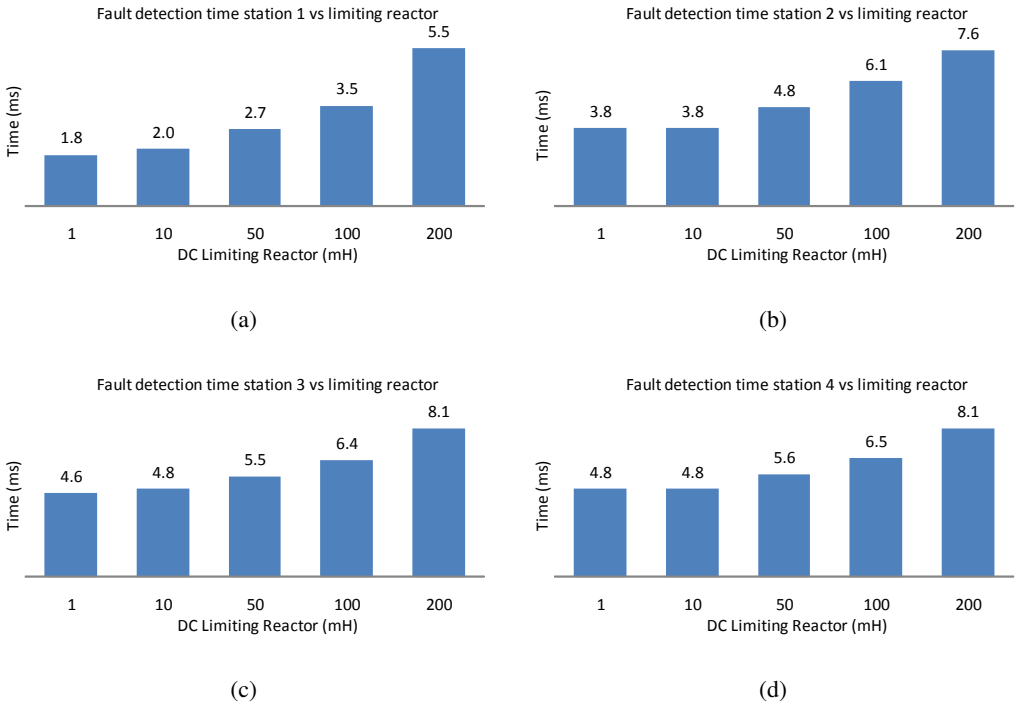


Figure 6.6: Fault signals for each positive pole VSC with use of different limiting reactor sizes for bipolar topology with ground return

From the simulations, it was derived that the detection method has the ability to distinguish the faulty line, within 0.6 ms. Therefore, this method fulfils the requirements for a successful selective fault detection method.

It has to be noted that although the faulty line is isolated in time, due to the line transport delay (1.1 ms), the VSC1p still experiences an overcurrent 2.7 ms after the fault occurence.

Current derivative fault detection simulation

The second selective method was also simulated for the same topology. From the simulations it was observed that in comparison to the case with metallic return, a specific current derivative threshold could be identified for the VSC attached to the faulty line. This can be attributed to the symmetry of the topology. The peak current derivative values monitored, are presented in Table 6.2.

Table 6.2: Current derivative peak values for each VSC for bipolar topology with ground return

Station	**di/dt peak (kA/ms)**	**Difference (%)**
VSC 1p	6.36	-2.1
VSC 2p	6.5	-
VSC 3p	6.355	-2.2
VSC 4p	6.35	-2.3

From the table values, a threshold of 6.4 kA/ms was chosen for the fault detection. This threshold is chosen based on the first current derivative peak after the fault.

Based on the previous observations, it can be concluded that this method also fulfils the selectivity requirement in this case. Moreover, the fault signal is generated within 0.4 ms from the fault, thus making it faster by 0.2 ms from the current direction selective method. However, this method could be difficult to implement in practice since the difference between the stations current derivative peak is rather small. The characteristics of the selective methods are summarized in Table 6.3.

Table 6.3: Comparison of selective fault detection methods

	Speed	Selectivity
di/dt	++	+
Idc direction	+	+

From Table 6.3 it can be concluded that both methods are applicable in this topology. The current derivative method is chosen to be investigated for this topology, as the current direction method was already studied for the bipolar topology with metallic return.

An inductor size of 100 mH is used for the simulations. This size is chosen based on the trade-off between inductor size, cost and network stiffness, as well as to accommodate a direct comparison between the two bipolar cases: metallic return and ground return.

Full Semiconductor DC Breaker (t_{open} = 1 ms)

The current derivative selective method is able to detect the fault 0.4 ms after its occurrence. At this moment the DC breakers are triggered and the faulty line is isolated from the DC

grid in 1.4 ms. Due to the discharge of the lines and the partial discharge of the DC link capacitors, the voltage and the current experience an oscillation before they reach a new steady-state.

A new operating point, with less than 1% voltage ripple, is reached within 300 ms from the fault as shown in Figure 6.7.

Figure 6.8 presents the AC-side converter currents for the positive pole converters. The negative pole converters AC currents and DC voltage are given in Appendix A.5. It can be observed that only the current of VSC1p changed and increased to a new steady-state level. This occurred because VSC1 was controlling the DC grid voltage.

At the pre-fault stage the VSC2p was feeding power to the DC grid. As soon as it was disconnected, this power needed to be provided by VSC1p, as VSC3p and VSC4p kept their power reference level steady. The rest of the positive and negative pole converters did not experience any transients and continued their normal operation unaffected by the fault.

Based on the requirements for a faulty line isolation, this case can be judged as successful; no converters are damaged and normal operation is resumed within a reasonable time period after the faulty line is isolated.

DC Breaker Hybrid I (t_{open} = 2 ms)

Using this breaker technology, the total DC breaker interruption time increases to 2 ms (see Table 5.9). With use of 100 mH limiting inductor, the VSC1p overcurrent protection is activated at 3.5 ms, namely 1.1 ms after the DC breakers opened (2.4 ms after the fault occurrence). This can be attributed to the transport delay of the line, which was calculated to be 1.1 ms. Therefore, the use of a higher inductor value, which would further decrease the rate of rise of the station current could help overcome this problem.

The DC voltage level of the positive pole stations is shown in Figure 6.9. Initially the voltage drops, following the voltage across the fault resistance. As soon as the faulty line is isolated, the VSC1p tries to recover the DC grid voltage level. However, at 3.5 ms the IGBTs of VSC1p are blocked and the voltage is no longer controlled.
After the DC breakers of line 1 open, the DC link capacitor gets discharged, up to the point where its voltage becomes equal to the peak value of the rms AC voltage, namely $\sqrt{2} \cdot 150kV = 212kV$ or 0.66 pu. The voltage level at the healthy stations VSC3p and VSC4p drops to 0.73 pu. This is attributed to the AC transformer configuration, as explained in Chapter 5, section 5.6.1.

The current at stations VSC1p and VSC2p becomes zero, after their respective lines are off, while VSC3p and VSC4p cannot exchange power, as they both maintain their power reference values and thus, they are both controlled at that moment to absorb power from the DC grid. As a result, initially they absorb power from the DC link and the energy storage elements of the lines, until their current levels drop to zero. In case the secondary winding of the AC transformer was grounded, the DC link voltage level would drop to zero, as it would be fully discharged through the ground return path and the converter negative phase leg would be bypassed. The AC current characteristics for the positive pole converters are shown in Figure 6.10. The negative pole converter AC currents and DC voltage observed are the same as the ones shown in Appendix A.5 for the case of Solid state breakers.

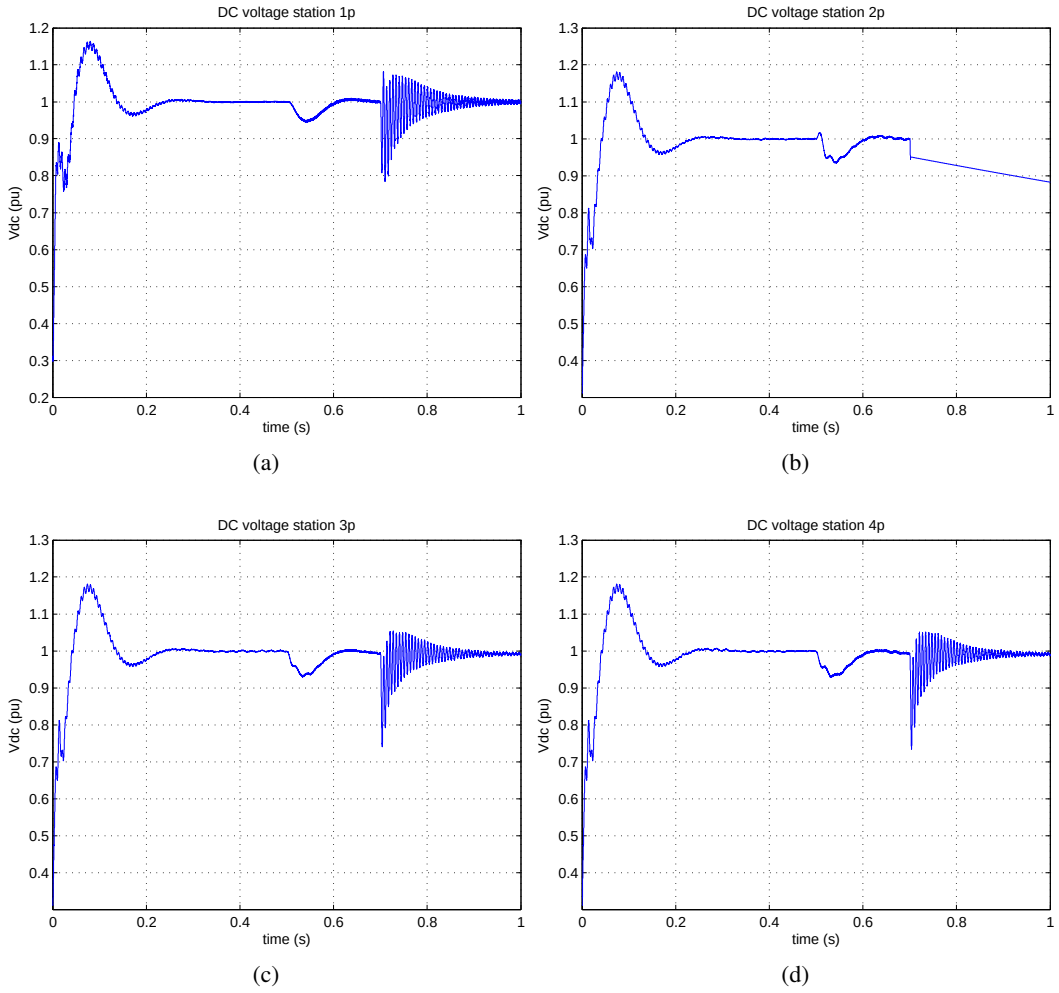


Figure 6.7: Positive pole VSCs DC voltage level for fault case with use of current derivative fault detection method and full semiconductor DC breakers

Although both VSC1p and VSC2p converters were isolated from the grid, they were not damaged, as the experienced currents remained within their rating capabilities. However, the faulty line isolation is not successful and more measures need to be taken to return to normal operation.

Hybrid II (t_{open} = 30 ms) and Resonance DC Breakers (t_{open} = 60 ms)

The other two simulated technologies have much higher interruption times. Simulation results for the positive pole VSCs with use of Hybrid II DC breakers are provided in Figure 6.11 and Figure 6.12. Regarding the negative pole converters, no change was observed in the AC currents and the DC voltage level and thus, the respective waveforms are the same

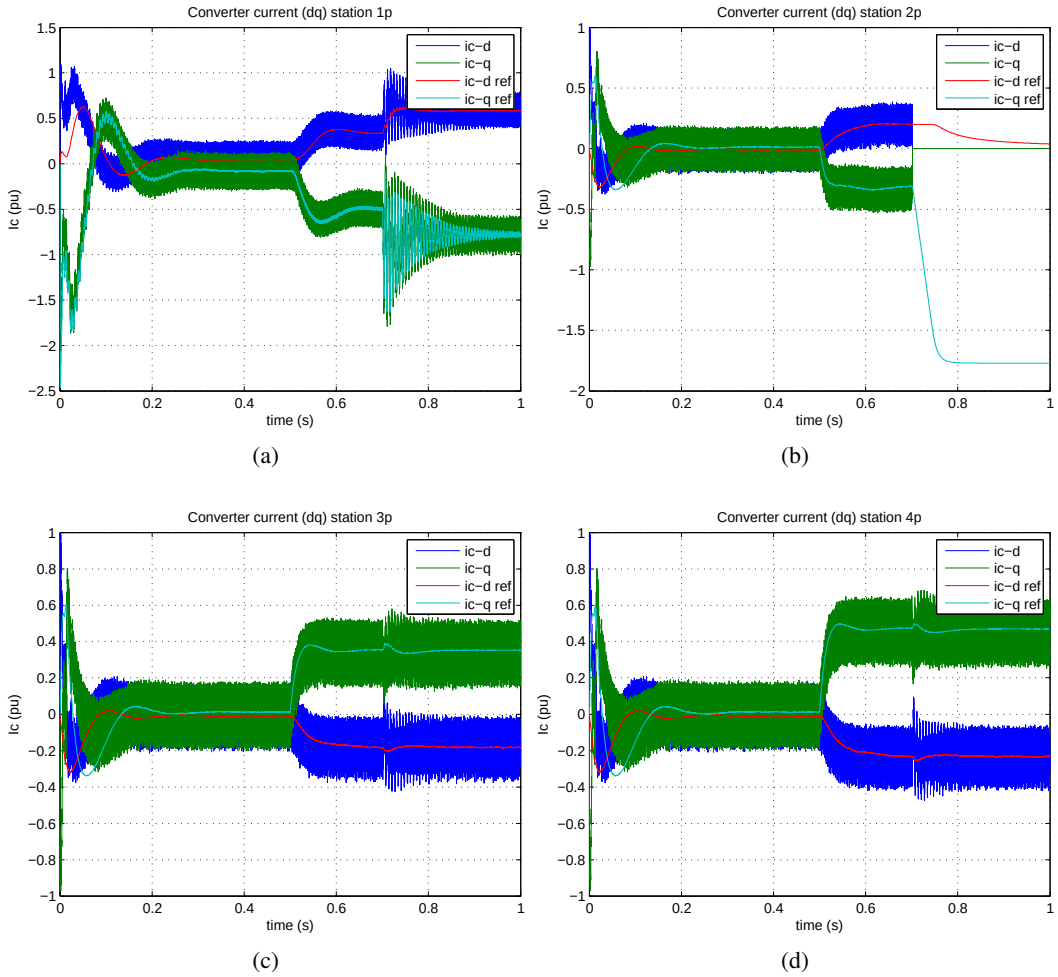


Figure 6.8: Positive pole VSCs AC current (dq) for fault case with use of current derivative fault detection method and full semiconductor DC breakers

as for the case of Solid state DC breakers presented in Appendix A.5.

It can be observed that the DC link voltage level drops to a point where it becomes equal to the voltage across the fault resistance, namely circa 0.5 pu. All the stations experience overcurrents at different moments (see Table 6.1), and all of them can be safely assumed to be damaged before the DC breakers are switched off.

This assumption is based on the current ratings of the HVDC converter valves, as presented in Table 5.5. All the stations experience high overcurrents for more than 1ms; more specifically for the whole period until the breakers open, which they are not able to withstand. The presented results do not take the ratings (thermal and electrical) into account and so the simulations continue as if the converters remain unharmed.

At the moment the breakers open, the DC link voltage increases instantly, due to the

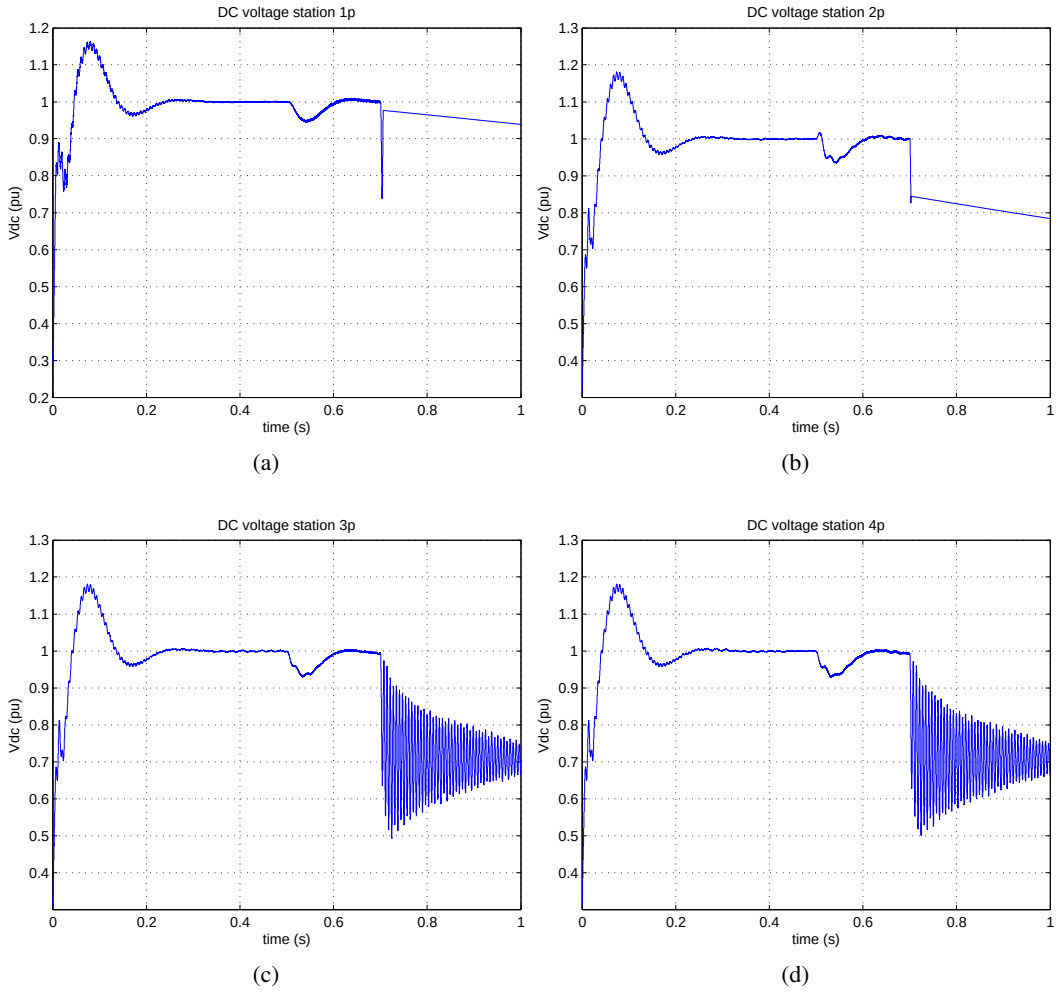


Figure 6.9: Positive pole VSCs DC voltage level for fault case with use of current derivative fault detection method and hybrid I DC breakers

current coming from the converter bridge, which is not propagated to the fault and then it starts dropping, following the characteristics that were already described for Hybrid I DC breaker case. The AC currents of the converters drop to zero.

Finally, the same grid response is observed for the resonance breakers, which are even slower, and are therefore omitted. The only difference in comparison with results for the DC breaker Hybrid II would be the moment in which the breakers are opened.

6.2.4 Partial Conclusions

The bipolar topology with ground return exhibits the same overall response with respect to the topology with metallic return. However, its performance is worse in absolute terms.

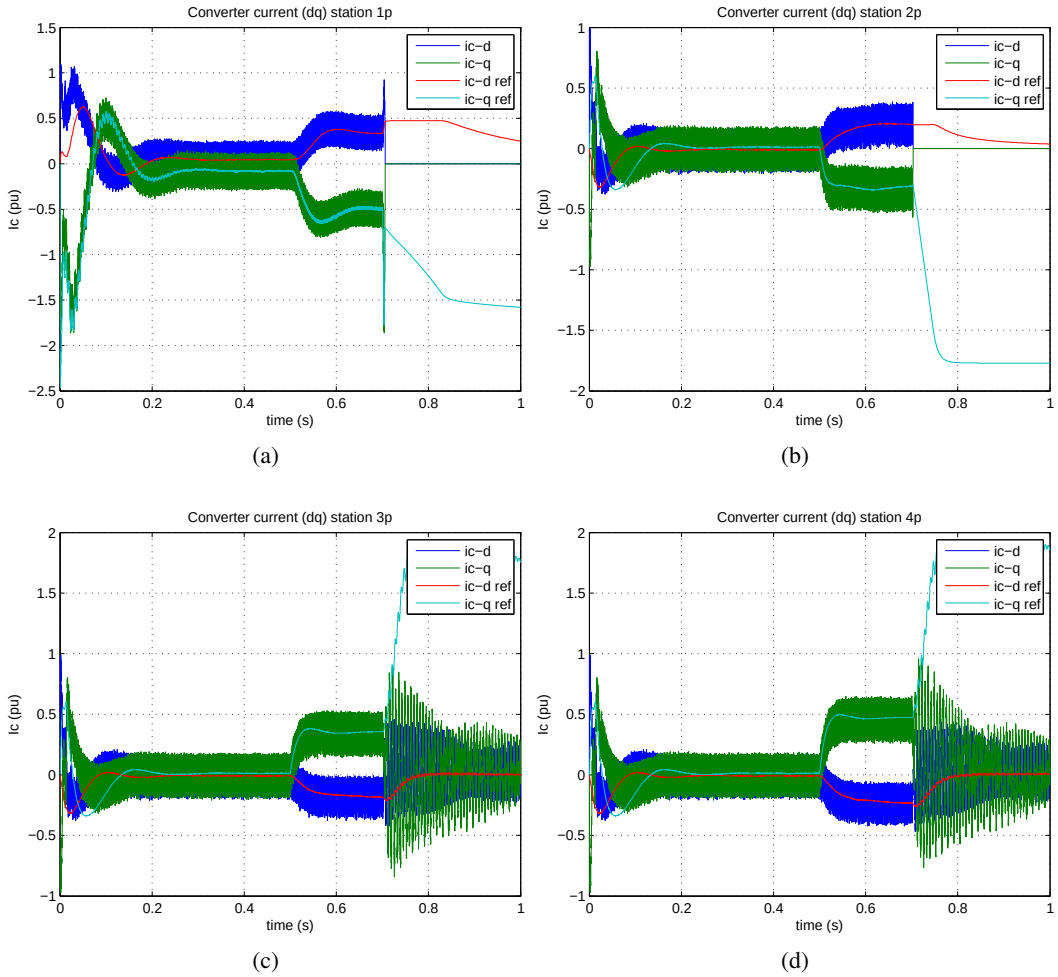


Figure 6.10: Positive pole VSCs AC current (dq) for fault case with use of current derivative fault detection method and hybrid I DC breakers

The fault current contributions from the stations are worse, although initially identical, since the used cables have the same characteristics. The VSCs are affected by the fault faster and therefore they experience high overcurrents within less than 0.4 ms.

Comparing Table 5.8 to Table 6.1, the overcurrents are experienced faster (up to 2 ms faster) in the case of ground return, thus leaving less time to the stations to react and for the breakers to isolate the fault without disturbing normal operation. Moreover, the station fault currents reach higher peaks, which can damage the VSCs. However, the use of limiting reactors can provide a solution to prevent this to some extent, along with the use of DC breakers. It also needs to be stressed that in both the investigated bipolar configurations, the negative pole converters were not influenced by the positive pole-to-ground fault.

Finally, only in case of the metallic return, small initial oscillations were observed at

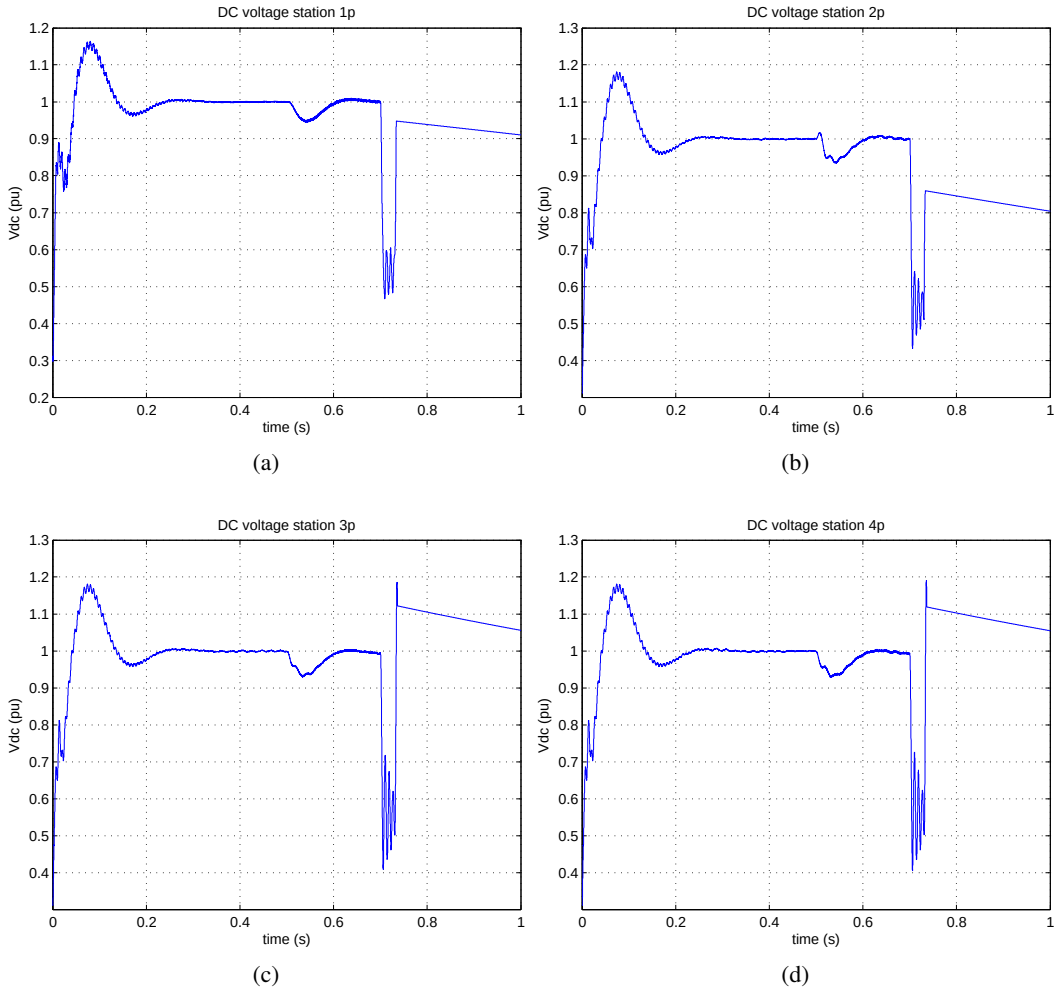


Figure 6.11: Positive pole VSCs DC voltage level for fault case with use of current derivative fault detection method and hybrid I DC breakers

the negative pole converter, which has its neutral directly grounded. This can be attributed to the fact that, in case of ground return, the fault current gets splitted into four, as it returns through four identical groundings in the grid. In case of metallic return only one return path is available and thus, the returning current was up to 19 pu during the transient period, affecting the converter attached directly to the neutral grounding.

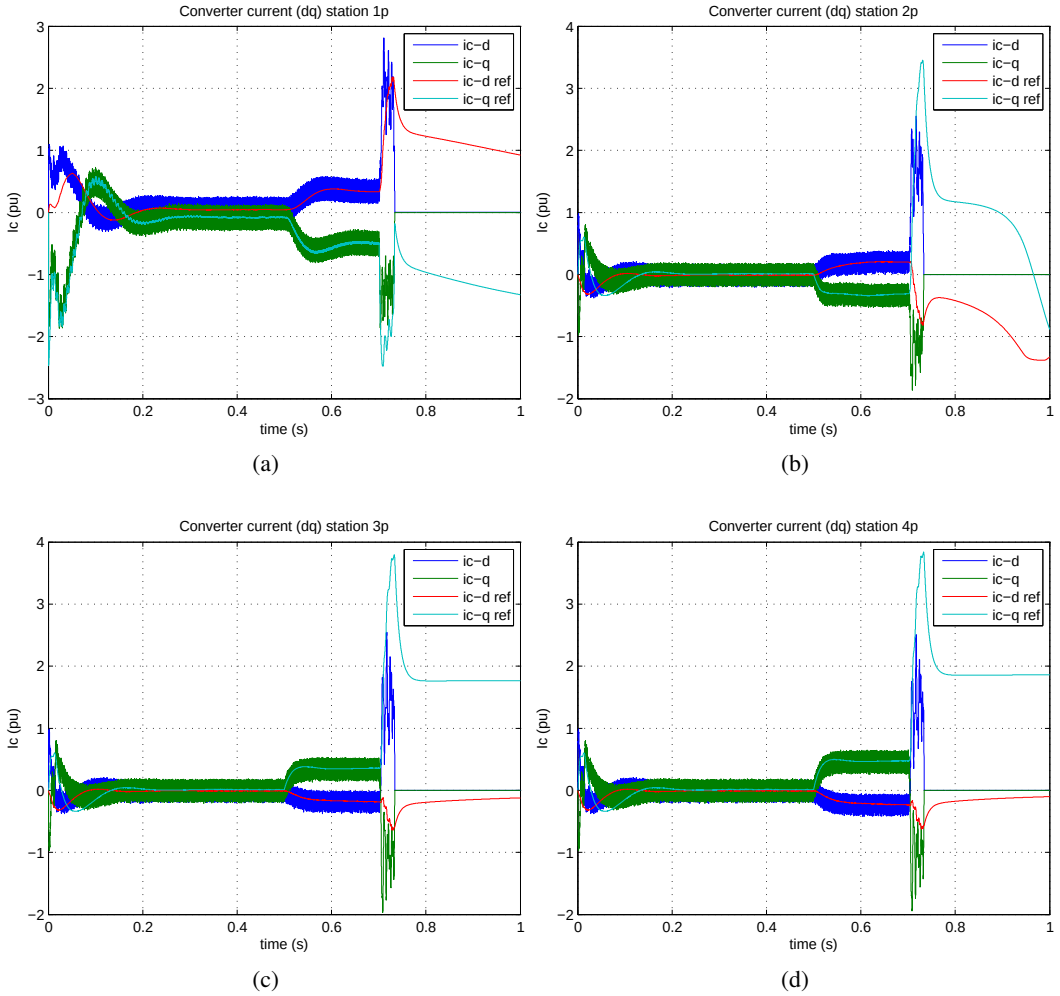


Figure 6.12: Positive pole VSCs AC current (dq) for fault case with use of current derivative fault detection method and hybrid I DC breakers

6.3 Asymmetric Monopole with Metallic Return

In this section the asymmetric monopolar topology with metallic return is examined for the same four-terminal HVDC configuration. The outline of the system is presented in Figure 6.13. This system can be directly derived from the respective bipolar configuration with metallic return if only the positive pole converter of the station is considered.

Compared to the bipolar topology, the VSC station power rating is halved, resulting in 600 MVA, while the positive pole DC voltage nominal level remains at +320 kV. The resulting nominal DC current remains at 1875 A. As the DC network specifications do not change, the DC cables and the DC link capacitor size are the same as for the bipolar configuration. The grid parameters can be found in Table 5.3.

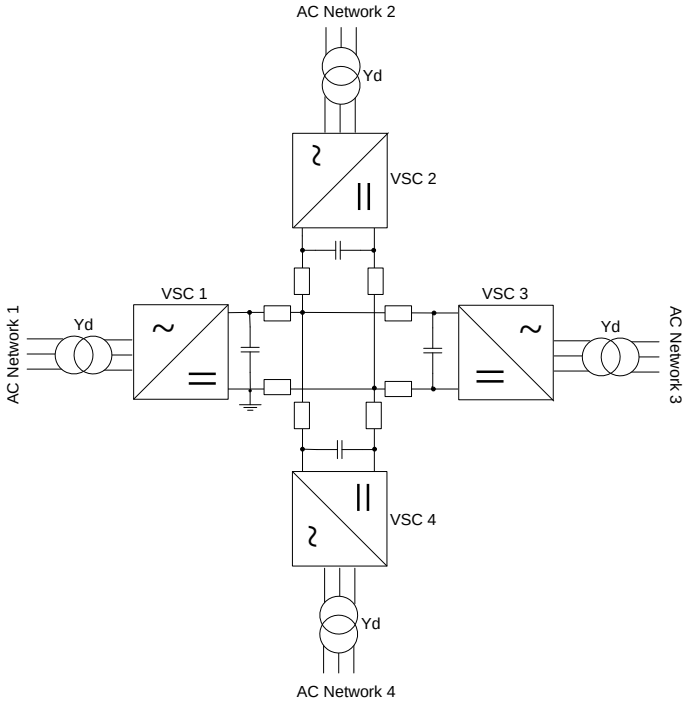


Figure 6.13: Four-terminal HVDC monopolar network with metallic return

On the AC side, the grid connections to the respective stations are kept the same. The converter is connected to the system with a star-grounded delta transformer, used to isolate the primary from the secondary and transform the voltage level from 380 kV to 150 kV needed for the converter rectification to work properly.

The AC filter size though needs to be adjusted to the new power rating of the converter. As previously discussed, the AC filter capacitors usually need to compensate for 10 to 20% of the station reactive power. Therefore, based on (5.1), the phase filter size is recalculated as follows:

$$0.2 \cdot Q_{phase} = \omega C V_{f,phase-rms}^2 \Rightarrow C = \frac{0.2 \cdot Q_{phase}}{\omega V_{f,phase-rms}^2} \Rightarrow C = \frac{0.2 \cdot (0.6e9/3)}{314 \cdot (220e3)^2} = 2.63uF \quad (6.1)$$

As the system parameters remain the same, the system reaction to a positive pole-to-ground can be safely considered equivalent to the response of the respective bipolar configuration with metallic return and thus there is no reason to investigate it in more detail.

It was seen in the bipolar configuration that a positive pole-to-ground DC fault did not influence the negative pole converters in any case, to an extent that a fault signal would be generated. Moreover, the negative pole converters operate independently from the positive pole VSCs under any circumstances. Therefore, the previous analysis, regarding the positive pole VSCs in the bipolar topology with metallic return, is considered adequate to understand

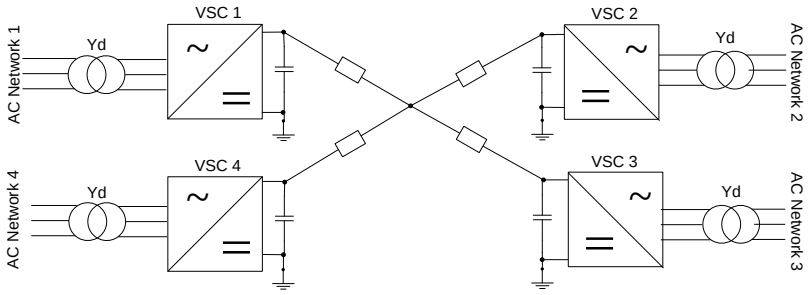


Figure 6.14: Four-terminal HVDC monopolar network with ground return

the monopolar system response and the same conclusions are applicable in both cases. The only difference between the bipolar and the monopolar topology with metallic return, is the inability of the latter to transfer half the station power capability in case of a pole-to-ground fault.

However, although the cost for the realization of such a topology is lower than the respective cost for the bipolar, due to the need of less DC cabling, less DC link capacitors and more importantly half the number of AC transformers and VSCs, there is no longer the redundancy that the negative pole converters offered. In case of a pole fault in the bipolar configuration there was always the possibility to transfer half of the rated power. This possibility does not exist in case of a monopolar configuration.

6.4 Asymmetric Monopole with Ground Return

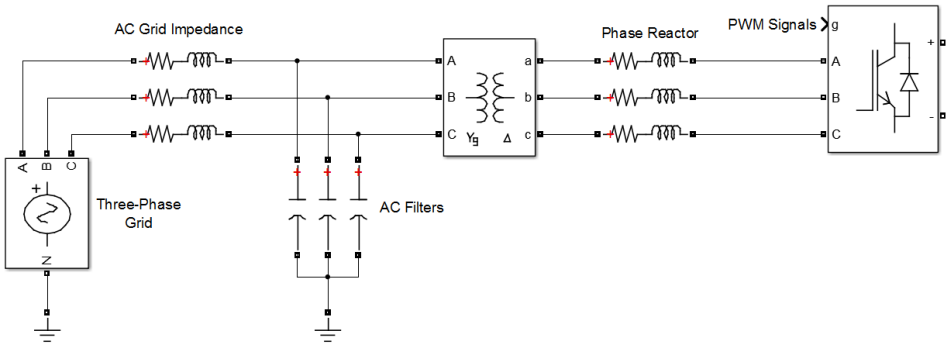
A four-terminal HVDC network with asymmetric monopole configuration with ground return is presented in Figure 6.14.

As mentioned in the previous section, this configuration is considered analogous to the bipolar configuration with ground return. The only system parameter that changes is the station power rating, which is halved (600 MVA) and the AC filter size (2.63 uF), which is also half of the one used in bipolar configuration.

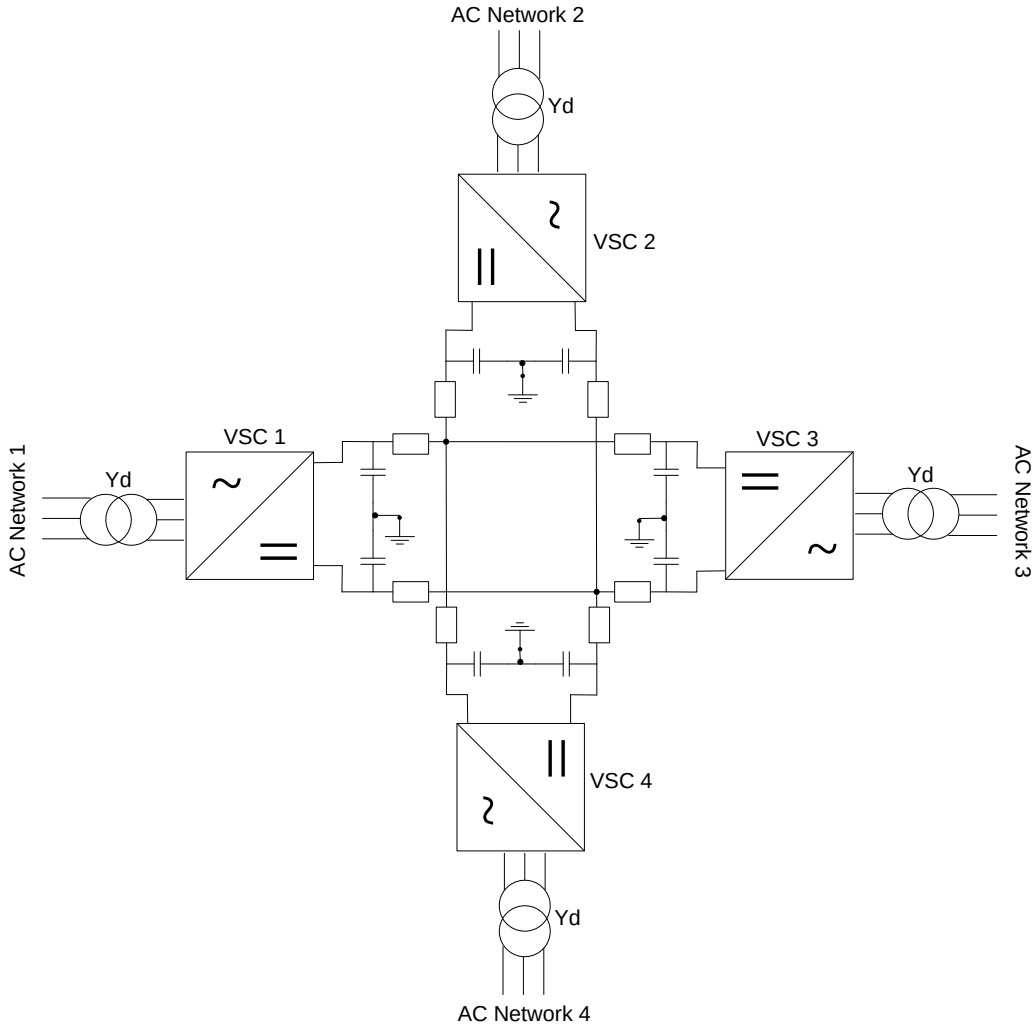
Consequently, the system response to a pole-to-ground fault can be considered the same as in the bipolar configuration, if only the positive-pole VSCs are considered and, as such, no further investigation is performed. In the bipolar topology, the negative pole VSCs are independent of the positive pole converters. Therefore, the conclusions drawn for the positive pole of the bipolar topology with ground return are applicable in this case as well, only without the half power transfer capability of the system in case of a pole-to-ground fault.

6.5 Symmetric Monopole

The symmetric monopolar configuration is different from the topologies already studied in the previous sections and therefore a complete system study is carried out. The topology is shown in Figure 6.15 along with the AC side scheme.



(a) Symmetric monopole station



(b) Four-terminal HVDC symmetric monopolar network

Figure 6.15: Symmetric monopole configuration

6.5.1 System Parameters

The power and the rms voltage level of the AC grids that are connected to the VSC stations remain the same as for the bipolar configuration. However, in order to keep an analogy in the study, each converter is chosen to have a rating of 600 MVA and the DC voltage level is chosen to be 320 kV.

In the symmetrical monopole configuration, this is translated into pole-to-pole voltage of 320 kV. If two capacitors are used on the DC side with a grounding in the middle, each of them takes up half of the total DC voltage, namely 160 kV.

A transformer is used on the AC side, to adjust the converter voltage level. This transformer can either be placed before or after the AC grid filters. For this case study, it is preferred to place it closer to the converter, to prevent any circulating current coming from the grounding of the filters to be fed to the converter. Moreover a grounded star-delta configuration (Yg-d) is used for the transformer. The secondary winding of the transformer is not grounded, in order to avoid circulation of fault currents and also block any zero-sequence components.

To ensure proper operation of the rectifier and to obtain undistorted current waveforms, the modulation index of the SVPWM (Space-Vector Pulse Width Modulation) is kept below 1.15. Therefore, an AC voltage level of 150 kV rms is chosen, as a 380 kV/150 kV transformer is a typical converter size for high voltage applications and is commercially available [88]. The system specifications are summarized in Table 6.4.

Based on the parameters provided, the AC filters, the smoothing reactor and the DC capacitors are selected. As already mentioned for the bipolar topology, a typical AC filter size can provided reactive power equal to 20% of the station rated power. The phase capacitor filter size is the same as calculated in (6.1), i.e. 2.63 uF. The phase reactor is also selected to add up to a total reactance of 0.15 pu, taking also into consideration the transformer leakage inductance. If the transformer equivalent impedance is 0.0005+0.05j pu, the phase reactor is designed to be 0.001+0.1j pu.

Moreover, based on its time constant, τ, the DC capacitor value is selected. A time constant between 5 and 10 ms is considered acceptable. In order to satisfy this criterion a

Table 6.4: Network Parameters

Models	Rated Power (GVA)	Impedance (pu)	Rated Voltage (kV)
AC Network 1	10	0.1+0.001j	380
AC Network 2	10	0.1+0.001j	380
AC Network 3	10	0.1+0.001j	380
AC Network 4	10	0.1+0.001j	380
VSC	0.6	-	AC Side: 150 DC Side: 320
Transformer	0.6	0.1+0.001j	Primary: 380 Secondary: 150

capacitor of 75uF was chosen. The estimated time constant is:

$$\tau = \frac{0.5 C_{dc} V_{dc}^2}{S_{VSC}} = \frac{0.5 \cdot (75e-6) \cdot (320e3)^2}{0.6e9} = 6.4ms$$

In the symmetric monopole configuration, there are two ways DC link capacitors can be connected. There is either one capacitor, or two capacitors of double capacitance, which are grounded in the middle.

The second configuration is more common in literature and research. Its main advantage is the existence of a ground point on the DC grid. This creates in fact two poles on the DC side, as one cable lies on a potential of $+V_{dc}/2$, while the return cable has a nominal potential of $-V_{dc}/2$. In this way the cable voltage ratings are lower. Moreover, a firm ground point prevents the DC voltage from floating. If the voltage floats, there is always the danger of an overvoltage occurrence on the converter IGBTs, as only the peak-to-peak DC voltage is controlled, while its absolute value remains uncontrolled.

However, the existence of a ground point on the DC side, results in a high peak current in case of a fault, due to the discharge of one DC link capacitor. During the fault, as long as the control of the VSCs is not lost, one capacitor is getting overcharged in order to compensate for the voltage drop. For this reason, both capacitors need to be rated for the full DC link voltage, for redundancy purposes.

Additionally, there are several types of grounding that can be used for this configuration. The middle point can either be grounded through a high impedance grounding or a low impedance one [89]. A low impedance grounding can be either resistive, inductive or solid, while the high impedance grounding uses an additional capacitor.

The different grounding methods have an impact on the fault current, as well as on the DC link voltage distribution among the two legs of capacitors. In the present, study the effect of different grounding schemes is not included and the worst case of the aforementioned ones, i.e. the solid grounding, is used.

In case a DC ground exists at the middle point of the DC link, the cables used in this topology need to be rated for a nominal current of $I_{n,DC} = P_{DC}/V_{n,DC} = 600MW/320kV = 1875A$, and a nominal voltage of $\pm 160kV$. Based on these specifications, submarine cables are chosen that have a conductor area of 2200 mm^2 and an ampacity of 2062 A, thus leaving a 10% safety margin [26].

The cable used can be the same as the one chosen for the bipolar topology, however, its isolation level can be lower, due to the lower voltage level, at which the cable is operated. The DC grid parameters used in the simulations are given in Table 6.5.

6.5.2 Control performance in normal operation

In order to check the control performance of the four-terminal system the order of events presented in Table 5.4 is simulated.

The active and reactive power of VSC1, on the secondary of the AC transformer and on the grid side are presented in Figure 6.16. The power measurements on the grid side have a smaller peak-to-peak ripple due to the smoothing effect of the AC filters. However, the

Table 6.5: DC grid parameters

DC grid parameters	Unit	Value
VSC station rated power (S_{VSC})	MVA	600
DC grid voltage level (V_{dc})	kV	$\pm$160
Rated current (+10%) (I_{dc})	A	2062
Conductor area (A)	mm^2	2200
Resistance (R)	Ω/km	0.0195
Inductance (L)	mH/km	0.2
Capacitance (C)	nF/km	220

reactive power is no longer zero on the grid side, as the AC filters contribute a 0.2 reactive power compensation. The respective waveforms for the remaining VSCs are presented in Appendix A.6.

Considering the active power control of the system, Figure 6.16 shows that the reference value is reached within 0.1 ms. The settling time is dependent on the amplitude of the active power reference change. In Figure 6.16(a), VSC1 needs to perform a step of 1 pu at 0.8 s. It can be seen that there is a higher overshoot and the active power settling time is longer, due to the fact that the DC voltage is controlled to 1 pu. The time is dependent not only on the controllers performance, but also on the current slope limitation of the IGBTs.

Regarding the reactive power exchanged with the AC grid, the AC grid power factor is controlled at unit at all times. However, it is observed that when a station absorbs power from the HVDC network, the reactive power peak-to-peak ripple increases.

In Figure 6.17 the actual AC converter current in (dq) is represented against the reference current at each moment. It can be deducted, that the control is fast and precise, always following the current reference signal.

Figure 6.18 shows the total DC link voltage at each station. Depending on the active power reference step performed, there is either an overshoot or an undershoot of 10 to 12%. However, the transient only lasts for less than 1 ms. When a power exchange is in place, the DC link voltage level slightly differs between the different stations. More specifically, when VSC3 is controlled to absorb 0.8 pu active power at 0.5 s, the respective DC link voltage is slightly (0.01 pu) lower than the one of VSC1,which is the station in charge of DC voltage level control. The opposite situation is observed when active power is fed to the grid from a station. This difference in voltage level can be attributed to the voltage drop in the lines. More specifically, if at a specific moment only 0.8 pu power is transferred from station 1 to station 4, a total current of 0.8 pu needs to travel a total distance of 200 km from the sending station. The unit-length resistance of the lines is 0.0195 Ω/km, thus resulting in a total 3.9 Ω. Consequently, the voltage drop on the line is calculated to be approximately 1.8% of the DC link nominal voltage.

It is also important to note that the DC voltage at the DC link needs to remain balanced, in order not to have any big difference in the power transmitted at each pole, which could result in overcharging of one capacitor over the other and possible failure.

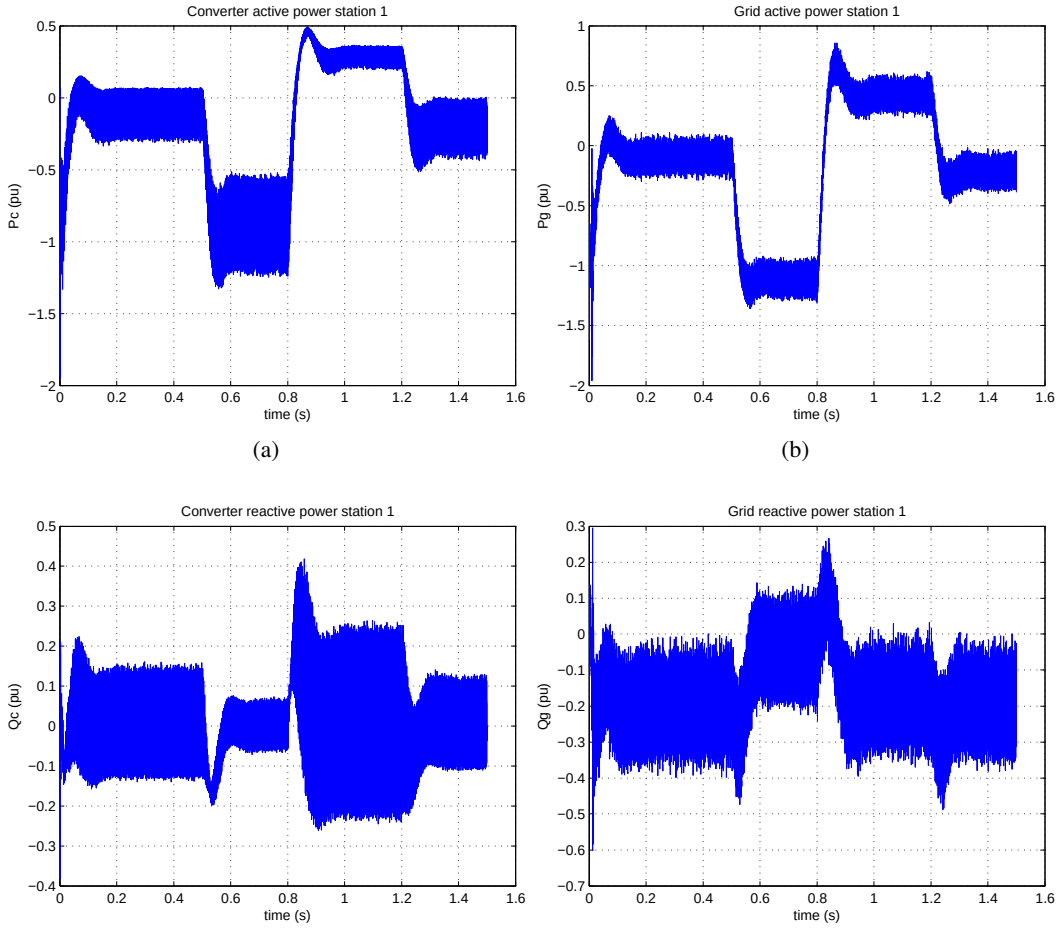


Figure 6.16: VSC1 active and reactive power in normal operation for symmetric monopole configuration

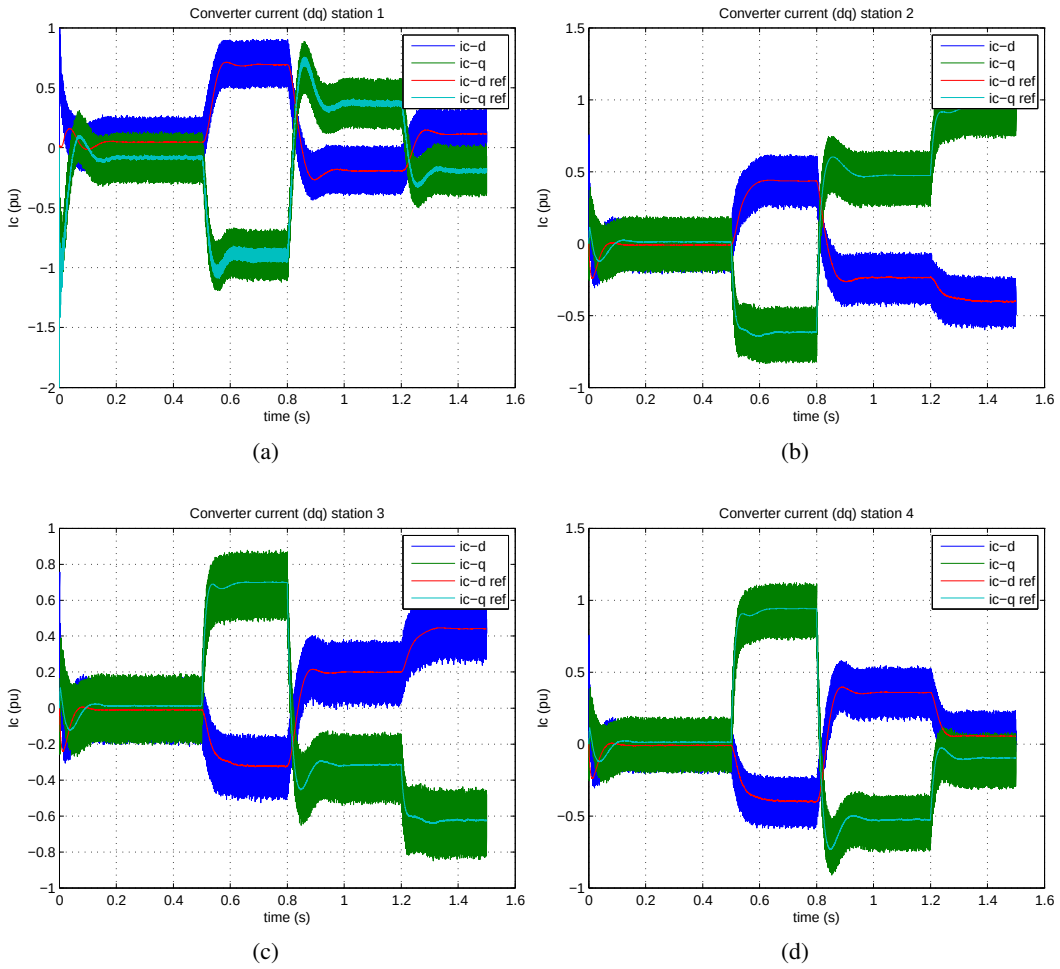


Figure 6.17: VSCs AC current (dq) in normal operation for symmetric monopole configuration

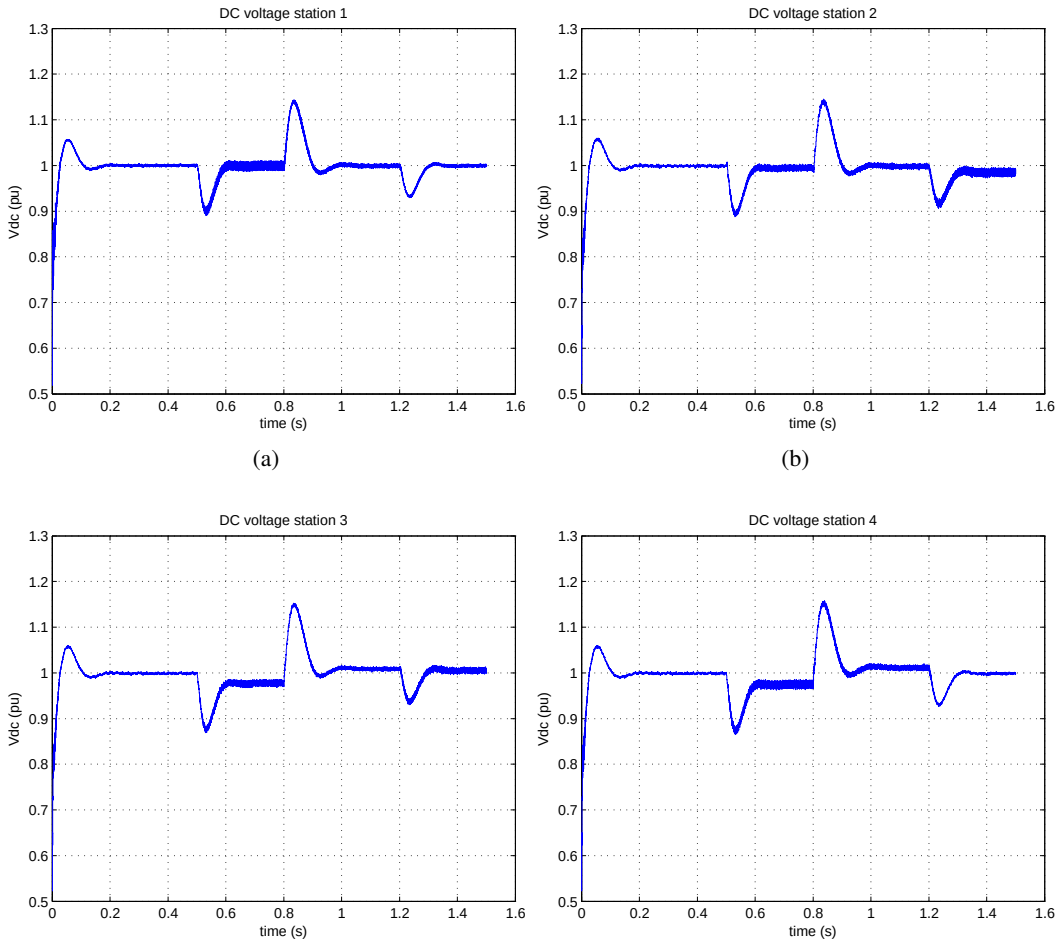


Figure 6.18: VSCs DC voltage in normal operation for symmetric monopole configuration

6.5.3 Symmetric Monopole positive pole-to-ground fault

After checking the controllers of the simulated system, a pole-to-ground fault is simulated. In order to investigate the way the fault currents are developed, no additional measures are taken. The fault is considered to be permanent and the stations are not disconnected at any point.

During the simulation, only the IGBTs over-current protection is working in order to block their operation as soon as the AC current of the converter exceeds the 2 pu threshold. The order of events in the simulation remains the same as presented in Table 5.7. The results are presented from Figure 6.19 until Figure 6.23.

As soon as a fault is applied, the DC link voltage drops. This can be seen in Figure 6.19. More specifically, the positive pole capacitor voltage begins to drop and finally drops to

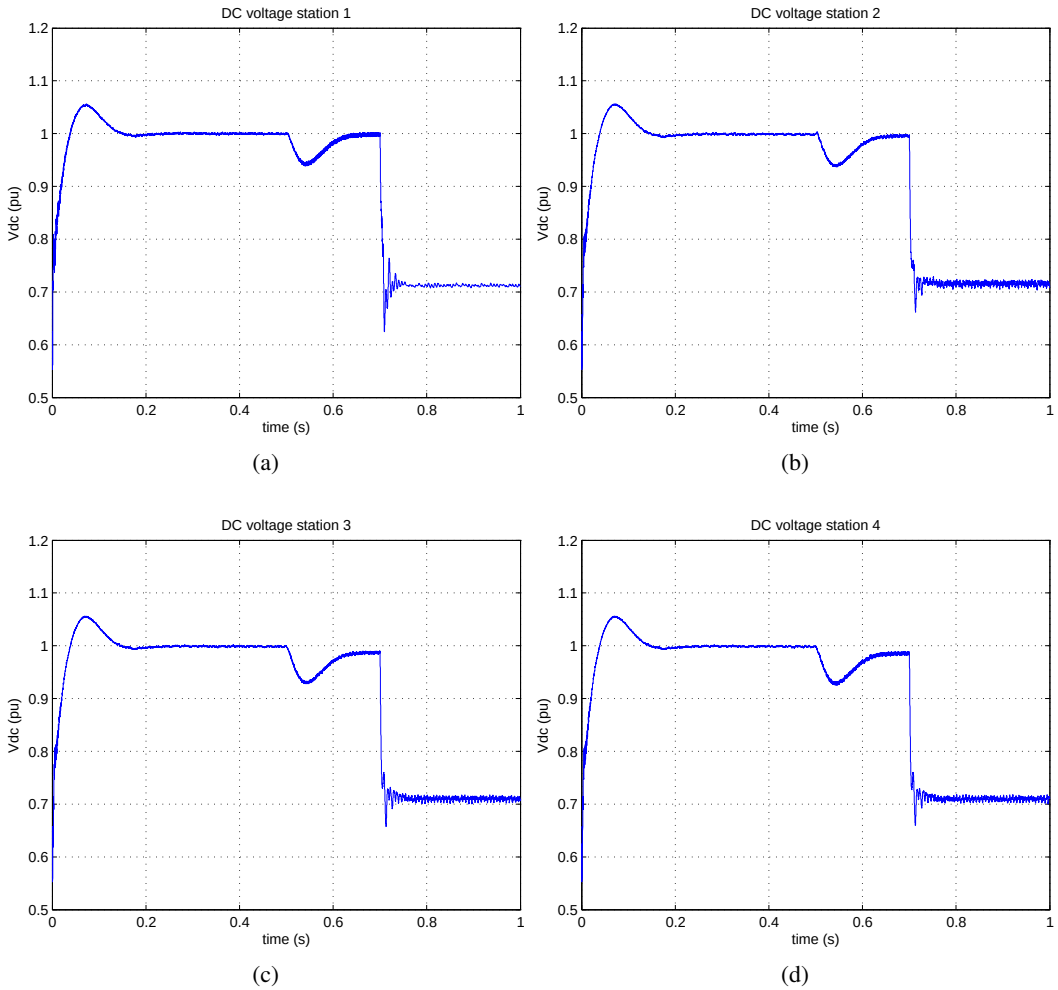


Figure 6.19: VSCs DC voltage for fault case in symmetric monopole configuration

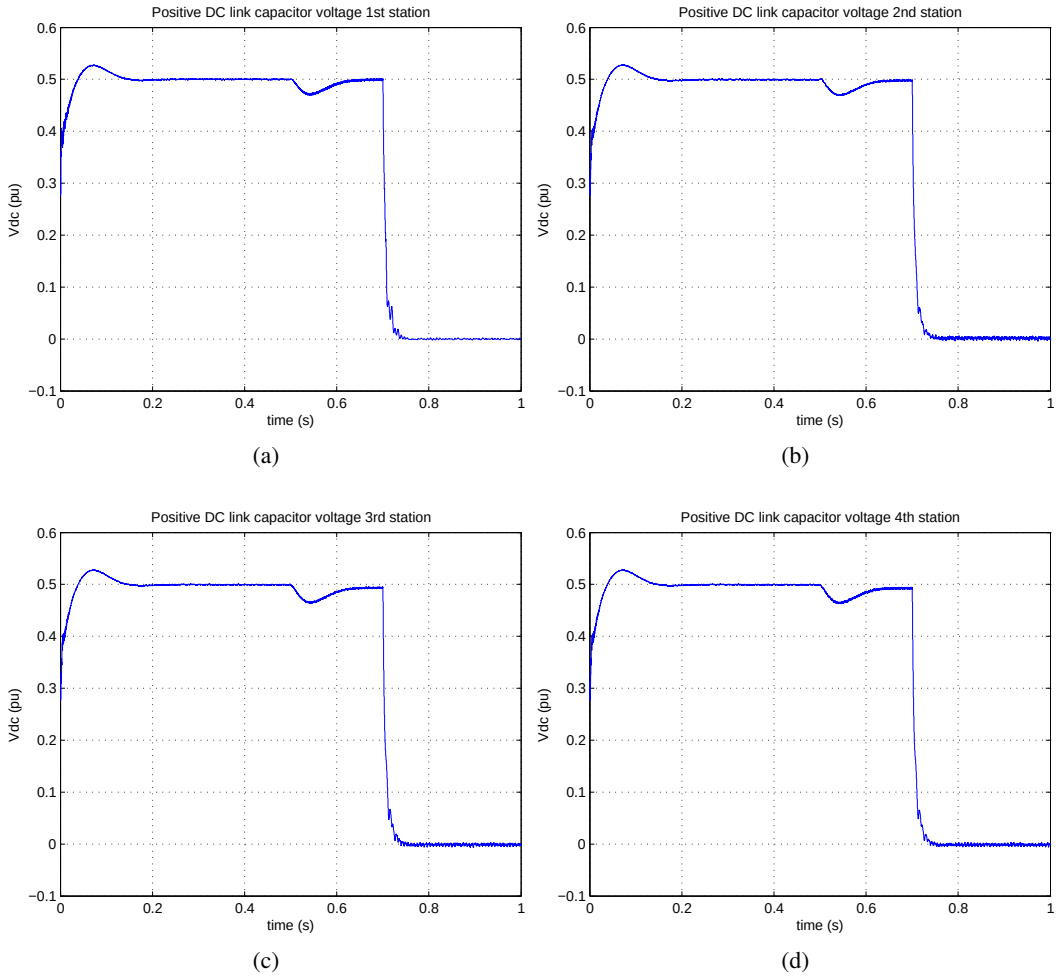


Figure 6.20: DC link positive arm capacitors voltage for fault case in symmetric monopole configuration

zero. At the same time, the negative pole capacitor starts getting overcharged as long as the DC voltage control is working. The positive and negative pole capacitor voltages become more explicit from Figure 6.20 to Figure 6.21.

The only converter directly influenced by the fault is VSC1. A pole-to-ground fault affects the DC link voltage level, for which VSC1 is responsible. When a drop in the voltage is monitored VSC1 reacts by supplying more current to the DC grid, in order to compensate for the voltage drop. However, after a certain time, depending on its power level before the fault occurrence, in this case 6.2 ms, an overcurrent is experienced at the converter and this is forced for its protection to block the IGBTs. At this moment, the DC grid voltage control is lost.

At the same time the rest of the stations continue controlling their power level, as their

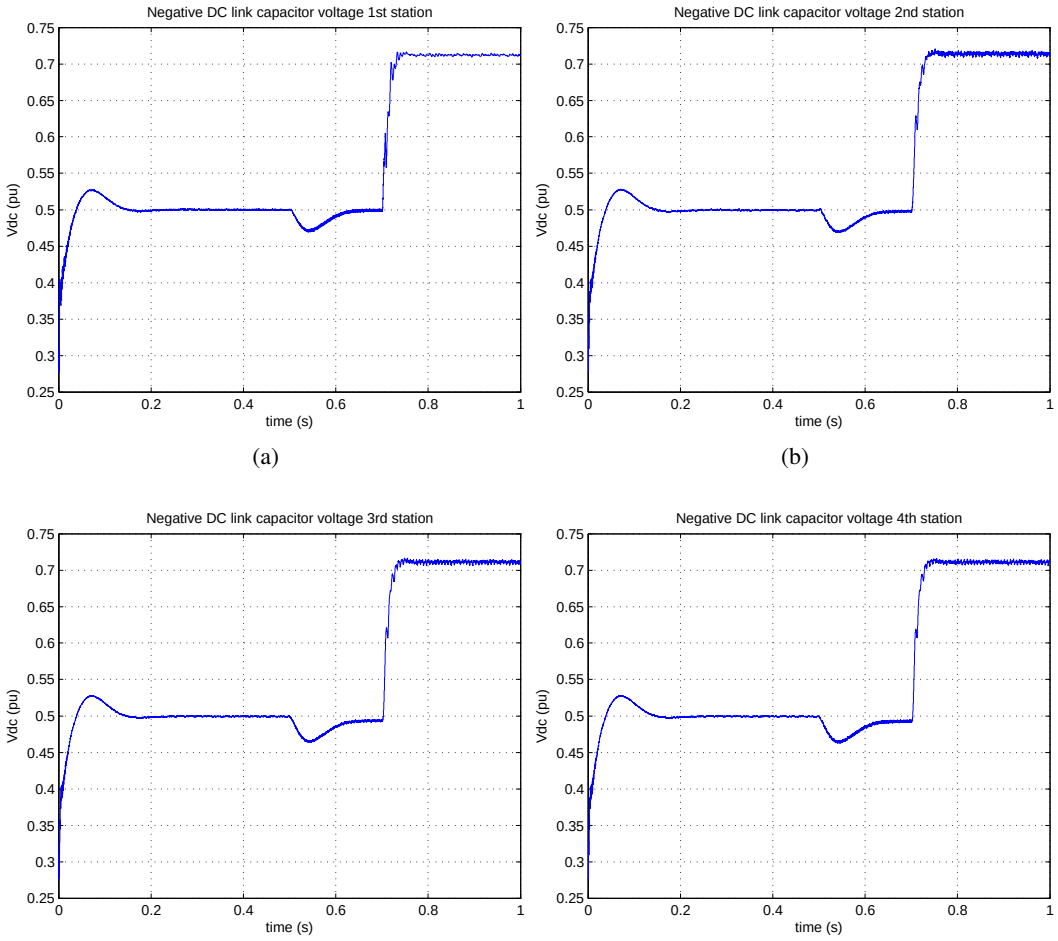


Figure 6.21: DC link negative arm capacitors voltage for fault case in symmetric monopole configuration

operation is not blocked. Due to this fact, the DC link voltage at VSC1 does not further drop. The negative arm capacitor does not get discharged through the non-ideal converter switches, but it remains at the level that it was at the moment VSC1 IGBTs were blocked. In this case this level was 0.71 pu and the modulation index for the system VSCs was 1.07.

It has to be noted, that in case all the converters were blocked, the DC link voltage level would drop until it became equal to the peak value of the line-to-line rms voltage on the AC side of the converter, namely 0.66 pu of the DC link nominal voltage.

At the moment an overcurrent is detected at VSC1, its IGBTs are blocked and as soon as the fault current becomes zero, the AC current of VSC1 becomes zero as well. The rest of the converters are not blocked and they continue exchanging power. However, the power levels are not kept the same as they were before the fault. This can be attributed to the

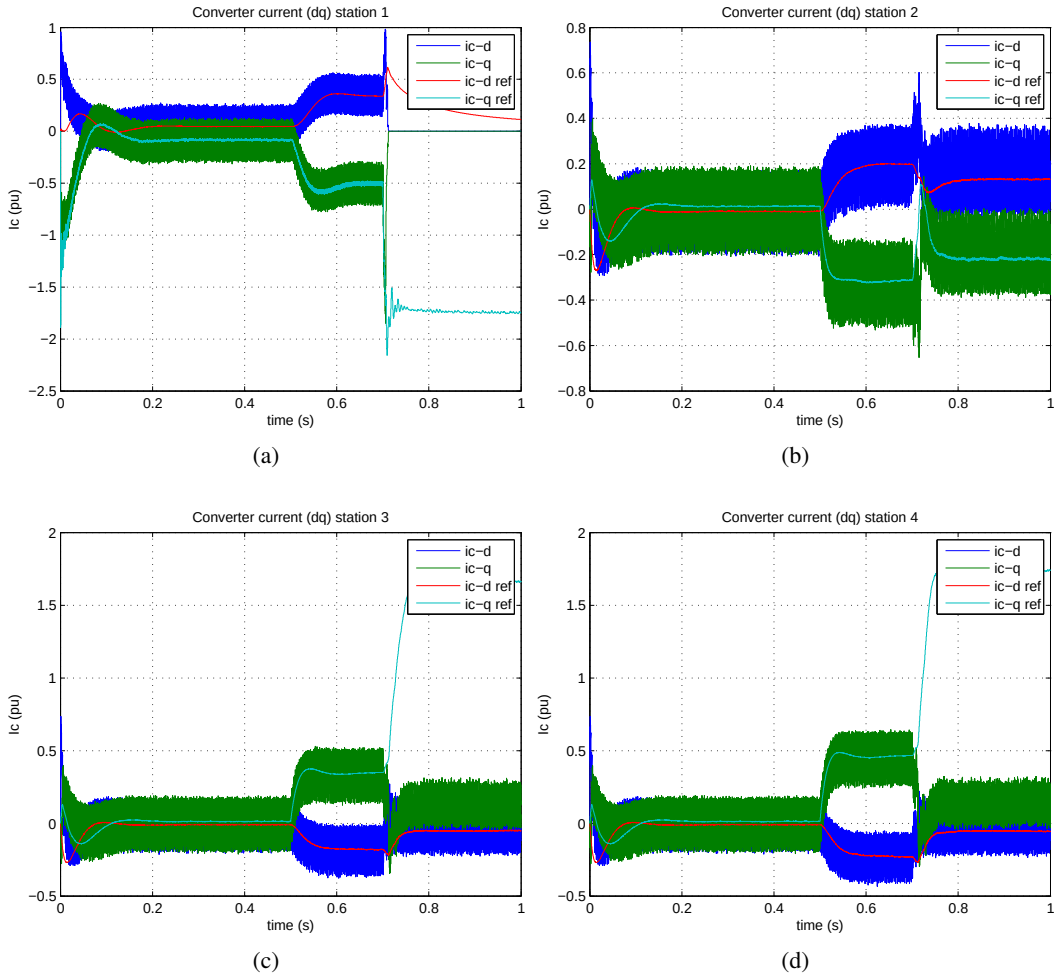


Figure 6.22: VSCs AC current (dq) for fault case in symmetric monopole configuration

change of the DC level at which the power exchange takes place.

The VSC1 DC link voltage is kept constant at 0.71 pu, as there is no available current path to get discharged. The positive arm DC link capacitors got discharged through the fault, and thus, the negative capacitors are directly connected to the output of the VSCs and they are the only ones setting the DC grid voltage level. Consequently, 0.71 pu is the voltage level of the negative arm capacitors, as shown in Figure 6.21.

VSC2 is the only station after the fault that feeds active power to the grid. At the pre-fault state, its power was controlled at -0.3 pu. After the fault, this reference is maintained. However, due to lack of another active power source and the fact that the DC link capacitors cannot get further discharged below 0.71 pu voltage, set by the VSC1 DC link negative arm capacitors, VSC3 and VSC4 are forced to reduce the amount of active power they absorb from the DC grid. More specifically, because of their symmetrical characteristics, the VSC2

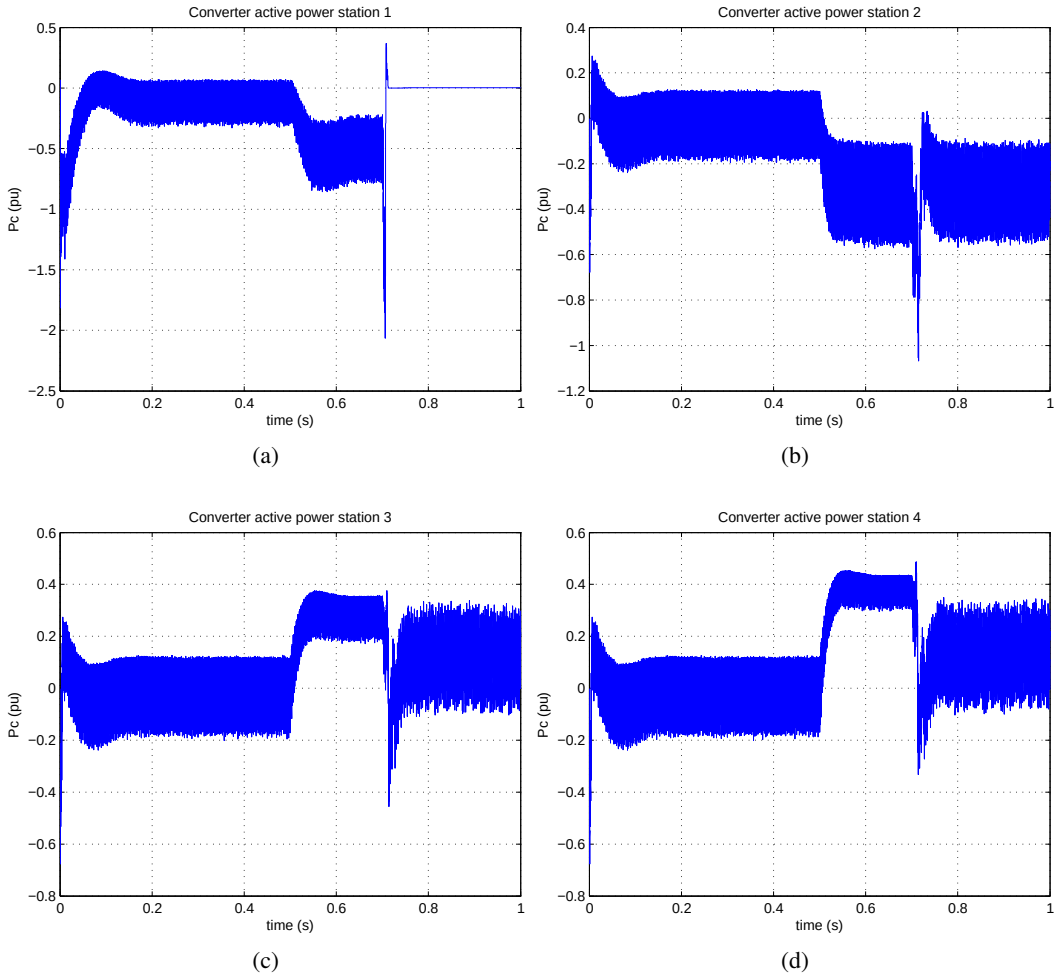


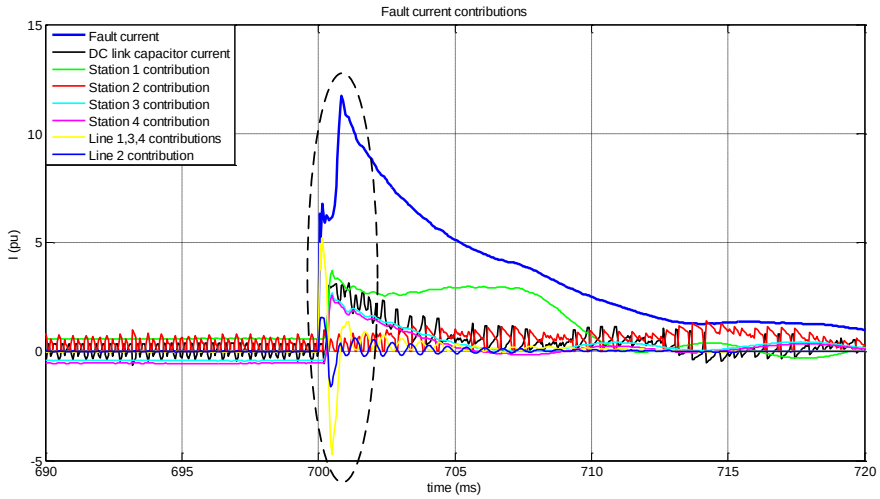
Figure 6.23: VSCs active power for fault case in symmetric monopole configuration

power is divided into two and thus each of them receives 0.15 pu. The data corresponding to the previous analysis can be found in Figure 6.22 and Figure 6.23.

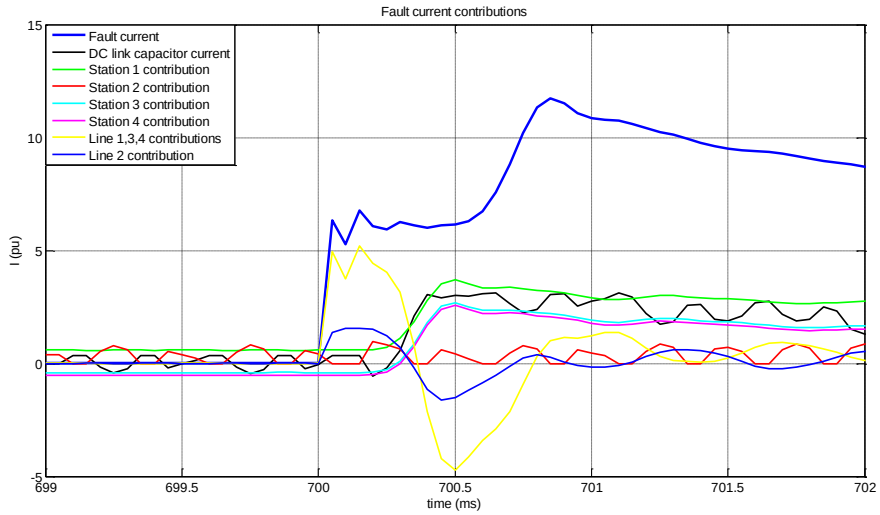
Fault current contributions

The DC currents developing during a fault can be seen in Figure 6.24. The first observation that can be made for this topology, when compared to the others investigated, is that the fault current does not sustain, but returns to zero after approximately 30 to 40 ms after it started. This can be mainly attributed to the fact that the AC grids are isolated via the transformers. This is also the reason why only the converter responsible for DC voltage control experiences an overcurrent.

From Figure 6.24(a), it can be seen that station 1 is the only one whose current is kept high for longer time, trying to control the DC voltage level. At the point it is blocked



(a) Fault current contributions



(b) Zoom-in view of circled region

Figure 6.24: Fault currents symmetric monopole

(6.5 ms), the DC link voltage is at 0.71 pu, the positive pole capacitor gets completely discharged and the fault current drops to zero.

Within 5 ms, the DC link positive pole capacitors at the other stations have got discharged and the rest of the fault currents are a result of the oscillation line energy storage components experience. In close-up shown in Figure 6.24(b), it can be observed that the initial fault current peak comes from the discharge of the HVDC lines. It is only after 0.3

ms that the DC link capacitors start getting discharged via the fault resistance, experiencing a high current derivative.

Because of the fact that the VSC stations do not in general experience overcurrents and only the DC voltage controlling stations do, after a comparatively long time, there is no need to use limiting reactors to further delay the occurence of the overcurrent. However, even if this is decided, the limiting reactors only need to be placed at the DC output of the station responsible for voltage control, thus saving in cost compared to the other topologies. In the remaining of the study, simulations are carried out on a system without limiting reactors.

Selective fault detection methods

In order to decide on which fault detection method suits this topology the best, simulations were run using full semiconductor breakers.

The detection method based on the current derivative was simulated first. As seen in Figure 6.24 as soon as the fault is applied, the positive DC link capacitors start getting discharged. Due to the point of fault occurrence in the DC grid (49 km from VSC2) all the stations realize almost at the same time the change. Consequently, the initial fault currents at the lines of the stations only come from the DC link capacitors, which are discharged in the same manner. The current derivative is almost identical for all the stations and no clear threshold can be decided.

As a result, the focus is turned to the current direction selective method. In the following sections, simulations results are provided for the use of different DC breaker technologies.

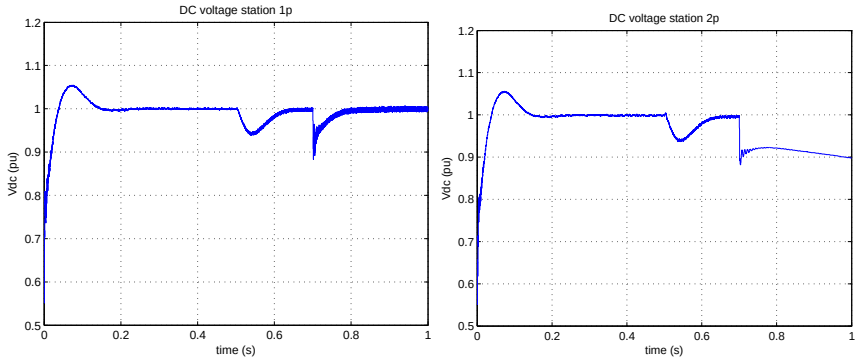
Full Semiconductor DC Breaker (t_{open} = 1 ms)

In this section the symmetric monopole topology is simulated along with DC breaker models, in order to investigate the possible isolation of the fault in time and the restoration of the remaining system operation. From the simulations, it was found that the fault was detected within 1.1 ms from its occurence, based on the current direction selective method. The DC link voltage at each station is presented in Figure 6.25. In Figure 6.26, the voltage of each VSC1 DC link arm is given.

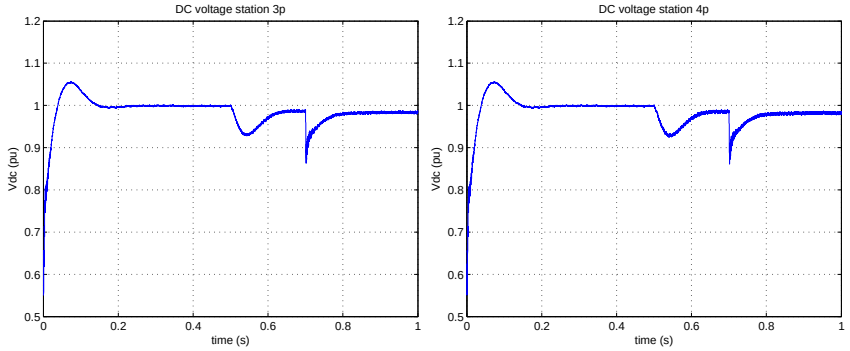
As soon as the fault is detected and isolated, VSC2 is disconnected from the rest of the network and its voltage starts decreasing. For the rest of the stations, as long as the VSC1 responsible for voltage control is still connected, the voltage is restored at its nominal level.

However, a problem can be identified after a closer look at the individual voltage levels of the DC link capacitors. The positive pole capacitor, which got discharged during the fault, in the post-fault stage only increases so that the total DC link voltage reaches back its nominal value. On the other hand, the negative pole capacitor, which got overcharged during the fault to compensate for the voltage drop of the positive pole, now remains unchanged.

This imbalance between the capacitors of the DC link can be crucial for the system performance, as the negative pole capacitor experiences higher stresses. The balance could be restored is a complete de-energization of the DC link and a new start-up of the system. Another idea would be to momentarily remove the ground connection (some milliseconds), in order for the DC link arm voltages to become balanced via control. However, it is not

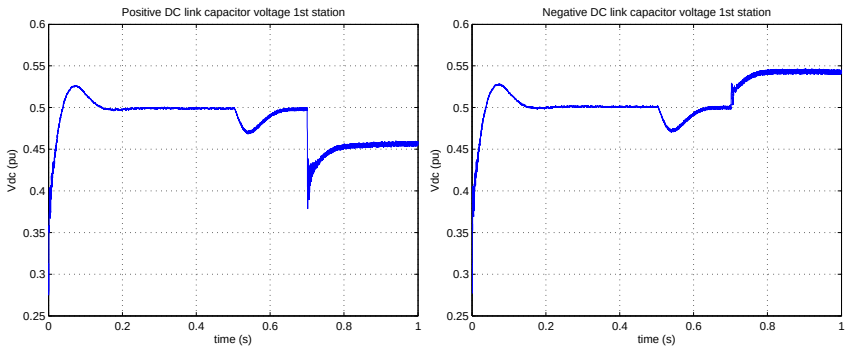


(a) (b)



(c) (d)

Figure 6.25: DC voltage for fault case in symmetric monopole with use of current direction fault detection method and full semiconductor DC breakers



(a) Positive pole capacitor (b) Negative pole capacitor

Figure 6.26: VSC1 DC link voltage for fault case in symmetric monopole with use of current direction fault detection method and full semiconductor DC breakers

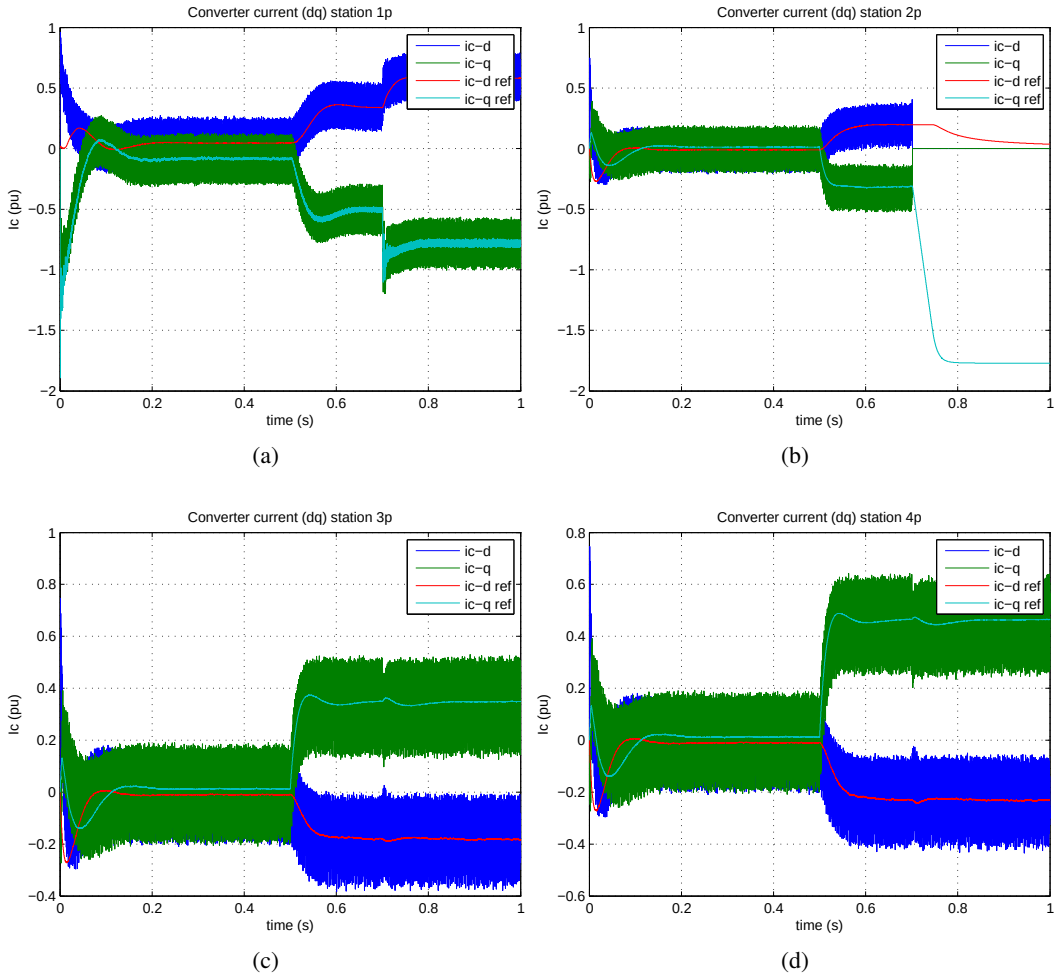


Figure 6.27: VSCs AC current (dq) for fault case in symmetric monopole with use of current direction fault detection method and full semiconductor DC breakers

certain if this concept can be implemented in reality and further research is needed. In the present study, this voltage unbalance exists in all the DC fault cases studied.

As long as the converter AC currents are concerned, there is an increase in the current of VSC1, since after the isolation of VSC2, it needs to supply more power to the grid to cover the power demands of stations 3 and 4. Consequently, an increase in the active power is also observed in Figure 6.28.

The fault isolation can be considered in this case successful, as the converters remain safe and the system gets restored after the isolation of the faulty line. However, the DC link voltage unbalance implication needs to be further evaluated when designing such a system.

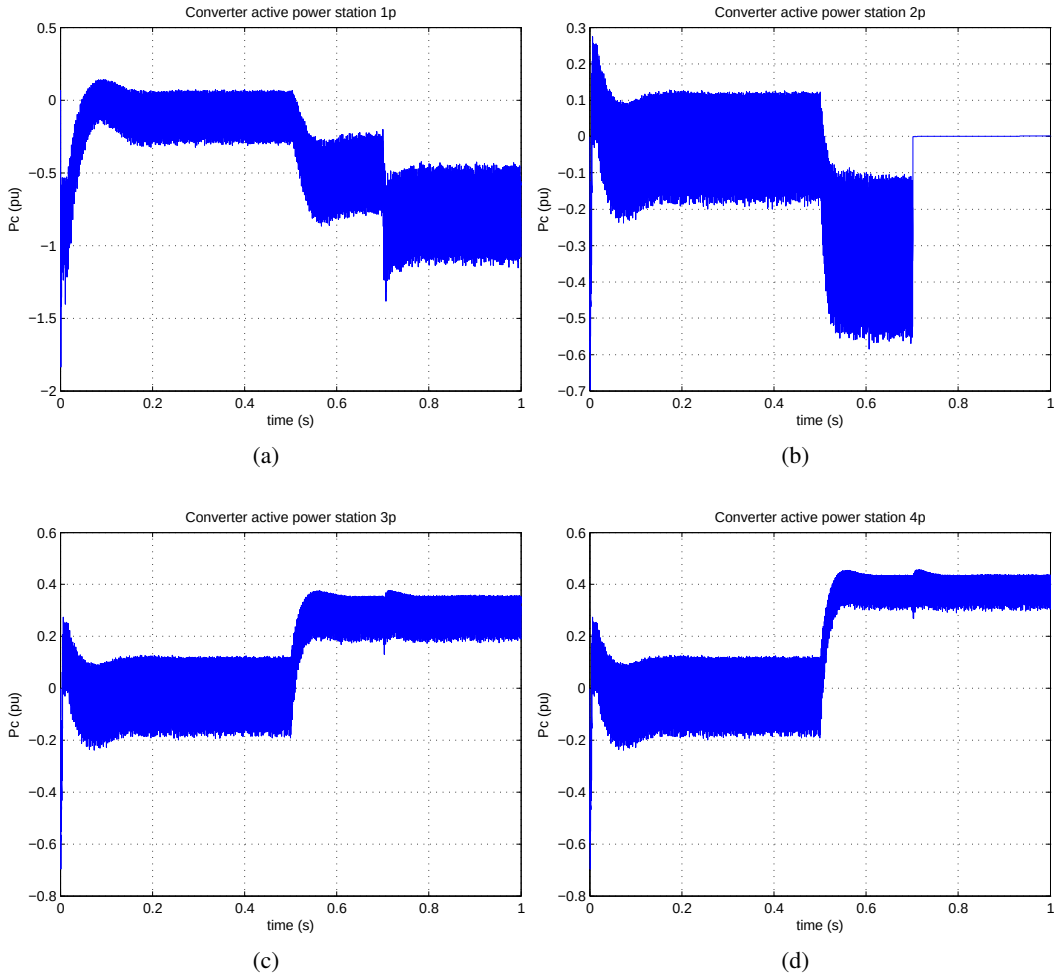


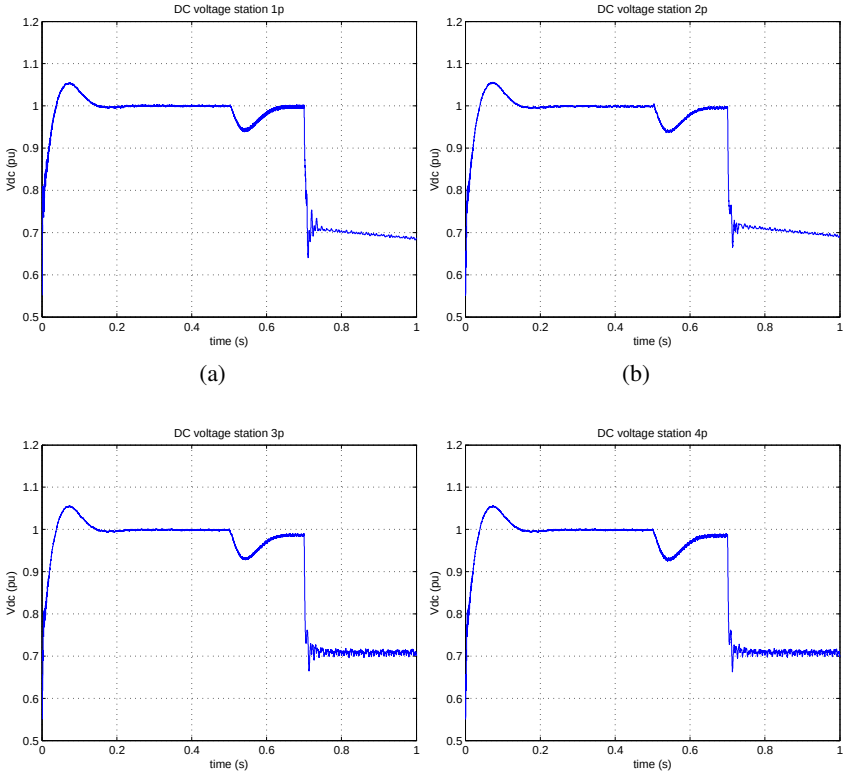
Figure 6.28: VSCs active power for fault case in symmetric monopole with use of current direction fault detection method and full semiconductor DC breakers

DC Breaker Hybrid I (t_{open} = 2 ms)

Regarding the use of a slower breaker with total interruption time of 2 ms, it was observed that the fault is successfully isolated at a total time of 3.1 ms, before VSC1 experiences an overcurrent. The response of the system thus remains the same as in the previous case and the same conclusions can be drawn.

Hybrid II (t_{open} = 30 ms) and Resonance DC Breakers (t_{open} = 60 ms)

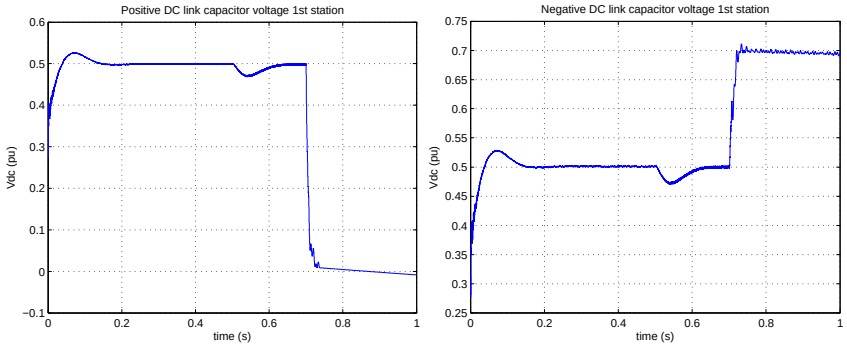
The Hybrid II breaker has a total interruption time higher than the time needed for VSC1 to experience an overcurrent and block its operation. The DC voltage, the AC currents and the active power at each station are presented in Figure 6.29 up to Figure 6.32.



(a) (b)

(c) (d)

Figure 6.29: VSCs DC voltage for fault case in symmetric monopole with use of current direction fault detection method and hybrid II DC breakers



(a) Positive pole capacitor (b) Negative pole capacitor

Figure 6.30: VSC1 DC link voltage for fault case in symmetric monopole with use of current direction fault detection method and hybrid II DC breakers

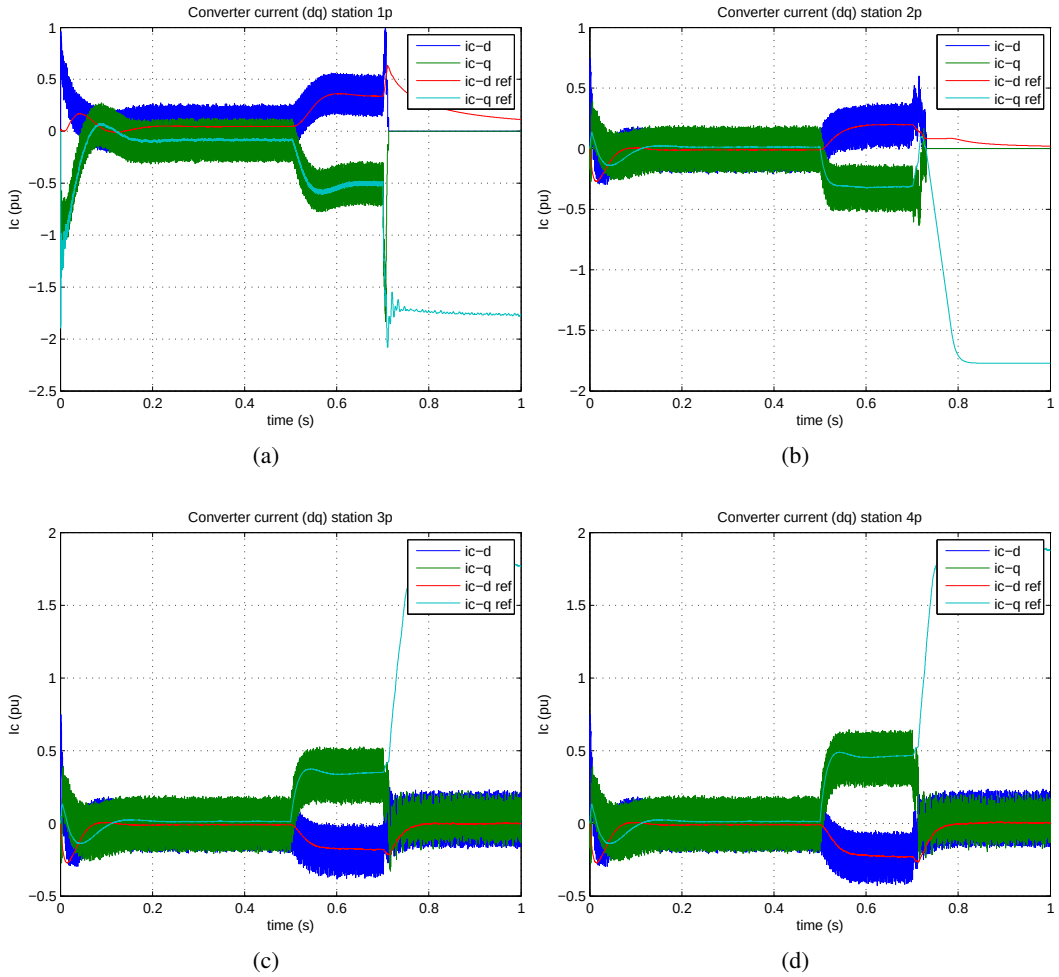


Figure 6.31: VSCs AC current (dq) for fault case in symmetric monopole with use of current direction fault detection method and hybrid II DC breakers

The DC voltage develops as if the fault was permanent, due to the high total interruption time of the DC breakers. The reason is that the system is not able to be restored and, therefore, the DC voltage level remains constant at the level reached right before VSC1 was blocked. The VSC1 DC link negative arm remains connected to the rest of the grid, through the middle-point ground, thus keeping the voltage level constant at 0.71 pu. Additionally, the capacitors cannot get discharged, through the diode bridge, as there is no available current path; diodes are reversely connected.

In the post-fault state, the DC link positive arm is totally discharged through the fault and the negative arms determine the DC grid voltage level. Moreover, the DC grid, after the fault, consists of only two interconnected stations that have not been blocked and can, thus, exchange power (VSC3 and VSC4), and the DC link negative arms of the two blocked

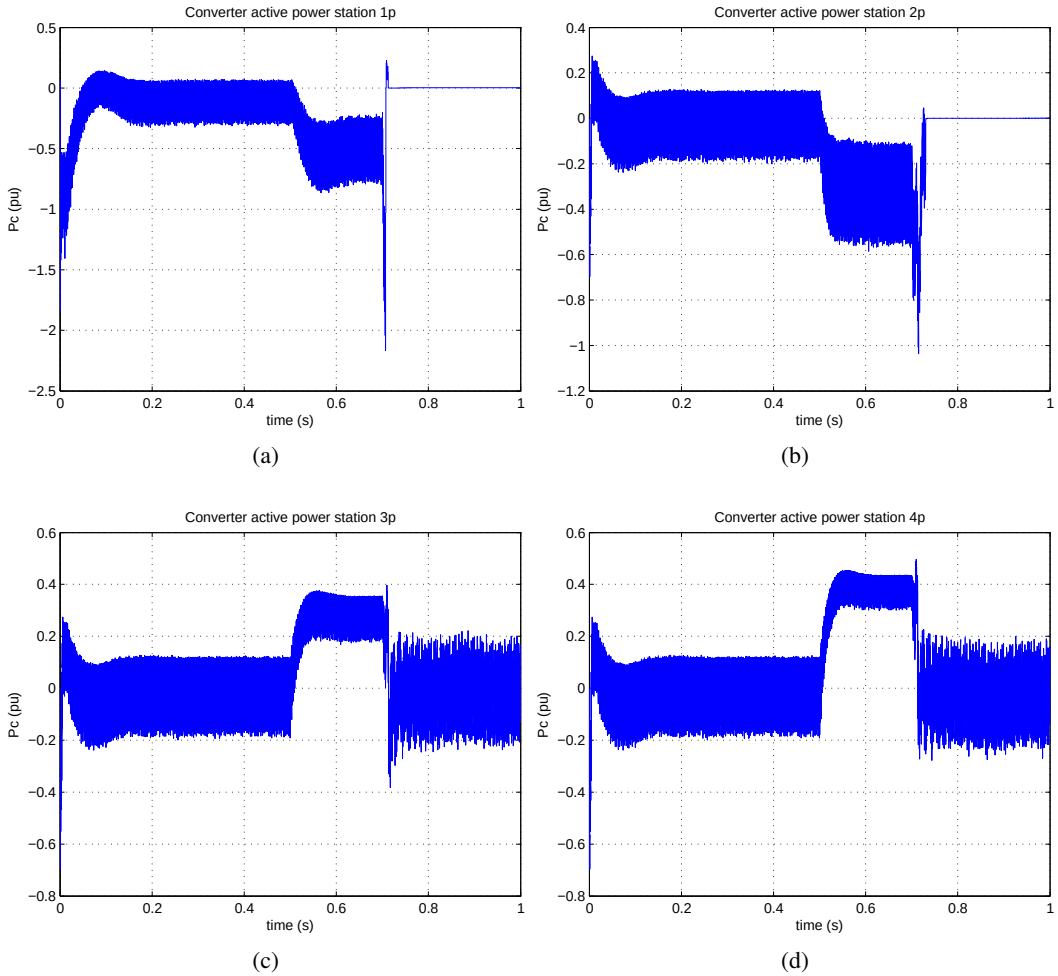


Figure 6.32: VSCs active power for fault case in symmetric monopole with use of current direction fault detection method and hybrid II DC breakers

VSCs (VSC1 and VSC2). Consequently, the DC voltage level cannot drop below 0.71 pu, as determined by the DC link capacitors of stations 1 and 2.

VSC3 and VSC4 maintain the power references they had before the fault occurrence. The two converters were controlled to absorb power from the grid in the pre-fault state. Therefore, they instantly absorb power from the DC lines to keep their power steady, however, as there is no other power source in the grid, after the DC breakers opening, and the negative arm capacitors cannot get discharged, their power and the AC currents get to zero. The converters are not able to exchange power unless their power references are changed.

Similar conclusions also apply for the resonant breakers, which are the slowest ones investigated in this thesis. Consequently, they cannot clear the fault in time, and thus, they are not further discussed.

6.5.4 Partial Conclusions

The symmetric monopole appears to be the best topology regarding the fault currents. The AC side of the converters is not affected, except for the ones controlling the voltage level. Additionally, as soon as the DC lines and DC link capacitors get discharged the fault current becomes zero.

Because of the grounding of the DC link mid-point, one half of the link gets connected in series with the fault and is overcharged during the fault period, partially compensating for the voltage drop in the other half of the DC link. However, this unbalance in the link cannot be restored even if the fault is quickly isolated. The only way the system can return in the pre-fault condition is by de-energizing it and starting it up normally.

The DC link balance during a fault can only be kept by using a high impedance grounding which does not allow the fault current through it. However, this possibility and its implications are out of the scope of this thesis and not further investigated.

Chapter 7

Conclusions

The need for energy trade and the increasing exploitation of the available global energy sources will require further investments in long-distance power transmission. To meet nowadays technological and financial requirements, HVDC technologies have significantly advanced since the first commercial HVDC link was built in 1954.

The VSC converters utilize fully controllable switches (IGBTs), which are controlled via modulation techniques. However, the use of IGBT valves in the converters consists a disadvantage in case of a DC fault as, even if the switches are blocked, there is still a path for the current via the valves anti-parallel diodes and the converters are prone to damage.

To improve the VSC performance, and limit the fault currents or isolate the fault, there are many proposed concepts. Multi-level converters (MMC) have been recently used, which can provide high AC voltage quality, with little filtering requirements. They either employ half-bridge or full-bridge submodules. Half-bridge submodules cannot handle high DC fault currents and their response does not differ from the one of two-level converters. Therefore, AC breakers and/or DC breakers are required to isolate the fault. On the other hand, full-bridge modules have the capability to suppress the DC fault current and even drive it to zero, by connecting the submodules DC capacitors with opposing DC voltages in series with the fault current. In this way, DC breakers with lower current ratings can be used to isolate the faulty line and no AC breakers opening is required.

Alternatively, the 'Handshaking Method' provides a solution to fast locate and isolate a faulty line, as well as restore a multi-terminal network operation, without the use of expensive DC breakers. This method uses a combination of AC breakers and two fast DC mechanical switches per DC line. Although the control is performed simultaneously at all the VSCs, no communication is needed among them. In this method, the opening and re-closing times of the AC breakers pose the highest time constraints.

On the other hand, in the 'Handshaking Method' faster fault isolation methods are necessary to avoid high converter stresses for long time periods, which can lead to failure. Additionally, although fault currents can be limited when using multi-level converters with full-bridge submodules, DC breakers are, nevertheless, required for the faulty line isolation.

Consequently, this thesis focused on the study of pole-to-ground DC faults in several multi-terminal HVDC grid configurations and the impact of different DC breaker technologies on DC contingencies.

To study the DC grid faults, a two-level VSC station model was designed and simulated using Matlab/Simulink, where the most important VSC station components were dimensioned and focus was given on the design of the control system. Additionally, overcurrent protection was implemented for the IGBT valves, based on their current ratings.

A distributed-parameters line model was chosen over a pi-equivalent model, as it can better simulate the dynamic behavior of DC cable lines during a fault due to its travelling wave characteristics. These characteristics are also important for analysing the DC fault currents propagation in the HVDC network.

To study the effect of DC faults on multi-terminal grids, a four-terminal grid with a radial configuration was selected due to its inability to accommodate the fault isolation, while keeping all the stations connected. Therefore, radial topologies were considered more challenging than meshed topologies for the purpose of this thesis. The following HVDC network operating topologies were investigated: bipole with metallic return, bipole with ground return, asymmetric monopole with metallic return, asymmetric monopole with ground return and symmetric monopole.

Regarding the VSC-HVDC system protection, the four most important DC breaker concepts were compared and simulated; the full semiconductor breaker, the hybrid I breaker, the hybrid II breaker and the resonance breakers. Two DC breaker control strategies were developed to successfully detect the fault and distinguish the faulty line. The first controller was based on the DC current direction in every DC line, whereas the second controller was based on the current derivative at the VSC terminals.

To study the different grid configurations a methodology was developed. First of all, the controllers of the VSCs were tested in normal operation. Secondly, the free response of the fault currents was monitored and the times at which the stations experienced an overcurrent were estimated. In the third step, limiting reactors were inserted, when necessary, to limit the peak fault current and reduce the rate of rise of the fault current, giving the fault detection controllers and the breakers additional time to act, before the VSCs experienced overcurrents. Finally, different interruption times were simulated corresponding to the different DC breaker technologies, to study their impact on the coordination of the grid stations and on the system protection.

Based on the performed theoretical study of DC fault currents and the simulation results, it is possible to assert that DC faults develop in three stages. During the first stage, the DC capacitors and the line energy storage elements get discharged through the fault, contributing the most to the DC fault current. In the second stage, the converter switches get blocked for their protection and the VSC acts as a diode bridge rectifier. Finally, in the third stage, there is a grid forced system response and the network reaches a new steady state operating point, at which the DC fault is only fed by the interconnected AC grids through the VSC stations.

The results from the dynamic simulations of DC faults have shown that in the bipolar configuration with metallic return, the grounding point of the DC side was the most crucial issue regarding the response of a network during a DC fault. The grounding point significantly influences the stations DC link voltage level and the contributions of the VSC currents to the DC fault during the steady-state. It also affects the time required for each VSC to experience an overcurrent and this needs to be considered in the design of fault

detection selective methods.

The current direction fault detection method was selected to control the DC breakers in this grid configuration. The current derivative selective method cannot be used in the bipolar topology with metallic return as the VSC with a direct neutral grounding experiences high current derivatives, as soon as a fault happens, irrespective of the fault point position.

Regarding the fault location, i.e. the distance between the fault and the VSC position, from the comparison of the case studies it can be concluded that, the closer the fault point is to the middle point, the more difficult it is for the system to detect and distinguish the faulty line, and the higher the peak value of the fault current is during the transient period.

From the DC fault currents analysis, there is a limited amount of time for the system to detect the fault and isolate the line, namely 1.6 ms. Up to now no DC breaker can successfully act in that time frame, taking into account the fault detection time needed (circa 0.6 ms) and the time it takes for the fault wave to travel to the VSC terminals (approximately 1.1 ms for the case studies). Because of that, limiting reactors were implemented, at the terminals of each VSC, to limit the peak current and delay its occurrence.

Moreover, it emerged from the simulations that the VSC responsible for the DC voltage control is the first to experience an overcurrent. This can be attributed to the fact that this station has the responsibility to provide for any excess power need in the grid, as it is not actively controlling its active power. The second station affected is the one closest to the network ground. The remaining stations, which control active power are the last to develop overcurrents. Among those, the fault is first detected at the station which injects active power into the DC network at the pre-fault stage, as, otherwise, the current direction needs first to change, which takes a few tenths of milliseconds, before feeding the fault.

Finally, for the analysed MTDC network, a successful fault isolation requires full semiconductor breakers with at least 100 mH reactors or hybrid I breakers with reactors of more than 200 mH inductance. The other two breaker technologies, i.e. the hybrid II and the resonant breakers, are not yet fast enough to handle DC contingencies for this kind of grid topology.

The second grid operating topology investigated was the bipole with ground return. In this topology, the fault current contributions from the stations are higher than in case of metallic return, as there is no return path impedance and the VSCs are affected earlier by the fault, experiencing high overcurrents within less than 1.8 ms. Additionally, the VSC fault currents reach higher peaks (4 pu) in steady state than when metallic return is used, which can damage the VSCs. For this reason, limiting reactors were used to limit the rate of rise of the DC fault currents.

In bipolar with ground return, both selective fault detection methods can be used, as they both combine selectivity with detection speed. A DC fault can be successfully isolated using full semiconductor breakers combined with at least 100 mH reactors or hybrid I breakers with reactors of inductance higher than 200 mH, i.e. same as for the bipolar configuration with metallic return.

After studying the response of bipolar grid topologies, monopolar configurations were simulated. It emerged from the simulations of positive pole-to-ground DC faults that, the stations with asymmetric monopole topology using metallic return share the same exact fault response with the positive pole converters in the bipolar configuration with metallic

return. Additionally, stations in asymmetric monopole topology with ground return share the same DC fault response with the positive pole converters in bipolar configuration with ground return. Consequently, the same conclusions drawn for the two bipolar cases apply for the asymmetric monopolar topologies as well. The only difference is their inability to transfer half of the stations power rating in case of a pole-to-ground fault.

From the investigated topologies, the one that differs significantly from the other topologies is the symmetric monopolar topology. This configuration appears, from the studied topologies, to have the best response with regard to pole-to-ground DC faults. The converters do not experience any overcurrents, except for the ones controlling the DC voltage level. Additionally, as soon as the DC lines and the respective DC link arm capacitors, depending on the faulty pole, get discharged, the fault current returns to zero in a new steady-state after approximately 25 to 30 ms.

In symmetric monopole, due to the DC link mid-point ground, half of the link gets connected in series with the fault and is overcharged during the fault period, partially compensating for the voltage drop in the other half of the DC link. However, this unbalance in the link cannot be restored automatically even if the fault is quickly isolated. The only tested way through which the system can return to its pre-fault condition is by de-energizing the MTDC network and starting it up normally. Another concept to resume normal operation includes de-blocking the IGBTs, after the fault isolation, and disconnecting the middle-point ground momentarily to control the DC link voltage and restore balance.

Regarding the symmetric monopole, no limiting reactors are necessary, as the affected converter does not experience an overcurrent sooner than 6.2 ms from the fault occurrence. As a result, the two fastest DC breaker technologies (Solid state breakers and hybrid I) are able to successfully isolate the fault without the need of additional protection measures. Hybrid II and resonance breakers cannot prevent a converter damage.

Considering all the analysed concepts, it can be concluded that the protection of MTDC networks is a manifold problem. Fault currents develop in less than 2 ms and therefore the time constraints are narrow for the system to react and isolate the fault and keep providing an uninterrupted power transfer. This thesis shows that limiting reactors are needed to successfully limit the fault currents magnitude and rate of rise. Moreover, the current direction method is proposed as a fast selective fault detection strategy which can be used in every grid topology. On the other hand, the current derivative method, although faster by circa 0.1 ms, is more difficult to implement in real systems due to the difficulty in determining a current derivative threshold value among the converters.

Finally, the hybrid I DC breaker is the breaker technology that combines low on-state losses with a low total interruption time and it is, thus, preferred over the other investigated DC breaker concepts.

7.1 Future Work

There are certain aspects, regarding HVDC grids and their protection, which need to be further investigated. Suggestions for future work include:

- Simulation models of multi-level converters need to be implemented to study more in detail their fault response. Special attention should be paid to full-bridge submodules and hybrid solutions proposed for fault current limitation;
- A combination of LCC and VSC technologies in a multi-terminal grid needs to be evaluated, especially in terms of control and protection;
- A more detailed analysis of the dynamics and control of the different DC breaker technologies is needed to evaluate them both in normal operation and in case of contingencies;
- EMTP analysis should be made to draw conclusions regarding the response of DC cables during a fault, and specifically during the transient stage, as Matlab/Simulink® does not offer a frequency-dependent line model;
- The DC cable thermal stresses during a DC fault should be analysed;
- The impact of different ground types (resistive, inductive, capacitive) on the developing fault currents should be studied;
- In the symmetric monopole configuration, the effect of middle-point grounding types on the voltage balance between the two DC link arms needs to be evaluated, in case of a DC fault;
- A study of short-circuit faults for the symmetric monopole and for bipolar topologies, at different points of the grid, is important, even though their probability is small;
- A sensitivity analysis needs to be conducted on the effect of the DC fault resistance, for different ground types, on the fault currents development;
- Different control strategies, such as wavelet-based methods and travelling wave methods, for fault detection and allocation should be further investigated and compared;
- Cost-benefit analysis has to be carried out in order to reach a final conclusion on the HVDC system design. This analysis should focus on the limiting reactor sizes and on the DC breaker technologies regarding HVDC protection;
- A laboratory set-up should be implemented to validate the simulation results regarding the natural response of the multi-terminal DC grids in case of a DC fault.

Appendix A

A.1 Bipole with metallic return: Normal Operation

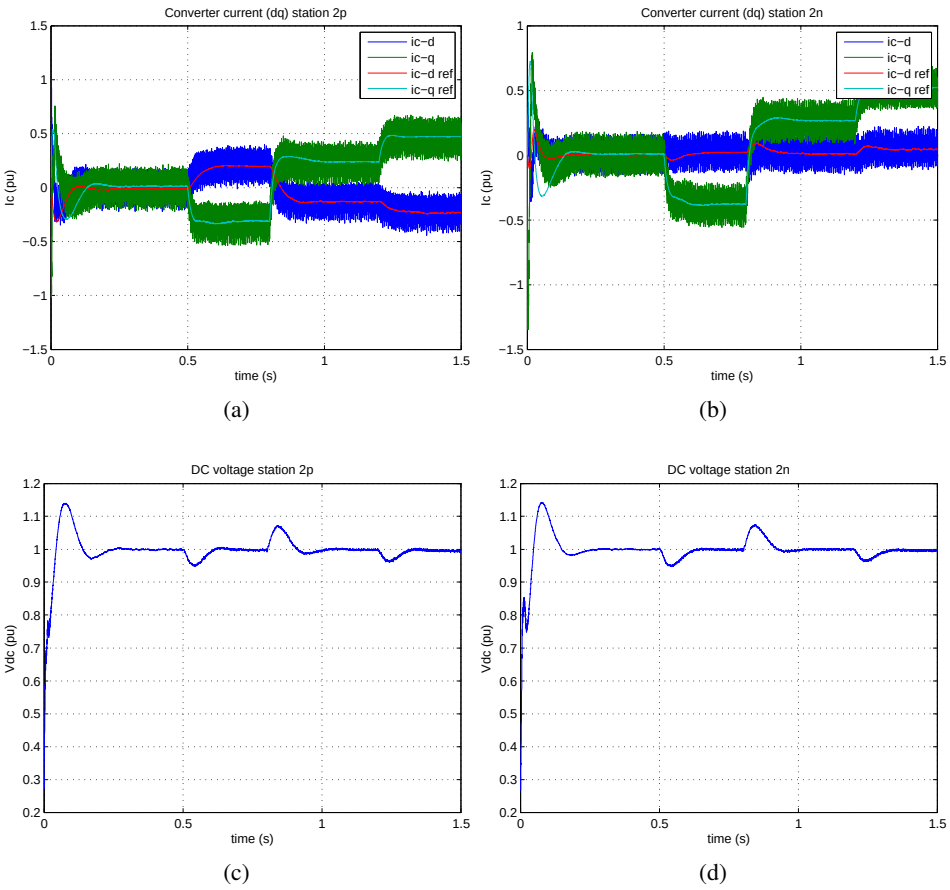


Figure A.1: VSC2 AC current (dq) and DC voltage in normal operation

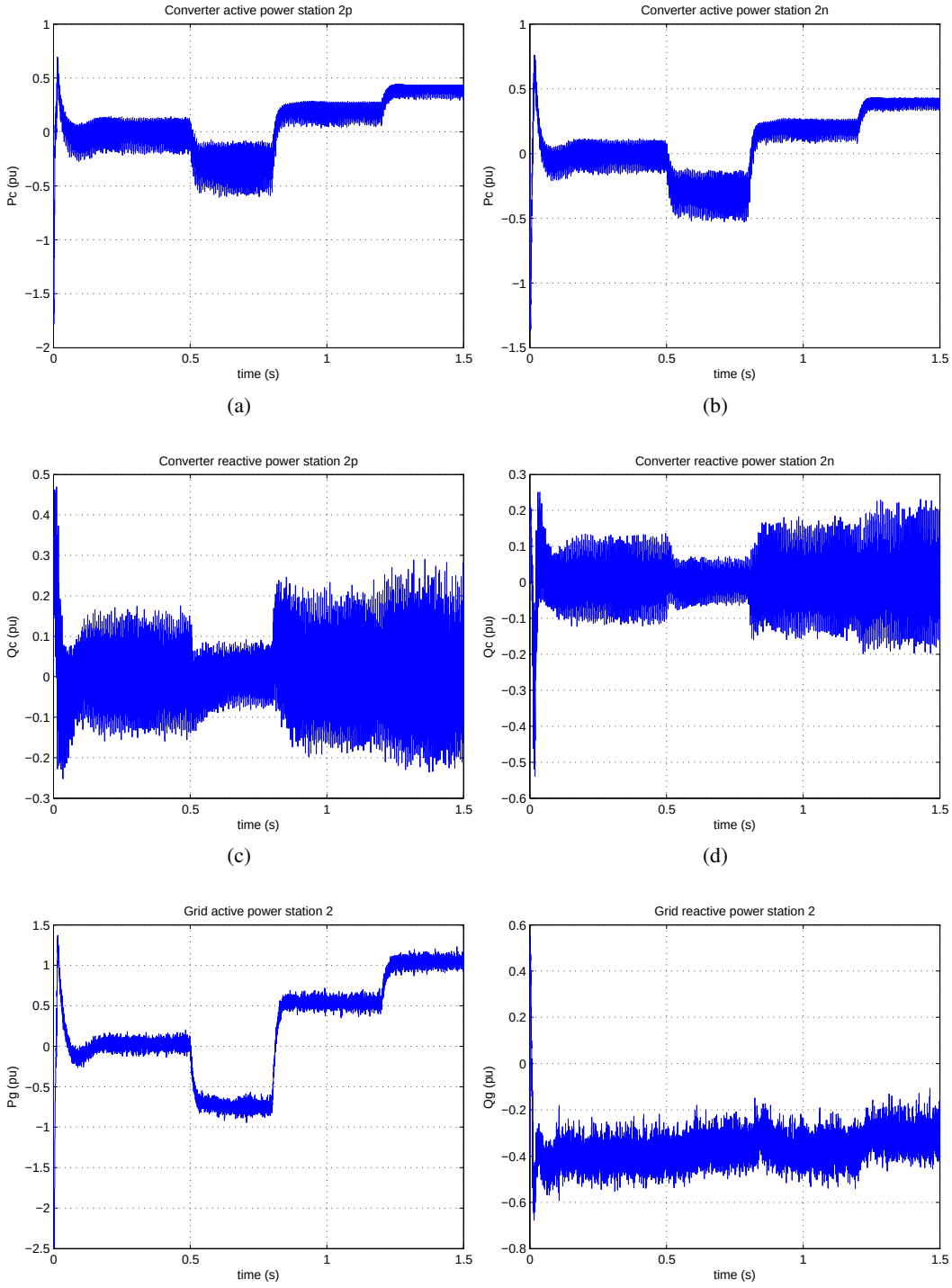


Figure A.2: VSC2 Active and reactive power in normal operation

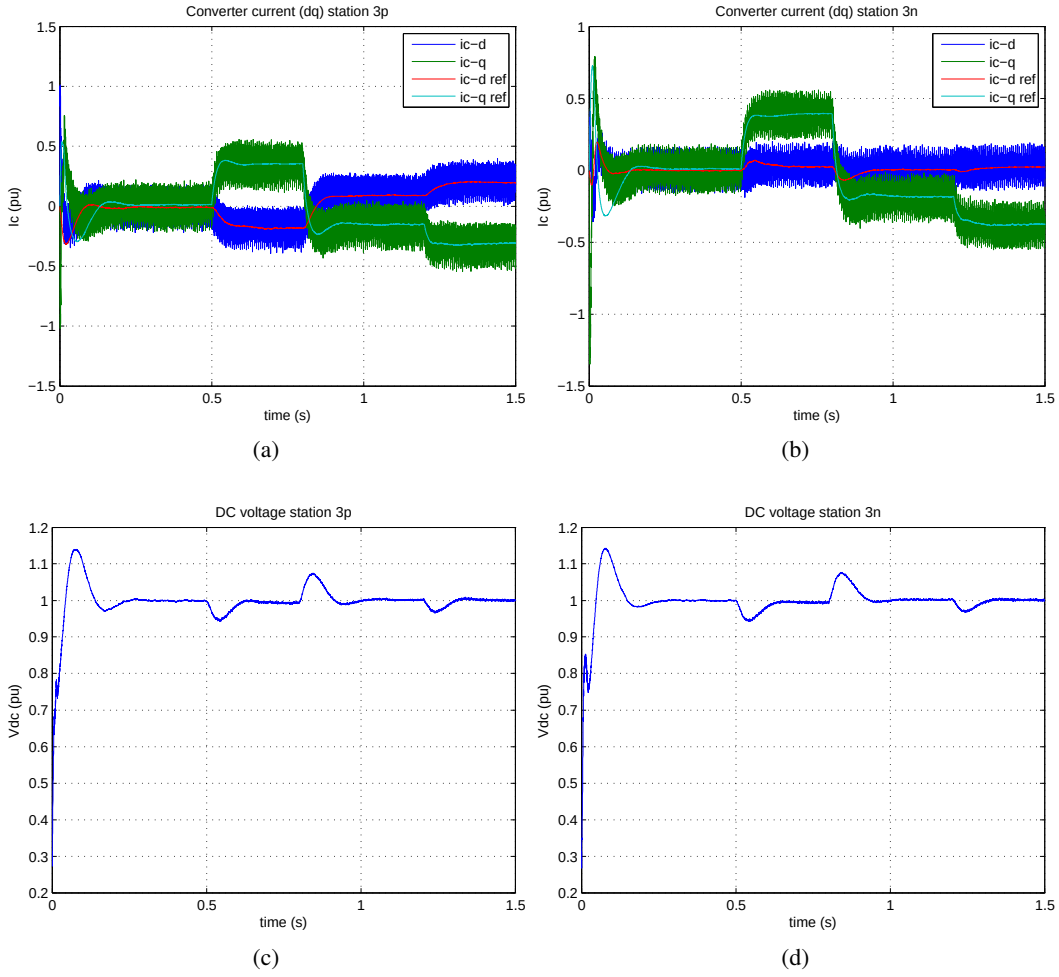


Figure A.3: VSC3 AC current (dq) and DC voltage in normal operation

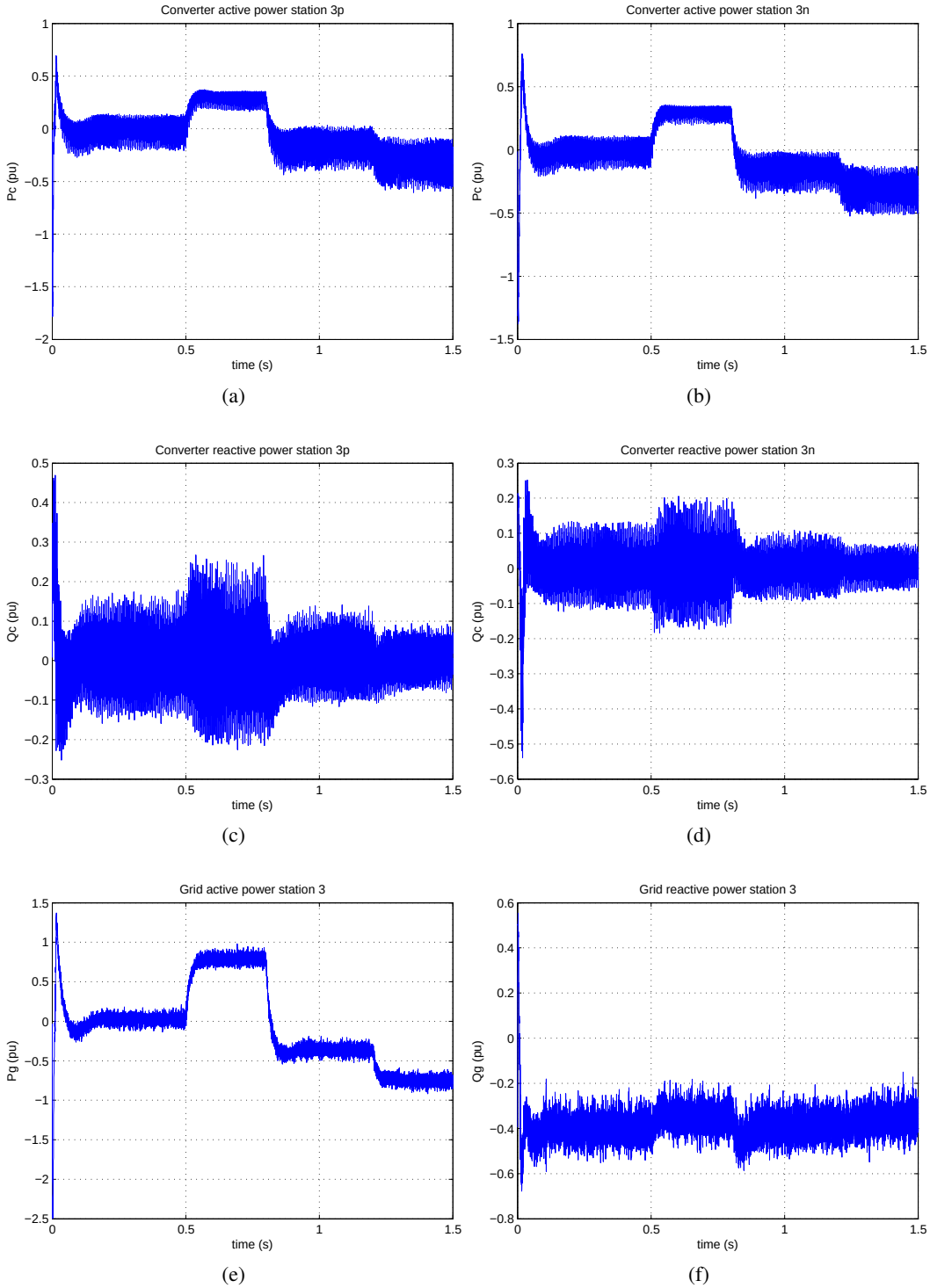


Figure A.4: VSC3 Active and reactive power in normal operation

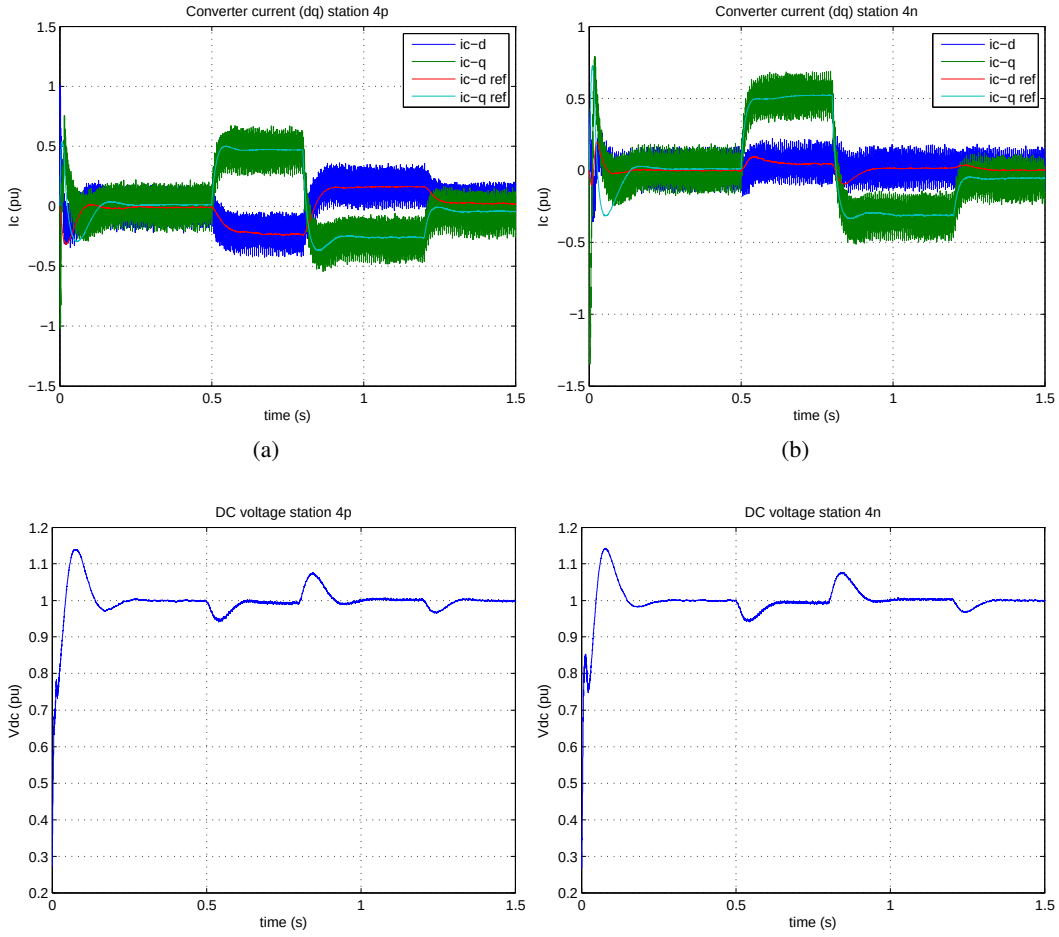


Figure A.5: VSC4 AC current (dq) and DC voltage in normal operation

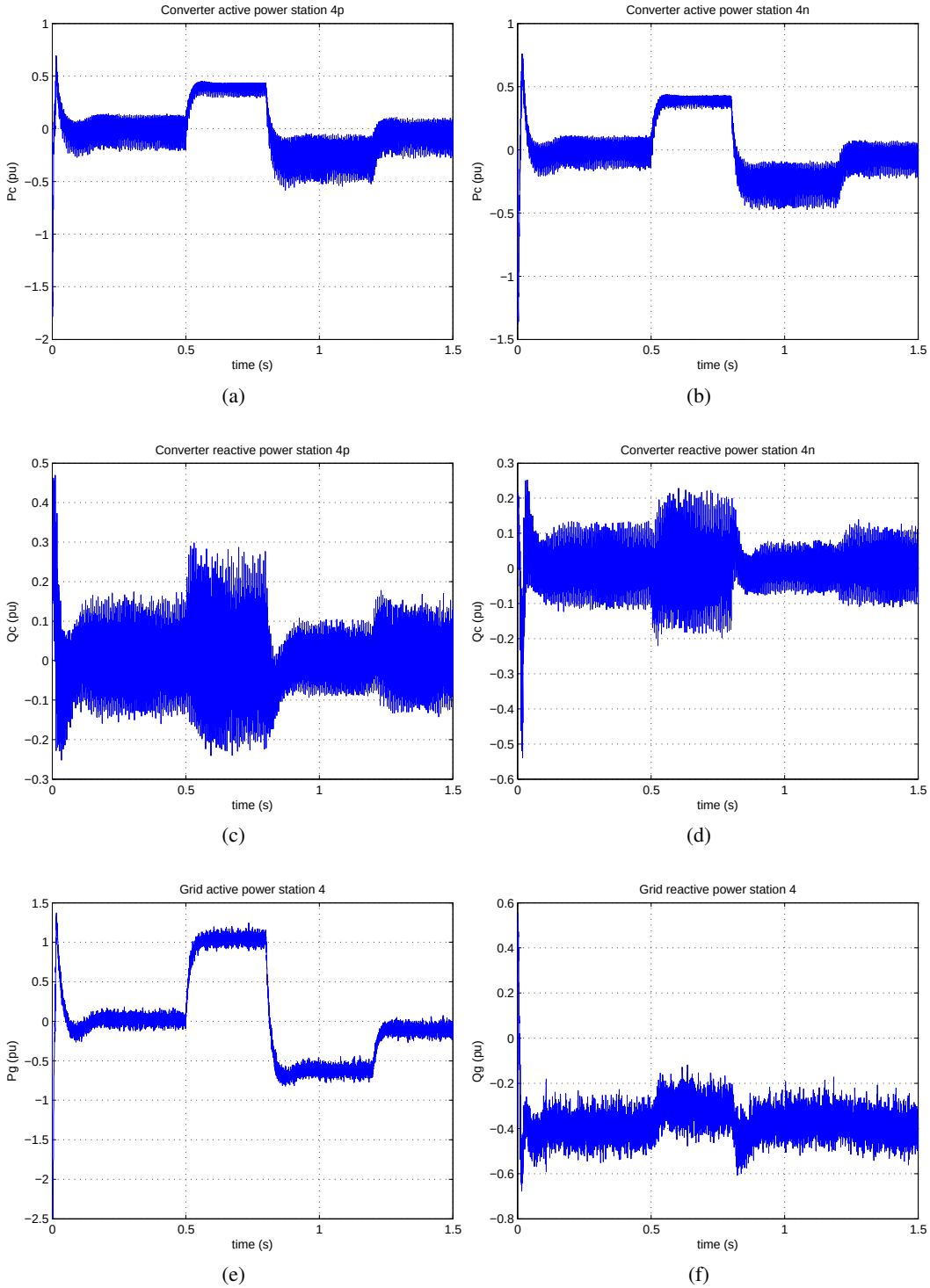
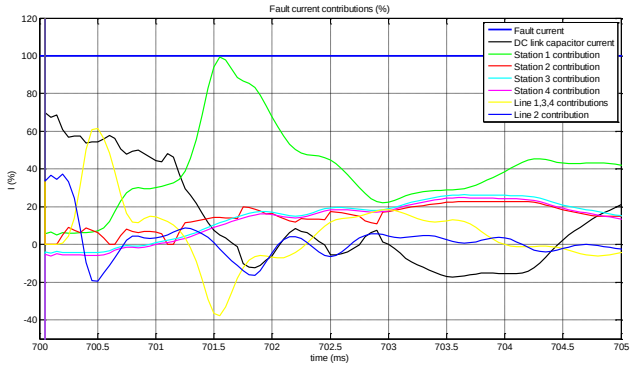
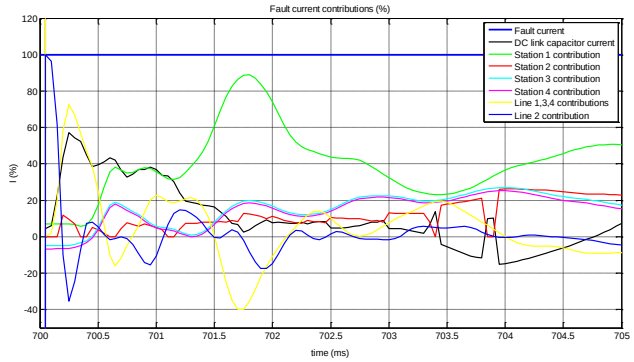


Figure A.6: VSC4 Active and reactive power in normal operation

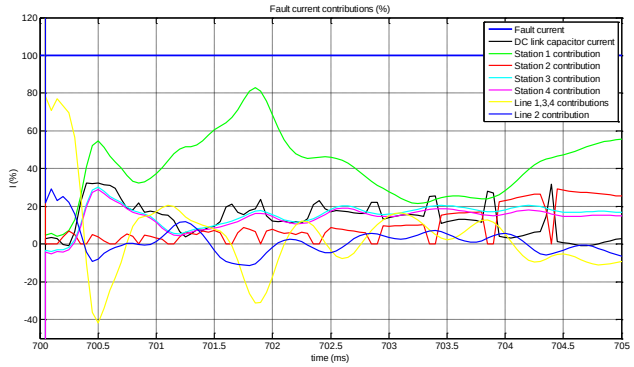
A.2 Bipole with metallic return: DC fault cases



(a) Case 1 (1 km from VSC2)

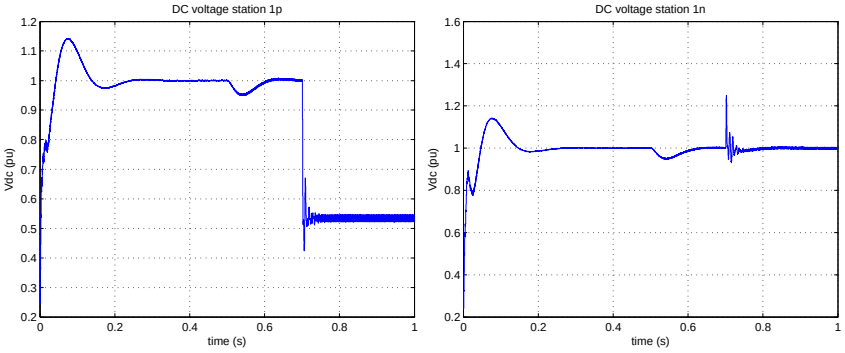


(b) Case 2 (25 km from VSC2)



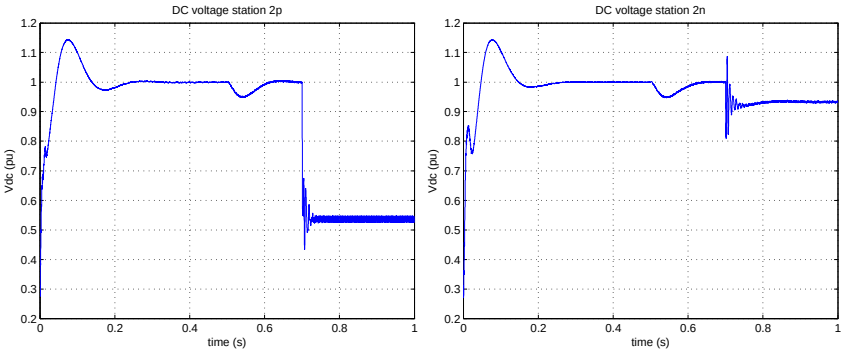
(c) Case 3 (49 km from VSC2)

Figure A.7: Fault current contributions in percentage in the different case studies



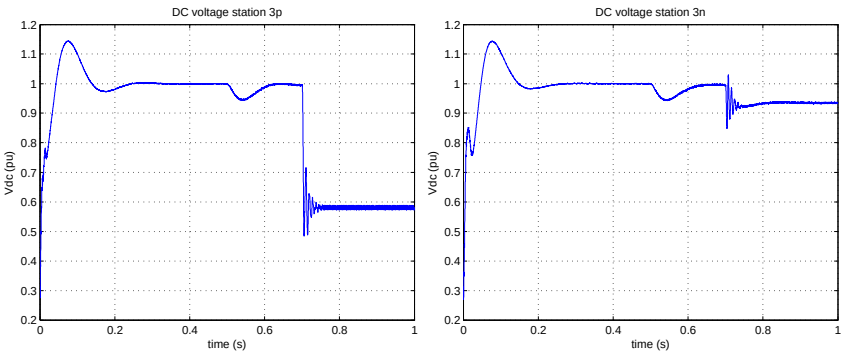
(a)

(b)



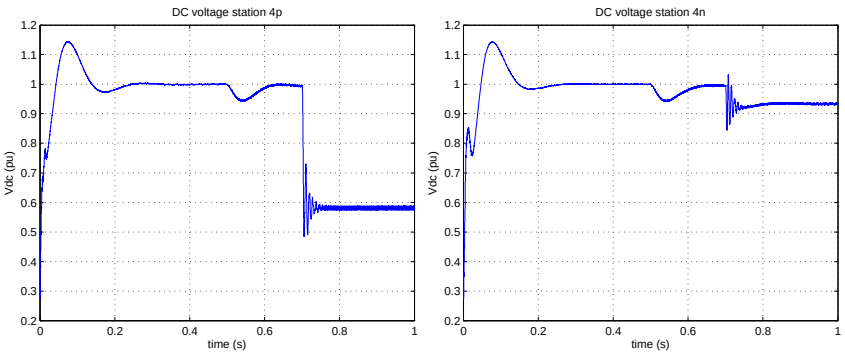
(c)

(d)



(e)

(f)



(g)

(h)

Figure A.8: DC Voltage fault case 1 (1km from VSC2)

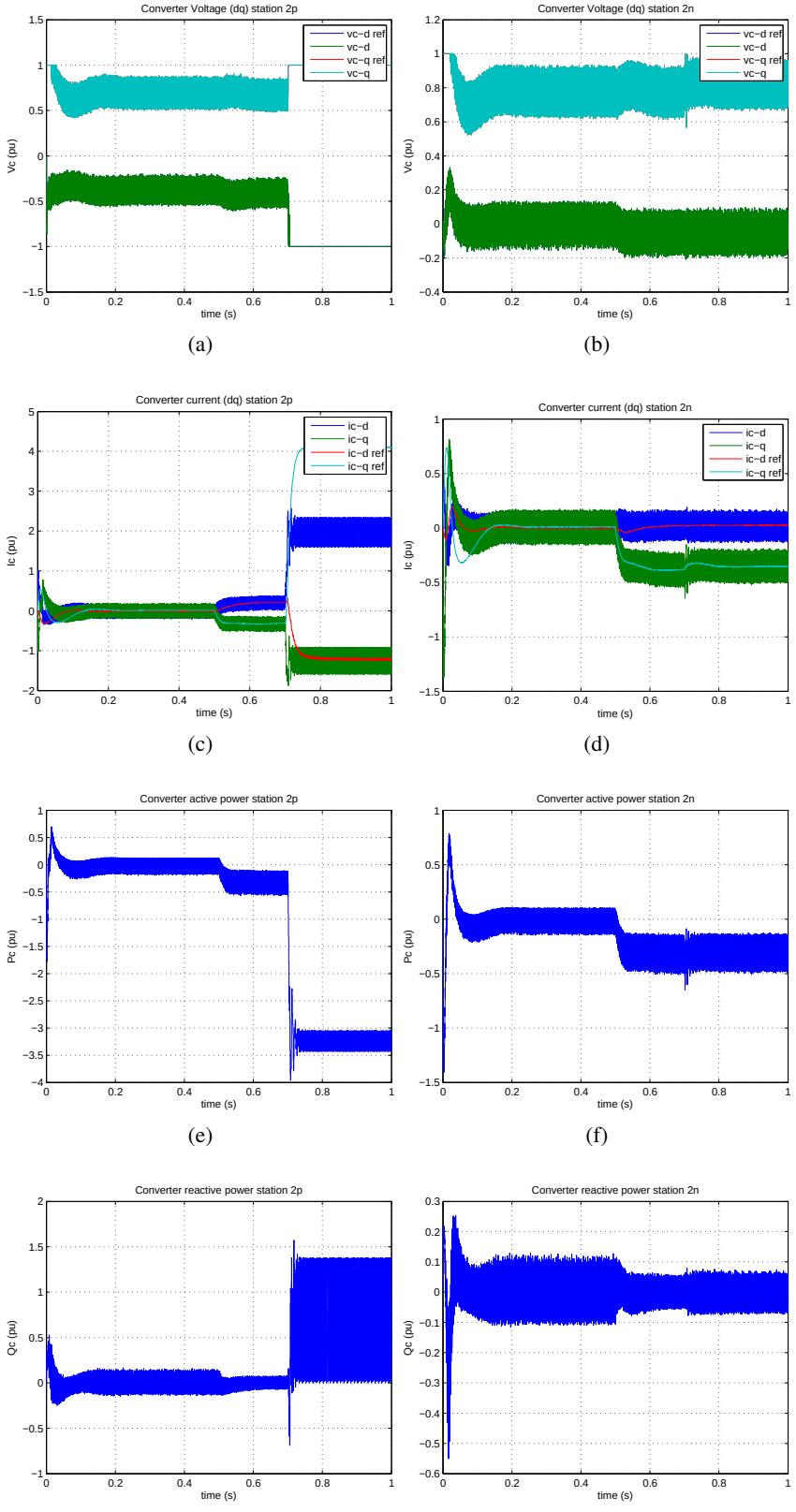


Figure A.9: VSC2 AC characteristics fault case 1 (1km from VSC2)

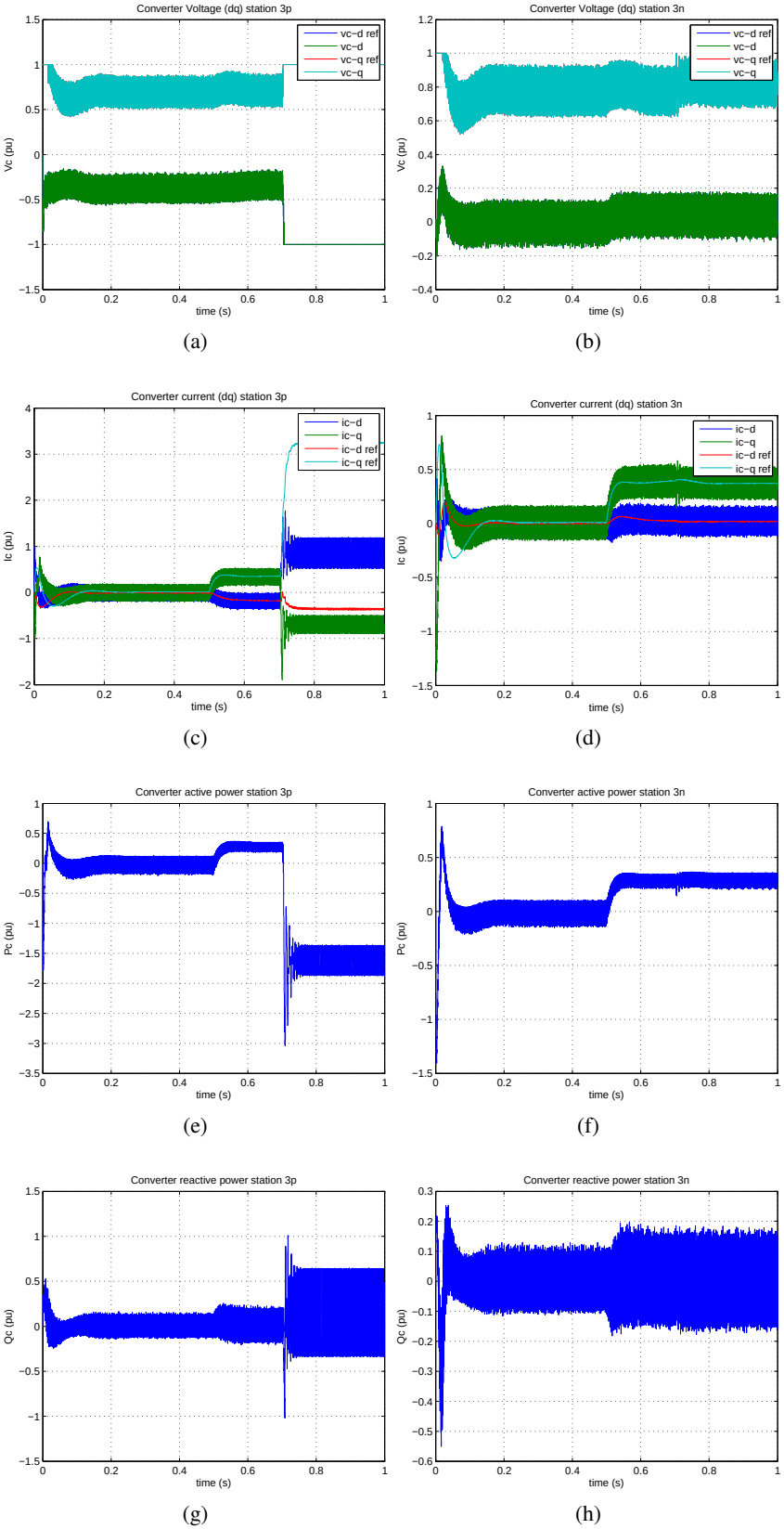
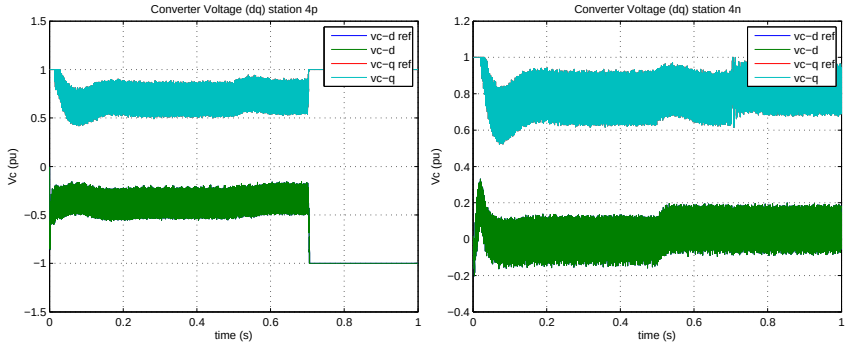
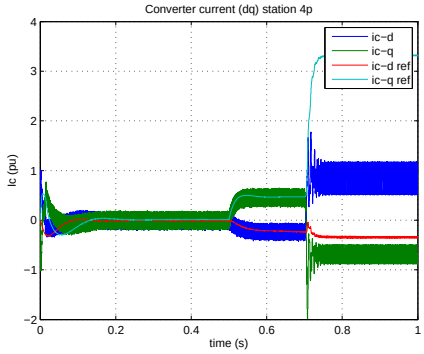


Figure A.10: VSC3 AC characteristics fault case 1 (1km from VSC2)

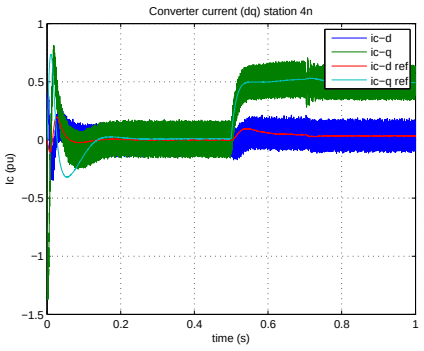


(a)

(b)



(c)



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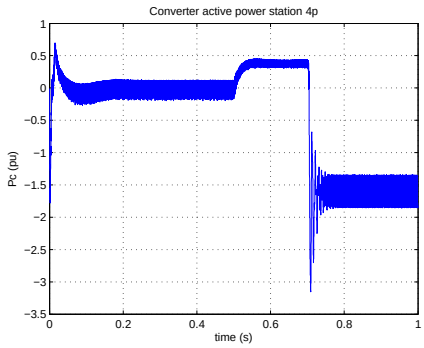

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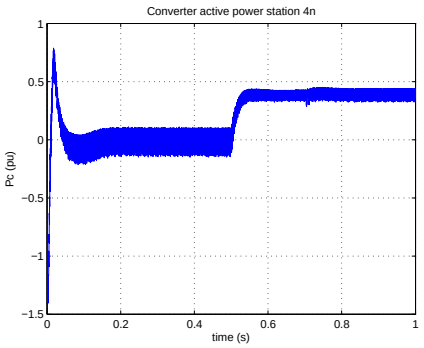

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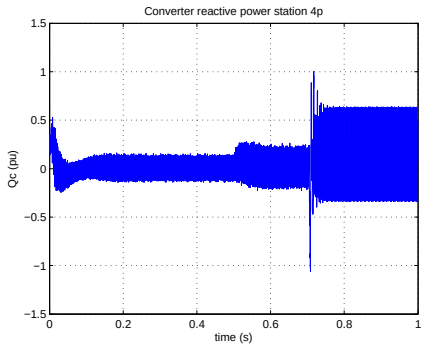
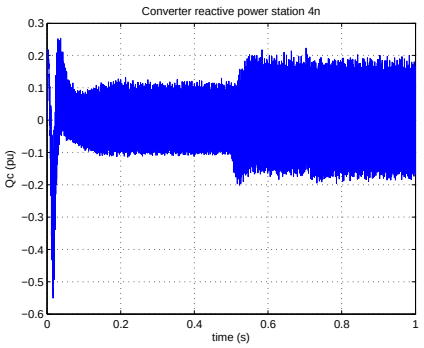


(g)



(h)

Figure A.11: VSC4 AC characteristics fault case 1 (1km from VSC2)

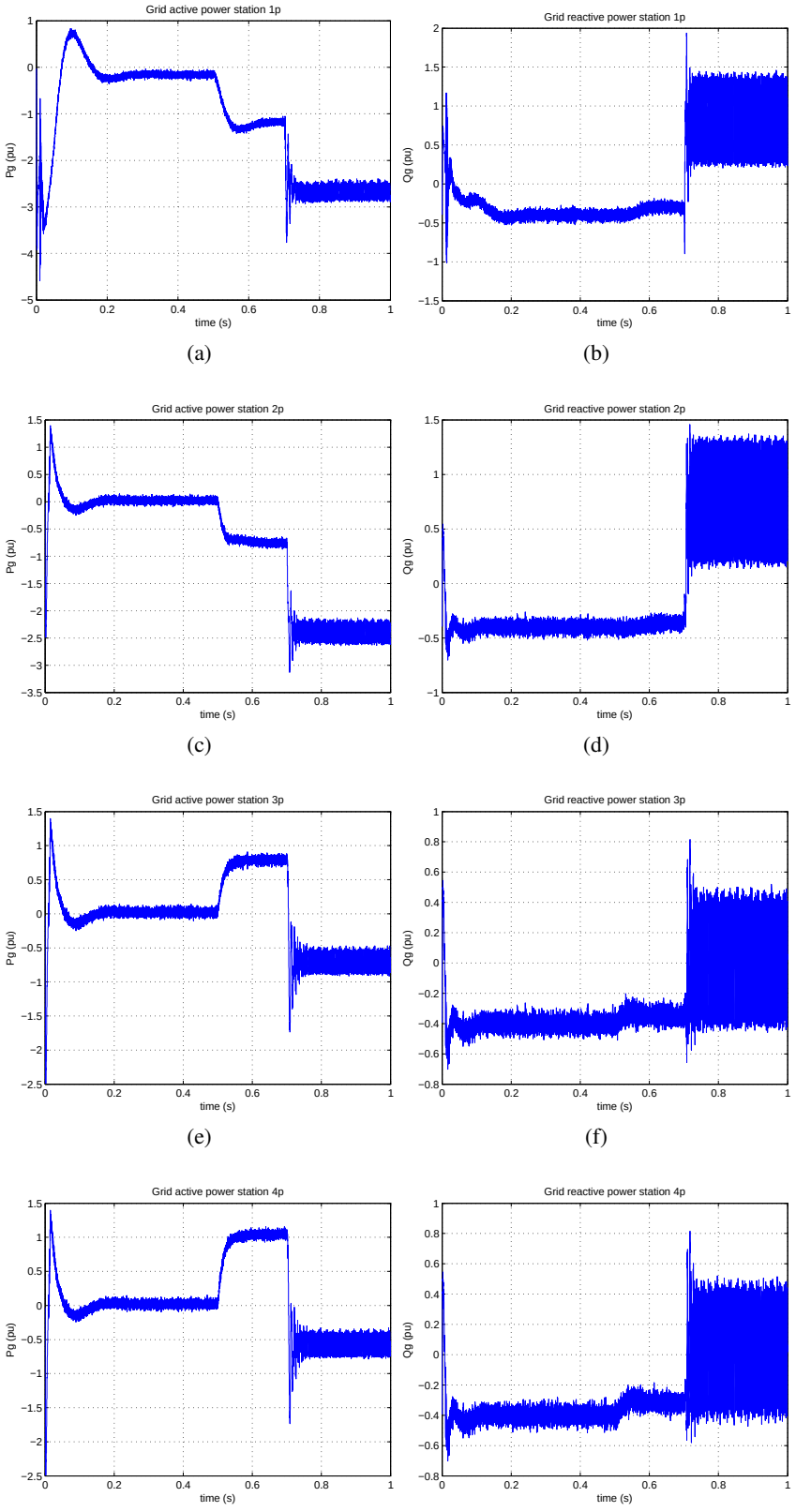
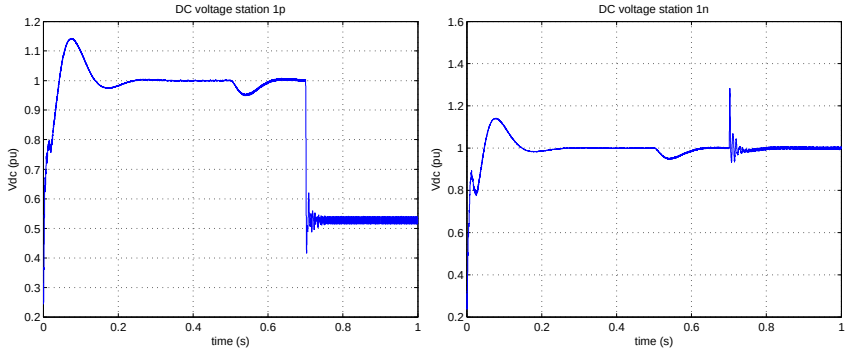
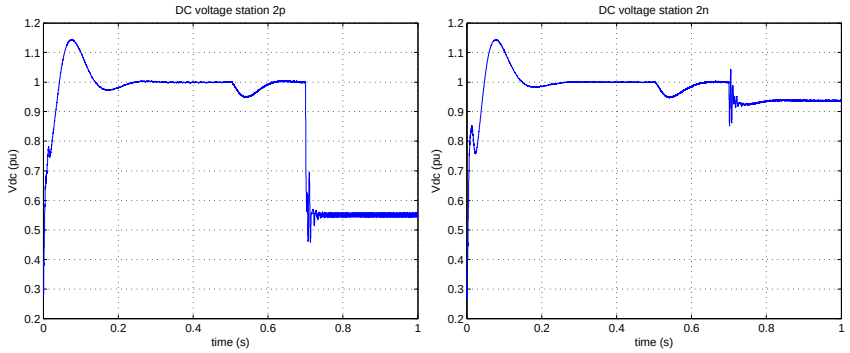


Figure A.12: Grid active and reactive power fault case 1 (1km from VSC2)



(a)

(b)



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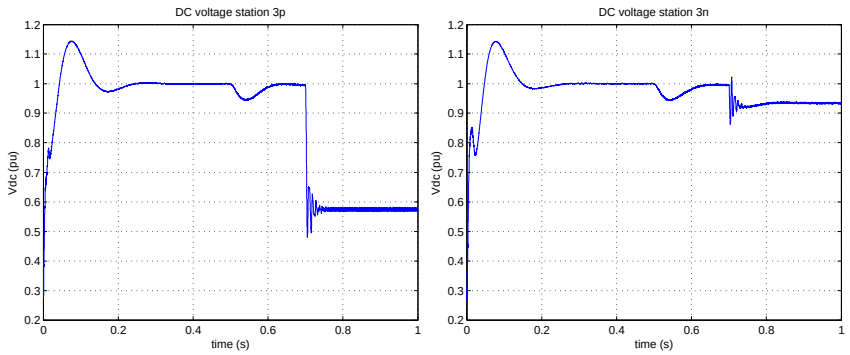

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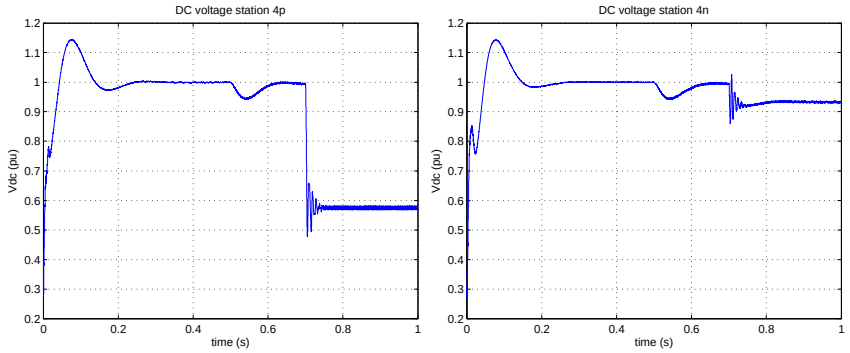
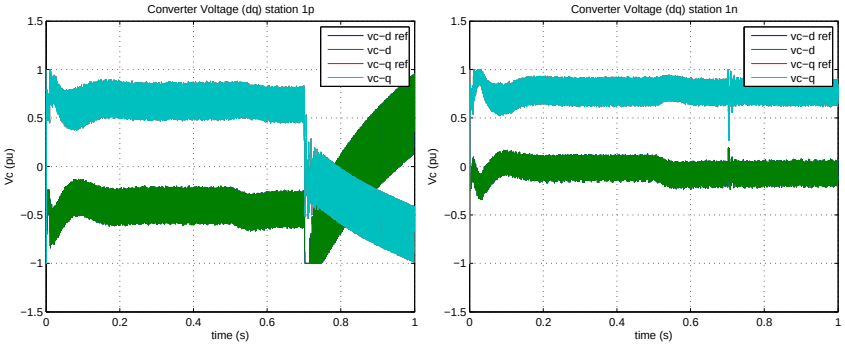
(f)



(g)

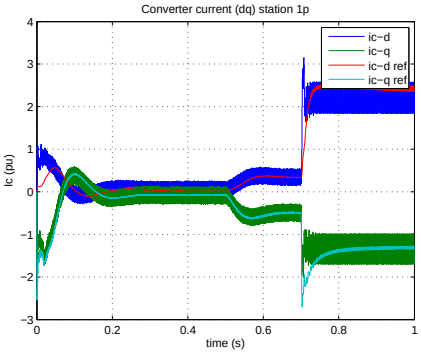
(h)

Figure A.13: DC Voltage fault case 2 (25km from VSC2)

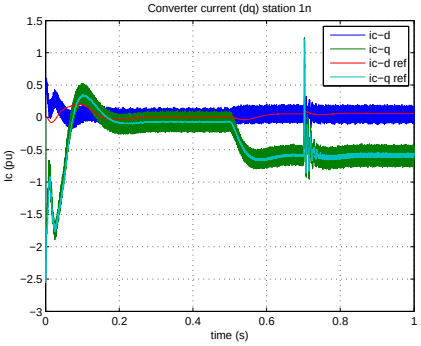


(a)

(b)



(c)



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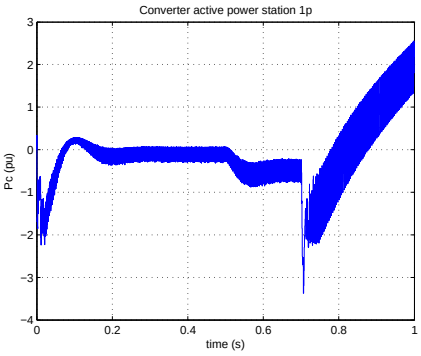

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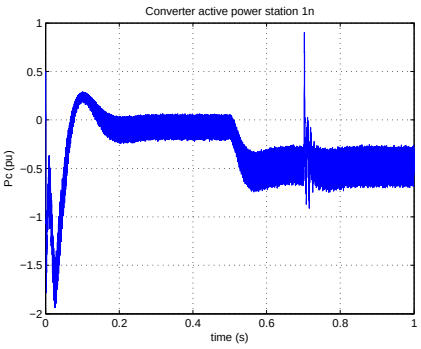

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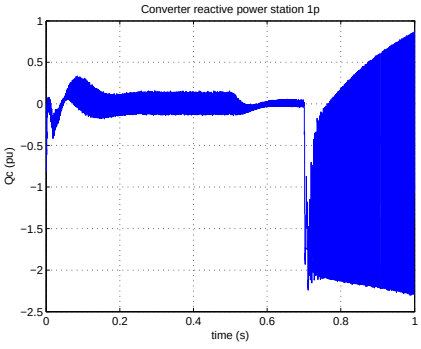

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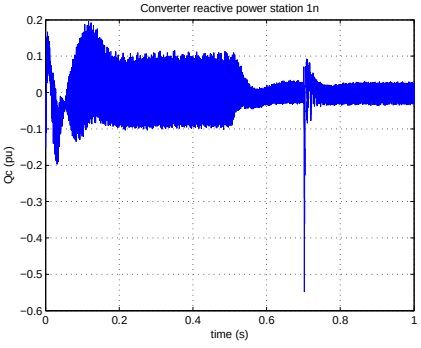


(h)

Figure A.14: VSC1 AC characteristics fault case 2 (25km from VSC2)

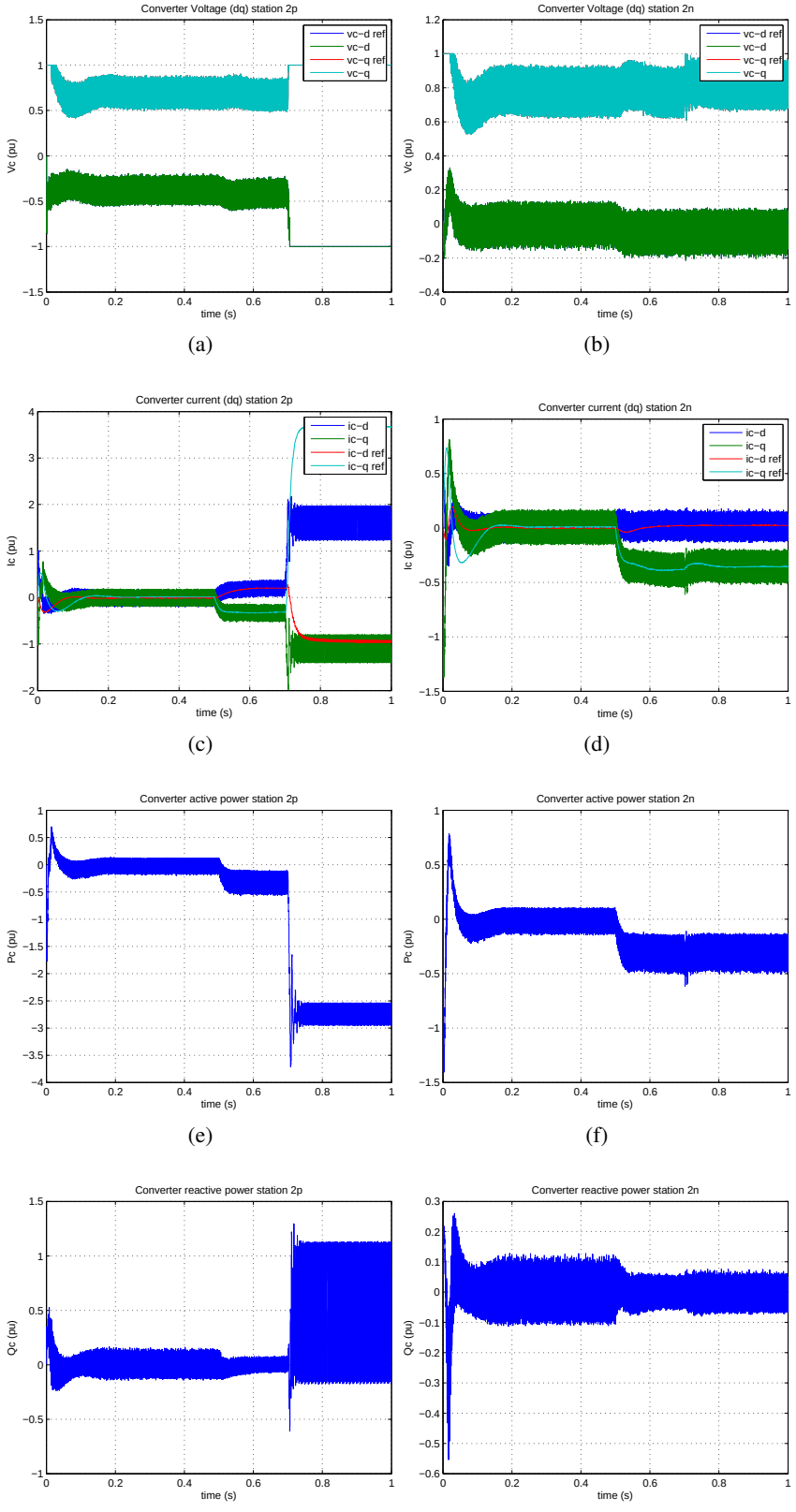


Figure A.15: VSC2 AC characteristics fault case 2 (25km from VSC2)

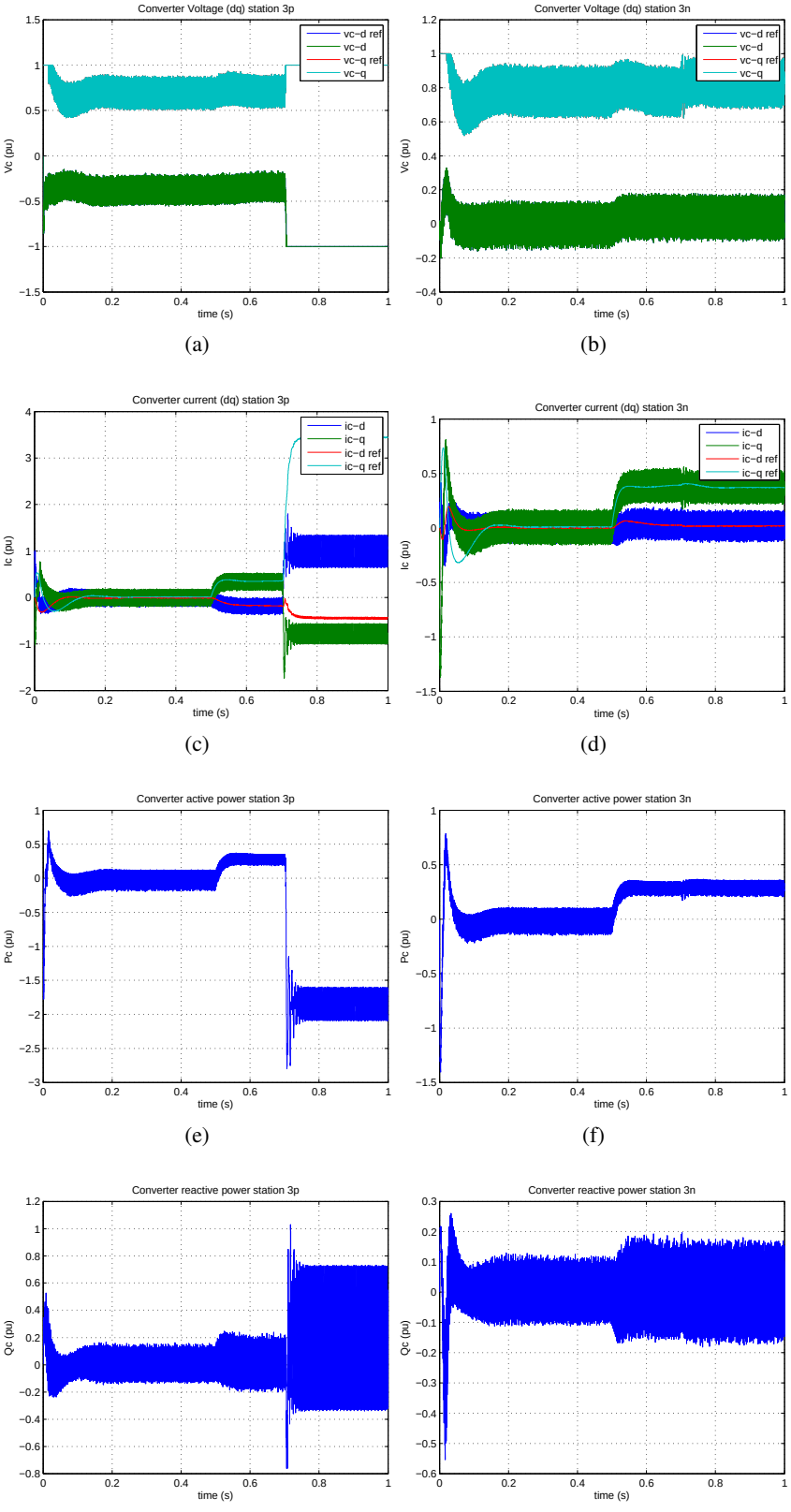


Figure A.16: VSC3 AC characteristics fault case 2 (25km from VSC2)

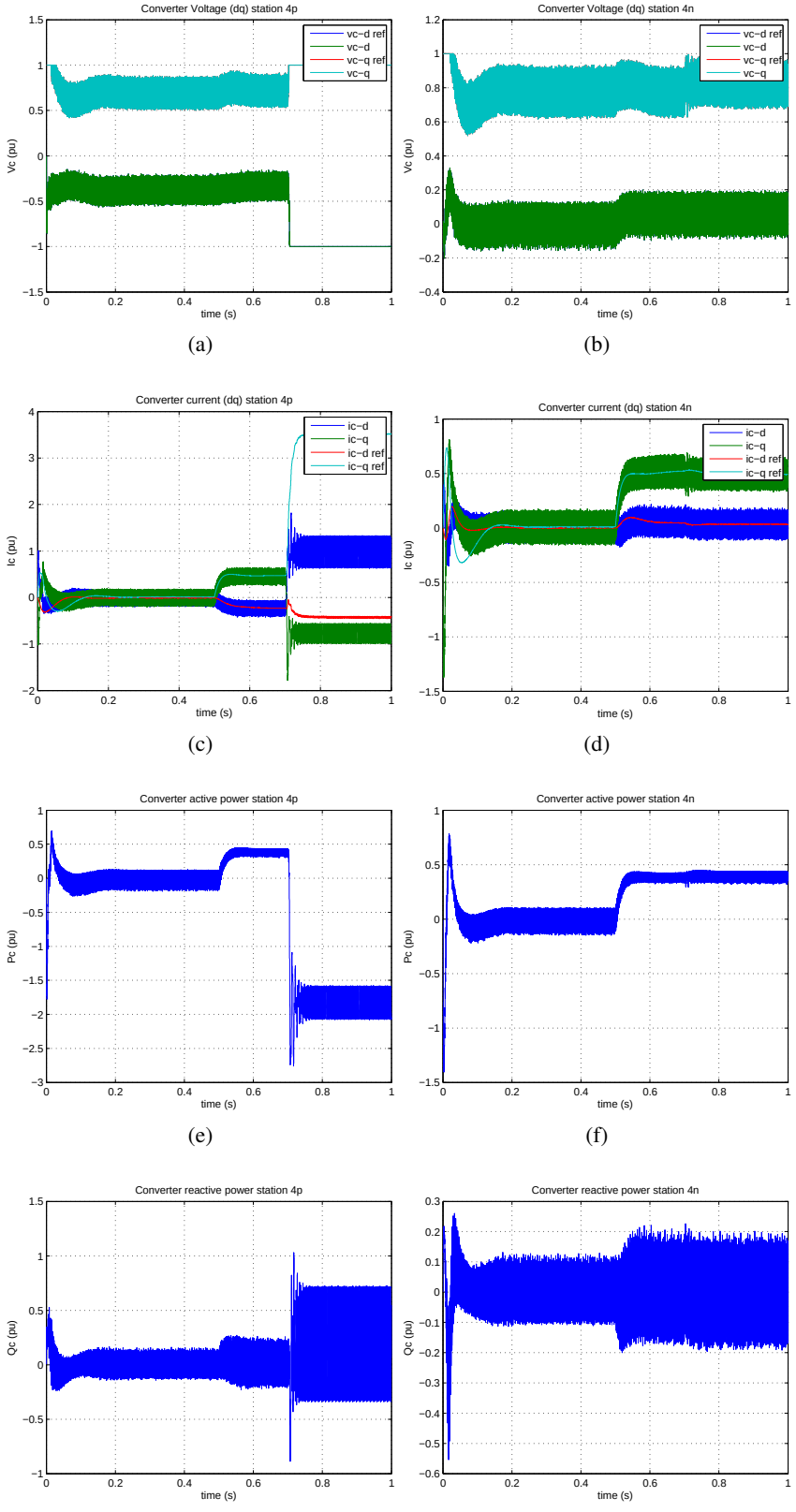


Figure A.17: VSC4 AC characteristics fault case 2 (25km from VSC2)

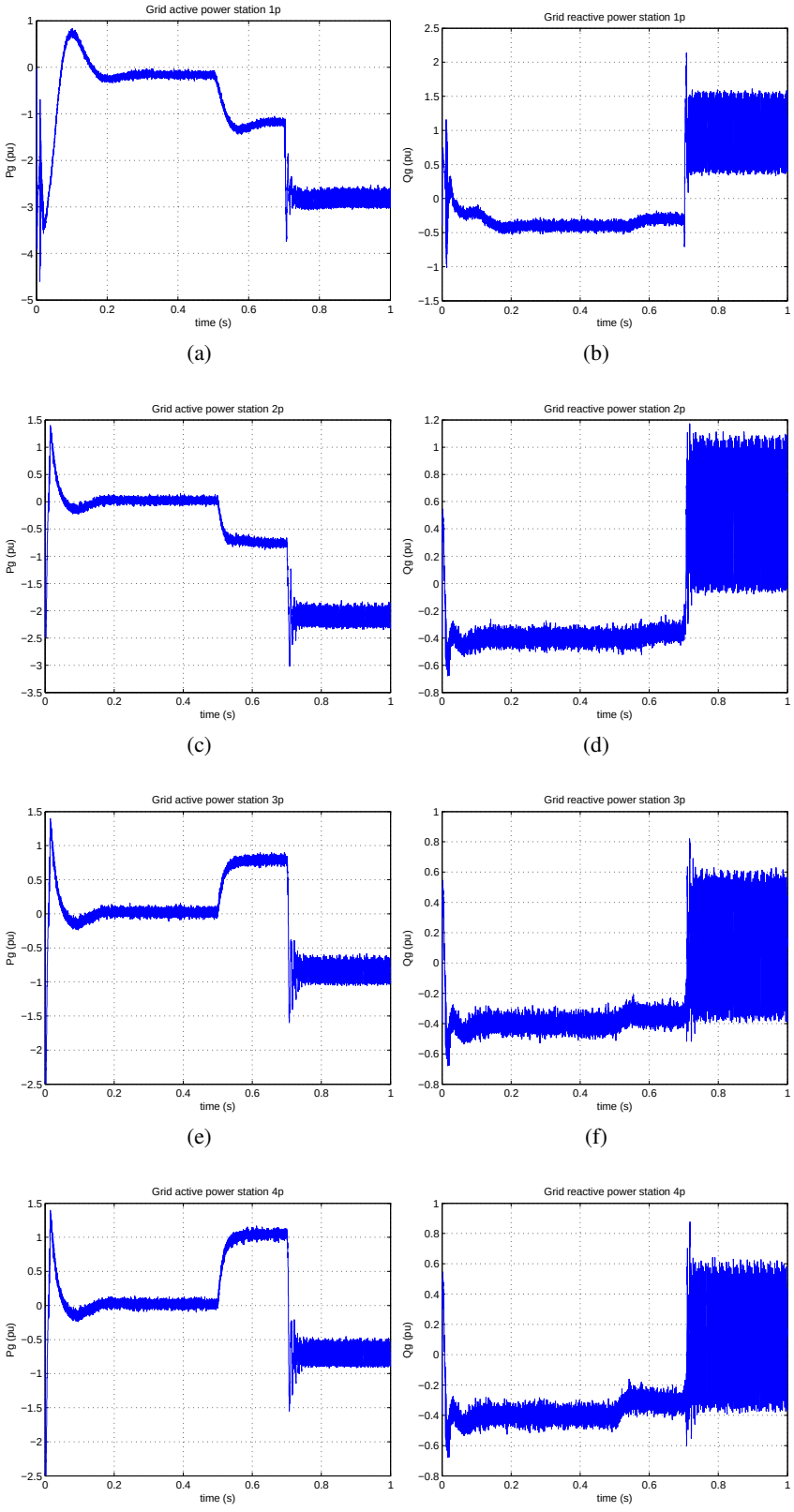
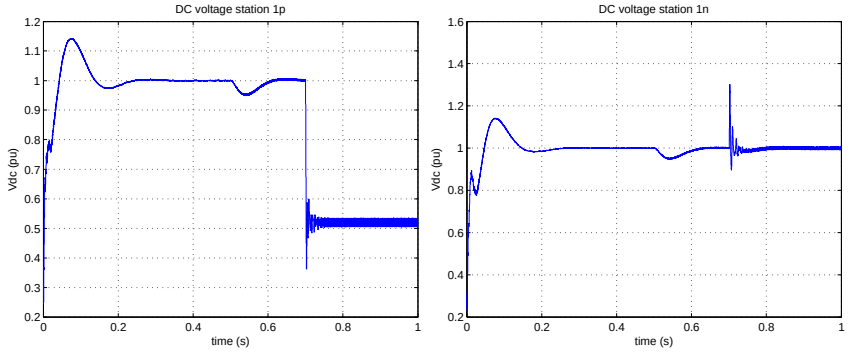
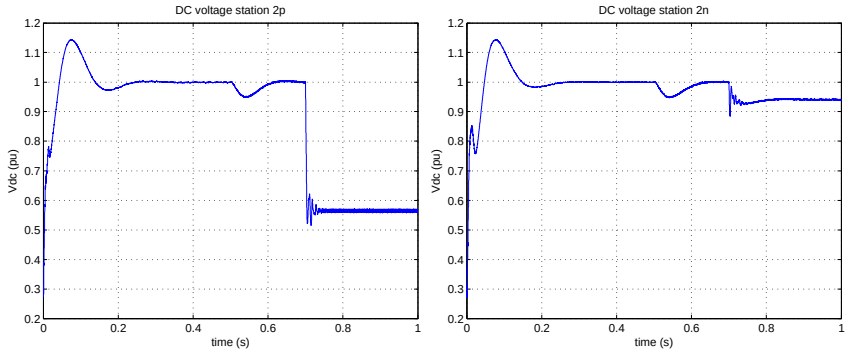


Figure A.18: Grid active and reactive power fault case 2 (25km from VSC2)



(a)

(b)



(c)

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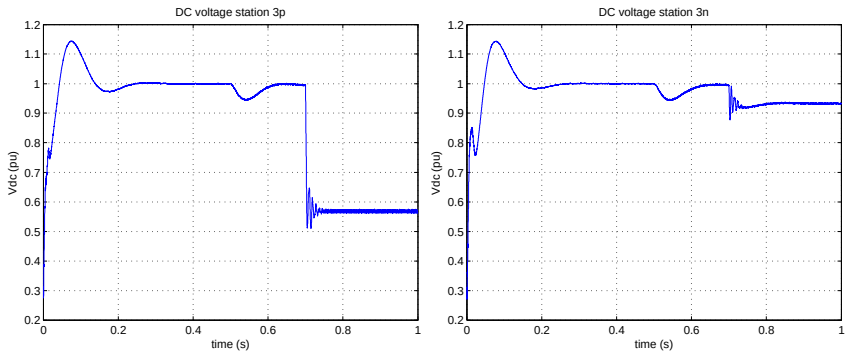

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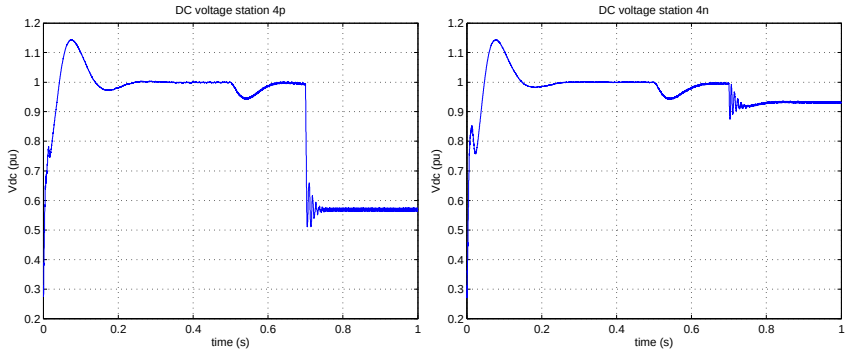


(g)

(h)

Figure A.19: DC Voltage fault case 3 (49km from VSC2)

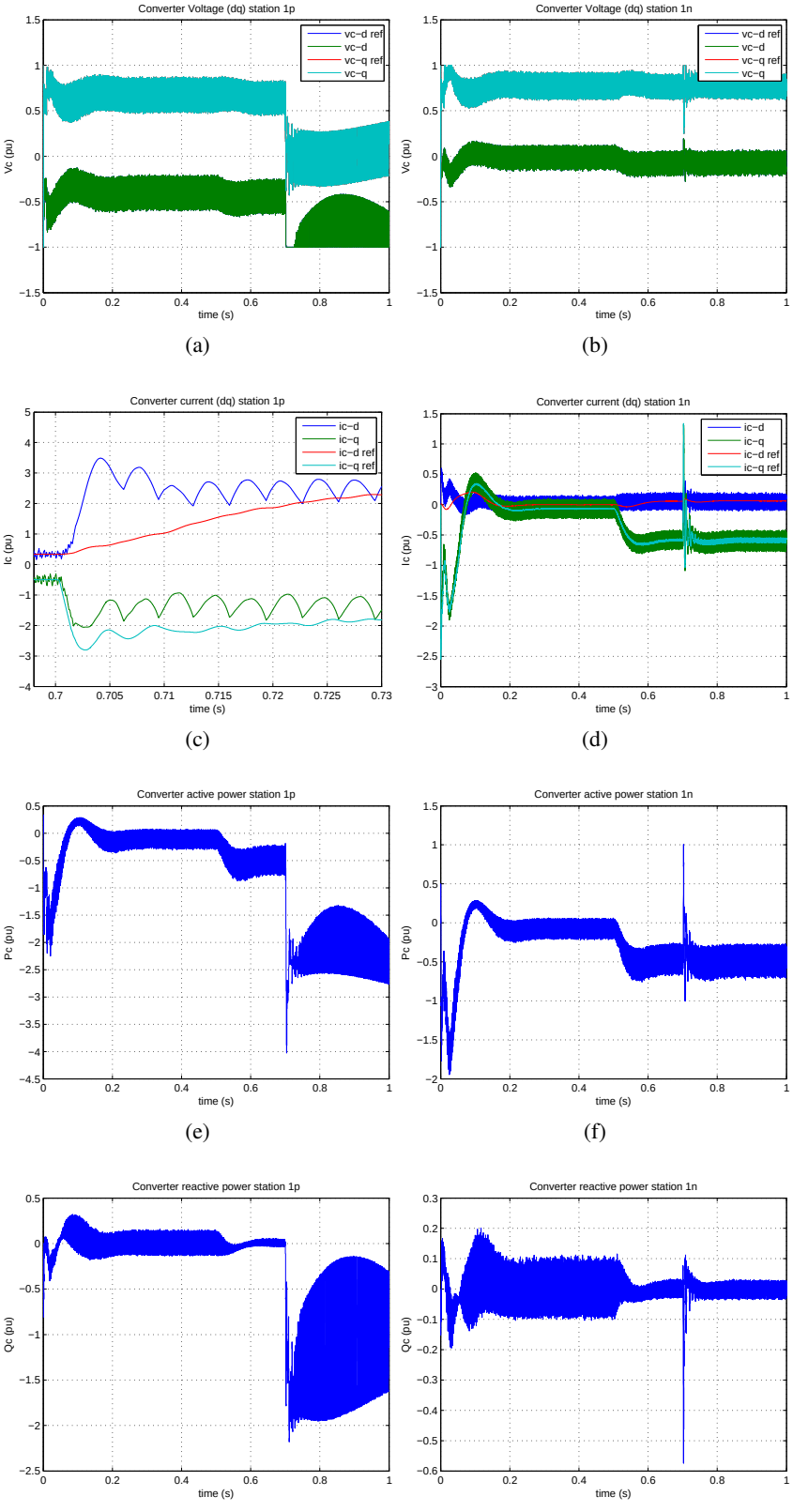


Figure A.20: VSC1 AC characteristics fault case 3 (49km from VSC2)

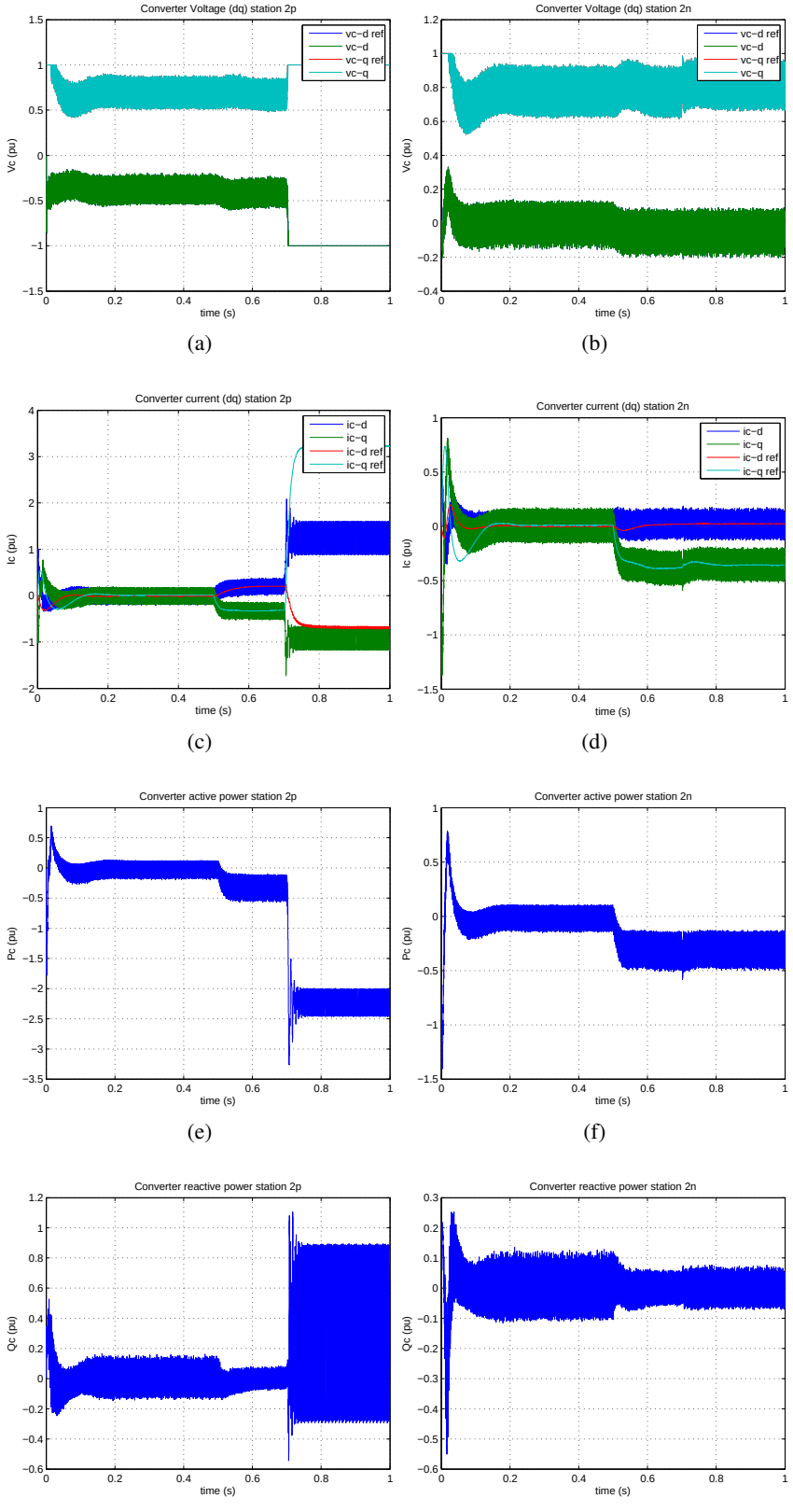


Figure A.21: VSC2 AC characteristics fault case 3 (49km from VSC2)

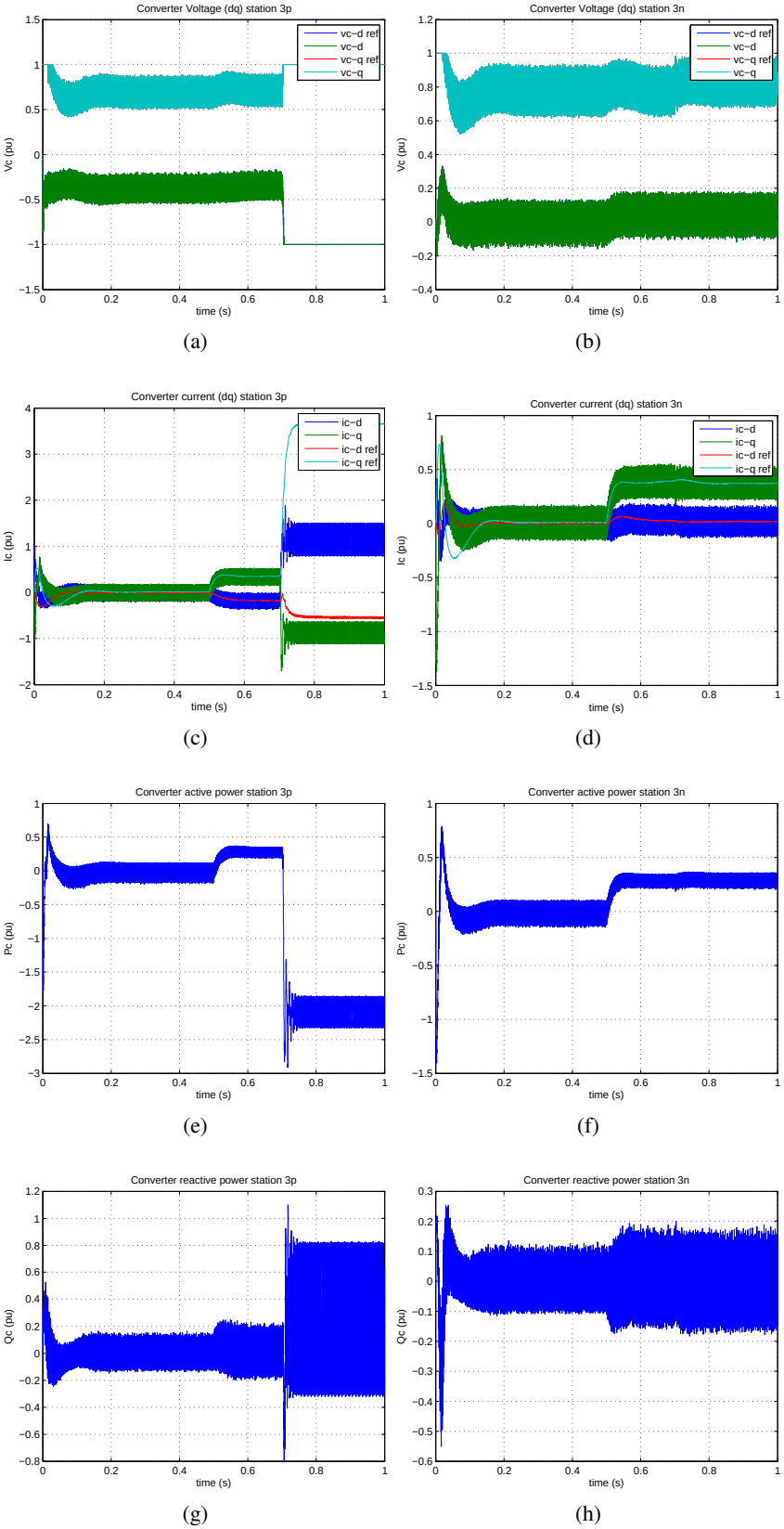
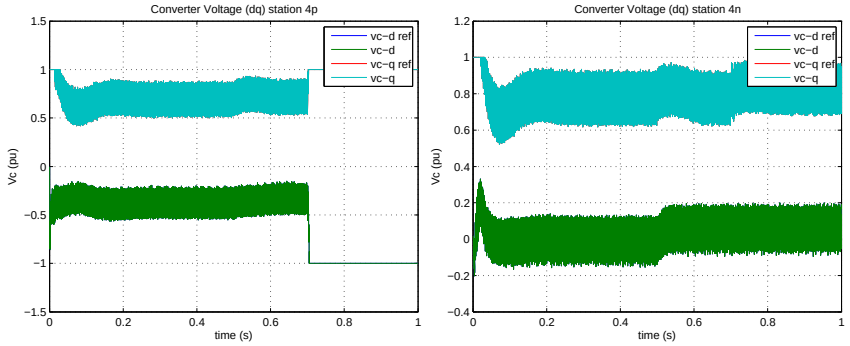
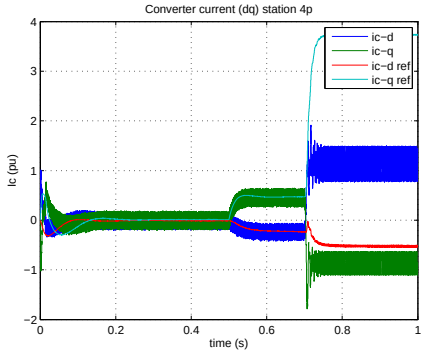


Figure A.22: VSC3 AC characteristics fault case 3 (49km from VSC2)



(a)

(b)



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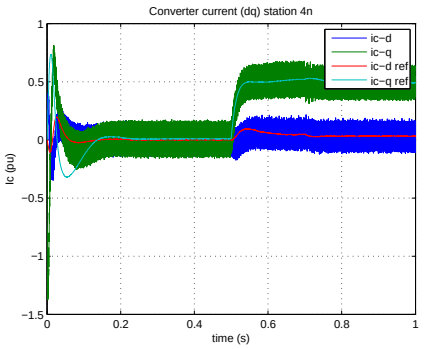

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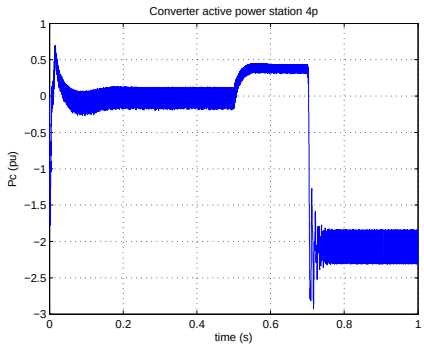
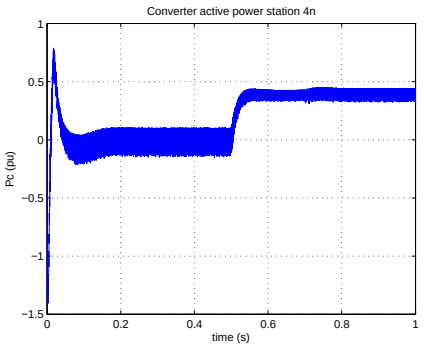
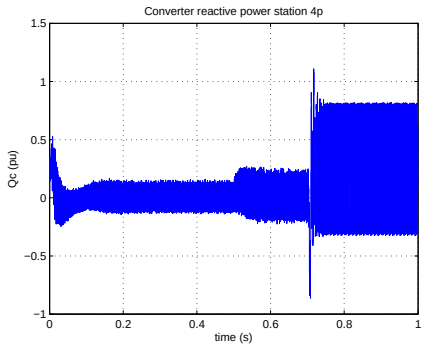


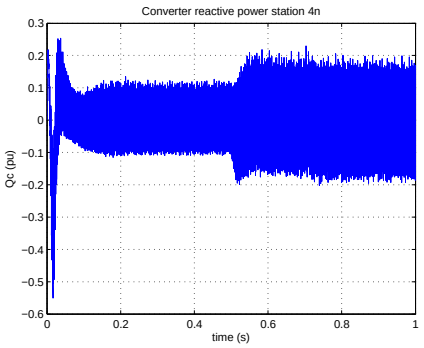
(e)



(f)



(g)



(h)

Figure A.23: VSC4 AC characteristics fault case 3 (49km from VSC2)

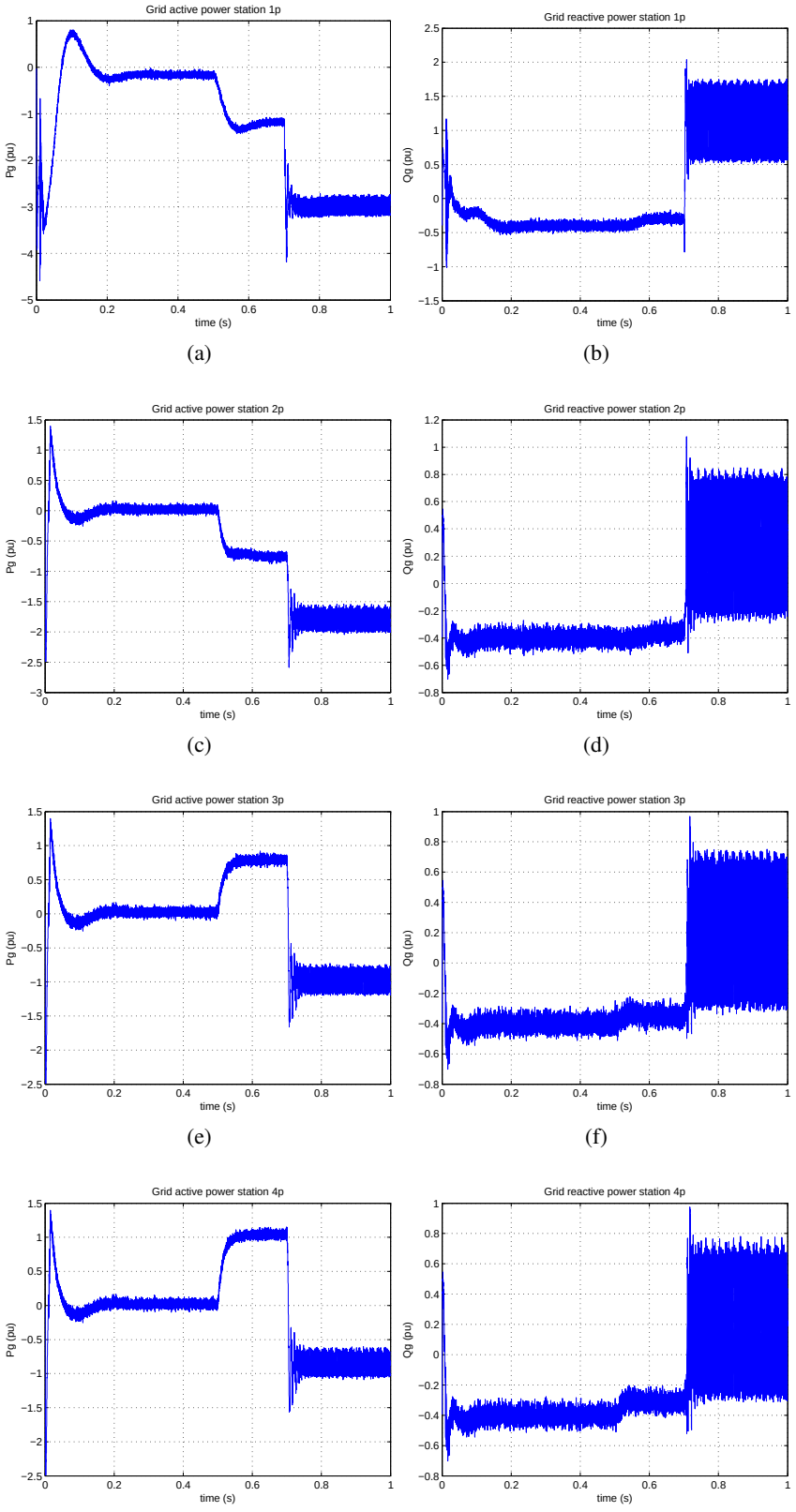
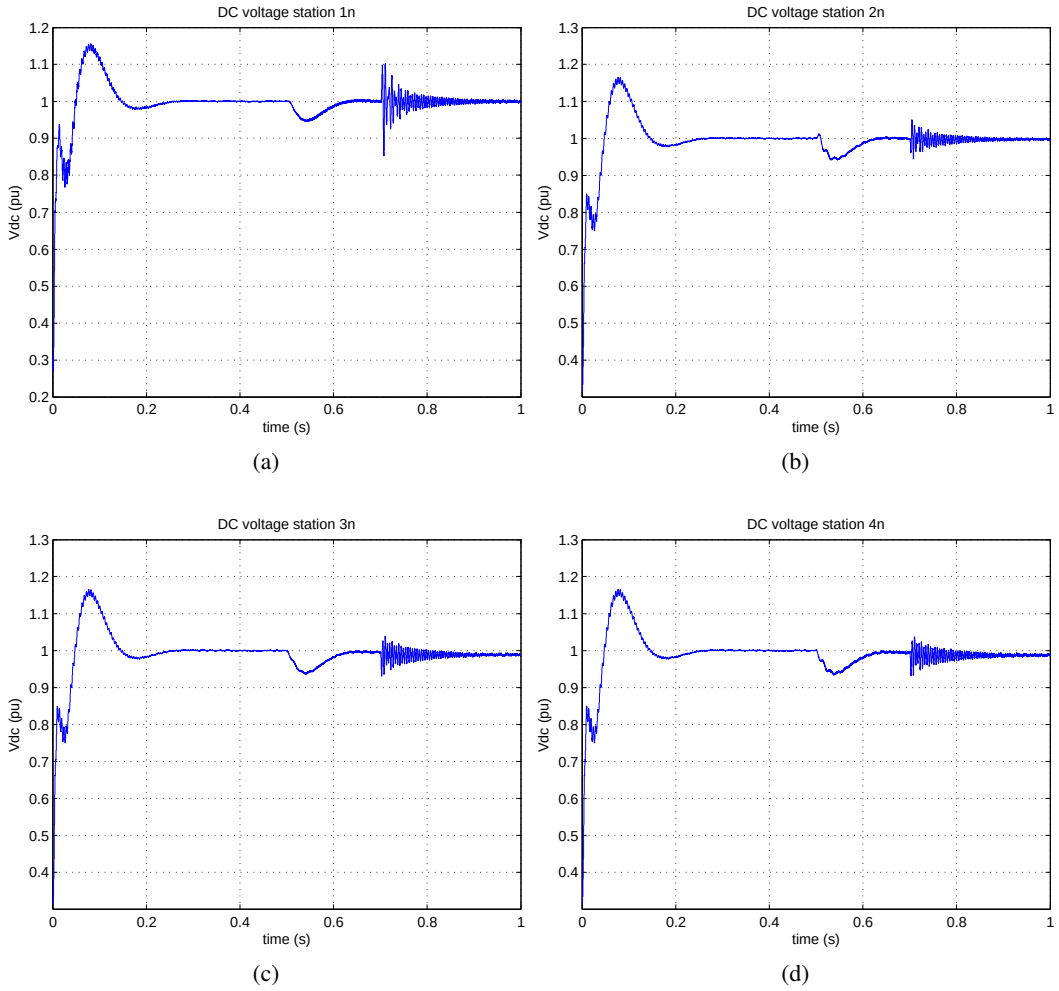


Figure A.24: Grid active and reactive power fault case 3 (49km from VSC2)

A.3 Bipole with metallic return: Current derivative fault detection (negative pole)



(a) (b) (c) (d)

Figure A.25: Negative pole VSCs DC Voltage level

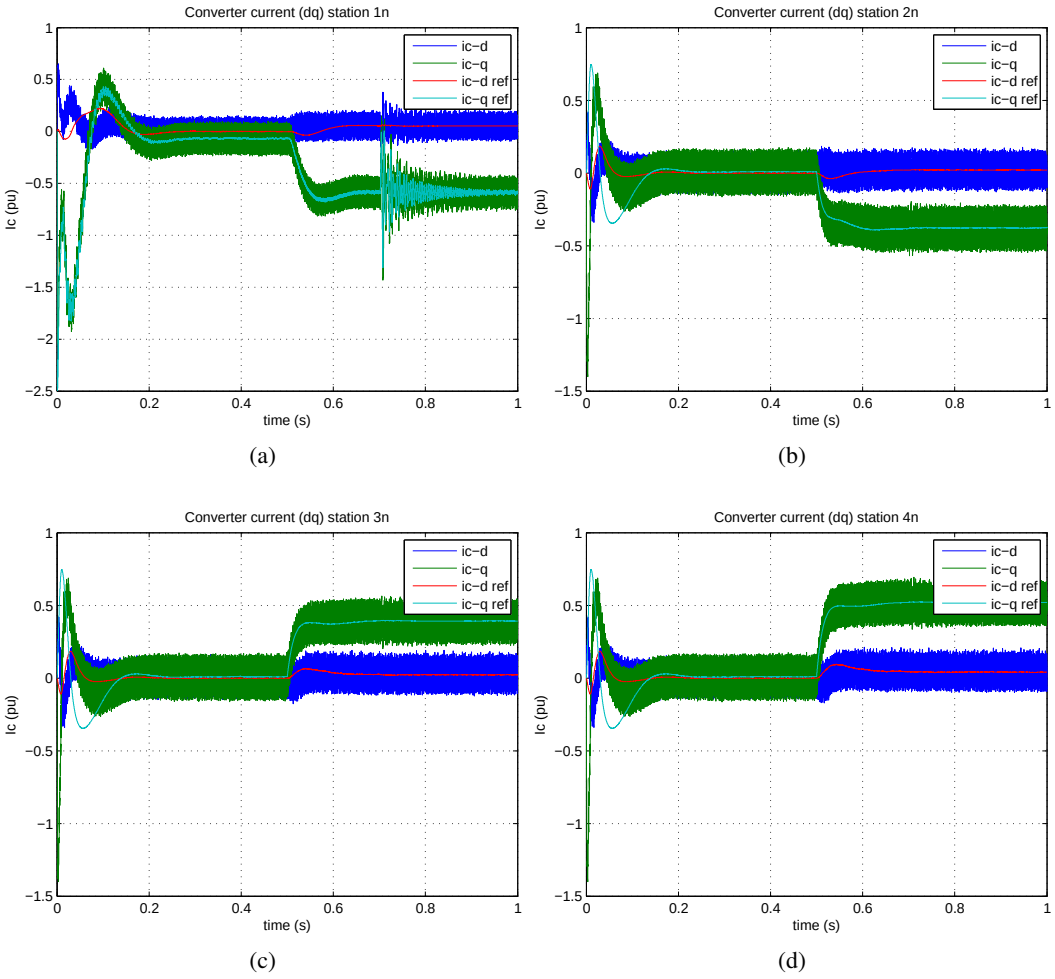


Figure A.26: Negative pole VSCs AC Current (dq)

A.4 Bipole with metallic return: Full Semiconductor DC Breakers (negative pole)

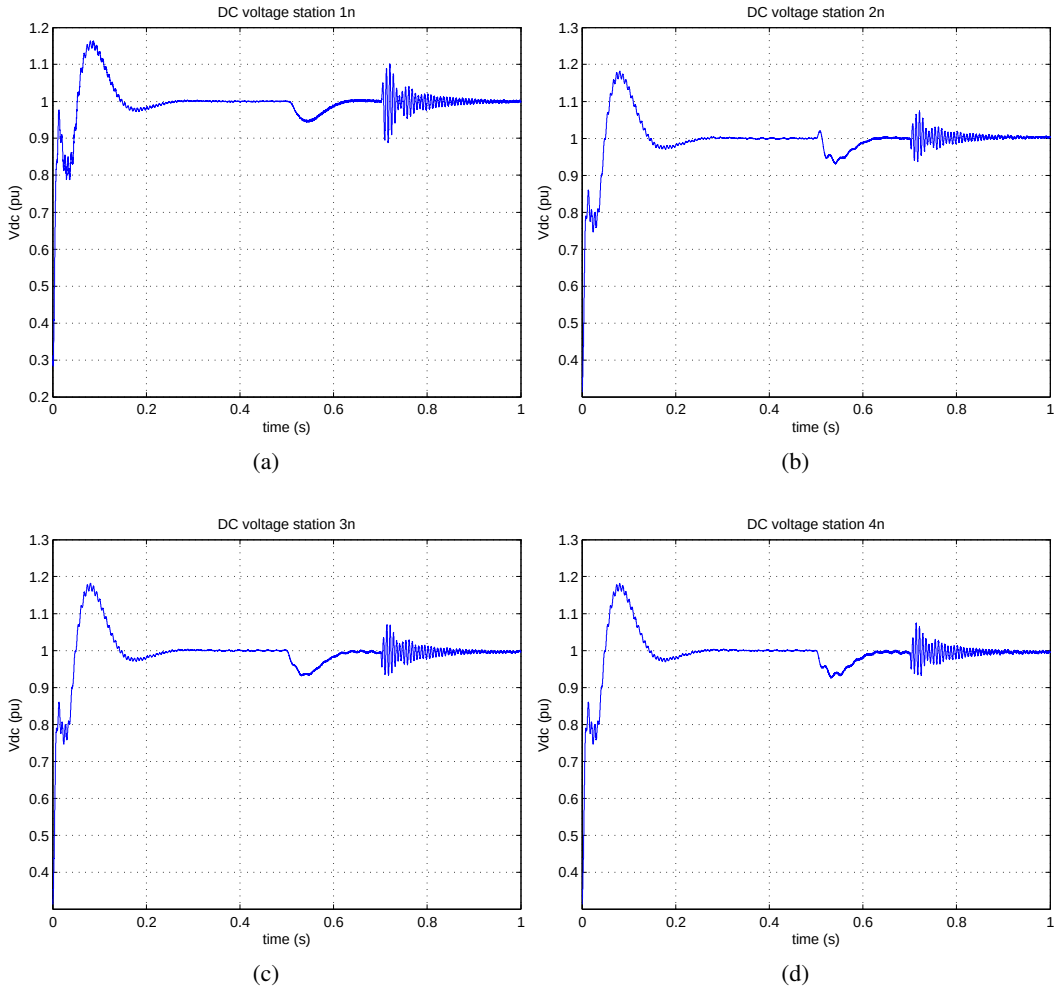


Figure A.27: Negative pole VSCs DC Voltage level in bipolar configuration with metallic return (Solid State DC breakers)

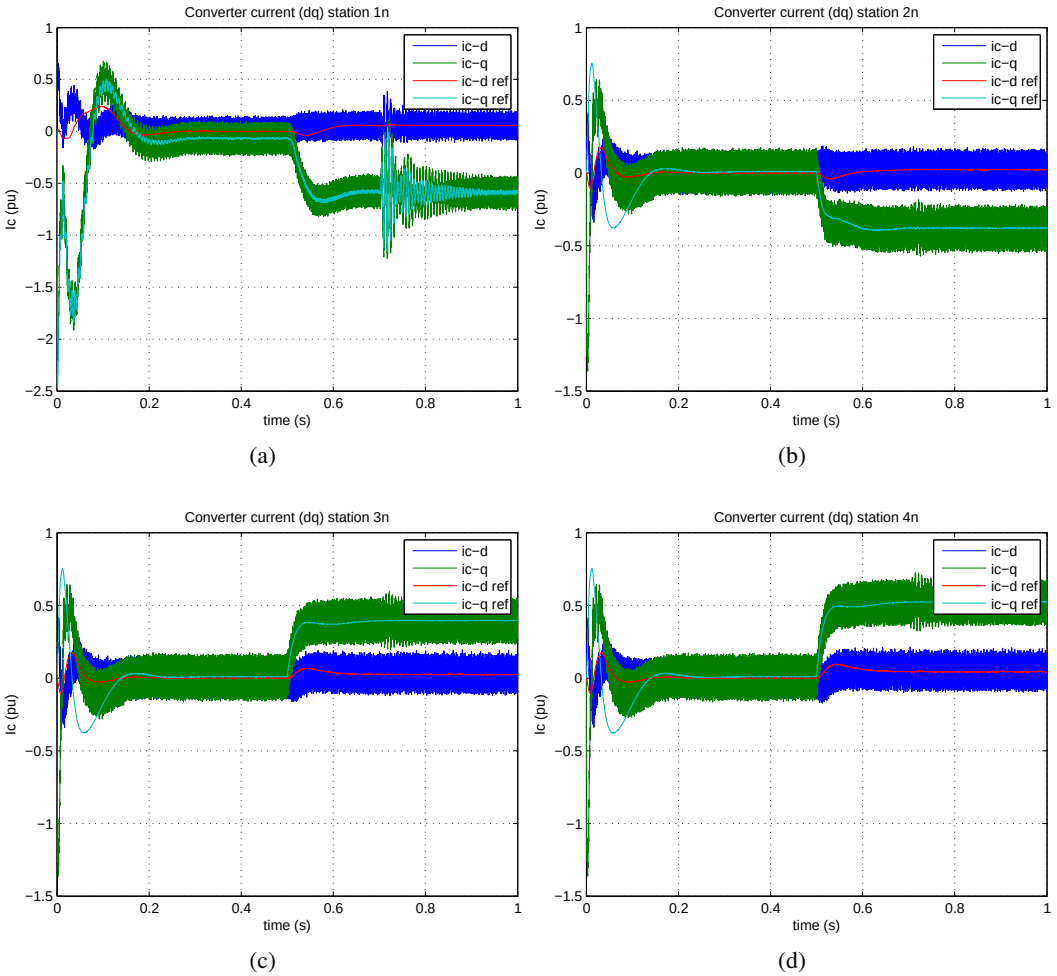


Figure A.28: Negative pole VSCs AC Current (dq) in bipolar configuration with metallic return (Solid State DC Breakers)

A.5 Bipole with ground return: Full Semiconductor DC Breakers (negative pole)

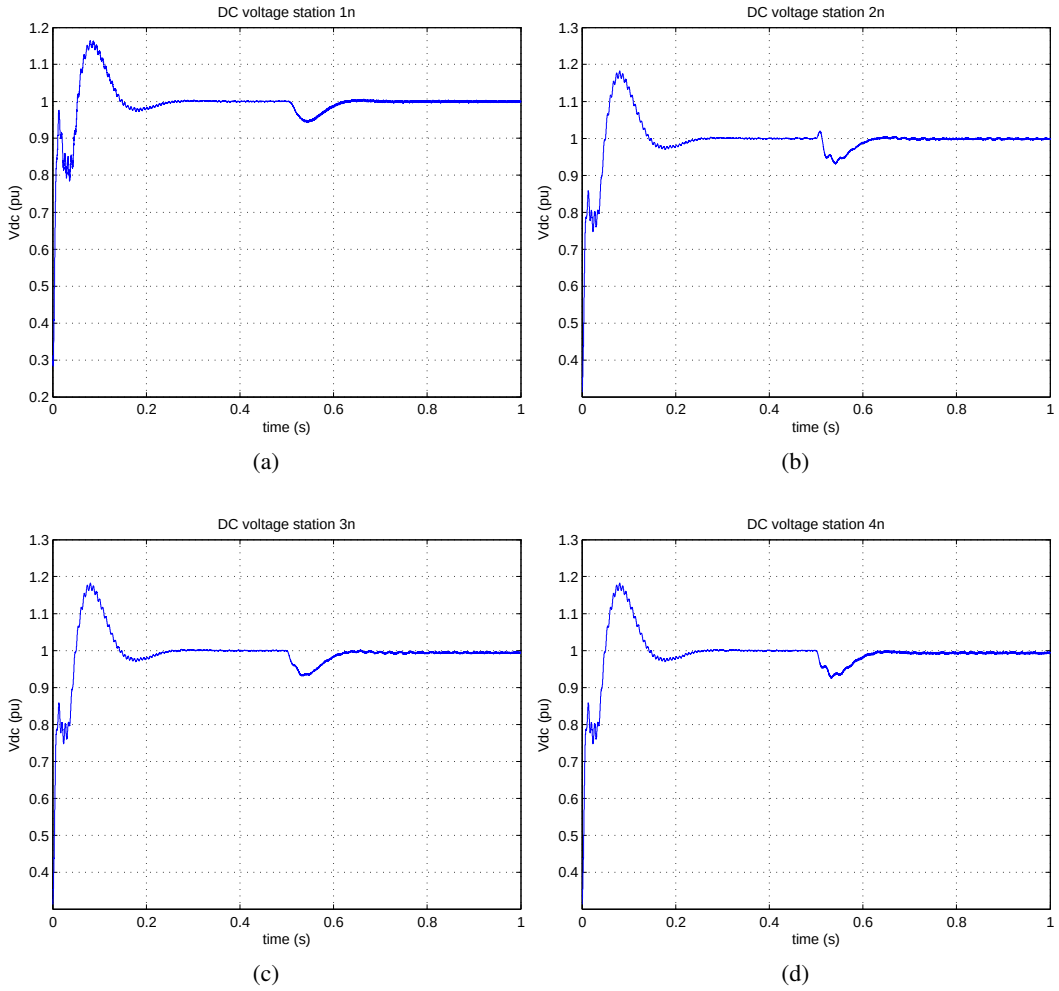


Figure A.29: Negative pole VSCs DC Voltage level in bipolar configuration with ground return (Solid state DC breakers)

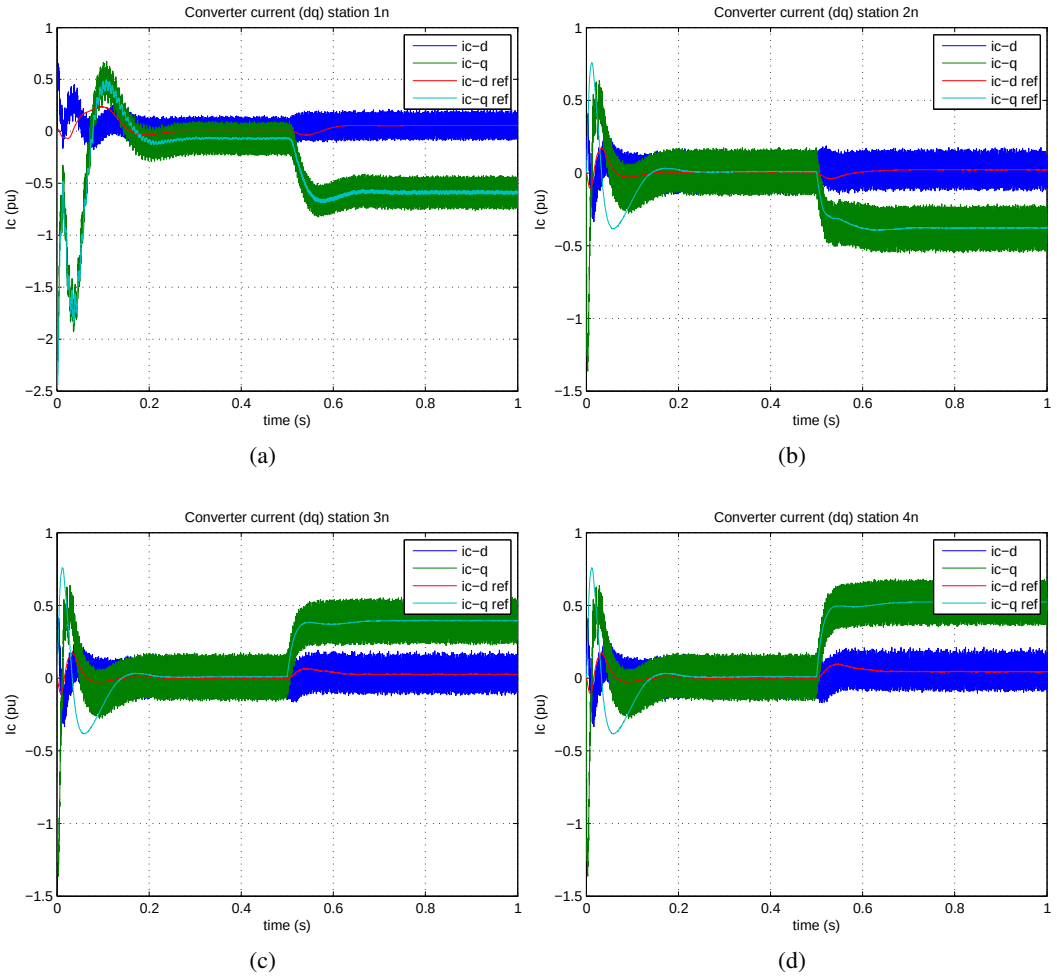


Figure A.30: Negative pole VSCs AC Current (dq) in bipolar configuration with ground return (Solid state DC breakers)

A.6 Symmetric Monopole: Normal Operation

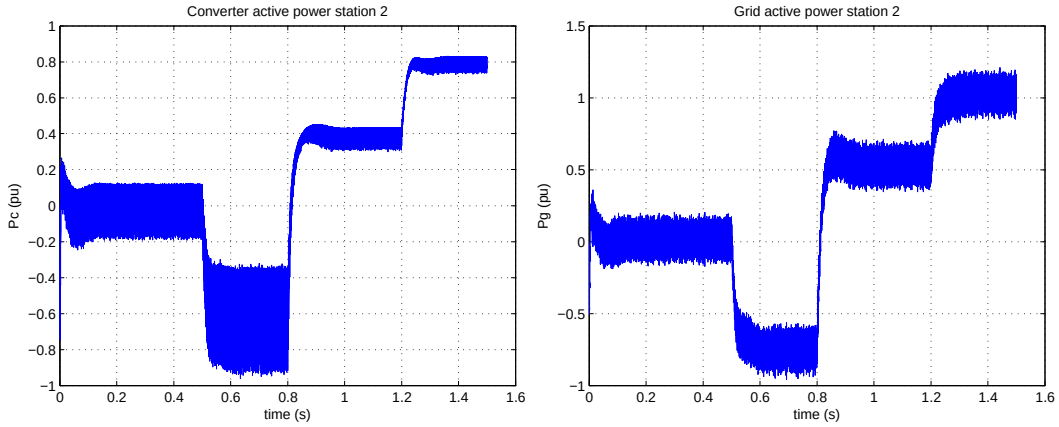


Figure A.31: VSC2 active and reactive power in normal operation

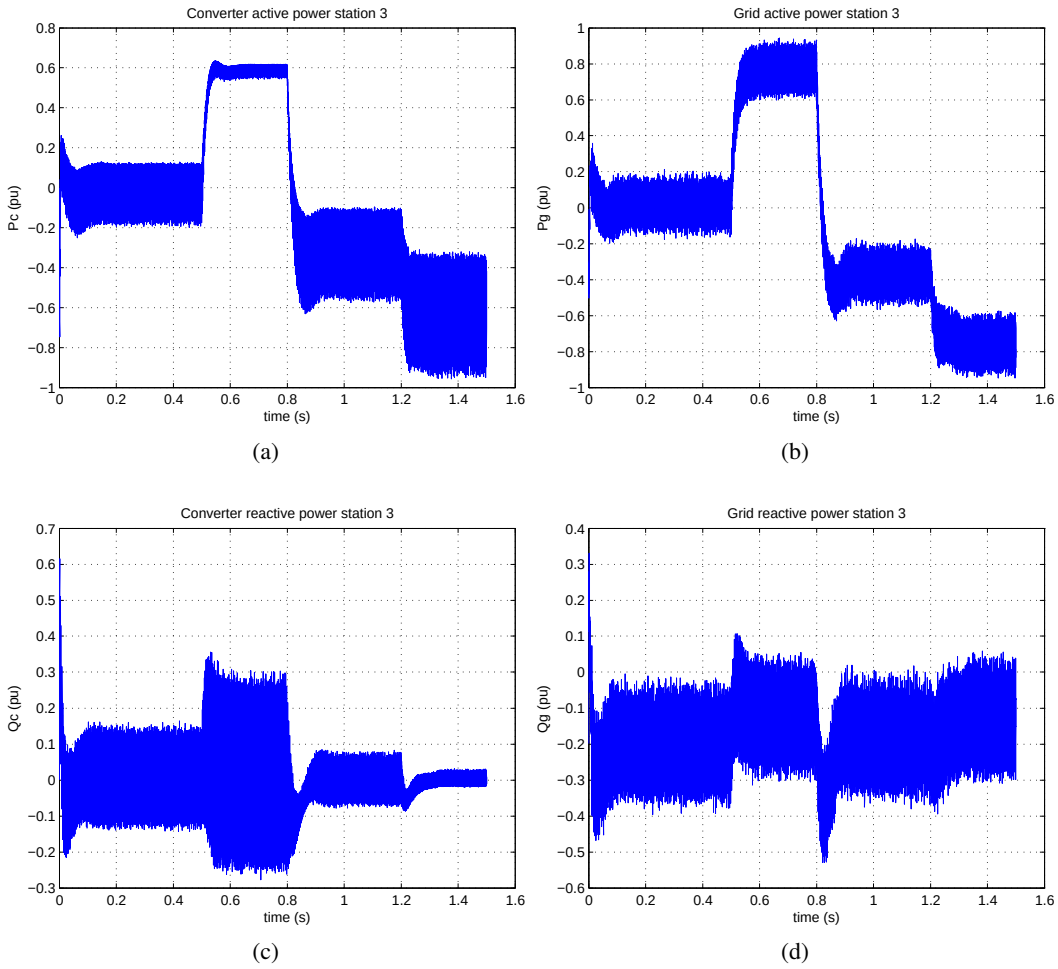


Figure A.32: VSC3 active and reactive power in normal operation

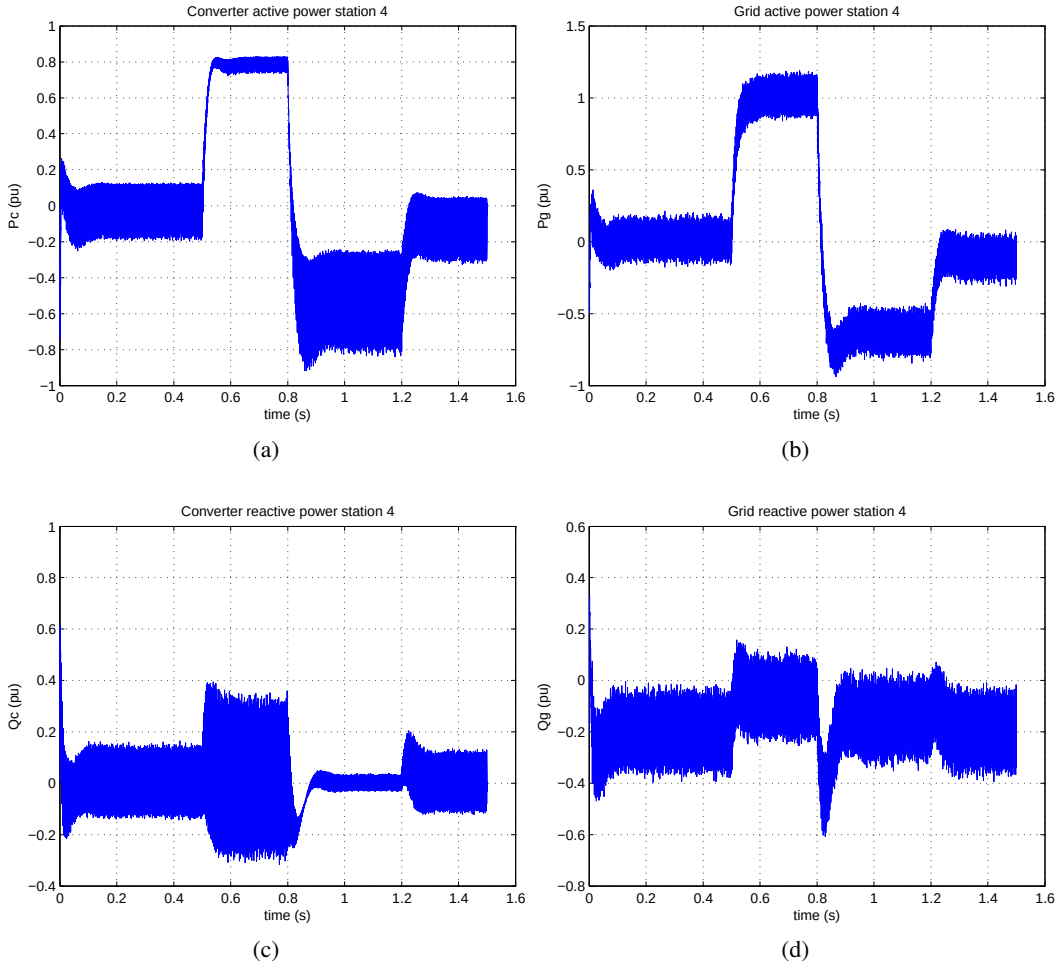


Figure A.33: VSC4 active and reactive power in normal operation

Appendix B

The Park or dq0 transformation was firstly introduced in 1929 by Robert H. Park [90]. It is primarily used in three-phase systems to simplify their analysis by transforming each three-phase quantity, in the abc-frame, into two DC quantities in the dq-frame. It has to be noted that there are two kinds of dq0-transformation, which can be used accordingly:

- The power invariant transformation, where $|X_{abc}| = \sqrt{2/3}\,|X_{dq}|$, is mainly used in machine analysis;
- The magnitude invariant transformation, where $|X_{abc}| = |X_{dq}|$, is used in control systems.

The Park transformation is performed in two steps. In this appendix, the power-invariant transformation steps are described. The first step is called the Clarke or $\alpha\beta0$-transformation and is used to perform a transition from the abc-coordinate frame to the $\alpha\beta0$-coordinate system. The Clarke transformation is described by the following equation:

$$x_{\alpha\beta0} = T \cdot x_{abc} \text{ with } T = \begin{pmatrix} \sqrt{2/3} & -1/\sqrt{6} & -1/\sqrt{6} \\ 0 & 1/\sqrt{2} & -1/\sqrt{2} \\ 1/\sqrt{3} & 1/\sqrt{3} & 1/\sqrt{3} \end{pmatrix} \tag{B.1}$$

The zero component is usually zero in balanced systems and thus it can be omitted in the second step.

The first step manages to reduce the dimensionality of the AC quantities, however, a new transformation to the dq-frame is necessary. In this way the stationary coordinate system $\alpha\beta$ is transformed into a synchronously rotating frame, which can be aligned to rotate with the voltage of the AC system. Due to the system rotation, the signals assume DC waveforms in steady-state conditions, simplifying the control of signals and systems [16]. The rotation transformation is given by:

$$x_{dq0} = R(\theta) \cdot x_{\alpha\beta0} \text{ with } R(\theta) = \begin{pmatrix} \cos\theta & \sin\theta & 0 \\ -\sin\theta & \cos\theta & 0 \\ 0 & 0 & 1 \end{pmatrix} \tag{B.2}$$

where $R^{-1}(\theta) = R^T(\theta) = R(-\theta)$ and θ is the AC system voltage angle. In case of a voltage source converter, the required AC grid angle value is provided by the phase-locked loop controller (PLL).

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Bibliography

[1] Asplund, G., "Sustainable energy systems with HVDC transmission," in *Power Engineering Society General Meeting, 2004. IEEE*, pp. 2299–2303 Vol.2, 2004.

[2] Meah, K. and Ula, S., "Comparative Evaluation of HVDC and HVAC Transmission Systems," in *Power Engineering Society General Meeting, 2007. IEEE*, pp. 1–5, 2007.

[3] Temesgen Mulugeta Haileselassie, "Control, Dynamics and Operation of Multi-terminal VSC-HVDC Transmission Systems," Master's thesis, Norwegian University of Science and Technology, 2012.

[4] ABB Group Media Relations, "ABB solves 100-year-old electrical puzzle new technology to enable future DC grid." Zurich, Switzerland, Nov. 7, 2012.

[5] Alstom Press Centre, "Alstom takes world leadership in a key technology for the future of very high voltage direct current grids." Feb. 21, 2013.

[6] Gunnar Asplund, Kjell Eriksson and Kjell Svensson, "DC transmission based on Voltage Source Converters," *CIGRE SC14 Colloquium in South Africa*, 1997.

[7] Rodrigues, S. and Pinto, R.T. and Bauer, P., *Dynamic Modeling and Control of Vsc-Based Multi-Terminal Dc Networks*. LAP Lambert Academic Publishing, 2012.

[8] Pinto, R.T. and Seta, P.L., *Dynamics and Control of VSC-based HVDC Systems: A Practical Approach to Modeling and Simulation*. LAP Lambert Academic Publishing, 2012.

[9] Candelaria, J. and Jae-Do Park, "VSC-HVDC system protection: A review of current methods," in *Power Systems Conference and Exposition (PSCE), 2011 IEEE/PES*, pp. 1–7, 2011.

[10] *Its time to connect (with offshore wind supplement)*. Rev 6, ABB AB Grid Systems HVDC, Ludvika, Sweden, 2010.

[11] Ake Carlson, "Specific requirements on HVDC converter transformers," *ABB Transformers AB*, 1996.

[12] Zhu, J. and Booth, C.D. and Adam, G.P. and Roscoe, A.J. and Bright, C.G., "Inertia Emulation Control Strategy for VSC-HVDC Transmission Systems," *Power Systems, IEEE Transactions on*, vol. 28, no. 2, pp. 1277–1287, 2013.

[13] Ackermann, T., *Wind Power in Power Systems*. Wiley, 2005.

[14] Giddani Kalcon and Grain P. Adam and Olimpo Anaya-Lara and Graeme Burt and K.L. Lo, "Analytical efficiency evaluation of two and three level VSC-HVDC transmission links," *International Journal of Electrical Power and Energy Systems*, vol. 44, no. 1, pp. 1 – 6, 2013.

[15] Jiuping Pan and Nuqui, R. and Srivastava, K. and Jonsson, T. and Holmberg, P. and Hafner, Y.-J., "AC Grid with Embedded VSC-HVDC for Secure and Efficient Power Delivery," in *Energy 2030 Conference, 2008. ENERGY 2008. IEEE*, pp. 1–6, 2008.

[16] Yazdani, A. and Iravani, R., *Voltage-Sourced Converters in Power Systems*. Wiley, 2010.

[17] Jiuping Pan, Reynaldo Nuqui, Le Tang and Per Holmberg, "VSC-HVDC Control and Application in Meshed AC Networks ," *IEEE-PES General meeting, Pittsburgh, Pennsylvania, USA.* , July 20-24, 2008.

[18] Akagi, H. and Watanabe, E.H. and Aredes, M., *Instantaneous Power Theory and Applications to Power Conditioning*. IEEE Press Series on Power Engineering, Wiley, 2007.

[19] Kundur, P. and Balu, N.J. and Lauby, M.G., *Power System Stability and Control*. EPRI power system engineering series, McGraw-Hill Education, 1994.

[20] Harnefors, Lennart and Nee, H-P, "Model-based current control of AC machines using the internal model control method," *Industry Applications, IEEE Transactions on*, vol. 34, no. 1, pp. 133–141, 1998.

[21] Kazmierkowski M.P., Krishnan R., Blaabjerg F. and Irwin J.D., *Control in Power Electronics*. Academic Press Series in Engineering, Elsevier Science, 2002.

[22] Zhang, Lidong, *Modeling and Control of VSC-HVDC Links Connected to Weak AC Systems*. PhD thesis, KTH, Electrical Machines and Power Electronics, 2010. QC20100607.

[23] Harnefors, Lennart and Bongiorno, M. and Lundberg, S., "Input-Admittance Calculation and Shaping for Controlled Voltage-Source Converters," *Industrial Electronics, IEEE Transactions on*, vol. 54, no. 6, pp. 3323–3334, 2007.

[24] Erik Koldby and Mats Hyttinen, "Challenges on the Road to an Offshore HVDC Grid," *Nordic Wind Power Conference 2009, Bornholm, Denmark.* , Sept. 10-11, 2009.

[25] Livermore, L., *Integration of Offshore Wind Farms Through High Voltage Direct Current Networks*. Cardiff University, 2013.

[26] *Its time to Connect Technical description of HVDC Light technology*. Rev 7, ABB AB Grid Systems HVDC, Ludvika, Sweden, 2012.

[27] Hydro-Quebec, TransEnergie Technologies, "SimPowerSystems For Use With Simulink." User's Guide Version 3, Online only.

[28] Power System Relaying Committee, "EMTP Reference Models for Transmission Line Relay Testing." WG report, Sep. 9, 2005.

[29] Mohamed Khatir, Sid Ahmed Zidi, "Comparison of HVDC line models in PSB/Simulink based on steady-state and transients considerations," *Acta Electrotechnica et Informatica Vol. 8, No. 2*, 2008.

[30] Bucher, M. K. and Walter, M. M. and Pfeiffer, M. and Franck, C.M., "Options for ground fault clearance in HVDC offshore networks," in *Energy Conversion Congress and Exposition (ECCE), 2012 IEEE*, pp. 2880–2887, 2012.

[31] Jin Yang, *Fault analysis and protection for wind power generation systems*. PhD thesis, University of Glasgow, 2011.

[32] Mallick, R. K. and Patnaik, R. K., "Fault analysis of voltage-source converter based multi-terminal HVDC transmission links," in *Energy, Automation, and Signal (ICEAS), 2011 International Conference on*, pp. 1–7, 2011.

[33] Franck, C.M., "HVDC Circuit Breakers: A Review Identifying Future Research Needs," *Power Delivery, IEEE Transactions on*, vol. 26, no. 2, pp. 998–1007, 2011.

[34] Greiner, C.J. and Langeland, T. and Solvik, J. and Rui, O.A., "Availability evaluation of Multi-Terminal DC networks with DC circuit breakers," in *PowerTech, 2011 IEEE Trondheim*, pp. 1–8, 2011.

[35] Jin Yang and Fletcher, J.E. and O'Reilly, J., "Short-Circuit and Ground Fault Analyses and Location in VSC-Based DC Network Cables," *Industrial Electronics, IEEE Transactions on*, vol. 59, no. 10, pp. 3827–3837, 2012.

[36] Lianxiang Tang and Boon-Teck Ooi, "Protection of VSC-multi-terminal HVDC against DC faults," in *Power Electronics Specialists Conference, 2002. pesc 02. 2002 IEEE 33rd Annual*, vol. 2, pp. 719–724 vol.2, 2002.

[37] Linden K. Jacobson B. Bollen MHJ. and Lundquist J., "Reliability study methodology for HVDC grids," in *Conference Proceedings, no. B4-108, CIGR 2010*.

[38] Red Penguin Associates Ltd, "Export transmission cables for offshore renewable installations Principles for cable routing and spacing." Revision 1.0Ł.

[39] Conseil international des grands rseaux lectriques B1, *Third-party Damage to Underground and Submarine Cables*. CIGR, 2009.

[40] Fujin Deng and Zhe Chen, "Design of Protective Inductors for HVDC Transmission Line Within DC Grid Offshore Wind Farms," *Power Delivery, IEEE Transactions on*, vol. 28, no. 1, pp. 75–83, 2013.

[41] Leelaruji, R. and Vanfretti, L. and Ghandhari, M. and Soder, L., "Coordination of protection and VSC-HVDC systems for mitigating cascading failures," in *Power System Technology (POWERCON), 2010 International Conference on*, pp. 1–8, 2010.

[42] Hatch Ltd, "The Lower Churchill Project - DC1210 - HVdc Sensitivity Studies." Muskrat Falls Project - CE-10 Rev. 1 (Public) - Final Summary Report.

[43] Jie Yang, Jianchao Zheng, Guangfu Tang and Zhiyuan He, "Characteristics and Recovery Performance of VSC-HVDC DC Transmission Line Fault," in *Power and Energy Engineering Conference (APPEEC), 2010 Asia-Pacific*, pp. 1–4, 2010.

[44] Bucher, M.K. and Franck, C.M., "Contribution of Fault Current Sources in Multiterminal HVDC Cable Networks," *Power Delivery, IEEE Transactions on*, vol. 28, no. 3, pp. 1796–1803, 2013.

[45] Junping Wang, Ah Choy Liew and Mat Darveniza, "Extension of dynamic model of impulse behavior of concentrated grounds at high currents," *Power Delivery, IEEE Transactions on*, vol. 20, no. 3, pp. 2160–2165, 2005.

[46] Predrag Pejovic in *Three-Phase Diode Bridge Rectifier With Low Harmonics*, Power Electronics and Power Systems, pp. 7–21, Springer US, 2007.

[47] Caliskan V., Perreault D.J., Jahns T.M. and Kassakian J.G., "Analysis of three-phase rectifiers with constant-voltage loads," in *Power Electronics Specialists Conference, 1999. PESC 99. 30th Annual IEEE*, vol. 2, pp. 715–720 vol.2, 1999.

[48] Meyer C., Schroder S. and De Doncker R.W., "Solid-state circuit breakers and current limiters for medium-voltage systems having distributed power systems," *Power Electronics, IEEE Transactions on*, vol. 19, no. 5, pp. 1333–1340, 2004.

[49] Sano, K. and Takasaki, M., "A surge-less solid-state dc circuit breaker for voltage source converter based HVDC transmission systems," in *Energy Conversion Congress and Exposition (ECCE), 2012 IEEE*, pp. 4426–4431, 2012.

[50] Jimmy Ehnberg and Thomas Nordlander, "Protection system design for MVDC collection grids for off-shore wind farms," tech. rep., Elforsk AB, Vindforsk-III, 2012.

[51] Jurgen Hafner, Bjorn Jacobson, "Proactive Hybrid HVDC Breakers - A key innovation for reliable HVDC grids," in *The Electric Power System of the Future - Integrating supergrids and microgrids, Cigr International Symposium Bologna (Italy)*, 13-15 September 2011 .

[52] Warne, D.F., *Newnes Electrical Power Engineer's Handbook*. Elsevier Science, 2005.

[53] Holaus, W. and Frohlich, K., "Ultra-fast switches- a new element for medium voltage fault current limiting switchgear," in *Power Engineering Society Winter Meeting, 2002. IEEE*, vol. 1, pp. 299–304 vol.1, 2002.

[54] Steurer M., Frohlich K., Holaus W. and Kaltenegger K., "A novel hybrid current-limiting circuit breaker for medium voltage: principle and test results," *Power Delivery, IEEE Transactions on*, vol. 18, no. 2, pp. 460–467, 2003.

[55] Pauli, B. and Mauthe, G. and Ruoss, E. and Ecklin, G. and Porter, J. and Vithayathil, J., "Development of a high current HVDC circuit breaker with fast fault clearing capability," *Power Delivery, IEEE Transactions on*, vol. 3, no. 4, pp. 2072–2080, 1988.

[56] D. Andersson and A. Henriksson, "Passive and Active DC Breakers in the Three Gorges-Changzhou HVDC Project," in *International Conference of Power Systems, ICPS, pp. 391395, Wuhan (China)*, 13-15 September 2001.

[57] Arora, R. and Mosch, W., *High Voltage and Electrical Insulation Engineering*. IEEE Press Series on Power Engineering, Wiley, 2011.

[58] Tore Martin Iversen, Sverre S. Gjerde and Tore Undeland, "High Reliable Multilevel Converter Topologies for a 10 MW, 100 kV Transformer-less Modular Offshore Wind Generator system," *EPE Joint Wind Energy and TD Chapters Seminar - Wind Energy Conversion*, 2012.

[59] Hans-Peter Nee and Lennart Angquist, "Perspectives on Power Electronics and Grid Solutions for Offshore Wind farms," tech. rep., Elforsk AB, Vindforsk-III, 2010.

[60] Flourentzou, N. and Agelidis, V.G. and Demetriades, G.D., "VSC-Based HVDC Power Transmission Systems: An Overview," *Power Electronics, IEEE Transactions on*, vol. 24, no. 3, pp. 592–602, 2009.

[61] Seyed Saeed Fazel, *Investigation and Comparison of Multi-Level Converters for Medium Voltage Applications*. PhD thesis, Technische Universitt Berlin, 2007.

[62] A. Lesnicar and R. Marquardt, "A new modular voltage source inverter topology," in *European Conference on Power Electronics and Applications (EPE), Toulouse, France*, 2003.

[63] Jacobson B. and Karlsson P. and Asplund G. and Harnefors L. and Jonsson T., "VSC-HVDC Transmission with Cascaded Two-Level Converters," in *CIGRE Conference Paris (France), Session B4-110*, August 2010 .

[64] Eicher, S. and Rahimo, M. and Tsyplakov, E. and Schneider, D. and Kopta, A. and Schlapbach, U. and Carroll, Eric, "4.5kV press pack IGBT designed for ruggedness and reliability," in *Industry Applications Conference, 2004. 39th IAS Annual Meeting. Conference Record of the 2004 IEEE*, vol. 3, pp. 1534–1539 vol.3, 2004.

[65] B. Jacobson, B. Westman and M. P. Bahrman, "500 kV VSC Transmission System for lines and cables," in *CIGRE 2012 San Francisco Colloquium (USA), Session B4-6*, March 2012.

[66] Friedrich, K., "Modern HVDC PLUS application of VSC in Modular Multilevel Converter topology," in *Industrial Electronics (ISIE), 2010 IEEE International Symposium on*, pp. 3807–3810, 2010.

[67] N. M. MacLeod, C. D. Barker, R. S. Whitehouse and W. Liang, "VSC HVDC Converter Design with Fault Blocking Capability for OHL Applications," in *EPRI HVDC FACTS Conference, Palo Alto (USA)*, August 2011.

[68] Merlin, M.M.C. and Green, T.C. and Mitcheson, P.D. and Trainer, D.R. and Critchley, D.R. and Crookes, R.W., "A new hybrid multi-level Voltage-Source Converter with DC fault blocking capability," in *AC and DC Power Transmission, 2010. ACDC. 9th IET International Conference on*, pp. 1–5, 2010.

[69] Alstom Grid, "THINK GRID Sharing Alstom Grid Innovation Practices." Issue 8.

[70] C.D. Barker, C.C. Davidson, D.R. Trainer and R.S. Whitehouse, "Requirements of DC-DC Converters to facilitate large DC Grids," in *CIGRE Symposium, Paris (France) B4-204*, August 2012.

[71] M. Davies, M. Dommaschk, J. Dorn, J. Lang, D. Retzmann and D. Soerangr, *HVDC PLUS Basics and Principle of Operation*. Siemens AG Energy Sector, Erlangen, Germany, 2011.

[72] Li, Yalong and Wang, Fred, "Analysis on Fault Current Stress for Power Switches in Modular Multilevel Converter Based DC System," 2013.

[73] Grain ADAM, Khaled AHMED, Nand SINGH, Stephen FINNEY and Barry WILLIAMS, "H-Bridge Modular Multilevel Converter (M2C) for High-Voltage Applications," in *21st International Conference on Electricity Distribution CIRED, Frankfurt (Germany)*, 2011.

[74] Adam G.P. and Ahmed K.H. and Finney S.J. and Bell K. and Williams B.W., "New Breed of Network Fault-Tolerant Voltage-Source-Converter HVDC Transmission System," *Power Systems, IEEE Transactions on*, vol. 28, no. 1, pp. 335–346, 2013.

[75] Zhai Jianyang, Ding Yifeng, Xu Bichuan and Li Yawen, "Wavelet and travelling wave based DC cable fault localization in MTDC," in *Environmental Electromagnetics (CEEM), 2012 6th Asia-Pacific Conference on*, pp. 206–209, 2012.

[76] Liu, Y. Sheng and G. Jiang, X. , "A Traveling Wave Fault Location Method for Earth Faults Based on Mode Propagation Time Delays of Multi-measuring Points," *Przegld Elektrotechniczny, ISSN 0033-2097, R. 88, nr. 3a, pp. 254-258*, 2012.

[77] Lianxiang Tang, *Control and Protection of Multiterminal DC Transmission Systems based on Voltage-Source Converters*. PhD thesis, McGill University, 2003.

[78] Lianxiang Tang and Boon-Teck Ooi, "Locating and Isolating DC Faults in Multi-Terminal DC Systems," *Power Delivery, IEEE Transactions on*, vol. 22, no. 3, pp. 1877–1884, 2007.

[79] ENTSO-E- European Network of Transmission System Operators for Electricity, "ENTSO-E Interconnected Network Grid Map."

[80] Oswald Mendrock, "Short-circuit current limitation by series reactors," *Energize*, pp. 45–49, 2009.

[81] Tamiru Woldeyesus Shire, "VSC-HVDC based Network Reinforcement," Master's thesis, Delft University of Technology, 2009.

[82] Alper etin, *Design and Implementation of a Voltage Source Converter based STATCOM for Reactive Power Compensation and Harmonic Filtering*. PhD thesis, Middle East Technical University, 2007.

[83] Mohan, N. and Undeland, T.M., *Power electronics: converters, applications, and design*. Wiley, 2007.

[84] Axelson, J., *Serial Port Complete: Programming and Circuits for RS-232 and RS-485 Links and Networks*. Lakeview Research, 1998.

[85] Pinto, Rodrigo Teixeira and Rodrigues, Slvio Fragoso and Wiggelinkhuizen, Edwin and Scherrer, Ricardo and Bauer, Pavol and Pierik, Jan, "Operation and Power Flow Control of Multi-Terminal DC Networks for Grid Integration of Offshore Wind Farms Using Genetic Algorithms," *Energies*, vol. 6, no. 1, pp. 1–26, 2012.

[86] D.M. Larruskain and I. Zamora and A.J. Mazn and O. Abarrategui and J. Monasterio, "Transmission and Distribution Networks: AC versus DC," in *9th. Spanish Portuguese Congress on Electrical Engineering. (9CHLIE), Marbella (Spain) 2005*, 2009.

[87] M.T. O'Brien and M. Zavahir, M. Clark, D. Boyle and P. Milosevic, "New Zealand Bipolar HVDC Earth/Sea Return Operation Environmental Experiences," in *Conference Proceedings, no. B4-206, CIGR 2006*.

[88] "Quality and Capacity Plan, Part II A, 2010-2016," tech. rep.

[89] Power Sub Working Group, The Green Grid, "Issues Relating to the Adoption of Higher Voltage Direct Current Power in the Data Center." White Paper 31.

[90] Park, R.H., "Two-reaction theory of synchronous machines generalized method of analysis-part I," *American Institute of Electrical Engineers, Transactions of the*, vol. 48, no. 3, pp. 716–727, 1929.