Systematic Design of EMI Resilient Negative-feedback Amplifiers

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Systematic Design of EMI-resilient Negative-Feedback Amplifiers

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Chapter 1

Introduction

According to Shannon [1], the information capacity of all electronic systems is constrained by three fundamental limitations: noise, bandwidth and signal power. For each of the three limitations the system has to be optimized. In a structured design process, functionality of the system is split into subsystems that can be optimized separately of each other.

Structured design methodologies concentrating on all three fundamental limitations have been developed for subsystems like negative-feedback amplifiers, oscillators, filters, bandgap references etc. [2]-[8]. All subsystems, and the electronic system as a whole, however, are also subjected to another limitation: interference from, and to other electronic systems.

Which interfering signals are present outside the system to be designed is in general unknown. The current trend of more numerous, more mobile, and more communicating electronic devices, increases the interference burden generally. It will be shown that the effect of interference can be modelled under very broad assumptions. This makes it possible to compute the effect of interference and design in such a way that its effect on the system is minimal. Another reason why interference is important and has to be taken into account during design is that the susceptibility to interference from other systems, and conversely the interference on other systems, is regulated by law.

An important subsystem of nearly all designs is the negative-feedback amplifier. The focus of this work will be on design methods to minimize the adverse effects of interference on negative-feedback amplifiers.

1.1 Electromagnetic Compatibility

Apart from realizing the intended functionality of an electronic system, the designer has to take care that it will not be affected adversely by external and internal interfering sources. On top of that, the designer should also take care that the circuit will not be a source of interference to other equipment. In other words, the designer has to realize adequate electromagnetic compatibility (EMC).

EMC is defined as *the ability of an electronic system to function properly in its intended electromagnetic environment and not be a source of pollution (interference) to that environment* [9]. When an electronic system is not capable of functioning properly in a given electromagnetic environment, electromagnetic interference (EMI) is encountered. EMI is defined as *any disturbance that interrupts, obstructs, or otherwise degrades or limits the effective performance of electronics/electrical equipment*[1].

EMI can be separated into three elements. First of all, a *source* of potentially interfering emission has to be present. Secondly, the emission has to be transported by some kind of *coupling* path before it can reach a *receptor* (the third requirement).

Emission can occur due to conduction and radiation. In case of conduction, interfering electrical signals are transported from a source to the equipment being disturbed by connected wires and cables. In the case of radiation, interfering signals are transported by electromagnetic fields; there is no need for a physical connection.

The immunity of a receptor is a measure of the amount of electromagnetic energy that may be coupled to it before its functionality is hampered. The opposite of immunity is susceptibility. Susceptibility is the inability of equipment to function properly in a certain electromagnetic environment. Immunity and susceptibility are often confused. The latter, however, is a fundamental property; it will always be possible to find or generate an electromagnetic environment that hampers the functionality of an apparatus [10].

Sources, receptors and coupling paths are not only found between different electronic systems, but also in the electronic system itself. The term *inter-system compatibility* is used when EMC between two or more systems is considered. *Intra-system compatibility* refers to EMC aspects within the system itself [10]. Figure 1.1 demonstrates the various levels of EMC. Inter-system compatibility is demonstrated by the arrows between systems I and II. Intra-system compatibility can be considered at different levels in a system. Between various devices in a system there has to be EMC, but also between the printed circuit boards (PCB) in the devices EMC has to be assured. EMC can even be considered at lower levels: the component level on the PCB and the component level in an integrated circuit.

In this work, the focus will be on the study of susceptibility problems. It is assumed that the source can't be controlled by the designer in case of inter-system incompatibility. Emphasis is placed on the coupling path and the receptor.

Total disregard of the coupling path during the design may result in large interfering signals reaching the receptor. This results in increased demands on the immunity. Design strategies to reduce the effectiveness of the coupling path as much as possible, thus relieving the immunity demands on the receptor, will be presented in Chapter 2. On top of that, design strategies to reduce the

[1] The International Electrotechnical Committee (IEC) has proposed to use 'interference' for the electromagnetic phenomenon that may degrade the performance of a device itself and 'disturbance' for the interfering signal that actually degrades the performance of a device. In this work this distinction will be followed.

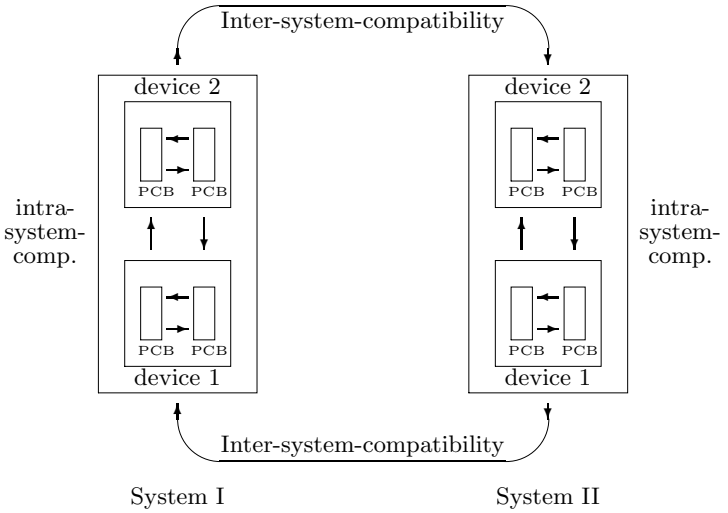


Figure 1.1: Inter-system compatibility and intra-system compatibility and EMC on various levels in the system. Every system, device, component etc. can both be a source and a receptor of EMI. The arrows represent the directions of possible interference.

susceptibility of the receptor, in this work the negative-feedback amplifier, as much as possible are also given. In effect, the problem of reducing susceptibility of the negative-feedback amplifier is extensively dealt with in Chapters 5 and 6.

The most obvious receptors are electronic devices, but also humans may be vulnerable to electromagnetic fields. For example, extremely low frequency fields may induce uncontrolled muscle movements and the experience of light flashes. Higher frequency fields will increase the temperature of tissue. The effects of electromagnetic fields on health will not be studied in this work. It is just mentioned for reasons of completeness. The interested reader is further referred to the literature, e.g., [11] or [12].

1.2 Possible sources of interference in hospitals

In private homes and offices the effects of interference can be annoying, but usually do not result in dangerous situations. Interference in hospitals can result in dangerous, life threatening situations. Therefore most hospitals restrict the use of mobile communications systems and ban them from operating theaters and intensive care units.

Most hospitals use a wireless internal communications system at this moment. Mobile communications using the terrestrial trunked radio (TETRA) standard in the 380-400 MHz band, walkie-talkie transmissions in the 450 MHz band, and

telemetry systems using the same band are well known sources of electromagnetic pollution [13]. Except for this, very little data is available on EMI measurement and characterization in hospitals. This is probably explained by the fact that characterization of one hospital complex could require 1 to 4 years to perform [13]. Therefore, measurements are often performed in a part of the hospital and in certain frequency bands [14][15]. A thorough study, however, does not seem to be available at the moment.

Hershey et. al [13] concluded from literature studies concerning field strengths in various hospitals that the electromagnetic field strength in the range 0.1-1000 MHz may vary considerably among hospitals. Maximum field strengths may vary between 0.4 V/m and 5.6 V/m. Unfortunately the studies are not always clear in specifying how the measurements were performed, e.g., if average or maximum values were recorded, what type of antenna was used, the polarization of the antenna, etc.

What came clear from this study from 1999 is a cluster of possible interfering fields in the range of 0.4-0.5 GHz and 0.8-0.9 GHz in most hospitals. This may correspond to telemetry systems used by the hospitals themselves and older generation GSM cell phones. Nowadays some clustering in the 1.8-2.4 GHz range may be expected due to more modern communication systems.

Some equipment used for diagnostic or treatment purposes use high frequencies and/or powers and may therefore generate interference themselves. These are unintentional emitters of electromagnetic fields. Two well-known potential sources of interference are magnetic resonance imaging (MRI) and diathermy (i.e., electrosurgery) equipment [15].

An MRI system is used to produce images of the inside of the human body. While doing this, strong electromagnetic fields with high frequencies are generated. These fields may interfere with systems for bio-potential measurements. More about the interference generated by an MRI can be found in Section 7.3 of Chapter 7.

Electrosurgery is a form of surgery in which high-frequency currents from 100 kHz to approximately 6 MHz [16] are used[2]. The application of such currents to human tissue results in a heating effect that is used to incise, destroy and remove tissue, and to seal blood vessels in order to maintain hemostasis [18][19].

The high-frequencies generated by electrosurgery equipment, coupled with the relatively high peak voltage of up to approximately 1 kV [18] during cutting, results in EMI problems in adjacent equipment. Electrocardiogram [20] and electroencephalogram [19] monitoring equipment may be especially hampered by electrosurgery equipment.

1.3 Examples of Electromagnetic Interference

If an electronic system is a too susceptible to the electromagnetic environment, its correct functioning may be hampered. The decrease in functionality may

[2]Different references specify somewhat different frequency ranges, e.g., [17] and [18] specify a range of 200 kHz to 3.0 MHz.

vary from hardly noticeable to complete malfunctioning. To get an idea of the effects of lack of immunity, some examples are given in this section. A distinction is made between EMI in medical and non-medical equipment, because EMI in medical equipment may result in life-threatening consequences, while in non-medical equipment the consequences may be bothersome but are often not life-threatening.

1.3.1 Examples of EMI in medical equipment

The past years showed an increase of reports that medical devices have failed to operate correctly because of interference from various emitters of high-frequency electromagnetic waves [21]. The consequences of these failures ranged from inconvenience to serious injuries and death. It appears that reasons for this problem are twofold: increasing numbers of electronically-controlled medical equipment that are susceptible to EMI and a significant increase in the number of EMI sources in the (hospital) environment.

For example, some apnea monitoring equipment failed to alarm when subjected to electric field strengths as low as 0.1 V/m in the FM broadcast band [22], while it should be able to withstand electric field strengths of at least 10 V/m, which is a regulatory demand for life supporting systems [23]. In the mid-1980s the US Food and Drug Administration (FDA) had become aware that approximately 60 infants died in the United States while being monitored for breathing cessation by one model of apnea monitor [21]. It was found that the devices failed to alarm because of EMI from mobile communication base stations several hundred meters away and FM radio broadcast stations more than one kilometer away.

Equipment for measuring bio-potentials like electrocardiogram (ECG), electroencephalogram (EEG), electromyogram (EMG), may be hampered by diathermy equipment [24]. Spikes may occur which may make it harder to interpret the measured bio-potentials. Sometimes the interference may even induce signals with larger amplitudes than the bio-potentials to be measured.

An additional problem area involves cardiac pacemakers and defibrillators. The dominant effect of EMI is loss of pacemaker adaptive control, causing the device to deliver stimuli either irregularly or at a preprogrammed fixed rate [21] so that the heart rhythm is not a function of the physical exertion to be delivered anymore. Also, pacemaker inhibition and/or asynchronous pacing are commonly observed when cellular phones are used up to distances of 23 cm [25].

Erroneous displays and latch-up of anaesthetic gas monitors during surgery have occurred [26]. Investigations revealed that interference from certain types of electrosurgery units disrupted the communication link between the monitor and a central mass spectrometer, causing the monitor to fail to display the concentration of anaesthetic gas in the operating room during surgery. Also, a type of anaesthetic gas monitor was found to present false measurement results when a C2000 communication system (using TETRA) was operated at 30 cm distance [27].

Magnetic resonance imaging (MRI) systems may generate so much interference that synchronizing the MRI system to the cardiac cycle in order to minimize artifacts in the image of the heart is very hard to do without taking special measures [28].

Detection of GSM signals in hearing aids results in disturbing signals with a frequency of approximately 217 Hz [29], which is in the audible range. Subjective perception of interference from handheld GSM telephones in hearing aids varies from barely perceptible to annoying and loud, starting when the phones are within one meter of the hearing aids and becoming louder when the phones are several centimeters away [21]. This makes it almost impossible for wearers of hearing aids to use GSM telephones.

Powered wheelchairs and scooters show susceptibility to electric fields in the frequency range of 1 MHz to 1 GHz and field strengths varying between 3 V/m and 40 V/m [30]. An electric field of 40 V/m seems very high, but since the wheelchairs are mobile it is not unlikely that the wheelchairs come in an environment where such a strong electromagnetic field exists.

There are reports of powered wheelchairs spontaneously driving off kerbs or piers when police vehicles, harbor patrol boats or amateur radios were used in the vicinity. When the EMI susceptibility was investigated, susceptibilities of the motion controllers of the wheelchairs were found in the range of 5 to 15V/m. At the lower end of the range, the electric brakes would release, which could result in rolling if the chair happened to be stopped on an incline; as the field strength at a susceptible frequency was increased, the wheels would actually begin turning, with speed being a function of field strength [26].

1.3.2 Examples of EMI in non-medical equipment

In principle all equipment may be disturbed by EMI. To limit the list, a few examples will be given. Most of them are adopted from [10] and [26], unless otherwise stated.

Radio-amateurs are familiar with complaints about their amateur radios interfering with television sets [31]. Unintentionally, their broadcasts may interfere with certain television channels. While broadcasting, they were also capable of controlling the room temperature because a type of electronic thermostat was too susceptible to the fields generated by the amateur radio station.

Radio broadcasts from the Dutch 'Wereldomroep' could be followed by listening to the telephone instead of the radio in some parts of the Dutch province Flevoland; the electronics in telephones acted as radio receivers[3]. The same kind of disturbance occurred near a medium wave transmitter in North London. New telephones installed in the neighborhood were constantly affected by BBC radio programmes.

In Germany, a particular make of car would stall on a stretch of Autobahn opposite a high power broadcast transmitter. Eventually that section of the

[3]Since 2007, the 'Wereldomroep' does not broadcast anymore from the Netherlands, but from other European countries [32]. This kind of EMI therefore probably does not occur anymore in Flevoland, but may occur at other places.

Autobahn had to be screened with wire mesh. Another type of car was equipped with a transmitter. When it was used, the central locking and electric sunroof would operate.

During the Falklands war the British HMS Sheffield was hit by a Exocet missile which damaged the ship (it sunk after several days). The radar was turned off because it interfered with the ship's satellite communications system.

EMI in aviation can become cumbersome. Between 1983 and 1996 over 97 EMI related events due to passenger 'carry on' electronic devices have been reported. Devices used by passengers, like phones, computers, CD players and video cameras may result in instrument or autopilot malfunction. Interference at airports has also been reported; interference to aeronautical safety communications at a US airport was traced to an electronic cash register a mile (1.6 km) away.

1.4 Regulations and standards

To prevent too much interference, governments provided early regulations about power levels that may be conducted or radiated and about susceptibility levels. For instance, as early as 1904 in the Netherlands the 'Telegraaf en Telefoonwet' was introduced [33].

Presently, most European countries (including the Netherlands) have adopted their national regulations from the recommendations of international committees, like the International Electrotechnical Committee (IEC) and the Comité International Spécial des Perturbations
Radioélectriques (CISPR). For the United States, the Federal Communications Commission (FCC) is responsible for regulations on interference.

In Europe regulations exist for both emission and susceptibility. Industrial, scientific and medical (ISM) equipment that does not use a form of radio communication is important because a lot of designs will have to comply with the standards of this group. As an example, emission and immunity levels of conducted disturbances are given in Table 1.1 and emission and immunity levels for radiated emissions are given in Table 1.2. The radiated emission levels have to be measured at a distance of 10 m from the source. More details regarding the measurement of emission and immunity levels can be found in [35]-[39]. Tables 1.1 and 1.2 were constructed using these standards[4].

Three different test levels are given for susceptibility measurements. The consequences of failure should be borne in mind in selecting the test level to be applied. Equipment may be used in a variety of locations, and therefore a variety of electromagnetic environments. The three different test levels correspond to three types of electromagnetic environments in which the equipment may have to function.

The three levels are defined as [35]:

[4]Since the regulations may change every few years, Tables 1.1 and 1.2 should be regarded as examples.

Table 1.1: Test levels regarding conducted emission and immunity to conducted disturbances of ISM equipment. See main text about levels.

	Frequency band (MHz)	dB (μV)
Conducted Emission levels	0.15 - 0.50	56 decreasing to 46
	0.5 - 5	46
	5 - 30	50
Immunity levels conducted disturbance	0.15 - 80	level 1: 120
		level 2: 130
		level 3: 140

Table 1.2: Test levels regarding radiated emission and immunity to radiated disturbances of ISM equipment. See main text about levels.

	Frequency band (MHz)	
Radiated Emission levels	30 - 230	30 dB (μV)
	230 - 1000	37 dB (μV)
	$>$ 1000	43.5 dB (μV)[34]
Immunity levels radiated disturbance	80 - 1000	level 1: 1 (V/m)
		level 2: 3 (V/m)
		level 3: 10 (V/m)

- Level 1 corresponds to a low-level electromagnetic radiation environment: levels typical of local radio/television stations located at more than 1 km, and transmitters/receivers of low power.

- Level 2 corresponds to a moderate electromagnetic radiation environment: low power portable transceivers (typically less than 1 W rating) are in use, but with restrictions on use in close proximity to the equipment. This is regarded to be a typical radiation level of a commercial environment.

- Level 3 corresponds to a severe electromagnetic environment: portable transceivers (2 W rating or more) are in use relatively close to the equipment but not less than 1 m. High power broadcast transmitters are in close proximity to the equipment and ISM equipment may be located close by. This is regarded as a typical industrial electromagnetic environment.

To simulate realistic, non-constant envelope interference, the immunity test signals specified in Tables 1.1 and 1.2 must be modulated with a 1 kHz sine wave at a modulation depth $m = 80\%$. Systems functionality may not seriously be hampered by these test signals. For the exact description of the amount of allowed functional deterioration and the description of the measurement set-up, the reader is referred to [40].

The standard for medical electrical equipment is comparable to the ISM standard and specifies an immunity to electromagnetic fields up to 3V/m in the 26-1000 MHz range [23]. Life supporting medical systems should even be immune to electromagnetic fields up to 10 V/m [23]. Before being put to market, compliance with the appropriate (medical) EMC standards of medical systems often has to be confirmed by a 'notified body', i.e., a test laboratory that is appointed by the government. In the Netherlands 'TNO Medical' and 'KEMA' are the most commonly known notified bodies.

Apart from the regulation regarding ISM equipment, medical equipment, and transmitters, there are many more regulations focussing on special product groups. The immunity and radiation demands may vary between different product groups. Treatment of all regulations are beyond the scope of this work.

In some situations more stringent emission or immunity limits are required. These limits can then be determined prior to the design and are called desirable requirements in contrast with the regulatory requirements.

As stated earlier, the type and level of interfering signals that may be expected is generally not known a priori due to the unknown electromagnetic field levels. Apart from measurements, the regulations, however, can be used to determine the EMC levels that the electronic system must comply with.

1.5 Determining EMC specifications

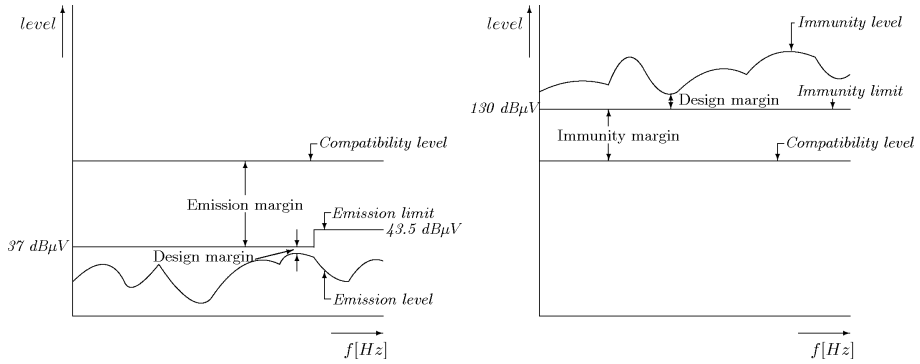
A system has to comply with both radiation and immunity regulatory/desirable requirements. To be safe, the design targets should be more restrictive than the requirements. Figures 1.2 (a) and (b) give a schematic that may be helpful to determine EMC specifications [10]. ISM regulatory emission and immunity requirements are indicated in figures 1.2 (a) and 1.2 (b), respectively.

First of all, a compatibility level is shown in both figures. This is the reference that can be used to come to emission and immunity levels in such a way that the system to be designed is EMC with all other equipment in the environment. The emission limit (Figure 1.2 (a)) is taken from the proper standard or should be chosen otherwise when the desired emission level is lower than the regulatory level. The designer has to make sure that the emission from his system is less than the emission limit. This can best be done by taking a design margin of 6 to 10 dB into account.

The immunity limit (Figure 1.2 (b)) is also taken from the proper standard or should be chosen such that interfering signal levels in the environment will always be less than the specified immunity limit. Again, a design margin of 6 to 10 dB ensures that the immunity level of the system will be adequate for that electromagnetic environment.

The design margin of 6 to 10 dB accounts for spread in component specifications that may influence EMC and also for variations in the EMC measurement set-up.

For an optimal design for EMC, the electromagnetic environment in which the system is going to be used has to be known prior to the design. The electromag-



(a) Emission. (b) Immunity.

Figure 1.2: Overview of EMC limits and margins. The designer has to make sure that emission levels remain below the emission limit (a) and the immunity level remains above the immunity limit (b).

netic environment, however, is not static. It may change with time. When the changes are not too severe (e.g., because equipment is added that complies to the emission regulations) the emission margin will decrease, but the compatibility level will most probably not be exceeded.

Unfortunately, it is impossible to foresee all future changes in the electromagnetic environment. A system that is designed to be immune to electromagnetic field strengths of 1 V/m can function satisfactorily in its environment, for example a room in a laboratory. However, if at a later date a radio transmitter is put to use in the direct neighborhood of the laboratory, it may cause the electromagnetic field to exceed 1 V/m and result in malfunctioning of the system.

The remainder of this work focuses on obtaining an adequate immunity. For reduction of emission levels, the interested reader is referred to the open literature, e.g., [41][42][34][43].

1.6 Origin of electromagnetic interference

Semiconductor devices, such as diodes and transistors, show a nonlinear behavior. Circuits realized with these devices will also show some kind of nonlinearity, even when they are supposed to be linear as in case of 'linear' negative-feedback amplifiers. The input-output relation of a nonlinear device like a transistor is given by:

$$i_o = u_i a_1 + u_i^2 a_2 + u_i^3 a_3 + \cdots + u_i^n a_n, \tag{1.1}$$

when u_i is the disturbing voltage at the input terminals (base-emitter or gate-source) of the nonlinear device and a_n are the Taylor series coefficients. The second-order term $u_i^2 a_2$ is in practice the main source of EMI, although higher

even order terms may also contribute to EMI. However, for practical nonlinear devices $a_4, a_6, \cdots$ increase less rapidly (or even get smaller) than a_2, while $u_i^4, u_i^6, \cdots$ decrease in value, since $u_i \ll 1\text{V}$ for nonlinear devices in amplifiers. The higher even order terms $u_i^4 a_4, u_i^6 a_6, \cdots$ are therefore (much) smaller than $u_i^2 a_2$, and may be neglected under certain conditions.

Nowadays, both analog and digital modulation are used. This classification, however, is on the basis of the modulating information being analog or digital. For determining EMI properties it is better to classify on the basis of the properties of the envelope of the high-frequency (ω_c) signal. Non-constant envelope modulation, constant envelope modulation, and constant envelope modulation that is periodically switched on and off can be distinguished. Both analog and digital modulation forms can be of the constant or non-constant envelope type.

Using Equation (1.1) and the mathematical description of the modulated interfering signal, the in-band detection can be determined. Table 1.3 gives the expressions of the detected current i_o for some modulation types. Voltage $\hat{u}_i$ will be defined in the next paragraph, $\hat{u}_c$ is the amplitude of the carrier wave.

Table 1.3: Overview of the detected (in-band) signal for some modulation types.

Modulation Type	Detected signal i_o (A)
Non-constant envelope AM	$a_2 \frac{\hat{u}_i^2}{2}\left(1+\frac{m^2}{2}\right) + a_2\hat{u}_i^2 m\cos(\omega_l)t + \frac{\hat{u}_i^2}{4}m^2\cos(2\omega_l)t$
Constant envelope FM, PM, FSK, etc.	$\frac{\hat{u}_c^2}{2}a_2$
'Switched' TDMA	$\approx a_2\hat{u}_c^2\left(\sum_{n=1}^{\infty}\frac{1}{n\pi}\sin(nT_1)\cos(n\omega_l t)\right) +$ $a_2\hat{u}_c^2\left(\sum_{n=1}^{\infty}\frac{1}{n\pi}(1-\cos(nT_1))\sin(n\omega_l t)\right)$

For illustration purposes, i_o is derived for an AM signal. The detected current for other modulation types can be determined using the same approach. An AM signal is mathematically described as: $u_i = \hat{u}_i[1 + m\cos(\omega_l t)]\cos(\omega_c t)$. Here, m is the modulation index ($0 < m \leq 1$), ω_c is the carrier frequency and ω_l the information frequency. Substituting u_i into the second term of Equation (1.1), it is found that the quadratic term generates signals at eight different frequencies, most of them being intermodulation products located near twice the carrier frequency [44]. There are also signals at DC, at the information frequency ω_l, and at $2\omega_l$. For negative-feedback amplifiers, it may often be assumed that the signals at ω_l, at $2\omega_l$, and possibly at DC, are in the pass-band and that ω_c and its harmonics and intermodulation products are not. The in-band disturbing signals can not be distinguished from the desired signal and may obscure it. The dominating disturbance is:

$$i_o = a_2\frac{\hat{u}_i^2}{2}\left(1+\frac{m^2}{2}\right) + a_2\hat{u}_i^2 m\cos(\omega_l)t + a_2\frac{\hat{u}_i^2}{4}m^2\cos(2\omega_l)t. \qquad (1.2)$$

Since $\hat{u}_i$ is smaller than 1 V and $m \leq 1$, the disturbing signal at $2\omega_l$ is at least four times smaller than the term at ω_l and may therefore often be disregarded. The direct current component may affect the integrity of the desired signal when DC is in the information band. However, since the disturbing signal at ω_l term is the largest, it will have the most detrimental effect.

Frequency modulation (FM), phase modulation (PM), frequency shift keying (FSK), and phase shift keying (PSK) are modulation methods resulting in carrier waves with a constant envelope, but with varying frequency resp. phase. The detected signal will be at DC only (see Table 1.3).

To make more efficient use of the available frequency spectrum, digital communication systems frequently use techniques like time division multiple access (TDMA) and frequency division multiple access (FDMA). TDMA is used by the global system for mobile communications (GSM) standard. TDMA uses short bursts of carrier wave interleaved by longer periods of silence, i.e., the carrier is switched on and off. Each phone has a time slot T_1 to transmit its message. If a time frame T has passed, the phone may transmit again [45]. Table 1.3 shows that pulses are detected, with T_1 being expressed in fractions of π, where T is equivalent to the full 2π radians of the sinusoid (the DC-term has been omitted, because it depends strongly on T_1.). For instance, in case of GSM, $T_1 = \frac{\pi}{4}$ s and $\omega_l = 1361.47$ rad/s (216.68 Hz). Table 1.4 presents an overview of some wireless communication systems using periodically on-off switching.

Table 1.4: Overview of some legal wireless communication standards using periodically on-off switched constant envelope waves [45][46].

	Frequency band (MHz)	P_{max} (W)	Modulation type	T_1 (μs)	T (ms)	det. $f_{fund.}$ (Hz)
C2000/ TETRA	380 – 400	3	FDMA, TDMA (π/4DQ)-PSK	14167	56.667	17.65
GSM-900	870–960	2	FDMA, TDMA	577	4.615	216.68
GSM-1800	1710–1880	1	FDMA, TDMA	577	4.615	216.68
DECT	1880–1900	0.25	FDMA, TDMA	417	10.000	100.00

The GSM standard also uses FDMA. Per time-frame the communication may switch to another channel [45]; a higher or lower frequency. This frequency shift is relatively small compared to the mean frequency, so this frequency 'hopping' is expected to give minor EMI effects compared to TDMA. Other digital communication standards like C2000/terrestrial trunked radio (TETRA) and digital enhanced cordless telecommunications (DECT) also use TDMA or FDMA.

The universal mobile telecommunications system (UMTS) is used to deliver multimedia services to the user in the mobile domain [47]. It uses wideband code division multiple access (W-CDMA) as radio transmission technology. Two transmission duplex techniques are used in UMTS, frequency division duplex (FDD) and time division duplex (TDD) [48]. Within the TDD operation, a transmission is split into 10 ms radio frames [47][48] which may be detected and result in interference with a frequency of 100 Hz.

Bluetooth is a short range (0-10m) wireless link technology aimed at replacing cables that connect phones, laptops, etc. [49]. It uses modulation types like Gaussian frequency shift keying (GFSK), time division multiplexing (TDM) and frequency hopping with 1600 hops/s. The latter may cause detection to occur [50], because the interference is not present at just one frequency, but at many frequencies.

Wireless local-area network (LAN) (IEEE 802.11a and g) and ultra wideband (UWB) use (orthogonal) frequency division multiplexing ((O)FDM) [50][51]. OFDM is a technique for transmitting data in parallel using a large number of modulated carriers with sufficient spacing so that the carriers are orthogonal. (O)FDM signals have a finite message length that depends on the data rate. Consequently, frame frequencies in the range from 363 Hz and 2.1 kHz can be expected, which may be detected [50], causing interference.

The term UWB usually refers to a technology for the transmission of information spread over an (-10 dB) operating bandwidth exceeding 500 MHz or 20 % of the center frequency [52]. Different UWB technologies are used. The first is classical impulse radio technology [53], which is an on-off switching of the ultra wide band signal. Its interference effect can be analyzed using the third equation given in Table 1.3. The earlier mentioned OFDM technology is the second technology. Two modulation schemes, multiple carrier OFDM and pulsed direct sequence code division multiple access (DS-CDMA) are used. Interference effects comparable to that of wireless LAN and Bluetooth can be expected [50]. The third technology that is used, is UWB-FM using a low emission level (-41.3 dBm/MHz)[54]. It uses double FM: a low-modulation index digital FSK followed by a high-modulation index analog FM is used to create a constant envelope UWB signal [55]. Hence, a DC-shift may be expected resulting from UWB-FM interference.

Table 1.5 presents an overview of legal transmitters in the Netherlands. It shows a variety of modulation types, transmitting power, and frequencies used. What interference source will be dominating depends on the circumstances. If equal amplitude of the interfering signal is assumed, constant envelope modulation (e.g., FM) is expected to result in less disturbance than the other modulation types. Amplitude modulated and on-off switched interference are expected to result in comparable values of disturbance. In the following chapters of this work, interfering signals will therefore be assumed to be AM for reasons of simplicity.

Note that non-intentional sources of interference may also cause EMI due to envelope detection[5] while having relatively low values of ω_c, e.g., MRI and

[5]In the remainder of this work EMI may be used as an abbreviation for envelope detection.

Table 1.5: Some legal transmitters in the Netherlands [56]. The maximum allowed power in AM-broadcasting depends on the licence. Maximum power (Radio 747 AM) is listed.

	Frequency band (MHz)	P_{max} (W)	Modulation type
Broadcast	0.15–26.1	$<$ 500 kW	AM
Amateur band	10.10–10.15	400	FM
Amateur band	10.10–21.45	400	AM
Amateur band	21.00–10.15	400	AM
Paging systems	26.1, 26.8875–26.9125	5W, 0.5	FSK
Amateur band	50.00–50.45	120	AM, FM
Broadcasting	87.5–108	$\leq$ 200 kW	FM
Amateur band	144–146	400	FM
Telemetry	433.05–434.79	10m	FM
Amateur band	430–440	400	FM
Bluetooth	2402–2480	0.1	GFSK, TDM, frequency hopping
Wireless LAN	2400–2483.5 [49][51] 5150–5825 [54]	0.1 1	(O)FDM
UWB	3800–8500 [56]	-41.3 dBm/MHz	(O)FDM, FM
UMTS	1899.9–2164.7 [56]	0.125–0.250	W-CDMA, [47] FDD, TDD [48]

electrosurgery equipment.

1.6.1 Additional circumstances affecting interference

The discussion so far has concentrated on the properties of the envelope of the interfering signal. Besides the envelope being constant or not, the received power of the interfering signal affects the amplitude of the disturbance. The received power depends on the distance between source and emitter and the efficiency of the transfer from the electromagnetic field to an interfering signal at the input of a nonlinear device. Usually wires and cables (interconnects) attached to the receptor behave like an antenna. The efficiency of the antenna behavior depends on the length of the wires and the orientation to the electromagnetic field. Besides the antenna behavior of the wires, the local field strength at the receptor is of importance. In practice, it is an important quantity as it is relatively easy to measure and it is also used in standards and regulations. The electromagnetic field strength (in the far field) can be approximated with [10]:

$$E = \sqrt{\frac{Z_0 P G}{4\pi r^2}}, \tag{1.3}$$

with E being the electric field component, Z_0 the wave impedance of $120\pi\ \Omega$, P the transmitted power, G the antenna gain and r the distance between source and receptor. EMC engineers often assume a G of 1.64 (i.e., antenna gain of a half-wavelength antenna) when approximating the expected E-field.

Usually the distance between radio transmitters in, for instance, the AM or FM bands are located several tens or even hundreds of kilometers from the receptor. At these large distances the chance of interference may be acceptably low. That is, however, not always the case as was shown in a few examples in Section 1.3.

Nowadays, transmitters can also be found at relatively small distances from receptors. For example, an increasing number of homes, offices, and hospitals are equipped with some kind of mobile wireless communication system like WLAN or DECT, etc. Personal communication systems are also widely used (GSM and UMTS). Due to the mobility of the transmitter of these communication systems, it may come in close proximity to a receptor and, despite the low transmission power ($<$ 3W, see Table 1.4), interfere with it. Users of GSM cell phones, for instance, cause an audible disturbance when operating at a small distance from an audio system.

1.7 Negative-feedback amplifiers

Electronic systems are widely used to transport and condition information from a source to a destination. The source may, e.g., be any kind of sensor transferring a physical quantity to an electrical current or voltage. The destination usually is a transducer transferring an electrical voltage or current to another physical quantity.

The information may be processed while being transported from source to load. This processing may be done in a digital as well as in an analog way. Nowadays, most of the signal processing is done digitally. The information exchange between sensor and the system, however, is always analog and will remain analog in the future. The load may be analog or digital.

This analog part usually involves some kind of amplification or filtering function. Since amplification is perhaps the most basic electronic function, a linear negative-feedback amplifier is assumed for the analog part of the electronic system in this work. The goal of (negative-feedback) amplifiers is to increase the energy level of information by multiplying it with a constant. While doing so, the fidelity of the transfer from input to output of the amplifier has to be assured. Using a systematic design approach [2][3], this is accomplished by orthogonalization.

Firstly, the source and load are characterized. Usually the information is best represented by either a voltage or a current. The source impedance is usually not accurately known and might even be nonlinear. By assuring that the amplifier does not significantly load the source, these inaccuracies and nonlinearities do not appear in the transfer. If the load is also nonlinear or an inaccurately known impedance, the correct choice (i.e.,voltage or current) for driving this impedance with maximum signal fidelity has to be made. From this characterization the

required type of negative feedback follows.

The active part of the amplifier consists of components that are capable of increasing the energy level of a signal, i.e., transistors. Transistors are inherently nonlinear devices and measures have to be taken to realize a linear transfer. This may be accomplished by realizing the negative feedback using a linear resistor network.

The next step in the design process is to optimize the input stage for noise behavior and the output stage for preventing clipping distortion. Then the bandwidth is designed to meet the specifications. The complete design process and at what stage EMI aspects enter the design process are extensively dealt with in Chapters 5 and 6.

1.7.1 A classification of errors in negative-feedback amplifiers

The information handling capacity of negative-feedback amplifiers is constrained by three fundamental limitations: noise, signal power, and bandwidth [3].

The three fundamental limitations lead to deviations from the intended output signal. Sometimes deviations from the intended output signal are called noise. Noise is, however, too narrow a term. Because of the different origin of the deviations and the (orthogonal) design steps that can be taken to minimize them, the term error will be used instead of noise. Noise will be used for errors that are stochastic in nature.

Apart from these fundamental limitations, errors generated by interference exist and they also negatively affect the information handling capacity of negative-feedback amplifiers. For convenience, a classification of the errors and an indication if, and how, it is possible to minimize the errors from various origins is given. The errors given all occur at the same time (except perhaps interference) and may interact. Chapter 5 will present methods for minimizing the errors.

A. Errors due to noise

Noise is caused by stochastic processes in the circuit. Errors due to noise can be divided into:

- signal amplitude independent noise
- signal amplitude dependent noise

Thermal noise comes from thermal agitation of electrons in resistive material and is an example of signal independent noise. The spectral noise density for thermal noise is given by the equation $S_{u_{th}} = 4kTR$, where k is Boltzmann's constant, T is the temperature in kelvin, R is the resistance, and S is the spectral density. Thermal noise is also called Johnson or white noise in literature [9] and has a Gaussian distribution.

When noise depends on biasing conditions, it may also be signal dependent due to small changes in the biasing due to the input signal. Some examples of

these signal dependent types of noise are: shot noise, excess noise, and burst noise.

Shot noise is associated with the uncertainty in a current of charge carriers crossing a potential barrier, e.g., a p-n junction. The spectrum of this source is given by $S_i = 2qI$, where q is the electron charge and I is the barrier current. The spectrum is flat as long as the transition time of the charge carriers is small with respect to the reciprocal value of the frequency. Shot noise has a Gaussian distribution.

Every imperfect contact between two materials, such as switches and relay contacts, but also carbon resistors and transistors show a noise component that depends on the frequency [3][9]. This noise contribution is called excess noise and is due to the statistical variations in the conduction, due to an imperfect contact between two materials or due to generation and recombination processes at the surface in semiconductor materials. The power density of these noise sources is inversely proportional to the frequency. That is why excess noise is often called $1/f$-noise. It is described as $S_i = K_1 I^a \frac{f_l}{f^b}$. The noise corner frequency f_l is of importance because at this frequency the excess noise is equal to the white noise. K_1 is a constant for a particular device, a is a constant in the range 0.5 to 2, b is a constant of about unity [57] and I is the current.

Burst noise, also called popcorn noise, is found in some integrated circuits and discrete transistors. The source of this noise is not fully understood, although it has been shown to be related to the presence of heavy-metal ion contamination [57]. Gold-doped devices show very high levels of burst noise. The spectral density of burst noise is of the form $S_i = K_2 I^c \frac{1}{1+(\frac{f}{f_c})^2}$. K_2 is a constant for a particular device, I is the bias current, c is a constant in the range 0.5 to 2 and f_c is the particular frequency for a given noise process. Burst noise is so named because an oscilloscope trace of this type of noise shows bursts of noise on a number (two or more) of discrete levels. The repetition rate of the noise pulses is usually a few kilohertz or less. If it is amplified and fed into a loudspeaker, it sounds like corn popping, with thermal noise providing a background frying noise, thus the name popcorn noise [9].

In properly designed negative-feedback amplifiers, current changes due to the input signal amplitude will not significantly change the bias conditions. But even when the input signal modulates the bias current up to 100 %, the noise is affected by (less than) only 2 dB. Signal dependent noise may therefore be neglected. The mean noise contribution is thus determined by the bias current. An exception may be a negative-feedback amplifier having a class-B stage as active part. For a class-B amplifier the current through the active device and therefore the shot noise is directly related to the signal level [7].

In linear, time-invariant (negative-feedback) amplifiers all noise sources generated by the transistors and feedback resistors can be transferred to an equivalent noise source at the input. When the amplifier is properly designed, the input stage of the amplifier has a much larger contribution to the equivalent noise source than the subsequent stages. From the equation giving the equivalent noise source, the optimal biasing current of the input transistor can then

be calculated [3]. The value(s) of the feedback resistor(s) are determined from both amplification and noise constraints.

B. Errors due to input signal power

When a signal is applied to an amplifier, errors due to distortion may occur. Characteristic for distortion is that frequency components can be found at the output that are not found in the input signal. Two types of distortion can be identified: weak and strong nonlinear distortion. Weak nonlinear distortion originates from the nonlinear device transfers; strong nonlinear distortion from clipping.

Input signals with a small amplitude may cause weak nonlinear distortion (Equation (1.1)). Strong nonlinear behavior resulting in clipping distortion is found when signals are that large that they no longer fit between the supply rails or the current driving capability of a stage is not sufficient [7]. As for an increasing input signal the output signal no longer increases, the signal which is fed back no longer changes and consequently the negative-feedback loop is broken. This severe type of distortion results in loss of information.

The errors due to the input signal can therefore be divided into errors resulting from:

- signals with small amplitude
- signals with large amplitude

Weak nonlinear distortion can be minimized by ensuring a small enough input signal is being applied to the active device(s). By ensuring enough loop gain this input signal can be made sufficiently small. Appropriate biasing of the amplifying stages is also beneficial for low weak nonlinear distortion [58][59][60][3].

Clipping distortion can occur in every stage of the amplifier, but it most likely that it will occur in the output stage where the signals are often the largest. It can be avoided by ensuring large enough voltage and current driving capabilities.

C. Errors due to bandwidth limitations

The speed of any amplifier is limited. When considering a negative-feedback amplifier it simply means that the output frequency components are not in correct proportion for fast signals, i.e., the waveform changes. When considering speed limitations, it is possible to distinguish between:

- small-signal speed limitations
- large-signal speed limitations

In case of small signals it is found that, from a certain frequency, the poles in the transfer begin to dominate and start to introduce errors, i.e., the bandwidth of the transfer is limited. Since this is caused by the gain being not constant with

frequency, this kind of distortion is called frequency distortion or linear distortion [61]. Linear distortion in negative-feedback amplifiers can be minimized by ensuring a large enough bandwidth.

Application-specific negative-feedback amplifiers often have two (complex) dominant poles determining the small-signal bandwidth. Depending on the positioning of the (complex) poles, errors due to overshoot may result in the frequency domain and in the time-domain. By forcing the poles in 'maximally flat magnitude' or Butterworth positions, overshoot in the frequency domain can be avoided. Overshoot in the time domain (transient response) can be avoided by forcing the poles into Bessel positions.

Large signals force large current swings to occur in the amplifier. Capacitances in the active part of the amplifier limit the speed of the voltage swings. At a certain amplitude and frequency of the signal, the speed at which the capacitances can be charged and discharged is not sufficient enough and slew-rate limiting occurs[6]. Slew-rate is defined as the maximum rate at which the output voltage can change [62]. To guarantee the required large-signal or full-power bandwidth, the slew-rate has to be large enough by assuring adequate current driving capabilities.

D. Errors due to interference

Interference may lead to disturbing signals at the input of the amplifier. Once again, a distinction can be made between small-signal disturbances that are either in-band or out-of-band, and large disturbing signals.

When the disturbing signal lies within the bandwidth of the amplifier, it is processed as if it is the intended signal, and thus subject to the same limitations as the intended signal. It can not be distinguished from it.

The effects of small disturbing signals with frequencies higher than the bandwidth have been investigated in Section 1.6. The main conclusion is that DC shifts and low-frequency components related to the envelope of the carrier wave are present at the output of the amplifier. These signals are undistinguishable from the intended signal and also subject to the same limitations. Errors due to a small-signal out-of-band disturbance result from weak nonlinear behavior, just as nonlinear distortion. In fact, it may be regarded as a form of nonlinear distortion.

Large disturbing signals have the same effect as large intended signals; it may result in clipping and/or slew-rate induced distortion.

1.7.2 Signal-to-error ratio

The designer's concern is to minimize errors because they limit the signal handling capability. Small signals, for example, might be lost in noise, or be obscured by distortion products from another larger signal or by disturbing signals. Effort

[6]The dual discussion holds for inductances. Inductances are nowadays hardly used in negative-feedback amplifiers, because they are usually bulky and far from ideal. They are therefore disregarded when dealing with amplifier design in this work.

has to be made to make the intended signal large compared to these errors. The ratio of the intended signal and the errors, the signal-to-error ratio (SER), can be regarded as a figure of merit of the signal handling performance of an amplifier for a given input signal and electromagnetic environment.

Assuming weak nonlinear behavior, the signal-to-error ratio at the output of an amplifier is given by:

$$SER = \frac{S_1}{S_{n,eq} + S_2 + S_3 + S_d + S_{\mathrm{ENV}}}, \tag{1.4}$$

where S_1 is the power of the desired signal. The subscript denotes the harmonic of the signal. $S_{n,eq}$ gives the total power of the noise generated by the negative-feedback amplifier. S_2 and S_3 represent the power of the second and third harmonic, respectively, of the desired signal[7]. A disturbance is represented by S_d for the rms power of a signal in the bandwidth and by S_{ENV} for the rms power of the detected envelope variations from a disturbance (much) larger than the bandwidth.

Under the (noise) conditions given in Subsection 1.7.1, it is reasonable to assume that noise will not have a significant effect on distortion and EMI behavior, and vice-versa. Distortion due to the intended signal will show no correlation with the effects due to disturbances (and vice-versa) since they originate from different sources. S_d and S_{ENV} both originate from disturbance(s) (which may be from different interfering sources), but the disturbances causing both are separated in the frequency domain, so there is no correlation. All errors in Equation (1.4) are therefore uncorrelated.

In Equation (1.4) the commonly known signal-to-noise ratio (SNR) $S_1/S_{n,eq}$ and the, somewhat less known, signal-to-distortion ratio $S_1/(S_2 + S_3)$ can be recognized. The signal-to-distortion ratio represents the relative distortion level in a similar manner as the SNR represents the relative random noise level. The SNR in a linear negative-feedback amplifier can be maximized through the separate optimization of the maximal tolerable signal power and the generated noise power [3]. Weak nonlinear distortion can be minimized by ensuring enough loop gain and appropriate biasing of the amplifying stages [58][59][60][3].

The signal-to-disturbance ratio is the desired signal power S_1 divided by the power of the signals resulting from the interfering signal $S_d + S_{\mathrm{ENV}}$. Chapters 2 and 5 will present measures to reduce $S_d + S_{\mathrm{ENV}}$.

1.8 Design for Electromagnetic Compatibility

Malfunctioning of equipment due to lack of EMC has a large impact on society because it may result in nuisances (e.g., radio programmes on the telephone) or life threatening situations (e.g., failing apnea monitoring systems). The examples

[7] The contributions of the amplitude of the second and/or third harmonic are assumed to be so much larger than the higher harmonics that it is common practice to limit the analysis to the third harmonic.

given in Section 1.3 highlight that. EMC should therefore be part of the design process.

Some work on incorporating EMC into the design process has been done. For example, a general method for systematically designing electromagnetically compatible electronics is presented in [43], and design techniques specifically aimed at the reduction of radiated electromagnetic fields are presented in [63]. A systematic design method specifically aimed at realizing a specified SER (thus including EMI) of application specific negative-feedback amplifiers has not been available up to now.

As far as EMC in the design of amplifiers is concerned, it is stated in literature that high-frequency EMI should not reach the input of the amplifier because it is very difficult to calculate the resulting errors in advance [10]. Typically, EMC textbooks therefore concentrate on filtering at the input of the amplifier [10][64][34] and filtered, balanced input configurations [26] to realize an acceptable SER. Unfortunately, this means that an input filter is realized without any knowledge of the EMI behavior of the amplifier itself. This results in design by trial and error, which should be avoided. Although filtering can give good results, there are other drawbacks. Filtering may degrade stability, worsen the noise behavior and, in case of balanced amplifier configurations, deteriorate the common-mode rejection ratio [26].

The purpose of this work is to present a design method for realizing the specified SER when (high-frequency) EMI reaches the input of the amplifier by decreasing the susceptibility of the amplifier itself. When it is found that the amplifier susceptibility can not be made low enough, the effects of an input filter can be examined by incorporating it in the calculations made during the design process. The filter can now be optimized for the specified susceptibility, without degrading noise performance or stability. The method presented may be regarded as additional to existing measures to reach EMC.

1.9 Outline of the thesis

Chapter 2 will give methods to determine disturbance amplitudes at the input of an amplifier due to electromagnetic waves that couple into the interconnect and measures for reducing this disturbance are also presented. From this it follows how much immunity has to be designed into the negative-feedback amplifier. Since we are primarily interested in disturbance due to out-of-band interference (which is often caused by sources located far away), crosstalk will not be discussed.

EMI effects like DC-shifts and AM detection in negative-feedback amplifiers result from nonlinear behavior of components. Nonlinearities will therefore be investigated in detail and models for nonlinear behavior of active components will be presented in Chapter 3. Single active devices often behave rather poorly, e.g., regarding their high-frequency and nonlinear behavior. Special combinations of stages, the cascode and the differential stage, have therefore been developed. The cascode stage has improved high-frequency and the differential stage improved

nonlinear behavior. Both combinations of stages are extensively dealt with in Chapter 4.

The design method for negative-feedback amplifiers with specified SER will be presented in Chapters 5 and 6. It will enable the designer to design for an accurate signal transfer, and also for noise, bandwidth, and EMI behavior. Chapter 7 presents the verification of the design method by presenting examples of realized amplifiers and their measured susceptibility. Finally, Chapter 8 presents the conclusions.

Chapter 2

Decreasing the disturbance coupled to amplifiers

Since the amplifier is often the first signal processing stage in a system, it is likely that it may be subjected to the highest levels of disturbance, although the signal level at its input is still low. The signal to error ratio (SER) may therefore be degraded severely and these losses in SER can not be compensated adequately by other signal processing stages. Therefore, this work concentrates on presenting design strategies for negative-feedback amplifiers with reduced EMI susceptibility. Moreover, it is assumed that the subsequent signal processing stages are less susceptible to disturbances, and that the disturbance level in these stages is lower.

Analysis is an important part of design. To analyze EM compatibility, the design is split in two parts: circuit components and interconnects [43][65]. The (active) circuit components[1] are responsible for nonlinear distortion of signals and envelope detection, which is analyzed with network theory. The interconnects are mainly responsible for disturbing signal transport, which is analyzed using electromagnetic field analysis. This chapter will present methods to estimate the disturbing signal in the interconnect(s) for a given EM environment, and measures for reducing this disturbance.

Section 2.1 presents a discussion about coupling of electromagnetic fields to the interconnects of negative-feedback amplifiers. Properties of the interconnect and their effect on the intended signal transfer is discussed in Sections 2.2 and 2.3, while methods to estimate the amount of disturbance induced in an interconnect connected to an amplifier are presented in Section 2.6. The disturbance can be common-mode, which may be transferred to a differential-mode disturbance. This effect, and some measures for reducing common-mode disturbances are

[1] Practical resistors, capacitors and inductors also show non-ideal behavior, specifically at higher frequencies. Their non-ideal behavior is extensively dealt with in textbooks, e.g., [66][41][34], to which the interested reader is referred. Possible nonlinear behavior of passive components, e.g., electrolytic capacitors are not investigated, but may be analyzed with the methods presented in this work.

described in Section 2.7. Disturbances can also be reduced by using a conductive shield. Shield design is therefore discussed in Section 2.8. Finally, Section 2.9 presents the conclusions.

2.1 Coupling of electromagnetic fields

In principle EM-fields can be coupled to the negative-feedback amplifier by coupling to the source, the interconnect between the source and amplifier, the amplifier, the interconnect between the load and amplifier, the load, and the interconnect to the power supply as Figure 2.1 shows. The resulting disturbance is depicted by voltage and current sources [42]. Source E_s may be a voltage or current signal source, and Z_l is the load impedance. Note that the depicted disturbance sources are differential-mode sources. Common-mode disturbances may also occur, but are not shown in Fig. 2.1.

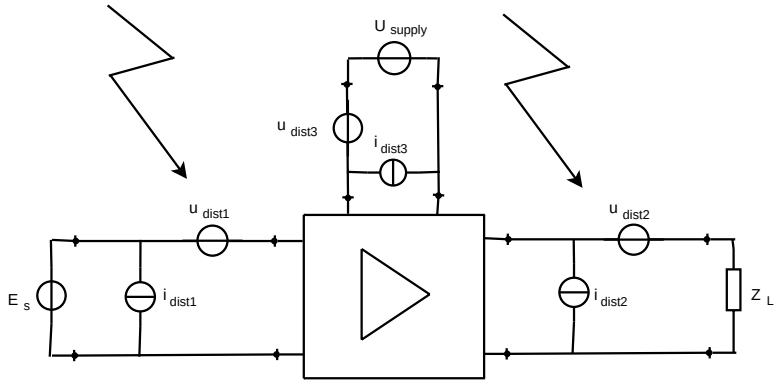


Figure 2.1: Interference coupling to an amplifier with source, load, power supply, and associated interconnects.

Designing for low EMI susceptibility is equivalent to minimizing the disturbing sources and/or decreasing their adverse effect on the signal-to-error ratio (SER).

It may be expected that the loop formed by source, interconnect, and the input of the amplifier and the output loop consisting of the amplifier, interconnect, and load, respectively, are much better receptors for EM fields than the amplifier. The latter usually has small dimensions and may be shielded or assumed to be shielded in the first design stages. Therefore, the design problem is simplified at this stage by assuming that interference picked up by the amplifier itself is negligible compared to that picked up by loops formed by the interconnects. The validity of this assumption has to be checked later in the design process and (if necessary) measures have to be taken to ensure that it is valid.

Interference reaching the amplifier via the input interconnect can not be distinguished from the intended signal when it is in the passband of the amplifier.

For an ideal amplifier, no adverse effects exist when the disturbance is out-of-band. As was discussed in Chapter 1, practical amplifiers will show adverse effects that are quadratically dependent on the disturbing signal reaching its input.

For the ideal amplifier, interference pick-up at the output-load interconnect results in an addition of the disturbance to the load signal. Usually the disturbance is much smaller than the intended signal. Some of the disturbance will be transferred to the input in practical amplifiers, where its effect will be the same as in the case where interference is coupled directly to the input. The disturbance caused by interference at the output may expected to be smaller compared to disturbance at the input, because some attenuation of the disturbance may be expected to occur in the transfer from output to input. Therefore, emphasis in this work is placed on the disturbance at the input of the amplifier, where its adverse effect is maximal.

In both the case of the ideal and the practical amplifier, the disturbing signal in the passband can not be distinguished from the information signal. Fortunately, a disturbance usually gets noticeable at higher frequencies, as will be shown in the next section. On top of that, measures to decrease the EM-coupling are usually effective at low frequencies and may become less effective at high frequencies (out-of-band). It may therefore be possible that the disturbance generated in the passband is still small enough to maintain the SER. The out-of-band interference may, however, cause deterioration of the SER.

In the remainder of this chapter we concentrate on determining the total disturbing signal at the input of an ideal amplifier. This disturbing signal gives the in-band SER to be expected directly and is also used in Chapters 5 and 6 to determine the SER due to envelope detection.

Finally, interference may be coupled to the power supply interconnect. For a balanced power supply the resulting disturbance is balanced out and does not degrade the system performance. When the balancing is not ideal, or when there is no balancing at all, the disturbance may hamper system performance. For the power supply, however, the signal of interest (i.e., DC voltage/current) and the disturbance are well separated in the frequency domain. Filtering at low frequencies (e.g., a few Hz), is thus a powerful method to prevent disturbances on the power supply that hamper the SER.

2.1.1 Coupling mechanisms

As was discussed earlier, the interconnects are responsible for transport of both the desired information and disturbance. The latter may also be called erroneous information or error(s) for short.

Errors in negative-feedback amplifiers can be divided in: errors due to noise, errors due to signal power, errors due to bandwidth limitations, and errors due to interference, as discussed in Chapter 1. Errors due to noise and signal power are mainly determined by the implementation of the negative-feedback amplifier. Apart from the negative-feedback amplifier bandwidth limitations and interference induced errors are also affected by the interconnect. The errors due to

bandwidth limitations and interference caused by non-ideal behavior of the interconnects are discussed in this chapter.

An ideal interconnect does not have any resistance and does not receive or radiate electromagnetic fields. The ideal interconnect is commonly used in drawing schematics. It is just a line that forms a node for the various components connected to it, and it does not affect the signal transfer in any way. Real interconnects do affect the signal transfer, radiate and receive electromagnetic fields, and therefore a model describing these effects on the signal transfer is required. The model of the interconnect should be as simple as possible, yet it should be able to predict errors due to bandwidth limitations and interference caused by the interconnect with reasonable accuracy.

The resistance and loss of electromagnetic fields may cause bandwidth limitations and linear distortion to occur in interconnects. Reception of electromagnetic fields cause disturbances (errors) to be induced in the interconnect. In this work it is assumed that the interconnect has to be designed so that it does not introduce bandwidth limitations, i.e., it does not degrade the bandwidth specifications, and it does not introduce unacceptably large errors due to interference.

Simple models for the interconnect are presented in Sections 2.2 and 2.6. These models can be used to analyze the generation of errors in the interconnect. They will be used to determine the remaining variables in the design of the interconnect such that for a given source, information domain and interference, a certain minimal SER can be maintained.

2.2 Electrical model of the interconnect

Any interconnect, whether it is a two-wire line, a coax cable, or a pair of traces on a printed circuit board, in essence is a two-port and thus shows a transfer between the input and output ports, and an impedance. The resistivity (ρ) of the conductor material causes the conductors to have a resistance that depends on the dimensions of the interconnect. The skin effect causes an 'AC' component to occur in the resistance that increases with the square root of the frequency [42].

The current flowing in the conductor generates magnetic fields both around and inside the conductor, resulting in an external inductance (i.e., the self inductance) and an internal inductance, respectively. This internal inductance is usually negligible compared to the external inductance [42]. Charge distributed over the conductor surface result in an electric field, resulting in a capacitance. The resistance, capacitance and inductance of the interconnect may result in errors in the information transfer due to bandwidth constraints or when reflections of the signal occur.

Interconnects, and complete systems can, based on their dimensions, be divided in electrically-small and electrically-large interconnects. 'Large' in the case of interconnects (and even complete systems) means that the dimensions of the interconnect become comparable to or greater than the wavelength, λ, of the

signal. For engineering purposes, an interconnect is electrically-large when it is larger or equal to $\lambda/10$ [41]. Smaller interconnects (i.e., $< \lambda/10$ in length) are regarded to be electrically-small. The signal may be both intended and parasitic due to a disturbance. Note that the same interconnect can be small for the intended signal but large for the disturbance, or vice-versa. The latter is not considered in this work.

Coupling of a disturbance depends on the distance between the interference source and the receptor. Here, two cases can also be distinguished since the distance (d) can be electrically-small or electrically-large. A distance is large when compared to the antenna size [43]; $d \geq 2D^2/\lambda$, with D being the maximum overall antenna dimension [67]. In the case of small dipoles, the distance becomes large at an approximate value of $\lambda/(2\pi)$ [41]. Distance d is then large when $d \geq \lambda/(2\pi)$. The latter boundary is usually used in EMC engineering.

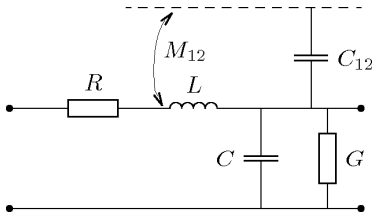
When d is small, the coupling is considered near-field, and when d is large, a far-field coupling problem [42][41]. The near-field coupling can be represented by a coupling capacitance and a mutual inductance. This is not the case for far-field coupling as the electromagnetic wave propagation has to be considered in that case.

For the coupling of interference, four different situations can be distinguished. When we take the length $\mathcal{L}$ of the interconnect as representative for the dimensions of the interconnect, we have [43]:

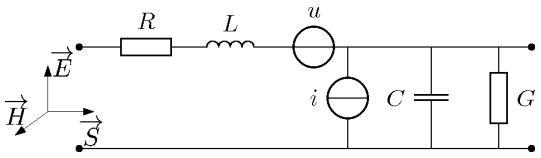
1. both $\mathcal{L}$ and d are small
2. $\mathcal{L}$ is small and d is large
3. $\mathcal{L}$ is large and d is small
4. both $\mathcal{L}$ and d are large

Case 1 results in coupling to a lumped element model representation of the interconnect via mutual inductance (M_{12}) and a coupling capacitance (C_{12}) [42], see Fig. 2.2(a). The distributed resistance of the interconnect is represented by a resistance (R), the inductance and capacitance by L and C, respectively, and the conductance between the conductors by G. Coupling of disturbance via mutual inductance and coupling capacitance is often called crosstalk.

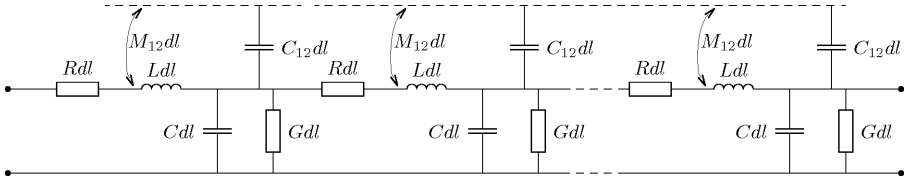
The second case (2, above) represents plane wave coupling to a small interconnect. In this work only the *receiving* small interconnect is considered. It is assumed that the designer can not do anything to reduce the interference generated by emitters at a large distance. The plane wave induces a voltage (represented by voltage source, u) and a current (represented by current source, i) in the lumped element model of the interconnect, as depicted in Fig. 2.2(b). The plane wave is represented three vectors $\overrightarrow{E}$, $\overrightarrow{H}$, and $\overrightarrow{S}$, being the electric field, the magnetic field, and the Poynting vector, respectively. The disturbance induced by the plane wave is represented by a single voltage (u) and current source (i) [42]. Estimating the effects of plane wave coupling on electrically-short interconnects is discussed in Subsection 2.6.1.



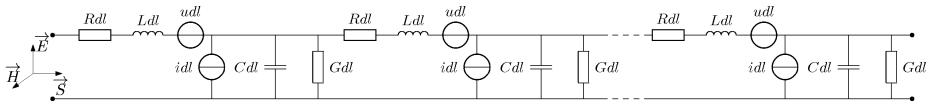
(a) Lumped representation of an electrically short interconnect. Crosstalk is represented by a lumped capacitance C_{12} and mutual inductance M_{12} to an interference source, which is depicted by the dotted line.



(b) Lumped representation of plane wave coupling to an electrically short interconnect. The disturbance induced by the plane wave can be represented by a voltage and current source.



(c) A uniform electrically-long interconnect suffering from crosstalk can be modelled by a cascade of infinitesimal length (dl) sections of the interconnect.



(d) A uniform electrically-long interconnect suffering from plane wave interference can be modelled by a cascade of infinitesimal length (dl) sections of the interconnect.

Figure 2.2: Representations of both electrically-small and large interconnects suffering from interference due to crosstalk (2.2(a), 2.2(c)) and plane wave coupling (2.2(b), 2.2(d)).

Case 3 gives coupling via distributed mutual inductance and coupling capacitance to transmission lines. In the case of transverse electromagnetic (TEM) field propagation, the fields have no component parallel to the uniform line conductors [42][67][68]. The model of an electrically-long interconnect suffering from near-field disturbance is shown in Fig. 2.2(c) [43]. The 'uniform' property of a

transmission line refers to the constancy of the conductor geometry (spacing and cross-sectional area), conductor material, and the surrounding dielectric medium over the length of the line [68]. The interconnect and its electrical properties are represented by a cascade of small sections (dl) of the interconnect. The same holds for the coupling parameters M_{12} and C_{12}.

Solving the transmission line equations [42][67][68] results in the familiar expressions for the characteristic impedance (Z_0) and the propagation constant (γ). Equations for determining the crosstalk in electrically-long interconnects are presented in [42] and [43]. In this work, we are interested in disturbance due to out-of-band interference. Since out-of-band interference is often caused by sources located far away, crosstalk is not discussed in this work. The interested reader is referred to literature for measures to decrease crosstalk, e.g., [43][42][34].

Finally, case 4 often depends on solving Maxwell's equation numerically. For some specific cases, like coupling to an isolated resonant antenna, analytical results are available, e.g., [69][67][70]. The coupling of electromagnetic waves to (cylindrical) antennas for various frequencies (i.e., also non-resonant frequencies) may be determined by approximate equations given in, e.g., [70]. In this work it is assumed that no isolated antennas (i.e., interconnects) occur. This means that a conductive (ground) plane is present at a small distance away from the interconnect. For this situation, analytical closed form equations exist [68] and will be presented in Subsection 2.6.2. Equations that also take nonuniformities of the interconnect into account can be found in [71], but will not be presented here for reasons of simplicity.

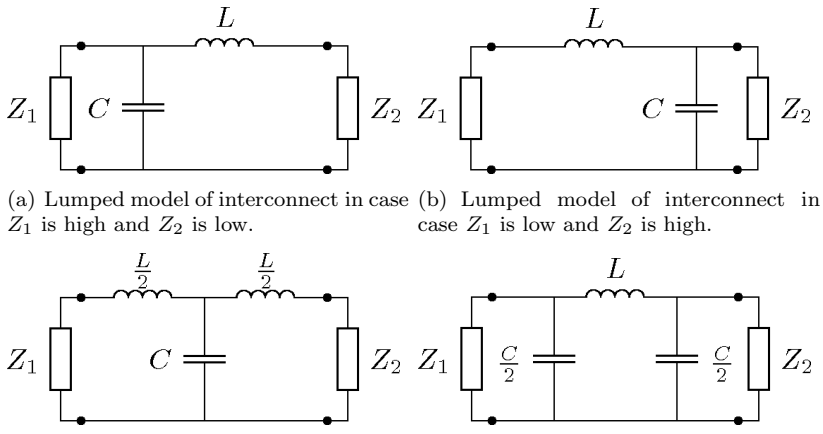
Fig. 2.2(d) depicts the electrically-long interconnect that is subjected to a plane wave. The effects of an interfering plane wave are now represented by the combined effects of infinitesimal voltage and current sources (udl and idl, respectively) [42]. Subsection 2.6.2 presents equations giving the total amount of disturbing current or voltage at the terminals of the interconnect. The combined effect of all sources (and the characteristic impedance) is thus taken into account in these equations.

The (lumped model) parameters R, L, C, and G can be determined from the equations presented in Table 2.1. Conductance G may often be neglected in practical cases, since $\omega C \gg G$, and R may often be neglected because it is smaller than the source impedance in most practical cases. These conditions are assumed in the remainder of this chapter.

2.3 Intended signal transfer in electrically-small interconnect

When the interconnect is electrically-small, its behavior can be modelled using lumped elements, as was shown in Section 2.2. However, the way the lumped components are connected depends on the terminating impedances. Since an interconnect can be terminated at both sides, there are two terminating impedances. The two terminating impedances result in four extreme cases: both

Z_1 and Z_2 are low (e.g., a short circuit), both Z_1 and Z_2 are high (e.g., an open connect), Z_1 is low and Z_2 is high, and Z_1 is high and Z_2 is low. These four combinations result in four lumped models of the interconnect (see Figure 2.3). Note that the lumped components are connected in such a way that their effect on the signal transfer is maximal.



(a) Lumped model of interconnect in case Z_1 is high and Z_2 is low.

(b) Lumped model of interconnect in case Z_1 is low and Z_2 is high.

(c) Lumped model of interconnect in case Z_1 and Z_2 are both low.

(d) Lumped model of interconnect in case Z_1 and Z_2 are both high.

Figure 2.3: The lumped model that best represents the electrical behavior of an electrically-small interconnect depends on the terminating resistances.

When it is assumed that Z_1 represents the impedance of the signal source and Z_2 the load of the source (i.e., the input impedance of the amplifier), it may easily be identified that Figure 2.3(a) represents the model of an interconnect of a current processing amplifier and Figure 2.3(b) represents the model of an interconnect of a voltage processing amplifier. Figures 2.3(c) and 2.3(d) represent situations that usually will not occur in case of negative-feedback amplifiers. They may, however, occur when EMC measures are taken, e.g., a shielding conductor connected to the reference via short circuits ($Z_1 = Z_2 = 0$), or a floating interconnect ($Z_1 = Z_2 = \infty$).

The inductance, capacitance, and resistance of the interconnect depend on its dimensions. The smaller the dimensions, the smaller the values of these lumped components become. The maximal dimensions of the interconnect therefore follow directly from the bandwidth requirement.

For example, consider a voltage domain information channel. Impedance Z_1 is the source impedance and is taken to be the source resistance R_s for simplicity. Z_2 is the input impedance of a voltage processing amplifier and is therefore ideally infinite. The transfer of the interconnect equals

$$H_u(s) = \frac{1}{s^2LC + s(R_sC + \frac{L}{Z_2}) + 1 + \frac{R_s}{Z_2}} \approx \frac{1}{s^2LC + sR_sC + 1}. \qquad (2.1)$$

From this equation it follows that the bandwidth, B, of the transfer is estimated as[2] $B \approx \frac{1}{2\pi R_s C}$ in most practical cases. For the bandwidth of the interconnect to have a negligible effect on the signal transfer and processing, it should be designed so that it is ≥ 5 times the bandwidth of the amplifier. From this requirement the maximal dimensions of the interconnect can be determined (see Subsection 2.5).

The solid line in Figure 2.4 shows H_u of an electrically-short interconnect in case L equals 1 μH, C equals 4 pF and the source impedance is a resistance R_s of 1 kΩ. The interconnect has no adverse effect on the signal transfer at low frequencies. The capacitance of the interconnect and the source resistance limit the bandwidth to about 39.8 MHz. Transfer H_u decreases at a rate of 20 dB/dec for frequencies higher than the bandwidth. L does not affect H_u in the depicted frequency range.

2.4 Intended signal transfer in electrically-large interconnect

The generally used name for a long interconnect is transmission line. The equations describing the behavior of long interconnects are therefore called transmission line equations. Both characteristic impedance, Z_0 and propagation constant, γ, determine the behavior of an electrically large interconnect.

Z_0 is given by [67][68]:

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}}. \tag{2.2}$$

The resistance per meter is given by R, the inductance per meter by L, the conductance per meter by G, and the capacitance per meter by C. For frequencies $\omega L \gg R$ and $\omega C \gg G$, the characteristic impedance reduces to $Z_0 = \sqrt{L/C}$. Note that compared to an interconnect without insulation, the Z_0 of an interconnect with insulation around the conductors is a factor $\sqrt{\varepsilon_r}$ lower, because C is the same factor larger. R, G, L, and C can be determined for various long interconnects with the equations presented in Section 2.5 (Table 2.1).

Propagation constant γ is defined as $\sqrt{(R + j\omega L)(G + j\omega C)} = \alpha + j\beta$, where α is the attenuation constant and β is the phase constant of the transmission line. It gives a measure for the attenuation and phase shift that a signal experiences while traveling across the transmission line.

The attenuation constant α represents dissipative losses in the conductors and in the dielectric medium and is for low loss lines given by $\alpha = \frac{R}{2Z_0} + \frac{GZ_0}{2}$ [68]. Resistance R increases with the square root of the frequency due to the skin effect (see Table 2.1). The equation for α is in Np/m. In dB/m it is $20 \log e \times \alpha \approx$

[2]When the current domain channel is evaluated, the same approximation for the bandwidth of the interconnect is found. The assumptions are now: Z_2 is ideally zero, and when not zero much smaller than Z_1. Z_1 is for simplicity also taken equal to the source resistance R_s.

8.686α [67]. The dielectric losses represented by G increase proportional to frequency. The phase constant β equals $\omega\sqrt{LC} = \omega\sqrt{\mu_0\mu_r\varepsilon_0\varepsilon_r}$ [67][68].

At high frequencies, α may be dominated by inhomogeneities in the cable construction giving much higher attenuation than that predicted by this simple equation. For example, the loss at mobile telecommunication frequencies is about $0.2-2$ dB/m, but losses over 10 dB/m have also been reported [72].

In electrically-large interconnects it is impossible to work in either voltage or current domain, because after traveling a quarter wavelength, a voltage becomes a current signal and vice-versa [43]. Since the power remains constant, power should be the domain of the information. Therefore, the impedances of the signal source (Z_s), the interconnect, and the input of the amplifier (Z_{in}) should match to ensure constant power transfer. The impedance of an electrically-large interconnect is called the characteristic impedance (Z_0). When $Z_s = Z_0 = Z_{in}$, the interconnect is properly terminated [68].

Ideally, the input impedances of voltage and current amplifiers are infinite and zero, respectively. Infinite or zero impedances prevent power transfer, and therefore the signal will be reflected, resulting in distortion[3]. To prevent this, the information channel should be terminated by adding, e.g., series or parallel resistances in the current and voltage domain channel, respectively, or by applying a dual-loop negative-feedback amplifier with input and output impedances matched to the impedance of the interconnect. However, matching the (input) impedance of the amplifier to the characteristic impedance of the interconnect has some drawbacks.

Firstly, the voltage or current source impedance ends up in the transfer of the amplifier. An inaccurate or even nonlinear source impedance, causes the transfer to be inaccurate. This should therefore be avoided.

Secondly, most information sources (should) operate either in the voltage or current domain and thus require either voltage or current domain transport of the signal, i.e., the source should be terminated either with an infinite or zero impedance in the frequency band of the information. Note that from this discussion follows that the signal source impedance usually does not match the characteristic impedance of the interconnect either.

For frequencies well above the passband, both terminating impedances could be made equal to the characteristic impedance by shunting the terminating impedance with a capacitively-coupled resistance of the appropriate value. This may have detrimental effects on the noise performance of an amplifier, so this should be carefully checked. Besides, source impedances are often characterized by a capacitive behavior at high frequencies. This makes it hard to accomplish a proper termination. We therefore limit this work to voltage and current domain signal transport.

For illustration purposes, it is shown what the consequences are of employing an electrically-large interconnect for transferring a voltage-domain signal. A comparable discussion holds for the current-domain channel. The transfer of

[3]Practical amplifiers do not have either zero or infinite input impedance, but values much lower or higher than Z_0 can be expected. Therefore, reflections will still occur.

the large interconnect between the source to the input of the voltage amplifier, H_u, is [68]

$$H_u = \frac{Z_0 Z_{in}}{(Z_0 Z_s + Z_0 Z_{in}) \cosh(\gamma \mathcal{L}) + (Z_0^2 + Z_s Z_{in}) \sinh(\gamma \mathcal{L})}, \tag{2.3}$$

with γ being the propagation constant, $\mathcal{L}$ the length of the interconnect, and Z_0 its characteristic impedance. Z_s and Z_{in} are the source impedance and the (ideally infinite) input impedance of the voltage amplifier, respectively.

The signal integrity may be seriously hampered in case of electrically-large interconnects. Because impedances Z_s and Z_{in} do not match the characteristic impedance of the transmission line, reflections occur in the interconnect. Transfer H_u now shows resonances and anti-resonances, instead of a smooth 20 dB/dec roll-off as in case of the short interconnect (see the dashed line in Figure 2.4). Although not clearly visible in a Bode diagram, the sign of the voltage

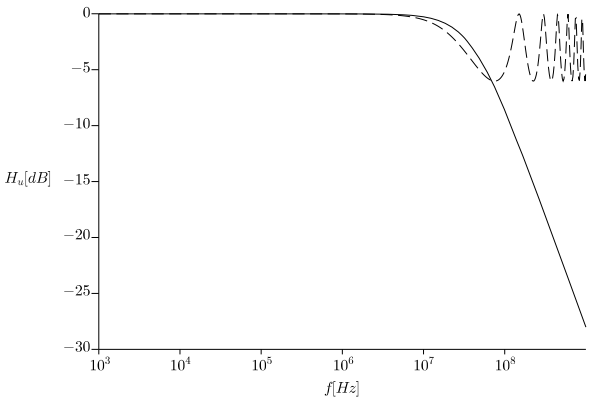


Figure 2.4: Transfers of two voltage domain channels with the same inductance and capacitance values (1 μH and 4 pF, respectively). The source impedance is $Z_s = 1$ kΩ and the amplifier's input impedance $Z_{in} = \infty$. The solid line depicts the Bode plot of the electrically-short channel. The dashed line depicts the Bode plot of an electrically-long channel with length $\mathcal{L}$ of 1 m and Z_0= 500 Ω.

reaching the amplifier may even become opposite to the sign of the voltage at the source, causing severe errors.

The first resonance[4] occurs at the frequency at which the interconnect length equals a quarter of the wavelength of the information. The following resonance frequencies occur at odd multiples of this frequency; $f_{res} = \frac{nc}{4\mathcal{L}}$, with

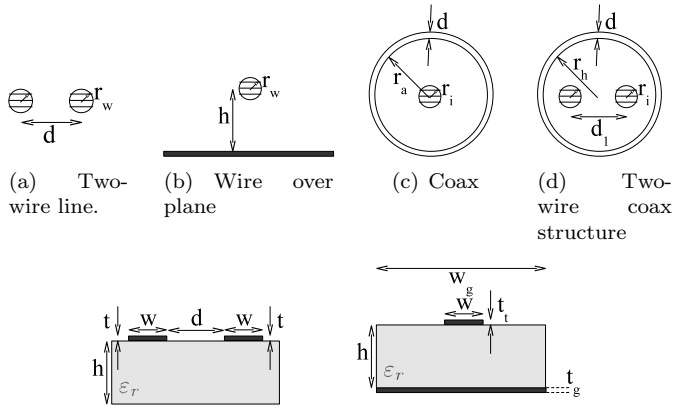
[4]The same convention as in [67] is used. High impedance or parallel resonant comparable transfers are called anti-resonant, whereas low impedance or series resonant comparable transfers are called resonant.

$n = 1, 3, 5 \cdots$, and c being the speed of light. The attenuation of the information that occurs at the resonance frequencies depends on Z_0. Lower values of Z_0 cause larger attenuation values than higher values of Z_0. At the anti-resonance frequencies ($f_{anti-res} = \frac{nc}{4\mathcal{L}}$, with $n = 2, 4, 6 \cdots$) the transfer from source to input voltage is about unity, when the attenuation constant is low.

To ensure signal integrity, interconnects should never become electrically-large with respect to the wavelength of the highest frequency of the information it has to transfer. The maximal dimension (length) of an interconnect should be designed to be smaller than $\lambda/10$. This limitation is not a problem for the amplifiers dealt with in this work. These special purpose negative-feedback amplifiers are assumed to have a moderate bandwidth, up to several tens of MHz.

2.5 Parameters of interconnects

For small interconnects, the lumped model parameters are of importance, and for large interconnects the characteristic impedance and the propagation constant are of importance. Deriving the equations for these parameters is beyond the scope of this work. Besides, these equations are presented in literature for several types of interconnects. For convenience, Fig. 2.5 shows some commonly encountered interconnects, and Table 2.1 presents equations for determining their parameters. More can be found in literature, e.g., [63][73][74][43][42][75].



(a) Two-wire line. (b) Wire over plane (c) Coax (d) Two-wire coax structure

(e) Coplanar strips (f) Microstrip

Figure 2.5: Some often encountered interconnects.

In all equations for R, the skin depth (represented by δ) occurs. The skin depth is given by $\delta = \sqrt{2\rho/(\mu\omega)}$ [41], with ρ being the resistivity of the conductor material, ω the angular frequency and $\mu = \mu_0\mu_r$, with μ_0 being the permeability of free space, and μ_r the relative permeability. The resistance thus increases

Table 2.1: Overview of the parameters of some commonly used interconnects (continued on the next page).

	R [Ω/m]	G [S/m]	L [H/m]	C [F/m]
Two-wire line [75] Fig. 2.5(a)	$\frac{\rho}{\pi\delta r_w}\frac{0.5d}{\sqrt{0.25d^2-r_w^2}}$	$\omega C\tan\delta_1$	$\frac{\mu_0}{\pi}\ln\left(\frac{0.5d+\sqrt{0.25d^2-r_w^2}}{r_w}\right)$	$\frac{\pi\varepsilon_{eff}}{\ln\left(\frac{0.5d+\sqrt{0.25d^2-r_w^2}}{r_w}\right)}$
wire-plane Fig. 2.5(b) [75]	$\underbrace{\frac{\rho}{2\pi\delta r_w}\frac{0.5d}{\sqrt{0.25d^2-r_w^2}}}_{wire}$ $+\underbrace{\frac{\rho_p}{2\pi\delta_p\sqrt{0.25d^2-r_w^2}}}_{gnd-plane}$	$\omega C\tan\delta_1$	$\underbrace{\frac{\mu_0}{2\pi}\ln\left(\frac{0.5d+\sqrt{0.25d^2-r_w^2}}{r_w}\right)}_{wire}$ $+\underbrace{\frac{\mu_0}{4\pi}\frac{\delta_p}{\sqrt{0.25d^2-r_w^2}}}_{gnd-plane};\ d=2h$	$\frac{2\pi\varepsilon_{eff}}{\ln\left(\frac{0.5d+\sqrt{0.25d^2-r_w^2}}{r_w}\right)};$ $d=2h$
coax Fig. 2.5(c) [75]	$\frac{\rho_i\left(1+\frac{\delta_i}{2r_i}\right)}{2\pi r_i\delta_i}+\frac{\rho_a}{2\pi r_a\delta_a}$	$\omega C\tan\delta_1$	$r_i>\delta_i,\ d>\delta_a$: $\frac{\mu_0}{2\pi}\ln\left(\frac{r_a}{r_i}\right)+\frac{\mu_0}{4\pi}\left(\frac{\delta_i}{r_i}+\frac{\delta_a}{r_a}\right)$	$\frac{2\pi\varepsilon_0\varepsilon_r}{\ln\left(\frac{r_a}{r_i}\right)}$
two-wire coax Fig. 2.5(d) [75]	$\approx\frac{\rho_i}{\pi r_i^2}\rho_i'+$ $\frac{4\rho_h}{\pi r_h\delta_h}\frac{(0.5d_1r_h)^2}{r_h^4-(0.5d_1)^4}+$ $\frac{\rho_i}{2\pi(0.5d_1)^2}\rho_z'\times$ $\left[1-\frac{(d_1r_h)^2}{r_h^4-(0.5d_1)^4}\right]^2;$ $r_i\le1.5\delta_i:\rho_i'\approx1+\frac{1}{48}\left(\frac{r_i}{\delta_i}\right)^4$ $r_i\ge1.5\delta_i:\rho_i'\approx\frac{1}{4}+\frac{r_i}{2\delta_i}+\frac{3\delta_i}{32r_i}$ $r_i<\delta_i:\rho_z'\approx\frac{1}{4}\left(\frac{r_i}{\delta_i}\right)^4$ $r_i>\delta_i:\rho_z'\approx\frac{r_i}{\delta_i}-\frac{1}{2}$	$\omega C\tan\delta_1$	$\approx\frac{\mu_0}{\pi}\left[\ln\left(\frac{d(r_h^2-(0.5d_1)^2)}{r_w(r_h^2+(0.5d_1)^2)}\right)+2\frac{\delta}{r_h}\frac{(0.5d_1r_h)^2}{r_h^4-(0.5d_1)^4}\right]$ $-\frac{\mu_0}{\pi}\left(\frac{r_w}{d_1}\right)^2\left(1-\frac{(d_1r_h)^2}{r_h^4-(0.5d_1)^4}\right)^2\lambda_z$ $r_w<\delta:\lambda_z=\frac{1}{12}\left(\frac{r_w}{\delta}\right)^4$ $r_w>\delta:\lambda_z=1-\frac{\delta}{r_w}$	$\frac{\pi\varepsilon_0\varepsilon_r}{\ln\left(\frac{d_1}{r_w}\frac{r_h^2-(0.5d_1)^2}{r_h^2+(0.5d_1)^2}\right)-A}$ $A=\left(1-\frac{(d_1r_h)^2}{r_h^4-(0.5d_1)^4}\right)^2$ $\times\left(\frac{r_w}{d}\right)^2$

Table 2.1: Overview of the parameters of some commonly used interconnects.

	R [Ω/m]	G [S/m]	L [H/m]	C [F/m]
Coplanar Strip Fig. 2.5(e)	$2\left(\frac{\rho}{wt} + \frac{\rho}{2(\delta w+\delta t)}\right)$ [42]	$\omega C \tan\delta_1$	$\frac{\mu_0}{\pi}\left[\ln\frac{\pi(d-w)}{w+t} + 1\right]$ [74]	$\varepsilon_{eff} C_0$ $C_0 = \frac{1}{c^2 L}$
Microstrip line Fig. 2.5(f)	$\underbrace{\left(\frac{\rho}{wt} + \frac{\rho}{2(\delta w+\delta t)}\right)}_{track} + \underbrace{\left(\frac{\rho}{w_g t_g} + \frac{\rho}{2(\delta w_g+\delta t_g)}\right)}_{gnd-plane}$ [42]	$\omega C \tan\delta_1$	$\underbrace{\frac{\mu_0}{2\pi}\ln\left(\frac{2\pi h}{w+(1+\pi)t_t} + \frac{w+t_t}{w+(1+\pi)t_t}\right)}_{track} + \underbrace{\frac{\mu_0}{2\pi}\ln\left(\frac{\pi h}{w_g+(1+\pi)t_g} + \frac{w_g+t_g}{w_g+(1+\pi)t_g}\right)}_{gnd-plane}$ [63]	$\varepsilon_{eff} C_0$ $C_0 = \frac{1}{c^2 L}$

with (the square root of the) frequency. In most practical cases, the external inductance (due to L) will be larger than the frequency dependent part[5] of R, and therefore, the latter effect may thus be disregarded. An exception may be a broad microstrip line; its 'AC' resistance is not negligible to the external inductance [76].

Conductance G is calculated from the capacitance C and the loss tangent $\tan\delta_1$ (third column of Table 2.1) [69]. The latter represents the power loss of the dielectric of the insulating medium between the conductors. It is equal to $\frac{1}{\rho\omega\varepsilon_0\varepsilon_r}$, where ρ is the usually large specific resistance of the medium and ε_r is the relative permittivity of the medium. When the medium is formed by a loss free medium, e.g., vacuum, $\tan\delta_1$ equals zero. For an impression of the order of magnitude of a good insulator: the loss tangent $\tan\delta_1$ of a typical polyethylene or teflon dielectric is of the order of $0.0004-0.0009$ up to about 3 GHz [69]. Conductance G will be much smaller than ωC in practical cases, and may therefore be disregarded during design.

For the two-wire line and the wire over a (conductive) plane, holds that the distance between the conductors is represented by d or by the height h of the wire over the plane, and the radius of the wires by r_w, see Figs. 2.5(a) and 2.5(b). The presented equation for the two-wire line (Table 2.1 row one) assume equal radii of the wires. The equations are valid under the assumption that $d > r_w$, skin depth (δ) is smaller than r_w, and height h is much higher than the skin depth (δ_p) of the ground plane [75].

For the coax cable and two-wire coax (Figs. 2.5(c) and 2.5(d); Table 2.1 third and fourth row), hold that r_a and r_h, respectively, are the radii of the outer conductor, r_i is the radius of the inner conductor, and d_1 is the distance between the two wires in the coax. The thickness of the outer conductor is represented by d. Note the constraints given in Table 2.1 for validity of the equations for the coax and two-wire coax.

When tracks on a printed circuit board are considered (the coplanar strips in Fig. 2.5(e) and the microstrip line in Fig. 2.5(f); Table 2.1 fifth and sixth row), the width of the tracks is w, t is the thickness of the track, w_g is the width of the ground plane, and h is the height of the printed circuit board material. The relative dielectric constant of the latter (typical glass-epoxy [42]) is ε_r. Note that the equations for calculating the inductance of the coplanar strips and the microstrip line hold when the length ($\mathcal{L}$) of the track is much larger than d and w [74].

The effective permittivity ε_{eff} in the equations for C (in rows 1, 2, 5, and 6), is determined by both the relative permittivity (ε_r) of the dielectric media (e.g., printed circuit board and wire insulation) and $\varepsilon_r \approx \varepsilon_0$ of air, because the field lines penetrate both the air and the dielectric. Determining ε_{eff} may be difficult, but some equations for determining it are presented in literature, e.g. [67]. For example, in case of a printed circuit board with $w/h \ll 1$, $\varepsilon_{\text{eff}} \approx 0.5(\varepsilon_r + 1)$.

[5]The low resistivity of conductors cause a low value of R at DC, which increases with $\sqrt{\omega}$. Evaluation of the equations given in Table 2.1 shows that even for small distances between the conductors, ωL is found to be much larger than the frequency dependent part of the resistance.

More accurate and elaborate equations which are valid for other ratios of w and h are found in literature, e.g., [67][42]. Parameter ε_{eff} may, however, also easily follow from measurements. Note that parameter c for determining C_0 (rows 5 and 6) is the speed of light in vacuum. C_0 is the capacitance without the dielectric medium.

The equations presented in Table 2.1 are relatively simple and lend themselves to hand calculations. Moreover, they show the relation between the parameters R, G, L, and C and the physical dimensions of the interconnect, and can therefore be used in the first design steps. More accurate (and more elaborate) models, which can be used in the subsequent design steps are readily available in modern simulators.

2.6 Coupling of interference to the interconnect

When the distance between interfering source and receptor is large, the receptor is in the far field. The electric ($\overrightarrow{E}$) and magnetic ($\overrightarrow{H}$) fields of the electromagnetic wave are perpendicular to each other and perpendicular to the direction of propagation, which is represented by the Poynting vector $\overrightarrow{S}$, see Figs. 2.6 and 2.7. This electromagnetic wave is called a plane wave and has a constant ratio of the $\overrightarrow{E}$ and $\overrightarrow{H}$ fields: the wave impedance $Z_w = E/H \equiv \sqrt{\mu_0/\varepsilon_0} = 120\pi\Omega$ [42].

In any interconnect (electrically short and long), disturbing signals are induced by interfering EM fields. These signals may be separated into antenna and transmission line currents [63]. The antenna current is, by definition, the sum of all currents at any cross-section of a transmission line. Both differential-mode and common-mode currents are transmission line currents.

The transmission line currents, in a (multi-conductor) transmission line, can be found via transmission line theory [42]. A vital restriction is that the distance, d, between the conductors of the transmission line satisfies $d \leq \frac{\lambda}{2\pi}$, with λ being the wavelength of the highest interfering signal [63]. Comparison of the far more elaborate antenna theory and this approach to determine the currents in a transmission line for spacings $d \leq \frac{\lambda}{2\pi}$ (even up to $\lambda/4$) show deviations between the two methods of less than 2 dB [68], and therefore the transmission line theory can be used.

When the conductor is $d > \frac{\lambda}{2\pi}$ far from a ground plane, the conductor has to be regarded as a monopole antenna [77]. The antenna current at its terminal has to be determined with antenna theory. For determining the antenna current and antenna impedance as a function of frequency, the reader is referred to literature, e.g., [70][78][63][77][69]. In this work it is further assumed that all signal paths satisfy the earlier mentioned condition since most signal paths are not isolated. They are parallel, or approximately parallel, to a conducting (ground) plane [68].

2.6.1 Plane wave coupling to electrically-short interconnects

Figure 2.6(a) shows an two-wire interconnect subjected to a plane wave[6]. It is terminated on one side by impedance Z_1 and on the other side by impedance Z_2. The electrical behavior of the two-wire line may be described by means of lumped-circuit models, i.e., an inductance (L_d) and capacitance (C_d), as is shown in Figs. 2.6(b) and 2.6(c). Parameters L_d and C_d can be determined using the equations presented in Table 2.1.

The electric field component of the plane wave generates a current in the loop, while the magnetic field component induces a voltage in the loop [42]. The generated current and voltage can be modelled by a current source in parallel with the impedances and a voltage source in series with the impedances [42], respectively, as Fig. 2.6 shows.

Figure 2.6(b) shows the lumped element model for an electrically-short voltage domain channel that is subjected to a plane wave and Fig. 2.6(c) shows the current domain variant.

The magnitude of the disturbing signal sources generated by the electromagnetic field depends on the orientation of the two-wire line in the field. Depending on the angle between the two-wire line and the field, the induced signals may vary between some maximum and minimum value. In EMC engineering it is customary to assume the worse case: maximal magnitude of the induced signal. This also makes sense from a design point of view, so in this work maximal coupling is assumed.

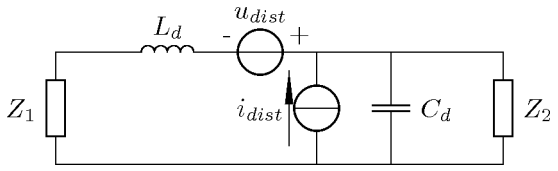
The magnitude of the disturbing voltage at the input of the voltage processing amplifiers can easily be determined by assuming Z_{in} to be infinite (see Fig. 2.6(d)), and the magnitude of the disturbing current at the input of the current processing amplifier by assuming Z_{in} to be zero (see Fig. 2.6(e)). The intended signal sources (i_s and u_s, respectively) and the source impedance Z_s are also depicted in Figs. 2.6(d) and 2.6(e). The signal source impedance will usually be composed of a resistance, R_s, shunted by a capacitance, C_s.

The practical negative-feedback amplifier will not have an infinite or zero input impedance. To simplify the design process, ideal amplifiers can be considered nevertheless. Deviations in the calculated disturbing signal due to deviations of Z_{in} from the ideal value presented to the input of the amplifier can be evaluated later. If the practical negative-feedback amplifier is designed properly, the constraints $Z_s << Z_{in}$ in case of voltage processing amplifiers and $Z_s >> Z_{in}$ in case of current processing amplifiers, respectively, hold. The deviations between the 'ideal' and 'practical' values of the disturbing signal are therefore expected to be small.

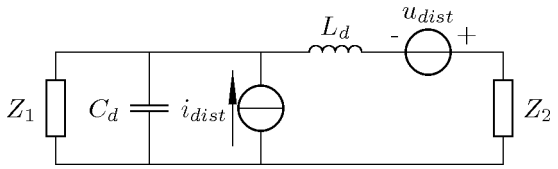
When a current processing amplifier is considered, the input impedance approaches zero. Therefore, Figure 2.6(e) should be used to determine the total disturbing signal. The total disturbing signal is the current flowing into the amplifier due to both disturbing sources. On the other hand, voltage processing

[6]Plane wave coupling to other types of interconnects can be analyzed in the same way.

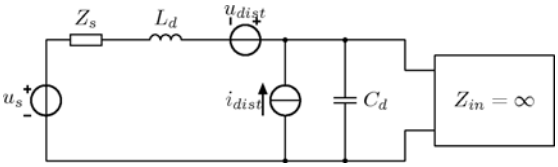
(a) Two wire excited by an electromagnetic plane wave.



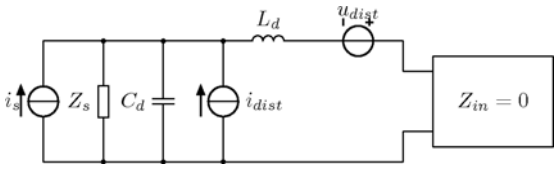
(b) Best lumped model representation in case $Z_1 < Z_2$



(c) Best lumped model representation in case $Z_1 > Z_2$



(d) When the signal source supplies a signal voltage u_s, the input impedance of the amplifier should be infinite.



(e) When the signal source supplies a signal current i_s, the input impedance of the amplifier should be zero.

Figure 2.6: Representation of plane wave coupling to a two-wire line. Impedance of the wires are represented by lumped components. An electromagnetic plane wave induces a signal that can be represented by a voltage and a current source, u_{dist} and i_{dist}, respectively.

amplifiers have a high input impedance, approaching infinity. The total disturbing voltage at the input terminals of the amplifier can now be determined using Figure 2.6(d).

The magnitude of the voltage source u_{dist} and the current source i_{dist} are

given by [42]

$$u_{dist} = j\omega\mu_0 A\overrightarrow{H} \tag{2.4}$$

and

$$i_{dist} = -j\omega CA\overrightarrow{E}, \tag{2.5}$$

respectively. Parameter A is the loop area given by the product of the length ($\mathcal{L}$) of the two-wire line and the distance between the conductors d. $\overrightarrow{H}$ and $\overrightarrow{E}$ are the magnetic and electric field components of the plane wave, respectively. The angular frequency of the plane wave is represented by $j\omega$ ($j = \sqrt{-1}$) and C is the capacitance per meter and follows from Table 2.1.

The orientation of the current source, i_{dist}, is as depicted in Figure 2.6. The orientation of the voltage source, u_{dist}, should be chosen such that the current resulting from this source generates a magnetic field that opposes the incident magnetic field [42]. The orientation of u_{dist} in Figures 2.6(b) to 2.6(d) thus complies with an electromagnetic field orientation as shown in Figure 2.6(a).

From the electric field the magnetic field can be calculated, by dividing it by the wave impedance (Z_w)

$$H = \frac{E}{Z_w}. \tag{2.6}$$

Using Figures 2.6(d) and 2.6(e) and Equations (2.4) and (2.5), the total disturbing signal due to an interfering plane wave can be determined.

$$\begin{aligned} u_{dist,tot} =& i_{dist}\frac{R_s + j\omega L_d\left(1 + j\omega R_s C_s\right)}{1 + j\omega R_s C_s + j\omega C_d\left(R_s + j\omega L_d\left(1 + j\omega R_s C_s\right)\right)} \\ &+ u_{dist}\frac{1 + j\omega R_s C_s}{1 + j\omega R_s C_s + j\omega C_d\left(R_s + j\omega L_d\left(1 + j\omega R_s C_s\right)\right)} \end{aligned} \tag{2.7}$$

and

$$\begin{aligned} i_{dist,tot} =& i_{dist}\frac{R_s}{R_s + j\omega L_d\left[1 + j\omega R_s\left(C_s + C_d\right)\right]} \\ &+ u_{dist}\frac{1 + j\omega R_s\left(C_d + C_s\right)}{R_s + j\omega L_d\left[1 + j\omega R_s\left(C_s + C_d\right)\right]}. \end{aligned} \tag{2.8}$$

The signal-to-disturbance ratio follows from $20\log\left(u_s/u_{dist,tot}\right)$ and $20\log\left(i_s/i_{dist,tot}\right)$, respectively.

Equation (2.7) for the voltage processing amplifier is dominated by the u_{dist} term, at least at lower frequencies. At higher frequencies, typically at the edge of validity of the model, i_{dist} can not be neglected anymore. However, for the major part of the frequency range it holds that u_{dist} determines $u_{dist,tot}$. Since u_{dist} is determined by the magnetic field, it can be concluded that voltage processing amplifiers are more susceptible to the magnetic field rather than the electric field component of the plane wave.

For the current processing amplifier, the dual case is found. Current source i_{dist} dominates Equation (2.8) which depends on the electric field. Therefore, it

can be concluded that current processing amplifiers are more susceptible to the electric field rather than to the magnetic field component of the plane wave.

Figure 2.8 shows the transfer (H_{pw}) of a plane wave to $u_{dist,tot}$ (dotted line). The interconnect is a two-wire ribbon cable with d =1.27 mm, r_w =190.5 μm and $\mathcal{L}_{\text{con}}$ = 20 cm. Source resistance is R_s = 10Ω and C_s = 1 pF. Up to approximately 150 MHz the interconnect can be regarded as electrically small. At 150 MHz the deviation of transfer H with the transfer obtained with the transmission line theory (Section 2.6.2) is about 2 dB. For lower frequencies, transmission line theory and the method presented in this section give the same results. The method presented in this subsection is, however, simpler.

2.6.2 Plane wave coupling to large interconnects

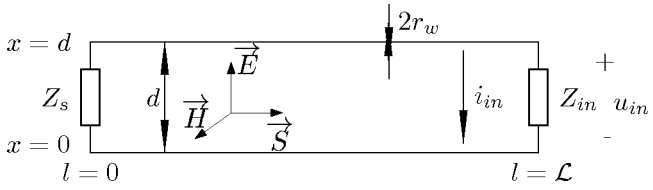


Figure 2.7: EM field coupling to an electrically-large interconnect. Note that the field may also have other orientations.

An interfering plane wave generates a disturbing current and voltage at the input terminals of the amplifier, see Figure 2.7. Under the condition that $d \leq \frac{\lambda}{2\pi}$ holds, current i_{in} and voltage u_{in} can be calculated with [68][72]:

$$\begin{aligned} i_{in}(\omega) = \; & \tfrac{1}{D}\textstyle\int_0^{\mathcal{L}} K(l,\omega)[Z_0\cosh\gamma l + Z_s\sinh\gamma l]dl + \tfrac{Z_0}{D}\int_0^d E_x^i(x,0,\omega)dx \\ & -\tfrac{1}{D}[Z_0\cosh\gamma\mathcal{L} + Z_s\sinh\gamma\mathcal{L}]\textstyle\int_0^d E_x^i(x,l,\omega)dx \qquad (2.9) \\ D = \; & (Z_0Z_s + Z_0Z_{in})\cosh\gamma\mathcal{L} + \left(Z_0^2 + Z_sZ_{in}\right)\sinh\gamma\mathcal{L} \\ u_{in}(\omega) = \; & i_{in}(\omega)Z_{in}, \end{aligned}$$

where Z_0 is the characteristic impedance of the interconnect, Z_s is the source impedance, Z_{in} is the input impedance of the amplifier, $E_x^i(x,0,\omega)$ is the electric field in the x direction (directed from the lower conductor to the upper conductor) incident on the source terminals, $E_x^i(x,l,\omega)$ the field in the x direction incident on the Z_{in} terminals, $\mathcal{L}$ is the length of the conductors, ω is the radial frequency of the field, and γ is the propagation constant of the line. $K(l,\omega)$ is the difference between the incident fields: $K(l,\omega) = E_l^i(d,l,\omega) - E_l^i(0,l,\omega)$, where $E_l^i(d,l,\omega)$ is the field incident in the length direction on the upper conductor and $E_l^i(0,l,\omega)$ is the field in the length direction incident on the lower conductor. Note that for the orientation of the plane wave in Fig. 2.7, K is zero since E_l is zero.

Solving the integrals for the field orientation depicted in Fig 2.7, results in:

$$\begin{aligned} i_{in}(\omega) =& E_x^i d \frac{Z_0}{D} \left\{ 1 - e^{-jk_0 \mathcal{L} \sin\Phi} \left(\cosh\gamma\mathcal{L} + \frac{Z_s}{Z_0} \sinh\gamma\mathcal{L} \right) \right\} \\ & - 2 \frac{E_l^i}{\gamma} \frac{Z_0}{D} \sinh\left(j \frac{k_0 d}{2} \sin\Psi \right) \left(\sinh\gamma\mathcal{L} + \frac{Z_s}{Z_0} (\cosh\gamma\mathcal{L} - 1) \right) \\ D =& (Z_0 Z_s + Z_0 Z_{in}) \cosh\gamma\mathcal{L} + \left(Z_0^2 + Z_s Z_{in} \right) \sinh\gamma\mathcal{L}, \end{aligned} \tag{2.10}$$

with $k_0 = \frac{2\pi}{\lambda}$ being the wave number of the plane wave, and Φ and Ψ are the angles that $\overrightarrow{S}$ makes with the interconnect.

Typically, disturbances at the termination on the amplifier side will show a 20 dB/dec increase with frequency. Anti-resonance points (i.e., maxima in the disturbance) and resonance points (minima) may occur. The first anti-resonance point typically gives the largest value of the disturbance and can be found at $f_p = \frac{v}{4\mathcal{L}}$ in case of resistive line termination, with v being the velocity of propagation on the line. The other anti-resonance and resonance points are found at $f_{ar} = nf_p$ and $f_r = (n-1)f_p$, respectively, with $n = 3, 5, 7 \cdots$. The exact resonance and anti-resonance frequencies may be shifted by a few percent when the terminations are formed by complex impedances instead of resistances.

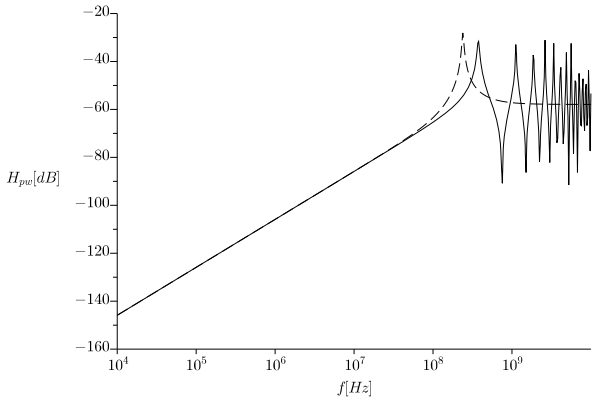


Figure 2.8: Transfer H_{pw} of a plane wave to a disturbing voltage at the input of a voltage processing amplifier. The orientation of the plane wave is depicted in Fig. 2.7. The interconnect is a two-wire ribbon cable with d =1.27 mm, r_w =190.5 μm and $\mathcal{L}_{\text{con}} = 20$ cm. Source resistance is $R_s = 10\Omega$ and $C_s = 1$ pF. The solid line is obtained with transmission line theory, the dashed line with the lumped model.

Attenuation factor α increases with frequency, thus increasing γ, and causes the depths of the anti-resonance points and the heights of the resonance points

to be diminished [68]. For this reason it may be expected that in practical cases f_p will indeed give the frequency at which maximal disturbance will occur.

Figure 2.8 shows with the solid line the transfer $H_{pw} = u_{in}/E$ for the interconnect presented in Subsection 2.6.1. Another example of the application of the presented equations can be found in [79][80], in which the disturbance induced in two-wire lines, twisted pairs, etc., by GSM phones is investigated using (among others) the method presented in this subsection.

2.6.3 Design for low plane wave coupling

The simplest and most straightforward measure that can be taken is to keep dimensions of the interconnect small. As long as the interconnect is electrically-small, the disturbance is inversely proportional to $\mathcal{L}$, i.e., a reduction of $\mathcal{L}$ of a factor two will also reduce the disturbance by a factor two. Moreover, a small distance (d) between the conductors causes lower values of u_{dist} and i_{dist}. The inductance of the interconnect decreases and the capacitance increases with decreasing distance. Designing (electrically-large) interconnects with a low value of $Z_0 = \sqrt{L/C}$ is thus beneficial.

Electrically-large interconnects may be designed such that the attenuation factor α, which forms the real part of γ, is large. This may be accomplished by designing for a relatively high conductor resistance, by selecting material with a high specific resistance, and a high value of the conductance G of the insulation between the conductors[7]. Since α increases with frequency, the beneficial effect on the transfer of interfering plane waves increases with frequency.

Higher values of the interconnect resistance and capacitance may, however, decrease the bandwidth of the interconnect too much, causing a distorted intended signal. Moreover, a higher value of R may decrease the signal to error ratio. A trade-off between the beneficial and detrimental effects of decreasing d and increasing R should be made in that case.

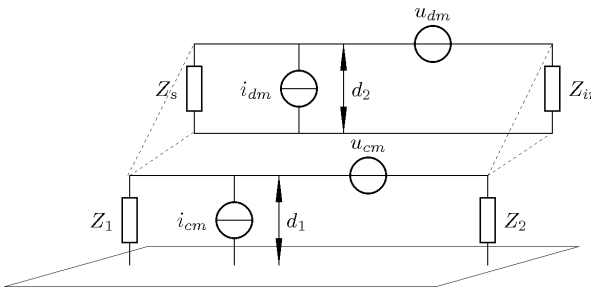
Another measure that can be taken is to prevent plane waves reaching the interconnect using shielding, e.g., by using a single conductive (ground) plane or a complete conductive enclosure. Shielding is discussed in Section 2.8. More about the positive effect of a conductive plane near an interconnect can be found in [68][43].

2.7 Differential and common-mode disturbances

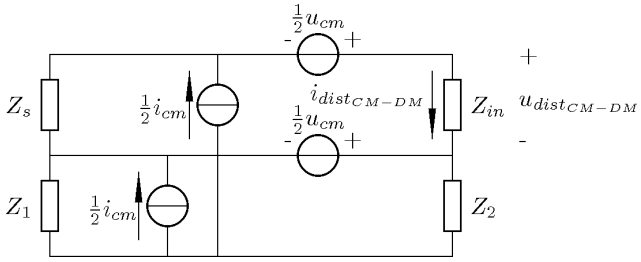
When disturbing signals are induced in an interconnect formed by, e.g., a wire over a conductive plane or a microstrip line, the disturbance is a differential signal and processed by the signal path comparable to the intended signal. When, however, an interconnect is placed over a conductive plane (which often occurs),

[7] Note that these recommendations are the opposite of the general case in which the intended signal has to be transferred and hence α should be as low as possible.

a disturbance is generated in the path formed by the conductive plane and the interconnect aside from the differential signal. This disturbance is called a common-mode disturbance, because it causes signals that are equal in magnitude and have the same direction [42] in both conductors of the interconnect. Common mode and differential-mode disturbances are elucidated in Fig. 2.9(a).



(a) The interconnect between Z_s and Z_{in} is connected via Z_1 and Z_2 to a conductive plane. Both common mode and differential-mode disturbance are induced in the interconnect. Note that usually holds $d_1 \gg d_2$.



(b) common-mode signals on interconnect

Figure 2.9: An interconnect is placed over a conductive plane. Differential-mode disturbances are generated in the path formed by both conductors of the interconnect, Z_s, and Z_{in}. Common-mode disturbances are generated in the path formed by the conductive plane, impedances Z_1 and Z_2 and the interconnect.

The common-mode disturbances can be found by using the same principles as discussed in Section 2.6, but now it is assumed that the conductor spacing in the interconnect is negligible compared with the distance between the interconnect and ground plane. All conductors in the interconnect are treated as a single wire with a diameter equal to the overall diameter of the interconnect. The disturbances found in this loop form the common-mode disturbances in the interconnect, which are assumed to divide equally among the conductors in the interconnect [68]. This is modelled in Fig. 2.9(b).

Although Figs. 2.9(a) and 2.9(b) present a representation valid for small interconnects, the discussion also holds for long interconnects. In the latter

case, the common-mode currents at the terminals of Z_{in} are of concern.

Note that the effective disturbing signal sources driving the common-mode disturbances are determined for a distance, d_1, to the ground plane that is much larger than the distance, d_2, between the conductors in the interconnect. Hence, the common-mode disturbances induced on the interconnect are much greater than the differential-mode disturbances [72][68]. The total disturbance at the terminals of the amplifier, i.e., at Z_{in} can now be evaluated.

The impedances Z_1 and Z_2 determine the total disturbance. Their effect is considered for the extremes of zero and infinite impedance. Four combinations are possible and they are evaluated for each of these four cases for both voltage and current processing amplifiers in Table 2.2. The disturbance voltage in the case of a voltage processing amplifier and the disturbing current in the case of a current processing amplifier are denoted $u_{dist_{CM-DM}}$ and $i_{dist_{CM-DM}}$, respectively. Just like in the previous cases, Z_s represents the source impedance and Z_{in} represents the input impedance of the amplifier[8].

Table 2.2: Common-mode to differential-mode conversion due to impedances Z_1 and Z_2.

Z_1	Z_2	$u_{dist_{CM-DM}}$	$i_{dist_{CM-DM}}$
∞	∞	0	0
∞	0	$\frac{i_{cm}}{2}\frac{Z_{in}Z_s}{Z_s+Z_{in}} \approx \frac{i_{cm}}{2}Z_s$	$\frac{i_{cm}}{2}\frac{Z_s}{Z_s+Z_{in}} \approx \frac{i_{cm}}{2}$
0	∞	$\frac{i_{cm}}{2}\frac{Z_{in}Z_s}{Z_s+Z_{in}} \approx \frac{i_{cm}}{2}Z_s$	$\frac{i_{cm}}{2}\frac{Z_s}{Z_s+Z_{in}} \approx \frac{i_{cm}}{2}$
0	0	$\frac{u_{cm}}{2}\frac{Z_{in}}{Z_s+Z_{in}} + \frac{i_{cm}}{2}\frac{Z_sZ_{in}}{Z_s+Z_{in}} \approx \frac{u_{cm}}{2} + \frac{i_{cm}}{2}Z_s$	$\frac{u_{cm}}{2}\frac{1}{Z_s+Z_{in}} + \frac{i_{cm}}{2}\frac{Z_s}{Z_s+Z_{in}} \approx \frac{u_{cm}}{2}\frac{1}{Z_s} + \frac{i_{cm}}{2}$

When both Z_1 and Z_2 are infinite, the common-mode signals cancel in Z_{in} (and Z_s) and no disturbing signal occurs [68]. This is equivalent to a balanced input.

When either Z_1 or Z_2 is zero, and the other infinite, only the common-mode currents will generate a disturbance. This is because making either Z_1 or Z_2 zero, short circuits the $i_{cm}/2$ current source of the conductor that is short circuited. Both common-mode voltages $u_{cm}/2$ are unaffected by the short circuit and cancel each other because they have the same sign.

[8]The model with the common-mode sources divided equally over both connectors as shown in 2.9(b) can also be used to determine common-mode to differential-mode conversion for other cases of imbalance, e.g., when Z_{in} is also loaded by an impedance at its top terminal.

When both Z_1 and Z_2 equal zero, both common-mode current and common-mode voltage determine the disturbing input quantities. Because the conductor is short circuited at both sides, both the lower common-mode current source and the lower common-mode voltage source are short circuited. It should be noted that $u_{cm}/2$ may be significantly larger than $i_{cm}/2$ (see, e.g., Equations (2.4) and (2.5)). Both $u_{dist_{CM-DM}}$ and $i_{dist_{CM-DM}}$ are typically dominated by $u_{cm}/2$.

Of course in practical situations neither Z_1 nor Z_2 will be zero or infinite. Using the models, the effect of different values of Z_1 and Z_2 between these extremes can readily be analyzed.

2.7.1 Decreasing the common-mode disturbance

The common-mode signals that are transferred to a differential total disturbance signal can be significantly decreased. Minimizing height d_1 is a simple and effective method.

Using a shielded cable as interconnect, e.g., a shielded two-wire, also decreases the common-mode signals. The common-mode signals are, ideally, confined within the shield and no conversion to a differential-mode disturbance signal at the input of the amplifier occurs. Shielded cables are, however, not ideal and some coupling to the amplifier input may still occur. See for instance, Subsection 2.8.2 and [41][9][34]. At the boundary of the interconnect and the amplifier, the shield should be connected to a highly conductive plate or enclosure. This shielding plate or enclosure forms a boundary between the common-mode signals and the amplifier. Sometimes a shield is called a current boundary for this reason [81].

Common-mode chokes are often recommended [9][34][43][41] because they effectively suppress a common-mode signal, while not affecting differential (i.e., the intended) signals [9]. A common mode choke may result in considerable reduction of the disturbance in the frequency range where it is effective, which may be limited up to, e.g., 30 MHz [9].

When the effect of a common-mode choke is evaluated for the situation depicted in Fig. 2.9(b) (and with the earlier presented combination of values of Z_1 and Z_2) it is found that it is only effective when both Z_1 and Z_2 are zero. It nullifies the $u_{cm}/2$ disturbance, but it does not affect the disturbance caused by $i_{cm}/2$.

2.8 Shield design

The disturbance from interfering sources can usually be reduced significantly when shielding with good conductive material is applied. Shield design is therefore dealt with briefly in this section. Appendix A presents a more in depth discussion.

The equations used to design the shield are taken from the work of Kaden [75]. In this work elaborate equations are presented for calculating shielding factors, $\mathcal{S}$, of conducting structures. These structures are: two (infinite) parallel

plates, the cylinder, and the sphere. The cylinder can be used to calculate the shielding factor of, e.g., a solid coax cable. The sphere is regarded as a good approximation for other three dimensional structures (enclosures) of the same volume. Shielding factor $\mathcal{S}$ is determined by both the shielding factor for magnetic, $\mathcal{S}_H$, and for electric fields, $\mathcal{S}_E$.

Shield design can in principle be straightforward. The shielding factor depends on the radius of the cylinder or the sphere (r_0), with respect to the wavelength of the interfering field, and the skin effect. In the region where $\lambda \gg r_0$, the shielding is determined by the conductor properties. When r_0 is of the same order of magnitude as (or larger than) λ, 'shielding breakdown' due to resonances occur. Shielding breakdown occurs at different frequencies for $\mathcal{S}_H$ and $\mathcal{S}_E$. Material that absorbs the EM energy can be used in this region to decrease the adverse effect of shielding breakdown. We will not elaborate on this. In this work the maximal frequency or maximal dimensions where the shield is effective will be determined.

Here, the following design strategy is proposed:

1. determine the conductor thickness for adequate $\mathcal{S}$ at the lowest interfering frequency

2. determine the maximum r_0 to prevent 'shielding breakdown' at the highest interfering frequency, or determine this frequency for a given r_0

Since $\mathcal{S}_H$ can be expected to determine $\mathcal{S}$ in case of $r_0 \ll \lambda$ ($\mathcal{S}_H \ll \mathcal{S}_E$, see Fig. A.1 on page 274, up to approximately 3 MHz), it suffices to design the shield for a certain minimal value of $\mathcal{S}_H$ at the lowest interfering frequency to be expected. Since $\mathcal{S}_H$ is determined by the attenuation of the magnetic field (a_s) in this frequency region (see appendix A), $\mathcal{S}_H$ increases with frequency, resulting in an even greater shielding factor for frequencies higher than designed for. $\mathcal{S}_E$ will automatically be sufficient also.

The required shield thickness, d, for a specified amount of a_s (e.g., $20\log|a_s|$= 40dB) and at a given frequency depends on the skin depth ($\delta = \sqrt{2\rho/(\mu\omega)}$), and can be approximated by

$$d \approx \begin{cases} a\frac{\mu_r\delta^2}{2r_0}\sqrt{10^{\left(\frac{a_s}{10}\right)}-1} & d < \delta \quad \text{('low frequencies')} \\ \delta\left[\ln\left(\frac{a\sqrt{2}\delta\mu_r}{r_0}\cdot 10^{\left(\frac{a_s}{20}\right)}\right)\right] & d > \delta \quad \text{('high frequencies'),} \end{cases} \tag{2.11}$$

which is derived from Equation (A.2), see page 272. The constant a equals 2 in the case of a cylinder and 3 in the case of a sphere.

Resonances in shielding (breakdown) are modelled by a correction factor (a_m). The shielding factor for magnetic fields is given by $\mathcal{S}_H = 20\log|a_s| + 20\log|a_m|$. The shielding factor for electric fields is $\mathcal{S}_E = 20\log|a_s| + 20\log|a_E|$. Correction factor a_E models both low and high-frequency electric field attenuation. Equations for both a_E and a_m are presented in appendix A.

The maximal dimensions of the shield should be smaller than the wavelength corresponding to the first resonance frequency, to prevent 'shielding breakdown'

due to resonances. An unacceptable decrease of $\mathcal{S}$ due to the frequency dependency of a_E or a_m, can be prevented by taking a slightly larger wavelength as lower limit. For cylindrical conductors, it is recommended to have a maximal radius of $r_0 = 0.25\lambda$, while for a spherical conductor a maximal radius of $r_0 = 0.4\lambda$ is recommended, and for a cube the maximal $a = 0.797\lambda$ is found [75].

For example, Equation (2.11) results in a thickness of 0.11 mm for a required $\mathcal{S}_H$ of 85 dB at 1 MHz for a copper sphere with r_0 =1 m. Proper shielding can be expected up to 120 MHz. When we have a copper cylinder with a radius of 6 cm and want to achieve a $\mathcal{S}_H$ of 40 dB at 30 kHz, a thickness d of 0.24 mm is found [75]. Up to 1.25 GHz there is proper shielding.

2.8.1 Shield design considerations

Factor $20 \log |a_s|$ gives rise to extremely large attenuation values for frequencies higher than, e.g., 10 MHz. In practice, these large attenuation values are not reached, since the necessary openings for interconnect feed through limit the reachable attenuation. Kaden proposes to use an upper limit of 12 Np (i.e., 104 dB) [75] since larger attenuations are hardly verifiable by measurements [82]. This upper limit is used when calculating $\mathcal{S}_H$ and $\mathcal{S}_E$ in Fig. A.1 [75].

Apertures in the enclosure are inevitable, so the practical upper limit makes sense. In order to maintain a high practical upper limit, one has to take care that currents can flow as unaffected by the apertures as possible. Large round apertures and slits do affect the current flow in the shield and therefore the shielding factor is reduced. It is better to use many small round holes instead of one big one for, e.g., cooling purposes [42]. A slit reduces the homogeneity of the current flow and a voltage is induced over the slit. Therefore electric and magnetic fields can enter the enclosure. In case of round holes, this also occurs, but now the current flow is much more homogeneous and therefore much less electric and magnetic energy enters the enclosure [41]. Apertures that are inevitable should therefore be round.

Holes in the enclosure should preferably be realized as cylinders perpendicular to the enclosure [75]. The attenuation ('Kamindämpfung'; 'Kamin' or 'chimney' damping) of these cylinders is $a_{k_E} = 20.85\frac{l}{r_0}$ [dB] for electric fields and $a_{k_H} = 15.98\frac{l}{r_0}$ [dB] for magnetic fields, with l being the length of the cylinder and r_0 the radius of the cylinder[9]. Cylinders with an $\frac{l}{r_0}$ ratio of 6 to 8 will thus provide enough attenuation [82]. The diameter of the cylinder should remain several times smaller than the wavelength of the interfering fields, in order to remain a waveguide beyond cut-off [82]. The corner wavelength for a cylindrical waveguide beyond cut-off is $\lambda_c = \frac{2\pi r_0}{1.841}$ [41]; the equations for the 'Kamindämpfung' are thus valid as long as $\lambda \gg \lambda_c$.

For additional practical guidelines in realizing and building shielding enclosures, the reader is referred to readily available EMC textbooks, e.g., [41][9][34].

[9]Kaden points out that the equations for the Kamindämpfung are accurate when l is larger than or of the same magnitude as r_0.

2.8.2 Surface transimpedance

When the signal paths (interconnects) and source and load are completely shielded, ideally no undesired EM coupling from external signal paths exists. This would be true when the shield is ideal, i.e., it would be a perfect conductor. Since the shield is not a perfect conductor (because, e.g., holes are present) currents induced by EM fields will penetrate the shield and produce a voltage distribution along the inside length of the shield. This voltage distribution in turn produces a current in the interior source and load impedances [68].

A typical way of calculating the EM coupling through a shield is to first calculate the current induced on the shield exterior by the incident field, assuming that the shield is a perfect conductor and completely encloses the internal signal path [42]. This shield current, i_{sh} diffuses through the shield wall to give a voltage drop on the *interior surface of the shield*, $du_{dist} = i_{sh} Z_t dx$. Z_t is the called the transfer impedance in EMC literature, e.g., [41][42][26]. Electronics engineers are more familiar with the name transimpedance to describe a current to voltage transfer ($u_{dist} = i_{sh} Z_t$). In this work the name transimpedance will therefore be used. Equivalently, a disturbing current inside a shield due to a voltage across the shield and the reference, may be calculated by using the concept of transadmittance (Y_t); transfer admittance in EMC literature. The current is given by $i_{dist} = u_{sg} Y_t$, where u_{sg} is the voltage between the shield and the reference conductive plane.

The approach of calculating a disturbing voltage inside a shield by using the concept of Z_t is equally valid for any shield, e.g., coax, triax, shielded pair, shielded multi-conductor, shielded multicoax, etc. [68], but it may, for instance, also be used in pcb design and grounding [83][84].

Solid coaxial shields usually show a low Z_t. For a solid cylindrical shield around an interconnect, Z_t in [Ω/m] is [75][42]

$$Z_t = \frac{1}{\sigma \pi D_m d} \frac{d\frac{1+j}{\delta}}{\sinh d\frac{1+j}{\delta}}, \tag{2.12}$$

with $D_m = 2r_0$ being the inner diameter of the shield, d the shield thickness, and $\sigma = 1/\rho$ the conductance of the material. For shield thicknesses less than a skin depth, $d \ll \delta$, the transimpedance reduces to the resistance $R_t = \frac{1}{\pi \sigma D_m d}$ since the shield current can completely diffuse to the interior of the shield. For wall thicknesses greater than a skin depth, the current on the exterior of the shield only partly diffuses through the shield wall, and Z_t decreases with increasing frequency. The interior and exterior of the shield are becoming isolated due to the skin effect. For a completely closed cylinder (e.g., a copper cylinder), Z_t will soon become negligibly small for frequencies at which the skin depth is effective.

When we have a braided shield, holes are present in the shield through which EM fields may leak. This causes Z_t to become inductive[10]. For instance, Z_t may be approximated by $Z_t \approx j\omega\mu_0 \frac{2}{3\pi^2} \frac{pr_o}{0.5 D_m}$ [75] in case of circular holes, with r_o

[10] Typically at approximately 1 MHz, Z_t will become dominated by the inductances according to graphs of Z_t for various types of coax cables and shielded cables in [41] and [9].

being the radius of the holes and $p = \frac{\nu r_o^2}{D_m}$. Parameter ν is the number of holes across the length $\mathcal{L}$ of the braid. Equations for calculating the effects of the properties of the braid on Z_t for practical coax cables, can be found in [85]. The equation for Z_t presented here is, however, simple and general design rules follow from it. It shows that Z_t for a given p increases with increasing r_o. Moreover, a large number of small holes is better than a small number of large holes, under the assumption that the total area remains equal [75].

2.8.3 Shielded electrically-small systems

Sometimes it is impossible to reduce the dimensions of an interconnect enough to obtain acceptable levels of disturbance. This may be the case when, e.g., another design requirement demands the interconnect to have some minimum dimensions that are too large from an EMI point of view. Reduction of the disturbance can now be obtained by shielding the system.

The disturbing signal source at the input of amplifiers can be determined by calculating the shield current (i_{sh}) and multiplying it with Z_t. An equation for i_{sh} is derived for a plane wave oriented as depicted in Fig. 2.7 from the transmission line equations presented in [68]. For other field directions the reader is referred to [68], but similar results can be expected. The shield current can be calculated from the average voltage that is induced across the shield by the EM-field. The average voltage that is induced is given by [68]

$$u_{sha} = E_x \frac{h}{2}(1 - e^{-jk_0\mathcal{L}})\mathcal{L}, \tag{2.13}$$

with h being the height of the shielded interconnect above a conductive plane, and $k_0 = 2\pi/\lambda$ being the wave number[11]. Since the shield is electrically short, $k_0\mathcal{L} < 1$, it was found (using the method described in [42]) that this equation can be very well approximated by[12]

$$u_{sha} \approx j\omega\mu_0 H\mathcal{L}h, \tag{2.14}$$

which is similar to Equation 2.4.

The shield current can now be determined with $i_{sh} = u_{sha}Y_t$. Transadmittance Y_t can be determined from Fig. 2.3(c), when low termination impedances Z_1 and Z_2 are assumed, which is the recommended case [41]. For Y_t is found

$$Y_t = \frac{1}{Z_2 + j\omega\frac{L_{sh}}{2} + \frac{Z_1 + j\omega\frac{L_{sh}}{2}}{1 + j\omega C_{sh}(Z_1 + j\omega\frac{L_{sh}}{2})}}. \tag{2.15}$$

Shield parameters L_{sh} and C_{sh} can be calculated using the equations presented in Table 2.1 (second row).

[11] For an electrically-small system holds $\mathcal{L} \leq 0.1\lambda$, resulting in a maximal wave number of $2\pi/(10\mathcal{L})$.

[12] Comparison of both equations showed a deviation of less than 2 % for short shields.

The disturbance voltage source ($u_{dist,sh}$) that appears at the input of the amplifier (see Figs. 2.6(d) and 2.6(e)) can now be determined. This voltage source equals $u_{dist,sh} = u_{sha} Y_{shield} Z_t$. The total disturbing signal (either current or voltage) at the input of a current processing and voltage processing amplifier can now be determined using Equations (2.7) and (2.8). The lumped parameters L_d and C_d are those of, e.g., coax.

Since u_{sha} has a zero in the origin, i_{sh} increases at a rate of 20 dB/dec up to the pole in Y_{shield}, after which it remains constant[13]. Disturbance voltage source $u_{dist,sh}$ equals $u_{sha} Y_{shield} Z_t$.

Compared to an unshielded interconnect with the same dimensions and height as a shielded one, $u_{dist,sh}$ appears to be a factor (the shielding factor) lower. This shielding factor may be approximated by

$$\mathcal{S} = \frac{u_{dist}}{u_{dist,sh}} \approx \frac{Z_1 + Z_2 + j\omega L_{sh}}{Z_t}. \tag{2.16}$$

For a high $\mathcal{S}$, the transimpedance Z_t should be as small as possible. The inductive part of Z_t should at least be much (e.g., 100 times) smaller than L_{sh}.

Although high values of the terminating impedances Z_1 and Z_2 seem beneficial (Z_1 and Z_2 in Fig. 2.3(c)), effort has to be made to keep them as low as possible, since high terminating impedances may cause capacitive coupling of a disturbance. This means that, e.g., pigtails to terminate the shield have to be avoided since they cause Z_1 and Z_2 to become inductive and hence deteriorate $\mathcal{S}$ with increasing frequency. Apart from that, direct inductive and capacitive coupling to the interior shielded wire over the length of the pigtail section occurs [42].

2.8.4 Shielded electrically-large systems

The design recommendations given in the subsection about shielded electrically-small systems also hold for large systems. The main difference encountered is that reflections in the shield may occur that degrade the shielding.

In case of a lossless shield, the current and voltage at the input of the amplifier

[13] At frequencies lower than the pole, the results of this equation are the same as will result from the transmission line approach [68] that will be presented in Section 2.8.4. For frequencies where i_{sh} remains constant, it is overestimated with an amount dependent on h. It was found that up to an $h = 50$ cm the overestimation is about 6 dB. Smaller heights result in smaller overestimations. This is acceptable.

is calculated with [68]

$$\begin{aligned} i_{in} =& E_x h \frac{Z_t \mathcal{L}}{PD} \int_0^{\mathcal{L}} \Big[\Big\{ (Z_0 - Z_1) \sin k_0 \mathcal{L} \sin k_0 l + j(Z_0 + Z_2) \sin k_0 \mathcal{L} \cos k_0 l \\ & - j(Z_1 + Z_2) \cos k_0 \mathcal{L} \sin k_0 l \Big\} \cdot \{ Z_c \cos k_{0i} l + j Z_s \sin k_{0i} l \} \Big] dl \\ P =& (Z_c Z_s + Z_c Z_{in}) \cos k_{0i} \mathcal{L} + j(Z_c^2 + Z_s Z_{in}) \sin k_{0i} \mathcal{L} \\ D =& (Z_0 Z_1 + Z_0 Z_2) \cos k_0 \mathcal{L} + j(Z_0^2 + Z_1 Z_2) \sin k_0 \mathcal{L} \\ u_{in} =& i_{in} Z_{in}, \end{aligned} \tag{2.17}$$

under assumption of a plane wave exiting the shield as depicted in Fig.2.7. With h being the height of the shield over the conductive plane, Z_0 being the characteristic impedance of the shield treated as a single wire over a conductive plane, Z_1 and Z_2 being the termination impedances of the cable shields (also treated as a single wire over a conductive plane). $\mathcal{L}$ is the length, and $k_0 = 2\pi/\lambda$ is the wave number. Z_c is the characteristic impedance of the interconnect inside the shield, and k_{0i} is the wave number of the interconnect inside the shield. Z_s is the source impedance and Z_{in} is the load impedance of the interconnect, i.e., the input impedance of the amplifier. E_x is the electric field component parallel to the terminations of the shielded signal path. For other directions of the EM field the interested reader is referred to [68].

At low frequencies, the equation given here gives the same result as the method presented in Subsection 2.8.3. Current i_{in} at the input terminals of the amplifier, shows a 20 dB/dec increase, which is consistent with the increase in Z_t with frequency. At higher frequencies, the resonance and anti-resonance points due to reflections are damped out when $Z_1 = Z_2 = 0$ and $Z_s = Z_{in} = Z_c$. When either Z_1 or Z_2 is infinite, i.e., an open end occurs, resonances start to occur that decrease the effectivity of the shield [68]. The shield should thus be connected at both sides to the reference via low impedances.

To simplify the design of shielded long interconnects, the equations given in Subsection 2.8.3 can be used. After all, up to the frequency that the interconnect becomes long, both the method for small interconnects and the one for long interconnects give the same result. An electrically-small shield with an appropriate $\mathcal{S}$, may be expected to have an appropriate $\mathcal{S}$ also when it becomes electrically-large as long as termination impedances Z_1 and Z_2 are low (zero). When the source impedance and the (input) impedance of the system (amplifier) are not matched to the characteristic impedance of the internal interconnect, reflections may occur that may increase the disturbance, as is the case for the unshielded long interconnect.

Better shielding behavior may be expected when the electrically-long shield is made electrically small by connecting it to the reference (ground) at multiple points spaced $\leq \lambda/10$ from each other [42]. The shielding factor $\mathcal{S}$ may than be estimated by using approximations valid for electrically-small systems.

2.9 Conclusions

The fidelity of the transfer of an amplifier is hampered by noise generated in the amplifier and by disturbances that may be in-band or out-of-band. This chapter deals with the interconnect properties. The interconnect properties may influence (low-pass filter) the transfer of the intended signal (e.g., from source to the amplifier) and determine the amount of disturbance coupled to the amplifier. These properties depend on the dimensions of the interconnect.

Equations that enable the designer to estimate the amount of disturbance coupled to the interconnect, and to determine the maximal dimensions of the interconnect for both the intended signal and the disturbance are presented. The presented equations are valid for plane-wave (far-field) coupling to both electrically-short and electrically-large interconnects, under assumption that the distance between the conductors remains smaller than $\lambda/(2\pi)$. Cross-talk (near-field) coupling is not considered.

Both common-mode and differential-mode disturbance can occur. Since common-mode loops are usually larger than differentia-mode loops, common-mode disturbance is usually larger also. Balancing the impedances that terminate the interconnects cancels the common -mode disturbance. Imbalances in these impedances causes common-mode to differential-mode conversion, thus increasing the total disturbance. A model and equations that can be used to analyze this effect are presented.

In general, it may be concluded that the smaller the dimensions of the interconnect, the smaller the disturbance coupled to it. Sometimes, other design requirements demand interconnect dimensions larger than allowed from a disturbance point of view. In that case, shielding may be applied. Equations to facilitate the design of shields (for both interconnects and enclosures) are also presented.

Chapter 3

Modelling of active devices

Active devices are the building blocks of (negative-feedback) amplifiers. There are three types of relevant active semiconductor devices: the bipolar junction transistor (BJT), the metal oxide semiconductor field effect transistor (MOSFET) and the field effect transistor operating with a reverse biased gate-source junction. Both the junction field effect transistor (JFET) and the metal semiconductor field effect transistor (MESFET) belong to the latter type.

In Chapter 1 was shown that nonlinear behavior of active devices results in distortion and susceptibility to electromagnetic interference (EMI). A thorough understanding of the three transistor types is necessary to be able to calculate nonlinear effects and to come to a design method for minimizing EMI in negative-feedback amplifiers. The subject of this chapter is to investigate the nonlinear behavior of the transistors and to present simplified models that can be used to calculate nonlinear effects. We strive for compatibility with the models used by circuit simulators like SPICE (simulation program with integrated circuit emphasis). SPICE model parameters are readily available and therefore convenient for use in EMI related analysis and design.

Section 3.1 discusses the BJT. The physics of the BJT is very well understood and accurately described by mathematical equations from the HICUM [86], MEXTRAM [87], and the Gummel-Poon [88] models. The HICUM and MEXTRAM models of BJTs are standardized by the Compact Model Council (CMC). These models accurately describe BJT behavior over a large bias current range (low and high-current effects) and at both low and high-frequencies. The Gummel-Poon model is less accurate than the HICUM and MEXTRAM models in describing, e.g., high-current effects and high-frequency effects. The design method, however, requires simple equations and models that enable hand calculations and give insight. For design purposes, a simple circuit model is therefore derived from the Gummel-Poon model that is valid for analyzing linear and second-order nonlinear behavior. It is comparable to the small-signal [57] hybrid-π model, which is only suited for linear analysis.

MOSFET modelling has been troublesome due to poor accuracy and complexity of the equations describing the physics of the MOSFET. This resulted in poor

accuracy from distortion calculations. Here, the results of the investigations of van Langevelde [89][90] will be used to model distortion more accurately, hence EMI effects will be modelled more accurately also. The results of van Langevelde et al. are used in Philips (now NXP) MOS model 11 [91], which is one of the roots of the CMC standard PSP model [92]. The MOSFET is discussed in Section 3.3. Finally, the JFET is discussed in Section 3.5 and the MESFET in Section 3.6.

Limitations of the validity of the models in this chapter are also presented. A limitation common to all models is that current and voltage breakdown due to excessive bias voltages and/or currents are not modelled. Breakdown effects are detrimental for the transistors.

3.1 The bipolar junction transistor

A large-signal model of the BJT is shown in Fig.3.1. It is a slightly modified version of the well-known Gummel-Poon model. It is modified such that it is only valid in the forward active region, i.e., the base-emitter is forward biased and the base-collector is reverse biased or short circuited, and a capacitance between the base terminal and the collector is added to model the distributed base-collector capacitance more effectively than is done in the original Gummel-Poon model[1] [88]. The actual derivation of the equations describing the movement of charge carriers is beyond the scope of this work. Specialized literature covers this subject [57].

The parasitic semiconductor material resistances r_B, r_E and r_C are easily identified. The nonlinear base-emitter voltage to base current transfer is modelled by two diodes. The left diode models the (usually dominating) base current I_{b1} and the right diode models the recombination current I_{b2} in the base-emitter depletion area.

Capacitances C_{je} and C_{de} represent the base-emitter junction and the base-emitter depletion capacitances, respectively. The capacitances C_{jc} and C_{bx} represent the distributed capacitance of the base-collector junction. C_{js} is the junction capacitance from the collector to the substrate in case of a monolithic npn BJT. Lateral pnp BJTs have a parasitic capacitance C_{bs} from base to substrate in place of C_{jc} [57]. This capacitance is also connected to the substrate, just like C_{js}. Discrete BJTs do not possess C_{js} or C_{bs}.

Finally, the nonlinear base-emitter voltage to collector current transfer is modelled by the voltage-controlled current source $I_c(U_{be})$. In the forward active region the collector current, I_c, is given by:

$$I_c = I_s e^{\frac{qU_{be}}{n_f kT}} \left(1 - \frac{U_{bc}}{U_{AF}}\right), \tag{3.1}$$

under assumption that no self heating, avalanche breakdown, etc., occurs. I_s is the saturation current, which is a measure of the minority carrier concentration

[1] Modern simulators like SPICE also use an extra capacitor to model the distributed collector-base capacitance [93].

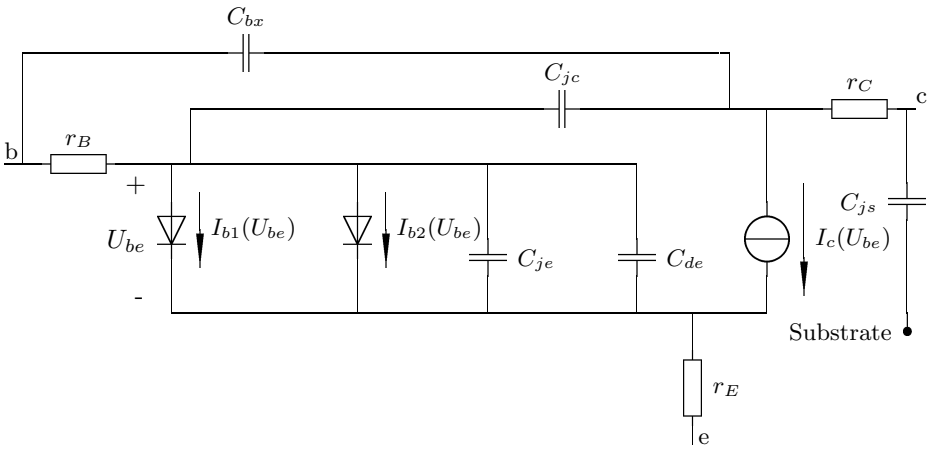


Figure 3.1: Modified Gummel-Poon model of a npn transistor. Valid for the forward region $U_{be} \geq 0$, $U_{bc} \leq 0$. Base current is modelled by the currents through both diodes. Collector current is represented by the voltage-controlled current source, $I_c(U_{be})$. Base-emitter capacitances are modelled by C_{je} and C_{de}, base-collector capacitance is modelled by both C_{jc} and C_{bx}, and C_{js} represents the collector-to-substrate capacitance. In discrete devices C_{js} is absent.

in the base [57], U_{be} is the base-emitter voltage, q is the electron charge, n_f is the forward emission coefficient (normally close to one), k is Boltzmann's constant and T is the temperature in Kelvin. U_{bc} is the base-collector voltage and U_{AF} is the Early-voltage.

The base-current is given by

$$I_b = I_{b1} = \frac{I_s}{\beta_f} e^{\frac{qU_{be}}{n_f kT}}, \tag{3.2}$$

where β_f is the forward current amplification factor. Recombination current I_{b2} is disregarded, because it represents a secondary effect.

In this work, the following symbol convention is used: an uppercase symbol with a lowercase subscript is used for the total voltage or current, i.e., the sum of the DC or bias quantity and the AC quantity. For example, I_c is the sum of the DC bias collector current and the (small-signal) AC collector current. Bias quantities are represented by an uppercase symbol with in the lowercase subscript an uppercase 'Q', e.g., I_{cQ} is the DC bias collector current. Small signal and AC quantities are represented by lowercase symbols with lowercase subscripts, e.g., i_c is the (small-signal) collector current. The amplitude or peak value of an AC quantity is indicated by '$\hat{}$' over the symbol, e.g., $\hat{i}_c$ is the amplitude of the small-signal collector current.

3.1.1 Deriving the components of the hybrid-π model

The Gummel-Poon model accurately describes the large-signal nonlinear behavior. For design purposes a simplified hybrid-π equivalent based on a first-order Taylor series approximation of the Gummel-Poon model is used. It is therefore only valid for small signals and nonlinear behavior is completely disregarded. For the investigation of EMI performance the model will be modified to include second-order nonlinear behavior.

A. Conductances

In case the BJT is forward biased, the BJT's response to an input voltage can be determined using Equations (3.1) and (3.2). For a sinusoidal input voltage u_{be} with an amplitude smaller than $\frac{2kT}{q}(\approx 52mV@300K)$, the resulting currents can be determined by means of a Taylor series [44][94][10]. Larger amplitudes require the use of modified Bessel-functions [10]. In well-designed negative-feedback amplifiers, it may be expected that signal amplitudes at the input of the BJT will almost always remain much lower than $\frac{2kT}{q}$, so this work will be limited to the Taylor expansion.

The general Taylor expansion for a device with a nonlinear $U-I$ characteristic is:

$$\begin{aligned} I_o = &\quad I_{oQ}(U_{dcQ}) + u_i a_1 + u_i^2 a_2 + \cdots + u_i^n a_n, \\ \text{where} \quad a_n = &\quad \frac{1}{n!}\frac{d^n I_{oQ}}{du_i^n}\bigg|_{U_{dcQ}}. \end{aligned} \tag{3.3}$$

The term a_1 in the expansion is the transistor transconductance g. Term a_2 is called the quadratic detection [10] or quadratic term [44], and is mainly responsible for a DC-shift and an output current component at twice the frequency of the input signal, i.e., a second harmonic of the input signal is generated. The higher order terms will generate higher harmonics of the input signal. This will be elaborated upon in Chapter 5.

EMI is primarily caused by the second-order term a_2. The hybrid-π model that is going to be presented will be sufficiently accurate to model both linear and quadratic effects. The expansion is therefore truncated after the second term. The remainder for the series truncated to n terms is defined to be $R_n(u_i) = I_o - [I_{oQ}(U_{dcQ}) + \Sigma_{k=1}^{n} u_i^n a_n]$ [44]. An upper bound for this remainder is given by the inequality $R_n(u_i) \leq |u_i|^{n+1}((n+1)!)^{-1}\left(q/(n_f kT)\right)^{n+1} \cdot I_o$ for the BJT [44]. The normalized truncation error is defined as the remainder R_n of the series divided by the value of the function being expanded [44]. For the BJT this results in

$$\begin{aligned} \mathcal{E}_n = &\quad \frac{R_n(\hat{u}_{be})}{I_o} \leq \frac{1}{(n+1)!}\left(\frac{q\hat{u}_{be}}{n_f kT}\right)^{n+1}, \\ \text{and} \quad \mathcal{E}_2 \leq &\quad \frac{1}{6}\left(\frac{q\hat{u}_{be}}{n_f kT}\right)^{3} \end{aligned} \tag{3.4}$$

for both base and collector current [44], where $\hat{u}_{be}$ is the amplitude of the base-emitter voltage. From Equation (3.4) it follows that the error we introduce is smaller than 1 percent for $\hat{u}_{be}$ up to 10 mV and smaller than 10 percent for $\hat{u}_{be}$ up to 22 mV. For BJTs used in negative-feedback amplifiers these are rather large voltages often leading to clipping distortion. Soft nonlinear behavior occurs when $\hat{u}_{be}$ remains small enough to avoid clipping distortion. In that case the following analysis holds.

Applying (3.3) to (3.1) and omitting the DC component gives as Taylor coefficients the transconductances, g_{mn}, of the n^{th} order, $n = 1, 2, 3 \cdots \infty$. Note that $g_{m1} = a_1$ and $g_{m2} = a_2$.

$$g_{mn} = \frac{1}{n!}\left(\frac{q}{n_f kT}\right)^n I_s e^{\frac{qU_{beQ}}{n_f kT}}\left(1 - \frac{U_{bcQ}}{U_{AF}}\right) = \frac{1}{n!}\left(\frac{q}{n_f kT}\right)^n I_{cQ} \tag{3.5}$$

The first two terms of (3.5) are

$$g_{m1} = \frac{q}{n_f kT} I_s e^{\frac{qU_{beQ}}{n_f kT}}\left(1 - \frac{U_{bcQ}}{U_{AF}}\right) = \frac{q}{n_f kT} I_{cQ} \quad [\mathrm{A/V}] \tag{3.6}$$

for the linear component of the transconductance and

$$g_{m2} = \frac{1}{2}\left(\frac{q}{n_f kT}\right)^2 I_s e^{\frac{qU_{beQ}}{n_f kT}}\left(1 - \frac{U_{bcQ}}{U_{AF}}\right) = \frac{1}{2}\left(\frac{q}{n_f kT}\right)^2 I_{cQ} \quad [\mathrm{A/V^2}] \tag{3.7}$$

for the second-order component of the transconductance.

The transconductance can be modelled by a nonlinear voltage-controlled current source i_c in a hybrid-π circuit representation of the equations. The current it delivers is equal to $g_{m1}u_{be} + g_{m2}u_{be}^2$, where u_{be} is the small-signal base-emitter voltage.

If the same is done with Equation (3.2) the following equations give the input conductances of the hybrid-π model.

$$g_{\pi 1} = \frac{q}{n_f kT}\frac{I_s}{\beta_f} e^{\frac{qU_{beQ}}{n_f kT}} \quad [\mathrm{A/V}] \tag{3.8}$$

$$g_{\pi 2} = \frac{1}{2}\left(\frac{q}{n_f kT}\right)^2 \frac{I_s}{\beta_f} e^{\frac{qU_{beQ}}{n_f kT}} \quad [\mathrm{A/V^2}] \tag{3.9}$$

It is, however, more customary to use input resistance r_π instead of $g_{\pi 1}$. The linear, and also the higher order, input resistances can be determined from the conductances by using inverse functions, e.g. [60]. The linear component of the input resistance can be determined from:

$$\frac{d}{dI_{bQ}} U_{beQ} = \left(\frac{d}{dU_{beQ}} I_{bQ}\right)^{-1} \tag{3.10}$$

resulting in :

$$r_\pi = \frac{1}{g_{\pi_1}} = \frac{\beta_f}{\left(\frac{q}{n_f kT}\right) I_s e^{\frac{qU_{beQ}}{n_f kT}}}. \tag{3.11}$$

r_π is modelled as a resistor between the internal base and emitter terminals, while the effect of $g_{\pi 2}$ can be modelled by a voltage-controlled current source, i_{b2}, of value $u_{be}^2 g_{\pi 2}$ shunting r_π.

Evaluating Equation (3.1) again, it can be concluded that I_c also depends on the base-collector voltage U_{bc}. When a Taylor expansion is performed with U_{bc} as variable, a linear output conductance is found:

$$g_o = \frac{I_s e^{\frac{qU_{beQ}}{n_f kT}}}{U_{AF}}. \tag{3.12}$$

Written as output resistance:

$$r_o = \frac{U_{AF}}{I_s e^{\frac{qU_{beQ}}{n_f kT}}}. \tag{3.13}$$

Output resistor r_o is to be modelled by a resistor in parallel with the voltage-controlled current source i_c.

It should be noted that voltages u_{be} and u_{ce} both change simultaneously. This causes a cross product in the collector current given by $i_{\text{cross}} = u_{be} u_{ce} g_x$, with $g_x = di_c/(du_{be} du_{ce})$ given by

$$g_x = \frac{q}{n_f kT} \frac{I_s e^{\frac{qU_{beQ}}{n_f kT}}}{U_{AF}} = \frac{q}{n_f kT} g_o \tag{3.14}$$

The detrimental effect of i_{cross} is expected to decrease with frequency, since u_{ce} typically decreases for frequencies higher than the amplifier bandwidth. Further, designing or selecting a BJT with a large Early voltage (U_{AF}) is beneficial for a low value of g_x (see also page 76).

In the Gummel-Poon model the Early voltage is assumed to be a constant [88]. Bipolar transistors having a relatively large base width indeed poses a constant U_{AF}. For BJTs with a base width below 0.1 μm, U_{AF} can however not be regarded as a constant anymore [95]. At low values of U_{bcQ}, U_{AF} is smaller than the constant value used by Gummel and Poon (and SPICE). For increasing U_{bcQ}, U_{AF} also increases until it becomes a constant that may be larger than the constant used by Gummel and Poon[2]. Detrimental (nonlinear) effects resulting from low U_{AF} are easily solved in the design process by cascoding the transistor and are therefore not considered further in this thesis. Current i_{cross} can also be made negligible by cascoding.

B. Capacitances

Finally, the nonlinear behavior of the capacitances has to be evaluated. The base-emitter capacitance, C_π, is determined by the sum of the base-emitter junction and the base-emitter diffusion capacitances. The diffusion capacitance

[2]The effects of bias dependent U_{AF} can be analyzed by performing simulations using the MEXTRAM model [87].

C_{DE} models the charge associated with the mobile carriers in the transistor, while the junction capacitance C_{JE} models the incremental fixed charge stored in the base-emitter space charge layer. When Q_{de} represents the charge associated with the collector current I_c, it holds that

$$Q_{de} = \tau_f I_c, \tag{3.15}$$

where τ_f is the base transit time in the forward direction [57]. Changes in charge due to changes in the base-emitter voltage u_{be} are given by [44]:

$$q_{de} = \tau_f \sum_{n=1}^{\infty} g_{mn} {u_{be}}^n \tag{3.16}$$

The incremental diffusion current equals the change of q_{DE} with time:

$$i_{de} = \frac{dq_{de}}{dt} = \frac{d}{dt}\left(\tau_f \sum_{n=1}^{\infty} g_{mn} {u_{be}}^n\right) = \tau_f \sum_{n=1}^{\infty} n g_{mn} {u_{be}}^{n-1} \frac{du_{be}}{dt} \tag{3.17}$$

The linear diffusion capacitances and the higher-order nonlinear capacitances can be derived from this equation.

The nonlinear base-emitter junction capacitance is given by [57][44]

$$C_{je} = \frac{C_{JE0}}{\left(1 - \frac{U_{beQ}}{\Phi_E}\right)^{m_E}}. \tag{3.18}$$

C_{JE0} is the value of the base-emitter junction capacitance at $U_{beQ} = 0$, Φ_E is the base-emitter built-in potential, m_E is the base-emitter capacitance grading factor, and the subscript Q represents the bias point. The base-emitter capacitance grading factor is often approximated by $m_E = 0.5$ under assumption of constant doping p-type and n-type regions and by $m_E = 1/3$ under assumption of a graded doping profile [57].

The capacitances C_{jc}, C_{bx} and C_{js} are all three junction capacitances and can be calculated in a similar manner as C_{je}.

$$\begin{aligned} C_{jc} &= \frac{C_{JC0}}{\left(1 - \frac{U_{bcQ}}{\Phi_C}\right)^{m_C}} \\ C_{bx} &= \frac{C_{JC0}}{\left(1 - \frac{C_{bxcQ}}{\Phi_C}\right)^{m_C}} \\ C_{js} &= \frac{C_{JS0}}{\left(1 - \frac{U_{csQ}}{\Phi_S}\right)^{m_S}}. \end{aligned} \tag{3.19}$$

Capacitances C_{jc} and C_{bx} are lumped approximations of the distributed capacitances between base and collector, see Figure 3.1. Capacitance C_{JC0} is the value of the, intrinsic, base-collector junction capacitance at $U_{bcQ} = 0$, Φ_C is

the base-collector barrier potential and m_C is the base-collector grading factor, $m_C = 0.5$ under assumption of constant doping p-type and n-type regions and by $m_C = 1/3$ under assumption of a graded doping profile [57]. The capacitance between the external base terminal and the collector is represented by C_{bx}. Finally, U_{bxcQ} is the bias voltage between the external base terminal and the intrinsic collector. C_{JS0} is the collector-substrate capacitance at zero bias voltage, Φ_S is the built-in voltage, U_{csQ} is the collector-substrate voltage, and m_S is a grading factor again.

Equation (3.17) and either (3.18) or (3.19) can be evaluated for second harmonic distortion and envelope detection properties.

C. Second harmonic distortion due to capacitances

For second harmonic distortion analysis equation (3.17) for i_{de} can be truncated after $n = 2$:

$$\begin{aligned} i_{de} &\approx \tau_f g_{m1} \frac{du_{be}}{dt} + 2\tau_f g_{m2} u_{be} \frac{du_{be}}{dt} \\ &\approx j\omega\tau_f g_{m1} u_{be} + j\omega 2\tau_f g_{m2} {u_{be}}^2 \\ &\sim \omega C_{de1} \hat{u}_{be} \cos\omega t + 2\omega C_{de2} \frac{\hat{u}_{be}^2}{2} \sin 2\omega t \end{aligned} \tag{3.20}$$

The second and third lines of Equation (3.20) are only valid in case that u_{be} is a sinusoid.

In a circuit representation, the changes in diffusion current can best be modelled by a capacitance of value $C_{de1} = \tau_f g_{m1}$ shunted by a voltage-controlled current source of value $\tau_f g_{m2} {u_{be}}^2$. For convenience, $\tau_f g_{m2}$ can be called C_{de2}.

As could be expected, there is a current at frequency ω proportional to the admittance ωC_{de1}. Also, there is a second harmonic component at 2ω that is proportional to $2\omega C_{de2}$. Note that in contrast with the second-order nonlinearity of g_m, there is no response at DC. In some cases the second harmonic content in diffusion current i_{de} cannot be neglected with respect to the second harmonic distortion generated by $g_{\pi 2}$ and g_{m2} (see Section 3.1.3).

The total base-emitter capacitance, C_π, is usually approximated by the sum of $g_{m1}\tau_f$ and C_{je}. It is assumed in this work that BJTs are biased in the mid-current region (see Subsection 3.1.2). The diffusion capacitance is much larger than the junction capacitance in this region, therefore $C_\pi \approx C_{de}$.

For evaluating the number of higher order terms of the diffusion capacitance that has to be taken into account for evaluating the second harmonic distortion, the truncation error has to be evaluated. The truncation error of C_{de} can be calculated using (3.4) since it depends on I_c in a comparable way as the transconductance. If, for instance, we aim at $\mathcal{E} < 1$ %, C_π equals $g_{m1}\tau_f$ for $\hat{u}_{be}$ up to 4mV. For larger voltages up to $\hat{u}_{be} = 10$mV, the voltage-controlled current source C_{de2} has to be incorporated in the model. It may be incorporated in voltage-controlled current source i_{b2}, since it is depends on $\hat{u}_{be}^2$ also.

The values of the junction capacitances (C_{jc}, C_{bx}, and C_{js}) depend on the collector to base or collector to substrate voltage. The biasing voltages U_{bcQ},

C_{bxcQ}, and U_{csQ} are negative in value. C_{jc}, C_{bx}, and C_{js} will therefore have values smaller than their zero bias value. Since the equations for the junction capacitances are similar (see (3.19)), their nonlinear behavior will be similar also. Therefore, only the nonlinear behavior of C_{jc} will be evaluated.

A Taylor expansion of the junction capacitance C_{jc} results in:

$$C_{jcn} = C_{jcQ} - \sum_{n=1}^{\infty} C_{jc(n-1)} \frac{1}{n} \frac{(m_C + n - 1)}{(U_{bcQ} - \Phi_C)} \hat{u}_{bc} \tag{3.21}$$

Truncation after $n = 2$ gives:

$$\begin{aligned} C_{jc} &\approx C_{jcQ} + C_{jc1} + C_{jc2} \\ C_{jc1} &= -C_{jcQ} \frac{m_C}{U_{bcQ} - \Phi_C} \hat{u}_{bc} \\ C_{jc2} &= -C_{jc1} \frac{1}{2} \frac{m_C + 1}{U_{bcQ} - \Phi_C} \hat{u}_{bc} \end{aligned} \tag{3.22}$$

Evaluating the truncation error when $n = 0$ and $n = 1$, results in:

$$\mathcal{E}_0 = -\frac{m_C}{U_{bcQ} - \Phi_C} \hat{u}_{bc} \tag{3.23}$$

respectively

$$\mathcal{E}_1 = \frac{m_C (m_C + 1)}{(U_{bcQ} - \Phi_C)^2} \frac{\hat{u}_{bc}^2}{2}. \tag{3.24}$$

The errors introduced by truncating after $n = 0$ or $n = 1$ for a given collector signal voltage can be calculated using (3.23) or (3.24), respectively. However, because $\hat{u}_{bc}$ and $\hat{u}_{cs}$ of a single BJT depend on the characteristics of the negative-feedback amplifier (loop-gain), it may be convenient to calculate the maximum signal amplitude for which the junction capacitances may be regarded as a constant.

The maximal signal amplitude for a certain truncation error, $\mathcal{E}_0$, is found by rewriting Equation (3.23):

$$\hat{u}_{bc} \leq -\mathcal{E}_0 \frac{U_{bcQ} - \Phi_C}{m_C}. \tag{3.25}$$

A large value of U_{bcQ} is beneficial. Voltage $\hat{u}_{bc}$ may have larger values before the junction potential cannot be regarded constant anymore. For instance, when $\mathcal{E}_0$ should remain smaller than 1 %, an $\hat{u}_{bc}$ of only about 20 mV is found when U_{bcQ} = -1V, while $\hat{u}_{bc}$ may rise to 50 mV when U_{bcQ} = -5V. Equation (3.25) also holds for C_{bx} and C_{js} when the right parameters are used.

The negative-feedback amplifier can be designed in such a way that the signal levels do not exceed the maximal amplitude, for instance by cascoding. This strategy may give good results for every amplifying stage, except perhaps for the output stage since higher output voltage levels are not uncommon. Assuming C_{jc}, C_{bx} (and C_{js}) to be constant may not be realistic in that case. For second

harmonic distortion analysis the junction capacitances of the output stage may therefore be evaluated upto C_{jx1} or even C_{jx2}. The junction capacitances of the other amplifying stages may usually be regarded as being constant.

For lateral transistors, C_{js} is connected between the intrinsic base and the substrate. If the intrinsic emitter resistance r_E of the lateral transistor is small, which it usually is, C_{js} can be regarded as being in parallel with C_π and its effects can be seen as being part of the junction capacitance C_{je}.

D. Envelope detection properties due to capacitances

The envelope detection properties are investigated for an AM signal in a similar manner as was done in Chapter 1. In case the base-emitter voltage is amplitude modulated, the current i_{de} can be determined from

$$i_{de} = \frac{d}{dt}\left(\tau_f \sum_{n=1}^{\infty} g_{mn}(\hat{u}_{be}(1 + m\cos\omega_l t)\cos\omega_c t)^n\right), \tag{3.26}$$

where ω_c is the (high-frequency) carrier frequency, ω_l is the low-frequency modulating signal, and m is the modulation depth.

Truncation after $n = 2$ results in:

$$\begin{aligned} i_{de} = &- m\omega_l C_{de1}\hat{u}_{be}\sin\omega_l t\cos\omega_c t - \omega_c C_{de1}\hat{u}_{be}(1 + m\cos\omega_l t)\sin\omega_c t + \\ &C_{de2}2\hat{u}_{be}(1 + m\cos\omega_l t)\cos\omega_c t\times \\ &(-m\omega_l\hat{u}_{be}\sin\omega_l t\cos\omega_c t - \omega_c\hat{u}_{be}(1 + m\cos\omega_l t)\sin\omega_c t)\,. \end{aligned} \tag{3.27}$$

After trigonometric manipulation and omittance of the ω_c, $2\omega_c$, $(\omega_c \pm \omega_l)$, and $(2\omega_c \pm \omega_l)$ responses, the demodulated signals can be found at ω_l and $2\omega_l$:

$$i_{de2} = \omega_l C_{de2}\left(m\hat{u}_{be}^2\sin\omega_l t + m^2\hat{u}_{be}^2\sin 2\omega_l t\right). \tag{3.28}$$

Frequency ω_l is usually several krad/s (for example the frequency of the detected envelope variations of AM, GSM, etc.) and C_{de2} is a factor $\left(\frac{q}{2n_f kT}\right)$ times higher than C_{de1}. The amplitude of the demodulated signals in current i_{de} can therefore be expected to be negligibly small compared to the demodulated signals due to $g_{\pi 2}$ and g_{m2}, since both $\hat{u}_{be}^2\sin\omega_l t$ and $\hat{u}_{be}^2\sin 2\omega_l t$ are multiplied by $\omega_l C_{de2}$. It therefore seems to be reasonable to neglect the second order nonlinear behavior of the diffusion capacitance in case of EMI.

Consider for example a BJT biased at a collector current of 1 mA with $g_{\pi 2}$= 3.7 mA/V^2, g_{m2}= 0.747 A/V^2, $C_\pi = C_{de1}$ = 36 pF, and C_{de2}= 696 pF/V. An u_{be} of 10 mV with a modulation depth of 1 and ω_l= $6.28{\cdot}10^3$ rad/s results in the following disturbing currents: $i_{C_{de2}}$= 437 pA, $i_{g_{\pi 2}}$= 374 nA, and $i_{g_{m2}}$= 74.7 μA. Clearly, $i_{C_{de2}}$ can be neglected.

For the junction capacitances a similar discussion holds. The responses at ω_l and $2\omega_l$ can expected to be even smaller since the junctions are reverse biased. Considering EMI only, the junction capacitances may be approximated by their linear values without making an unacceptable error.

E. Medium signal hybrid-π model

The resulting hybrid-π model is shown in Figure 3.2. Because it is valid for larger signals than the conventional hybrid-π model, it might be called 'the medium signal hybrid-π model'. It contains three nonlinear components. The

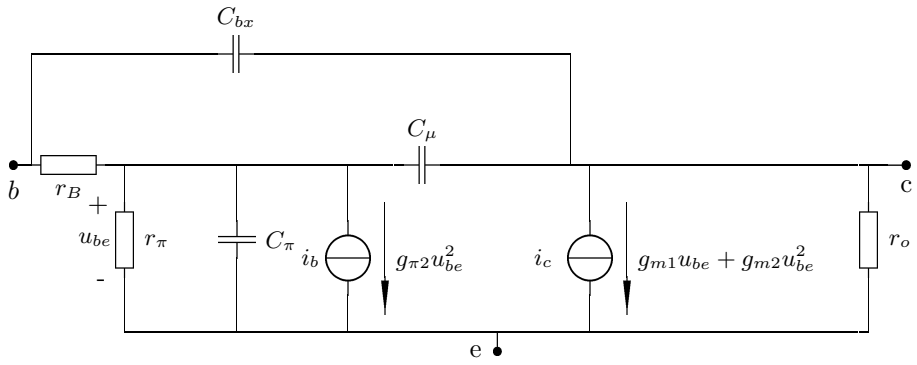


Figure 3.2: Medium signal hybrid-π model for calculating the linear and quadratic transfers of the BJT. The transconductance is modelled by a voltage-controlled current source i_c having both a linear and a quadratic transfer. Second-order nonlinearity of r_π is modelled by a voltage-controlled current source i_b and second-order nonlinearity of C_π may also be incorporated in it. The latter may be omitted in case of EMI and in some other cases (see main text). Note that C_{js} and parasitic capacitances and/or inductances from interconnects on the die have been omitted for simplicity. When desired, they can easily be added at the appropriate places.

first important nonlinear component is i_c, the nonlinear voltage-controlled current source that represents the nonlinear voltage to current transfer of the BJT. The second voltage-controlled current source, i_b, represents nonlinear behavior of the input resistance and, if desired[3], the diffusion capacitance part of C_π. Note that capacitance C_{jc} is called C_μ in this model.

With this 'medium signal hybrid-π model' both the linear and second-order transfer can be calculated, i.e., second harmonic distortion (for signals in the pass band of the amplifier) and envelope detection.

The direct current amplification factor is an important quantity that does not directly appear in the hybrid-π model. It is defined as the ratio of the collector current and the base current. Using Equations (3.1) and (3.2), the *dc* current amplification factor is easily derived to be:

$$\beta_{dc} = \frac{I_{cQ}}{I_{bQ}} = \beta_f \left(1 - \frac{U_{bcQ}}{U_{AF}}\right). \tag{3.29}$$

[3]For increased accuracy in second-harmonic distortion analysis.

F. Driving the BJT with medium amplitude signals

In this subsection the linear and quadratic behavior of the hybrid-π circuit when driven with an input signal is described. Both current and voltage drive are considered. For convenience, it is assumed that C_π determines the high frequency behavior. Therefore, C_μ and C_{bx} are omitted from the analysis. The collector current i_c is considered as the output signal, while small-signal quantity u_{ce} is assumed zero. Figure 3.3 presents the circuit diagram.

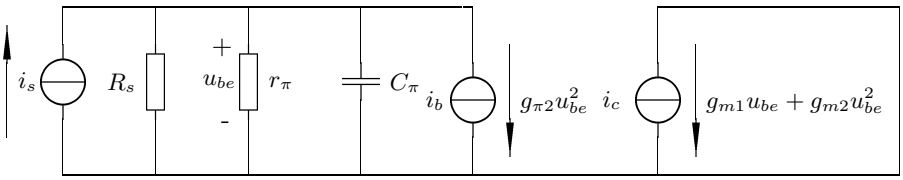


Figure 3.3: Medium signal hybrid π model used to calculate the linear and quadratic transfers from i_s to $i_c = g_{m1}u_{be} + g_{m2}u_{be}^2$.

Initially, resistor R_s will be assumed to be infinite and the frequency is assumed to be so low that C_π may be disregarded. The resistance r_B can be neglected because it is in series with an ideal current source for $R_s \to \infty$. The base-emitter voltage u_{be} is now given by:

$$u_{be} = i_s r_\pi - (i_s r_\pi)^2 g_{\pi 2} r_\pi. \tag{3.30}$$

The *ac* collector current ($i_c = g_{m1}u_{be} + g_{m2}u_{be}^2$) is

$$i_c = i_s g_{m1} r_\pi + i_s^2 r_\pi^2 \left(g_{m2} - g_{m1} r_\pi g_{\pi 2}\right) - 2 i_s^3 r_\pi^4 g_{\pi 2} g_{m2} + i_s^4 r_\pi^6 g_{\pi 2}^2 g_{m2}. \tag{3.31}$$

A collector current with a linear, a quadratic, a cubic, and a fourth-order term results. The ratio of the linear terms in the collector current and the signal current gives the small-signal current gain factor β_{ac} [57],

$$\beta_{ac} = g_{m1} r_\pi = \beta_f \left(1 - \frac{U_{bcQ}}{U_{AF}}\right). \tag{3.32}$$

Note that $\beta_{dc} = \beta_{ac}$, see (3.29).

The second-order term can be written as:

$$i_{c2} = i_s^2 r_\pi^2 \left(g_{m2} - g_{m1} r_\pi g_{\pi 2}\right) = i_s^2 r_\pi^2 \left(g_{m2} - \beta_{ac} g_{\pi 2}\right) = i_s^2 \beta_{ac2} = 0 \tag{3.33}$$

When Equations (3.6), (3.7), (3.11), and (3.9) are used to evaluate β_{ac2}, it is found to equal zero. Note that now the expression for β_{ac} is known, it follows $g_{\pi 2} = g_{m2}/\beta_{ac} (r_\pi = 0, g_{\pi 2} \to \infty$, for β_{ac}=0).

Third- and fourth order current amplification factors also appear. Theoretically, the $(i_s r_\pi)^4$ term will give rise to some envelope detection. Its effect, however, can only be evaluated when all distortion terms up to the fourth are

taken into account. When all terms of i_c up to the fourth-order are evaluated (using inverse functions [44]), β_{ac3} and β_{ac4} are found:

$$\beta_{ac3} = 0 \tag{3.34}$$

$$\beta_{ac4} = 0. \tag{3.35}$$

In fact, all higher order β_{ac} terms are zero. From this evaluation can be concluded that *in case of current driving the* BJT*, no envelope detection nor second-order distortion will occur.* The latter corresponds to the findings of other authors [60][96].

Next, the effects of a finite value of R_s are considered. For the linear and quadratic term in i_c can the following expressions be derived:

$$\begin{aligned} i_{c1} = &\quad i_s \beta_{ac} \frac{R_s}{R_s + r_{\pi 1}} \quad \text{Current driving} \\ \text{and} \quad i_{c1} = &\quad u_s g_{m1} \frac{r_{\pi 1}}{R_s + r_{\pi 1}} \quad \text{Voltage driving,} \end{aligned} \tag{3.36}$$

with u_s being the signal voltage when voltage drive is considered (i.e., i_s, R_s converted to u_s, R_s via Thévenin's theorem).

The second-order term in i_c is given by

$$\begin{aligned} i_{c2} = &\quad i_s^2 \left(\frac{R_s r_\pi}{R_s + r_\pi} \right)^2 \left\{ g_{m2} - g_{m1} g_{\pi 2} \frac{r_\pi R_s}{r_\pi + R_s} \right\} \\ = &\quad i_s^2 \left(\frac{r_\pi R_s}{R_s + r_\pi} \right)^2 \left\{ g_{m2} \frac{r_\pi}{R_s + r_\pi} \right\} \quad \text{Current driving} \\ \text{and} \quad i_{c2} = &\quad u_s^2 \left(\frac{r_\pi}{R_s + r_\pi} \right)^2 \left\{ g_{m2} \frac{r_\pi}{R_s + r_\pi} \right\} \quad \text{Voltage driving.} \end{aligned} \tag{3.37}$$

A finite value of R_s seems to have a detrimental effect on i_{c2}. The lower the value of R_s, the larger i_{c2} becomes. That is in accordance with what is found when the voltage driven situation is considered. The base-resistance r_B is considered to be a part of R_s.

Comparing current and voltage drive, it can be seen that the quadratic term (the g_{m2} term between the brackets in Equation (3.37)) is the same in both situations. The main difference is the magnitude of R_s. In case of current drive its value is much larger than the value of r_π, resulting in a small quadratic term, approaching zero. Voltage drive occurs in those situations that R_s has a value comparable to or smaller than r_π. The quadratic term is relatively large in that case, with a maximum of $u_s^2 g_{m2}$ when R_s approaches zero. For values of R_s between the two extremes, the second-order is also somewhere between the extremes. This is consistent with [96][60]. So, the extreme values of R_s determine whether the BJT behaves as a linear, current-controlled current source or as a nonlinear voltage-controlled current source.

The difference between current and voltage driving can be explained by considering that current-driving a BJT causes a nonlinear u_{be} to occur which is a

natural logarithm function of the signal current, that in turn generates an i_c that is a natural exponential function of u_{be}. Since both functions are complementary, a linear transfer from signal current to i_c occurs. A finite value of R_s hampers the 'quality' of the transfer of i_s to the nonlinear u_{be} required for a linear i_s-i_c transfer. When driving the BJT with an ideal voltage source, the linear signal voltage causes u_{be} to be linear also. This voltage generates a nonlinear i_c. No linearizing action whatsoever occurs in case of ideal voltage driving the BJT.

G. Cross-product distortion

The cross product current i_{cross} has been disregarded up to now, however, it does affect the current due the second-order nonlinearity. It is taken into account with

$$i_{c2} = u_s^2 \left(\frac{r_{\pi 1}}{R_s + r_{\pi 1}}\right)^2 \left(g_{m2}\frac{r_{\pi 1}}{R_s + r_{\pi 1}} - g_{m1}g_x\frac{r_o Z_l}{r_o + Z_l}\right), \qquad (3.38)$$

where Z_l is the load impedance. It can be seen that i_{c2} is now dependant on the load, and hence u_{ce}. Assuming that the effect due to g_x is considered negligible when its value is equal or smaller than y times the value of the g_{m2} term, it is found that Z_l has to satisfy the following relation

$$Z_l \leq y\frac{r_{\pi 1} r_o}{2R_s + r_{\pi 1}} = y r_o \frac{1}{2\frac{R_s}{r_\pi} + 1} = y\frac{U_{AF}}{I_{cQ}}\frac{1}{\left(2R_s\frac{q}{n_f kT\beta_{ac}}I_{cQ} + 1\right)}. \qquad (3.39)$$

The value of coefficient y is chosen by the designer. It may, e.g., have a value of 0.1 or even lower. A high value of the Early voltage, and thus r_o, is beneficial since it allows Z_l to increase. Since r_o is inversely proportional to I_{cQ}, it is clear that lower values of Z_l follow for higher bias currents.

Equation (3.39) also shows that the maximum value of Z_l depends on the driving resistance, R_s. In case of ideal voltage driving, it follows that Z_l should have a value lower than yr_o. Increasing values of R_s result in lower allowable values of Z_l. In fact, in case of ideal current driving, ideal current loading, i.e., $Z_l = 0$, is required. For a reasonably high driving resistance, e.g., $R_s \approx 10r_\pi \cdots 100r_\pi$, the Z_l requirement can usually be met by cascoding the BJT.

When the BJT is applied in a negative-feedback amplifier, a negligible contribution from g_x to the second order nonlinearity can in general be accomplished by cascoding the BJT (low Z_l) and/or by ensuring enough loop gain. Collector-emitter voltage u_{ce} can be kept low in that way. Moreover, both driving impedance and load impedance generally decrease with increasing frequency, thus easing the design of a negative-feedback amplifier with negligible contribution from g_x to the second harmonic distortion.

Under the assumption that ω_c is much larger than the amplifier bandwidth, a negligible contribution to the EMI behavior of the negative-feedback amplifier can often be expected from g_x because the product $u_{be}(\omega_c)u_{ce}(\omega_c)$ is often negligibly low.

In the remainder of this chapter it is assumed that the effect of g_x is negligible.

3.1.2 Secondary effects affecting BJT nonlinearity

Besides the primary functionality of the BJT discussed up to now, some secondary effects may occur. Both at low and high currents these secondary effects occur. Figure 3.4 shows the base and collector currents as function of the base-emitter voltage.

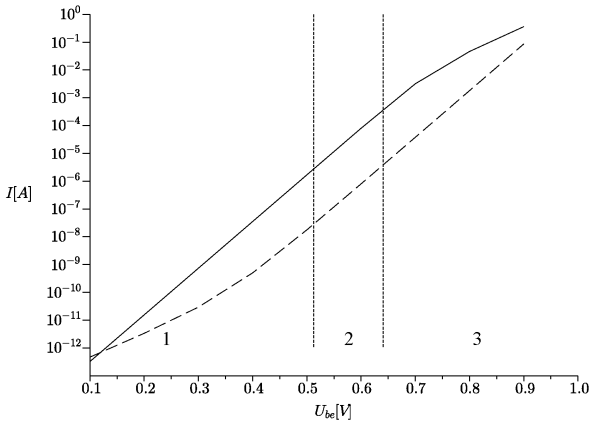


Figure 3.4: Gummel plot of a BJT. The solid line is I_c, the dotted line is I_b. Area 1 is the low-current region, area 2 the mid-current region, and area 3 the high-current region.

At low values of the collector current (i.e., the low-current region indicated by area 1), the current due to recombination in the base-emitter depletion layer and at its surface becomes of the same order of magnitude as the base-emitter current that controls the collector current [97] and cannot be neglected. The current due to recombination is depicted by current I_{b2} in Fig. 3.1 and adds to the base current:

$$I_{bQ} = I_{b1} + I_{b2} = \frac{I_s}{\beta_f} e^{\left(\frac{qU_{beQ}}{n_f kT}\right)} + I_{se} e^{\left(\frac{qU_{beQ}}{n_e kT}\right)}. \tag{3.40}$$

I_{se} is the base-emitter leakage saturation current. The coefficient n_e is the low-current, forward region emission coefficient. Coefficient n_e= 2 when recombination in the base-emitter layer is the main contributor [87].

For increasing bias levels, i.e., increasing U_{be}, current I_{b1} increases more than current I_{b2} [57][88]. At the boundary of the low-current and mid-current regions, I_{b2} can be neglected since I_{b1} has become much larger. The current gain β_{ac} therefore increases with increasing collector current in the low-current region, see Fig.3.5(a).

High and low-current effects are negligibly small in the mid-current region. The mid-current region is region 2 in Figure 3.4. The transistor behaves as

discussed in Subsection 3.1.1. Current gain β_{ac} is (virtually) constant in this region, as can be seen in Fig.3.5(a).

At high current levels the injection of minority carriers into the base region is significant with respect to the majority carrier concentration [88]. This results in a longitudinal electric field in the base-region that hampers the diffusion of majority carriers and supports the diffusion of minority carriers. At the same time the injection of majority carriers into the emitter region increases [88].

High current level effects are incorporated in the expressions for the collector current [88][60]

$$I_{cQ} = 2\frac{\left(1 - \frac{U_{bcQ}}{U_{AF}}\right)}{(1 + X_Q)} I_s e^{\left(\frac{qU_{beQ}}{n_f kT}\right)} = \frac{2}{(1 + X_Q)} I_{cQ,\text{prim.}} \tag{3.41}$$

with

$$X_Q = \sqrt{1 + 4\frac{I_S}{I_{KF}} e^{\left(\frac{qU_{beQ}}{n_f kT}\right)}}. \tag{3.42}$$

$I_{cQ,\text{prim.}}$ is the collector current when only primary effects are taken into account, see Equation (3.1). High level injection effects are represented by the knee current[4], I_{KF}.

Equation (3.41) shows that I_c will increase less with increasing U_{be} than in the mid-current region. This is depicted by region 3 in Fig. 3.4. Current gain β_{ac} therefore decreases with increasing collector current, see Fig.3.5(a).

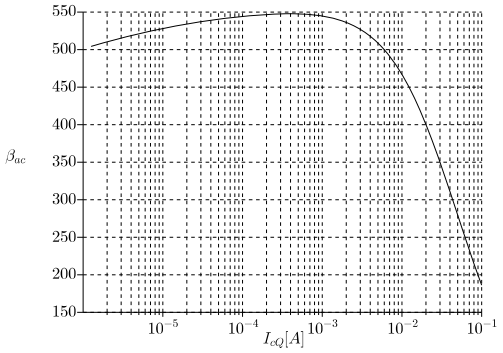
The linear and second-order nonlinear parameters can be determined again by calculating $g_{m1} = dI_c/dU_{be}$, $g_{m2} = 0.5d^2I_c/dU_{be}^2$, $g_{\pi 1} = dI_b/dU_{be}$, and $g_{\pi 2} = 0.5d^2I_b/dU_{be}^2$, using (3.41) and (3.40) for I_c and I_b, respectively. Especially in the low and high-current region, all four parameters differ from the value that is found when using the equations in Subsection 3.1.1.

Current gains β_{ac} and β_{ac2} can be determined using the circuit shown in Figure 3.3. The resulting current gain $\beta_{ac} = r_\pi g_{m1}$ is depicted in Fig.3.5(a). Figure 3.5(b) shows $\beta_{ac2} = r_\pi^2(g_{m2} - \beta_{ac}g_{\pi 2})$. Terms g_{m2} and $\beta_{ac}g_{\pi 2}$ will vary with I_{cQ}. When both terms are equal, β_{ac2} will be zero. This occurs at one specific value of I_{cQ} in the mid-current region. Current gain β_{ac} is constant at this current.

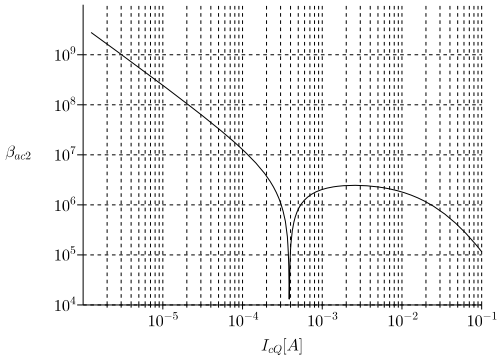
Figures 3.6(a) and 3.6(b) show the second harmonic of the collector current, i_{c2}, and the second-order harmonic distortion $HD_2 = i_{c2}/i_{c1}$ as function of the signal source resistance R_s. Both decrease for higher R_s values and then stabilize at a more or less constant value ($HD_2 \approx 0.1$ %) for resistances larger than the optimal value of R_s. In this case the optimal value is $R_s = 1$ MΩ.

From Figure 3.6 can be concluded that i_{c2} can be minimized for a given R_s, by biasing it at the correct value of I_{cQ}. Unfortunately, it does not seem to be possible to derive a closed form analytical solution for determining the optimal I_{cQ} from the presented equations. Again, the cancellation of second

[4]It is represented by I_K in the MEXTRAM model [87]. It should be noted that high current effects are modelled more accurately in this model.



(a) Linear term of β_{ac} as function of I_{cQ}.



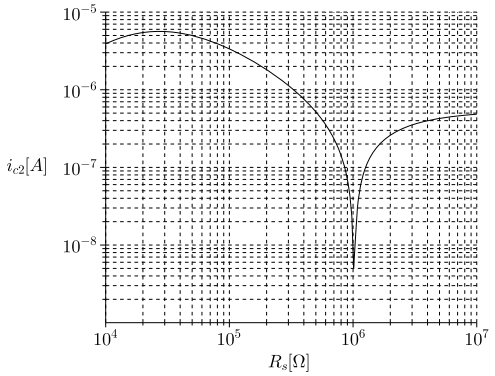
(b) Absolute value of the quadratic term of β_{ac2} as function of I_{cQ}.

Figure 3.5: Alternating current amplification factors as function of I_{cQ}. Figure 3.5(a): $\beta_{ac}(I_{cQ})$ and 3.5(b): $\beta_{ac2}(I_{cQ})$

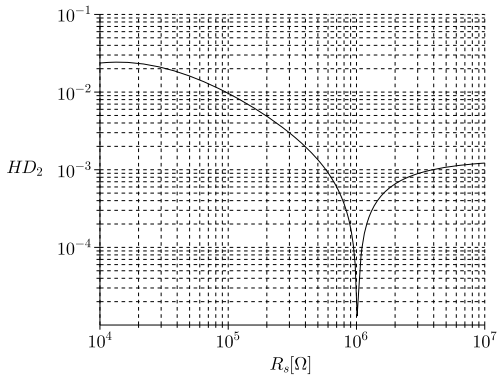
order distortion is perfect at one (bias) point only. This is in agreement with the finding of other authors [98].

The optimum value of I_{cQ} for a zero β_{ac2} (and zero HD_2) is subjected to spread in the values of β_f, I_s, I_{se}, and I_{KF} between various devices of the same transistor type. It is therefore more sensible to specify a range for which β_{ac2} is reasonably low for low distortion design: the usable mid-current region.

The lower limit of the usable mid-current region is given by the value of U_{beQmin} at which I_{b1} is a factor b larger than I_{b2}. The detrimental effect of I_{b2} may be neglected for values of U_{beQ} larger than U_{beQmin}. A factor $b = 20$ seems to be a reasonable value. From Equation (3.40) it follows that U_{beQmin} is given



(a) Quadratic component i_{c2} as function of R_s.



(b) Second-order distortion HD_2 as function of R_s.

Figure 3.6: Second order nonlinear current i_{c2} and second-order distortion HD_2 of a $BC847C$ BJT biased at $I_{cQ} = 1\text{mA}$ and $U_{ceQ} = 5\text{V}$ as a function of R_s. Signal current i_s is $0.73\mu\text{A}$.

by:

$$U_{beQmin} = \frac{kT}{q}\frac{n_f n_e}{n_f - n_e}\ln\left(\frac{1}{b\beta_f}\frac{I_s}{I_{se}}\right). \tag{3.43}$$

If the decrease in I_{cQ} due to high-current effects is limited to a maximum of c (e.g., $c = 0.1$ is reasonable), it follows from Equation (3.41) that the maximal value of U_{beQ} is:

$$U_{beQmax} = \frac{n_f kT}{q}\ln\left(\frac{cI_{KF}}{4I_s}\right). \tag{3.44}$$

Second-order conductance $g_{\pi 2}$ will be exactly equal to g_{m2}/β_{ac} for one bias current only. For other current values there will be a deviation between the

actual value of $g_{\pi 2}$ and g_{m2}/β_{ac}, causing $\beta_{ac2} = r_\pi^2(g_{m2} - \beta_{ac}g_{\pi 2})$ to be small in the mid-current region, but not zero anymore.

Apart from the ideal bias point where the deviation between $g_{\pi 2}$ and g_{m2}/β_{ac} will be larger, this deviation is expected to be largest at the edges of the mid-current region (see Fig. 3.5(b)). Coefficients b and c in Equations (3.43) and (3.44) have been given such values that the deviation is maximally $3\% \cdots 4\%$ for most BJTs[5]. As a result of the deviation there will be an uncertainty in the actual value of the second-order nonlinearity. It may be larger or smaller than expected. The latter is just convenient, the first may be harmful.

When x is denoted as the ratio of[6] $g_{\pi 2}$ and g_{m2}/β_{ac}, the second-order nonlinearity given by Equation (3.37) can be rewritten as

$$g'_{m2} = g_{m2} - g_{m1}g_{\pi 2}\frac{R_s r_\pi}{R_s + R_\pi} = g_{m2}\left(\frac{r_\pi + R_s(1-x)}{R_s + r_\pi}\right). \tag{3.45}$$

In case $x = 1$ we have the ideal condition $g_{\pi 2} = g_{m2}/\beta_{ac}$; in this work $0.97 \leq x \leq 1.03$ is used. Low values of R_s do not introduce large deviations compared to (3.37). Current drive, i.e., high values of R_s, decreases g'_{m2} but increases the uncertainty in its actual value.

For design purposes, at least as first-order design, the equations in the previous section may be used when the BJT is biased in the mid-current region. Some accuracy is exchanged for simplicity. Throughout the remainder of this work it is assumed that the BJTs are biased in the mid-current region and the (approximate) Equations (3.6)−(3.9) and (3.45) are used.

Finally, current crowding occurs at high current levels where the base current produces a voltage drop in the base that tends to forward bias the base-emitter junction preferably around the edges of the emitter. Thus the transistor action tends to occur along the emitter periphery rather than under the emitter itself and the distance from the base contact to the active base region is reduced [57]. Consequently, the value of r_B is reduced.

In low-noise and/or high frequency amplifiers where a low r_B is important, an effort is made to maximize the periphery of the emitter that is adjacent to the base contact [57], by e.g., applying multiple base and emitter stripes, thus decreasing the value of r_B. On top of that, in a well designed negative-feedback amplifier, effort has been made to minimize the adverse effects of r_B. Changes in its value will thus have negligible effects. Therefore, r_B is considered to be a constant in this work.

3.1.3 BJT second-order nonlinear behavior as function of frequency

Next, the frequency dependency of the transfers have to be determined. The nonlinear parameters are determined from the equations given in Subsection

[5] In case of some older BJTs b and c should be adjusted for a deviation of $3\% \cdots 4\%$.
[6] Note that β_{ac} may easily be determined by simulation.

3.1.2. For now, the nonlinear effects of C_π and C_μ are disregarded. By inspection of Figure 3.3, the linear and quadratic transfers are given by:

$$i_{c1} = i_s g_{m1} r_{\pi 1} \frac{R_s}{R_s + r_\pi + s R_s r_{\pi 1} C_{\pi 1}} \tag{3.46}$$

and

$$i_{c2} = \quad i_s^2 m \left(\frac{R_s}{R_s + r_{\pi_1} + s R_s r_{\pi 1} C_{\pi_1}} \right)^2 \left(g_{m2} - g_{m1} g_{\pi 2} \frac{R_s r_\pi}{R_s + r_\pi + 2 s R_s r_\pi C_\pi} \right), \tag{3.47}$$

$$i_{c2} = \quad i_s^2 m \left(\frac{R_s}{R_s + r_{\pi_1} + s R_s r_{\pi 1} C_{\pi_1}} \right)^2 \times \tag{3.48}$$

$$\left(g_{m2} - g_{m1} (g_{\pi 2} + 2 s C_{\pi 2}) \frac{R_s r_\pi}{R_s + r_\pi + 2 s R_s r_\pi C_\pi} \right).$$

In these equations, s is the Laplace operator and the coefficient m equals 0.5 in case of second harmonic distortion and the modulation depth in case of EMI. Equation (3.47) does not take the nonlinear effect of C_π into account, while Equation (3.48) does, with $C_{\pi 2} = \tau_f g_{m2}$.

Both linear and quadratic transfers are depicted in Figure 3.7(a) and Figure 3.7(b). The transfer is depicted by the solid line in Figure 3.7(b). The crosses in Figure 3.7(b) are SPICE simulation results. Both calculations and simulations are in good agreement.

The effect of the nonlinear C_π can be modelled by incorporating its effect in voltage-controlled current source i_b, as is shown in Figure 3.8 and (3.48).

Comparing Figs. 3.7(b) with the SPICE simulations, it may be concluded that both Equation (3.47) and (3.48) give satisfactory results. Equation (3.48) is more accurate; $C_{\pi 2}$ tends to linearize the transfer a bit in this case. Equation (3.47) is, however, for design purposes accurate enough. The transfer given by (3.47) and depicted by the dashed line in Figure 3.7(b) are comparable to the results given in [96]. In that paper, however, the current gain is assumed to be constant. In this example the nonlinear behavior of the current gain was also taken into account.

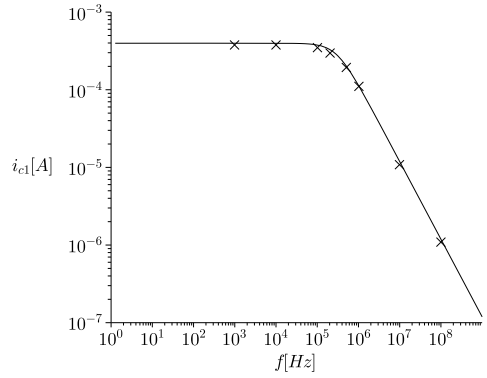
Note that in case of EMI that $C_{\pi 2}$ can be disregarded, and Equation (3.47) should be used.

3.1.4 Model limitation

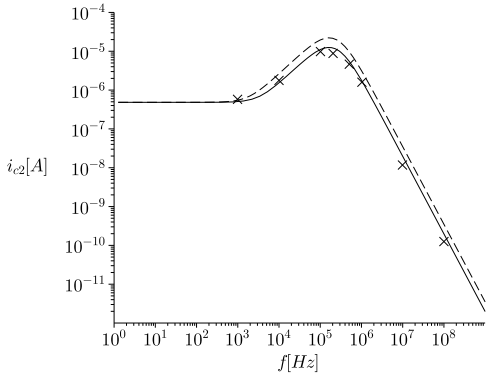
This work uses the well known Gummel-Poon model to extract a hybrid-π model that can be used to analyze linear and second-order nonlinear responses. The validity of the Gummel-Poon model is, however, limited to approximately 10% of the transit frequency f_t [99][43]. For higher frequencies, a disagreement is observed between transfer measurements and circuit analysis[7].

For (nonlinear) analysis and design at frequencies above $0.1 f_t$ the nonlinear model presented in [43][44], the MEXTRAM, and HICUM models can be used. Second harmonic analysis at these frequencies will otherwise show discrepancies due to inaccurate modelling of the linear and nonlinear capacitance C_π.

[7] The disagreement is not observed in FET hybrid-π models [99].



(a) Linear component of i_c as function of frequency.



(b) Second harmonic of i_c as function of frequency. Dashed line is without effect of $C_{\pi 2}$, solid line is with effect of $C_{\pi 2}$.

Figure 3.7: Linear and second harmonic components in i_c as function of frequency, with signal current $i_s = 0.73\mu A$ and $R_s = 10$ MΩ. The crosses are SPICE simulation results, the lines are calculated.

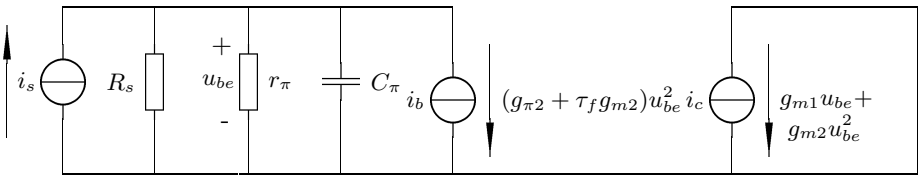


Figure 3.8: Hybrid-π model with second-order nonlinearity of C_π incorporated in current source i_b.

In analysis and design of EMI (envelope detection) of negative-feedback amplifiers, usually with a bandwidth smaller than $0.1f_t$, an inaccuracy in the (linear) frequency transfer could be observed for frequencies higher than $0.1f_t$. Detection is, however, a low frequency effect that hardly depends on the nonlinear capacitance. It is expected that the error made in this case is small enough to allow use of the hybrid-π model presented in this work, at least in the early design steps.

The hybrid-π model is expected to give accurate results for $\hat{u}_{be}$ up to 10mV under the condition of current loading. If the latter is not the case, cross term transconductance g_x may cause inaccuracies.

3.2 Field-effect transistors

The type of transistor to be discussed here consists of two heavily doped regions called source and drain in the bulk, and an isolated region called gate. The electric fields between gate-source/bulk and drain-source create a channel of charge carriers between source and drain and therefore the current flowing from source to drain. Hence the name field-effect transistor (FET).

Two types of field effect transistors will be discussed: the metal-oxide-semiconductor field-effect transistor (MOSFET) and the junction field-effect transistor. For the latter type, both the junction field-effect transistor (JFET) and the metal-semiconductor field-effect transistor (MESFET) will be discussed briefly.

JFETs are always depletion type transistors, MOSFETs may be either depletion or enhancement type [100]. Depletion type FETs have a conducting channel when no electric fields are applied. Applying an electric field between gate and source/bulk will cause a decrease in charge carriers in the channel and hence a decrease in current. In enhancement type FETs no conducting channel exists when no electric fields are present. Electric fields between gate-source/bulk and drain-source create a channel. An increase in the electric fields cause an increase in charge and hence in current in the channel.

3.3 The metal-oxide-semiconductor field-effect transistor

The following explanation of the MOSFET is based on a n-channel enhancement device, but with the appropriate change of signs for charge and potential it also holds for p-channel and depletion devices. Figure 3.9 shows the structure of a typical n-channel device.

A p-type doped area, called bulk or substrate, contains two heavily doped n-type regions called source and drain, respectively. On top of the bulk there is a thin layer of silicon dioxide[8] (or a 'high-k' dielectric in FETs $\leq$ 45 nm [102][103])

[8]Silicon dioxide is an insulator. The insulating layer separates the gate from the substrate. Therefore, these devices are also called insulated-gate FETs or IGFETs [101].

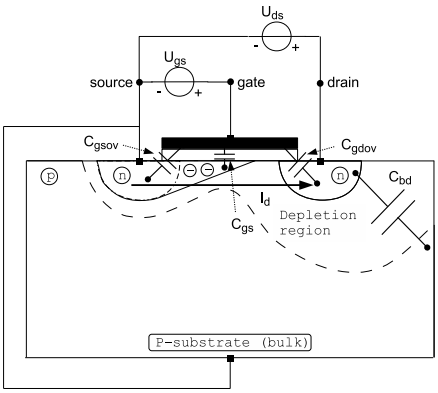


Figure 3.9: N-channel MOSFET with bias voltage sources. The MOSFET is depicted in the saturation region. The pinched channel is indicated by the minus signs. The parasitic capacitances are shown. Material resistances are omitted for clarity.

covered with the gate electrode (metal[9] or polycrystalline silicon), (black). Note that the gate overlaps the source and drain, creating overlap capacitances C_{gsov} and C_{gdov}. The depletion layer capacitance between the drain and the substrate is C_{bd}, while the charge in the channel creates a capacitance C_{gs}.

When a voltage U_{gs} is applied, the concentration of charge carriers below the gate area is altered. Three different operation conditions can be distinguished: accumulation, depletion and saturation.

The regions of operation are determined by the gate-source voltage U_{gs}, the drain-source voltage U_{ds} and the threshold voltage U_t. The first two voltages can be chosen by the designer; the latter is determined by the fabrication process and is given by [104]

$$U_t = U_{FB} + \Phi_B + \gamma\sqrt{\Phi_B}. \tag{3.49}$$

U_{FB} is the flat band voltage (-1.050 V for silicon/SiO_2), γ is the body effect coefficient, (typically 1/2 [$\sqrt{V}$] [57]), and Φ_B is the surface potential at the onset of strong inversion (0.95 V).

A non-zero source-bulk voltage, U_{sb}, can occur in analog integrated circuit design and may cause a change in the threshold voltage [57]. The new threshold voltage is given by $U_{tb} = U_t + \gamma(\sqrt{\Phi_B + U_{sb}} - \sqrt{\Phi_B})$ [104]. The effect of a non-zero U_{sb} on MOSFET behavior may be analyzed in a similar way ($U_{sb} = 0$ is analyzed in this work for simplicity).

For gate-source voltages (slightly) less than U_t and $U_{ds} > 0$, an accumulation layer of positive charge is formed between source and drain [91][105]. Drain current I_d is exponentially dependent on U_{gs} and much smaller than when $U_{gs} > U_t$. Nonlinear behavior of the MOSFET in accumulation can be expected

[9] hence the name MOSFET

to be comparable to the voltage driven BJT and therefore the same considerations hold. Furthermore, MOSFETs in accumulation are used mainly in very low power applications at relatively low signal frequencies [57]. Very low power negative-feedback amplifiers are beyond the scope of this work. Therefore, the accumulation region is not investigated further.

Depletion occurs when $U_{gs} > U_t$ and $U_{ds} \ll 2(U_{gs} - U_t)$ [57] and a thin layer of electrons is formed at the surface of the silicon directly under the oxide, see Figure 3.9. The free electrons act as a conducting channel between the source and drain regions. The voltage difference across the channel approximately equals U_{ds} [91] and current I_d will increase almost linearly with U_{ds}. Consequently, this operating region is often called *linear region*. Also, it may be called *Ohmic-* or *triode region* [57]. The triode region is not very useful for amplification purposes due to the resistor like behavior of the FET. It is therefore not investigated further in this work.

When $U_{gs} > U_t$ and U_{ds} is high (e.g., $> (U_{gs} - U_t)$), saturation occurs. The gate-drain voltage is now smaller than the threshold voltage. This means that the channel no longer exists at the drain, see Fig. 3.9. As a result, the average electric field in the source-drain channel does not depend on the drain-source voltage but instead on the voltage across the channel [57]. As a consequence, I_d becomes independent of U_{ds}. In other words, I_d saturates for U_{ds} above a certain saturation voltage $U_{dssat\infty}$, hence the name *saturation* for this bias region [91]. $U_{dssat\infty}$ is the saturation voltage of an ideal long channel MOSFET [104]. In literature, $U_{dssat\infty}$ may also be called *pinch-off voltage* (e.g., [57] [60]) hence also the name *pinch-off region* may be used. In the saturation region I_d will increase approximately quadratically with U_{gs}.

It may seem strange that in case of a depleted drain region that current can reach the drain contact. The voltage $U_{ds} - U_{dssat\infty}$ across the pinched-off region, however, creates a strong electric field which transports electrons from the strongly inverted region to the drain [103].

In case of a long-channel MOSFET[10] $U_{dssat} \approx U_{dssat\infty}$, with $U_{dssat\infty}$ being given by[11]

$$U_{dssat} \approx U_{dssat\infty} = U_{gs} - U_{FB} + \frac{\gamma^2}{2} - \gamma\sqrt{U_{gs} - U_{FB} + \frac{\gamma^2}{4}} - \Phi_B, \qquad (3.50)$$

while for a short-channel[12] MOSFET holds $U_{dssat} \approx U_{dssat\infty} \cdot (1 - F(L))$ [104]. The correction factor $F(L)$ decreases with increasing channel-length and it causes U_{dssat} to become lower than $U_{dssat\infty}$. Its formula is given in [104][91]. Factor $F(L)$ lowers the output resistance (see Eq. (3.64)) and it affects the output nonlinearity in a complex way. These detrimental effects are easily solved in the

[10] The error made in case of long-channel MOSFETs is less than 1 % [104]

[11] $U_{dssat} \approx U_{dssat\infty} = U_{gs} - U_{FB} + \frac{\gamma^2}{2} - \gamma\sqrt{U_{gs} + U_{sb} - U_{FB} + \frac{\gamma^2}{4}} - \Phi_B$ when source and bulk are not short circuited.

[12] The channel-length of short-channel MOSFETs is typically in the submicrometer range [103]. Section 3.4.2 presents an equation that can be used to determine whether a MOSFET has a long or short-channel.

design process by cascoding short-channel MOSFETs. Therefore, (3.50) is used in this work (Section 3.4.4).

Since $U_{FB} = U_t - \Phi_B - \gamma\sqrt{\Phi_B}$ holds, Equation (3.50) can be written in the form:

$$U_{dssat} \approx (U_{gs} - U_t) + \frac{\gamma^2}{2} - \gamma\left(\sqrt{(U_{gs} - U_t) + \Phi_B + \gamma\sqrt{\Phi_B} + \frac{\gamma^2}{4}} - \sqrt{\Phi_B}\right). \tag{3.51}$$

For calculating the drain current the following equation can be used [104]:

$$I_d = \mu C_{ox}\frac{W}{L}\left(U_{gs} - U_t - \frac{1}{2}U_{dssat} - \gamma\left(\sqrt{\frac{1}{2}U_{dssat} + \Phi_B} - \sqrt{\Phi_B}\right)\right)U_{dssat}. \tag{3.52}$$

Textbooks typically approximate U_{dssat} by $U_{dssat} = U_{gs} - U_t$ and the equation for the drain current is, as a result, reduced to $I_d = \beta(U_{gs} - U_t)^2$. However, a depletion layer exists between the physical pinch-off point in the channel at the drain and the drain itself [57]. The length of this depletion layer depends on the value of U_{ds}. Therefore, the length of the channel also depends on U_{ds}. Increasing values of U_{ds} result in an increased depletion layer and a smaller effective channel length L. I_d therefore tends to increase with increasing U_{ds}. This phenomenon is called channel length modulation (CLM).

As a first-order approximation, this effect is assumed to be linear. Taking CLM into account, the equation for the drain current becomes [105]

$$I_d = \beta_{\text{FET}}(U_{gs} - U_t)^2(1 + \lambda(U_{ds} - U_{dssat})). \tag{3.53}$$

λ is a parameter used for a first-order characterization of the channel length modulation.

The value of I_d depends on the size of the MOSFET, the gate oxide capacitance per unit area (C_{ox}) and the average electron mobility μ_0. This dependence is given by the transconductance parameter $\beta_{\text{FET}} = \mu_0 C_{ox}\frac{W}{L}$, [57][91]. I_d is proportional to β_{FET}. The value of β_{FET} may be maximized by choosing a large $\frac{W}{L}$ ratio and C_{ox}.

3.4 FET hybrid-π model

A hybrid-π model valid for both MOSFET and JFET will be presented in this section. Therefore, both linear small-signal and second-order nonlinear parameters will be derived in the next subsections. Firstly, the primary, or first-order, effects are modelled. The secondary effects affecting (non)linearity are then modelled.

3.4.1 First-order approximations

The easiest way to determine the FET response to a change in input or output voltage is by performing a Taylor series expansion of Equation (3.53). This

results in transconductance terms from u_{gs}, output conductance terms from u_{ds} and cross terms from $u_{gs}u_{ds}$.

The linear transconductance is given by

$$g_{m1} = 2\sqrt{\beta_{\text{FET}} I_{dQ}(1 + \lambda(U_{dsQ} - U_{dssat}))}. \tag{3.54}$$

The transconductance thus increases or decreases with the square root of bias current I_{dQ}.

The second-order nonlinear transconductance is given by

$$g_{m2} = \beta_{\text{FET}}(1 + \lambda(U_{dsQ} - U_{dssat})). \tag{3.55}$$

Transconductance g_{m2} is dominated by the transconductance factor β_{FET}. In contrast to the BJT, it is thus found for the FET that g_{m2} is virtually independent of its bias current.

Only a linear term is found for the output conductance. It is given by

$$g_{ds1} = \frac{\lambda}{(1 + \lambda(U_{dsQ} - U_{dssat}))} I_{dQ} \tag{3.56}$$

or, equivalently, the output resistance of a FET is written as

$$r_{ds} = \frac{(1 + \lambda(U_{dsQ} - U_{dssat}))}{\lambda I_{dQ}}. \tag{3.57}$$

When λ is small, r_{ds} may be approximated by $r_{ds} \approx 1/(\lambda I_{dQ})$ [105].

In addition to the currents resulting from $u_{gs}g_{m1}$, $u_{gs}^2 g_{m2}$ and $u_{ds}g_{ds1}$, a current resulting from cross terms due to variations in both u_{gs} and u_{ds} is found:

$$i_{\text{cross}} = 2\beta_{\text{FET}}(U_{gsQ} - U_t)\lambda \cdot u_{gs}u_{ds} = g_x \cdot u_{gs}u_{ds}. \tag{3.58}$$

Current i_{cross} can be made insignificant when the designer selects a FET with a low value of λ, i.e., a FET that does not suffer much from CLM, and biases it at an adequate drain current. FETs with short channels suffer more from CLM and will have a large λ, so i_{cross} may reach non-negligible values for these FETs. The same considerations for minimizing the effects of i_{cross} in negative-feedback amplifiers hold as for the BJT. Cascoding the FET ensures that u_{ds} is small and that i_{cross} will be insignificant with respect to the other currents.

3.4.2 Secondary effects

Up to now, secondary effects that will affect I_d were disregarded. These are: mobility reduction, material resistance and nonlinear channel length modulation.

Incorporating more secondary effects in a model inevitably results in increased complexity. Analytical results will be more correct, but synthesis will be hampered by the increased complexity. A trade-off between model accuracy and designability has to be found. We will therefore limit our discussion to those effects that may occur in MOSFETs and operating regions of the MOSFET when

used in amplifier design. The saturation region is most often encountered in amplifier design, since the FET is able to deliver more gain in this region. Only secondary effects affecting FET behavior in the saturation region are therefore modelled.

Carrier mobility is not constant. It is affected by both the electric field from the gate-bulk voltage (mobility reduction) and the electric field originating from the drain source voltage (velocity saturation). Mobility reduction stems from phonon scattering (μ_{ph}), charge carrier scattering due to the quantum vibrations of the crystal lattice, and surface roughness scattering (μ_{sr}) of charge carriers due to roughness of the interface between silicon crystal and the gate oxide [89]. Surface roughness scattering is especially important under strong inversion conditions, because the strength of the interaction is governed by the distance of the carriers from the surface; the closer the carriers are to the surface, the stronger the scattering due to the surface roughness will be. Mobility degradation is both gate and drain-source voltage dependent. Besides the drain current, it will also affect the derivatives of I_d to U_{gs} (g_{m1} and g_{m2}) and of I_d to U_{ds} (g_{ds1} and g_{ds2}).

The velocity of the carriers is proportional to the electric field originating from U_{ds}. For high values of U_{ds}, carriers acquire more energy than the available thermal energy. These carriers are therefore not in thermal equilibrium with the surrounding lattice, and when they collide with the lattice they lose energy and their speed saturates [60]. This leads to a decrease in drain current in saturation [103][57]. Velocity saturation will affect the drain current, reduce the transconductance, and because of its dependence on U_{ds}, velocity saturation also affects output conductances g_{ds1} and g_{ds2} [90].

An important phenomenon is CLM. CLM is caused by the depletion layer width at the drain, that increases as the drain voltage is increased. It is dependent on the drain-source voltage and mainly affects g_{ds1} and g_{ds2}; and its effect typically increases in small devices with low-doped substrates. Drain voltage induced nonlinearity in the drain current in saturation is caused mainly by channel length modulation [90].

The source and drain areas exhibit parasitic material resistances. Although the effects of these resistances are negligible for long channel MOSFETs ($L \geq 10\mu$m), the voltage drop across the source and drain regions are no longer negligible for short channel MOSFETs biased at high currents [89]. The parasitic resistances may therefore incorporated in the MOSFET model in a similar manner as for the BJT model.

The voltage dependency of the material resistance observed for channel lengths smaller than 2μm is disregarded for reasons of simplicity. Still, because the effects depend on the gate voltage and the surface potential, the material resistance, also called series resistance [91] does influence the nonlinear behavior of the MOSFET. Its influence can be expected to be mainly on the transconductance and may be accounted for by regarding it as a feedback resistance in the source.

Nowadays, it is possible to realize submicron MOSFETs with gate lengths down to several nanometers [102][103][106]-[108]. An attractive advantage of

these short-channel MOSFETs in RF design is the high transit frequency (f_t) that can be obtained. For example, a maximum f_t higher than 200 GHz is observed for a 50 nm n-channel MOSFET [108]. The intrinsic voltage gain $\mu = g_{m1}r_{ds1}$ of such short devices, however, may be lower than that of longer devices [60]. This may be explained by the fact that velocity saturation has a dominant effect in submicron devices, limiting the value of g_{m1} [57] and the CLM effect increases for decreasing channel length [91], reducing the value of r_{ds}. To increase μ, the designer can choose to cascode the short-channel MOSFET.

For a MOSFET biased at high U_{dsQ}, the electric field near the drain may reach very high values. Electrons travelling through the channel from source to drain are accelerated by the high electric field and gain so much energy that they are no longer in thermal equilibrium with the surrounding lattice. They are therefore called hot carriers [57]. These electrons may create extra electron-hole pairs by exciting electrons from the valence band into the conductance band. Some of the manifestations of hot electrons on MOSFET operation are breakdown and substrate current caused by impact ionization (weak-avalanche or even avalanche breakdown) resulting in a bulk current [91], oxide charges owing to tunnelling of charge carriers into oxide states, and photocurrents caused by electron-hole recombination with emission of photons [103]. The bulk current that is generated adds to the drain current. Transconductances g_{m1} and g_{m2} are less affected by hot electrons than g_{ds1} and g_{ds2}.

Hot electrons are most likely to be a problem in short-channel MOSFETs, where the electric field near the drain is likely to be high [57]. Long-channel MOSFETs suffer less from hot electrons. P-channel MOSFETs suffer less from hot carriers because the impact ionization coefficient for holes is much smaller than for electrons [104]. Hot electrons can be avoided by biasing the MOSFET at lower drain-source voltages [104], e.g., $U_{dsQ} \leq 3U_{dssat}$.

The designer determines the dimensions of the FET in a certain application. A short channel length is usually chosen in (very) high frequency applications, while a large area is generally used in current mirror design to reduce the effects of device mismatch (see page 144).

The transition from long-channel to short-channel is given by the following empirical equation [103]:

$$L_{min} = 0.4 \left(r_j t_{ox} \left(W_d + W_s \right)^2 \right)^{\frac{1}{3}} . \tag{3.59}$$

Where t_{ox} is the oxide thickness, r_j the source and drain junction depths, and W_d and W_s are the drain and source junction depletion region depths, respectively. For channel-lengths smaller than L_{min}, MOSFETs are regarded short-channel devices.

3.4.3 MOSFET model limitations

Shorter channel devices are more sensitive to self-heating than longer channel devices, since the thermal resistance increases with decreasing channel area [91].

Submicron devices used at high gate voltages show a significant effect of self-heating on the drain current [90]. Self-heating is not modelled in this work. It is assumed that either the channel length L is long enough to neglect self-heating, or that the bias conditions are such that self-heating does not occur. Besides, studies have shown that self-heating does not introduce nonlinear behavior itself, because it is a linear effect [90]. Another effect that is disregarded in this work, is static feedback. Static feedback is the induction of excess mobile charge in the inversion layer that increases the drain bias beyond saturation, when the average distance between the conducting drain and the channel becomes small [91]. It is inversely proportional to L and linearly coupled to U_{ds} [90][103]. For reasons of simplicity, it is assumed in this work that the drain-source voltage remains low enough to disregard static feedback.

Quantum mechanical effects can not be neglected in modelling short-channel devices [91]. The consequence is a non-zero gate current [107] due to tunnelling of charge carriers through the extremely thin insulating silicone-dioxide layer. Linearity is not affected by the non-zero gate current for devices down to 50 nm, but due to the gate-source resistance not being infinite, it may affect circuit design [107]. Again, this effect is neglected because it is a linear effect.

Finally, another short-channel effect, that is not dealt with in this work, is drain-induced barrier lowering. As U_{ds} increases, the drain depletion region moves closer to the source depletion region, resulting in a significant field penetration from drain to source. Due to this field penetration, the potential barrier at the source is lowered which results in an increased injection of electrons by the source; i.e., the drain current increases and r_{ds} decreases[13] [91]. Drain induced barrier lowering mainly affects MOSFET behavior in subthreshold (it decreases the threshold voltage) [91][103] and may give a slight increase of the drain current, additional to CLM, in the saturation region. However, drain-induced barrier lowering is neglected since CLM dominates.

3.4.4 Modelling the secondary effects

Hot electrons will affect the total drain current. The total drain current is $I_{\text{dtot}} = I_d + I_{hot}$. I_d is the drain current in saturation, that may be affected by CLM and velocity saturation (see Equation (3.61) and (3.68)). Current I_{hot} is due to the hot electrons and is given by [104][91]

$$I_{hot} = \begin{cases} 0 & \text{for: } U_{dsQ} \leq \eta_h \cdot U_{dssat} \\ a \cdot I_d e^{\left(-\frac{V_a}{U_{dsQ} - \eta_h U_{dssat}}\right)} & \text{for: } U_{dsQ} > \eta_h \cdot U_{dssat}. \end{cases} \tag{3.60}$$

Parameter a is the factor of the hot electron current, η_h is the factor of the drain-source voltage above which hot electrons occurs, V_a is a parameter that corresponds to the channel length [91][104].

The secondary effects affect the transconductances g_{m1} and g_{m2} and the output conductances g_{ds1} and g_{ds2}. These effects are modelled next.

[13] Again, a too low r_{ds} can be solved by cascoding the FET.

A. Output conductances

Equation (3.52) predicts that the drain current is independent of U_{ds} in saturation. In reality, however, the drain current varies slightly as U_{ds} is varied due to CLM. For a transistor in the saturation region with drain current ($I_{d,sat}$), given by (3.52), it is possible to incorporate CLM by

$$I_d = \frac{I_{d,sat}}{G_{\Delta L}} \tag{3.61}$$

with

$$G_{\Delta L} = 1 - \alpha \ln\left(\frac{U_{dsQ} - U_{dssat} + \sqrt{(U_{dsQ} - U_{dssat})^2 + U_P^2}}{U_P}\right) \tag{3.62}$$

[91], where α is the channel length modulation factor and U_P is the characteristic voltage of the channel modulation. Both α and U_P are considered empirical parameters[14], and α is inversely proportional to the channel length L [91]. CLM will therefore become more prominent with decreasing L.

Note that in saturation it often holds[15] that $U_{ds} - U_{dssat} \gg U_P$. CLM can thus be simplified to

$$G_{\Delta L} = 1 - \alpha \ln\left(\frac{2(U_{dsQ} - U_{dssat})}{U_P}\right). \tag{3.63}$$

Clearly, $G_{\Delta L}$ will introduce nonlinearities in the drain current when U_{dsQ} is varied.

Performing a Taylor expansion for u_{ds} in the bias point results in a linear conductance

$$g_{ds1} = \frac{\alpha}{(U_{dsQ} - U_{dssat})G_{\Delta L}} I_{dQ} \tag{3.64}$$

and when hot electrons occur

$$g_{ds1,hot} = g_{ds1} \cdot \left(1 + a \cdot e^{\left(-\frac{V_a}{U_{dsQ} - \eta_h U_{dssat}}\right)}\right) + \frac{V_a}{(\eta_h U_{dssat} - U_{dsQ})^2} I_{hot} \tag{3.65}$$

is found.

Note that Equations (3.64) and (3.65) lose validity when $U_{dsQ} = U_{dssat}$. This is because the smooth transition from the linear region to the saturation region has not been modelled. In case U_{dsQ} is slightly larger than U_{dssat}, both equations will be valid again. Output conductance $g_{ds1(hot)}$ will decrease with increasing U_{dsQ}. Hot electrons cause the linear output conductance to increase, as Equation (3.65) shows. The output resistance r_{ds1} equals $1/g_{ds1}$ or $1/g_{ds1,hot}$ in case of hot electrons.

[14] MOSFET model 11 uses $\alpha = 0.025$ and $U_p = 50$ mV as default/typical values.

[15] When $U_{ds} - U_{dssat} = 5U_P$ the difference between between (3.62) and (3.63) is less than 0.5%.

For the second-order nonlinear part of g_{ds},

$$g_{ds2} = -\frac{1}{2}\frac{\alpha}{(U_{dsQ} - U_{dssat})^2}\frac{1}{G_{\Delta L}}\left(1 - \frac{2\alpha}{G_{\Delta L}}\right) I_{dQ} \tag{3.66}$$

and

$$\begin{aligned} g_{ds2,hot} =& g_{ds2} \cdot \left(1 + a \cdot e^{\left(-\frac{V_a}{U_{dsQ} - \eta_h U_{dssat}}\right)}\right) + \\ & a \cdot \left(\frac{1}{2} I_{dQ} V_a \frac{V_a + 2\eta_h U_{dssat} - 2U_{dsQ}}{(\eta_h U_{dssat} - U_{dsQ})^4} + g_{ds1}\frac{V_a}{(\eta_h U_{dssat} - U_{dsQ})^2}\right) \times \\ & e^{\left(-\frac{V_a}{U_{dsQ} - \eta_h U_{dssat}}\right)} \end{aligned} \tag{3.67}$$

are found. The effect of g_{ds2} (and $g_{ds2,hot}$) is modelled by a voltage-controlled current source of value $u_{ds}^2 g_{ds2(hot)}$ at the output of the hybrid-π model. This current source may increase the second-order nonlinearity of the MOSFET while it does not contribute to the linear behavior. Its effect may thus be troublesome.

From Equation (3.66), it can be seen that near the transition point from the linear region to the saturation region g_{ds2} has the largest value. For increasing U_{dsQ}, g_{ds2} will decrease. It must therefore be noted that from a circuit design point of view one should avoid biasing a MOSFET at $U_{dsQ} = U_{dssat}$ for low distortion applications[16], as g_{ds1} and g_{ds2} are maximum there [104]. Moreover, biasing at $U_{dsQ} = U_{dssat}$ means that the FET may go from the saturated region to the linear region and vice-versa due to the output signal voltage. This generates substantial amounts of distortion [60].

Output conductance g_{ds2} is negative. The effect of hot electrons cause a zero crossing of the second-order nonlinear output conductance [89] at some value of U_{dsQ}, as follows from (3.67). Designing for the zero crossing point is not recommended because of the uncertainties in the parameter values.

B. Transconductances

The drain current is affected by both velocity saturation and channel length modulation. I_d is given by

$$I_d = \frac{I_{d,sat}}{G_{vsat} G_{\Delta L}}. \tag{3.68}$$

G_{vsat} represents the effects of velocity saturation and mobility degradation. It is given by [91]

$$G_{vsat} = \sqrt{G_{mob}^2 + (\theta_{sat} U_{dssat})^2}. \tag{3.69}$$

[16] This is consistent with the findings of [104] and [91]. In these publications is also shown that third harmonic distortion is maximal too when $U_{dsQ} = U_{dssat}$.

θ_{sat} is the velocity saturation parameter and G_{mob} represents mobility reduction. The latter is given by

$$\begin{aligned} G_{mob} =& 1 + \sqrt{\theta_{ph} U_{eff}^{\frac{3}{2}} + \theta_{sr} U_{eff}^4} \\ U_{eff} =& \eta \left(\gamma \sqrt{\Phi_B} + \eta (U_{gsQ} - U_t) \right). \end{aligned} \tag{3.70}$$

The coefficients of mobility reduction due to phonon scattering and surface roughness are θ_{ph} and θ_{sr} respectively. Parameter η depends on device process technology, temperature and surface orientation. It is assumed to be $\frac{1}{2}$ for electrons and $\frac{1}{3}$ for holes [91].

Deriving g_{m1} and g_{m2} results in

$$\begin{aligned} g_{m1} = & \underbrace{\left[\frac{1}{(U_{gs} - U_t) - \frac{1}{2} U_{dssat}} \left(1 + \Gamma \frac{(U_{gs} - U_t) - U_{dssat}}{U_{dssat}} \right) \right.}_{(1)} - \\ & \underbrace{\frac{1}{2 G_{vsat}^2} \left[\frac{2 G_{mob}}{3 (G_{mob} - 1)} \eta^2 \frac{\theta_{ph} + 6 \theta_{sr} {U_{eff}}^{\frac{10}{3}}}{{U_{eff}}^{\frac{1}{3}}} + 2 {\theta_{sat}}^2 U_{dssat} \Gamma \right]}_{(2)} - \\ & \left. \underbrace{\frac{\alpha}{G_{\Delta L}} \frac{\Gamma}{(U_{DS} - U_{dssat})}}_{(3)} \right] I_{dQ} \end{aligned} \tag{3.71}$$

with

$$\Gamma = \frac{(U_{gs} - U_t) - U_{dssat} + \gamma \sqrt{\Phi_B}}{(U_{gs} - U_t) - U_{dssat} + \gamma \left(\frac{1}{2} \gamma + \sqrt{\Phi_B} \right)}.$$

Term (1) dominates g_{m1}, term (3) due to the gate-source voltage dependency of the channel length modulation effect is usually negligible when care has been taken to assure that U_{DS} is sufficiently larger than U_{dssat}. Term (2) represents the effect of velocity saturation mobility degradation on g_{m1}.

Taking hot electrons into account, we find

$$\begin{aligned} g_{m1,hot} =& g_{m1} \left(1 + a \cdot e^{\left(- \frac{V_a}{U_{dsQ} - \eta_h U_{dssat}} \right)} \right) - I_{hot} V_a \eta_h \times \\ & \left[\frac{1 - \frac{\gamma}{2 \sqrt{(U_{gsQ} - U_t) + \Phi_B + \gamma \sqrt{\Phi_B} + 0.25 \gamma^2}}}{(\eta_h U_{dssat} - U_{dsQ})^2} - \frac{2 \eta_h U_{dssat}}{(\eta_h U_{dssat} - U_{dsQ})^3} \times \right. \\ & \left. \left(1 - \frac{\gamma}{2 \sqrt{(U_{gsQ} - U_t) + \Phi_B + \gamma \sqrt{\Phi_B} + 0.25 \gamma^2}} \right) \right]. \end{aligned} \tag{3.72}$$

$$
\begin{aligned}
g_{m2} =& \frac{1}{2}\Bigg[\Bigg[\frac{\Gamma U_x + U_{dssat}}{\left(U_x + \frac{1}{2}U_{dssat}\right)U_{dssat}} - \nu\Bigg]^2 + \Bigg[\frac{-\left(1-\frac{1}{2}\Gamma\right)}{\left(U_x+\frac{1}{2}U_{dssat}\right)^2}\left(1+\Gamma\frac{U_x}{U_{dssat}}\right) + \\
& \frac{1}{U_x+\frac{1}{2}U_{dssat}}\left\{\frac{\Gamma}{U_{dssat}}\left(\left[\frac{(1-\Gamma)^2}{\Gamma\upsilon} - \frac{\Gamma}{U_{dssat}}\right]U_x + (1-\Gamma)\right)\right\} + \\
& \frac{\left(\Psi + 2{\theta_{sat}}^2 U_{dssat}\Gamma\right)^2}{2{G_{vsat}}^4} - \frac{1}{2{G_{vsat}}^2}\left\{\frac{\eta^3}{3}\left(40\eta^2\frac{G_{mob}}{G_{mob}-1}\theta_{sr}{U_{eff}}^2 - \frac{\Psi}{U_{eff}}\right)\right. \\
& \left. - \frac{\Psi^2}{2{G_{mob}}^2}\frac{1}{G_{mob}-1} + 2{\theta_{sat}}^2\Gamma^2\left(1+\frac{(1-\Gamma)^2}{\Gamma^2}\frac{U_{dssat}}{\upsilon}\right)\right\} + \\
& \frac{\alpha^2}{{G_{\Delta L}}^2}\frac{\Gamma^2}{\left(U_{DS}-U_{dssat}\right)^2}\left\{1 - \frac{G_{\Delta L}}{\alpha}\left[\frac{(1-\Gamma)^2}{\Gamma^2}\frac{U_{DS}-U_{dssat}}{\upsilon} + 1\right]\right\}\Bigg]\Bigg] I_{dQ}
\end{aligned}
\tag{3.73}
$$

with

$$
\begin{aligned}
\upsilon =& (U_{gs} - U_t) - U_{dssat} - \frac{1}{2}\gamma + \gamma\sqrt{\Phi_B} \\
U_x =& (U_{gs} - U_t) - U_{dssat}
\end{aligned}
$$

$$
\Psi = \frac{2}{3}\eta^2\frac{G_{mob}}{G_{mob}-1}\frac{\theta_{ph} + 6\theta_{sr}{U_{eff}}^{\frac{10}{3}}}{U_{eff}^{\frac{1}{3}}}
$$

$$
\nu = \left(\frac{\Psi + 2{\theta_{sat}}^2 U_{dssat}\Gamma}{2{G_{vsat}}^2} + \frac{\alpha}{G_{\Delta L}}\frac{\Gamma}{U_{DS}-U_{dssat}}\right)
$$

and

$$
\begin{aligned}
g_{m2,hot} =& g_{m2}\cdot\left(1 + a\cdot e^{\left(-\frac{V_a}{U_{dsQ}-\eta_h U_{dssat}}\right)}\right) - g_{m1}\cdot a\cdot e^{\left(-\frac{V_a}{U_{dsQ}-\eta_h U_{dssat}}\right)}\times \\
& V_a\eta_h\left(1-\varsigma\right)\cdot\left(\frac{1}{(\eta_h U_{dssat} - U_{dsQ})^2} - 2\frac{\eta_h U_{dssat}}{(\eta_h U_{dssat} - U_{dsQ})^3}\right) + \\
& \frac{1}{2}I_{hot}V_a\eta_h\left(\frac{\frac{2\varsigma}{\gamma^2}(\eta_h U_{dssat}(2U_{dsQ} - \eta_h U_{dssat}) - U_{dsQ}^2))}{(\eta_h U_{dssat} - U_{dsQ})^4} + \right. \\
& \left.\frac{\eta_h\left(1-\varsigma\right)^2\cdot(2(\eta_h U_{dssat} - U_{dsQ}) + V_a)}{(\eta_h U_{dssat} - U_{dsQ})^4}\right)
\end{aligned}
\tag{3.74}
$$

where

$$
\varsigma = \frac{\gamma}{2\sqrt{(U_{gsQ} - U_t) + \Phi_B + \gamma\sqrt{\Phi_B} + 0.25\gamma^2}}. \tag{3.75}
$$

Comparing equation (3.54) with (3.71) and (3.55) with (3.73), the following is observed: at low values of U_{gsQ} little difference is found between the values

predicted by the simple equations for g_{m1} and g_{m2} and the elaborate equations for the transconductances. The same holds for I_{dQ}. At higher values of U_{gsQ}, mobility reduction and velocity saturation start to influence I_d. As a result I_d will be less than given by (3.53), and g_{m1} and g_{m2} will both be smaller than given by (3.54) and (3.55).

The equations for g_{m1} and g_{m2} are elaborate and do not give much insight for design purposes, so the simpler equations (3.54) and (3.55) are preferably used. Up to some maximum bias voltages $U_{gs,max}$ and $U_{ds,max}$ they can be used without introducing too much error, e.g., $< 10\%$.

These maximal values of the gate-source ($U_{gs,max}$) and drain-source voltages ($U_{ds,max}$) are, for simplicity, determined for two cases. The first case is valid for MOSFETs with a long channel, e.g., $L \gg 2.4$ μm, since velocity saturation is negligible in that case [103], so mobility reduction determines G_{vsat}. The second case assumes G_{vsat} to be determined by velocity saturation, as is often the case in short-channel MOSFETs, e.g., $L < 1$ μm.

In the first case, a maximum U_{gs} can be determined from (3.70) for a certain maximum amount of mobility reduction

$$U_{gs,max} = \frac{1}{\eta}\left[\frac{1}{\eta}\frac{(G_{mob,max}-1)^2}{\theta_{ph}}\sqrt{\frac{(G_{mob,max}-1)^2}{\theta_{ph}}} - \gamma\sqrt{\Phi_B}\right] + U_t \quad (3.76)$$

with $G_{mob,max} = 1.06$. Using this equation and equation (3.51), the corresponding maximum $U_{DSsat,max}$ can be found.

Channel length modulation also affects I_d and its nonlinear behavior. CLM is limited when U_{dsQ} does not exceed $U_{ds,max}$. Voltage $U_{ds,max}$ follows from (3.63) and (3.51).

$$\begin{aligned} U_{ds,max} =& (U_{gs,max} - U_t) + \frac{\gamma^2}{2} - \\ & \gamma\left(\sqrt{(U_{gs,max} - U_t) + \Phi_B + \gamma\sqrt{\Phi_B} + \frac{\gamma^2}{4}} - \sqrt{\Phi_B}\right) + \frac{U_P}{2}e^{\frac{c}{\alpha}} \end{aligned} \quad (3.77)$$

with $c = 1 - G_{\Delta L}$. A value of $G_{\Delta L} = 0.98$ is proposed, since CLM is than only 2 %.

In the second case, $U_{DSsat,max}$ follows from (3.69) and can be approximated by $U_{DSsat,max} \approx G_{vsat,max}/\theta_{sat}$. Using this approximation and (3.51), the maximal gate-source voltage can be determined as

$$U_{gs,max} = U_t - \gamma\sqrt{\Phi_B} - \frac{1}{2}\gamma^2 + \frac{G_{vsat,max}}{\theta_{sat}} + \frac{1}{2}\gamma\left(\gamma + 2\sqrt{\Phi_B + \frac{G_{vsat,max}}{\theta_{sat}}}\right) \quad (3.78)$$

with $G_{vsat,max} = 1.06$. U_{dsQ} is preferably chosen $\leq 3U_{DSsat,max}$ to limit detrimental effects of hot electrons. Moreover, cascoding the MOSFET also reduces these detrimental effects.

The equations and values of $G_{mob,max}$, $G_{vsat,max}$ and c presented here will, for a MOSFET biased at $U_{gs,max}$ and $U_{DS,max}$, present an I_{dQ} being about 3 %

lower than the current given by first-order equation (3.53). Transconductance g_{m1} is about 4 % lower and g_{m2} is about 8 % lower. For smaller values of $G_{mob,max}$ and $G_{vsat,max}$ ($1.00 \leq G_{mob,max}, G_{vsat,max} \leq 1.06$) and of c, the deviations will be smaller. For simplicity, the equations given here do not take hot electrons into account. Using the same approach as given here, however, equations taking hot electrons can be derived.

I_{dQ}, g_{m1} and g_{m2} can thus be determined using the first-order equations when $U_{gs} \leq U_{gs,max}$ and $U_{dssat} < U_{ds} \leq U_{ds,max}$ to sufficient accuracy. In the remainder of this work it will be assumed that $U_{gs} \leq U_{gs,max}$ and $U_{dssat} < U_{ds} \leq U_{ds,max}$ and therefore the simple equations for g_{m1} and g_{m2} will be used.

C. Capacitances

In the saturation region [57]

$$\begin{aligned} C_{gs} =& \frac{2}{3} W L C_{ox} + C_{gsov} \\ C_{gd} =& C_{gdov}. \end{aligned} \tag{3.79}$$

This indicates that in saturation, a small change in U_{ds} does not contribute to the gate or channel charge, since the channel is pinched off. Instead, the entire channel charge is assigned to the source terminal, giving a maximum value of the capacitance C_{gs} [103].

Assuming that the source and drain regions each diffuse under the gate by L_d, the gate-source and gate-drain overlap capacitances are given by [57]

$$C_{gsov} = C_{gdov} = W L_d C_{ol} \tag{3.80}$$

Drain-bulk capacitance C_{bd} is a junction capacitance and can be calculated using Equation (3.18). The capacitances may be regarded as constants, hence they do not affect envelope detection properties.

D. Modified hybrid-π model for FETs

Figure 3.10 shows the hybrid-π model for evaluating medium signal linear and second-order nonlinear behavior of a FET.

When a voltage driven FET loaded by resistor R_l is considered, both the linear and the second-order nonlinear parts of the drain current i_d can be calculated. Neglecting higher order terms,

$$\begin{aligned} i_d =& i_{d1} + i_{d2} \\ i_{d1} =& u_{gs} g_{m1} \\ i_{d2} =& u_{gs}^2 m \left(g_{m2} + g_{m1}^2 g_{ds2} \left(\frac{r_{ds} R_l}{r_{ds} + R_l} \right)^2 \right). \end{aligned} \tag{3.81}$$

Coefficient m can be taken 0.5 for second-order distortion and equals the modulation depth in the case of envelope detection. Current i_{d2} may become zero for

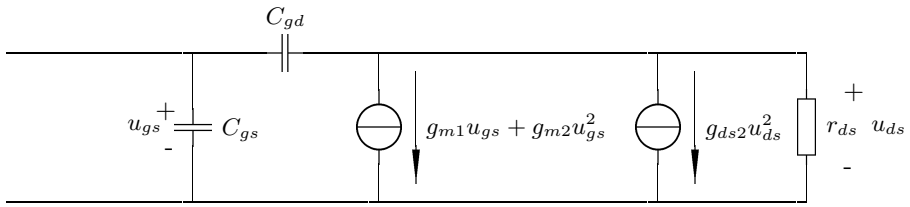


Figure 3.10: Medium signal hybrid-π model for calculating the linear and quadratic transfers of the FET. The transconductance is modelled by a voltage-controlled current source having both a linear and a quadratic transfer. Another voltage-controlled current source represents the nonlinear behavior of the output conductance. Note that C_{bd} and parasitic capacitances and/or inductances from interconnects on the die have been omitted for simplicity.

a certain value of R_l, since both g_{m1} and g_{m2} are positive, while g_{ds2} is negative when hot electrons do not occur. Measurements and simulations presented in [109] show a cancelation of second-harmonic distortion as predicted by Equation (3.81).

Especially for higher values of R_l, the g_{ds2} term may become much larger than g_{m2} in (3.81). As a result both envelope detection and second-harmonic distortion increases. The designer has to ensure that R_l remains low enough to

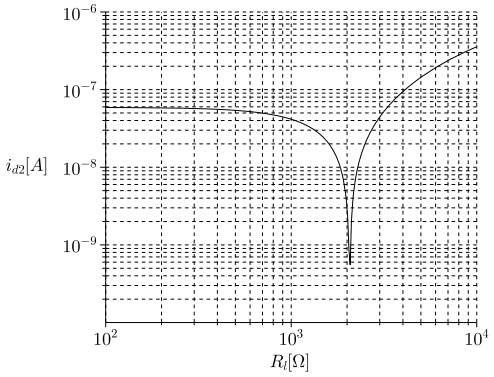


Figure 3.11: Second order nonlinear component (distortion or EMI) in the drain current. Parameters: $u_s = 10$ mV, m= 0.5, $g_{m1} = 5.98$ mA/V, r_{ds}= 7.55 kΩ, $g_{m2} = 1.18$ mA/V^2, $g_{ds2} = -12.54$ μA/V^2.

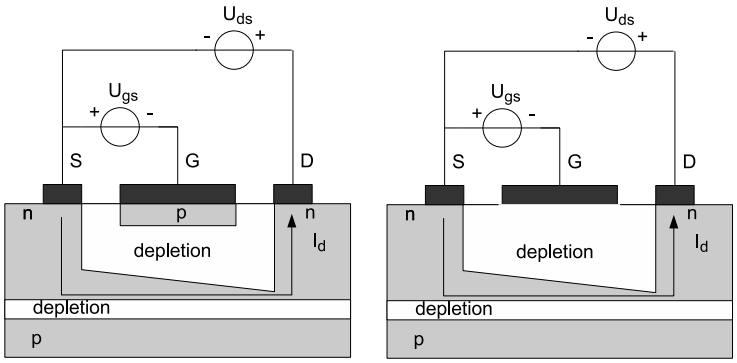
avoid the detrimental effect of g_{ds2}. When $R_l \leq 1/20 r_{ds}$ it is found that i_{d2} is mainly determined by g_{m2}. This is the preferred situation. After all, besides being a source of nonlinearity, the transconductance also contributes to the linear increase of the signal transfer, while the output conductance (g_{ds2}) does not.

A straightforward manner to realize a low R_l is to cascode the common-source stage. Under the assumption of adequate loop gain in the common-gate or common-base stage, its input resistance is about $1/(g_{m1})$. In the case of equal biasing and identical devices it is expected that the contribution of g_{ds2} can be neglected. For the parameters given in Fig. 3.11 the contribution of g_{ds2} to i_{d2} is about 1% when the FET is cascoded.

Moreover, due to parameter uncertainties in FETs of the same type from different fabrication runs, it is not possible to design for zero second-order nonlinearity. It is therefore recommendable to suppress the nonlinear output conductance so that only the second-order nonlinear transconductance remains. As general design rule, FETs should be cascoded to cancel the detrimental effect of the second-order voltage-controlled current source $g_{ds2}u_{ds}^2$. In the remainder of this work it is therefore assumed that all FETs are cascoded. More about cascoding is found in Chapter 4.

3.5 The junction field-effect transistor

Just like in case of the MOSFET, a conducting channel between source and drain controls the current through the device. The conducting channel in a junction field-effect transistor (JFET) is controlled by a gate-source and a gate-drain voltage. Usually, a reverse biased p-n junction will control the conductivity of the channel. Saturation occurs when the channel is pinched-off in the drain region (see Figs. 3.12(a) and 3.12(b)).



(a) Conducting drain-source channel is controlled by a reverse-biased pn-junction in a JFET.

(b) Conducting drain-source channel is controlled by a reverse-biased metal-semiconductor junction (Schottky barrier) in a MESFET.

Figure 3.12: Junction FETs in the active forward (i.e., saturation region). The channel between drain and source is pinched-off near the drain.

An equation presented in textbooks (and used by SPICE) for the drain cur-

rent in the saturation region (or forward active region) ($U_{ds} \geq U_{gs} - U_t$) is a good approximation to measured device characteristics in the case of long gate length (≥ 5 μm) [110], and is given by (e.g., [109][93][110])

$$\begin{aligned} I_d = \quad & \beta_{\text{FET}}(U_{gs} - U_p)^2 \left[1 + \lambda U_{ds}\right] \\ \text{where} \quad \beta_{\text{FET}} = \quad & \frac{I_{dss}}{U_p^2}. \end{aligned} \tag{3.82}$$

Velocity saturation may occur in short-channel devices. This effect may be approximated using the same equations that will be presented in Section 3.6 about the MESFET.

I_{dss} is the drain to source current with the gate shorted to the source, i.e., the maximal drain current that may flow through the JFET. U_p is the pinch-off voltage, which is comparable with U_t of the MOSFET. Parameter λ is again used for the first-order characterization of channel length modulation. With known fabrication process parameters λ can be calculated exactly [111]. Also, λ is often given in SPICE models, and it can be measured easily. Channel length modulation in saturation is, however, a nonlinear effect and is therefore not correctly modelled by the (constant) λ.

Kuntman [109] proposes a non-physics based nonlinear CLM equation. It seems to present reasonably accurate results, but both U_{dsQ} and U_{dssat} have to be carried to the same unknown power, and also an unknown coefficient is used in the equations. The two unknowns have to be determined from measurements of g_{ds1}. A physics-based equation for CLM is presented by Hartgring [112]. It is, however, based on a one-dimensional solution of Poisson's equation in the pinch-off region and is therefore expected to be inaccurate. When the models of Kuntman and Hartgring are used, a linear r_{ds} and nonlinear g_{ds2} are found. This is also found when equation (3.63) is used to model CLM. Some preliminary calculations show that (3.63) gives values for r_{ds} closer to values given in datasheets than the equations of Kuntman and Hartgring. More research has to be performed, however. This is beyond the scope of this work.

To determine g_{m1}, g_{m2}, g_{ds1}, and g_{ds2} exactly, equations (3.71), (3.73), (3.64), and (3.66) can be used. Since g_{ds2} may hamper low second-order behavior, a JFET should be cascoded also. In that case, Equations (3.54), (3.55) and (3.57) can be used for design purposes. Cascoded JFETs are therefore assumed in the remainder of this work.

The gate-source and gate-drain capacitances are formed by junction capacitances and can be approximated using (3.18). The total capacitance is C_{iss} where C_{gs} is about 75% and C_{gd} about 25% of C_{iss} [110].

3.6 The metal-semiconductor field-effect transistor

MESFET (GaAs) devices are constructed with a metal-semiconductor junction gate instead of a p-n junction gate [110], see Fig. 3.12(b). The channel is controlled in the same manner as the JFET.

Metal-semiconductor junctions in GaAs are easier to process and have lower resistance than a GaAs p-n junction. The low resistance of the gate is important to keep the noise figure of the FET low [113] and also minimize its effect on the frequency response. The electrom mobility and drift velocity of a GaAs device are five and two times higher than Si, respectively. In addition, the peak drift velocity is reached at a much lower electric field for GaAs. Also, the parasitic capacitances are small [110]. This leads to a much higher f_t (20 GHz, L= 0.7 μm [113][110]) than the Si JFET, which may be beneficial in the design of wideband/high-frequency amplifiers.

Sophisticated models have been developed for SPICE that accurately describe MESFET behavior [114][115]. These models are not suited for hand calculations. Therefore, a slightly less accurate model that is suited for hand calculations and design will be presented. It is the Raytheon or Statz model that is also used in SPICE [110][93]. The drain current in this model is given by

$$I_d = \beta_{\text{FET}} \frac{(U_{gs} - U_t)^2}{1 + b(U_{gs} - U_t)} (1 + \lambda U_{ds}). \tag{3.83}$$

Just like short-channel MOSFETs, MESFETs suffer from velocity saturation. This is represented by b, the velocity saturation parameter. Up to the bias point that may move the velocity saturation point toward the source, reducing the effective channel length, velocity saturation tends to reduce I_d, almost linearizing it. The other parameters have the same meaning as in case of the JFET.

For the transconductances is derived to hold

$$\begin{aligned} g_{m1} =& 2\sqrt{\beta_{\text{FET}} I_{dQ}(1 + \lambda U_{dsQ})} \times \\ & \frac{b\sqrt{\beta_{\text{FET}} I_{dQ}(1 + \lambda U_{dsQ}) + 4\left(\frac{\beta_{\text{FET}}}{b}\right)^2 (1 + \lambda U_{dsQ})^2}}{2\beta_{\text{FET}}(1 + \lambda U_{dsQ}) + I_{dQ} b^2 \left(1 + \sqrt{1 + \left(\frac{4\beta_{\text{FET}}}{b^2 I_{dQ}}\right)(1 + \lambda U_{dsQ})}\right)} \end{aligned} \tag{3.84}$$

and

$$\begin{aligned} g_{m2} =& \beta_{\text{FET}}(1 + \lambda U_{dsQ}) \times \\ & \left(\frac{1}{1 + b(U_{gsQ} - U_t)} - b(U_{gsQ} - U_t) \frac{2 + b(U_{gsQ} - U_t)}{(1 + b(U_{gsQ} - U_t))^3} \right). \end{aligned} \tag{3.85}$$

For r_{ds}, the same equation as (3.57) is found. Although the simple equation does not give rise to g_{ds2}, it may be assumed that an actual device will exhibit a g_{ds2}. However, since r_{ds} is usually low, and may fall with frequency to 50 % off its initial value due to dispersion[17], MESFETs are usually cascoded in practical designs [113]. The effects of second-order nonlinear term g_{ds2} are then negligible. Therefore, in this work it will be assumed that MESFETs are cascoded.

[17] Dispersion is thought to be related to the, e.g., trapping of carriers at the channel-substrate interface. Dispersion takes place at low frequencies. In the example given in [113] at about 10 kHz.

The cross-product transconductance is found to be given by

$$g_x = 2\beta_{\text{FET}}(U_{gsQ} - U_t)\lambda \left[\frac{1}{1 + b(U_{gsQ} - U_t)} - \frac{b}{2} \frac{(U_{gsQ} - U_t)}{(1 + b(U_{gsQ} - U_t))^2} \right]. \quad (3.86)$$

C_{gs} will be about 85% and C_{gd} will be about 15% of the total capacitance C_{iss} [110]. These metal-semiconductor junction capacitances may also be approximated using Equation (3.18), with m_e= 0.5 [113].

3.7 Conclusions

Both linear and second order nonlinear behavior of transistors has been investigated, from which modified, i.e., medium signal, hybrid-π circuit models have been derived. A hybrid-π model valid for the BJT and another valid for FETs have been presented.

It was found that if the BJT is voltage driven ($R_s \ll r_\pi$) the weak nonlinear behavior of the BJT is determined by the nonlinear transconductance. When the signal source exhibits current source characteristics ($R_s \gg r_\pi$) and the load of the BJT is a current load (i.e., the load impedance is much smaller than r_o) the signal transfer of the BJT is completely determined by β_{ac}. Especially in the mid-current region, the nonlinearity of β_{ac} is negligibly low. The BJT is therefore preferably current driven and current loaded and biased in the mid-current region for low distortion behavior. Equations for determining the mid-current region were presented.

The total nonlinear behavior of the FET is represented by two voltage-controlled current sources at the output of the hybrid-π model. One represents the nonlinearity of the transconductance and is controlled by u_{gs}, and the other represents the nonlinearity of the output conductance/resistance, r_{ds}, and is controlled by u_{ds}. The combined action of both controlled nonlinear sources determines the total nonlinear behavior of the FET. The nonlinearity of the output conductance was found to be troublesome, since it may increase the total nonlinear behavior of the FET, while it does not increase the linear signal power in any way. The detrimental effects of the nonlinear output conductance are negligible when the FET is cascoded. Second-order nonlinearity is determined by the nonlinearity of the transconductance in that case. FETs are therefore preferably cascoded when used in low distortion or low-EMI susceptible amplifiers.

Secondary effects like mobility reduction complicate the equations for the linear and second-order nonlinear transconductances (g_{m1} and g_{m2}) of the MOSFET. Given constraints on the bias current and drain-source voltage, the (well known) simple equations for g_{m1} and g_{m2} can, however, be used. Equations for determining the allowable bias conditions were also presented.

Chapter 4

The Cascode and Differential amplifier stages

Single active devices often have a rather poor behavior regarding accuracy of their transfers, high-frequency behavior, linearity, etc. To improve the accuracy of the transfers, special combinations of active devices have been developed. These combinations often consist of two active devices connected in such a way that the total behavior of the combination is that of one active device with improved behavior. In this chapter two special combinations of active devices will be presented and their linear and second-order nonlinear behavior will be analyzed. These two special stages are the cascode stage and the differential stage.

4.1 Cascode stages

The name 'cascode' stems from the time that vacuum-tubes were the active devices used in electronics. In those days, a cascode was a **casc**ade of common-cathode and common-grid stages joined at the an**ode** of the first stage and the cath**ode** of the second stage [57]. Nowadays, the name cascode is still used for the analogous configuration of semiconductor devices.

Although cascode stages are formed by two active devices, it is common practice to regard the cascode as one active device with improved performance. The cascode stage does, for instance, not suffer from the Miller effect and the detrimental effect of both the cross term transconductance g_x and nonlinear output conductance for a single transistor is made negligible. A detailed description of the cascode is therefore given in this chapter.

Since there are two types of semiconductor devices and the cascode is formed by two devices, four possible cascode configurations exist. These are the BJT-BJT, the FET-BJT, the BJT-FET and the FET-FET cascode. These four combinations are depicted in Fig. 4.1. After a generic discussion of cascodes, the four depicted cascode stages are discussed.

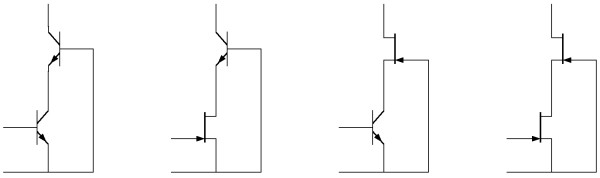


Figure 4.1: The four possible cascode stages. Biasing is omitted for clarity. From left to right: the BJT-BJT, the FET-BJT, the BJT-FET and the FET-FET cascode

4.2 Generic cascode

Figure 4.2 shows a generic small-signal representation of the cascode. With the necessary changes, it holds for both BJTs and FETs. Resistance r_{ss} represents a series resistance equal to r_B in case of a BJT and equal to the gate series resistance in case of a FET. This resistance has been omitted from the second transistor model for simplicity. Modified hybrid-π models of the cascode stages, that will show the same linear behavior, will be derived from Fig. 4.2. Sources representing nonlinear behavior are not shown in Fig. 4.2, but will be added to the modified hybrid-π models of the cascode stages.

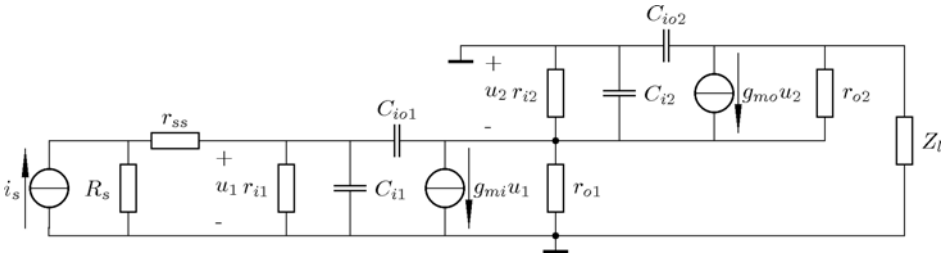


Figure 4.2: Generic small-signal cascode representation.

By inspection of Fig. 4.2, the output resistance (r_{oCa}) of a cascode stage at low frequency can be written as

$$r_{oCa} = \frac{r_{o1}r_{i2}}{r_{o1}+r_{i2}} + r_{o2}\left(1 + g_{mo}\frac{r_{o1}r_{i2}}{r_{o1}+r_{i2}}\right). \tag{4.1}$$

Resistances r_{i2} and r_{o2} are the input and output resistance of the loading stage (a current follower), respectively, and r_{o1} is the output resistance of the input stage. The transconductance of the current follower is g_{mo}. Resistance r_{oCA} may reach considerably higher values than r_{o1} and r_{o2}. Capacitance C_{io2} is in parallel with r_{oCa}. The output impedance of a cascode is thus given by $r_{oCa}//C_{io2}$. This impedance has a pole $p_{oCa} \approx -1/(r_{oCa}C_{io2})$. Since there is a capacitance

($\approx C_{i2}$) shunting r_{i2}, another pole is present in the output impedance at $p_i \approx -1/((r_{o1}//r_{i2})C_{i2})$. Pole $|p_{oCa}|$ is located at a lower frequency than $|p_i|$ in practical cases. The latter pole is therefore disregarded in the cascode model.

The input stage is loaded by the single-stage current follower (CF) with an input impedance of

$$Z_{inCF} = \frac{r'_{i2}}{1 + r'_{i2}(g_{mo} + sC_{i2})} = \frac{1}{\frac{1}{r'_{i2}} + g_{mo} + sC_{i2}} \tag{4.2}$$

and

$$r'_{i2} = r_{i2}//r_{o1}//(r_{o2} + R_l).$$

When $g_{mo} \gg 1/r'_{i2}$, as is often easy to realize, $Z_{inCF} \approx 1/g_{mo} \cdot 1/(1+sC_{i2}/g_{mo}))$ or $Y_{inCF} \approx g_{mo} + sC_{i2}$. This admittance[1] loads the input stage. The input admittance Y_{inCF} is approximately g_{mo} up to ω_T of the CF ($\omega_{T\mathrm{CF}}$), after which it reduces in value. It may thus be expected that when the input impedance of the CF stage is low enough at low frequencies, it will also be low enough at frequencies approaching and higher than f_t of the transistor.

The voltage across C_{io1} thus equals $u_1(1+g_{mi}/Y_{inCF})$. As a consequence, the current through C_{io1} equals $u_i sC_{io1}(1 + g_{mi}/Y_{inCF})$. The loading with the CF stage has as consequence that a capacitance equal to $C'_{io1} = C_{io1}(1+g_{mi}/Y_{inCF})$ is shunting C_{i1} (Miller approximation). For frequencies lower than the pole in Y_{inCF}, which is approx. equal to f_t, $C'_{io1} = C_{io1}(1+g_{mi}/g_{mo})$ and for frequencies higher than this pole its value reduces to $C'_{io1} \approx C_{io1}$. This kind of representation suggests that feedback from the output to the input of the input stage is virtually eliminated. The Miller effect is suppressed by the CF, but feedforward from input to output still remains.

The current gain in the pass band of the CF stage equals

$$A_{tCF} = \frac{g_{mo}r_{i2}}{1 + g_{mo}r_{i2}} \frac{1}{1 + \frac{r_{i2}\frac{r_{o1}+r_{02}}{r_{o1}r_{o2}} + Z_l\frac{r_{o1}+r_{i2}}{r_{o1}r_{o2}}}{1+g_{mo}r_{i2}}}. \tag{4.3}$$

For a good functioning cascode (i.e., it behaves as a transistor with almost unilateral behavior) the current gain of the CF should be one. Current gain A_t approaches one when $g_{mo}r_{i2} \gg 1$, $g_{mo} \gg 1/r_{i2}$, and $r_{o2} \gg Z_l$. A Z_l much lower than r_{o2} (e.g. approaching zero) is preferred. This case is called current loading in this work. The transconductance is approximately equal to g_{mi} and the input impedance is $r_{ss} + r_{i1}//Z_{(C_{i1}+C'_{io1})}$.

The transfer from input signal to output current has two poles under current load conditions ($Z_l = 0$). One is the pole of the CF stage and has a value $p_{\mathrm{CF}} \approx -\omega_{T\mathrm{CF}}$ [2], with $\omega_{T\mathrm{CF}}$ being the angular transit frequency of the BJT or FET used in the CF. The other pole is determined by the input stage and the signal

[1] In deep sub-micron technology (CMOS $\leq$ 90 nm), the low value of r_{o2} lowers Y_{inCF}. The designer should therefore check for proper cascode behavior.

source. It follows from Fig. 4.2 (under assumption that $r_{ss} \ll R_s$)

$$p_i = -\frac{R_s + r_i}{R_s} \frac{1}{r_i(C_{i1} + C_{io1}(1 + g_{mi}/Y_{inCF}))} \quad \text{(cascoded)} \quad \text{and} \quad (4.4)$$

$$p_i = -\frac{R_s + r_i}{R_s} \frac{1}{r_i(C_{i1} + C_{io1})} \quad \text{(uncascoded)},$$

with R_s being the signal source resistance. Pole $|p_i|$ shifts to a higher frequency for decreasing values of R_s. This is called resistive broadbanding.

The value of p_i for an uncascoded current loaded stage is also given in (4.4) for illustration purposes. Pole $|p_i|$ of the cascoded stage is shifted to a lower frequency by an amount of $(1 + g_{mi}/Y_{inCF})$ compared to the pole of an uncascoded current loaded stage. Note that the pole of an uncascoded stage that is loaded by a high impedance (voltage load) is typically located at a (much) lower frequency due to the Miller effect.

C_{io1} causes a zero in the right half plane at $z = g_{mi}/C_{io1}$ [2], or (written differently) $z = \omega_{Ti}(C_{i1} + C_{io1})/C_{io1}$. This zero may be located at a frequency higher than poles $|p_i|$ and $|p_{\text{CF}}|$. It can be expected that $|p_i|$ will be located at a lower frequency than $|p_{\text{CF}}|$ in practical cases.

The contribution of the CF stage to the second-order nonlinear behavior of the cascode is negligible with respect to the input stage. This is due to the feedback action and the earlier mentioned conditions for $A_{t\text{CF}}$ approaching one, i.e., a high loop gain. It can be calculated exactly by using the method described in Chapter 5 or in [116], to determine the second-order nonlinear behavior of single-stage negative-feedback amplifiers . An example will be give in subsection 4.2.1.

Under assumption of $\omega_{T\text{CF}} = \omega_{Ti}$, the transfer of the input signal to the output current decreases by 40 dB/dec for frequencies higher than $|p_{\text{CF}}|$ up to z. For frequencies higher than z, this reduces to 20 dB/dec. The slope of the envelope detection properties due to EMI are therefore twice as steep. To simplify the design process, the high frequency behavior is approximated by using p_i only.

The discussion about the generic cascode model and equations hold for the four possible cascode types. By changing the parameter names to those of a BJT (CE, CB) or FET (CS, CG), the parameters listed in Table 4.1 are found. Note that resistor r_{ss} may usually be neglected and $r_i \to \infty$ in case of FETs. The equations for p_i are discussed in Subsections 4.2.1 to 4.2.4.

Two modified hybrid-π models follow from the previous discussion and using the parameters given in Table 4.1. One for the cascoded BJT and one for the cascoded FET.

The hybrid-π model capable of describing both linear and second-order behavior of the cascoded BJT (a CE stage loaded by a CF (a common-base (CB) or a common-gate (CG) stage)) is shown in Figure 4.3. At the input, a voltage-controlled current source of value $g_{\pi 2\text{CE}}u_{be}^2$ represents the second-order nonlinearity of the base current due to the nonlinear conductance $(1/r_\pi)$ of the CE stage. At the output there is also a voltage-controlled current source of value $g_{m1\text{CE}}u_{be} + g_{m2\text{CE}}u_{be}^2$ that represents the linear and second-order nonlinear term

Table 4.1: Overview of the parameters of the cascode combinations.

Cascode	p_i [rad/s]$\approx$	p_o [rad/s]	z [rad/s]	r_{oCa} [Ω] $\approx$	C_{oCa} [F]
BJT-BJT	$-\frac{R_s+r_{\pi CE}}{R_s}\frac{\omega_{TCE}}{\beta_{acE}}$	$-\omega_{TCB}$	$\frac{g_{mCE}}{C_{\mu CE}}$	$r_{\pi CB}+r_{oCB}(1+\beta_{acCB})$ $\approx \beta_{acCB}\cdot r_{oCB}$	$C_{\mu CB}$
FET-BJT	$\frac{-1}{R_s(C_{gsCS}+C_{gdCS})}$	$-\omega_{TCB}$	$\frac{g_{mCS}}{C_{gdCS}}$	$r_{\pi CB}+r_{oCB}(1+\beta_{acCB})$ $\approx \beta_{acCB}\cdot r_{oCB}$	$C_{\mu CB}$
BJT-FET	$-\frac{\frac{R_s+r_{\pi CE}}{R_s\cdot r_{\pi CE}}\times 1}{C_{\pi CE}+C_{\mu CE}\left(1+\frac{g_{mCE}}{g_{mCG}}\right)}$	$-\omega_{TCG}$	$\frac{g_{mCE}}{C_{\mu CE}}$	$r_{dsCG}+r_{oCE}(1+\mu_{CG})$ $\approx \mu_{CG}\cdot r_{oCE}$, $\mu_{CG}=g_{mCG}\cdot r_{dsCG}$	C_{gdCG}
FET-FET	$\frac{-1}{R_s\left(C_{gsCS}+C_{gdCS}\left(1+\frac{g_{mCS}}{g_{mCG}}\right)\right)}$	$-\omega_{TCG}$	$\frac{g_{mCS}}{C_{gdCS}}$	$r_{dsCG}+r_{dsCS}(1+\mu_{CG})$ $\approx \mu_{CG}\cdot r_{dsCS}$, $\mu_{CG}=g_{mCG}\cdot r_{dsCG}$	C_{gdCG}

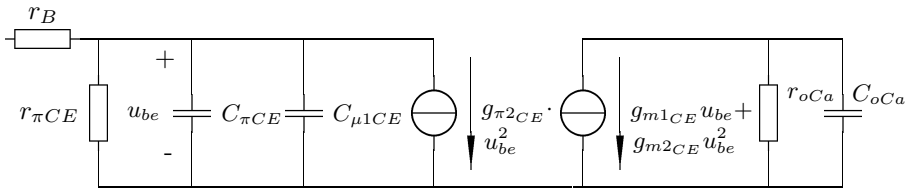


Figure 4.3: Modified hybrid-π model for the cascoded BJT. Valid for linear and second-order nonlinear transfer analysis. $C_{\mu 1CE}$, r_{oCa}, and C_{oCa} depend on whether the BJT is cascoded by a FET or a BJT. See text for details.

of the collector current due to the exponential input voltage to output current relation of the CE stage.

Figure 4.4 shows the hybrid-π model of a common-source (CS) stage cascoded by a current follower. The FET has two sources of nonlinearity, the transconduc-

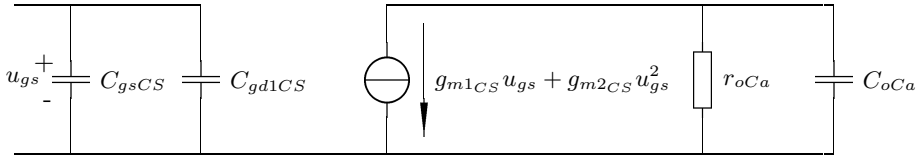


Figure 4.4: Modified hybrid-π model for the cascoded FET. Valid for linear and second-order nonlinear analysis. C_{gd1CS}, r_{oCa}, and C_{oCa} depend on whether the FET is cascoded by a FET or a BJT. See text for details.

tance and the output conductance. As was shown in Chapter 3, the nonlinear output conductance causes a drain current $i_{d2} = g_{ds2}u_{ds}^2$. A larger output voltage swing causes a larger contribution of the nonlinear output conductance to the total second-order nonlinear behavior. For the same reasons, cross-term transconductance g_x will also add to the nonlinear behavior.

The low input impedance of either the CB or CG stage, that usually is in a range of tens to hundreds of Ohms (depending on the bias current), effectively nullifies the effects of g_{ds2CS} and g_{xCS}. The resulting nonlinear behavior is thus only determined by the nonlinear transconductance, provided that the CB stage is biased in the mid-current region.

Note that the zero in the right half plane does not follow from analysis of Figs. 4.3 and 4.4.

4.2.1 BJT-BJT cascode

The BJT-BJT cascode consists of a common-emitter (CE) stage loaded by a common-base (CB) stage. Figure 4.3 presents its hybrid-π model.

For the current loaded CE stage the transit frequency is $\omega_T = g_{m1}/(C_{\pi\mathrm{CE}} +$

$C_{\mu\text{CE}}$) and for the cascode stage by $\omega_T = g_{m1}/(C_{\pi\text{CE}} + C_{\mu 1\text{CE}})$, with[2] $C_{\mu 1\text{CE}} \approx C_{\mu\text{CE}}(1 + g_{m1CE}/g_{m1CB})$. Since usually $C_\pi > C_{\mu 1}$ in the mid-current region, a cascode will therefore add virtually the same p_i to the amplifier design as a CE stage, see Table 4.1. The equality $1/[r_{\pi CE}(C_{\pi CE} + C_{\mu Ce})] = \omega_{TCE}/\beta_{acCE}$ has been used to derive the equation for p_i.

Besides the qualitative discussion of the contribution to the nonlinear behavior of the cascode of the CF stage given earlier, the following qualitative discussion may elucidate that discussion for a CB stage. The current gain of the CB stage is well approximated by $\alpha = \frac{\beta_{ac}}{1+\beta_{ac}} \frac{1}{1+j\frac{\omega}{\omega_T}}$ [2] if r_{oCB} is large compared to $r_{\pi CB}$. When the CB stage is biased in the mid-current region, the nonlinearity of β_{ac} is extremely low. As a result, α is also linear, and hence its contribution to the nonlinear behavior of the cascode is negligible compared to the contribution of the CE stage.

To support the qualitative discussions, the relative contributions of the CB and CE stage are compared and quantified in the following example. Use has been made of the method presented in Chapter 5 for determining the second-order nonlinear behavior of the CB stage. Consider a voltage driven cascode stage consisting of a CE and CB stage of type BC847 BJT, both biased at an I_{cQ} of 1 mA and U_{ceQ} of 5V. For an u_{be} of 10 mV, the linear output current delivered to a load resistance R_l of 5 kΩ is 384.3 μA. The second-harmonic component in the output current resulting from the CE stage is 36.8 μA and the second-order component generated by the CB stage is 37.3 nA. Only 0.1 % of the second-harmonic current is generated by the CB stage, which can safely be neglected.

The frequency response and the resulting envelope detection properties are the same as for the generic cascode.

4.2.2 FET-BJT cascode

The FET-BJT cascode consists of a CS stage loaded by a CB stage. Figure 4.4 shows the hybrid-π model.

It is found that the gate-drain capacitance seems to shunt the gate-source capacitance C_{gs} and has a value given by $C_{gd1\text{CS}} = C_{gd\text{CS}}(1 + g_{m1\text{CS}}/g_{m1\text{CB}})$. Usually, $g_{m1\text{CB}}$ is larger (e.g., $5\times \cdots 10\times$) than $g_{m1\text{CS}}$ and therefore $C_{gd1\text{CS}} \approx C_{gd\text{CS}}$. A FET-BJT cascode will therefore add virtually the same p_i to the amplifier design as a CS stage, see Table 4.1.

The CS stage introduces a zero at $z = g_{m1\text{CS}}/C_{gd\text{CS}}$. This zero will, in practical cases, most probably be located at a higher frequency than the input pole, but at a lower frequency than $\omega_{T\text{CB}}$. Frequencies between the input pole and the zero are attenuated with 20 dB/dec. A flat response is observed between the zero and $\omega_{T\text{CB}}$, and frequencies higher than $\omega_{T\text{CB}}$ are attenuated with 20 dB/dec. In the case of envelope detection due to EMI, the slopes will be twice

[2]When the same devices are used for the CE and CB stages, and the biasing of the devices is the same, this reduces to $C_{\mu 1\text{CE}} = 2C_{\mu\text{CE}}$.

as steep. Note that the frequency response and therefore the envelope detection due to EMI differs from the generic cascode.

4.2.3 BJT-FET cascode

Cascading a CE stage with a CG stage results in a BJT-FET cascode. Figure 4.3 also presents the hybrid-π model in this case. Care has to be taken to make sure that pole $p_o = |-\omega_{T\mathrm{CG}}|$ is located at a higher value than pole $|p_i|$, otherwise the hybrid-π model given in Figure 4.3 is not valid anymore.

The value of r_{oCa} is strongly dependent on the type of FET used. Some FETs, usually short channelled FETs, may show low values of μ_{CG} resulting in a relatively low value of r_{oCa}. Compared to the BJT-BJT cascode, a lower r_{oCa} can be expected.

Table 4.1 gives the equation for p_i. It is similar to the equation of p_i of the BJT-BJT cascode. However, usually it is found that $g_{m1\mathrm{CE}} > g_{m1\mathrm{CG}}$ which results in a value of $C_{\mu 1\mathrm{CE}}$ that may be considerably larger than in case of a BJT-BJT cascode. Pole $|p_i|$ is expected to be at a considerable lower frequency now, since $C_{\mu 1\mathrm{CE}}$ is in this case larger than in case of the BJT-BJT cascode.

It can be a tedious task to select or design a FET that satisfies the $\omega_{T\mathrm{CG}}$ demand and combines it with a high μ_{CG}. Since both BJTs and FETs are available, it is much easier to design a BJT-BJT cascode. On top of that, since the BJT-BJT cascode shows both a higher $|p_i|$ and a higher r_{oCa} ($\beta_{ac\mathrm{CB}}$ is usually larger than μ_{CG}), the BJT-BJT cascode can be regarded as superior and is therefore recommended. Envelope detection properties are therefore not discussed.

4.2.4 FET-FET cascode

Cascading a CS stage with a CG stage results in the FET-FET cascode. Its hybrid-π model is shown in Figure 4.4.

Pole p_i is formed by the capacitance of the CS stage and the source resistance (see Fig. 4.2 and Table 4.1). The total capacitance is the sum of $C_{gs\mathrm{CS}}$ and[3] $C_{gd\mathrm{CS}}(1 + g_{m\mathrm{CS}}/g_{m\mathrm{CG}})$. $C_{gd\mathrm{CS}}$ has the same order of magnitude as $C_{gs\mathrm{CS}}$ for FETs in saturation. Compared to an uncascoded CS stage with short-circuited output (current loading), the FET-FET cascode therefore shows a pole at a considerably lower frequency for the same circuit driving the gate. The frequency shift can have a value of approx. $(C_{gs\mathrm{CS}} + C_{gd\mathrm{CS}})/(C_{gs\mathrm{CS}} + 2C_{gd\mathrm{CS}})$ for equal devices and biasing.

The frequency response and the resulting envelope detection properties are the same as for the generic cascode.

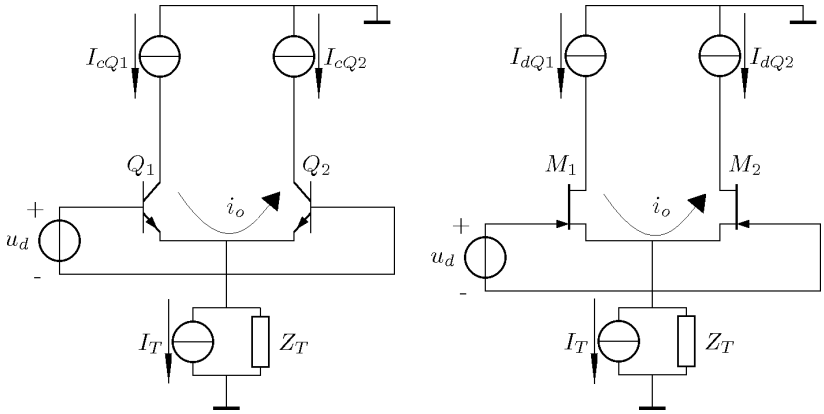
4.3 Traditional view on differential stages

In amplifier design, stages with an odd-symmetric input-output characteristic (e.g., a differential stage) is often used. Ideally, these stages do not show offset

[3] $C_{gd1\mathrm{CS}} = 2C_{gd\mathrm{CS}}$ in case of equal FETs and equal biasing.

or even-order nonlinearity and are therefore very useful.

Figure 4.5(a) shows a circuit diagram of the bipolar differential stage; replacing the BJTs by FETs results in the FET differential stage. Transistors Q_1 and Q_2 are biased at I_{cQ1} and I_{cQ2} respectively, and their sum I_T is sunk by the tail current source. Differential voltage u_d causes an output current i_o. In order



(a) BJT differential stage. (b) FET differential stage.

Figure 4.5: Differential stages with bias current sources. Circuitry for maintaining correct values of bias voltages and currents is omitted for clarity. Biasing is discussed in Subsection 4.6.2.

to derive simple equations, the Early effect is neglected and it is assumed that the BJTs are biased in the mid-current region. For the moment, the effect of the current source output impedance Z_T is disregarded.

In case of equal BJTs and biasing, the (large signal) output current, $i_o = i_{c1} - i_{c2}$, is given by

$$i_o = I_T \tanh\left(\frac{q u_d}{2 n_f k T}\right), \tag{4.5}$$

as can be found in many textbooks, e.g. [57]. Neglecting current flow in Z_T, I_T equals $I_{cQ1} + I_{cQ2}$, q is the electron charge, n_f is the forward emission factor, k is Boltzmann's constant, T is the absolute temperature in Kelvin, and u_d is the differential input voltage. The Taylor series expansion of the hyperbolic tangent function has no even-order terms (i.e., odd function). The transconductance is $g_m = \frac{1}{2}\frac{q}{n_f k T} I_T$, which equals the transconductance of Q_1 and Q_2.

For saturated FETs in the differential stage, the output current $i_o = i_{d1} - i_{d2}$ equals:

$$i_o = \begin{cases} -I_T & u_d < -\sqrt{\frac{I_T}{\beta_{\mathrm{FET}}}} \\ \frac{u_d}{2}\sqrt{2\beta_{\mathrm{FET}} I_T - \beta_{\mathrm{FET}}^2 u_d^2} & |u_d| \le \sqrt{\frac{I_T}{\beta_{\mathrm{FET}}}} \\ I_T & u_d > \sqrt{\frac{I_T}{\beta_{\mathrm{FET}}}}. \end{cases} \tag{4.6}$$

The drain currents of FET$_1$ (M_1) and FET$_2$ (M_2) are I_{dQ1} and I_{dQ2}, respectively. I_T is the sum of I_{dQ1} and I_{dQ2}, and β_{FET} is the transconductance factor. For values of $|u_d| \leq \sqrt{I_T/\beta_{\text{FET}}}$ Equation (4.6) is an odd function and the transconductance is found to equal $g_m = \frac{1}{2}\sqrt{2\beta_{\text{FET}} I_T}$. The FET differential stage is depicted in Fig. 4.5(b).

On basis of the discussion so far, it can be concluded that no even-order distortion nor EMI (envelope detection) will occur since there are no even-order terms in the series expansion of both BJT and FET differential stages. Differential stage modelling therefore traditionally concentrates on the linear and weakly nonlinear input to output transfer that is odd in order. Specifically, third-order nonlinearity has been paid close attention since it is an important source of distortion and intermodulation [117] in high-frequency, non-feedback amplifiers, and also in operational [118] and other negative-feedback amplifiers using differential input stages.

However, if the parameters and the biasing of the devices are slightly different (e.g., due to mismatch), the input-output characteristic is not perfectly odd symmetric and even-order nonlinearity will appear, resulting in even-order distortion and susceptibility to EMI. Depending on the amount of mismatch, second-harmonic and second-order intermodulation distortions may dominate the third-order effects, resulting in amplifiers with higher harmonic distortion than expected. This, and the resulting susceptibility to EMI, forces the designer to consider second-order nonlinearity during the design phase as well.

Second-order distortion [119] and EMI [120] in perfectly balanced differential stages (equal bias currents and perfect component matching) have been investigated for design purposes, especially for the special case that the input of one of the devices is grounded [121]. The occurrence of second harmonic distortion and EMI was explained by the mixing effect of fluctuations of the bias current and of the differential input voltage simultaneously [119][121]. The fluctuation of the bias current depends on the impedance of the current source connected to the emitter-emitter resp. source-source node, Z_T. The higher the impedance Z_T, the lower the second-order distortion and EMI susceptibility, and vice-versa. Usually, impedance Z_T is mainly capacitive, and second harmonic distortion and EMI, at low frequency are therefore negligible [119].

Although valuable knowledge has been published about second harmonic distortion and EMI susceptibility of negative-feedback amplifiers using differential input stages, e.g., [58][120] -[124][125], a method to evaluate the effects of imperfect biasing, transistor mismatch and of simultaneously applying a signal to both inputs of the differential stage thereby exciting its second-order nonlinearity, does not seem to be developed up to now. The simple equations given in this section cannot be used for that purpose. Deriving a method that takes these imperfections into account is very well possible, and this will be done in the next sections.

4.4 New differential stage model

An accurate analysis of both linear and second-order nonlinear response to small signals for a differential stage can be derived from linear superposition. Therefore, a generic model will be presented in this section. The input and output quantities may be voltages or currents, and are denoted by E.

The superposition model of the differential stage is given in Figure 4.6. It is based on the observation that the current source impedance, Z_T (see Figure 4.5), provides series feedback to the input of both transistors, i.e., the differential stage can be regarded as an amplifier with local negative feedback. The model is therefore valid under assumption that no clipping occurs, i.e., the transistors remain in the forward active region. Both differential and common-mode behavior can be analyzed with the model, but note that the common-mode feedback via Z_T is not explicitly shown in Fig. 4.6. Feedback is determined by various transfers in the model.

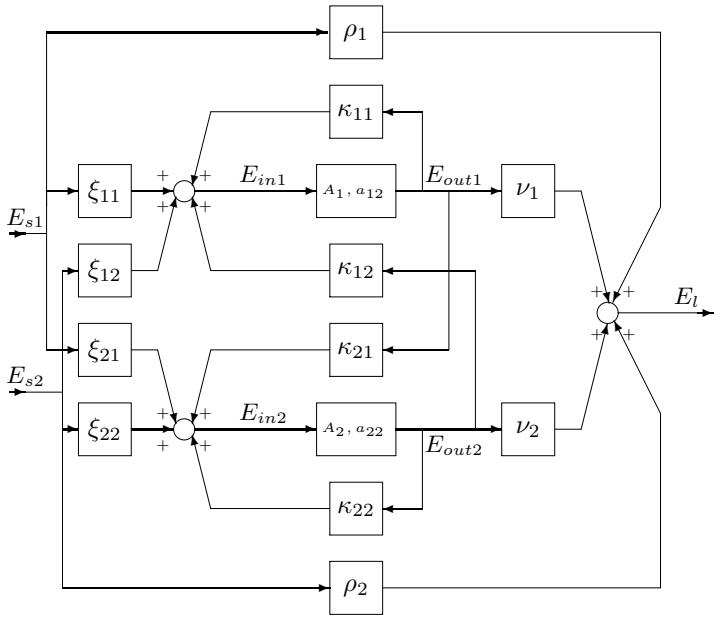


Figure 4.6: Superposition model of a differential stage

The differential stage is driven by two signal sources, E_{s1} and E_{s2}. The signal sources transfer their signals to the inputs of the differential stage, E_{in1} and E_{in2}, as shown in Fig. 4.6. The transfers from signal source E_{s1} to E_{in1} and E_{in2} are ξ_{11} and ξ_{21}, respectively, and the transfers from E_{s2} to E_{in1} and E_{in2}, ξ_{12} and ξ_{22}, respectively. The 'ξ_{xx}' transfers represent loading of the inputs. The first number in the subscript of a transfer refers to the corresponding transistor of the differential model shown in Figs. 4.5 and 4.8(a), the second number corresponds to an effect caused by the transistor with that number or the signal

source connected to it. For example, the transfer E_{s1} (u_s in Fig. 4.8(a)) to the input of transistor Q_1 is ξ_{11}, the transfer E_{s2} (i_s in Fig. 4.8(a)) to transistor Q_2 is ξ_{22}, the transfer E_{s2} to Q_1 is ξ_{12}, the transfer from Q_2 to Q_1 is κ_{12}, etc.[4]

A fraction of E_{out1} is fed-back to E_{in1} via κ_{11} and to E_{in2} via κ_{21}. Similarly, a fraction of E_{out2} is fed-back to E_{in1} via κ_{12} and to E_{in2} via[5] κ_{22}. Output quantities E_{out1} and E_{out2} are equal to A_1E_{in1} and A_2E_{in2}, where A_1 and A_2 are the linear transconductances of Q_1 and Q_2, respectively. The second-order transconductance is represented by a_{12} (Q_1) and a_{22} (Q_2). Transfers ν_1 and ν_2 are the output transfers from E_{out1} and E_{out2} to the output signal E_l (output loading) and transfers ρ_1 and ρ_2 are the direct transfers from E_{s1} and E_{s2} to E_l, respectively. The feedforward transfers ρ_1 and ρ_2 are usually so small that they can be neglected.

Each transfer is determined under the condition that all other signal sources are zero, e.g., $\xi_{11} = \frac{E_{in1}}{E_{s1}}\Big|_{E_{out1}=E_{out1}=E_{s2}=0}$, $\kappa_{22} = \frac{E_{in2}}{E_{out2}}\Big|_{E_{out1}=E_{s1}=E_{s2}=0}$, etc. The superposition of all transfers then gives the behavior of the differential stage. An example is presented in Subsection 4.4.1. Note that all transfers are determined by the signal source impedances, by Z_T and the hybrid-π parameters of both transistors. Since the hybrid-π parameters depend on the biasing of the device, choosing a different bias point will alter both the linear and second-order behaviors.

It follows from Figure 4.6 that the transfers from the signal sources to the inputs of the active devices is given by

$$E_{in1}(s) = \frac{E_{s1}(s)\left[\xi_{11}(s)(1-A_2\kappa_{22}(s))+\xi_{21}A_2\kappa_{12}(s)\right]}{1-\left[A_1\kappa_{11}(s)+A_2\kappa_{22}(s)+A_1A_2(\kappa_{12}(s)\kappa_{21}(s)-\kappa_{11}(s)\kappa_{22}(s))\right]} + \frac{E_{s2}(s)\left[\xi_{12}(s)(1-A_2\kappa_{22}(s))+\xi_{22}(s)A_2\kappa_{12}(s)\right]}{1-\left[A_1\kappa_{11}(s)+A_2\kappa_{22}(s)+A_1A_2(\kappa_{12}(s)\kappa_{21}(s)-\kappa_{11}(s)\kappa_{22}(s))\right]} \tag{4.7}$$

and

$$E_{in2}(s) = \frac{E_{s1}(s)\left[\xi_{21}(s)(1-A_1\kappa_{11}(s))+\xi_{11}(s)A_1\kappa_{21}(s)\right]}{1-\left[A_1\kappa_{11}(s)+A_2\kappa_{22}(s)+A_1A_2(\kappa_{12}(s)\kappa_{21}(s)-\kappa_{11}(s)\kappa_{22}(s))\right]} + \frac{E_{s2}(s)\left[\xi_{22}(s)(1-A_1\kappa_{11}(s))+\xi_{12}(s)A_1\kappa_{21}(s)\right]}{1-\left[A_1\kappa_{11}(s)+A_2\kappa_{22}(s)+A_1A_2(\kappa_{12}(s)\kappa_{21}(s)-\kappa_{11}(s)\kappa_{22}(s))\right]}, \tag{4.8}$$

where s is the Laplace variable.

The linear output signals are now $E_{out1}(s) = E_{in1}(s)A_1$ and $E_{out2}(s) = E_{in2}(s)A_2$, and the signal in the load is

$$E_l(s) = E_{s1}(s)\rho_1(s) + E_{out1}(s)\nu_1(s) + E_{s2}(s)\rho_2(s) + E_{out2}(s)\nu_2(s). \tag{4.9}$$

[4] In case of the FET differential stage, Q_1 and Q_2 should be replaced by M_1 and M_2, respectively.

[5] In this work, feedback in amplifiers is usually denoted by β. To prevent confusion with β, feedback action is denoted by κ in the superposition model of the differential stage.

The effects of single-ended loading, (i.e., taking the output signal of one device only; $\nu_1(s) \neq \nu_2(s)$), and differential loading (i.e., taking the difference of the output signal of both devices; $\nu_1(s) = \nu_2(s)$), can be made explicit in this way of modelling.

The second-order nonlinear outputs are given by $E_{out1} = mE_{in1}^2(s)a_{12}$ and $E_{out2} = mE_{in2}^2(s)a_{22}$. Coefficient m equals 0.5 for second-harmonic distortion and equals the modulation depth (AM) in case of EMI. Using Figure 4.6 the second-order, weakly nonlinear response can be derived for both FET and BJT differential stages. From Figure 4.6, it can be shown that

$$\begin{aligned} E_{l,\omega_l} = m & \frac{1}{1-(A_1\kappa_{11,\omega_l} + A_2\kappa_{22,\omega_l} + A_1A_2(\kappa_{12,\omega_l}\kappa_{21,\omega_l} - \kappa_{11,\omega_l}\kappa_{22,\omega_l}))} \times \\ & \left[[E_{in1}(s)]^2 a_{12}\nu_{1,\omega_l} \left(1 - A_2\left(\kappa_{22,\omega_l} - \kappa_{21,\omega_l}\frac{\nu_{2,\omega_l}}{\nu_{1,\omega_l}}\right)\right) \right. \\ & \left. + [E_{in2}(s)]^2 a_{22}\nu_{2,\omega_l} \left(1 - A_1\left(\kappa_{11,\omega_l} - \kappa_{12,\omega_l}\frac{\nu_{1,\omega_l}}{\nu_{2,\omega_l}}\right)\right)\right] \end{aligned} \tag{4.10}$$

for the FET differential pair holds[6]. The subscript ω_l is used to distinguish second-order responses from the input frequency, ω_c. In case of second-harmonic distortion, ω_l is twice the input frequency. In case of EMI, it is the low frequency variation of the high frequency envelope.

For matched transistors, biasing, signal sources and loading impedances, $a_{12} = a_{22}$, $A_1 = A_2$, $\kappa_{11,\omega_l} = \kappa_{12,\omega_l} = \kappa_{21,\omega_l} = \kappa_{22,\omega_l}$, $\nu_{1,\omega_l} = \nu_{2,\omega_l}$, and $E_{in1} = -E_{in2}$. Equation (4.10) shows that E_{l,ω_l} is zero for matched devices, as expected. In the case of mismatched devices, biasing, signal sources or loading, the E_{in1} and E_{in2} terms between the brackets do not cancel anymore, and second-harmonic distortion and EMI susceptibility will occur.

The voltage-controlled current source at the input of the BJT hybrid-π model complicates the determination of the total second-order behavior of the differential stage. Each current source also has a transfer to E_{in1} resp. E_{in2}. These transfers are: $\gamma_{11} = E_{in1}/i_1$, $\gamma_{21} = E_{in2}/i_1$, $\gamma_{12} = E_{in1}/i_2$ and, $\gamma_{22} = E_{in2}/i_2$. Here, $i_1 = b_{12}E_{in1}^2$ and $i_2 = b_{22}E_{in2}^2$ are the currents of the voltage-controlled current sources at the inputs of Q_1 and Q_2 of the differential stage, respectively. The coefficients b_{12} and b_{22} represent the nonlinearity of the input impedance of the BJT, i.e., they represent the effect of $g_{\pi 2} = g_{m2}/\beta_{ac}$. For reasons of simplicity, the $\gamma_{x,x}$ transfers, which are only relevant for the second-order response, are not drawn in Figure 4.6.

For the second-order behavior of the BJT differential stage, it can be shown

[6]Under the assumption that the nonlinearity of the FET output conductance is negligible, e.g., due to cascoding.

that

$$E_{l,\omega_l} = m\frac{1}{1-(A_1\kappa_{11,\omega_l}+A_2\kappa_{22,\omega_l}+A_1A_2(\kappa_{12,\omega_l}\kappa_{21,\omega_l}-\kappa_{11,\omega_l}\kappa_{22,\omega_l}))}\times$$
$$\Bigg\{[E_{in1}(s)]^2\nu_{1,\omega_l}\Bigg[a_{12}\left(1-A_2\left(\kappa_{22,\omega_l}-\kappa_{21,\omega_l}\frac{\nu_{2,\omega_l}}{\nu_{1,\omega_l}}\right)\right)+$$
$$b_{12}\Bigg(A_1\gamma_{11,\omega_l}+A_2\gamma_{21,\omega_l}\frac{\nu_{2,\omega_l}}{\nu_{1,\omega_l}}+$$
$$A_1A_2\left(\gamma_{11,\omega_l}\left(\frac{\nu_{2,\omega_l}}{\nu_{1,\omega_l}}\kappa_{21,\omega_l}-\kappa_{22,\omega_l}\right)+\gamma_{21,\omega_l}\left(\kappa_{12,\omega_l}-\frac{\nu_{2,\omega_l}}{\nu_{1,\omega_l}}\kappa_{11,\omega_l}\right)\right)\Bigg)\Bigg]+$$
$$[E_{in2}(s)]^2\nu_{2,\omega_l}\Bigg[a_{22}\left(1-A_1\left(\kappa_{11,\omega_l}-\kappa_{12,\omega_l}\frac{\nu_{1,\omega_l}}{\nu_{2,\omega_l}}\right)\right)+$$
$$b_{22}\Bigg(A_1\gamma_{12,\omega_l}\frac{\nu_{1,\omega_l}}{\nu_{2,\omega_l}}+A_2\gamma_{22,\omega_l}+$$
$$A_1A_2\left(\gamma_{12,\omega_l}\left(\kappa_{21,\omega_l}-\kappa_{22,\omega_l}\frac{\nu_{1,\omega_l}}{\nu_{2,\omega_l}}\right)+\gamma_{22,\omega_l}\left(\kappa_{12,\omega_l}\frac{\nu_{1,\omega_l}}{\nu_{2,\omega_l}}-\kappa_{11,\omega_l}\right)\right)\Bigg)\Bigg]\Bigg\}. \tag{4.11}$$

If b_{12} and b_{22} are zero, (4.11) reduces to (4.10), as expected.

Equations (4.10) and (4.11) show that E_{l,ω_l} can become zero in the case of ideal balancing: when $E_{in1} = -E_{in2}$. The worst case situation occurs when either ν_{1,ω_l} or ν_{2,ω_l} is zero. The second-order nonlinear behavior is then comparable to that of an unbalanced device having a second-order nonlinear term of $a_2/2$. However, this is an extreme situation. In practical cases it can be expected to be smaller, because even in case of single-ended loading, neither ν_{1,ω_l} nor ν_{2,ω_l} will be zero. The model and equations presented here are valid generally.

When E_{s2} is assumed to be zero and transistor Q_1 has a load of 0 Ω, the equations reduce to a 'common-collector (CC)-common-base (CB)' stage, also sometimes called the non-inverting version of the CE-stage, or its FET equivalent. It will yield the same results as presented in the literature in [119][121]. It is investigated in more detail in appendix C.1.

The following discussion is based on the BJT differential stage, but it also holds for the FET differential stage. When C_μ is neutralized, complete isolation between the input and output of the differential stage may exist (unilaterality). In that case, the superposition model of Figure 4.6 reduces to the model in Figure 4.7 (in which it is also assumed that both ρ_1 and ρ_2 are negligible)[7]. Because now there is no signal path from collector to base, the only feedback action possible is that of the sum of the emitter currents to both bases (see Fig. 4.5), i.e., (common-mode) feedback due to Z_T. This feedback action to input 1 is represented by κ_1 and the feedback action to input 2 is represented by κ_2. It is found that $\kappa_1 = \kappa_{11} = \kappa_{12}$ and $\kappa_2 = \kappa_{21} = \kappa_{22}$.

[7]When there is finite isolation between the input and output of the differential stage Fig. 4.6 has to be used. However, *when the effect of C_μ is negligible, e.g., at relatively low frequencies*, this model and the following equations apply.

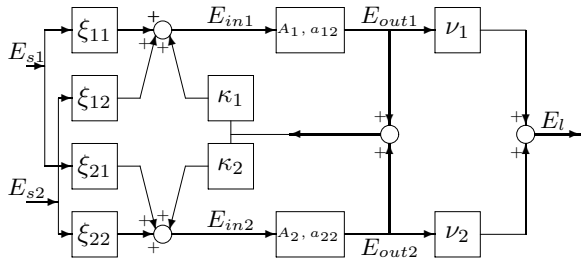


Figure 4.7: Simplified differential stage superposition model. Direct transfers from E_{s1} and E_{s2} to the load are assumed to be negligible, and are therefore not shown.

From Fig. 4.7 follows

$$E_{in1}(s) = \frac{E_{s1}(s)\left[\xi_{11}(s)(1 - A_2\kappa_2(s)) + \xi_{21}A_2\kappa_1(s)\right]}{1 - \left[A_1\kappa_1(s) + A_2\kappa_2(s)\right]} + \frac{E_{s2}(s)\left[\xi_{12}(s)(1 - A_2\kappa_2(s)) + \xi_{22}(s)A_2\kappa_1(s)\right]}{1 - \left[A_1\kappa_1(s) + A_2\kappa_2(s)\right]} \tag{4.12}$$

$$E_{in2}(s) = \frac{E_{s1}(s)\left[\xi_{21}(s)(1 - A_1\kappa_1(s)) + \xi_{11}(s)A_1\kappa_2(s)\right]}{1 - \left[A_1\kappa_1(s) + A_2\kappa_2(s)\right]} + \frac{E_{s2}(s)\left[\xi_{22}(s)(1 - A_1\kappa_1(s)) + \xi_{12}(s)A_1\kappa_2(s)\right]}{1 - \left[A_1\kappa_1(s) + A_2\kappa_2(s)\right]} \tag{4.13}$$

and

$$\begin{aligned} E_{l,\omega_l} = {} & m\frac{1}{1 - (A_1\kappa_{1,\omega_l} + A_2\kappa_{2,\omega_l})} \times \\ & \left[[E_{in1}(s)]^2 a_{12}\nu_{1,\omega_l}\left(1 - A_2\kappa_{2,\omega_l}\left(1 - \frac{\nu_{2,\omega_l}}{\nu_{1,\omega_l}}\right)\right)\right. \\ & \left. + [E_{in2}(s)]^2 a_{22}\nu_{2,\omega_l}\left(1 - A_1\kappa_{1,\omega_l}\left(1 - \frac{\nu_{1,\omega_l}}{\nu_{2,\omega_l}}\right)\right)\right]. \end{aligned} \tag{4.14}$$

Under these assumptions hold $\gamma_c = \gamma_{12} = \gamma_{21}$

$$E_{l,\omega_l} = m\frac{1}{1-(A_1\kappa_{1,\omega_l}+A_2\kappa_{2,\omega_l})}\times$$
$$\Bigg\{[E_{in1}(s)]^2\nu_{1,\omega_l}\Bigg[a_{12}\left(1-A_2\kappa_{2,\omega_l}\left(1-\frac{\nu_{2,\omega_l}}{\nu_{1,\omega_l}}\right)\right)+b_{12}\Bigg(A_1\gamma_{11,\omega_l}+$$
$$A_2\gamma_{c,\omega_l}\frac{\nu_{2,\omega_l}}{\nu_{1,\omega_l}}+A_1A_2\left(\gamma_{11,\omega_l}\kappa_{2,\omega_l}\left(\frac{\nu_{2,\omega_l}}{\nu_{1,\omega_l}}-1\right)+\gamma_{c,\omega_l}\kappa_{1,\omega_l}\left(1-\frac{\nu_{2,\omega_l}}{\nu_{1,\omega_l}}\right)\right)\Bigg)\Bigg]+$$
$$[E_{in2}(s)]^2\nu_{2,\omega_l}\Bigg[a_{22}\left(1-A_1\kappa_{1,\omega_l}\left(1-\frac{\nu_{1,\omega_l}}{\nu_{2,\omega_l}}\right)\right)+b_{22}\Bigg(A_1\gamma_{c,\omega_l}\frac{\nu_{1,\omega_l}}{\nu_{2,\omega_l}}+$$
$$A_2\gamma_{22,\omega_l}+A_1A_2\left(\gamma_{c,\omega_l}\kappa_{2,\omega_l}\left(1-\frac{\nu_{1,\omega_l}}{\nu_{2,\omega_l}}\right)+\gamma_{22,\omega_l}\kappa_{1,\omega_l}\left(\frac{\nu_{1,\omega_l}}{\nu_{2,\omega_l}}-1\right)\right)\Bigg)\Bigg]\Bigg\}. \tag{4.15}$$

All expressions given for E_{l,ω_l} show that it consists of contributions of E_{in1}^2 and E_{in2}^2 that are frequency dependent (ω_c). Both E_{in1}^2 and E_{in2}^2 are multiplied by second-order nonlinear terms that have opposite signs. The second-order nonlinear terms consist of the initial nonlinearity of the active part (a_2, b_2), multiplied by a term given by the ratio of the loop gains ($A_x\kappa_x$) weighted by ν_x. In case of second-harmonic distortion, they are frequency dependent ($\omega_l = 2\omega_c$); in case of EMI, the second-order nonlinear terms are (virtually) frequency independent (ω_l). Since this work concentrates on EMI, it is therefore chosen to use E_{l,ω_l} instead of $E_l(\omega_l)$ (or $E_{l,\omega_l}(\omega_c)$ and $E_l(\omega_l,\omega_c)$, respectively).

4.4.1 Design considerations regarding EMI

This section mainly concentrates on EMI design considerations. It can, however, be reasonably assumed that measures taken for low EMI performance are beneficial for low second-harmonic distortion also.

As Equations (4.10) and (4.11) show, the second-order output current is determined by $E_{in1}(s)$, $E_{in2}(s)$ and by several transfers at frequency ω_l. In the case of EMI a simplification can be made. Although EMI is usually caused by high-frequency effects, its results occur at low frequency: DC shifts and detection of low-frequency envelope variations [10]. It is reasonable to assume that the transfers at ω_l in this case will not deviate much from their DC values. A good approximation of the EMI susceptibility can therefore be determined by using DC values of the linear transfers in equations (4.10) and (4.11). Frequency dependency of E_{l,ω_l} is then determined by $E_{in1}(s)$ and $E_{in2}(s)$. E_{l,ω_l} may have a maximal value at a frequency ω_{max}.

Frequency ω_{max} can be determined by considering that $E_{in1}(s)$ and $E_{in2}(s)$ have opposite signs, but are equal in magnitude in the ideal, balanced case. Their sum is zero and the common-mode rejection is infinite. Due to imbalance caused by transistor mismatch, currents and impedances, $E_{in1}(s)$ and $E_{in2}(s)$ start to differ. The common-mode component (CM) at a specific frequency is defined as $CM(s) = (E_{in1}(s) + E_{in2}(s))/2$ [57]. EMI susceptibility is maximal

when CM(s) reaches its maximum. This effect may be compared to common-mode to differential-mode conversion. The CM(s) of $E_{in1}(s)$ and $E_{in2}(s)$ found from Figures 4.6 and 4.7 are given by

$$\begin{aligned} CM(s) =& \frac{1}{2}\frac{1}{1-(A_1\kappa_{11}(s)+A_2\kappa_{22}(s)+A_1A_2(\kappa_{12}(s)\kappa_{21}(s)-\kappa_{11}(s)\kappa_{22}(s)))} \\ & \Big(E_{s1}(s)\cdot\Big\{\xi_{11}(s)\cdot[1-(A_2\kappa_{22}(s)-A_1\kappa_{21}(s))]+ \\ & \xi_{21}(s)\cdot[1-(A_1\kappa_{11}(s)-A_2\kappa_{12}(s))]\Big\} \\ & + E_{s2}(s)\cdot\Big\{\xi_{12}(s)\cdot[1-(A_2\kappa_{22}(s)-A_1\kappa_{21}(s))]+ \\ & \xi_{22}(s)\cdot[1-(A_1\kappa_{11}(s)-A_2\kappa_{12}(s))]\Big\}\Big) \end{aligned} \tag{4.16}$$

and

$$\begin{aligned} CM(s) = & \frac{1}{2}\frac{1}{1-(A_1\kappa_1(s)+A_2\kappa_2(s))}\times \\ & \Big(E_{s1}(s)\cdot(\xi_{11}(s)[1-(A_2-A_1)\kappa_2(s)]+\xi_{21}(s)[1-(A_1-A_2)\kappa_1(s)]) \\ & + E_{s2}(s)\cdot(\xi_{12}(s)[1-(A_2-A_1)\kappa_2(s)]+\xi_{22}(s)[1-(A_1-A_2)\kappa_1(s)])\Big), \end{aligned} \tag{4.17}$$

respectively.

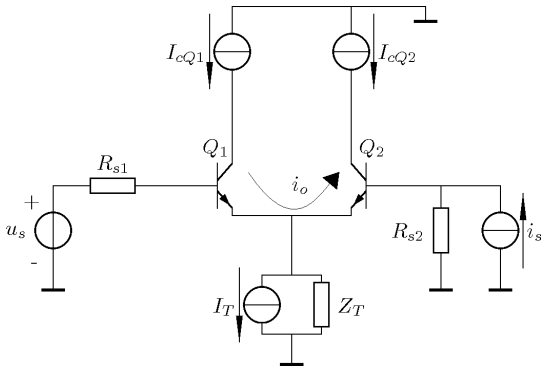
For example, consider the differential stage in Fig. 4.8(a), and its small-signal representation in Fig. 4.8(b). Both Q_1 and Q_2 have their own signal source and signal source impedance, as may occur when it is used in a negative-feedback amplifier. Signal source i_s may, for instance, be the amplifier's output signal that is fed back to the input by a feedback network represented by equivalent resistance R_{s2}. In this example, the current source output impedance Z_T consists of a resistance of 10 MΩ shunted by a capacitance C_T of 10 pF.

Transistor Q_1 is driven by a voltage source, $\hat{u}_s = 10$mV, with series source resistance $R_{s1} = 1$ kΩ and transistor Q_2 by a current source $\hat{i}_s = 100$ nA with parallel source resistance $R_{s2} = 10$ kΩ. These relatively low signal magnitudes are chosen to assure the validity of the hybrid-π models (see Chapter 3).

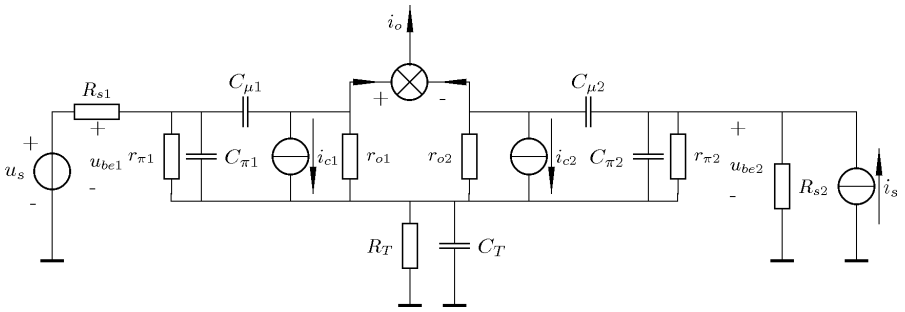
The differential stage delivers output current $i_o = i_{c1} - i_{c2}$. Currents i_{c1} and i_{c2} are subtracted by an ideal floating subtractor with an impedance of 0 Ω. Figure 4.7 is used to analyze the linear and second-order nonlinear behavior of the differential stage.

Both transistors are of type BC847. The linear hybrid-π parameters were determined using the SPICE model[8] provided by NXP [126] the second-order

[8] version of 2007 (which is equal to the version of 2012).



(a) Bipolar differential stage with two signal sources. Biasing is only partly shown. Circuitry for maintaining correct values of bias voltages and currents is omitted for clarity.



(b) Small-signal model of the differential stage of Fig. 4.8(a). The subtraction point is floating and has an impedance of 0 Ω.

Figure 4.8: BJT differential stage with signal sources and its hybrid-π representation.

nonlinear parameters followed from the equations given in Chapter 3. The linear and second-order parameters are listed in Table 4.2.

Table 4.2: BC847 [126] hybrid-π parameters I_{cQ1}= I_{cQ2}= 0.5 mA, U_{ceQ1}= U_{ceQ1}= 4 V

r_B = 8.8 Ω	g_{m1}= 19 mA/V
r_π = 26.8 kΩ	g_{m2}= 376 mA/V^2
C_π = 28.6 pF	$g_{\pi 2}$= 731.7 μV^2
C_μ = 1.54 pF	$C_{\pi 2}$= 320 pF/V
r_o = 103 kΩ	f_T= 102 MHz

Table 4.3 presents an overview of the transfers that follow from Fig. 4.8(b). The DC values of $\xi_{11}(s)$, $\kappa_2(s)$, etc., are indicated by an extra '0' in the subscript (e.g., ξ_{110} and κ_{20} are the DC transfers of $\xi_{11}(s)$ and $\kappa_2(s)$, respectively.). Each transfer shows the same poles, and has either one or two zeros. The poles and zeros are estimated from Fig. 4.8(b). Comparable transfers may be found for other source and load values. However, the expressions for the poles and zeros may change. Note that r_B is neglected in these approximations, due to its low value.

Equation (4.17) can written in a slightly different form

$$\begin{aligned} CM(s) =& \frac{1}{2}\frac{1}{1-(A_1\kappa_1(s)+A_2\kappa_2(s))}\times \\ & \Big(E_{s1}(s)\cdot(\xi_{11}(s)+\xi_{21}(s))+E_{s2}(s)\cdot(\xi_{12}(s)+\xi_{22}(s))\Big), \end{aligned} \tag{4.18}$$

that is valid under the assumption that the $(A_x - A_y)\kappa_z$ terms are of minor influence. This is a valid assumption, since for practical situations A_1 and A_2 will not differ much in case of matched transistors. If A_1 and A_2 differ too much, (4.17) should be used.

Equation (4.18) is comparable to the common-mode gain multiplied by the input signals. It shows the familiar response of the common-mode gain versus frequency: at low frequency CM(s) is small, for frequencies higher than a zero it increases with 6 dB/oct., and for frequencies higher than the bandwidth ω_0 it decreases with 6 db/oct. (e.g., [57]). It is found that the complicated expression for the zeros due to the ξ_{xx} terms can be approximated by one zero (z_T) determined by the time constant of the current source impedance.

The frequency at which the CM(s) is maximal, ω_{max}, is determined by differentiating Equation (4.17) or (4.18) with respect to ω and equating this result to zero. This yields an accurate, equation with many terms that does not give much insight. Therefore, an alternative method is used that is only slightly less accurate, but gives much more insight.

The value of CM starts to increase due to z_T until, due to the poles, it starts to decrease. The -3 dB frequency of this transfer gives a reasonably accurate approximation of ω_{max}. The -3 dB frequency, ω_0, follows from the denominator of (4.18) and is $\omega_0^n = \prod_{i=1}^{n} |p_i|[1-(A_1\kappa_{10}+A_2\kappa_{20})]$. For determining ω_0, only dominant poles should be multiplied with the loop gain [127][3], with $[1-(A_1\kappa_{10}+A_2\kappa_{20})]$ being the loop gain of the differential stage. Whether a pole is reckoned in the dominant group or not depends on the particular situation. Generally, we will refer to a pole of the loop transfer function as dominant if it can be located in the bandwidth determining group [2]. Term ω_0^n thus equals the loop gain poles product of the differential stage.

Frequency ω_0 is in this case determined by $\omega_0 = \sqrt{[1-(A_1\kappa_{10}+A_2\kappa_{20})]p_1p_3}$. Pole p_2 does not affect ω_0, since its effect is counteracted by $z_{\kappa 1}$ (when determining the root locus, it is found that p_2 ends in $z_{\kappa 1}$).

Equations (4.17) or (4.18) can now be evaluated at both $\omega_0 \approx \omega_{max}$ and at $\omega = 0$. Whichever result is the largest dominates the EMI susceptibility. For

Table 4.3: Overview of the transfers, poles and zeros of Fig. 4.8(b). The extra '0' in the subscript of the transfers stands for their DC values.

Transfer	zero [rad/s]	zero [rad/s]
$\xi_{110} = \frac{r_{\pi1}}{r_{\pi1}+R_{s1}+R_T//(R_{s2}+r_{\pi2})}$	$z_{\xi111} \approx -\frac{1}{(r_{\pi2}//R_T)(C_{\pi2}+C_T)}$	$z_{\xi112} \approx -\frac{1}{R_{s2}\frac{C_{\pi2}C_T}{C_{\pi2}+C_T}}$
$\xi_{210} = -\frac{r_{\pi2}R_T}{R_{s2}+r_{\pi2}+R_T} \cdot \frac{1}{r_{\pi1}+R_{s1}+R_T//(R_{s2}+r_{\pi2})}$	$z_{\xi21} \approx -\frac{1}{r_{\pi1}C_{\pi1}}$	-
$\xi_{120} = -\frac{r_{\pi1}R_T}{R_{s1}+r_{\pi1}+R_T} \cdot \frac{R_{s2}}{r_{\pi2}+R_{s2}+R_T//(R_{s1}+r_{\pi1})}$	$z_{\xi12} \approx -\frac{1}{r_{\pi2}C_{\pi2}}$	-
$\xi_{220} = \frac{R_{s2}r_{\pi2}}{r_{\pi2}+R_{s2}+R_T//(R_{s1}+r_{\pi1})}$	$z_{\xi221} \approx -\frac{1}{(r_{\pi1}//R_T)(C_{\pi1}+C_T)}$	$z_{\xi222} \approx -\frac{1}{R_{s1}\frac{C_{\pi1}C_T}{C_{\pi1}+C_T}}$
$\kappa_{10} = -r_{\pi1}\frac{R_T//(R_{s2}+r_{\pi2})}{R_{s1}+r_{\pi1}+R_T//(R_{s2}+r_{\pi2})}$	$z_{\kappa1} \approx -\frac{1}{(R_{s2}//r_{\pi2})C_{\pi2}}$	-
$\kappa_{20} = -r_{\pi2}\frac{R_T//(R_{s1}+r_{\pi1})}{R_{s2}+r_{\pi2}+R_T//(R_{s1}+r_{\pi1})}$	$z_{\kappa2} \approx -\frac{1}{(R_{s1}//r_{\pi1})C_{\pi1}}$	-
$\gamma_{110} = -r_{\pi1}//[R_{s1}+(R_T//(R_{s2}+r_{\pi2}))]$	$z_{\gamma111} \approx -\frac{1}{[(R_{s1}+R_{s2})//r_{\pi2}]C_{\pi2}}$	$z_{\gamma112} \approx -\frac{1}{(R_{s1}//R_{s2}//R_T)C_T}$
$\gamma_{210} = -\frac{r_{\pi2}R_T}{R_{s2}+R_T+r_{\pi2}} \cdot \frac{r_{\pi1}}{R_{s1}+r_{\pi1}+R_T//(R_{s2}+r_{\pi2})}$	$z_{\gamma211} \approx -\frac{1}{R_{s1}C_{\mu1}}$	-
$\gamma_{120} = -\frac{r_{\pi1}R_T}{R_{s1}+R_T+r_{\pi1}} \cdot \frac{r_{\pi2}}{R_{s2}+r_{\pi2}+R_T//(R_{s1}+r_{\pi1})}$	$z_{\gamma121} \approx -\frac{1}{R_{s2}C_{\mu2}}$	-
$\gamma_{220} = -r_{\pi2}//[R_{s2}+(R_T//(R_{s1}+r_{\pi1}))]$	$z_{\gamma221} \approx -\frac{1}{(r_{\pi1}//R_{s2}//R_T)(C_{\pi1}+C_T)}$	$z_{\gamma222} \approx -\frac{1}{R_{s1}\frac{C_{\pi1}C_T}{C_{\pi1}+C_T}}$
pole [rad/s]	pole [rad/s]	pole [rad/s]
$p_1 \approx -\frac{1}{(r_{\pi1}//r_{\pi2}//R_T)(C_{\pi1}+C_{\pi2}+C_T)}$	$p_2 \approx -\frac{1}{R_{s2}\frac{C_{\pi2}(C_{\pi1}+C_T)}{C_{\pi1}+C_{\pi2}+C_T}}$	$p_3 \approx -\frac{1}{R_{s1}\frac{C_{\pi1}C_T}{C_{\pi1}+C_T}}$

matched devices and biasing, it will be found that the maximum susceptibility is at ω_{max}. When biasing and/or the devices are not identical, it may be found that max. susceptibility occurs at lower frequencies than ω_{max}. For convenience, the DC value of CM(s) and z_T are given in (4.19)

$$CM(0) = \frac{1}{2}\frac{1}{1-(A_1\kappa_{10}+A_2\kappa_{20})}\Big(E_{s1}\cdot(\xi_{110}+\xi_{210}) + E_{s2}\cdot(\xi_{120}+\xi_{220})\Big) \quad (4.19)$$
$$z_T = -\frac{1}{R_T C_T}.$$

As stated earlier, the extra '0' in the subscript represents the DC value of the transfer (e.g., ξ_{110} and κ_{20} are the DC values of $\xi_{11}(s)$ and $\kappa_2(s)$, respectively).

In general, feedback theory encourages the designer to make the loop gain as large as possible. Here however, both E_{in1} and E_{in2} are determined by a ratio in which $A_x\kappa_x$ terms appear in both the numerator and the denominator (see, e.g., equations (4.12) and (4.13)). For low EMI susceptibility, $A_1\kappa_1(s)$ and $A_2\kappa_2(s)$ should therefore be as equal as possible to realize $E_{in1} \approx E_{in2}$. To minimize the influence of Z_T on $\kappa_1(s)$ and $\kappa_2(s)$, it is recommended that Z_T is an order of magnitude larger than the source and input impedances of the active devices.

Ideally, the poles of the differential stage are determined only by the time constants of the active devices. The capacitance of the current source impedance I_T, however, also contributes to the pole frequencies (see Table 4.3). A large capacitance value compared to the other capacitances, shifts $|p_1|$ and $|p_3|$ to a lower frequency. The capacitance also determines zero z_T, which shifts to a lower frequency. The effect is as follows: frequency ω_0 will shift to a lower frequency by a factor given by $\sqrt{\Delta_1 p_1 \Delta_3 p_3}$ (as follows from the expression for ω_0), with Δ_1 and Δ_3 being the shift of p_1 and p_3, respectively. This results in a considerably lower shift than that of the open loop poles $|p_1|$ and $|p_3|$ and zero z_T. As a result the magnitude of CM(s) can increase over more octaves before it will decrease again. Maximum EMI susceptibility will thus occur at a lower frequency and its magnitude will be larger. This effect is quite important since an extra octave of increase in CM(s) may increase EMI susceptibility by 12 dB.

A straightforward conclusion is that the capacitance of the current source should be as low as possible (at least by a factor of 10 to 20) than the input capacitances of the active devices for low EMI behavior in the differential stage. Figure 4.9 shows CM(s) as a function of frequency for the circuit of Fig. 4.8(b) with C_T = 10 pF (solid line) and C_T= 1 pF (dotted line). It can be seen that with C_T= 1 pF, zero $|z_{T,1pF}|$ is located at a higher frequency than $|z_{T,10pF}|$, when C_T= 10 pF. The maximal value of CM(s) is lower, and shifted to a higher frequency $f_{0,1pF}$, with $f_0 = \omega_0/(2\pi)$.

Large differences between R_{s1} and R_{s2} result in differences in the zero locations of the various ξ transfers. It may happen that at frequencies higher than ω_0 the slope of $CM(s)$ is altered and, hence, the slope of the EMI susceptibility. When the differential stage is being used in a negative-feedback amplifier, the designer can make R_{s1} and R_{s2} as equal as possible by carefully designing the feedback network. It should, however, be noted that the feedback action itself will also affect CM(s) and EMI behavior (see Chapter 5).

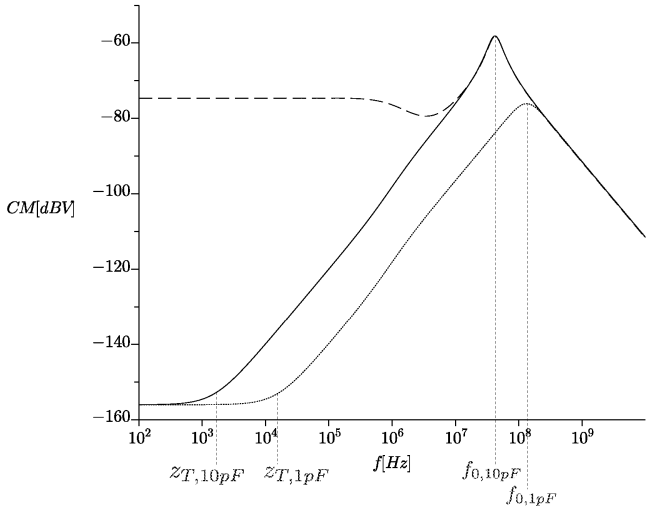
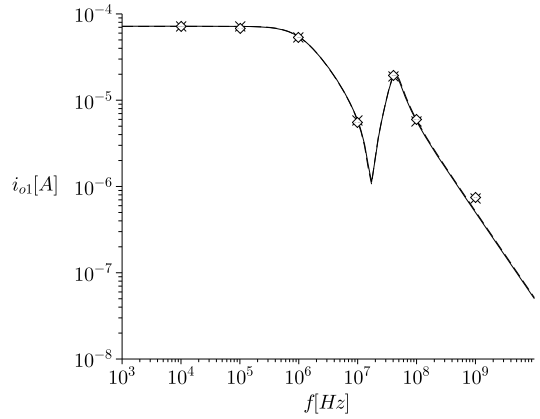


Figure 4.9: Solid line and dotted line show CM for the balanced case with C_T = 10 pF and C_T = 1 pF, respectively. The dashed line shows CM in case of 10 % current imbalance and C_T =10pF.

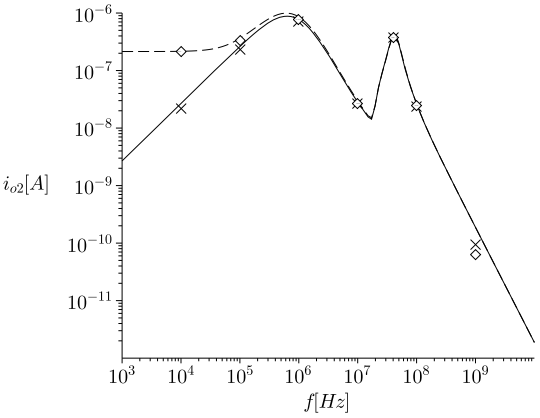
The effect of current and device mismatches manifests itself in unequal DC values of the transfers. The poles and zeros will typically not differ much for small mismatches. Therefore, $\omega_{max} \approx \omega_0$ can be expected at the same frequency, but low frequency CM(s) has higher magnitude values due to the mismatches, and second-order nonlinear behavior is higher. The higher magnitude of CM(s) at low frequencies is shown by the dashed line in Fig. 4.9, that represents the case that $I_{cQ1} = 0.524$mA and $I_{cQ2} = 0.476$mA, an imbalance of approx. 10 %.

Comparable effects of z_T and current (im)balance can be expected, when second-harmonic distortion and EMI are evaluated using the parameters given in Table 4.2. The linear differential current, the second-harmonic distortion current and the EMI susceptibility for signal frequencies between 10 kHz and 10 GHz, with a 1 kHz modulation of the envelope with modulation depth m=0.5 were calculated and are depicted in Figs. 4.10(a), 4.10(b), 4.11(a), and 4.11(b), respectively, for the case $I_{cQ1} = I_{cQ2} = 0.5$mA (solid lines), and for the case $I_{cQ1} = 0.524$mA and $I_{cQ2} = 0.476$mA, an imbalance of approx. 10 % (dashed lines).

Note that in Fig. 4.11(b) C_T has a value of 1 pF instead of 10 pF. The crosses (balance) and diamonds (imbalance) are SPICE simulation results. The method used seems to give adequate accuracy. The discrepancy shown between the simulation results and calculation at 1 GHz are due to neglecting four non-dominant poles and zeros (all located $> 5\omega_0$) in the transfers.



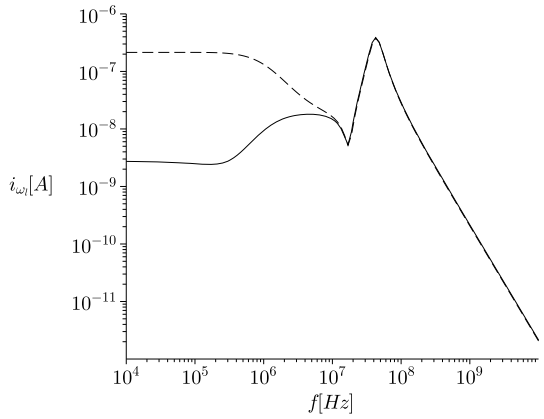
(a) Linear output current i_{o1}. Small bias current imbalances have little effect on the linear output current.



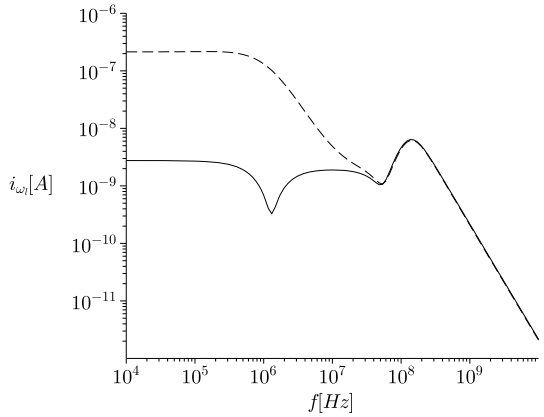
(b) Second-harmonic output current i_{o2} ($\omega_l = 2\omega_c$). At low frequencies second-harmonic distortion is much higher in case of bias current imbalance.

Figure 4.10: Solid lines show the predicted output current of Fig. 4.8(a) as function of frequency using the model of Fig. 4.7 in case of equal biasing. Dashed line shows the same output current in case of a 10% bias current mismatch between I_{cQ1} and I_{cQ2}. Crosses (balanced currents) and diamonds (10% imbalance) show SPICE simulation results. C_T is 10 pF.

It follows from Fig. 4.10(a) that the linear output current is hardly affected by the 10 % current imbalance. The output current is constant until it reaches the signal bandwidth of approximately 1.1 MHz ($\approx -p_2/(2\pi)$), after which it



(a) Magnitude of the detected 1 kHz EMI component ($\omega_l = 2\pi$krad/s). Current imbalance causes a significant increase in EMI at lower frequencies. C_T =10pF.



(b) Magnitude of the detected 1 kHz EMI component. Current imbalance causes a significant increase in EMI at lower frequencies. C_T = 1pF.

Figure 4.11: Solid lines show the EMI output current of Fig. 4.8(a) as function of frequency using the model of Fig. 4.7 in case of equal biasing. Dashed line shows the same output current in case of a 10% bias current mismatch between I_{cQ1} and I_{cQ2}. Fig. 4.11(a): current source capacitance C_T is 10 pF, and Fig. 4.11(b): C_T is 1 pF.

decreases until it starts to increase again, causing a dip.

This dip is caused by u_{be1} and u_{be2} and can therefore be found in both the

linear and the second-order transfers. Base-emitter voltages u_{be1} and u_{be2} are (among other terms) determined by $(1-A_2\kappa_2(s))/[1-(A_1\kappa_2(s)+A_2\kappa_2(s))]$ and $(1-A_1\kappa_1(s))/[1-(A_1\kappa_2(s)+A_2\kappa_2(s))]$, respectively. The numerators of these equations result in zeros, causing the dip at about 17 MHz in Figs. 4.10(a), 4.10(b), and 4.11(a) (and at 51 MHz in Fig. 4.11(b)). The extra zero-pole combination ($\approx$ 450 kHz and 2 MHz) in Fig. 4.11(a) and the extra dip in Fig. 4.11(b) at approximately 1.3 MHz in the (balanced case) EMI components, are also caused by the (differing numerators of the) expressions for u_{be1} and u_{be2}. It does not seem to be possible to easily pinpoint the parameter(s) that determines the zero-pole combination and the dip in the figures.

Both the magnitude of the linear and the second-order transfers increase until the 'bandwidth' of the feedback is reached. This frequency can be approximated by $\omega_0/(2\pi)$, i.e., the same equation as for the maximal magnitude of CM(s). Figures 4.10(a)−4.11(a) show a peak at 42 MHz, while f_0 is 44 MHz. Figure 4.11(b) shows the peak at 142 MHz and $f_o \approx 134$ MHz. The inaccuracy caused by the approximation is 4.5 % and 1.5 %, respectively. This is acceptable for design purposes.

Fig. 4.10(b) shows the magnitude of the second-harmonic of the input signals. second-harmonic distortion increases up to the bandwidth of the differential stage and then decreases. The second-harmonic distortion is already relatively high in the unbalanced case, and it increases up to about the same value as in the balanced case, reaching this value near the bandwidth. From about 17 MHz the second-harmonic distortion increases again until it reaches the peak value at f_0. Maximal second-harmonic distortion however, occurs at a lower frequency of approx. 632 kHz. Determining this maximum is considerably more difficult because it depends on several transfers that cannot be approximated with their DC value. Numerical simulation seems to be the easiest method.

The maximal magnitude of the detected 1kHz EMI component in Figure 4.11(a) is at 42 MHz and amounts 388 nA. Reducing C_T to 1 pF results in maxima of $i_{o\omega_l} = 6.42$ nA at 142 MHz (see Figure 4.11(b)). The higher the magnitude of CM(s), the higher the magnitude of the detected component. Therefore, maximum EMI has been reduced considerably and shifted to a higher frequency, when C_T is reduced to 1 pF, since the maximal magnitude of CM(s) has also been reduced and shifted to a higher frequency (see Fig. 4.9).

Balancing of the currents results in low EMI susceptibility at lower frequencies. In case of C_T being 10 pF, $i_{o\omega_l}$ remains between 2.8 nA and 18 nA and in case of C_T being equal to 1 pF, $i_{o\omega_l}$ is maximally 6.4 nA. The 10 % bias current imbalance has major effects at lower frequencies. For both values of C_T, $i_{o\omega_l}$ increases to a value of 212 nA. In case of a low C_T, EMI susceptibility may thus be largest at relatively low frequencies when the differential stage is imbalanced. In this case, it may show increased susceptibility in the AM radio band. If EMI susceptibility is too high at low frequencies, effort has to be made to reduce the imbalance, e.g., by assuring a better matching of the bias quantities and of the transistors.

4.5 Simplified differential stage hybrid-π models

The formal model and equations given in the previous section present some design rules (use matched devices, keep bias currents as equal as possible, design for a high value of Z_T), but it is complex as a starting point. When starting with the design of a negative-feedback amplifier, the design effort is greatly reduced when simple models that give sufficient accuracy can be used by the designer. Simple modified hybrid-π models of the differential stages, both bipolar and FET, will be given in this section. These models exchange some accuracy for simplicity. From analysis using the models it directly follows what can be done to decrease EMI generated in the differential stage. Also, the design of negative-feedback amplifiers with specified EMI behavior is simplified by using the simplified models. In subsequent steps, the design can then be evaluated and analyzed using the more elaborate, but more accurate, model of the differential stage given in the previous section.

Evaluating the equations of the various transfers in Figure 4.6 by using the modified hybrid-π models of the BJT and the FET at DC ($\xi_{11}(0)$, $\xi_{12}(0)$, etc.), it is possible to obtain expressions for both linear and second-order nonlinear behavior valid for EMI analysis. This is an elaborate task resulting in large expressions. These expressions are therefore derived in Appendix C. In the following subsections, the expressions are used to derive modified hybrid-π models. The equations and the models hold when $\beta_{ac} \gg 1$ and the intrinsic voltage gain of the FET $\mu = g_{m1} r_{ds} \gg 1$. Furthermore, it is assumed that $g_{m1} r_p \gg 1$, where $r_p \approx (r_{ds1} + R_{l1})//(r_{ds2} + R_{l2})//R_T$ in case of a FET differential stage, and $r_p \approx (r_{o1} + R_{l1})//(r_{o2} + R_{l2})//(r_{\pi 1} + R_{s1})//(r_{\pi 2} + R_{s2})//R_T$ in case of a BJT differential stage. These assumptions are usually easily met.

The subscripts 1 and 2 refer to the parameters of Q_1/M_1 and Q_2/M_2 respectively, as depicted in Figure 4.5. R_{l1} and R_{l2} are the load resistances of transistors Q_1/M_1 and Q_2/M_2.

4.5.1 Modified hybrid-π model of the BJT differential stage

The modified hybrid-π model of the BJT differential stage is derived using Figure 4.12. Capacitances are added to the hybrid-π model later. Using this figure and Equations (4.12) and (4.13), it follows for u_{be1} and u_{be2}

$$
\begin{aligned}
u_{be1} = & \frac{g_{m2} r_p \left(1 + \frac{R_{l1}}{r_{o1}}\right)}{1 + \left(g_{m1}\left(1 + \frac{R_{l2}}{r_{o2}}\right)\left(1 + \frac{R_{s2}}{r_{\pi 2}}\right) + g_{m2}\left(1 + \frac{R_{l1}}{r_{o1}}\right)\left(1 + \frac{R_{s1}}{r_{\pi 1}}\right)\right) r_p} \times \\
& \left(u_{s1} \left\{ 1 + \frac{R_{s2} + r_{\pi 2}}{\beta_{ac2} r_{o2}} \left(1 + \frac{r_{o2} + R_{l2}}{r_{o1} + R_{l1}} \left(1 + \frac{r_{o1} + R_{l1}}{R_T} \right) + \frac{r_{o2} + R_{l2}}{R_{s2} + r_{\pi 2}} \right) \right\} \right. \\
& \left. - u_{s2} \left\{ 1 + \frac{1}{\beta_{ac2}} \left(1 + \frac{R_{l2}}{r_{o2}} \right) \right\} \right),
\end{aligned}
\tag{4.20}
$$

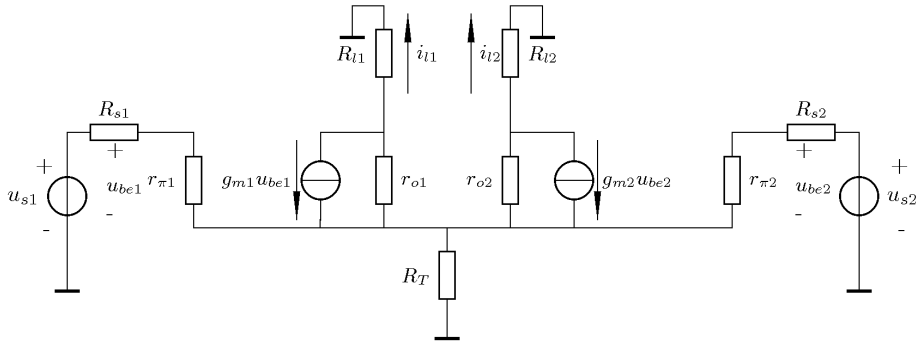


Figure 4.12: Low-frequency BJT differential stage small-signal model.

$$
\begin{aligned}
u_{be2} = & \frac{g_{m1} r_p \left(1 + \frac{R_{l2}}{r_{o2}}\right)}{1 + \left(g_{m1}\left(1 + \frac{R_{l2}}{r_{o2}}\right)\left(1 + \frac{R_{s2}}{r_{\pi 2}}\right) + g_{m2}\left(1 + \frac{R_{l1}}{r_{o1}}\right)\left(1 + \frac{R_{s1}}{r_{\pi 1}}\right)\right) r_p} \times \\
& \left(-u_{s1}\left\{1 + \frac{1}{\beta_{ac1}}\left(1 + \frac{R_{l1}}{r_{o1}}\right)\right\} + \right. \\
& \left. u_{s2}\left\{1 + \frac{R_{s1} + r_{\pi 1}}{\beta_{ac1} r_{o1}}\left(1 + \frac{r_{o1} + R_{l1}}{r_{o2} + R_{l2}}\left(1 + \frac{r_{o2} + R_{l2}}{R_T}\right) + \frac{r_{o2} + R_{l2}}{R_{s1} + r_{\pi 1}}\right)\right\}\right).
\end{aligned}
\tag{4.21}
$$

Apart from the assumptions already given above, it is also assumed that the coefficients of signal voltages u_{s1} and u_{s2} in Equations (4.20) and (4.21) can be approximated by one. This is valid in case $\beta_{ac1}, \beta_{ac2} \gg 1$ and $R_{l1}, R_{l2} \ll r_{o1}, r_{o2}$.

Applying these approximations will yield equations with adequate accuracy and, facilitated by a circuit/modified hybrid-π representation of the differential stage, can be used for design purposes. This will be shown with a numerical example on page 135.

Simplifying Equations (4.20) and (4.21) with the assumptions given, the following approximate equations are found. Base resistances r_{B1} and r_{B2} are assumed to be part of the resistance R_{s1} and R_{s2}, respectively.

The base-emitter voltages are found to be approximated by

$$
u_{be1} \approx (u_{s1} - u_{s2}) \frac{r_{\pi 1 a}\left(1 + \frac{R_{l1}}{r_{o1}}\right)}{(R_{s1} + r_{\pi 1})\left(1 + \frac{R_{l1}}{r_{o1}}\right)\frac{\beta_{ac2}}{\beta_{ac1}} + (R_{s2} + r_{\pi 2})\left(1 + \frac{R_{l2}}{r_{o2}}\right)}, \tag{4.22}
$$

where[9] $r_{\pi 1a} = \beta_{ac2}/g_{m1}$, and

$$u_{be2} \approx (u_{s2} - u_{s1}) \frac{r_{\pi 2}\left(1 + \frac{R_{l2}}{r_{o2}}\right)}{(R_{s1} + r_{\pi 1})\left(1 + \frac{R_{l1}}{r_{o1}}\right)\frac{\beta_{ac2}}{\beta_{ac1}} + (R_{s2} + r_{\pi 2})\left(1 + \frac{R_{l2}}{r_{o2}}\right)}. \quad (4.23)$$

To facilitate a circuit design approach, the differential base to base voltage, $u_d = u_{be1} - u_{be2}$, is introduced. With $r_{\pi t} = r_{\pi 1a}\left(1 + \frac{R_{l1}}{r_{o1}}\right) + r_{\pi 2}\left(1 + \frac{R_{l2}}{r_{o2}}\right)$, u_d can be written as

$$u_d = (u_{s1} - u_{s2}) \frac{r_{\pi t}}{r_{\pi t} + R_{s1}\left(1 + \frac{R_{l1}}{r_{o1}}\right)\frac{\beta_{ac2}}{\beta_{ac1}} + R_{s2}\left(1 + \frac{R_{l2}}{r_{o2}}\right)}. \quad (4.24)$$

Source resistances R_{s1} and R_{s2} are multiplied by $\left(1 + \frac{R_{l1}}{r_{o1}}\right)\frac{\beta_{ac2}}{\beta_{ac1}}$ and $\left(1 + \frac{R_{l2}}{r_{o2}}\right)$, respectively. In case of (almost) matched transistors and equal biasing and with load resistances much smaller than the output resistances of the transistors, these coefficients are approximately one. Note that in case of current drive, u_{s1} and u_{s2} may be replaced by $i_{s1}R_{s1}\left(1 + \frac{R_{l1}}{r_{o1}}\right)$ and $i_{s2}R_{s2}\left(1 + \frac{R_{l2}}{r_{o2}}\right)$, respectively, to calculate the correct value of u_d.

Equations for the currents in the loads R_{l1} and R_{l2} (both linear and due to detection of EMI) are derived in Appendix C. Under the same assumptions as used for deriving the approximate equations for u_{be1} and u_{be2} and using the results of Appendix C, the following approximate equations are found. The linear transconductance of the differential stage is found to be given by:

$$g_{mt} = \frac{i_{c1} - i_{c2}}{u_d} = \frac{g_{m1}g_{m2}\left(\left(1 + \frac{R_{l1}}{r_{o1}}\right) + \left(1 + \frac{R_{l2}}{r_{o2}}\right)\right)}{g_{m1}\left(1 + \frac{R_{l2}}{r_{o2}}\right) + g_{m2}\left(1 + \frac{R_{l1}}{r_{o1}}\right)}. \quad (4.25)$$

The differential output current $(i_{l1} - i_{l2})$ is thus given by

$$i_l = -u_d g_{mt} \frac{r_{ot}}{r_{ot} + R_{l1} + R_{l2}}, \quad (4.26)$$

where $r_{ot} = r_{o1} + r_{o2}$.

The unbalanced output currents i_{l1} and i_{l2} equal

$$i_{l1} = -u_d g_{mt} \frac{r_{o1}}{r_{ot}} \frac{r_{ot}}{r_{ot} + R_{l1} + R_{l2}} \quad (4.27)$$

and

$$i_{l2} = u_d g_{mt} \frac{r_{o2}}{r_{ot}} \frac{r_{ot}}{r_{ot} + R_{l1} + R_{l2}}. \quad (4.28)$$

[9] Deriving (4.22) results in $r_{\pi 2}\frac{g_{m2}}{g_{m1}}\left(1 + \frac{R_{l1}}{r_{o1}}\right) = \frac{\beta_{ac2}}{g_{m1}}\left(1 + \frac{R_{l1}}{r_{o1}}\right) = r_{\pi 1a}\left(1 + \frac{R_{l1}}{r_{o1}}\right)$ for the numerator.

The transconductance in case of single-ended loading thus appears to be r_{o1}/r_{ot} respectively r_{o2}/r_{ot} as large as the transconductance in case of differential loading. For not too large differences in biasing and transistor matching, the single-ended transconductance is thus about one-half the differential transconductance.

The detection terms in the currents $i_{c1\omega_l}$ and $i_{c2\omega_l}$ are derived to be equal to

$$\begin{aligned} i_{c1\omega_l} =& u_d^2 \left(\frac{r_{\pi 1a}\left(1+\frac{R_{l1}}{r_{o1}}\right)}{r_{\pi t}} \right)^2 m \frac{r_{\pi 1}}{R_{s1}+R_{s2}+r_{\pi 1}+r_{\pi 2}} \times \\ & \left\{ a_{12} - a_{22}\left(\frac{g_{m1}}{g_{m2}}\right)^3 \left(\frac{\left(1+\frac{R_{l2}}{r_{o2}}\right)}{\left(1+\frac{R_{l1}}{r_{o1}}\right)} \right)^2 \right\} \end{aligned} \tag{4.29}$$

and

$$\begin{aligned} i_{c2\omega_l} =& u_d^2 \left(\frac{r_{\pi 2}\left(1+\frac{R_{l2}}{r_{o2}}\right)}{r_{\pi t}} \right)^2 m \frac{r_{\pi 2}}{R_{s1}+R_{s2}+r_{\pi 1}+r_{\pi 2}} \times \\ & \left\{ a_{22} - a_{12}\left(\frac{g_{m2}}{g_{m1}}\right)^3 \left(\frac{\left(1+\frac{R_{l1}}{r_{o1}}\right)}{\left(1+\frac{R_{l2}}{r_{o2}}\right)} \right)^2 \right\}. \end{aligned} \tag{4.30}$$

Two second-order nonlinearity coefficients can be defined. Firstly, $a'_{21}(0)$, giving the detection current in the first transistor, and secondly $a'_{22}(0)$, giving the current in the second transistor:

$$\begin{aligned} a'_{21}(0) =& \frac{r_{\pi 1}}{R_{s1}+R_{s2}+r_{\pi 1}+r_{\pi 2}} \left(\frac{r_{\pi 1a}\left(1+\frac{R_{l1}}{r_{o1}}\right)}{r_{\pi t}} \right)^2 \times \\ & \left\{ a_{12} - a_{22}\left(\frac{g_{m1}}{g_{m2}}\right)^3 \left(\frac{\left(1+\frac{R_{l2}}{r_{o2}}\right)}{\left(1+\frac{R_{l1}}{r_{o1}}\right)} \right)^2 \right\} \end{aligned} \tag{4.31}$$

$$\begin{aligned} a'_{22}(0) =& \frac{r_{\pi 2}}{R_{s1}+R_{s2}+r_{\pi 1}+r_{\pi 2}} \left(\frac{r_{\pi 2}\left(1+\frac{R_{l2}}{r_{o2}}\right)}{r_{\pi t}} \right)^2 \times \\ & \left\{ a_{22} - a_{12}\left(\frac{g_{m2}}{g_{m1}}\right)^3 \left(\frac{\left(1+\frac{R_{l1}}{r_{o1}}\right)}{\left(1+\frac{R_{l2}}{r_{o2}}\right)} \right)^2 \right\}. \end{aligned} \tag{4.32}$$

The detection terms in the load currents, $i_{l1\omega_l}$, $i_{l2\omega_l}$, and $i_{l\omega_l}$ are now given

by

$$\begin{aligned} i_{l1\omega_l} &= i_{c1\omega_l}\frac{r_{o1}}{r_{ot}+R_{l1}+R_{l2}} - i_{c2\omega_l}\frac{r_{o2}}{r_{ot}+R_{l1}+R_{l2}} \\ i_{l2\omega_l} &= i_{c2\omega_l}\frac{r_{o2}}{r_{ot}+R_{l1}+R_{l2}} - i_{c1\omega_l}\frac{r_{o1}}{r_{ot}+R_{l1}+R_{l2}} \\ i_{l\omega_l} &= i_{l1\omega_l} - i_{l2\omega_l}. \end{aligned} \tag{4.33}$$

Evaluating these equations, it appears to be possible to define one second-order nonlinear term that can be used to determine all three currents,

$$\begin{aligned} a_2'(0) =& a_{21}'(0)\left(\frac{r_{o1}}{r_{ot}} + \frac{\beta_{ac2}}{\beta_{ac1}}\frac{r_{o2}}{r_{ot}}\right) \\ =& -a_{22}'(0)\left(\frac{r_{o2}}{r_{ot}} + \frac{\beta_{ac1}}{\beta_{ac2}}\frac{r_{o1}}{r_{ot}}\right) \end{aligned} \tag{4.34}$$

and thus,

$$i_{l1\omega_l} = u_d^2 m a_2'(0)\frac{r_{ot}}{r_{ot}+R_{l1}+R_{l2}} \tag{4.35}$$

and

$$i_{l2\omega_l} = -u_d^2 m a_2'(0)\frac{r_{ot}}{r_{ot}+R_{l1}+R_{l2}}. \tag{4.36}$$

The differential output current is now

$$i_{l\omega_l} = 2u_d^2 m a_2'(0)\frac{r_{ot}}{r_{ot}+R_{l1}+R_{l2}}. \tag{4.37}$$

Just as was the case for current i_l, $i_{l\omega_l}$ is two times as large as in case of single-ended loading. It is important to observe that for $a_2'(0)$ not equal to zero, differential loading of the balanced stage does not result in a zero value of $i_{l\omega_l}$. When $a_2'(0) = 0$, because the terms between the braces of the equations for $a_{21}'(0)$ and $a_{22}'(0)$ are zero, no detected currents appear in both the case of single-ended and differential loading. These terms can only equal zero when there are no mismatches between the transistors, the biasing of the transistors is exactly equal, and loading resistances $\frac{R_{l1}}{r_{o1}}$ and $\frac{R_{l2}}{r_{o2}}$ are also exactly equal. In practical cases, these conditions are already hard to meet in differential stages. For differential stages with two single-ended loads, it is impossible to meet the conditions since $\frac{R_{l1}}{r_{o1}} \neq \frac{R_{l2}}{r_{o2}}$. Hence, in such practical cases, a larger detected current can be expected.

An increase in the value of $a_2'(0)$ can be observed when either R_{l1} or R_{l2} rises above the value of r_o. To minimize the adverse effect of inequalities in R_{l1} and R_{l2}, it is recommended to realize values of r_o much larger than the load resistances. If necessary, cascoding can be used to increase the values of r_{o1} and r_{o2}. Inequalities in bias values and mismatches between the BJTs will increase the value of $a_2'(0)$. It is, however, impossible to avoid these inequalities, although measures can be taken to minimize them, as will be discussed in Section 4.6.

Voltage driving both BJTs results in the largest second-order nonlinearity for a certain amount of imbalance. Current driving at least one of the BJTs seems to be advantageous for lowering the second-order nonlinearity. These observations

are analogous to the unbalanced BJT. The fact that only one BJT has to be current driven may ease the design effort in some cases. The designer should, however, be aware that in case of current driving just one BJT, EMI will be low at relatively low frequencies of ω_c. There will be much worse EMI behavior at ω_0, as was explained in the previous section. It is therefore recommended to drive both BJTs with a signal current source. Perfectly matched transistors and biasing results in zero second-order nonlinearity. This is independent of voltage or current driving of the balanced stage.

A modified hybrid-π model for the BJT differential stage is given in Figure 4.13. It facilitates a simple approach for analysis and design of BJT differential stages. Both the hybrid-π model and the equations given in this section can be used to design negative-feedback amplifiers with specified EMI behavior. Sources and loads are omitted for clarity in Figure 4.13. Base resistances (r_B) are depicted in the figure for completeness. Capacitance $C_{\pi t} = (C_{\pi 1}^{-1} + C_{\pi 2}^{-1})^{-1}$. The input signals are applied to terminals e_{s1} and e_{s2}.

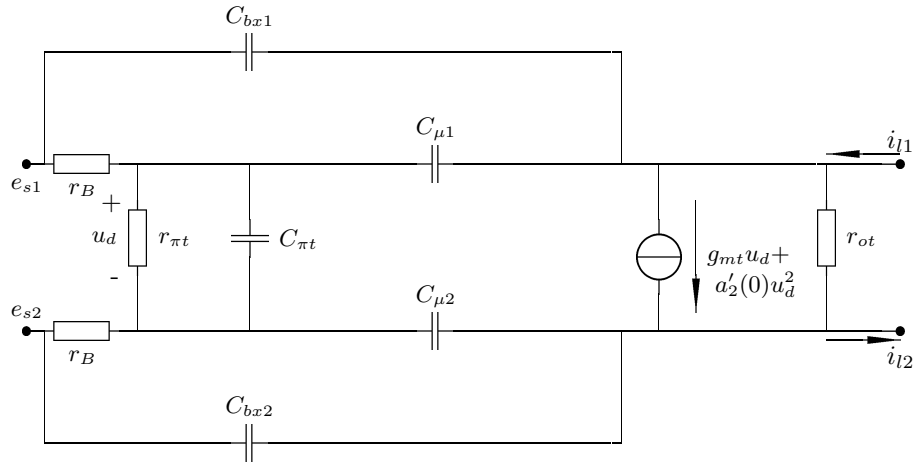


Figure 4.13: BJT differential stage hybrid-π model suitable for both linear and EMI analysis and design. See text for the conditions for validity of this model.

It is not immediately clear from the expression for $a_2'(0)$ what the effect of an increase or decrease in bias current will be. Therefore, $a_2'(0)$ will be expressed in terms of bias parameters and parameters that account for inequalities. Transistor mismatches resulting in unequal β_{ac} are taken into account by $\delta = \frac{\beta_{ac2}}{\beta_{ac1}}$, and inequalities in bias currents are taken into account by $\upsilon = \frac{I_{cQ2}}{I_{cQ1}}$. Inequalities in r_o resulting from differences in the Early voltage are taken into account by $\Lambda = \frac{U_{AF2}}{U_{AF1}}$. Here, the equation for $a_2'(0)$ has been expressed in terms of the parameters of BJT 1 (Q_1 in Fig. 4.5(a)). It may, however, also be expressed in

terms of BJT 2 (Q_2 in Fig. 4.5(a)),

$$a_2'(0) = \frac{1}{2}\left(\frac{q}{n_f kT}\right)^2 I_{cQ1}\frac{\upsilon\beta_{ac1}}{\frac{q}{n_f kT}I_{cQ1}\left(R_{s1}+R_{s2}\right)\upsilon+\beta_{ac1}(\upsilon+\delta)}\times \left[\frac{\upsilon^2\left(1+\frac{R_{l1}}{r_{o1}}\right)^2-\left(1+\frac{R_{l2}}{r_{o2}}\right)^2}{\left[\upsilon\left(1+\frac{R_{l1}}{r_{o1}}\right)+\left(1+\frac{R_{l2}}{r_{o2}}\right)\right]^2}\right]\frac{\upsilon}{\upsilon+\Lambda}\left(1+\delta\frac{\Lambda}{\upsilon}\right). \tag{4.38}$$

The linearizing effect of high-valued source resistances from current driving is clearly recognized; $a_2'(0)$ decreases with increasing values of $R_{s1}+R_{s2}$. In the case of some imbalance, $a_2'(0)$ will therefore behave like g_{m2} of a single BJT for changes in bias current.

By differentiating (4.38) with respect to υ, δ, or Λ, it is possible to determine which of these terms affects the value of $a_2'(0)$ the most. When this is done, still under the assumption of negligible load resistances, it is found that $a_2'(0)$ is affected most by unequal values of the bias currents. The effect of a 10% current imbalance is several hundreds of times larger than the effect of 10% imbalance in the β_{ac} values or the Early voltages. Careful, equal biasing of the BJTs is thus more important than BJT matching.

The effect of unequal currents is demonstrated by the following example. If I_{cQ2} is 10 % larger than I_{cQ1}, it is found that, under the assumption that $R_{s1}=R_{s2}=0$ and $R_{l1}\ll r_{o1}$ and $R_{l2}\ll r_{o2}$, that $a_2'(0)$ is about equal to $0.5g_{mt}$. When the 10 % inequalities are reversed, $a_2'(0)$ is about equal to $-0.5g_{mt}$. With a $\pm 2\%$ inequality between I_{cQ1} and I_{cQ2}, $a_2'(0)$ is approximately equal to $\pm 0.1g_{mt}$. These relatively large values of $a_2'(0)$ can not be neglected in low distortion and low EMI design. Unequal values of β_{ac} ($\pm 10\%$) and U_{AF} ($\pm 10\%$) hardly affect $a_2'(0)$. Lower values of $a_2'(0)$ are found when the inequalities are reduced and/or $R_{s1}+R_{s2}$ are increased.

To be able to estimate EMI, equations for CM are needed also. CM(0) is approximated by

$$CM(0)\approx\frac{1}{2}(u_{s1}-u_{s2})\frac{\left(r_{\pi 1a}\left(1+\frac{R_{l1}}{r_{o1}}\right)-r_{\pi 2}\left(1+\frac{R_{l2}}{r_{o2}}\right)\right)}{r_{\pi t}+R_{s1}\left(1+\frac{R_{l1}}{r_{o1}}\right)\frac{\beta_{ac2}}{\beta_{ac1}}+R_{s2}\left(1+\frac{R_{l2}}{r_{o2}}\right)}. \tag{4.39}$$

As was argued in Subsection 4.4.1, the EMI component in the differential stage output current is either dominant at lower frequencies of ω_c, due to imbalances in biasing and inequalities in the transistors, or at a higher frequency, ω_{max}, due to the capacitance of the current source connected to the emitter (source) nodes. It was shown that by evaluating the expression for CM(s), it is possible to determine if EMI at ω_{max} is dominating EMI behavior. It is advantageous to be able to determine the dominating EMI susceptible frequency using the simplified method discussed in this section. In short, we have to determine whether CM(0) or CM(ω_0) is dominating EMI.

A first order approximation of CM(ω_0) is given by

$$CM(\omega_0) \approx \frac{1}{2}(u_{s1}-u_{s2})\frac{1}{\left(1-\frac{j\omega_0}{p_a}\right)}\times \frac{\left(r_{\pi 1a}\left(1+\frac{R_{l1}}{r_{o1}}\right)\left(1-\frac{j\omega_0}{z_1}\right)-r_{\pi 2}\left(1+\frac{R_{l2}}{r_{o2}}\right)\left(1-\frac{j\omega_0}{z_2}\right)\right)}{r_{\pi t}+R_{s1}\left(1+\frac{R_{l1}}{r_{o1}}\right)\frac{\beta_{ac2}}{\beta_{ac1}}+R_{s2}\left(1+\frac{R_{l2}}{r_{o2}}\right)}. \quad (4.40)$$

Zeros z_1 and z_2 are given by the input circuit of the hybrid-π circuit and the source resistances. For the example of Section 4.4.1 (Fig. 4.8(a)), these zeros are given by $z_1 \approx -\frac{1}{R_{s1}(C_T^{-1}+C_{\pi 1}^{-1})^{-1}}$ and $z_2 \approx -\frac{1}{R_{s2}(C_T^{-1}+C_{\pi 2}^{-1})^{-1}}$. Frequency $\omega_0 \approx \sqrt{(1+(g_{m1}+g_{m2})r_p)p_l p_h}$, where r_p is given by the parallel equivalent of the input resistances, $r_p \approx (R_{s1}+r_{\pi 1})//(R_{s2}+r_{\pi 2})$, pole p_h is approximated by $p_h \approx -\frac{1}{(R_{s1}//R_{s2})C_T}$, and pole p_l can best be approximated by $p_l = \frac{1}{\tau_1+\tau_2}$, with $\tau_1 \approx ((R_{s1}+R_{s2}+r_{\pi 2})//r_{\pi 1})C_{\pi 1}$ and $\tau_2 \approx ((R_{s1}+R_{s2}+r_{\pi 1})//r_{\pi 2})C_{\pi 2}$. Pole $p_a \approx -\frac{1}{((R_{s1}+R_{s2})//r_{\pi t})C_{\pi t}}$ is the dominant pole of the linear transfer of the differential stage.

In case of equal bias currents and $C_T = 10$ pF, $|CM(0)| \approx 870nV$ and $|CM(\omega_0)| \approx 138\mu V$. Clearly, EMI susceptibility will be higher at ω_0 than at DC. Using the approximate method presented in this section, it is found that $\omega_0/(2\pi)$ is approximately 44 MHz, resulting in an $i_{o\omega_l}$ of 380 nA. Figure 4.11(a) gives 42 MHz and 388 nA respectively. With 10 % unbalance in the bias currents, $|CM(0)| \approx 181\mu V$ and $|CM(\omega_0)| \approx 1mV$. Still, EMI will dominate at ω_0.

A C_T of 1 pF results in the balanced case in $|CM(0)| \approx 870nV$ and $|CM(\omega_0)| \approx 122\mu V$. The approximate method results in $\omega_0/(2\pi) \approx 134$ MHz and $i_{o\omega_l} \approx 6.4$ nA. From Figure 4.11(b) follows $\omega_0/(2\pi) \approx 142$ MHz and an $i_{o\omega_l}$ of 6.4 nA. The unbalanced case now results in $|CM(0)| \approx 181\mu V$ and $|CM(\omega_0)| \approx 132\mu V$. Only in this last case does EMI susceptibility dominate at lower frequencies instead of at ω_0.

For the unbalanced cases, $a_2'(0)$ is found to be equal to -7.82 mA/V^2 and $i_{l1\omega_l} = -i_{l2\omega_l} \approx -218$ nA. Figures 4.11(a) and 4.11(b) show virtually the same results: $|i_{l1\omega_l}| = |-i_{l2\omega_l}| = 212$ nA. If the method is used at 10 kHz, a value of 2.7 nA is found for $i_{o\omega l}$ in the balanced cases. Figures 4.11(a) and 4.11(b) give $i_{o\omega l}$= 2.8 nA at 10 kHz.

The simple, approximate method presented in this section shows adequate precision in both linear and EMI transfer calculations[10]. Moreover, due to its simplicity, it facilitates design of low EMI-susceptible negative-feedback amplifiers using differential stages.

4.5.2 Modified hybrid-π model of the FET differential stage

Under the conditions mentioned earlier, the transconductance, second-order non-linear transconductance, and the expressions for the linear and EMI (ω_l) output

[10]The low-frequency inaccuracy of the linear transfer is 1.5 % and the maximal inaccuracy found in the EMI calculation is 2.8 %, in this example.

currents are derived in this section. Also a modified hybrid-π model of the FET differential stage usable for design will be presented. The equations will be presented in such a manner that the effect of different component values, and differences in matching and biasing are made explicit.

The linear transconductance is found to be approximated by

$$g_{mt} = \frac{g_{m1}g_{m2}\left(\left(1+\frac{R_{l1}}{r_{ds1}}\right)+\left(1+\frac{R_{l2}}{r_{ds2}}\right)\right)}{g_{m1}\left(1+\frac{R_{l2}}{r_{ds2}}\right)+g_{m2}\left(1+\frac{R_{l1}}{r_{ds1}}\right)}. \tag{4.41}$$

The differential current, $i_{l1}-i_{l2}$ can be calculated with (4.26) when $r_{o1} \to r_{ds1}$, $r_{o2} \to r_{ds2}$, $r_{ot} \to r_{dst}$, and $r_{dst} = r_{ds1} + r_{ds2}$. Nonlinear behavior of r_{dst} is not modelled because it is (and should) made negligible by cascoding the FETs. Similarly, the single-ended currents i_{l1} and i_{l2} can be calculated with (4.27) and (4.28), respectively.

The detected signals in the load currents, $i_{l\omega_l}, i_{l1\omega_l}$, and $i_{l2\omega_l}$ can be calculated with Equations (4.35)-(4.37). However, the second-order nonlinear term $a_2'(0)$ changes. Using the same approach as in Subsection 4.5.1, $a_2'(0)$ is found to be given by

$$a_2'(0) = \quad a_{21}'(0)\left(\frac{r_{ds1}}{r_{dst}}+\frac{\left(1+\frac{R_{l2}}{r_{ds2}}\right)}{\left(1+\frac{R_{l1}}{r_{ds1}}\right)}\frac{r_{ds2}}{r_{dst}}\right), \tag{4.42}$$

and $a_{21}'(0)$ by

$$\begin{aligned} a_{21}'(0) = &\left(\frac{g_{m2}\left(1+\frac{R_{l1}}{r_{ds1}}\right)}{g_{m1}\left(1+\frac{R_{l2}}{r_{ds2}}\right)+g_{m2}\left(1+\frac{R_{l1}}{r_{ds1}}\right)}\right)^3 \times \\ &\left\{a_{12}-a_{22}\left(\frac{g_{m1}}{g_{m2}}\right)^3\left(\frac{\left(1+\frac{R_{l2}}{r_{ds2}}\right)}{\left(1+\frac{R_{l1}}{r_{ds1}}\right)}\right)^2\right\}. \end{aligned} \tag{4.43}$$

It is possible to express $a_2'(0)$ in terms of $a_{22}'(0)$, as demonstrated in Subsection 4.5.1. We will not elaborate on this, since it will give the same results as the expressions presented here.

A modified hybrid-π model for the FET differential stage as presented in Figure 4.14 follows from the previously derived equations. Capacitances C_{gs} and C_{gd} may be regarded as constant for both the JFET and MOSFET(see Chapter 3). Total gate-source capacitance C_{gst}, is given by

$$C_{gst} = \frac{C_{gs1}C_{gs2}}{C_{gs1}+C_{gs2}}, \tag{4.44}$$

where C_{gs1} is the gate-source capacitance of FET 1 (M_1 in Fig. 4.5(b)) and C_{gs2} is the gate-source capacitance of FET 2 (M_2 in Fig. 4.5(b)). C_{gd1} and C_{gd2} in

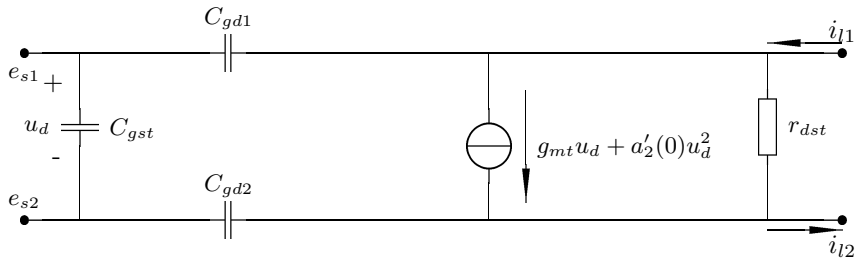


Figure 4.14: FET differential stage hybrid-π model suitable for both linear and EMI analysis and design.

Figure 4.14 are the gate-drain capacitances of FET 1 respectively FET 2. The second-order nonlinearity factor $a_2'(0)$ is given by

$$a_2'(0) \approx \beta_{\text{FET1}} \cdot \frac{1+\Lambda\upsilon[1+\lambda_1 I_{dQ_1}(R_{l1}+R_{l2})]}{\Lambda\upsilon(1+R_{l1}\lambda_1 I_{dQ_1})} \cdot \frac{\delta}{\sqrt{\delta\upsilon}} \cdot \frac{\Lambda\upsilon}{\Lambda\upsilon+1} \times \frac{\upsilon\sqrt{\delta\upsilon}(1+\lambda_1 R_{l1} I_{dQ_1})^2 - (1+\Lambda\lambda_1\upsilon R_{l2} I_{dQ_1})^2}{\left[1+\Lambda\lambda_1\upsilon R_{l2} I_{dQ_1} + \sqrt{\delta\upsilon}(1+\lambda_1 R_{l1} I_{dQ_1})\right]^2}. \tag{4.45}$$

Transistor mismatches resulting in unequal β_{FET}s and channel length modulation factors λ, are accounted for by $\delta = \frac{\beta_{\text{FET}_2}}{\beta_{\text{FET}_1}}$ and $\Lambda = \frac{\lambda_2}{\lambda_1}$, respectively. Inequalities in bias currents are taken into account by $\upsilon = \frac{I_{dQ2}}{I_{dQ1}}$. Here, the equation for $a_2'(0)$ has been expressed in terms of FET 1. It may, however, also be expressed in terms of FET 2.

$a_2'(0)$ can only become zero when a_{12} equals a_{22}, g_{m1} and g_{m2} are equal, and when $\frac{R_{l1}}{r_{ds1}}$ and $\frac{R_{l2}}{r_{ds2}}$ have the same value. A rapid increase in the value of $a_2'(0)$ can be observed when either R_{l1} or R_{l2} rise above the value of r_{ds}. To minimize the adverse effect of inequalities in R_{l1} and R_{l2}, it is recommended to realize values or r_{ds} much larger than the load resistances. If necessary, cascoding can be used to increase the value of r_{ds1} and r_{ds2}. Note that the hybrid-π model of Figure 4.14 should be modified accordingly in that case (see Section 4.1).

Inequalities in bias values and mismatches between the FETs will increase the value of $a_2'(0)$. It is, however, impossible to avoid these inequalities, although measures can be taken to minimize them, as will be discussed in Section 4.6. In case of a ±10% current imbalance ($\upsilon = \pm 10\%$), and also ±10% mismatch in δ and Λ, worst-case values of $a_2'(0) \approx -53 \cdot 10^{-3}\beta_{\text{FET1}}$ resp. $a_2'(0) \approx 48 \cdot 10^{-3}\beta_{\text{FET1}}$ are found, under the assumption that secondary effects like mobility degradation, etc., do not occur and R_{l1} and R_{l2} are much smaller than r_{ds}. Unequal values of the bias currents cause greater changes in $a_2'(0)$ than unequal FET parameters. The effect, however, does not dominate $a_2'(0)$ as much as in case of a BJT differential stage. It will in practical cases be, e.g., a factor 3–5 greater than the effects of unequal FET parameters on $a_2'(0)$. In the case of FET

differential stages, matching is therefore more important than in case of BJT differential stages.

As long as the load resistances are much smaller than r_{ds}, Λ hardly affects $a_2'(0)$. Finally, an increase in bias current of the FETs does usually not lead to a significant decrease of $a_2'(0)$.

Further, the approximate equation for CM(0) is given by

$$CM(0) \approx \frac{1}{2}(u_{s1} - u_{s2}) \frac{g_{m2}\left(1 + \frac{R_{l1}}{r_{ds1}}\right) - g_{m1}\left(1 + \frac{R_{l2}}{r_{ds2}}\right)}{g_{m1}\left(1 + \frac{R_{l2}}{r_{ds2}}\right) + g_{m2}\left(1 + \frac{R_{l1}}{r_{ds1}}\right)}. \tag{4.46}$$

It is expected that $CM(0)$ will have a larger value than $CM(\omega_0)$ in practical, well designed cases. Therefore, we suffice with the equation for $CM(0)$. The equation for $CM(\omega_0)$ may be derived using the same approach as presented in Subsection 4.5.1.

4.6 Reducing differential pair second-order nonlinearity

The second-order nonlinearity should be as low as possible. In this section, some design considerations, e.g., about biasing the differential stage and about matching transistors are presented.

4.6.1 Design considerations

Load impedances higher than the output impedances of the transistors should be avoided since this will increase a_2' of the differential stage if R_{l1} and R_{l2} are not exactly equal. The impedance mismatch formed by the (high) output impedances of the transistors and the (low) load impedances must thus be large, i.e., the differential stage should drive as low an impedance as possible (i.e., a shortcircuit or current load, e.g., a current amplifying input).

In case of inequalities that cannot be altered by the designer, the signal-to-error ratio (SER) should be made as large as possible otherwise. It is possible to increase the SER in case of the FET differential stage by increasing the bias current, since g_{mt} increases with the bias current and $a_2'(0)$ is almost independent of the bias current under current load conditions. In other words, at the expense of increased power consumption, the SER can be increased. The SER is inversely proportional to the square root of the bias current. The straightforward bias current dependency of the SER is not observed in the BJT differential stage.

Parameter $a_2'(0)$ of the BJT differential stage can be reduced by current driving it and ensuring that the signal source impedances match as much as possible, so that $a_2'(\omega_0)$ will be small. This may not always be possible when the BJT differential stage is used as an input stage. For instance, in the case of shunt feedback at the input, the source impedance driving one transistor is expected to be much larger than the 'source impedance' of the other, which is usually

zero. When used as an output stage, matching source impedances and current driving may be possible. A differential input stage, cascoded if necessary, can provide current drive to a (BJT) differential output stage with very high and nearly equal impedances and $a_2'(\omega_c)$ can reach low values. The contribution to the open loop gain will remain equal to the current gain α (Chapter 5) of the differential stage, while it will add only a small amount of nonlinearity to the negative-feedback amplifier.

Finally, the output impedance of bias current sources connected to the differential stage, e.g., at the emitter (source) node, should be higher than the input impedances in the hybrid-π model of the transistors. At higher frequencies, the capacitance of the current source dominates the output impedance. For low EMI behavior, this capacitance should be an order of magnitude lower than the input capacitances of the transistors (e.g., C_π or C_{gs}).

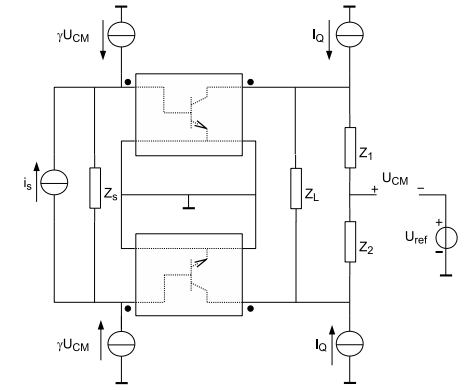
4.6.2 Biasing differential stages

Correct biasing of the differential stage depends on the signal source and load. There are four possibilities for driving and loading differential amplifiers, each requiring its own biasing scheme [8]. For biasing differential stages the same considerations hold:

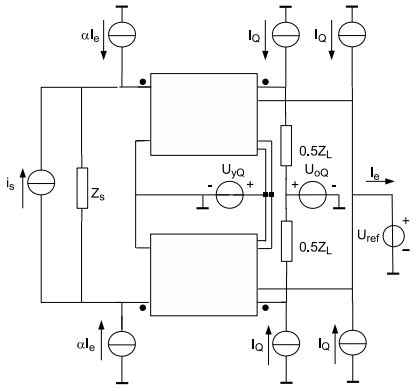
- differential amplifier with floating source and floating load
- differential amplifier with floating source and fixed load
- differential amplifier with fixed source and floating load
- differential amplifier with fixed source and fixed load

Figure 4.15 shows these four biasing schemes. The dots depict the orientation of the amplifiers or the transistors forming the differential stage, respectively (see the dashed BJTs depicted in Figs. 4.15(a) and 4.15(c) (FETs can be used also)). Note that Figs. 4.15(b) and 4.15(d) need dummy outputs. This can not be realized with a single differential stage. The circuit in the boxes becomes more complex. Therefore, transistors are not depicted in the figures.

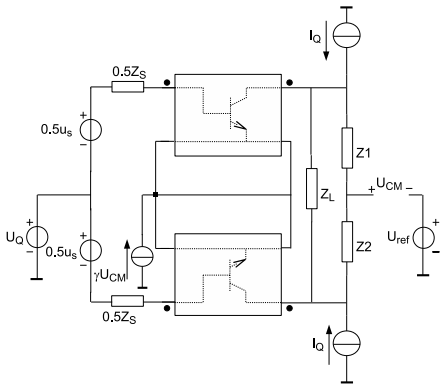
A differential stage with floating source and floating load, see Fig. 4.15(a), requires two bias current sources to deliver bias currents I_Q to the transistors. The common-mode voltage (U_{CM}) at the output has to be measured and compared to a reference voltage in order to set its value. The difference voltage is amplified by two voltage-controlled current sources, γU_{CM}. When the loop gain of this common-mode feedback loop is large enough, each controlled current source delivers a current to the base of the differential stage, thus setting the value of $U_{beQ1,2}$ that corresponds to bias current I_Q. The bias currents set the collector voltage to the reference voltage. Note that for the biasing, no current source is required at the emitter node. This node can be connected to a voltage source or 'ground' (the reference). In order not to degrade the differential stage quality, $Z_1 = Z_2 \gg Z_L$ should hold. Two examples of complete differential



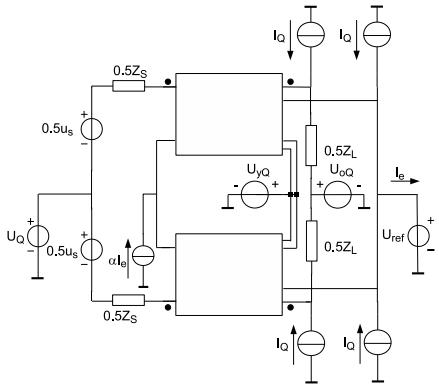
(a) The biasing scheme for a differential amplifier with floating source and floating load.



(b) The biasing scheme for a differential amplifier with floating source and fixed load.



(c) The biasing scheme for a differential amplifier with fixed source and floating load.



(d) The biasing scheme for a differential amplifier with fixed source and fixed load.

Figure 4.15: Biasing schemes for differential amplifiers [8]. Note that the schemes hold for both complete amplifiers and differential stages. See text for discussion.

negative-feedback amplifiers using this biasing technique can be found in [128] and in [8].

Note that the omittance of the current source at the common emitter node does not affect CM(s) or EMI behavior of the differential stage, as the emitter node remains floating for the differential input signal (i_s in Fig. 4.15(a)). Both linear and second-order nonlinear behavior can still be determined using the models and equations presented in this chapter. In this case, however, the current source impedances of the (voltage-controlled) current sources (γU_{CM}) affect the differential stage behavior, in a similar way as a current source at the emitter node.

Fig. 4.15(b) depicts the bias scheme for differential amplifiers with floating source and fixed load. In order to make the bias currents of the output stage equal to I_Q, an identical dummy output is formed inside the amplifier.

The difference between the currents coming from the dummy outputs and I_Q, I_e, is amplified and fed to the inputs of the differential amplifier by means of current-controlled current sources αI_e, thus setting the output currents to I_Q. Voltage source U_{oQ} sets the output voltage of the output stage, while U_{ref} sets the output voltage of the dummy stage. U_{yQ} sets the remaining outputs to a defined value. It may, however, also be zero or a supply voltage. Note that the transistors of the dummy output should be matched to those of the differential stage for accurate biasing. An example can be found in [129].

A differential stage with fixed source and floating load (see Fig. 4.15(c)) requires the same kind of common-mode voltage comparison with a reference value as the differential stage with floating source and floating load. The bias currents I_Q are again supplied by two current sources. The error voltage is now amplified by a voltage-controlled current source γU_{CM} that sets the bias currents equal to I_Q and the output voltage to U_{ref}. The fixed source U_Q is usually the common-mode voltage component of the signal source, which sets the input voltages to a defined value.

In case of a fixed source and a fixed load, a combination of Figs. 4.15(b) and 4.15(c) is required, as Fig. 4.15(d) shows. The voltages are set by U_Q, U_{yQ}, and U_{ref} respectively. Error current I_e is amplified by αI_e that sets the bias currents to I_Q. For a more elaborate treatise of a systematic way of biasing any active device, including differential stages, the reader is referred to [3][8] or [130].

From an EMI and distortion point of view it should be noted that with these bias schemes some even-order distortion and EMI will be injected into the differential stage since these signals are common mode. Both EMI and distortion behavior will degrade to some extent by common-mode feedback.

The control signal current for biasing is either supplied by the controlled current source at the emitter node (Figs. 4.15(c) and 4.15(d)), or by two controlled current sources at the bases (Figs. 4.15(a) and 4.15(b)). The first option is the worst from an EMI and distortion point of view, since now the bias current I_T ($I_T = \gamma U_{CM}$ or $I_T = \alpha I_e$) will not only be a DC value, but will also have a component at ω_l. The latter signal is injected in both transistors and the mixing effect discussed in Section 4.3 will occur, deteriorating the SER. In the

second option (Figs. 4.15(a) and 4.15(b)), the ω_l component is a common-mode signal at the input of the differential stages and, hence, is suppressed. Since common mode suppression is not infinite, a small deterioration of EMI can still be expected. This is most easily checked during simulation of the design.

Beside the controlled sources, the independent current sources I_Q are important since unequal currents in the differential stage have an adverse effect on the EMI behavior. Therefore some additional remarks on the bias current circuitry are given next.

A. Bias current circuitry

Current sources can be realized by using a (supply) DC voltage and converting it to a current by means of a transadmittance amplifier. The voltage and the feedback resistance R_E determine current I_T delivered by the current source. The active part of the amplifier can be implemented by one or more transistors.

A straightforward way to realize a (controlled) high impedance current source, is to use or design a transistor to be used in the current source with a low collector-base junction capacitance and reverse bias this junction with an as large as possible voltage in order to reduce C_μ as much as possible. The output impedance is given by $z_{out} = r_{out}/(1 + j\omega r_{out}(C_\mu + C_{js}))$ [3], with $r_{out} \approx r_o(1 + g_m R'_e)$, r_o being the output resistance of the BJT and R'_e being the shunt of R_E and r_π. Capacitance C_{js} is the junction capacitance from the collector to the substrate in case of a monolithic npn BJT. A similar discussion holds for FETs.

To obtain a current source with a very high output resistance (e.g., ≥ 10 MΩ), it can be implemented with a cascode instead of a single transistor [2]. Now, $r_{out} \approx (1 + g_m R'_e) r_{oCA}$ and a dominant pole is found at $p \approx -1/((1 + g_m R'_e) 2 r_o (C_\mu + C_{js}))$. This pole is usually located at a lower frequency than in case of the non-cascode current source implementation. A non-dominant pole and a zero can be found at higher frequencies. The impedance at high frequencies (e.g., ≥ 100 MHz) is typically comparable to that of the non-cascode current source implementation. Using a cascode is therefore only beneficial in those cases where the interfering frequencies are relatively low.

When current sources with a very high output resistance have to be realized with submicron FETs with low r_{ds}, a multistage implementation of the active part may be necessary. The output resistance may than be approximated by the product of the loop gain and r_{ds}.

On top of these methods, the designer may decide to add a series impedance in the output of the implemented current source, to increase the total output impedance of the current source at high frequencies. An alternative is to add an inductor in series with feedback resistor R_E of the controlled current source implementation. When the active part of the current source is a cascode, the inductor forms a parallel LC circuit with capacitance C_π. In a limited frequency band very high values of Z_T can expected due to the high impedance of a parallel LC circuit at resonance. However, due to bulkiness and the far from ideal behavior of inductors, care should be taken when using them.

Current sources I_Q should be equal as much as possible, since they have to supply the same currents. These current sources are usually realized with (special forms of) current mirrors. The simplest form of a BJT current mirror has a 'mirrored' current equal to $1/(1+\frac{2}{\beta_{ac}})$ and a pole at half the transit frequency [3] in case the collector-emitter voltages are equal. The limited value of β_{ac} will limit the equality of the currents in the current mirror; e.g., a β_{ac} of 100 will produce an inequality of 2 %. By increasing the loop gain in the current mirror, the accuracy of the current mirror improves.

On top of these limitations, mismatch of the transistors and inequality in the collector-emitter voltages occur. Due to mismatches in the saturation current I_s, that may typically range from
$\pm$ 1 % to $\pm$ 10 % depending on geometry [57], and the (possibly) considerable differences in U_{ceQ} the accuracy of the mirror action is further impaired (Early voltage). Improvement can be obtained by cascoding the transistors, thus reducing the adverse effect of the Early voltage.

By means of series feedback (applying emitter resistances) the effects of mismatches in I_s and U_{ceQ} can be reduced. When $g_m R_E \gg 1$, inequalities in I_s can be neglected [57] and the effects of inequalities in U_{ceQ} are reduced by the loop gain, $1+g_m R_E$ [66], R_E being the emitter degeneration resistance value. Note that the improvement is determined by the ratio of the DC voltage across R_E and the thermal voltage $(n_f kT)/q$. An improvement by a factor 10 requires a voltage drop across R_E of $9(n_f kT)/q \approx 230$mV. The maximal improvement that can be obtained in this way is limited to a factor β_{ac} [66].

Under these conditions the error in the mirrored current can be obtained with [57],

$$\begin{aligned} \frac{\Delta I_{cQ}}{I_{cQ}} &\approx \frac{g_m R_E}{\alpha_{Fac}+g_m R_E}\left(-\frac{\Delta R_E}{R_E}+\frac{\Delta \alpha_{Fac}}{\alpha_{Fac}}\right) \\ \alpha_{Fac} &= \frac{\beta_{ac}}{1+\beta_{ac}}, \end{aligned} \tag{4.47}$$

where the 'ΔX' parameters are the mismatch parameters given by $\Delta X = X_1 - X_2$ (e.g., $\Delta I_{cQ} = I_{cQ1} - I_{cQ2}$, $\Delta R_E = R_{E1} - R_{E2}$), and the other parameters are average parameters determined by $\frac{1}{2}(X_1+X_2)$ (e.g., $I_{cQ} = 0.5(I_{cQ1}+I_{cQ2})$). Q_1 and Q_2 are the transistors of the current mirror, and R_{E1} and R_{E2} are their respective emitter degeneration resistances.

The mismatch in current gain β_{ac} may be significant. It can easily be on the order of 10% for discrete devices. The resistances used to implement R_E usually have better matching properties than transistors. Resistor mismatch depends on geometry and typically ranges from $\pm$ 0.1 % to $\pm$ 2 %. For example, in case of $\pm$ 2 % mismatch in R_E of 1 kΩ, $\pm$ 10% mismatch in β_{ac} (β_{ac}= 100), and g_m being 40 mA/V, a mismatch in currents in the current mirror of $\approx \pm$ 2 % is found.

Current mirrors can also be realized with FETs. Care should be taken to ensure saturated FETs. In contrast with BJT current mirrors, no errors due to DC gate current exists. Due to channel length modulation, current errors caused by unequal drain-source voltages are generally larger compared to the

BJT current mirror. By cascoding or applying series feedback this error can be reduced.

From Reference [57] the error in the currents of the current mirror is taken. Although not explicitly noted in [57] this equation only holds when the channel length modulation effect has been made ineffective.

$$\frac{\Delta I_{dQ}}{I_{dQ}} = \frac{\Delta \frac{W}{L}}{\frac{W}{L}} - \frac{2\Delta U_t}{U_{gsQ} - U_t} \tag{4.48}$$

The current mismatch consists of two components. The first is dependent of the width, W, and the length, L, of the FET and contributes a fractional current mismatch that is independent of its bias point. The second is dependent on the threshold voltage mismatch, ΔU_t, and increases as the overdrive $U_{gsQ} - U_t$ is reduced.

In discrete amplifier design, it is often seen that current sources are implemented with resistors. The current-controlled current sources should, however, not be realized with a resistor since due to the expected relatively low value (several kΩ) the EMI behavior of the differential pair will be severally impaired. The same holds when implementing the uncontrolled current sources providing I_Q with resistors. Although resistors may provide the right currents, a twofold adverse effect may occur when applied in a negative-feedback amplifier. Firstly, the loop gain may be reduced by the moderate values of the resistors. Secondly, due to the same moderate values, a subsequent BJT stage may become voltage driven instead of current driven and hence the EMI behavior of the negative-feedback amplifier will be affected. This is discussed more elaborately in Chapter 5.

4.6.3 Transistor matching

An elaborate treatise of device mismatch modelling in differential stages is beyond the scope of this work. The interested reader is revered to specialized literature, e.g., [131]. This subsection will only present some general ways to improve device matching.

In general, differences between devices can be kept small by giving them large (effective) areas. For instance, the differences in saturation current $I_{s1,2}$, and therefore differences in $U_{beQ1,2}$ or $I_{cQ1,2}$, can be made small by making the emitter areas relatively large with respect to the mask inaccuracies. Placing devices close to one another and giving them the same orientation is also beneficial to minimize differences between them. Common centroid layout [131][57] will often also reduce mismatch, since it is possible to ensure that both devices share the same centroid and that they are symmetrical.

Mismatch in MOSFETs is related to an area term $\sim 1/\sqrt{WL}$ [132], with W and L being the width and length of the MOSFET, respectively. A large area thus improves transistor matching. It should be noted, however, than in case of β_{FET} (and U_t) mismatch for equal area devices, a wide channel device with short channel length (large W/L ratio) has poorer matching than an equal area narrow channel transistor with relatively long channel length (small W/L ratio).

This difference in matching can be as much as 300% [132]. Also, it seems to be beneficial to bias submicron MOSFETs at such a high voltage that velocity saturation occurs. Due to this 'intrinsic feedback mechanism', less current mismatch than predicted by $\sim 1/\sqrt{WL}$ occurs [133]. Biasing in this region has, however, other drawbacks as discussed in Chapter 3.

4.7 Conclusions

The non-ideal behavior of active devices may be improved by, e.g., cascoding and balancing techniques resulting in an odd symmetric input output characteristic, as in the differential stage.

A cascode of active devices provides an unilateral input output transfer, increases the output impedance, neutralizes the Miller effect, and nullifies the effects of the cross term transconductance g_x and nonlinear output conductances. The nonlinear behavior of the transconductance (g_{m2}) is not affected.

Even-order nonlinearity is, ideally, absent in differential stages and thus second-harmonic distortion and EMI do not occur. Ideal differential stages do not exist and their nonlinear behavior is also affected by their surroundings. Non-ideal behavior of differential stages has been modelled and equations for linear and second-order nonlinear behavior have been presented, as well as design rules for minimizing second-order nonlinearity.

The transistors are preferably current driven and current loaded for low second-order nonlinearity. Current drive is especially beneficial in the case of a BJT differential stage. Current loading is beneficial for either type of transistor.

It has been found that the impedance of (controlled) current sources for biasing of the differential stage should be much larger than the input impedances of the differential stage itself. second-order nonlinearity is then minimized, even at high frequencies. Also the bias currents through the devices should be as equal as possible for low second-order nonlinearity, since the adverse effect of current unbalance on second-order nonlinearity is generally larger than that of device inequality. Some design rules for realizing (matched) current sources and devices were also given.

Chapter 5

Design of EMI-resilient single-stage amplifiers

It is well known that all amplifier types suffer from distortion. Less known, however, is that all amplifiers, including negative-feedback amplifiers, are to a certain extent susceptible to interfering out-of-band signals from the environment called electromagnetic interference (EMI).

Distortion in negative-feedback amplifiers has been investigated previously (e.g., [58][59][60][96] [118][134] [135]) and also EMI effects have been investigated by others, e.g., [122][136][123][137][138] [121][139]. Much is known about designing low distortion amplifiers already. The research of EMI effects in negative-feedback amplifiers mainly concentrated on operational amplifiers. Apart from analyzing EMI effects in operational amplifiers, some research for ways of designing them with increased EMI immunity has also been performed, and operational amplifier designs with increased EMI immunity have been presented (e.g., [123][136][138][121][139][125]). EMI immunity of operational amplifiers can be increased by using a completely balanced topology [123][136], or by increasing the immunity of the differential input stage (e.g., [125][120]).

The design of application-specific negative-feedback amplifiers with low EMI susceptibility is underexposed. Some design rules are presented in [43], but a detailed design method is not given. Of course, the earlier mentioned ways to decrease EMI susceptibility in operational amplifiers may also be used in application-specific negative-feedback amplifiers. However, other design aspects, such as the type of feedback, loop gain, etc., and their effects on EMI susceptibility should also be taken into account.

A design methodology for obtaining application-specific negative-feedback amplifiers with an adequate EMI immunity is presented in this work. Because it is an extensive subject, the methodology for the design of single-stage negative-feedback amplifiers is discussed in this chapter. The methodology for the design of dual-stage negative-feedback amplifiers and a general discussion about the design of negative-feedback amplifiers with a specified signal-to-error ratio are

presented in Chapter 6. The methodology can, to a large extent, also be used to design negative-feedback amplifiers with low second-harmonic distortion, because second-harmonic distortion and EMI effects are closely related.

This chapter starts with a generic discussion on error reduction techniques and systematic design of negative-feedback amplifiers with specified noise and bandwidth behavior in Sections 5.1 and 5.2. A model for analyzing both linear and second-order nonlinear behavior of single-stage negative-feedback amplifiers is presented in Section 5.3. Design rules for single-stage amplifiers with low envelope detection behavior (and some design examples) are presented in Sections 5.4 and 5.5. Finally, some conclusions are given.

5.1 Error reduction techniques

The objective of error reduction techniques is to improve the linearity of the desired amplifier transfer. Errors can be reduced by compensation, error feedforward and negative feedback [2]. Each of these techniques or combinations of them can be used to improve the quality of the amplifier transfer. Error reduction techniques have to be used to prevent the signal-to-error ratio (SER) from becoming too low.

5.1.1 Compensation

Compensation of amplifying stages (transistors) and amplifiers is commonly used to correct for errors due to offset, nonlinearity, inaccuracy, drift, and temperature dependence [8]. Two types of compensation can be distinguished: additive and multiplicative compensation.

Stages are combined to convert the nonlinear input-output relation into odd symmetry input-output relations in case of additive compensation. The differential stage (also called anti-series stage) and the complementary parallel stage (e.g., class AB stage) are examples of stages using additive compensation. With identical or complementary devices and identical biasing, it is possible to obtain proper compensation. Practical devices, however, are not exactly identical, nor is the biasing. As a result the compensation is not ideal and some even-order nonlinearity remains. This results in EMI susceptibility and the production of even harmonics. The resulting amount of second-order nonlinearity in the differential stage can be estimated using the equations given in Chapter 4.

Multiplicative compensation uses a compensation network in cascade with the amplifying stage. In order to accomplish compensation, the compensation network should have an input-output relation that is the inverse of the amplifying stage. This method has limited use since it depends on reproducibility and predictability of the transistor properties, that are usually not known accurately enough. The current mirror may be regarded as an example of multiplicative compensation[1]. Multiplicative compensation is beyond the scope of this work.

[1] The input current is transferred to a base-emitter voltage that logarithmically (ln) depends on that current by one BJT. This voltage is multiplied by the exponential relation between

Compensation of amplifiers can be used to increase EMI immunity. Reitsma [43] demonstrated a low-power microphone preamplifier for hearing instruments with increased EMI immunity by subtracting the output signals of two low-power transconductance amplifiers. Both transconductance amplifiers are designed for low distortion [140] and are subjected to the same interference. The signal from the microphone, however, is connected to only one of the amplifiers. As a result of the subtraction, the resulting EMI is small, while the amplified microphone signal is not affected. As a result the signal-to-error ratio (SER) is increased with respect to the uncompensated amplifier. In that particular design, on average, compensation attenuates the detected signal by 22 dB between 1 GHz and 4 GHz.

5.1.2 Error feedforward

The technique of error-feedforward obtains an error signal by comparing an accurately known fraction of the output of a device with the input signal and passes the resulting error signal through an error amplifier that is similar to the first. Finally, both output and amplified error signals are subtracted to obtain a corrected output signal. This technique seems attractive, but it can be difficult to implement and is therefore restricted to some special cases only [8]. Error feedforward is therefore not considered in this work.

5.1.3 Negative feedback

When a fraction of the output variable (or an internal one [8]) is used to modify an input of the system, there is feedback. If it occurs in such a way that the difference between the fraction that is fed back and the input signal is nullified, it is called negative feedback. The higher the loop gain, the smaller the difference becomes. When the loop gain approaches infinity the difference goes to zero.

Due to the feedback, the transfer from input to output is hardly affected by errors originating from the active devices. Negative feedback also affects the input and output impedances. Therefore, it is possible to prevent errors originating from the source and load impedances by proper selection of the negative-feedback configuration.

Practical negative-feedback amplifiers do not have infinite loop gain. Negative feedback, however, remains a very powerful error reduction technique. It can even be regarded as the most powerful method of error reduction, because it is independent of balancing or component matching and yet has the potential to reduce the errors to zero.

Two classes of amplifiers using negative-feedback can be distinguished: general purpose amplifiers (operational amplifier, operational transconductance amplifier, current differencing/Norton amplifier) and the dedicated amplifier. The general purpose amplifier is applicable to a wide range of source and load

base-emitter voltage and collector current to a linear output current by another BJT.

impedances and feedback factors with minimal risk of becoming unstable. General purpose amplifiers are usually internally compensated such that (approximately) a first-order roll-of in the frequency behavior is obtained [62] so that the chance of instability is minimized.

Designing with general purpose amplifiers is usually very easy, but there are some drawbacks. Firstly, the noise performance will seldom be optimal for the specific application for which the general purpose amplifier is used. Secondly, feedback is usually limited to parallel feedback at the output (voltage sensing) using passive negative-feedback networks only, since commercially available general purpose amplifiers only have one output port.

Dedicated amplifiers are designed for a specific source, load and feedback factor. The order of the frequency behavior can be larger than one, because the impedances of the source and load are (or should be!) better known. The frequency behavior may therefore be second or even third order. Higher order behavior will almost always result in instability and should therefore be avoided.

Dedicated amplifiers can be optimized for noise performance and all types of negative-feedback networks can be applied without difficulty. In general, the dedicated amplifier will have better performance than a general purpose amplifier. A disadvantage is that the design effort is larger than for a general purpose amplifier.

Besides the direct negative-feedback discussed thus far, indirect negative-feedback also exists. The output quantity is sensed indirectly and/or the input quantity may be compared indirectly by means of a dummy stage. Indirect negative-feedback amplifiers may be found in low-voltage circuits [8]. Indirect feedback is beyond the scope of this work.

A. Types of negative-feedback amplifiers

Voltages are measured by connecting the measurement device (in this case the feedback network) in parallel with the load Z_l. This type of voltage sensing thus results in parallel feedback at the output. Currents are measured by connecting the feedback network in series with Z_l. Current sensing thus results in series feedback at the output.

The source voltage and the feedback voltage are subtracted by connecting the feedback network in series with the input, thus generating the difference signal. The source current and the feedback current are subtracted by connecting the feedback network in parallel with the input.

It is common practice to name a type of feedback after the way the feedback network is connected to the input and output. If we limit ourselves to a single-loop feedback network there are four possibilities: series-series, series-parallel[2], parallel-series and parallel-parallel feedback. The first series or parallel term in the name corresponds to the subtraction at the input, and the second series or parallel term corresponds to the sensing at the output.

Source, load and feedback networks have to be connected to an active part

[2]In literature also 'shunt' is used instead of parallel.

that can supply power to the load and can 'do' something with the difference signal. As a theoretical component suited for design, the nullor is used [141][2][3].

The nullor consists of a coupled nullator and norator. The nullator is a fictitious component that by definition has zero voltage difference between its terminals while no current flows through it. The norator (also fictitious) can generate any arbitrary value of voltage across its terminals and current through it. Because of the defined properties of nullator and norator they can be used as a pair to form a two-port (the nullor), which can act as the active part of a negative-feedback amplifier. Figure 5.1 shows the symbols of the nullor, the nullator, and the norator.

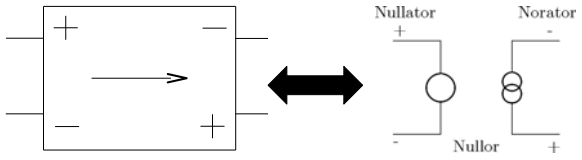
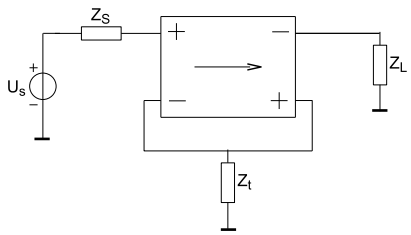
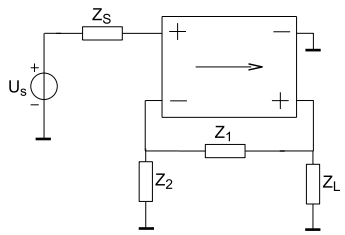


Figure 5.1: The nullor.

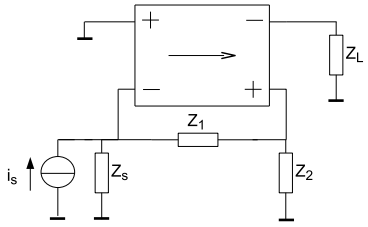
The nullor represents an active part having infinite gain under all drive and load conditions. To make the gain finite, feedback has to be applied. The norator then adapts its output in such a way that the port constraints of the nullator are met.



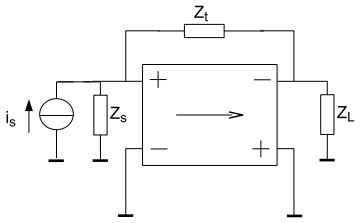
(a) Transadmittance amplifier



(b) Voltage amplifier



(c) Current amplifier



(d) Transimpedance amplifier

Figure 5.2: The four possible single-loop negative-feedback amplifiers using one ports and nullors. More complicated feedback networks (e.g., 'π' or 'T') are possible also, but not shown for simplicity.

Figure 5.2 shows nullors with all four types of single loop negative feedback. Firstly, we have series-series feedback. The output current through the load is measured and converted to a voltage that is compared to the voltage of the signal source. The nullor adapts its output current so that the voltage to be compared will exactly equal the voltage of the signal source (otherwise the port constraints are violated). The transfer from input to output is thus a transadmittance; an input voltage is accurately 'transferred' into an output current. This type of amplifier is thus called a transadmittance amplifier. Often, this type of amplifier is called transconductance amplifier. Since the transfer may have a real and imaginary part, thus is not restricted to conductance only, the more general name admittance will be used in this work.

Following the same reasoning it is found that series-parallel feedback results in the voltage amplifier, parallel-series feedback results in the current amplifier, and parallel-parallel feedback results in the transimpedance amplifier. For the same reason as given earlier for the transadmittance amplifier, in this work the name transimpedance amplifier is used instead of transresistance amplifier.

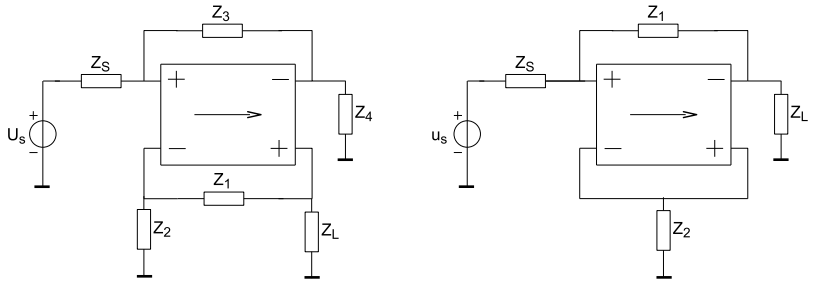
The input impedance and output impedance of these negative-feedback amplifiers are either infinite or zero. Series feedback results in infinite input and output impedance, while parallel feedback results in zero input and output impedance. The transadmittance amplifier is realized with series-series feedback and therefore has both infinite input and output impedance, and the voltage amplifier has series-parallel feedback around the nullor, resulting in an infinite input impedance and zero output impedance. The same straightforward reasoning gives zero input impedance and infinite output impedance for the current amplifier and zero input impedance and zero output impedance for the transimpedance amplifier.

Note that Figure 5.2 shows the feedback network realized with impedances. It is however not restricted to impedances. Non-energic feedback is possible, too. Feedback with non-energic linear one-ports result in a short circuit. Applying this to the voltage amplifier and current amplifier results in the voltage follower and current follower, i.e., the voltage gain respectively current gain equals one. The ideal transformer and gyrator are non-energic two-ports and can be used to realize voltage and current negative-feedback amplifiers (using a transformer) and transimpedance and transadmittance amplifiers (using a gyrator). The practical transformer is a rather poor approximation of the ideal transformer, but it can be used. The gyrator does not exist as a passive network. For the investigation of negative feedback amplifiers using ideal transformers and gyrators we therefore refer to specialized literature [2].

There are two kinds of negative-feedback amplifiers using dual-loop negative feedback realized with impedances [2]. The input impedance depends on the load impedance, and the output impedance depends on the source impedance of these negative-feedback amplifiers.

Figure 5.3(a) presents a configuration of which both voltage gain and current gain are determined by the feedback loops. The transimpedance is also accurately determined. An accurate input impedance can be realized when the

load impedance is accurately known or infinite; an accurate output impedance can be realized when the source impedance is accurately known or infinite. This configuration is used, for example, for realizing an accurate and linear low-noise damping resistance for magneto-dynamic transducers, e.g. [142].



(a) Fixed voltage and current amplifier

(b) Fixed transimpedance and transadmittance amplifier

Figure 5.3: Two possible dual-loop negative-feedback amplifiers using resistive one ports and nullors.

By fixing the transimpedance- and transadmittance, an amplifier is obtained of which the input impedance and output impedance also depends on the load- and source impedance; see Figure 5.3(b). With this configuration also the voltage- and current amplification are accurately fixed [2]. Accurate input and output resistances can be obtained when it holds that $R^2 = Z_1 Z_2$, where $R = R_{in} = R_{out} = R_{source} = R_{load}$. Due to this property this amplifier is suited for use in characteristic impedance matching. It has also been successfully used as a low-noise load to accurately fix the quality factor of a resonator in infra-red telemetry systems [143][144].

Dual-loop feedback offers the possibility to apply negative feedback to one loop and positive feedback to the other loop. An accurately known negative input impedance of the amplifier can now be obtained, that can be used as a low noise undamping circuit for resonators, which can result in low-noise harmonic oscillators [4][7][5]. Positive feedback is, however, beyond the scope of this work. Therefore, neither single-loop nor dual-loop positive-feedback will be considered.

Dual-loop negative-feedback amplifiers can be analyzed and designed using the same approach as for single-loop negative-feedback amplifiers. Therefore, in the remainder of this work only single-loop negative-feedback amplifiers are considered.

5.1.4 Introduction to systematic negative-feedback amplifier design

Negative-feedback amplifier design can best be done using a systematic design approach, which consists of 7 distinguishable steps [3]:

1. The source and load have to be specified in terms of impedance and signal (amplitude, bandwidth, and, e.g., signal-to-noise ratio, distortion, etc.).

2. From this the appropriate type of feedback is selected.

3. The input stage is designed for noise performance.

4. The output stage is designed to minimize clipping distortion.

5. Bandwidth and distortion/EMI performance have now to be checked and

6. Frequency compensation has to be provided.

7. Finally, the bias network is designed.

In exceptional cases, one stage may be capable of meeting both noise specifications and output requirements. If now bandwidth and envelope detection (and distortion) requirements are met also, only the bias circuitry has to be designed and a single-stage negative-feedback amplifier is obtained. Usually, however, a separate input stage and output stage are necessary to meet noise and load driving requirements, simultaneously.

Optimal frequency compensation is achieved by using phantom zero compensation. Usually we compensate to achieve a Butterworth characteristic (having a maximally flat magnitude transfer), since the required location of the poles follows in a straightforward manner from the product of the poles and the loop gain (LP product). On top of that, a Butterworth characteristic may often be required to meet the specifications. Frequency compensation is extensively dealt with in [3].

In case the LP product can not be made sufficiently large to meet bandwidth and/or EMI performance, an intermediate stage can be added to increase the LP product. The biasing constraints of this stage depend on the maximum signal current it has to supply to the output stage. If the bandwidth and distortion/EMI requirements are still not reached, the gain of the negative-feedback amplifier can be reduced, thus lowering the LP product constraints.

It may be the case that bandwidth and distortion requirements are met and still the EMI requirement is not met. In that case it may be necessary to enhance the loop gain further, or to filter the signal before it reaches the input of the amplifier.

The seven design steps will be described in more detail in Section 5.2, Subsections 5.2.1 to 5.2.7. The systematic design approach is extended with three extra steps: (a) estimating the disturbance at the input of the amplifier, (b) determining the value of the equivalent envelope detection source, and (c) adjusting the biasing of the transistors to meet minimal LP product requirements. Step (a) can be done using the methods of Chapter 2. Methods for steps (b) and (c) are presented in Sections 5.3 to 5.5 in this chapter (single-stage amplifiers), and in Sections 6.1 to 6.4 in Chapter 6 (dual-stage amplifiers). A complete overview of the proposed design strategy is finally presented in Section 6.5 in Chapter 6.

5.2 Systematic negative-feedback amplifier design strategy

In this work negative-feedback amplifiers are considered with both signal source and load having one common terminal connected to the reference, i.e., ground, as depicted in Figure 5.2.

As discussed in Chapters 1 and 2, negative-feedback amplifiers are (part of) electronic systems that transport electrical signals carrying information from a source to a load. The goal of negative-feedback amplifiers is to increase the energy level of the signal by multiplying it with a constant. While doing so, the fidelity of the transfer from input to output of the negative-feedback amplifier has to be assured.

It was argued that the fidelity of the transfer may be hampered by errors due to noise, distortion, and interference. Effort has to be made to make the intended signal large compared to these errors. The ratio of the intended signal and the errors, the signal-to-error ratio (SER), can be regarded as a figure of merit of the signal handling performance of an amplifier for a given input signal and electromagnetic environment. An equation for the SER is presented (together with the constraints for its validity) in Chapter 1 (pages 24 and further). For convenience, the equation is repeated here:

$$SER = \frac{S_1}{S_{n,eq} + S_2 + S_3 + S_d + S_{\mathrm{ENV}}}. \tag{5.1}$$

S_1 is the power of the desired signal. The subscript one denotes the first harmonic. $S_{n,eq}$ gives the total power of the noise generated by the negative-feedback amplifier. S_2, S_3 represent the power of the second and third harmonic of the desired signal. Disturbance is represented by S_d for the rms power of a signal in the bandwidth and by S_{ENV} for the rms power of the detected envelope variations from a disturbance (much) higher than the amplifier bandwidth.

Using a systematic or structured design approach SER maximization is accomplished by orthogonalization[3] [3]. Orthogonalization means that different design aspects are optimized independently in such a sequence that they do not affect each other. In practice there will be no true orthogonality, but special measures can, and will be, taken to make the assumption of orthogonality true. For instance, by using input stages with high gain, the noise generated in subsequent stages can be ignored. The noise performance of the negative-feedback amplifier can now be optimized by proper design of the input stage only.

In Subsections 5.2.1−5.2.4, the design steps for meeting the desired amplification with the intended SNR and signal-to-distortion ratio are summarized. For an elaborate treatise of the subject, the reader is referred to [3]. The design steps for meeting the signal-to-disturbance ratio are presented in the following sections.

[3]The discussion about the systematic or structured design strategy of negative-feedback amplifiers is based on the work of several authors: [2][7] and [3]. Many of the discussed design steps are described in all these three references. Since [3] is the latest publication and easily available, this citation will generally be used in this work.

5.2.1 Amplifier specifications

Given an application for the negative-feedback amplifier, the specifications for the amplifier must follow from this application. The source and load are therefore characterized. The source may be a sensor that transfers the physical information into the electrical domain or some kind of physical or chemical process that generates information in the electrical domain, e.g., bio-potentials. Usually the information is best represented by either a voltage or a current. The bandwidth and the amplitude of the signal are determined during the source characterization.

The source impedance is usually not accurately known and might even be nonlinear. By assuring that the amplifier does not significantly load the source, these inaccuracies and nonlinearities do not appear in the transfer.

The characterization of the signal, amplitude and bandwidth, and the source impedance determine the upper value of the SER, i.e., the SNR of the source without noise, distortion or disturbance originating from the amplifier. Equation (5.1) shows that the SER with amplifier and interference can be expected to be lower than the SNR of the source itself. (Note that $S_{n,eq}$ in Equation (5.1) resembles the total noise generated by both the amplifier and the source.) The designer is left with the difficult consideration how much lower the SER may become.

A helpful tool for making this choice may be the noise figure (NF) [2][145], which quantifies the amount that the initial SNR deteriorates due to the errors the amplifier introduces. It may be calculated by taking the sum of the (equivalent) noise powers of the source and the amplifier and dividing this sum by the noise of the source only. Usually its value is given in dB. By also incorporating the error powers of the distortion and disturbance components, NF represents the difference between the initial SNR and the SER: $SER = SNR_{source} - NF$. Upper and lower limits for NF are hard to give in general terms. They depend on the application. For example, in instrumentation design, an NF of 3 dB, i.e., the errors the amplifier introduces are equal in magnitude to the errors originating from the source, may be acceptable, while in RF-design often noise figures smaller than 1 dB are required [146].

When we design for equal contributions of both noise power, (distortion,) and EMI power to NF, and therefore the SER, the most optimal design regarding the SER results. After all, when a lot of design effort is put into low noise design while EMI dominates the SER, this effort is wasted. Similarly, design effort and power is wasted when EMI is designed to be much lower than the noise. Therefore, EMI should have at most the same order of magnitude as the noise.

The load is the actuator that may or may not transfer the signal to another physical domain. If the load is a nonlinear or inaccurately known impedance as well, a correct choice, voltage or current, for driving this impedance with maximum signal fidelity has to be made. Again, the inaccuracies of the load impedances should not occur in the signal transfer. Also the maximal signal level allowed in the load has to be determined.

From the signal source and load specifications follow the bandwidth and the

amplification requirements. The proper type of feedback has to be established next.

5.2.2 Determining the proper type of feedback

Signal sources that can best be approximated as voltage sources should not be loaded with a low impedance, i.e., they should not have to deliver a current since in that case the inaccurate source impedance negatively affects the fidelity of the signal transfer. Therefore, signal sources that behave as voltage sources should be loaded with infinitely high impedances. The amplifier thus has to have series feedback at the input. For signal sources that can best be represented by current sources, the dual situation holds and they should therefore be loaded with infinitely low (zero) impedances. The amplifier should therefore make use of parallel feedback at the input.

Sometimes, e.g., in case of electrically short active antennas, there is no preference for voltage- or current source representation of the signal source. An electrically short antenna can be modelled as a voltage source with a linear capacitive source impedance [147][6][70]. Hence, both open terminal voltage and (short circuit) current accurately represent the received signal. Therefore, the choice for infinite or zero input impedance has to be made on basis of other considerations. The input of an active antenna is usually protected for electrostatic discharge by protection diodes. When an amplifier with infinite input impedance is chosen, for instance a voltage follower, the voltage-dependent and nonlinear diode capacitance has a negative effect on the fidelity of the signal transfer. This is prevented by using an amplifier with zero input impedance [147], for instance a transimpedance amplifier, which is therefore the better choice[4].

Loads that are best driven by voltage sources imply parallel feedback at the output and when they are best driven by currents, series feedback at the output should be used. The output impedance of the negative-feedback amplifier will then go to zero and infinity, respectively.

The type of feedback is now known. The amount of amplification required follows from the signal source amplitude and the maximally allowed signal in the load.

5.2.3 Noise performance

Signals are usually smallest at the input of the amplifier. This is thus the place where noise can have the largest detrimental effect. For this reason, the many noise sources in an amplifier are usually modelled by an equivalent input noise source at the input of the amplifier. In this way, the equivalent input noise can be compared directly with the incoming intended signals and the effect of the noise on those signals is easily determined [57]. The noise performance determines the maximal attainable SER.

[4]The configuration of Fig. 5.3(b) can also be used to avoid power loss at the output.

To reduce the number of amplifying stages contributing to the equivalent noise source of the nullor approximation, and thus to keep the noise level as low as possible, input stages with high gain should be selected. The noise generated in the subsequent stages can then be ignored and the SNR is determined by the source, the feedback network and the input stage.

The type of feedback, and the value of the feedback factor, was determined in the previous phase of the design process. In case of the voltage amplifier and the current amplifier, the impedance level of the feedback network can be freely chosen and can be determined such that its noise contribution is reduced to an acceptable level. This may be at the expense of increased power consumption.

The common emitter (CE) and common source (CS) stages have the largest gain and should therefore be used as input stage [3]. The noise of active devices is represented by both a voltage noise source and a current noise source at the input of the device. Figure 5.4 shows representations of the low frequency noise

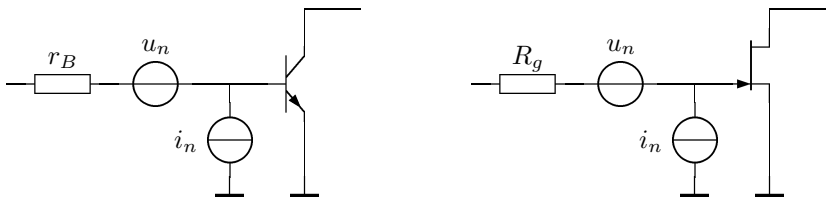


Figure 5.4: Noise models of the BJT and FET respectively. The transistors themselves are modelled by noise free intrinsic transistors.

model of the bipolar junction transistor (BJT) and field effect transistor (FET) respectively [3]. The equivalent noise voltage respectively noise current of the BJT are given by

$$S_{u_n} = 4kT\left(r_B + \frac{1}{2g_{m1}}\right) \tag{5.2}$$

$$S_{i_n} = \frac{4kTg_{m1}}{2\beta_{dc}}\left(1 + \frac{f_l}{f}\right). \tag{5.3}$$

These equations are valid under the assumption that $\beta_{dc} \approx \beta_{ac} \gg 1$ and the highest frequency of interest is much lower[5] than the transit frequency ($\omega \ll \omega_T/\sqrt{\beta_{ac}}$). The constants and variables have the same meaning as in Chapter 3. The corner frequency at which the flicker noise power of the base current noise equals the white noise power is denoted by f_l.

For BJTs, the voltage noise source and the current noise source decrease and increase respectively for increasing collector current, since g_{m1} is proportional to I_{cQ}. A minimum in the noise contribution of the BJT can thus be found.

[5]For higher frequencies, the expression for S_{i_n} becomes more complicated. See [3] in case noise at higher frequencies should be taken into account.

The equivalent noise voltage respectively noise current source of the FET are given by

$$S_{u_n} = \frac{4kTc}{g_{m1}} \left(1 + \frac{f_l}{f}\right) \tag{5.4}$$

$$S_{i_n} = 2qI_{gQ} + \frac{4kTc}{g_{m1}} \left(2\pi f(C_{gs} + C_{gd})\right)^2 \left(1 + \frac{f_l}{f}\right). \tag{5.5}$$

The $4kTc/g_{m1}$ term in both noise sources of the FET origin from the same source; the noise of the drain current. Obviously, there is correlation between the sources. If, as is the case for the MOSFET, the gate current I_{gQ} is negligible, the noise sources are completely correlated. Proportionality constant c was not discussed in Chapter 3. It is a ratio of the channel conductance and the transconductance that depends on the bias voltages of the device. It is common practice, however, to use a single value for it. For FETs in saturation follows for the JFET $c = 2/3$ and for MOSFETs $2/3 \leq c \leq 4/3$ from theory [3]. Practically, c values up to about 2 can be found for MOSFETs [3]. For FETs in weak inversion hold $c = 1/2$.

The gate resistance R_g contributes $4kTR_g$ to the spectral density of the voltage noise. Since the gate is generally made of a highly doped semiconductor or metal, R_g is low and its noise contribution is often negligible.

Both voltage and current noise reduce for increasing drain current. The noise contribution of the FET can thus be decreased at the expense of increased power consumption.

Apart from the CE and CS stage the differential stage also has large gain values, comparable to those of the CE and CS stage. The BJT or FET differential stage can therefore also be used as input stage. The difference is that the spectral noise density of the voltage noise is twice as large, $S_{u_{ns}} = 2S_{u_n}$, and the spectral current noise density is halve as large, $S_{i_{ns}} = S_{i_n}/2$, compared with the spectral noise densities of the CE and CS stage[6].

Both source impedance and the impedance of the feedback network determine the relative contribution of the input transistor noise sources to the total equivalent noise source. The effect of the feedback network on the noise is twofold. Firstly, it generates noise itself with a value corresponding to the real part of the equivalent impedance. In case of series feedback at the input, the (equivalent) impedance of the feedback network is in series with the source impedance as far as noise is concerned, and in case of parallel feedback at the input the (equivalent) impedance of the feedback network is in parallel with the source impedance [3].

Secondly, it enlarges the noise contribution of the nullor implementation. The current noise contribution of the input stage to the equivalent voltage noise of the voltage amplifier and transadmittance amplifier is enlarged (Norton-Thévenin transform). For low noise performance, the (equivalent) impedance of the feedback network should be as low as permitted. For the current amplifier and the

[6]Generally, it holds that connecting n identical devices in series results in an in increase of $S_{u_{ns}} = nS_{u_n}$ and a decrease of $S_{i_{ns}} = S_{i_n}/n$. For the parallel connection of n devices the dual holds, i.e., $S_{u_{np}} = S_{u_n}/n$ and $S_{i_{np}} = nS_{i_n}$ [3].

transimpedance amplifier the dual holds; the voltage noise contribution of the input stage to the equivalent current noise source is enlarged (Thévenin-Norton transform). The (equivalent) impedance of the feedback network should be as high as permitted for low noise performance, in this case.

For the voltage amplifier the equivalent impedance is formed by the parallel connection of feedback impedances Z_1 and Z_2 (see Fig. 5.2). The equivalent impedance of the transadmittance amplifier is formed by feedback impedance $Z_t = 1/Y_t$. For the transimpedance amplifier the equivalent impedance is also formed by the feedback impedance Z_t. In case of the current amplifier, the equivalent impedance is formed by the series connection of feedback impedances Z_1 and Z_2.

The equivalent noise voltage power respectively noise current power is found by integrating the noise power spectra over the bandwidth; $\overline{u_{n,eq}{}^2} = \int_{f_l}^{f_h} S_{u_{n,eq}} df$ [V^2] and $\overline{i_{n,eq}{}^2} = \int_{f_l}^{f_h} S_{i_{n,eq}} df$ [A^2], with f_l and f_h being the lowest and highest corner frequency, respectively. To make the concept of SNR more manageable, $\overline{u_{n,eq}{}^2}$ respectively $\overline{i_{n,eq}{}^2}$ can be used instead of the spectral power density. After all, we are interested in maximizing the power of the intended signals from the source, which should always be within the amplifier bandwidth, with respect to the noise generated within that bandwidth.

5.2.4 Distortion

In Chapter 1, it was shown that three different origins of distortion can be identified. Distortion due to a too small bandwidth leads to frequency or linear distortion. This kind of distortion can be avoided in a straightforward manner: design for a large enough bandwidth. The other two forms of distortion originate from either strong nonlinear behavior originating from too limited voltage and/or current drive capabilities or weak nonlinear behavior of the active devices.

A. Clipping distortion

When used in the nullor approximation of negative-feedback amplifiers, the transistors should remain in their forward active region. Clipping occurs when one or more of the boundaries of the forward active region are crossed. This severe type of distortion results in loss of information and should therefore be avoided at all times.

Clipping distortion can occur in every stage of the amplifier, but it is most likely that it will occur in the output stage where the signals are most often the largest. Depending on the type of negative-feedback amplifier, either the peak voltage or the peak current is specified.

Table 5.1 gives an overview of the bias demands made on the output stage to prevent clipping distortion. The demands depend on the type of feedback used. A negative-feedback amplifier with a voltage output, and thus parallel feedback at the output, has a specified peak voltage that it should be able to deliver. The bias voltage follows in a straightforward manner from $\hat{u}_{out}$ (being

Table 5.1: Bias quantities of the output stage, being a CE stage or a CS stage. The equations are given for an npn BJT and N-channel FET, respectively. It is only a matter of inverting polarities and changing $>$ into $<$ to obtain the equations for the pnp BJT and the P-channel FET.

Feedback type at output	I_{cQ}, I_{dQ}	U_{ceQ}, U_{dsQ}
Parallel	$I_{cQ} = \frac{3}{2}\hat{i}_{out} = \frac{3}{2}\frac{\hat{u}_{out}}{\lvert Z_p(\omega_0)\rvert}$ $I_{dQ} = \frac{3}{2}\hat{i}_{out} = \frac{3}{2}\frac{\hat{u}_{out}}{\lvert Z_p(\omega_0)\rvert}$	$U_{ceQ} > \hat{u}_{out} + U_{ceMIN}$ $U_{dsQ} > \hat{u}_{out} + U_{dsSAT}$
Series	$I_{cQ} = \frac{3}{2}\hat{i}_{out}$ $I_{dQ} = \frac{3}{2}\hat{i}_{out}$	$U_{ceQ} > \hat{i}_{out}R_{series} + U_{ceMIN}$ $U_{dsQ} > \hat{i}_{out}R_{series} + U_{dsSAT}$

the peak output voltage) and the minimal voltage to remain in the active forward region, U_{ceMIN}. Here, U_{ceMIN} is defined to be the collector emitter voltage corresponding to the situation that U_{bc} equals zero, i.e., $U_{ceMIN} = U_{beQ}$.

The impedance of the parallel connection of the feedback network and the load (Z_p) determine the corresponding peak current ($\hat{i}_{out}$) that the output stage has to deliver. At the upper edge of the bandwidth (ω_0) this impedance can be expected to be the lowest (under assumption of a capacitive load) while $\hat{u}_{out}$ may still be considerable. Hence, $\hat{i}_{out}$ should be determined at ω_0. To prevent the occurrence of current clipping (slewing distortion), the output stage should be biased at a current larger than $\hat{i}_{out}$. A good rule for choosing the bias current, is making it equal to $3/2\hat{i}_{out}$. When the maximal current, $\hat{i}_{out}$, is being delivered to $Z_p(\omega_0)$ a current equal to $1/2\hat{i}_{out}$ is still running through the output device, preventing it from becoming too slow due to transit frequency (ω_T) degradation [3].

A negative-feedback amplifier with a current output (series feedback at the output), has a specified peak current it should be able to deliver to the load. The bias current follows from the previous discussion to prevent current clipping and ω_T degradation. Consequently, the peak voltage needs to be determined.

The peak voltage is determined by the series connection of the load impedance and the impedance of the feedback network (Z_{series}), and $\hat{i}_{out}$. The output voltage of the amplifier is thus lowest when the impedances have the highest values, usually at the lower edge of the bandwidth. As worst case approximation the series resistance of the feedback and load can be used: R_{series}.

Although less likely, the stage driving the output stage could suffer from clipping distortion also. The driving stage must be able to supply enough current to ensure the output stage of being able to supply $\hat{i}_{out}$ to the load. Hence, it should be able to deliver the peak base or gate current, both at low frequencies and at ω_0. A bias current 1.5 times this peak current can be chosen. The voltage that the driver has to deliver to the output stage is usually very small, e.g., ≤ 10 mV, and therefore it follows straightforward that the driver stage can be biased at a non critical voltage $U_{ceQ} > U_{ceMIN}$ and $U_{dsQ} > U_{dsSAT}$, respectively.

Note that the driver stage can both be the input stage and the intermediate stage. The bias current of the input stage is determined on basis of noise requirements. As long as this bias current meets the criterium of $I_{Q,driver}$, which it usually does, it can drive the output stage without problems.

As shown, clipping distortion can be prevented by appropriately biasing of the output (and intermediate) stage. This does not affect the design of the input stage, i.e., the design steps of the input stage (noise) and clipping distortion (output stage) are orthogonal.

B. Weak nonlinear distortion

At this stage of the design procedure clipping is prevented and only weak nonlinear and frequency distortion may still occur. Assuring a large enough bandwidth to prevent frequency distortion is treated in Subsection 5.2.6. Here, weak nonlinear distortion is treated.

In Chapter 3 the weak nonlinear behavior of both BJT and FET was described. It was found that for low nonlinear behavior, the BJT is preferably current driven (and loaded) and biased in the mid-current region, and that the FET should be current loaded with an impedance smaller than about $0.1r_{ds}$. Cascoding the FET is a straightforward way to accomplish this. From the discussion in Chapter 3, it can be concluded that *the total nonlinear behavior demonstrated by an active device not only depends on its initial nonlinear behavior but also on the impedances connected to it.*

The weak nonlinear input−output relation results in harmonic distortion (Chapter 1) and intermodulation distortion [134][44]. With an input voltage of $u_i = \hat{u}_i \cos(\omega t)$ an active device with a nonlinear input voltage-output current relation generates an output current equal to

$$\begin{aligned} I_o =& I_O(U_{DC}) + \left(\frac{1}{2}g_{m2}\hat{u}_i^2 + \frac{3}{8}g_{m4}\hat{u}_i^4 + \cdots\right) + \\ & \left(g_{m1}\hat{u}_i + \frac{3}{4}g_{m3}\hat{u}_i^3 + \frac{5}{8}g_{m5}\hat{u}_i^5 + \cdots\right)\cos(\omega t) + \\ & \left(\frac{1}{2}g_{m2}\hat{u}_i^2 + \frac{1}{2}g_{m4}\hat{u}_i^4 + \cdots\right)\cos(2\omega t) + \\ & \left(\frac{1}{4}g_{m3}\hat{u}_i^3 + \frac{5}{16}g_{m5}\hat{u}_i^5 + \cdots\right)\cos(3\omega t) + \cdots \end{aligned} \tag{5.6}$$

Here, in contrast to Chapter 1, the Taylor coefficients are already replaced by the transconductance terms g_{mn}. Apart from the component at ω, harmonic distortion components are also generated.

The nth harmonic distortion component is defined as the ratio of the component of frequency $n\omega$ to the one at the fundamental, ω [134]. From Equation (5.6), $HD_2 = \hat{u}_i \frac{g_{m2}}{2g_{m1}}$ and $HD_3 = \hat{u}_i^2 \frac{g_{m3}}{4g_{m1}}$ are found. The second order harmonic distortion is proportional to u_i and the third-order harmonic distortion to u_i^2. Another way for looking at distortion is by using intercept points [3]. We will not elaborate on this.

Inspecting Equation (5.6) further, it is seen that the intended signal at ω is not only determined by g_{m1}, but also by the odd order nonlinear terms of the transconductance. Input signal u_i is usually smaller than 1V. It can therefore be expected that $\frac{3}{4}g_{m3}\hat{u}_i^3 \gg \frac{5}{8}g_{m5}\hat{u}_i^5 + \cdots$. The intended transconductance can thus be approximated as being deteriorated by the third-order term only: $i_{o1} \approx \left(g_{m1}\hat{u}_i + \frac{3}{4}g_{m3}\hat{u}_i^3\right)\cos(\omega t)$. In general, g_{m3} can have the same or the opposite sign as g_{m1}. The value of i_{o1} can thus be larger or smaller than expected. This is called gain expansion respectively gain compression [44].

The gain compression/expansion ratio is the ratio of the actual magnitude of the fundamental response to the magnitude that would have existed in case of perfect linearity [44]. The compression/expansion point is the $\hat{u}_i$ for which the gain is compressed or expanded by 1 dB or 3 dB. Both points are used in practice. The k dB (k is ± 1 dB or ± 3 dB) compression/expansion point can be found with $CP_{kdB} = \sqrt{\left|\frac{4}{3}\left(10^{\frac{k}{20}} - 1\right)\frac{g_{m1}}{g_{m3}}\right|}$. The 1 dB expansion point for the BJT is about 25.6 mV and the 3 dB expansion point is about 47.0 mV. Note that when the recommended maximal $\hat{u}_i$ of 10 mV is used, the corresponding amount of expansion is only approximately 0.16 dB.

For low distortion behavior the relative current swing, i.e., the ratio of I_o and the bias current I_Q [134], should be small. The relative current swing is also called signal-to-bias ratio [59][60]. Reduction of the relative current swing is possible by increasing the bias current of a current driven BJT. In the mid-current region, the nonlinearity, and hence weak distortion, is low. A doubling of I_{cQ} thus lowers the relative current swing by a factor two for a given input current, reducing the distortion even further.

In the voltage driven case there is 'g_m distortion' [7]. The relative current swing in FETs can be decreased by increasing I_{dQ}, since g_{m1} increases approximately with the square root of I_{dQ} and g_{m2} hardly changes with I_{dQ}. For a given input voltage the current swing decreases by a factor of approximately $\sqrt{2}$ when I_{dQ} is doubled.

The relative current swing of a voltage driven BJT can not be reduced by increasing the bias current. For example, consider the output current of a voltage driven BJT, biased at 1mA and at 2mA, respectively. The analysis of the output current is limited to the first three harmonics. An I_{cQ} of 1 mA results in $g_{m1} = 38.6$ mA/V, $g_{m2} = 0.74$ A/V^2, and $g_{m3} = 9.6$ A/V^3, and for an I_{cQ} of 2 mA, it follows $g_{m1} = 77.2$ mA/V, $g_{m2} = 1.48$ A/V^2, and $g_{m3} = 19.2$ A/V^3. For an input voltage of 5 mV this results in the first case in $i_o = 193\mu + 9.25\mu + 300n = 202.55\mu$A. The relative current swing is 0.203. In the second case we have for the same input voltage $i_o = 386\mu + 18.50\mu + 600n = 405.1\mu$A. The relative current swing is, again, 0.203. The only possibility of reducing the relative current swing, and thus the g_m distortion of the voltage driven BJT is by reducing the input voltage.

Application of the sum of two cosine waveforms at ω_1 and at ω_2 and amplitudes $\hat{u}_{i1}$ and $\hat{u}_{i2}$ gives rise to output signal components at ω_1, ω_2 and their

multiples. When nonlinearities above the third-order are neglected we find:

$$\begin{aligned} I_o =& I_O(U_{DC}) + \frac{1}{2}g_{m2}\left(\hat{u}_{i1}^2 + \hat{u}_{i2}^2\right) + \\ & \left(g_{m1}\hat{u}_{i1} + \frac{3}{4}g_{m3}\hat{u}_{i1}^3 + \frac{3}{2}g_{m3}\hat{u}_{i1}\hat{u}_{i2}^2\right)\cos(\omega_1 t) + \\ & \left(g_{m1}\hat{u}_{i2} + \frac{3}{4}g_{m3}\hat{u}_{i2}^3 + \frac{3}{2}g_{m3}\hat{u}_{i1}^2\hat{u}_{i2}\right)\cos(\omega_2 t) + \frac{1}{2}g_{m2}\hat{u}_{i1}^2\cos(2\omega_1 t) + \\ & \frac{1}{2}g_{m2}\hat{u}_{i2}^2\cos(2\omega_2 t) + \frac{1}{4}g_{m3}\hat{u}_{i1}^3\cos(3\omega_1 t) + \\ & \frac{1}{4}g_{m3}\hat{u}_{i2}^3\cos(3\omega_2 t) + g_{m2}\hat{u}_{i1}\hat{u}_{i2}\{\cos(\omega_1+\omega_2)t + \cos(\omega_1-\omega_2)t\} \\ & + \frac{3}{4}g_{m3}\hat{u}_{i1}^2\hat{u}_{i2}\{\cos(2\omega_1+\omega_2)t + \cos(2\omega_1-\omega_2)t\} + \\ & \frac{3}{4}g_{m3}\hat{u}_{i1}\hat{u}_{i2}^2\{\cos(2\omega_2+\omega_1)t + \cos(2\omega_2-\omega_1)t\} \end{aligned} \tag{5.7}$$

Apart from the two linear responses and their harmonics, terms at sum and difference frequencies can be found, i.e., the intermodulation products. The second-order nonlinearity gives rise to intermodulation terms at $\omega_1 \pm \omega_2$ and the third-order nonlinearity to intermodulation terms at $2\omega_1 \pm \omega_2$ and $2\omega_2 \pm \omega_1$.

Second-order intermodulation distortion (IM_2) is defined by the ratio of the component at frequency $\omega_1 \pm \omega_2$ to the one at ω_1 or ω_2 [134]. Under the assumption of $\hat{u}_i = \hat{u}_{i1} = \hat{u}_{i2}$, $IM_2 = \frac{g_{m2}}{g_{m1}}\hat{u}_i$ is found. Likewise, third-order intermodulation (IM_3) is defined by the ratio of the component at frequencies $2\omega_1 \pm \omega_2$ and $2\omega_2 \pm \omega_1$ to the one at ω_1 or ω_2. Under the same assumption of equal signal amplitudes it yields $IM_3 = \frac{3}{4}\frac{g_{m3}}{g_{m1}}\hat{u}_i^2$.

Comparison of HD_2, HD_3, IM_2 and IM_3, shows that $IM_2 = 2HD_2$ and $IM_3 = 3HD_3$. There is a one-to-one correspondence between harmonic and intermodulation distortion. It is thus sufficient to specify only one of them [134].

It is possible that two high-frequency signals generate a response at $\omega_1 - \omega_2$, $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ that may be in the pass band of an amplifier. Therefore, this will be addressed in Subsection 5.2.5.

The discussion sofar is related to the individual components. In negative-feedback amplifiers however, the linear and nonlinear behavior depends on the contribution of the various active devices to the linear and nonlinear transfer, and the signal levels in these devices. Also, the domain of the signal can be of importance.

For example, a cascade of CE stages made to approximate a nullor in an amplifier with series feedback at the input has a voltage comparison at the input. The input CE stage is therefore voltage driven and its nonlinear behavior is determined by the nonlinearity of its transconductance. If the following stage is current driven it contributes only the small β_{ac} nonlinearity to the overall nonlinearity. The latter can be reduced by increasing the bias current of the stage, thus reducing the relative current swing [7] due to the input current

delivered by the preceding stage. The following stage is current driven when its input impedance is much smaller than the output impedance of the input stage[7]. The impedance mismatch between the two active stages should therefore be as large as possible.

The nonlinear behavior of the input stage is not affected by increasing its bias current; the relative current swing is given for a given input voltage. There is, however, a positive effect of increasing the bias current of the input stage. The transconductance g_{m1} increases linearly with I_{cQ}. As a result the 'loop gain' of the negative-feedback amplifier increases, which results in a decrease of the input voltage of the CE stage. Of course, an increase in loop gain also reduces β_{ac} distortion as the input current of the current driven stage is reduced. The concept of loop gain and its beneficial effects on distortion and EMI susceptibility will be extensively dealt with in the following sections.

The negative-feedback amplifier shows a linear transfer from input to output with a magnitude determined by the feedback factor. The second-order and third-order nonlinear behavior of the negative-feedback amplifier are determined by its second-order and third-order nonlinearity factors. These factors give the total second-order respectively third-order nonlinearity from the input to the output terminals of the output stage. In case of the series feedback amplifier mentioned earlier, the input is the base-emitter voltage of the input stage and the output is the collector current of the output stage.

Both second-order nonlinearity factor D_2 and third-order nonlinearity factor D_3 are frequency dependent in multiple stage negative-feedback amplifiers. This will be shown in Section 6.1, where the frequency dependency of D_2 is investigated in detail. The HD_2 and HD_3 of the amplifier may therefore differ for different frequencies and equal input signals.

The input signal of a negative-feedback amplifier is represented by E_s which can be either a voltage or a current, depending on the application. For the load signal the same holds and is therefore called E_l. The signal in the load is now $E_l(\omega) \approx E_s A_t(\omega) + \frac{1}{2}E_s^2 A_{t2}(\omega) + \frac{1}{4}E_s^3 A_{t3}(\omega)$, where $A_t(\omega)$ is the frequency dependent linear transfer, $A_{t2}(\omega)$ is the second-order nonlinearity and $A_{t3}(\omega)$ is the third-order nonlinearity of the negative-feedback amplifier. In this work, all errors are compared at the input to the input signal. Therefore the distortion components in the output have to be transferred to an equivalent signal source at the input of the negative-feedback amplifier, which is further regarded being linear.

For the equivalent second-order respectively third-order distortion input signal, it follows that

$$E_{s2}(\omega) = \frac{1}{2}E_s^2 \frac{A_{t2}(\omega)}{A_t(\omega)} = \frac{1}{2}E_s^2 \frac{c_1(\omega)D_2(\omega)}{A_t(\omega)} \tag{5.8}$$

$$E_{s3}(\omega) = \frac{1}{6}E_s^3 \frac{A_{t3}(\omega)}{A_t(\omega)} = \frac{1}{6}E_s^3 \frac{c_2(\omega)D_3(\omega)}{A_t(\omega)}. \tag{5.9}$$

The powers of $E_{s2}(\omega)$ and $E_{s3}(\omega)$ are used to determine the signal-to-distortion ratio, which is obviously frequency dependent. Coefficients $c_1(\omega)$ and $c_2(\omega)$ are

[7]The output impedance of an active stage is shunted by the impedance of the bias circuitry. The impedance of the bias circuitry should therefore be made as large as possible

frequency dependent transfers from the signal source to the input of the input device. Here, it is only possible to give qualitative guidelines for low distortion design, since a method to determine $A_t(\omega)$, $A_{t2}(\omega)$, and $A_{t3}(\omega)$ is not presented yet. In the discussion about design of negative-feedback amplifiers with specified EMI behavior, guidelines will be given that facilitate qualitative and quantitative measures. In general, the design method presented there can be adapted to low distortion design also.

Signal levels in the nullor approximation are smallest at the input and largest at the output. When the output is loaded by a shunt impedance the relative current swing in the output stage increases, resulting in increased distortion. Apart from the load and feedback network impedance (in case of parallel feedback), no additional impedances are therefore allowed to shunt the load. In case of series feedback at the output, impedances shunting the load increase the relative current swing in the output stage also. This will increase distortion. On top of that, the accuracy of the transfer from input to output is hampered, since the output current of the amplifier is not exactly equal to the current delivered to the load.

Note that an excessively low impedance of the feedback network will increase the distortion when we have parallel feedback at the output. The feedback network affects both noise and distortion. From this it follows that in case of a voltage amplifier, complete orthogonality can only be assumed when the source impedance is much higher than $Z_1//Z_2$ (see Fig. 5.2 (b)), and $Z_1 + Z_2$ is much higher than Z_l. Specifically the latter demand is not always possible to meet without sacrificing the first. In case of a transimpedance amplifier, noise and distortion behavior cannot be affected in an orthogonal way by altering the feedback impedance. Increasing the transimpedance Z_t (see Fig. 5.2 (d)) simultaneously improves the noise behavior and lowers the loading of the output stage. Lack of orthogonality does not complicate the design of this amplifier.

At this stage of the design process, however, the feedback impedances are already determined. The possible effects of the feedback impedances are only discussed for demonstration purposes.

Trying to prevent a large relative current swing by adding an impedance in series with the load, in case of parallel feedback at the output, is not an option. To reach the specified amplitude of the load voltage, the voltage gain or transimpedance now has to increase. Apart from the resulting decrease in loop gain, we also have the same relative current swing in the output stage again.

In case of series feedback at the output, an additional impedance in series with the load may decrease the loop gain[8] and, in case of a FET output stage, the nonlinearity of the output resistance may become more prominent. On top of that, a larger voltage swing is necessary to deliver the current to the load, which may result in a higher supply voltage. In summary, series or shunt impedances at the output of a negative-feedback amplifier should be avoided.

Series and shunt impedances at the input of active devices in a negative-

[8] When the output resistance of the output stage remains much higher than the additional series impedance, the decrease may be negligible.

feedback amplifiers, e.g., in an attempt to decrease the distortion, should likewise be avoided. Although the use of series impedances with CE stages seems beneficial because it will be 'more' current driven, the adverse effects of the accompanying reduction in loop gain will outweigh this positive effect [2]. This, will also be elucidated in the next sections.

A more elaborate, similar qualitative discussion regarding the effects of shunt and series impedances on amplifier distortion can be found in [2].

The effects of local feedback in addition to global feedback on distortion are, in contrast to common opinion, not beneficial [60][3]. Though the stage with local feedback may be linearized more, it can be shown that the distortion of the other stage(s) increases and the overall loop gain decreases. This, also, will be investigated in more detail in Section 6.1.

Apart from the increase in distortion, applying local feedback to the input stage of a negative-feedback amplifier will also increase the total noise generated by the amplifier due to the additional noise contribution of both the local feedback impedance and the increased noise contribution of the subsequent stage to the total noise [7]. When very carefully applied, local negative-feedback applied to the output stage may, as an exception to the rule, slightly reduce second-order distortion (see Section 6.1) [60]. This reduction is slight and usually not worth the increased design effort.

The application of local feedback stages in negative-feedback amplifiers should be limited to increasing the performance of stages (e.g., cascoding) in the nullor approximation with respect to bandwidth requirements or for improving the linearity of the stage, e.g., FET-BJT and FET-FET cascode. In other cases it should be avoided.

Concluding, the active part can best be realized with CE, CS and differential stages that may be cascoded. Increasing the bias current of these stages will increase the loop gain and generally decrease the relative current swing. On top of that, specifically when the stage(s) succeeding the input stage is a BJT, it is beneficial to try to keep its output impedance much higher than the input impedance of the following CE stage, thus lowering the contribution of the second CE stage to the total nonlinearity of the negative-feedback amplifier.

5.2.5 Interference

In Chapter 2 it was shown that interference may be coupled into the input of negative-feedback amplifiers. As a result an extra disturbing voltage source is generated in series with the intended signal voltage source and an extra disturbing current source is generated in parallel with the intended signal current source, respectively. When the disturbing signal lies in the bandwidth of the amplifier, it is processed as if it were the intended signal, subject to the same limitations as the intended signal. It can not be distinguished from it. The only way to avoid intolerably large errors due to this disturbance source is by reducing its value. This is accomplished by decreasing the effectiveness of the coupling path to the amplifier.

Disturbing signals with frequencies higher than the bandwidth may also be reduced by decreasing the effectiveness of the coupling path to the amplifier, decreasing the susceptibility of the amplifier or by filtering at the input of the amplifier. The first option has been investigated in Chapter 2. The latter option should be applied with care. The impedances of the filter network may affect the noise performance of the negative-feedback amplifier adversely and also hamper stability. On top of that, in order to be able to design an effective filter, the effects of the out-of-band signals on the amplifier behavior should be known.

The effects of small disturbing signals with frequencies higher than the bandwidth have been investigated in Chapter 1. The main conclusion is that envelope detection occurs, i.e., DC shifts and low-frequency envelope variations of the carrier wave are present at the output of the amplifier. Envelope detection is troublesome and it may, like noise, also be modelled as an equivalent signal source at the input of the negative-feedback amplifier, that is now thought to be linear.

A design method will be presented in the following sections to minimize the adverse effects of envelope detection. It is believed that the design considerations given are also beneficial for the design of low distortion amplifiers, although third-order nonlinearity is not explicitly dealt with.

Large disturbing signals have the same effect as large intended signals; they may result in clipping and/or slew-rate induced distortion. Clipping due to large disturbing signals should be avoided by either increasing the clipping levels of the negative-feedback amplifier or by decreasing the disturbing signal.

If the disturbing signal contains frequency components ω_1 and ω_2 much higher than the bandwidth, a frequency component in the amplifier pass band may be generated due to intermodulation (see Equation (5.7)). In order to generate a difference frequency in the amplifier pass band, the difference of ω_1 and ω_2 should be within the pass band. Moreover, as the disturbing frequencies increase, the frequency separation between the two signals has to become smaller in order to generate a signal in the pass band. It therefore becomes less likely that a spurious signal will be generated in the pass band of the amplifier for increasing frequency of the disturbance.

For example, when we have a negative-feedback amplifier with a bandwidth of 1Mrad/s (assuming low pass response), the difference of ω_1 and ω_2 should be smaller than, or maximally equal to, 1Mrad/s. For an ω_1 of 10Mrad/s, this means that ω_2 may be maximally 10% higher or lower in frequency. When ω_1 is 100 Mrad/s, ω_2 may only be <1% higher or lower.

If a spurious signal in the amplifier pass band does occur due to intermodulation, it is most likely that it will be generated by the second-order nonlinearity of the negative-feedback amplifier [148]. Its amplitude and deteriorating effect on the SER may be calculated using the same approach as for envelope detection, which will extensively dealt with in the following sections. Apart from that, it may be expected that the design method to be presented for negative-feedback amplifiers with low susceptibility to envelope detection will also decrease errors from disturbing intermodulation.

It should be noted that for disturbing frequencies near the upper edge of the bandwidth, both envelope detection and linear transfer of the disturbing signal occurs. The linear transfer can be expected to dominate in that case. For increasing frequency, envelope detecting starts to dominate. Whether or not the linear transfer near the upper band edge is troublesome (or not) depends on the application of the negative-feedback amplifier. If the disturbing signal is (a little) higher than the bandwidth it may be possible to filter it out.

5.2.6 Bandwidth

Thus far, the design process (may have) resulted in an input stage for which the bias requirements are determined from noise calculations, and an output stage for which the biasing is determined from clipping distortion requirements.

Now, it should be checked whether or not the bandwidth requirement is met. The feasible bandwidth can be estimated by calculating the DC loop gain and poles that result from the negative-feedback amplifier. The nullor is approximated by the cascade of the hybrid-π models of both input an output stages.

The bandwidth with n (real) poles follows from the product of the poles and the DC loop gain, the so-called loop-gain-poles product (LP product) [3]:

$$B = \sqrt[n]{LP} \tag{5.10}$$

The bandwidth to be met determines a minimum value of the LP product. When it is too low, the required bandwidth will never be reached. Note that it may occur that not all poles can be moved in bandwidth determining positions. These poles are called non-dominant poles. In general, it can be determined whether a pole is dominant by checking if the sum of the loop poles is less negative than the sum of the closed loop poles [127][3]:$\sum_{i=1}^{n} p_{li} \geq \sum_{i=1}^{n} p_{si}$ with p_{li} being the loop poles and p_{si} being the closed loop or system poles.

Bandwidth, weak-distortion and EMI behavior are not orthogonal, since all three requirements depend on the LP product. Measures to increase the bandwidth will affect distortion and EMI behavior. However, since measures to increase the bandwidth usually lead to an increase in the loop gain, both distortion and envelope detection will decrease. It is therefore not a drawback that optimization of these three negative-feedback amplifier properties is not orthogonal. As will be shown later, measures to force the dominant poles in, e.g., Butterworth positions, also positively influence envelope detection and distortion.

When the bandwidth requirement is met, this does not automatically mean that the EMI requirement regarding envelope detection is met. It is possible that the latter specification is not met and that the loop gain has to be increased to meet the EMI requirement. Therefore, in addition to the design method described in [3], the envelope detection is checked and measures to improve it are taken at this point in the design process. The preferred method is to increase the LP product to a sufficient value.

In the next sections, a method is presented to determine the necessary LP product. Because the bias currents of the stages appear in the resulting equations, these can be used to determine the bias currents necessary to obtain the

specified EMI behavior. Usually the bias current of (one of) the stages has to be increased. Increasing the bias current of the output stage has as side effect that the current clipping level increases. An increase in input stage bias current may reduce its noise contribution further (FET), but may also increase it (BJT). The increase is usually small for reasonable increases of BJT bias current.

5.2.7 Bias circuitry

The last phase of the design process is providing the active stages with the necessary bias currents and voltages. Care has to be taken not to decrease the loop gain. Generally this means that currents have to be provided by current sources. Providing bias currents via a resistor to the power supply (which is particularly common practice in discrete amplifier design) may have two drawbacks. The first, and most severe drawback, is that the loop gain decreases. The second drawback may occur in case of BJT stages; due to the bias resistor the 'mode' of operation of the BJT may change from current driven to voltage driven, resulting in increased nonlinear behavior. So, using bias resistors is only allowed when the designer is convinced distortion and EMI susceptibility do not increase unacceptably.

Several methods exist to realize voltage sources. A voltage source may, e.g., be realized by means of a voltage divider connected to the power supply or by forcing a constant current through a resistor thereby generating a voltage. The impedance of the voltage sources may be lowered at signal frequencies of interest by means of parallel capacitances.

An extensive treatise of the systematic biasing of amplifiers is beyond the scope of this work, but can be found in [3] and [130].

5.3 Envelope detection in single-stage negative-feedback amplifiers

Evaluating envelope detection in negative-feedback amplifiers is simpler when fewer nonlinear active parts are used in the nullor approximation. Since the single-stage negative-feedback amplifier is a one stage nullor approximation, it is the simplest negative-feedback amplifier. It is therefore used as a starting point for a design methodology for negative-feedback amplifiers with specified envelope detection properties. Much of the method presented in this section has been published earlier [116].

To come to a simple method for describing the second-order nonlinear effects (i.e., envelope detection, second harmonic distortion), we introduce an equivalent signal source at the input of the negative-feedback amplifiers which accounts for these effects [149][10], under the condition that no clipping occurs. The amplifier can now further be regarded as being linear.

To determine the equivalent signal source in case of single-stage negative-feedback amplifiers, the transfer of the input signal source to the base-emitter

or gate-source voltage has to be determined first. The resulting equivalent base-emitter or gate-source voltage can then be transferred to an equivalent source at the input of the amplifier. The asymptotic gain model [2] can be used for this. The asymptotic gain model is based on the superposition model [2], under the assumption of the gain going to infinity. Figure 5.5 shows this model.

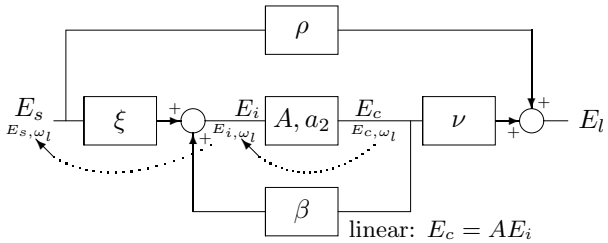


Figure 5.5: Asymptotic gain model. Dotted lines show the transfers from the demodulated signal to an equivalent signal source at the input.

The linear transfer of the active part is represented by A [3], and the second-order transfer by a_2. Its linear output is $E_c = E_i A$. As the signals can be both voltages or currents, they are denoted by E. From the output of the controlled source there is a feedback action to the input, represented by β. Signal source E_s delivers a signal to E_i. Loading effects of E_s are represented by transfer ξ. Transfer ν accounts for loading of A when delivering signal to the load. Any direct signal transfer from the source to the load is represented by ρ. Transfers ρ, ξ, β and ν can readily be determined by using superposition: $\rho = \left.\frac{E_l}{E_s}\right|_{E_c=0}$, $\xi = \left.\frac{E_i}{E_s}\right|_{E_c=0}$, $\beta = \left.\frac{E_i}{E_c}\right|_{E_s=0}$, and $\nu = \left.\frac{E_l}{E_c}\right|_{E_s=0}$.

The following equations are derived from the model:

$$E_i = E_s\xi + E_i A\beta \tag{5.11}$$

$$E_l = E_s\rho + E_i A\nu \tag{5.12}$$

Note that in case of a *single-stage* negative-feedback amplifier E_i is u_{be} or u_{gs} and A becomes the transconductance factor g_{m1} of the transistor[9].

The transfer from E_s to E_l can now be derived to be:

$$A_t = \rho + \nu\xi\frac{A}{1 - A\beta}. \tag{5.13}$$

[9]In case of a multistage negative-feedback amplifier (with and without local feedback), the expression for A becomes more complicated. See Subsection 6.1.

The superposition model will become the asymptotic gain model if the loop gain becomes infinite ($A\beta \to \infty$). The transfer function is then given by [2][3]:

$$A_t = \rho \frac{1}{1 - A\beta} + A_{t\infty} \frac{-A\beta}{1 - A\beta}, \tag{5.14}$$

where $A_{t\infty}$ is referred to as the asymptotic gain.

In all practical amplifier designs the first term in this equation will be much smaller than the second and can therefore be neglected. In case of a high loop gain $A\beta$, the transfer is determined by the feedback network only [3] and $A_{t\infty}$ can be regarded as the inverse of the feedback factor. The expression for the E_l to E_s related transfer is in reality a function of frequency, with all transfers being a function of frequency themselves. In this case $A_t(\omega)$ can be written as

$$A_t(\omega) = A_{t\infty} \frac{-A\beta(\omega)}{1 - A\beta(\omega)}. \tag{5.15}$$

Output E_c will contain a demodulated component at ω_l when there is an high frequency out-of-band disturbing signal (ω_c) with a low frequency varying envelope (ω_l) present at the input:

$$E_{c,\omega_l} \approx a_2 \frac{\hat{E}_i^2}{2} \left(1 + \frac{m^2}{2}\right) + a_2 \hat{E}_i^2 m \cos(\omega_l t) + a_2 \frac{\hat{E}_i^2}{4} m^2 \cos(2\omega_l t). \tag{5.16}$$

Term m is the modulation depth. Equation (5.16) is similar to the first equation of Table 1.3, and therefore the same considerations hold (see Chapter 1, page 19).

The amplitude of the DC component is maximally 3/4 of that of the component at ω_l. Both the DC component and ω_l term may deteriorate the SER. This is, however, only the case when DC is within the information band. When this is not the case, the DC component does not deteriorate the SER. Therefore, in most cases it can be expected that the spurious response at ω_l is the most detrimental one. The design measures taken to minimize the spurious response at ω_l are equally effective on the response at DC. The discussion will, however, concentrate on the response at ω_l.

So, as a result of the nonlinear behavior of the active part, there is a signal $E_{c,\omega_l}(\omega_c)$ with a frequency ω_l, that depends on frequency ω_c. $E_{c,\omega_l}(\omega_c)$ has to be related to an equivalent signal source $E_{s,\omega_l}(\omega_c)$. The latter can be compared directly with the noise and the intended in-band signal, to determine the SER. E_{s,ω_l} can be determined in two steps. Firstly, an equivalent E_{i,ω_l} is determined that would cause the same E_{c,ω_l} in case the active part would be linear. That is easily accomplished, since for a specific value of E_{c,ω_l} a related value of E_i (E_{i,ω_l}) can be found using the linear relation A between input and output. Secondly, this source is recalculated to an equivalent source E_{s,ω_l} at the input of the amplifier, which is possible since Fig. 5.5 shows a clear relation between E_s and E_i. In Figure 5.5 this is indicated with dotted arrows. Note that $E_{s,\omega_l} \cdot A_{t,\omega_l}$ will cause the same amplitude of the envelope detected signal in the load as would

be obtained with $E_{c,\omega_l} \cdot \nu_{\omega_l}$, under assumption that $\rho(\omega_l)$ is much smaller than the second term in (5.13).

An equation for E_{s,ω_l} will be derived for an active part consisting of a FET or a BJT, respectively. Note that the model presented in Figure 5.5 and the equations presented assume a second-order nonlinearity that solely depends on E_i. This is the case when the active part is a cascoded FET, with which we therefore will start the analysis.

Considering the spurious response at ω_l, for E_{c,ω_l} we can write

$$E_{c,\omega_l}(\omega_c) = E_i(\omega_c)^2 m a_2 + E_{c,\omega_l}(\omega_c) A \beta_{\omega_l} \tag{5.17}$$

The first part of this equation follows in a straightforward manner from the second-order nonlinearity of the active part. The second part is due to the fact that $E_{c,\omega_l}(\omega_c)$ is presented to the input E_i again by the feedback factor β_{ω_l}, after which this part is amplified with a factor A. After some straightforward mathematical manipulation for $E_{c,\omega_l}(\omega_c)$, it is found that its value depends on the loop gain at ω_l:

$$E_{c,\omega_l}(\omega_c) = E_i(\omega_c)^2 m a_2 \frac{1}{1 - A\beta_{\omega_l}}. \tag{5.18}$$

If the transfer of the active part is now assumed to be linear, the demodulated signal can be assumed to be the result of an equivalent signal at its input.

$$E_{i,\omega_l}(\omega_c) = E_i(\omega_c)^2 m \frac{a_2}{A} \frac{1}{1 - A\beta_{\omega_l}} \tag{5.19}$$

E_i for a linear amplifier for any arbitrary frequency can be calculated with [3]:

$$E_i(\omega) = E_s \frac{\xi(\omega)}{1 - A\beta(\omega)} = E_s \chi(\omega) \tag{5.20}$$

The ratio $\frac{\xi}{1-A\beta}$ is important in this work, so it has been given the symbol χ.

Combining (5.19) and (5.20) gives the relation between $E_{i,\omega_l}(\omega_c)$ and $E_s(\omega_c)$. Using Equation (5.20) again at ω_l, the equivalent signal source E_{s,ω_l} can now be derived to be:

$$E_{s,\omega_l}(\omega_c) = E_s^2 \chi(\omega_c)^2 m \frac{a_2}{A} \frac{1}{\xi_{\omega_l}}. \tag{5.21}$$

When the active part is a BJT, the effects of the the nonlinear input impedance of the BJT should also be incorporated in the equations. Therefore, an extra transfer is added to the superposition model that is only active at ω_l. The transfer is called γ_{ω_l} (see Chapter 4). For the BJT, i_{ω_l} is given by $i_{\omega_l} = g_{\pi_2} \hat{u}_{be}^2$. Transfer γ_{ω_l} is the impedance that transfers the current from current source $g_{\pi_2} \hat{u}_{be}^2$ to a voltage ($\hat{u}_{be}(\omega_l)$). Incorporating γ into Equation (5.17) results in an $E_{c,\omega_l}(\omega_c)$ given by

$$E_{c,\omega_l}(\omega_c) = E_i(\omega_c)^2 m a_2 + E_{c,\omega_l}(\omega_c) A \beta_{\omega_l} + E_i(\omega_c)^2 g_{\pi_2} A \gamma_{\omega_l} m. \tag{5.22}$$

After some straightforward mathematical manipulation along the same lines as the previous considerations, for $E_{s,\omega_l}(\omega_c)$, it can now be found:

$$E_{s,\omega_l}(\omega_c) = E_s^2 \chi(\omega_c)^2 m \frac{(a_2 + g_{\pi_2}\gamma_{\omega_l} A)}{A} \frac{1}{\xi_{\omega_l}} \tag{5.23}$$

Since a_2 and $g_{\pi_2}\gamma_{\omega_l}$ have opposite signs their sum may become small. This may be the case when the negative-feedback amplifier has parallel feedback at the input. In that case, $a_2 \approx g_{\pi_2}\gamma_{\omega_l}$ and the second-order nonlinearity may approach zero. With series feedback at the input, γ_{ω_l} may become a small value. As a result a_2 will dominate the second-order nonlinearity.

For convenience, a second-order nonlinearity term D_2 is introduced. In case of a FET, $D_2 = \frac{a_2}{A}$ and in case of a BJT $D_2 = \frac{(a_2 + g_{\pi_2}\gamma_{\omega_l} A)}{A}$. In general $E_{s,\omega_l}(\omega_c)$ is given by

$$E_{s,\omega_l}(\omega_c) = E_s^2 \chi(\omega_c)^2 m D_2 \frac{1}{\xi_{\omega_l}} \tag{5.24}$$

The value of the equivalent source E_{s,ω_l} can be decreased by decreasing E_s^2 and by decreasing $\chi(\omega_c)^2$. $\chi(\omega_c)^2$ can be decreased by increasing the loop gain $A\beta(\omega)$, for instance by increasing A. When the active part is a FET, an increase in A may give an extra reduction of E_{s,ω_l} because a_2 does not strongly depend on A.

Due to the frequency dependency of $\chi(\omega_c)^2$ exclusively, the amplitude of the detected envelope will vary for different carrier frequencies. For design purposes it is therefore required to know the frequency dependent behavior of $\chi(\omega_c)^2$.

Note that this method is related to the Volterra approach [44][94], which characterizes the response of a weakly nonlinear system by taking the linear and nonlinear transfers into account and adding the results [44]. However, when circuits other than extremely simple ones are analyzed with the Volterra approach, the algebraic representation becomes very complex [60], which hampers design. The method presented here is (relatively) simple and suited for a design approach. It only takes the linear and the nonlinear response at ω_l into account[10]. This approximation is allowed since the intended signal and the detected signal are much larger than the (intermodulation) products from the signal, disturbance, and noise (see also Subsection 1.7.1 and [43]).

5.3.1 Frequency dependency of the nonlinear behavior of a single-stage negative-feedback amplifier

In the previous section, it has been shown that D_2 is multiplied with the square of the disturbing signal and $\chi(\omega_c)^2$. The frequency dependency of $\chi(\omega_c)$ thus has a large effect on EMI susceptibility (and distortion) and will therefore be investigated. For describing the frequency dependency the Laplace operator ($s = j\omega$) will be used.

[10]The same holds for the dual-stage negative-feedback amplifiers models in Chapter 6 and the differential stage models in Chapter 4.

$\chi(s)$ is determined by the ratio of $\xi(s)$ and $1 - A\beta(s)$ and will therefore show a frequency dependent value, resulting in a frequency dependent value of the equivalent input signal source. Here, the frequency dependency of $\chi(s)$ will be investigated using single-stage representations of the nullor in the negative-feedback amplifier. The transfer is assumed to have two time constants that may result in a first or second-order transfer[11].

Figure 5.6 shows the four single-loop negative-feedback amplifiers using resistive one ports in the feedback network. The active part is represented by a voltage-controlled current source and an input and output impedance. It is comparable to the small-signal model of a FET with linear output resistance (a cascoded FET) or a differential pair (both with C_{gd} neglected for simplicity). Further, each amplifier has a signal source which is assumed to be resistive, represented by resistor R_s and a load represented by resistor R_l and parallel capacitor C_l, which is typical for practical amplifiers.

When the transfers $\beta(s)$ and $\xi(s)$ are determined, the same poles are found for both transfers. $\beta(s)$ does not have zeros in case of parallel feedback at the output, i.e., the transimpedance and voltage amplifier. Transfer $\xi(s)$ however, does have a zero (z_ξ) in all cases and $\beta(s)$ has a zero (z_β) in case of series feedback at the output, i.e., in case of the transadmittance and the current amplifier. Zero z_β is determined by the load (R_l and C_l) and is located near or coincides with the pole due to C_l.

The locations of the poles may be determined exactly, but usually it is much easier to estimate them [3]. To simplify the coming analysis, we assume that for transimpedance and current amplifiers the source and/or feedback resistance(s) are much larger than load R_l. For voltage amplifiers, an R_1 larger than R_2, and for transadmittance amplifiers an R_l smaller than R_t are assumed. The influence of R_s on the location of the pole does not dominate in these cases. Table 5.2 gives the resulting approximate expressions for the poles and zeros z_ξ and z_β, for each amplifier in Figure 5.6. It is assumed that $|p_l| < |p_i|$. When $|p_i| < |p_l|$ different equations result for the poles and z_ξ [116]. The expression for z_β remains the same as given in Table 5.2.

Due to the fact that $|p_l|$ and $|z_\xi|$ are located at (nearly) the same frequency, they tend to cancel each other, which results in a first-order transfer for $\xi(s)$. Transfer $\beta(s)$, however, remains second-order in case of parallel feedback at the output and also reduces to a first-order transfer in case of series feedback at the output, since $|p_l|$ and $|z_\beta|$ cancel.

Table 5.3 presents some important results that may apply to a (single stage) negative-feedback amplifier. It lists equations for the bandwidth (ω_0) of $A_t(s)$, for $\chi(s)$, the maximum value of $\chi(s)$ and the frequency at which it occurs, i.e., χ_{max} and ω_{max}, respectively. The equations for χ_{max} in the first and second rows are valid in case that $|p_l|$ is located at a lower frequency than $|p_i|$. Transfer $\chi(s)$ will equal $\chi_0 = \xi_0/(1 - A\beta_0)$ at low frequencies, and its value will increase due to either p_l or z_ξ that occurs in the numerator, up to ω_{max} where its maximum

[11] The following discussion is based on a similar discussion given in [116] with some additional remarks.

Table 5.2: Approximate locations of the poles and zeros z_ξ and z_β in case $|p_l| < |p_i|$

	p_i(rad/s)	p_l(rad/s)	z_ξ(rad/s)	z_β(rad/s)
Transimp. amp.	$-\frac{1}{(R_s//R_t)C_i}$	$-\frac{1}{((R_l//r_o)//(R_t+R_s))C_l}$	$-\frac{1}{(R_l//r_o//R_t)C_l}$	–
Voltage amp.	$-\frac{1}{(R_s+R_1//R_2)C_i}$	$-\frac{1}{((R_l//r_o)//(R_1+R_2))C_l}$	$-\frac{1}{((R_l//r_o)//(R_1+R_2))C_l}$	–
Current amp.	$-\frac{1}{(R_s//(R_1+R_2//r_o))C_i}$	$-\frac{1}{(R_l//(r_o+R_2//(R_1+R_s)))C_l}$	$-\frac{1}{(R_l//(r_o+R_1//R_2))C_l}$	$-\frac{1}{R_lC_l}$
Transadm. amp.	$-\frac{1}{(R_s+R_t//r_o)C_i}$	$-\frac{1}{(R_l//(r_o+R_t))C_l}$	$-\frac{1}{(R_l//(r_o+R_t))C_l}$	$-\frac{1}{R_lC_l}$

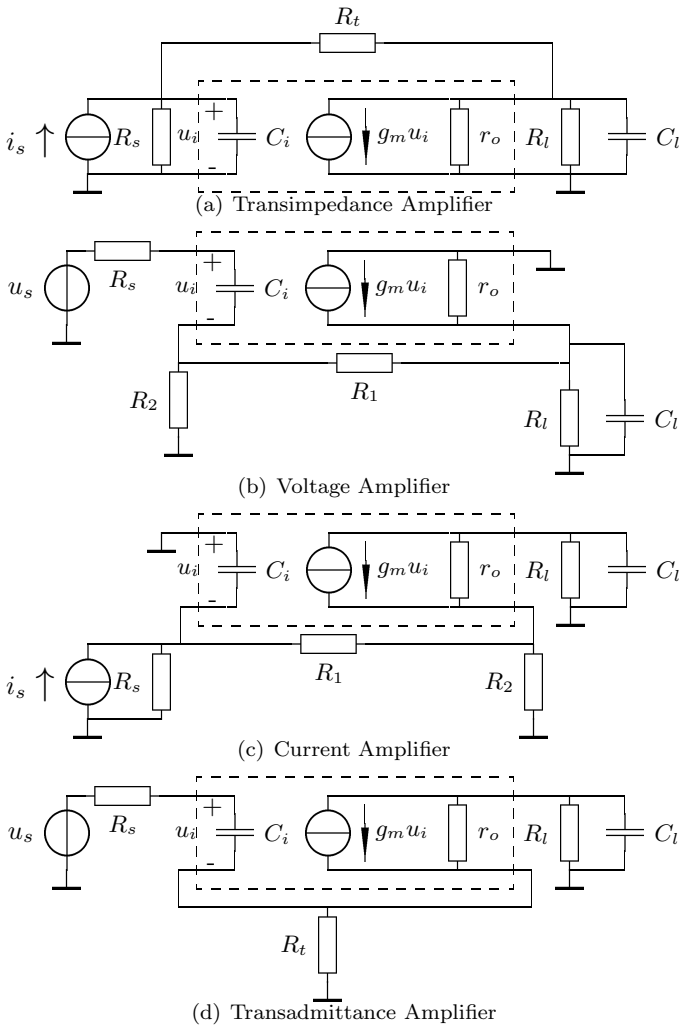


Figure 5.6: The four possible types of single-loop negative-feedback amplifiers using resistive one ports. The active part is comparable to the hybrid-π model of a (cascoded) FET or differential pair.

(χ_{max}) is reached.

When $|p_i|$ is located at a lower frequency than $|p_l|$, the equations for $\beta(s)$, $\xi(s)$ and $\chi(s)$ remain the same. The difference is the location of the zero (due to p_l) in $\chi(s)$. This zero is now located at a frequency higher than $|p_i|$ or even ω_0. If the zero is located relatively near ω_0, its influence is visible in an increase of $\chi(\omega_0)$, which is less than in case $|p_l| < |p_i|$. When it is located relatively far from ω_o, e.g. $|z| \approx 5\omega_0$, its effect is negligible and a flat transfer up to the upper

Table 5.3: Transfer χ of a single-stage negative-feedback amplifier. The effect of two poles (either one or both being dominant) and of a zero in ξ (present or not) are taken in to account.

Parallel feedback at the output						
			Bandwidth	χ		
z_ξ	p_l	p_i	ω_0	$\chi(s)$	$\omega_{max} \approx$	$\chi_{max} \approx$
no	d	d	$\sqrt{p_l p_i (1-A\beta_0)}$	$\xi_0 \frac{p_l p_i \left(1-\frac{s}{p_l}\right)}{s^2 - s\left(p_l + p_i - A\beta_0 \frac{p_l p_i}{z_{ph}}\right) + p_l p_i (1-A\beta_0)}$	ω_0	$\frac{\chi_0}{2\zeta}\sqrt{\frac{{\omega_0}^2+{p_l}^2}{{p_l}^2}}$
yes	d	d	$\sqrt{p_l p_i (1-A\beta_0)}$	$\xi_0 \frac{p_i p_l \left(1-\frac{s}{z_\xi}\right)}{s^2 - s\left(p_l + p_i - A\beta_0 \frac{p_l p_i}{z_{ph}}\right) + p_l p_i (1-A\beta_0)}$	ω_0	$\frac{\chi_0}{2\zeta}\frac{\omega_0}{z_\xi}$
no	d	nd	$(1-A\beta_0)p_l$	$\xi_0 \frac{p_l p_i \left(1-\frac{s}{p_l}\right)}{s^2 - s(p_l+p_i) + p_l p_i (1-A\beta_0)}$	$\sqrt{\omega_0 \lvert p_i \rvert}$	$\chi_0 \frac{\omega_{max}^2}{p_l(p_i+p_l)}$
yes	d	nd	$(1-A\beta_0)p_l$	$\xi_0 \frac{p_i p_l \left(1-\frac{s}{z_\xi}\right)}{s^2 - s(p_l+p_i) + p_l p_i (1-A\beta_0)}$	$\sqrt{\omega_0 \lvert p_i \rvert}$	$\chi_0 \frac{\omega_{max}^2}{z_\xi(p_i+p_l)}$
Series feedback at the output						
			Bandwidth	χ		
z_ξ	p_l	p_i	ω_0	$\chi(s)$	$\omega_{max} \approx$	$\chi_{max} \approx$
no	no	d	$(1-A\beta_0)p_i$	$\frac{\xi_0 p_i}{-s+(1-A\beta_0)p_i}$	0	χ_0

band edge results; χ_{max} equals χ_0 in this case. The effect of the pole locations, $|p_l| < |p_i|$ and $|p_i| < |p_l|$, respectively, on $\chi(\omega)$ and $E_{s,\omega_l}(\omega)$ is demonstrated in Section 7.1 and in [116].

Two closed loop poles originate from the characteristic polynomial of $\chi(s)$ (which is the same as that of $A_t(s)$), and which may be located at unfavorable locations, resulting in overshoot in the amplitude characteristic of $\chi(s)$. Overshoot can be avoided by using frequency-compensation techniques to force the closed loop poles in, e.g., Butterworth positions. This frequency compensation can best be done using phantom zeros [3]. A phantom zero is a zero in $A\beta(s)$ that coincides with a pole in $A_{t\infty}$. It therefore does not occur in the amplifier transfer function $A_t(s)$.

For a Butterworth characteristic, damping factor $\zeta = -\left(p_l + p_i - A\beta_0 \frac{p_l p_i}{z_\beta}\right)/2\omega_0$ should equal $1/\sqrt{2}$; without frequency compensation it is usually smaller. Uncompensated negative-feedback amplifiers will therefore show a worse distortion and detection behavior for frequencies near ω_0 than frequency compensated ones, under the assumption of equal LP products.

It may occur (e.g., in case of a BJT as active part and $R_1 > R_s + r_\pi$) that z_ξ is located at a lower value than p_l. Now, both $\xi(s)$ and $\beta(s)$ have a second-order transfer. In that case, the equations to be used are given in Row 2 of Table 5.3. With comparable values of the LP product χ_{max} will therefore show a larger value than in case z_ξ is canceled by p_l (Row 1), while ω_{max} remains the same. It appears that the value of χ_{max} is strongly dependent on the ratio of ω_0 and z_ξ. This ratio may become that large that χ_{max} will approach one. The distortion and envelope detection will thus be large at ω_0. A second-order transfer of $\xi(s)$ thus results in a worse distortion and envelope detection behavior than for a first order transfer of $\xi(s)$. If possible, it should be avoided.

Rows 3 and 4 give the equations in case p_l is dominant and p_i is not[12], resulting in a first order transfer of $A_t(s)$. Row 4 presents the equations in case of an uncanceled z_ξ, which may occur when R_l has such a low value that r_π starts to influence $\xi(s)$. Transfer $\chi(s)$ still shows two system poles that remain real. It should be noted that $\omega_{max} > \omega_0$. Therefore envelope detection will be maximal at a frequency (much) higher than the bandwidth also[13]. Note that χ_{max} can become large.

In case of series feedback at the output (Row 6), no detrimental effect of the load impedance occurs because its pole in $\beta(s)$ and $\xi(s)$ is completely compensated by a zero at virtually the same frequency, as is shown in Table 5.2. *Series feedback at the output thus results in a first order transfer for* $\chi(s)$. Transfer $\chi(\omega)$ equals χ_0 up to ω_0 and decreases with 20 dB/dec with increasing frequency. As approximation of the maximum value of $\chi(\omega)$ for maximal EMI susceptibility, χ_0 can be used.

[12]The other way around occurs much less in practical cases and is therefore not presented.

[13]Something comparable apparently also occurs in case of compensated operational amplifier negative-feedback amplifiers, due to the dominant pole from the Miller compensation. In [41] figures are shown of measured EMI as function of frequency. Maximal EMI is measured at frequencies much higher than the amplifier bandwidth.

In general, a large value of the LP product is beneficial. It results in a lower value of $\chi(\omega)$ at low frequencies and a lower χ_{max} than in case of a lower LP product. Note that EMI susceptibility requirements are easier to meet in case of series feedback at the output than in case of parallel feedback at the output, for comparable values of the LP product.

5.4 Design for a specified envelope detection behavior

At this point in the design process, the disturbing signal $E_s(\omega_c)$ is known and the negative-feedback amplifier consists of the feedback network and a hybrid-π representation of the active part. It is possible to analyze the envelope detection properties of the single-stage negative-feedback amplifier with the method described in the previous subsections. The hybrid-π values obtained from the active part in the bias point necessary to meet the load requirements can be used for this.

It is, however, more convenient to derive an analytical equation that can be used for synthesis purposes also. Expression (5.24) shows that we have to determine χ, D_2 and ξ_{ω_l}. As was argued in Chapter 2 and in Subsection 5.3.1, the maximal value of $E_{s,\omega_l}(\omega_c)$ is determined by χ_{max}, which therefore has to be determined. The approximate expressions for χ_{max}, (listed in Table 5.3), can be very well used for this.

Determining the analytical equation comes down to determining χ_{max} and D_2, and to use this in Equation (5.24). The resulting expression can then be solved for the linear transconductance (g_{m1}), which, in turn, can be used to determine the minimal bias current. This procedure is elucidated next with two examples.

5.4.1 Example: minimal bias current in a single-stage voltage follower

Assume we have a load impedance consisting of the shunt of a resistance of 5 kΩ and a capacitance of 1 nF. The intended signal has peak values of 100 mV up to a frequency of approximately 0.5 MHz. The source impedance can be represented by a single resistance of 100Ω. Assume the other information transfer requirements are such that a voltage follower can meet them.

In this example noise calculations are disregarded for simplicity. From the load impedance at 0.5 MHz and the peak value that may occur in the source signal it follows that a BJT should be biased at a minimal I_{cQ} of about 500 μA. The U_{ceQ} is not critical as long as it is larger than about 800 mV. Here, an U_{ceQ} equal to 2 V has been chosen.

The minimal loop gain requirement, and from this the bias current to meet the envelope detection requirement, has to be found. The *BC548B*[14] npn BJT

[14] To calculate the various transfers, the NXP SPICE model has been used.

is used in this example.

Now assume that a disturbing peak voltage is induced equal to $u_d = 1$ mV with m being 0.8 and that u_{s,ω_l} may have a maximal amplitude of 15 μV. The bias requirements of the BJT have to be found in order to meet the EMI demand.

It follows that $p_l \approx -\frac{1}{R_l C_l}\frac{r_\pi+R_s+R_l}{r_\pi+R_s}$, $p_i \approx -\frac{\omega_t}{\beta_{ac}}\frac{r_\pi+R_s}{R_s}$, $z_\xi = -\frac{1}{R_l C_l}$, $A\beta_0 = -g_{m1}\frac{r_\pi R_l}{R_l+R_s+r_\pi}$, $\xi_0 = \frac{r_\pi}{r_\pi+R_s+R_l}$. For simplicity it is assumed that the BJT can be biased in the mid-current region. In that case $g_{\pi 2} \approx \frac{g_{m2}}{\beta_{ac}}$ and $g_{m2} \approx \frac{q}{2n_f kT} g_{m1}$. Using these approximations for D_2, it is derived to hold: $D_2 = \frac{q}{2n_f kT}\frac{r_\pi}{r_\pi+R_s+R_l}$.

The equivalent voltage source u_{s,ω_l} is given by

$$u_{s,\omega_l}(\omega_{max}) \approx u_d^2 \chi_{max}^2 m \frac{q}{2n_f kT},$$

when we use Equation (5.24) and approximate ξ_{ω_l} by ξ_0. This is allowed because ξ_0 and ξ_{ω_l} will usually not deviate much from each other when ω_l is located in the passband.

Since $|p_l|$ can be expected to be located at a frequency much lower than $|p_i|$, $|p_l|$ is regarded as dominant, resulting in a first order behavior of $A_t(\omega)$. From the relatively low value of R_s and the high value of R_l it follows that it is likely that $|z_\xi|$ is that much smaller than $|p_l|$ that they will not cancel each other. ξ will thus have two poles and one zero. From the equations presented in the sixth row of Table 5.3 follow that χ_{max} is approximated by $\xi_0 \frac{p_l}{z_\xi}$ in this case. For $u_{s,\omega_l}(\omega_{max})$ it then follows

$$u_{s,\omega_l}(\omega_{max}) \approx u_d^2 m \left(\frac{r_\pi}{r_\pi + R_s}\right)^2 \frac{q}{2n_f kT} = u_d^2 m D_2'.$$

This equation can be solved for r_π, and from r_π bias current I_{cQ} can be determined.

$$r_\pi = \frac{-R_s\left(u_{s,\omega_l}(\omega_{max}) + \sqrt{u_{s,\omega_l}(\omega_{max})^2 - u_{s,\omega_l}(\omega_{max})\left(u_{s,\omega_l}(\omega_{max}) - d\right)}\right)}{u_{s,\omega_l}(\omega_{max}) - d}$$

$$d = u_d^2 m \frac{q}{2n_f kT}$$

It follows that r_π should have a value of 6.586 kΩ. Since r_π is related to g_{m1} ($r_\pi = \beta_{ac}/g_{m1}$), I_{cQ} can easily be calculated from r_π.

With $I_{cQ} = (n_f kT\beta_{ac})/(qr_\pi)$ and $\beta_{ac} \approx \beta_f = 294$, bias current I_{cQ} is therefore approximately 1.16 mA. This value is rounded up to 1.2 mA. Although the disturbing voltage u_d is only 1 mV, a relatively large bias current is required to achieve an $u_{s,\omega_l}(\omega_{max})$ of 15 μV.

When the approximations are checked using the hybrid-π parameters obtained with SPICE, we find $z_\xi = -2.19 \cdot 10^5$ rad/s, $p_l = -3.75 \cdot 10^5$ rad/s, $p_i = -1.45 \cdot 10^8$ rad/s, $A\beta_0 = -119.1$. Transfer $A_t = 0.99$ with a bandwidth of B= 45.04 Mrad/s (7.17 MHz). The frequency at which ω_{max} occurs is approximately 82.36 Mrad/s (13.11 MHz) and χ_{max} is approximately 0.982.

AC analysis in SPICE shows a χ_{max} of 0.914 at 79.11 Mrad/s (12.59 MHz), an A_t of 0.995 with a bandwidth of 53.34 Mrad/s (8.49 MHz). Because $|p_i|$ is only a factor three larger than the bandwidth obtained with $(1 - A\beta_0)p_l$, it does influence transfer A_t by slightly increasing its bandwidth [2], as the AC analysis shows. The approximations are in acceptable agreement with the AC analysis. Transient analysis shows an amplitude of the envelope detected signal of 12.2 μV. The disturbing signal used had a ω_c of 79.11 Mrad/s and a ω_l of 6283 rad/s.

With a bias current of 1.2 mA and an U_{ceQ} of 2V, β_{ac} is 286 and r_π is 6.30 kΩ. The maximal equivalent voltage $u_{s,\omega_l}(\omega_{max})$ now equals 14.96 μV, which is indeed the value designed for. Both designed and simulated values agree satisfactorily.

If a FET is considered as voltage follower, some changes appear compared with the BJT voltage follower. Two poles are found at approximately $p_l = -\frac{1}{R_l' C_l}$ and $p_i = -\frac{1}{R_s(C_{gs}+C_{gd})}$. The zero in ξ appears at $z_\xi = -\frac{1}{R_l' C_l}$. As a result $\xi(s)$ shows a first order transfer with only one pole at p_i. Also in case of a FET it can be expected that $|p_l| \ll |p_i|$. As a result the voltage follower $A_t(s)$ may show a first order transfer (depending on the loop gain).

χ_{max} is given in row 5 of Table 5.3. Elaborating this equation results in $\chi_{max} = \xi_0 = 1$. For $u_{s,\omega_l}(\omega_{max})$ it then follows

$$u_{s,\omega_l}(\omega_{max}) \approx u_d^2 m D_2 = u_d^2 m \frac{1}{2(U_{gsQ} - U_t)}.$$

Solving this equation for U_{gsQ} and inserting the result in the (simplest) equation for the drain current of a saturated FET (see Chapter 3) results in

$$I_{dQ} = \beta_{\mathrm{FET}} \left(m \frac{u_d^2}{2u_{s,\omega_l}(\omega_{max})} \right)^2.$$

Depending on the transconductance factor β_{FET}, the required I_{dQ} may be low. For instance, when a JFET of type J310 is considered, β_{FET} equals 3.384 mA/V^2. To meet the envelope detection constraint I_{dQ} has to be at least 2.5 μA. This current is much lower than required for meeting the linear output requirements. The required higher current results in a lower value of $u_{s,\omega_l}(\omega_{max})$, which is only beneficial.

To meet the minimum bandwidth requirement it was found that the FET has to be biased at an I_{dQ} of 0.8 mA. Pole p_l is located at approximately -213.2·10^3 rad/s, pole p_i at about -1.67·10^9 rad/s and zero z_ξ is also located at approximately -213.2·10^3 rad/s. Loop gain $A\beta_0$ is found to be -15.7. The bandwidth is approximately 3.56 Mrad/s (566 kHz). χ_{max} is expected to occur at about 77.1 Mrad/s (12.3 MHz) and has a value of 1. SPICE simulations show χ_{max} at 12.6 MHz and it has a value of 0.996. The bandwidth of A_t is 572 kHz.

Using these values and Equation (5.24) it is found that $u_{s,\omega_l}(\omega_{max})$ has a value of about 832 nV. SPICE simulations show a value of about 800 nV, which is in close agreement.

In these particular examples it was shown that meeting the envelope detection constraints for even a fairly low value of u_d resulted in an I_{cQ} higher than

required for the linear output requirements in case of a BJT, and an I_{dQ} for meeting the envelope detection constraints much lower than for meeting the linear output requirements in case of a FET.

Due to the fact that for the emitter follower D_2' is approximately 18.7 and D_2 of the source follower is approximately 1.0, while in both cases χ_{max} is virtually equal to one, the emitter follower performs less than the source follower regarding the envelope detection property. The amplitude of envelope detection is thus about 18.7 times as large in case of the BJT follower compared to the FET voltage follower.

5.4.2 Example: minimal bias current in a single-stage current follower

Here, the envelope detection properties of the single-stage current follower, i.e., CB stage and CG stage are investigated. Assume the current source impedance is represented by a resistance of 1 MΩ and the load impedance can be represented by a parallel connection of an 1 kΩ resistance and a capacitance of 100 pF. At the input a disturbing current of 100 μA is induced with m=1. The detected envelope may have a peak amplitude of 10 nA. For the CB stage a BJT of type BC548B can be used and for the CG-stage a FET of type J310. The minimal bias currents have to be determined for the BJT and the FET.

For the CB stage we find single pole transfers for both $\beta(s)$ and $\xi(s)$ since the pole due to C_l is cancelled by a zero due to C_l at virtually the same frequency in both transfers. The remaining pole is due to the BJT and is located at $p_i \approx -\frac{\omega_t}{\beta_{ac}} \frac{R_s r_o + r_\pi(R_s+r_o)}{R_s r_o}$. For sufficiently high values of R_s and r_o the pole can be approximated by $-\frac{\omega_t}{\beta_{ac}}$.

Since both $\xi(s)$ and $\beta(s)$ are first order transfers, $\chi(s)$ will also be a first order transfer. The maximal value of $\chi(s)$ thus equals χ_0. In the usually valid case that R_l is much smaller than r_o, it is found that χ_0 can be approximated by $\frac{1}{g_{m1}}$. Transfers ξ_0 and γ_0 are found to be equal and given by $-\frac{r_\pi R_s(r_o+R_l)}{r_\pi(R_s+r_o+R_l)+R_s(r_o+R_l)}$.

The second-order nonlinearity factor in the mid-current region is found to be given by $D_2 = \frac{q}{2n_f kT} \frac{r_\pi(R_s+r_o)}{r_\pi(R_s+r_o)+R_s r_o}$. It can be seen that for very large values of both R_s and r_o, D_2 approaches zero. In practical cases D_2 has a non-zero value.

Using these equations it is found that i_{s,ω_l} is approximated by

$$i_{s,\omega_l} = i_d^2 \frac{1}{g_{m1}^2} \frac{R_s + r_o}{R_s r_o} m \frac{q}{2n_f kT}.$$

Apparently, i_{s,ω_l} depends on the parallel connenction of R_s and r_o. Depending on the source and the transistor properties, and its bias current, R_s or r_o can become dominant, but they may also have values in the same order of magnitude. In the latter case neither is dominating and the shunt determines i_{s,ω_l}. By considering that $r_o = \frac{U_{AF}}{I_c Q} = \frac{qU_{AF}}{n_f kT g_{m1}}$, for the minimal value of g_{m1} it is found:

$$g_{m1} \approx \frac{i_d^2}{4U_{AF} i_{s,\omega_l}} m + \frac{i_d}{2i_{s,\omega_l}} \sqrt{\frac{i_d^2}{4U_{AF}^2} m^2 + 4 i_{s,\omega_l} \frac{q}{2n_f kT} \frac{1}{R_s} m}.$$

With the given values a minimal g_{m1} equal to 9.9 mA/V is found, resulting in a bias current I_{cQ} of only approximately 260 μA.

SPICE simulations show an ω_t of 253 Mrad/s and a β_{ac} of 286. Resistances r_π and r_o are 28k9 and 241 kΩ respectively. Pole p_i is therefore located at 1 Mrad/s. For the bandwidth is found 252.6 Mrad/s (40.2 MHz). SPICE simulations show a bandwidth of approximately 41.4 MHz.

Analysis of the envelope detection property in SPICE show a detected component of approximately 7.7 nA instead of 10 nA. This is most probably due to neglecting the (small) deviation between the actual value of $g_{\pi 2}$ and its approximated value of g_{m2}/β_{ac} in the mid-current region (see Chapter 3). Incorporating this effect gives a detected value of 12 nA$-$8.1 nA in case $0.97 \leq x \leq 1.03$. The calculation is accurate enough for a first design approach.

The validity of the method and expressions given here, were also checked by simulating the CB stage using nonlinear voltage controlled current sources as replacement of the BJT. The envelope detection of the resulting circuit amounted to 10.08 nA, which is the expected amplitude under assumption that $g_{m2} = q/(n_f kT) g_{m1}$ and $g_{\pi_2} = g_{m2}/\beta_{ac}$.

Using a FET as active stage in the current follower results in the common gate stage (CG stage). When the CG stage is analyzed it follows that the direct transfer from source to load, ρ, may have an exceptionally large value compared to the $\nu\xi\frac{A}{(1-A\beta)}$ term in (5.13). This is due to the fact that ρ is determined by the ratio of R_s and $R_s + r_{ds} + R_l$. Since a CG stage is a current follower, R_s is expected to have a large value, while R_l will be (much) lower than r_{ds}. The output resistance of a FET may be much lower than R_s also (as is the case for the FET used here). As a result ρ may already approach one, leaving only a small contribution of the controlled current source in the FET to A_t.

The asymptotic gain model does give a value that is accurate enough for A_t, but in case of envelope detection considerable errors may occur if the results of the asymptotic gain model are applied without care. After all, due to the possible large value of ρ it may dominate transfer A_t while it does not contribute to the nonlinearity. The nonlinear behavior is determined by the $\nu\xi\frac{A}{(1-A\beta)}$ term or, for short, $(A_t - \rho)$. See appendix B for derivation of equations that are valid for this case.

Because the equivalent signal source should result in the correct value of the detected envelope in the load signal after multiplication with A_t, the effect of ρ is taken into account in the equation for the equivalent signal source

$$i_{s,\omega_l}(\omega_c) = i_d(\omega_c)^2 m \chi(\omega_c)^2 D_2 \frac{1}{\xi_{\omega_l}} \left(1 - \frac{\rho_(\omega_c)}{A_t(\omega_c)}\right).$$

For decreasing values of ρ this equation reduces to the familiar Equation (5.24).

Using the same values for R_s, R_l and C_l as for the CB stage, first order transfers for $\xi(s)$ and $\beta(s)$ are found. So, χ_{max} may here also be approximated by χ_0. Under the reasonable assumption that r_{ds} is much larger than R_l, χ_0 can be approximated by $1/g_{m1}$ and $\xi_0 \approx \xi_{\omega_l}$ by the parallel connection of r_{ds} and R_s. For transfer ρ follows $R_s/(R_s + r_{ds})$.

The maximal value of the equivalent input current source, i_{s,ω_l}, can now be approximated by

$$i_{s,\omega_l} \approx i_d^2 m \frac{1}{g_{m1}^2} \frac{1}{R_s} D_2$$

Using the approximations $g_{m1} = 2\sqrt{\beta I_{dQ}}$ and $D_2 = \frac{\beta}{2\sqrt{\beta I_{dQ}}}$, it follows that bias current I_{dQ} can be approximated with:

$$I_{dQ} \approx \frac{1}{4} \sqrt[3]{\frac{1}{\beta} \left(\frac{i_d^2 m}{i_{s,\omega_l} R_s} \right)^2}$$

A bias current I_{dQ} of approximately 176 μA is found. This value, however, is not sufficient when a signal is disturbing the amplifier at the upper band edge of the bandwidth. To deliver a modulated current to the load with an amplitude of 100 μA and modulation depth one, means that the FET has to be biased at at least 200 μA. To prevent the FET from becoming too slow when delivering the current to the load, it should be biased at approximately 1.5 times this current.

With I_{dQ} 300 μA and (a not critical) U_{dsQ} of 4 V, for $A\beta_0$ a value of about -294 is found and p_i is located at approximately -2.1 Mrad/s. Since p_l, z_β, and z_ξ cancel, a bandwidth of 624.8 Mrad/s (99.4 MHz) is found. SPICE simulations show a bandwidth of 95.3 MHz.

A_t has a value equal to $295/296 = 0.997$ and ρ equals 0.848. For i_{s,ω_l} a value of 4.1 nA is found. SPICE simulations show a value for i_{s,ω_l} of 4.8 nA.

For these particular values of the source and load impedance comparable values of the bias currents are found for both CB and CG stage. The values of i_{s,ω_l} are comparable also. For the BJT and FET types used, no special preference regarding the envelope detection properties are found. They perform comparably well. The choice for FET or BJT should in this case be made on other considerations.

5.5 Design requirements for low EMI susceptibility in single-stage amplifiers

Single-stage negative-feedback amplifiers implementations are usually limited to the voltage follower, current follower, the shunt-shunt, and the series-series feedback types. As was shown, envelope detection properties of negative-feedback amplifiers with a current output, i.e., series feedback at the output, are generally better, thus produce smaller amplitude of the detected signals, than the envelope detection properties of amplifiers with a voltage output. This is due to the fact that $\chi(s)$ does not show an increase in its value due to a zero in case of series feedback at the output, while it does in case of parallel feedback at the output. If the load permits it, it should therefore preferably be driven by a current.

Overshoot in $\chi(s)$ may occur for any type of negative feedback when the transfer is of a higher order than one. In single-stage negative-feedback amplifiers the order is usually maximally two. Due to a too low value of the damping

factor ζ overshoot occurs in both transfer $A_t(s)$ and in $\chi(s)$. The same frequency compensation techniques that can be used to increase ζ to, for instance $1/\sqrt{2}$ for Butterworth compensation, are also beneficial for compensating the overshoot in $\chi(s)$. Since the envelope detection depends on χ^2 it is important that frequency compensation is always applied.

A high LP product is beneficial for low envelope detection of the amplifier. The high LP product decreases the value of transfer $\chi(s)$ from signal source to the input of the nonlinear component. Increasing the bias current of a transistor may increase the LP product due to the increase in g_m. For BJTs g_m increases linearly with increasing current. The g_m of FETs increases more or less with the square root of the drain current.

The bias current should, however, not be made larger than necessary, since this would result in a waste of power. As was shown, closed form equations can be derived that give the minimum bias current required for a certain specified EMI behavior.

The design of a single stage negative-feedback amplifier is demonstrated in Chapter 7. A single-stage transimpedance amplifier is designed with EMI induced errors comparable to the total white noise that is generated by the amplifier. The active part consists of a cascode.

5.6 Conclusions

A systematic design approach for application specific negative-feedback amplifiers, which can be used to design for a certain noise, distortion, and bandwidth performance, is extended to incorporate second-order nonlinear performance also. However, the latter is limited to EMI performance of single-stage negative-feedback amplifiers in this chapter (although measures to reduce EMI susceptibility are believed to be beneficial for reducing second-harmonic distortion also). It is shown how the bias current of the transistor for meeting the EMI, noise, and bandwidth requirements can be determined.

It has been shown that single-stage negative-feedback amplifiers with series feedback at the output suffer much less from EMI than amplifiers with parallel feedback at the output. If possible, series feedback at the output should thus be favored over parallel feedback at the output.

Frequency compensation should be applied to the amplifier (in order to obtain a Butterworth characteristic). Uncompensated amplifiers will show overshoot in the desired transfer and also in EMI susceptibility near the upper edge of the bandwidth.

Chapter 6

Design of EMI-resilient dual-stage amplifiers

Chapter 5 presented an introduction to systematic amplifier design, concentrating on noise, bandwidth, and proper signal transfer. It also presented a method to design single-stage negative-feedback amplifiers with low EMI susceptibility. This chapter concentrates on designing multiple-stage negative-feedback amplifiers with low specified EMI susceptibility. To limit the complexity of the analysis, the number of stages is restricted to two in this work. However, using the method presented in this chapter, a model and equations that can be used for amplifiers with three active stages can also be derived. More than three stages usually leads to stability problems [3], and therefore is of little interest.

Section 6.1 presents a new model enabling analysis of second-order nonlinearity and EMI behavior of dual-stage negative-feedback amplifiers. The effects of both global and local negative-feedback can be analyzed with this model. It will be shown that applying local feedback has some drawbacks. When local feedback is avoided, the model can be simplified and used for analysis and design. The simplified model is presented and analyzed in Section 6.2. In Section 6.3, combinations of input and output stages are analyzed, resulting in design rules for negative-feedback amplifiers with a specified signal-to-error ratio (SER). Some technology considerations are presented in Section 6.4 and the proposed design methodology for low EMI susceptible negative-feedback amplifiers is presented in Section 6.5. Finally, a design example and conclusions are presented in Sections 6.6 and 6.7, respectively.

6.1 Design considerations for low EMI-susceptible dual-stage negative-feedback amplifiers

Describing EMI susceptibility of single-stage amplifiers can be done by using the simple model presented in Fig. 5.5. This model, however, does not adequately

describe distortion related effects like EMI of multistage amplifiers, because the contribution to the total nonlinearity of the individual stages does not become clear. The influence of the individual stages on each other does not become clear either. Therefore, a model will be presented that is based on Fig. 5.5, but also takes the nonlinear behavior of the individual active stages into account. The model will be valid for a dual-stage negative-feedback amplifier.

6.1.1 Dual-stage negative-feedback amplifier model

A model that can be used to determine the EMI related effects in dual-stage amplifiers is presented in Figure 6.1. It is comparable to the model presented in Section 5.3 and the same considerations hold (see Pages 170-174), i.e., it only takes the linear and the nonlinear (EMI) response at ω_l into account. In

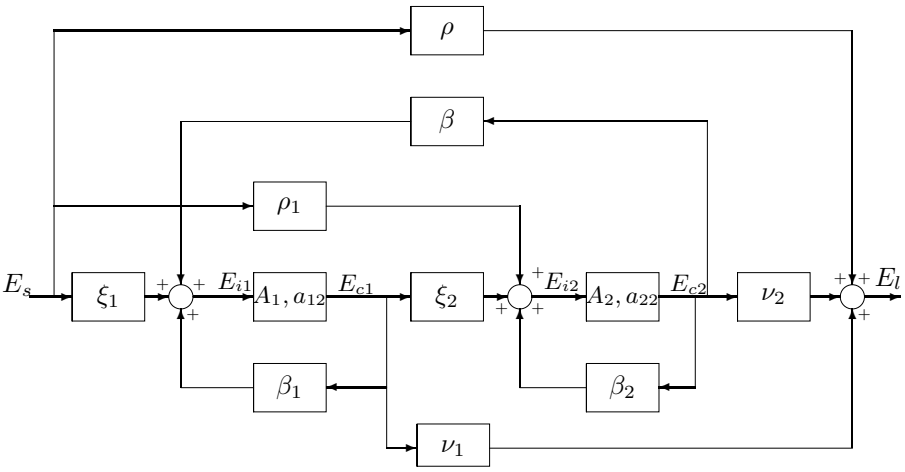


Figure 6.1: Model of a dual-stage negative-feedback amplifier.

principle, a three stage negative-feedback amplifier can be modelled in the same way. However, since the dual-stage model presented here already results in quite complicated transfers, we will not elaborate on this.

In Figure 6.1 two amplifying stages called A_1 and A_2 can be recognized. Their linear output signals are $E_{c1} = E_{i1}A_1$ and $E_{c2} = E_{i2}A_2$ respectively. Signal source E_s and load signal E_l are easily recognized also. Direct feed-through from the source to the load is depicted by ρ. Feed-through from the signal source to the the input of the second stage is depicted by ρ_1. The direct transfer from input signal E_s to the input of the first stage E_{i1} is represented by ξ_1. Local feedback applied to the input stage is depicted by β_1. From the output of the input stage there is a direct transfer to the output signal, ν_1. As a matter of fact, because the transfer shunts the output stage, it could also be seen as a feed-through. Therefore, it could also be called ρ_2.

Transfer ξ_2 represents the transfer from E_{c1} to the input of the second stage E_{i2}. Local feedback applied to the output stage is represented by β_2 and global feedback from the output E_{c2} to the input of the input stage E_{i1} is depicted by β. Finally, ν_2 is the transfer from E_{c2} to the output signal E_l.

From this rather complicated model some important equations have to be derived. First of all, to be able to draw conclusions regarding nonlinear behavior the linear transfers E_{i1} and E_{i2} as a function of the input signal E_s have to be derived. The linear transfer from E_s to E_l, (A_t) has to be determined also.

From Figure 6.1 the three following equations can easily be determined[1]

$$E_l = E_s\rho + E_{i1}A_1\nu_1 + E_{i2}A_2\nu_2, \tag{6.1}$$

$$E_{i1} = E_s\xi_1 + E_{i1}A_1\beta_1 + E_{i2}A_2\beta, \tag{6.2}$$

and

$$E_{i2} = E_{i1}A_1\xi_2 + E_s\rho_1 + E_{i2}A_2\beta_2. \tag{6.3}$$

From these three equations it follows for E_{i1}, E_{i2} and A_t:

$$E_{i1} = E_s\frac{1}{1-A_1\beta_1}\left(\xi_1 + A_2\beta\left[\frac{\rho_1(1-A_1\beta_1)+A_1\xi_1\xi_2}{(1-A_1\beta_1-A_2\beta_2)-A_1A_2(\xi_2\beta-\beta_1\beta_2)}\right]\right), \tag{6.4}$$

$$E_{i2} = E_s\left[\frac{\rho_1(1-A_1\beta_1)+A_1\xi_1\xi_2}{(1-A_1\beta_1-A_2\beta_2)-A_1A_2(\xi_2\beta-\beta_1\beta_2)}\right], \tag{6.5}$$

and

$$\begin{aligned} A_t =& \rho + \xi_1\frac{A_1\nu_1}{1-A_1\beta_1} + A_2\left(\nu_2 + \frac{A_1\beta\nu_1}{1-A_1\beta_1}\right)\times \\ & \left(\frac{\rho_1(1-A_1\beta_1)+A_1\xi_1\xi_2}{(1-A_1\beta_1-A_2\beta_2)-A_1A_2(\xi_2\beta-\beta_1\beta_2)}\right). \end{aligned} \tag{6.6}$$

Unfortunately, Equation(6.6) is large and cannot easily be reduced by letting the loop gain go to infinity. So, it does not seem to be possible to reduce the model to an asymptotic gain model. The local feedback loops β_1, β_2 and the feed through transfers ρ_1 and ν_1 prevent it.

In case of global feedback only and negligible values of ρ_1 and ν_1 the model simplifies and it becomes possible to set up an asymptotic gain model. (It must be noted that for actual transistors the capacitance between base and collector or gate and drain will introduce a frequency dependent local feedback, though.) In Section 6.2 this asymptotic gain model will be presented.

6.1.2 Envelope detection in negative-feedback amplifiers using global- and local feedback

In the following derivations we only look at envelope detection as a result of EMI. Again, a carrier wave with frequency ω_c higher than the bandwidth of the

[1]Note that Mason's rule (e.g., [150]) can also be applied to determine E_{i1}, E_{i2}, and A_t.

amplifier is assumed. Further, it is assumed that the low frequency modulation ω_l of the envelope is within the bandwidth of the amplifier. The modulation index is represented by m.

It follows from Figure 6.1 that for the demodulated signal in the outputs E_{c1} and E_{c2} hold

$$\begin{aligned} E_{c1,\omega_l}(\omega_c) =& E_{i1}(\omega_c)^2 m a_{12} \frac{1}{1 - A_1\beta_{1,\omega_l}} \times \\ & \left[1 + \frac{A_1 A_2 \xi_{2,\omega_l}\beta_{\omega_l}}{(1 - A_1\beta_{1,\omega_l} - A_2\beta_{2,\omega_l}) - A_1A_2(\xi_{2,\omega_l}\beta_{\omega_l} - \beta_{1,\omega_l}\beta_{2,\omega_l})}\right] \\ & + E_{i2}(\omega_c)^2 m a_{22} \frac{A_1\beta_{\omega_l}}{(1 - A_1\beta_{1,\omega_l} - A_2\beta_{2,\omega_l}) - A_1A_2(\xi_{2,\omega_l}\beta_{\omega_l} - \beta_{1,\omega_l}\beta_{2,\omega_l})} \end{aligned} \tag{6.7}$$

and

$$\begin{aligned} E_{c2,\omega_l}(\omega_c) =& E_{i1}(\omega_c)^2 m a_{12} \frac{A_2\xi_{2,\omega_l}}{(1 - A_1\beta_{1,\omega_l} - A_2\beta_{2,\omega_l}) - A_1A_2(\xi_{2,\omega_l}\beta_{\omega_l} - \beta_{1,\omega_l}\beta_{2,\omega_l})} \\ & + E_{i2}(\omega_c)^2 m a_{22} \frac{(1 - A_1\beta_{1,\omega_l})}{(1 - A_1\beta_{1,\omega_l} - A_2\beta_{2,\omega_l}) - A_1A_2(\xi_{2,\omega_l}\beta_{\omega_l} - \beta_{1,\omega_l}\beta_{2,\omega_l})} \end{aligned} \tag{6.8}$$

For the demodulated term in the output it follows:

$$E_{l,\omega_l}(\omega_c) = E_{c1,\omega_l}(\omega_c)\nu_{1,\omega_l} + E_{c2,\omega_l}(\omega_c)\nu_{2,\omega_l}. \tag{6.9}$$

Usually $E_{c1,\omega_l}(\omega_c)\nu_{1,\omega_l}$ will be much smaller than $E_{c2,\omega_l}(\omega_c)\nu_{2,\omega_l}$. Therefore, the envelope detection in the output signal will be dominated by E_{c2,ω_l}. For the remainder of this chapter, we therefore concentrate on E_{c2,ω_l}.

We are interested in finding an equivalent input signal source that accounts for the envelope detection term, while the amplifier is further considered being linear. Considering that $E_{i2,\omega_l}(\omega_c) = E_{c2,\omega_l}(\omega_c)/A_2$ and combining equations (6.5), (6.8), the expression for the equivalent signal source becomes

$$\begin{aligned} E_{s,\omega_l}(\omega_c) =& E_s^2 m \frac{1}{\rho_{1,\omega_l}(1 - A_1\beta_{1,\omega_l}) + A_1\xi_{1,\omega_l}\xi_{2,\omega_l}} \times \\ & \left(a_{12}\xi_{2,\omega_l}\left[\frac{1}{(1 - A_1\beta_1(\omega_c))}\left(\xi_1(\omega_c) + A_2\beta(\omega_c)\Upsilon(\omega_c)\right)\right]^2 + \right. \\ & \left. \frac{a_{22}}{A_2}(1 - A_1\beta_{1,\omega_l})\Upsilon(\omega_c)^2\right), \end{aligned} \tag{6.10}$$

with

$$\Upsilon(\omega_c) = \frac{\rho_1(\omega_c)(1 - A_1\beta_1(\omega_c)) + A_1\xi_1(\omega_c)\xi_2(\omega_c)}{[1 - A_1\beta_1(\omega_c) - A_2\beta_2(\omega_c)] - A_1A_2\left[\xi_2(\omega_c)\beta(\omega_c) - \beta_1(\omega_c)\beta_2(\omega_c)\right]}. \tag{6.11}$$

The coefficients of a_{12} and a_{22} may have opposite signs. From a mathematical point of view, it is possible that the envelope detection becomes zero at a certain frequency.

By investigating Equation (6.10) it is possible to draw some conclusions. For practical amplifier designs we may expect $\rho_{1,\omega_l}(1 - A\beta_{1,\omega_l}) << A_1\xi_{1,\omega_l}\xi_{2,\omega_l}$ (a large value of the latter is beneficial for a small value of the equivalent signal source). Equation (6.10) can now be approximated to be

$$E_{s,\omega_l}(\omega_c) \approx E_s^2 m \frac{1}{A_1\xi_{1,\omega_l}} \times \left(a_{12}\left[\frac{\xi_1(\omega_c) + A_2\beta(\omega_c)\Upsilon(\omega_c)}{(1 - A_1\beta_1(\omega_c))}\right]^2 + \frac{a_{22}(1 - A_1\beta_{1,\omega_l})}{A_2\xi_{2,\omega_l}}\left[\Upsilon(\omega_c)\right]^2 \right). \tag{6.12}$$

Large values of $A_1\xi_{1,\omega_l}$ decrease the influence of the second-order nonlinearity term of the input stage (a_{12}). The local loop gain $(1 - A_1\beta_1(\omega_c))$ tends to linearize the input stage. The local loop gain is, however, dependent on the signal frequency. It can be expected that for the usually high frequency ω_c its effect is negligibly small. Note that the product $A_2\xi_2$ equals the current gain (α_2) of the output stage[2], and therefore the low frequency current gain $\alpha_{20} \approx \alpha_{2,\omega_l} = A_2\xi_{2,\omega_l}$. The product $A_1\xi_{1,\omega_l}$ equals the low frequency current gain of the input stage in case of parallel feedback at the input (ξ transfers current to voltage and A_1 transfers voltage to current) but in case of series feedback at the input, it does not (ξ is a dimensionless transfer ≤ 1). Therefore, $A_1\xi_{1,\omega_l}$ is used the equations instead of α_{10} in the sequel.

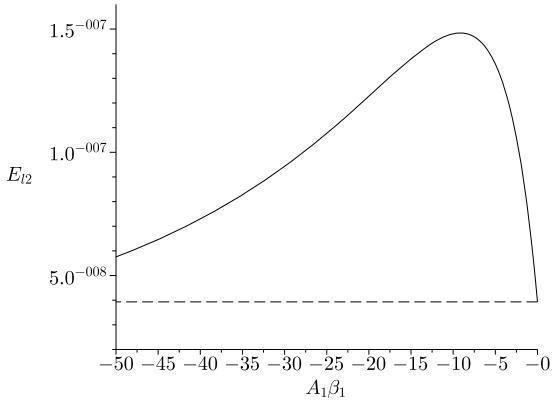
The influence of the nonlinearity term of the output stage (a_{22}) decreases for larger values of $A_1\xi_{1,\omega_l}$ and α_{20}. It is, however, also very clear that applying negative feedback to the input stage results in an increase of the influence of a_{22}. This increase is equal to the local loop gain $(1 - A_1\beta_{1,\omega_l})$. It can therefore be concluded that applying local feedback to the input stage is detrimental to the EMI susceptibility and distortion for those frequencies where term $\Upsilon(\omega_c)$ is not yet dominating. Depending on the design, $\Upsilon(\omega_c)$ may already become dominating for frequencies in the bandwidth.

The observations regarding the increased distortion due to global feedback is consistent with the findings of other authors [59][7][2]. Note that the type of feedback, series or shunt, is in principle unimportant. Both are detrimental for distortion. The load of the local feedback on the signal path is different in both cases [60], therefore the current gain of the output stage $\alpha_{20} = A_2\xi_{2,\omega_l}$ may differ in both cases, resulting in different values of E_{s,ω_l}.

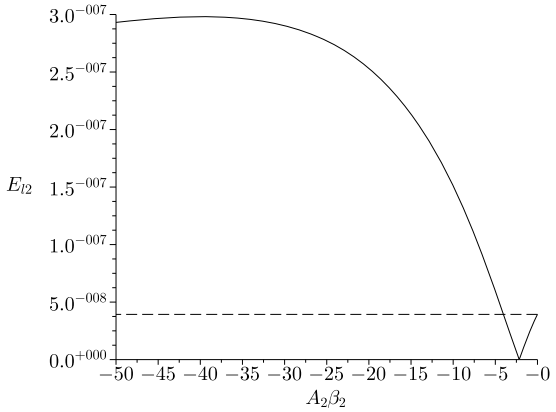
Using Equation (6.10) it is possible to determine the effects of global feedback in detail. For instance, by differentiating the equation to β_1 and equating the result to zero, maximum or minimum values for β_1 can be obtained. The same can be done for β_2.

[2]For a BJT output stage $\alpha_2 = \xi_2 A_2 = -\frac{\beta_{ac2}}{1+\beta_{ac2}\frac{j\omega_c}{\omega_{T2}}}$, $\alpha_{20} = -\beta_{ac}$, and for a FET output stage $\alpha_2 = -\frac{\omega_{T2}}{j\omega_c}$, $\alpha_{20} = -\frac{\omega_{T2}}{j\omega_l}$ are found.

Calculations for the rather academic case of a signal frequency near zero hertz shows that for varying $A_1\beta_1$ (β_2 is 0), a maximum in the second-harmonic distortion is found, see Figure 6.2(a). For varying values of $A_2\beta_2$ (β_1 is 0) one obtains a maximum and a minimum, Figure 6.2(b). The possibility of reducing second-order distortion by applying moderate amounts of feedback to the output stage, agrees with [59]. Figure 6.2 also clearly shows that the value $A_2\beta_2$ should



(a) Distortion as a function of $A_1\beta_1$.



(b) Distortion as a function of $A_2\beta_2$.

Figure 6.2: (a) second-order distortion as a function of $A_1\beta_1$ and β_2=0 (b) second-order distortion as a function of $A_2\beta_2$ and β_1=0. The frequency is near zero Hz for both cases. The dashed lines represent the second-order distortion in case of global feedback only. Parameters used: A_1=1 mA/V, a_{12} = 0.1 mA/V^2, A_2= 10 mA/V, a_{22}= 1 mA/V^2, ξ_1= 90 k, ξ_2= -10 k, $\rho = \rho_1$=0, ν_2= 1, β= 200, E_s= 1 μ[-].

be chosen very carefully. A wrong value of $A_2\beta_2$ results in an increase of second-order distortion, because the minimum is located in a relatively small area while the maximum is located in a relatively large area.

Local feedback also has its influence on $\Upsilon(\omega_c)$, see Equation (6.11). For low EMI susceptibility the denominator, which represents the global loop gain, should be large. Local feedback applied to the input stage increases the numerator and tends to decrease the global loop gain (β has the opposite sign of β_1, β_2 and ξ_2). Local feedback applied to the output stage will usually decrease the global loop gain also.

It seems that for a high global loop gain A_1 and α_2 have to be large. Non-zero values of β_1 and β_2 tend to decrease the global loop gain. A frequency dependent increase of E_{s,ω_l} can thus be expected. On top of that, a non-zero value of β_1 also increases the influence of the second-order nonlinearity term of the output stage (a_{22}). It may therefore be concluded that local feedback has to be avoided when designing amplifiers with a large SER.

Several calculations for frequencies ω_c and ω_l do not seem to show advantages on EMI for non-zero values for β_1 or β_2. But even when a type of global feedback could be found that reduces EMI with respect to the case with global feedback only, this may still not be advantageous. After all, the SER is also determined by distortion; it may very well be the case that EMI demands may be met, while the SER is not reached due to too much distortion.

The observations made so far point out that, for low EMI susceptibility, the parameters $A_1\xi_1$ and α_{20} have to be large. The contribution of the second stage to the total second-order nonlinearity (and therefore to the EMI and second harmonic distortion behavior) can be minimized by assuring a large current gain of the second stage. An obvious way to do this is by using a BJT or FET with a high current gain as second stage and by assuring that none or as little as possible current gain of this device is lost in the implementation of the negative-feedback amplifier.

6.1.3 Concluding remarks about local feedback

It was shown that local feedback applied to the input stage has an adverse effect on the envelope detection. Apart from reducing the global feedback, it tends to increase the effect of the second-order nonlinearity of the output stage. Both effects outweigh the linearizing effect of the local feedback on the input stage. Because this linearizing effect is frequency dependent, its effect at frequency ω_c is questionable.

Local feedback applied to the output stage reduces the global loop gain also. An extra adverse effect on the envelope detection by increasing the second-order nonlinearity of the input stage is not present. Calculations made at a frequency near zero herz show that moderate amounts of local feedback applied to the output stage may have a positive effect on reducing the second-order distortion. It is expected that this is not the case anymore at ω_c since the effect of local feedback can be expected to be negligible due to low values of $\beta_2(\omega_c)$ and $\Upsilon(\omega_c)$.

It may be concluded that for low values of the equivalent input source, $A_1\xi_1$ and α_{20} have to be large and local feedback has to be avoided. If local feedback is avoided, a new simplified model of dual-stage negative-feedback amplifiers can be used for analysis and design.

6.2 Model of a dual-stage negative-feedback amplifier without local feedback

When local feedback is omitted, the model presented in Fig. 6.1 can be reduced to the model shown in Figure 6.3. It was further assumed that ρ_1 and ν_1 are so small that they can be omitted from the model. As a result, the simplest model for analysis and design of dual-stage negative-feedback amplifiers is obtained.

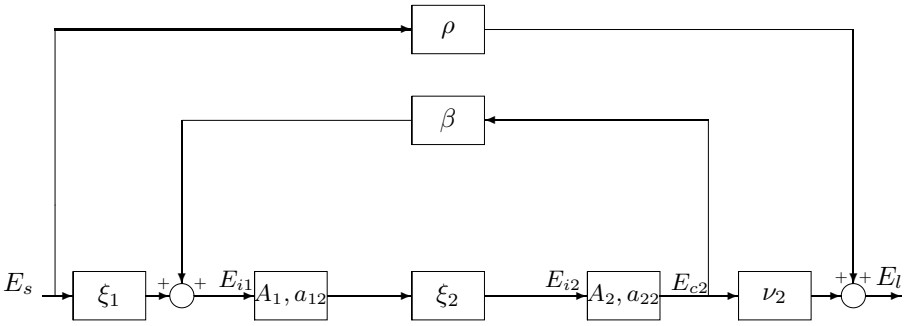


Figure 6.3: Simplified model of a dual-stage negative-feedback amplifier without local feedback.

Following the same considerations as in case of the asymptotic gain model for single-stage negative-feedback amplifiers (see pages 170–174), it is now found for A_t

$$A_t = \rho\frac{1}{1 - A_1A_2\xi_2\beta} + A_{t\infty}\frac{-A_1A_2\xi_2\beta}{1 - A_1A_2\xi_2\beta} = \rho\frac{1}{1 - A_1\alpha_2\beta} + A_{t\infty}\frac{-A_1\alpha_2\beta}{1 - A_1\alpha_2\beta}, \tag{6.13}$$

with $\alpha_2 = A_2\xi_2$. In all practical amplifier designs the first term in this equation will be much smaller than the second. This results in

$$A_t = \frac{E_l}{E_s} = A_{t\infty}\frac{-A_1\alpha_2\beta}{1 - A_1\alpha_2\beta}. \tag{6.14}$$

Equivalent to the traditional asymptotic gain model, the design of an amplifier is reduced to two successive steps. The first is the determination of $A_{t\infty}$ and

the second step is the realization of an adequate loop transfer $A_1\alpha_2\beta$. When the second step is realized, $A_{t\infty}$ can be regarded to be the reciprocal of the feedback factor.

For E_{i1} and E_{i2} it follows from Figure 6.3

$$E_{i1} = E_s \frac{\xi_1}{1 - A_1\alpha_2\beta} = E_s\chi_1 \tag{6.15}$$

and

$$E_{i2} = E_s A_1\xi_1\xi_2 \frac{1}{1 - A_1\alpha_2\beta} = E_s\chi_2. \tag{6.16}$$

The equations presented here fully describe the linear behavior of a dual-stage negative-feedback amplifier.

6.2.1 Envelope detection in negative-feedback amplifiers with global feedback only

Under the same assumptions as in Section 6.1.2, it follows from Figure 6.3 that for the demodulated signal in the output E_{c2} it holds

$$E_{c2,\omega_l}(\omega_c) = E_s^2 m \frac{\xi_1(\omega_c)^2}{\left(1 - A_1\alpha_2(\omega_c)\beta(\omega_c)\right)^2} \frac{1}{1 - A_1\alpha_{20}\beta_{\omega_l}} \left[a_{12}\alpha_{20} + a_{22}A_1^2\xi_2(\omega_c)^2\right]. \tag{6.17}$$

An equivalent signal source $E_{i2,\omega_l}(\omega_c)$ can be found by dividing (6.17) by A_2 when we further assume A_2 to be linear. Transferred back into an equivalent input signal source gives

$$E_{s,\omega_l}(\omega_c) = \frac{E_{c2,\omega_l}(\omega_c)}{A_2} \frac{(1 - A_1A_2\xi_{2,\omega_l}\beta_{\omega_l})}{A_1\xi_{1,\omega_l}\xi_{2,\omega_l}} = \frac{E_{c2,\omega_l}(\omega_c)}{A_2} \frac{(1 - A_1\alpha_{20}\beta_{\omega_l})}{A_1\xi_{1,\omega_l}\xi_{2,\omega_l}}. \tag{6.18}$$

Substitution of (6.17) in (6.18) yields

$$E_{s,\omega_l}(\omega_c) = E_s^2 m\chi_1(\omega_c)^2 \left[a_{12}\frac{1}{A_1\xi_{1,\omega_l}} + a_{22}\frac{A_1\xi_2(\omega_c)^2}{\xi_{1,\omega_l}\alpha_{20}}\right]. \tag{6.19}$$

The same conclusions about the current gain of the second stage (α_{20}) can be drawn as in Section 6.1.2. Further, large values of $A_1\xi_{1,\omega_l}$ are also beneficial.

When BJTs are considered, the effect of the nonlinear voltage-current relation at the input of the BJT has to be taken into account by incorporating $\gamma_{1,\omega_l} = \left.\frac{E_{i1,\omega_l}}{i_{1,\omega_l}}\right|_{E_s=E_{c2}=0}$ and $\gamma_{2,\omega_l} = \left.\frac{E_{i2,\omega_l}}{i_{2,\omega_l}}\right|_{E_s=E_{c2}=0}$ in Equation (6.19), with $i_{1,\omega_l} = b_{12}u_{be1}^2$ and $i_{1,\omega_l} = b_{22}u_{be2}^2$; see also Section 5.3 and Chapter 4. For

$E_{s,\omega_l}(\omega_c)$ we can now be write

$$\begin{aligned} E_{s,\omega_l}(\omega_c) =& E_s^2 m \chi_1(\omega_c)^2 \frac{1}{\xi_{1,\omega_l}} \times \\ & \left[\frac{(a_{12} + b_{12}\gamma_{1,\omega_l} A_1)}{A_1} + (a_{22} + b_{22}\gamma_{2,\omega_l} A_2) \frac{A_1}{A_2^2} \frac{\alpha_{20}}{\left(1 - \frac{j\omega_c}{p_o}\right)^2} \right] \\ =& E_s^2 m \chi_1(\omega_c)^2 \frac{1}{\xi_{1,\omega_l}} \left[\frac{a'_{12}}{A_1} + \frac{A_1}{A_2^2} \frac{\alpha_{20}}{\left(1 - \frac{j\omega_c}{p_o}\right)^2} a'_{22} \right] \\ =& E_s^2 m \chi_1(\omega_c)^2 \frac{1}{\xi_{1,\omega_l}} D_2(\omega_c), \end{aligned} \tag{6.20}$$

with p_o being the pole introduced by the output stage. Use has been made from the equality $\frac{\xi_2^2(\omega_c)}{A_2 \xi_{2,\omega_l}} = \frac{\xi_{20}^2}{A_2 \xi_{20}} \left(\frac{1}{1 - \frac{j\omega_c}{p_o}} \right)^2 = \frac{\alpha_{20}}{A_2^2} \left(\frac{1}{1 - \frac{j\omega_c}{p_o}} \right)^2$ to derive Equation (6.20). Note that D_2 is now frequency dependent and that, typically, the output stage will dominate $E_{s,\omega_l}(\omega_c)$ when $\omega_c < |p_o|$.

In case either the first or the second stage is a FET, the corresponding γ_{ω_l} is zero. Using Equation (6.20), $E_{s,\omega_l}(\omega_c)$ can thus be determined for any combination of active semiconductor.

When the terms between the brackets are considered, it can be seen that it should be possible to make the equivalent input signal source zero at a certain frequency. From Equation (6.19) follows that this is the case when the following equality is satisfied

$$\frac{a_{12}}{A_1} = a_{22} A_1^2 \frac{\xi_2(\omega_c)^2}{\alpha_{20}}. \tag{6.21}$$

It is clear that cancellation of the second-order nonlinearity terms can occur at one single frequency only. It is therefore not possible to design a dual-stage negative-feedback amplifier with zero EMI susceptibility over a large frequency range. For frequencies lower than the zero E_{s,ω_l} frequency, the second stage (output stage) dominates the second-order nonlinearity. The input stage dominates the second-order nonlinearity for frequencies higher than that frequency.

Equation (6.20) shows that $E_{s,\omega_l}(\omega_c)$ is now determined by both the linear transfer $\chi_1(\omega_c)$ and $D_2(\omega_c)$. In Subsections 6.2.2–6.2.4, both $D_2(\omega_c)$ and $\chi_1(\omega_c)$ will be investigated. From the expression for $\chi_1(\omega_c)$ conclusions about the most beneficial dominant poles and type of feedback will be presented and from investigating $D_2(\omega_c)$ it will follow which stage will dominate $E_{s,\omega_l}(\omega_c)$ at which ω_c. From the product of $\chi_1^2(\omega_c) D_2(\omega_c)$ conclusions will be presented about the preferred technology to be used and about biasing of the input and output stage.

6.2.2 Second-order nonlinearity factor as a function of frequency

The second-order nonlinearity factor D_2 is frequency dependent in case of a dual-stage negative-feedback amplifier, as Equation (6.20) clearly shows. Taking linearizing effects of BJTs and differential stages into account by a'_{12} and a'_{22}, D_2 is given by

$$D_2(\omega_c) = \frac{a'_{12}}{A_1} + \frac{A_1}{A_2^2}\alpha_{20}\frac{1}{\left(1-\frac{j\omega_c}{p_o}\right)^2}a'_{22}. \tag{6.22}$$

Clearly, the output stage will (in most practical cases) dominate $D_2(\omega_c)$ when $\omega_c \ll |p_o|$, since a'_{22} is multiplied by the large α_{20}. Only in the exceptional case of an a'_{22} being much lower than a'_{12}, this may not be the case.

The value of $D_2(\omega_c)$ has decreased by 6 dB at $\omega_c = |p_o|$, and it will decrease further at a rate of -40 dB/dec. At a particular frequency (ω_k), the contribution of the input and output stage to D_2 will be equal, but with opposite sign. The second-order nonlinearity factor thus equals zero at this frequency[3], and the input stage starts to determine $D_2(\omega_c)$ for higher frequencies. The frequency above which the input stage determines $D_2(\omega_c)$, ω_k, can be approximated by

$$\omega_k \approx \left| -p_o + p_o\sqrt{1-4\left(1+\frac{1}{\sqrt{2}}\frac{a'_{22}}{a'_{12}}\left(\frac{A_1}{A_2}\right)^2\alpha_{20}\right)}\right|. \tag{6.23}$$

For a very low value of a'_{12} (as can be the case in a very well balanced input stage) ω_k may get a very high value. In the inverse situation, i.e., $a'_{12} \gg a'_{22}$, a'_{12} is dominating at every frequency and ω_k loses its meaning.

6.2.3 The effect of an additional stage on χ_1

With an additional amplifying stage in the active part of the negative-feedback amplifier, the equations for $\xi_1(s)$ and $\beta(s)$ and their poles do not change much compared with the equations given in Section 5.3. The main effect of the additional stage is that it increases the LP product with a factor ω_T [3]. For $\chi_1(s)$ it can now be written

$$\chi_1(s) \approx \xi_{10}\frac{N_{\chi_1}}{LP_1\omega_{T2}} \approx \frac{\xi_{10}}{A_1\beta_0\alpha_{20}}\frac{N_{\chi_1}}{p_1\frac{\omega_{T2}}{\alpha_{20}}} = \chi_{10}\frac{N_{\chi_1}}{p_1\frac{\omega_{T2}}{\alpha_{20}}}, \tag{6.24}$$

where LP_1 is the loop gain poles product of a single stage negative-feedback amplifier and ω_{T2} is the transit frequency of the additional stage. A_1 is the transconductance of the first stage, α_{20} is the DC current gain of the additional stage, and pole p_1 is a pole originating from the single stage case (LP_1) and is independent of the additional stage. Numerator N_{χ_1} represents the zeros of

[3]It should be noted that some EMI susceptibility may remain, even when $D_2(\omega_c)$ equals zero, since EMI susceptibility originates from even-order nonlinearity. Even when the second-order nonlinearity is cancelled, other even-order nonlinearities may not.

$\chi_1(s)$. This equation is valid for values of $-A\beta_0\alpha_{20} \gg 1$, which is usually the case.

As long as ω_{T2} is larger than the bandwidth given by LP_1, the bandwidth increases [3]. The order of the system also increases and as a result frequency compensation will become more difficult. Now pole $|\frac{\omega_{T2}}{\alpha_{20}}|$ may appear (depending on the kind of negative-feedback) as a(n) (additional) zero in N_{χ_1}, increasing the initial number of zeros with one. Both the poles in the denominator and the zero(s) in the numerator will determine χ_1 and will cause a maximum in $E_{s,\omega_l}(\omega_c)$. This will be investigated in Subsection 6.2.4.

As a result of the additional stage, the value of χ_{10} (the DC value of $\chi_1(s)$) decreases with a factor equal to α_{20}. This is in principle beneficial for a low E_{s,ω_l}, as can be seen from Equation (6.19). E_{s,ω_l} is, however, determined by two stages now instead of one. The additional stage also adds second-order nonlinearity besides adding α_{20} to the loop gain. Note that the contribution of the second-order nonlinearity of the additional stage is additive, while its contribution to the LP product is multiplicative, see for instance Equation (6.19). The increase of the LP product therefore outweighs the drawback of the increased second-order nonlinearity term.

Let us compare the expected $E_{s,\omega_l}(\omega_c)$ of a single-stage and a dual-stage negative-feedback amplifier in case $\omega_c \ll |p_o|$. $E_{s,\omega_l}(\omega_c)$ of a single stage and dual-stage negative-feedback amplifier can be approximated by

$$E_{s,\omega_l \mathrm{single-stage}} \sim \frac{\xi_{10}^2}{(A_1\beta_0)^2}\frac{a_{12}}{A_1}$$

and

$$E_{s,\omega_l \mathrm{dual-stage}} \sim \frac{\xi_{10}^2}{(A_2\beta_0)^2}\frac{a_{22}}{\alpha_{20}A_1}.$$

Typically, $A_2 \geq A_1$, a_{22} will be of the same order of magnitude as a_{12}, and β_0 will be about equal in both cases. It may thus be expected that $E_{s,\omega_l}(\omega_c)$ of a dual-stage negative-feedback amplifier may be approximately α_{20} times lower than that of a single stage negative-feedback amplifier. This means that a BJT with a large β_{ac} or a FET with a large value of $\omega_{T2}/j\omega_l$ should be used as output stage. Moreover, $E_{s,\omega_l}(\omega_c)$ decreases with increasing A_2. This means that for a low $E_{s,\omega_l}(\omega_c)$ the bias current of the output stage should be relatively large; usually larger than the bias current of the input stage.

6.2.4 Maximal value of χ_1 of a dual-stage negative-feedback amplifier

In case of a dual stage negative-feedback amplifier, we may expect three poles: one originating from the load, one originating from the input stage, and one from the output stage. Not all three poles may belong to the dominant group. Often only two poles will be dominant, which will be assumed in this section.

The pole of the load is usually determined by the load capacitance and the parallel connection of the output resistance of the output stage and the feedback

resistance. The output stage itself will introduce a pole at $p_o = -\frac{\omega_{T_o}}{\beta_{ac_o}}$ under the assumption of current loading. Under the same assumption the input stage will add a pole at $p_i = -\frac{\omega_{T_i}}{\beta_{ac_i}}\frac{R_x+R_s}{R_x}$, where R_x is formed by the input resistance of the input stage and feedback resistance(s), and R_s is the source resistance. Compared to the pole that would be introduced at $\omega_{T_i}/\beta_{ac_i}$, the actual pole location is shifted to a higher frequency due to 'resistive broadbanding'[4].

Table 6.1 presents an overview of the three possible pole combinations and the resulting equations for determining EMI susceptibility. It lists equations for the bandwidth (ω_0) of $A_t(s)$, for $\chi_1(s)$, its maximum value ($\chi_{1,max}$) and the frequency at which it occurs ($\omega_{max} \approx \omega_0$), and $\chi^2_{1,max}D_2(\omega_{max})$. $E_{s,\omega_l}(\omega_c)$ is (among other parameters, see (6.20)) determined by the product $\chi_1(\omega_c)^2D_2(\omega_c)$. The maximum value of $E_{s,\omega_l}(\omega_c)$ at ω_0 is thus determined by $\chi_1(\omega_0)^2D_2(\omega_0)$, which equals $\chi^2_{1,max}D_2(\omega_{max})$.

The first row gives the equations in case p_l and p_o belong to the dominant group, and p_i does not. $\chi_{1,max}$ may reach considerable values for increasing ω_c, depending on the value of ζ and the locations of p_o and p_l. For instance, in case of a voltage amplifier, ξ_{10} has a value of approximately one. $\chi_{1,max}$ may reach a value several times as large as that (overshoot) due to a low value of ζ.

Consider the product $\chi_1(\omega_c)^2D_2(\omega_c)$. The effect of p_o in $D_2(\omega_c)$ is cancelled by the zero in the numerator of $\chi_1(\omega_c)$ that is caused by the same pole. The detrimental effect of the decrease in loop gain due to p_o is thus cancelled by an equal decrease in D_2 due to the same pole, i.e., the output stage contributes less to both loop gain and D_2.

$\chi_1(\omega_c)^2D_2(\omega_c)$ is still determined by the second-order nonlinearity of the output stage as long as $\omega_0 < \omega_k$, which may be the case when $|p_o| > |p_l|$. In case $|p_o| < |p_l|$, it may occur that $\omega_k < \omega_0$. The input stage will now determine the second-order nonlinearity of the negative-feedback amplifier at frequency ω_0.

The solid line in Fig. 6.4 shows an example of $\chi_1(\omega_c)^2D_2(\omega_c)$ when p_l and p_o belong to the dominant group. The output stage is the main contributor to $D_2(\omega_c)$ at ω_0. Between $|p_l|$ and ω_0 there is a +40 dB/dec slope, and for frequencies higher than ω_0 the slope is -20 dB/dec. For frequencies higher than the non-dominant pole the slope is -40 dB/dec. This is the worst combination of the poles and the non-dominant pole discussed in this section; it will result in a large value of $\chi^2_{1,max}D_2(\omega_{max})$ and $\chi_1(\omega_c)^2D_2(\omega_c)$ decreases with a lower slope for frequencies higher than the bandwidth than in the case the dominant group is determined by the other poles (Rows 2 and 3 of Table 6.1). Figure 6.4 shows that the maximal value of $\chi_1(f)^2D_2(f)$ is 44.1 dB at 1.1 MHz, with $f = \omega_c/(2\pi)$. When the approximate equations given in Table 6.1 are used, for $\chi^2_{1,max}D_2(\omega_{max}/(2\pi))$ a value of 43.9 dB is found at 1 MHz.

In case p_o does not belong to the dominant group and p_i and p_l do, the equations presented in row 2 of Table 6.1 can be used to determine the EMI behavior of the negative-feedback amplifier. The equation for $\chi_1(s)$ is similar to the equation found in row 1 of Table 5.3, and therefore the same discussion as given in Section 5.3.1 holds. It also holds that $|p_i| < |p_l|$ results in lower

[4] A comparable discussion holds for FETs.

Table 6.1: Transfer χ_1 of a dual-stage negative-feedback amplifier. The effect of three poles (two belonging to the dominant group (d), one not (nd)) are taken in to account.

Parallel feedback at the output						
			Bandwidth	χ_1		
p_i	p_l	p_o	$\omega_0 \approx \omega_{max}$	$\chi_1(s)$	$\chi_{1,max} \approx$	$\chi^2_{1,max} D_2(\omega_{max}) \approx$
nd	d	d	$\sqrt{p_o p_l (1 - A_1\beta_0\alpha_{20})}$	$\xi_{10} \frac{p_o p_l (1-\frac{s}{p_o})(1-\frac{s}{p_l})}{s^2 - s(p_o+p_l-A_1\beta_0\alpha_{20}\frac{p_o p_l}{z_{ph}}) + (1-A_1\beta_0\alpha_{20})p_o p_l}$	$\frac{\chi_{10}}{2\zeta}\frac{\omega_0}{p_o p_l} \times \frac{1}{\sqrt{\omega_0^2 + (p_l+p_o)^2}}$	$\omega_0 < \omega_k$: $\chi^2_{1,max}\frac{A_1}{A_2^2}\alpha_{20}\frac{1}{\left(1-\frac{j\omega_0}{p_o}\right)^2}a'_{22}$
						$\omega_0 > \omega_k$: $\chi^2_{1,max}\frac{a'_{12}}{A_1}$
d	d	nd	$\sqrt{p_i p_l (1 - A_1\beta_0\alpha_{20})}$	$\xi_{10} \frac{p_i p_l (1-\frac{s}{p_l})}{s^2 - s(p_l+p_i-A_1\beta_0\alpha_{20}\frac{p_i p_l}{z_{ph}}) + (1-A_1\beta_0\alpha_{20})p_i p_l}$	$\frac{\chi_{10}}{2\zeta}\sqrt{\frac{\omega_0^2+p_l^2}{p_l^2}}$	$\chi^2_{1,max}\frac{A_1}{A_2^2}\alpha_{20}a'_{22}$
Series feedback at the output						
d	nd	d	$\sqrt{p_i p_o (1 - A_1\beta_0\alpha_{20})}$	$\xi_{10} \frac{p_o p_i (1-\frac{s}{p_o})}{s^2 - s(p_o+p_i-A_1\beta_0\alpha_{20}\frac{p_o p_i}{z_{ph}}) + (1-A_1\beta_0\alpha_{20})p_o p_i}$	$\frac{\chi_{10}}{2\zeta}\sqrt{\frac{\omega_0^2+p_o^2}{p_o^2}}$	$\chi^2_{10}\frac{A_1}{A_2^2}\alpha_{20}a'_{22}$

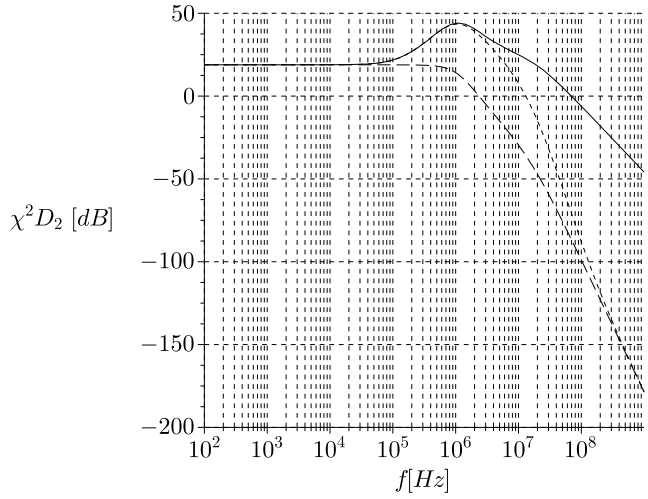


Figure 6.4: An example of $\chi_1(f)^2 D_2(f)$, with $A_1 = 28{\cdot}10^{-3}$ A/V, $A_2 = 80{\cdot}10^{-3}$ A/V, $\alpha_{20} = -304$, $\beta_0 = 1.701$, $a_{12} = 20A_1$, and $a_{22} = 20A_2$. The solid line results from: p_l=-1·10^6 rad/s, p_o=-3·10^6 rad/s, and p_i=-100·10^6 rad/s. The dotted line holds for the case p_l=-1·10^6 rad/s, p_i=-3·10^6 rad/s, and p_o=-100·10^6 rad/s, and the dashed line holds for the case p_o=-1·10^6 rad/s, p_i=-3·10^6 rad/s, and p_p=-100·10^6 rad/s. p_p is a non-dominant pole that may result from the load, but may also originate from some other time constant in the nullor implementation. The bandwidth is 1MHz and $f_k = \omega_k/2\pi \approx 7.8$MHz in all three cases.

values of $\chi_{1,max}$ than in case $|p_i| > |p_l|$. The difference may, however, be less pronounced than in case of the single stage negative-feedback amplifier.

$\chi_1(\omega_c)^2 D_2(\omega_c)$ will show a comparable response as in the previous case and $\chi^2_{1,max} D_2(\omega_{max})$ may have a value equal to the previous case, in case of an equal LP product. Between ω_0 and non-dominant pole $|p_o|$ it, however, decreases with 40 dB/dec. For frequencies higher than $|p_o|$, $\chi_1(\omega_c)$ decreases at a rate of 80 dB/dec. On top of that D_2 decreases with 40 dB/dec between $|p_o|$ and ω_k, at which it stabilizes at a constant value determined by the second-order nonlinearity of the input stage. Between $|p_o|$ and ω_k a maximal decrease of 120 dB/dec of $\chi^2_{1,max} D_2(\omega_{max})$ may thus be expected[5]. $\chi_1(\omega_c)^2 D_2(\omega_c)$ will further decrease with 80 dB/dec for frequencies higher than ω_k.

The dotted line in Fig. 6.4 shows the susceptibility to EMI for this combination of dominant and non-dominant poles. Here, the slope is about -100 dB/dec between $|p_o|$ and ω_k and -80 dB/dec for frequencies higher than ω_k. The maximal

[5]Note that p_o and ω_k may not always be separated by a decade or integer numbers of decades.

value of $\chi_1(f)^2 D_2(f)$ is 43.5 dB at 1.1 MHz, as can be seen in Fig. 6.4. When the approximate equations given in Table 6.1 are used, for $\chi^2_{1,max} D_2(\omega_{max}/(2\pi))$ a value of 42.5 dB is found at 1 MHz.

The case that p_i and p_o are the dominant poles gives comparable results as the previous case. Row 3 presents the equations for this case. Note that dual-stage negative-feedback amplifiers with *series feedback at the output* will show the same behavior as this case. The non-dominant pole usually originates from some time constant in the nullor implementation instead of from a load capacitance, in case of series feedback at the output. Therefore, the non-dominant pole is called p_p instead of p_l.

$D_2(\omega_0)$ is determined by the output stage. The zeros of $\chi_1(\omega_c)^2$ are cancelled by the poles in $D_2(\omega_c)$. Although $\chi_1(\omega_c)$ will show an increase between p_o and ω_o, this increase is cancelled by an equal decrease in $D_2(\omega_c)$. *In case of series feedback at the output we thus have a flat $\chi_1(\omega_c)^2 D_2(\omega_c)$ up to the bandwidth, after which it decreases with frequency. This is the same as the single stage implementation.* The dashed line in Fig. 6.4 shows the response $\chi_1(\omega_c)^2 D_2(\omega_c)$.

$\chi_1(\omega_c)^2 D_2(\omega_c)$ will show a flat response up to ω_0, after which it decreases at a rate of 40 dB/dec. Frequencies higher than the non-dominant pole are attenuated with a rate of 80 dB/dec.

The maximal value of $\chi_1(f)^2 D_2(f)$ is 18.9 dB at 0 Hz (see Fig. 6.4). Note that $\chi_1(\omega_0)^2 D_2(\omega_0)$ is 13.4 dB, almost 6 dB lower, as can be expected. When the approximate equations given in row 3 of Table 6.1 are used, for $\chi^2_{1,max} D_2(\omega_{max}/(2\pi))$ a value of 18.9 dB is found. This equals its value at 0 Hz, which is a reasonable approximation of $\chi_1(\omega_0)^2 D_2(\omega_0)$. We can thus conclude that the approximate equations presented in Table 6.1 are accurate enough for design purposes.

A. $E_{s,\omega_l}(\omega_c)$ with frequency dependent disturbance

Up to now, we have considered the disturbance to be constant since this simplifies the discussion. The disturbance is however frequency dependent as we have seen in Chapter 2. Under assumption of an electrically short interconnect the disturbance increases with 20 dB/dec. For the various combinations of dominant and non-dominant poles as discussed earlier and presented in Fig. 6.4, the resulting $E_{s,\omega_l}(\omega_c)$ in case of a +20 dB/dec disturbance is depicted in Fig. 6.5.

The graphs are normalized in such a way that the maximal value of $E_{s,\omega_l}(\omega_c)$ depicted by the dashed line corresponds to 0 dB. This case may occur, as stated earlier, with series feedback at the output. It can be seen that with equal values of LP, the maximal value of $E_{s,\omega_l}(\omega_c)$ may be up to almost 60 dB lower than the maximal value of $E_{s,\omega_l}(\omega_c)$ in case of parallel feedback at the output (solid line). It clearly demonstrates the advantage of series feedback at the output and disadvantage of parallel feedback at the output.

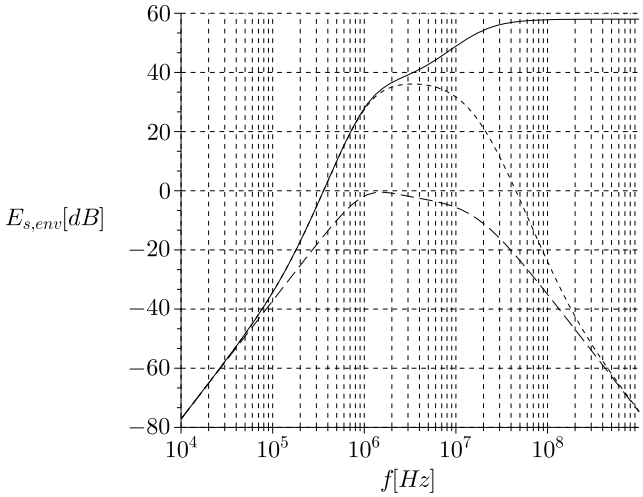


Figure 6.5: An example of $E_s(\omega_l) = E_{s,env}$ for the various pole combinations discussed in the text. The solid line results from: p_l=-1·10^6 rad/s, p_o=-3·10^6 rad/s, and p_i=-100·10^6 rad/s. The dotted line holds for the case p_l=-1·10^6 rad/s, p_i=-3·10^6 rad/s, and p_o=-100·10^6 rad/s, and the dashed line holds for the case p_o=-1·10^6 rad/s, p_i=-3·10^6 rad/s, and p_p=-100·10^6 rad/s. The graphs are normalized so that maximal susceptibility of the latter pole combination corresponds to 0dB.

B. Effect of the non-dominant pole on χ_1

The non-dominant pole has negligible effect on the transfers when it is located at a frequency of approximately 5 times or more than ω_0. Frequently, it is found that the third, non-dominant pole, is located at a lower frequency. This results in peaking in $A_t(\omega_c)$ and $\chi_1(\omega_c)$, even when frequency compensation has been applied. Under assumption of a frequency compensated second-order system with an additional non-dominant pole, the denominator of the expression for $\chi_1(s)$ can be approximated by [2]

$$s^2 - s\left[p_1 + p_2 + \frac{A\beta_0 p_1 p_2}{p_3} - \frac{A\beta_0 p_1 p_2}{z_{ph}}\right] + \omega_0^2. \tag{6.25}$$

Under assumption that $|p_1| < |p_2|$ are dominant poles, $|p_3| > \omega_0$ and z_{ph} is the phantom zero that compensates a second-order system. The effect of p_3 is that p_2 shifts to frequency p_2', with p_2' being equal to

$$p_2' = p_2 + \frac{-\omega_0^2}{p_3}. \tag{6.26}$$

The amount of peaking can be estimated from $\zeta' = -\frac{p_1+p_2'+\omega_0^2/z_{ph}}{2\omega_0}$ and the appropriate equation for $\chi_1(s)$ from Table 6.1. The non-dominant pole causes (extra) peaking in $\chi_{1,max}$ and will thus deteriorate EMI behavior near the upper edge of the bandwidth.

Overcompensation will reduce the peaking, but may not always succeed in completely avoiding peaking. The necessary overcompensation, i.e., the new value of z_{ph}, can be calculated from ζ'.

6.3 E_{s,ω_l} of a dual-stage negative-feedback amplifier

The equivalent source E_{s,ω_l} can be calculated from Equation (6.20). It is, however, convenient for design purposes to have some simplified equations that can be used in the early stages of the design. For each of the four single feedback amplifiers in Fig. 5.2, an approximate equation for E_{s,ω_l} has therefore been determined by deriving an expression for $E_s^2 m\chi_0^2 \frac{1}{\xi_{i0}} D_2(0)$. The approximate equations hold in case $\omega_c < \omega_k$. Further, it has been assumed that the output impedance of the output stage is much larger than the load impedance.

The equations can be adjusted so that they are valid up to the bandwidth ω_0 where the maximal value of E_{s,ω_l} can be expected. This can be done by incorporating the effect of p_o and the expected maximal value of χ_i in the equations. Section 6.6 presents an example of the design of a voltage amplifier using the equations with the effect of p_o accounted for.

Table 6.2 gives an overview of the approximate equations of E_{s,ω_l} for the various negative-feedback amplifiers. The component labels, i.e., R_s, R_t, R_1, etc., correspond to those shown in Figures 5.2 and 5.6 (pages 151 and 177), respectively. The subscripts i and o denote an input stage and output stage quantity, respectively.

It can be seen that E_{s,ω_l} is affected by the load, the feedback network, and the low frequency second-order nonlinearity factor of the amplifier, $D_2(0)_{\text{amp}}$. $D_2(0)_{\text{amp}}$ for every type of two stage nullor implementation is given by

$$D_2(0)_{\text{amp}} = \left(\frac{a_{12}'}{A_i^2 \alpha_{20}^2} + \frac{a_{22}'}{\alpha_{20} A_2^2} \right). \tag{6.27}$$

$D_2(0)_{\text{amp}}$ is affected by both input and output stage parameters. To get the relations between second-order nonlinearity and component and bias parameters clear, $a_{12}'/(A_i^2\alpha_{20}^2)$ and $a_{22}'/(\alpha_{20}A_2^2)$ are investigated, subsequently some design rules will be presented.

A. Second-order nonlinear dependencies of the input stage

The input can be a single BJT, FET or a differential stage (BJT or FET). Here, the single stages are considered. The differential input stage is considered in Subsection 6.3.2. Most conclusions given here, are, however, valid for both single and differential stage.

Table 6.2: Overview of E_{s,ω_l} for the various dual-stage negative-feedback amplifiers. See text for the conditions under which these equations are valid approximations.

	$u_{s,env}/i_{s,env} \sim$	BJT input	FET input
voltage amplifier:	$u_s^2 m \left(\frac{R_1+R_2+R_l}{R_2 R_l}\right)^2 \cdot \left(\frac{1}{A_i}c+d\right) D_2(0)_{\text{amp}}$	$c=1, d=\frac{R_s+R_2//(R_1+R_l)}{\beta_{aci}}$	$c=1$ $d=0$
transadmittance amplifier:	$u_s^2 m \frac{1}{R_t^2} \cdot \left(\frac{1}{A_i}c+d\right) D_2(0)_{\text{amp}}$	$c=1, d=\frac{R_s+R_t}{\beta_{aci}}$	$c=1$ $d=0$
transimpedance amplifier:	$i_s^2 m \left(\frac{R_t+R_l}{R_l}\right)^2 \cdot \left(\frac{1}{A_i}c+d\right) D_2(0)_{\text{amp}}$	$c=\frac{R_s+R_t+R_l}{R_s(R_t+R_l)}, d=\frac{1}{\beta_{aci}}$	$c=1$ $d=0$
current amplifier:	$i_s^2 m \left(\frac{R_1+R_2}{R_2}\right)^2 \cdot \left(\frac{1}{A_i}c+d\right) D_2(0)_{\text{amp}}$	$c=\frac{R_s+R_1+R_2}{R_s(R_1+R_2)}, d=\frac{1}{\beta_{aci}}$	$c=1$ $d=0$

The contribution of the input stage to $D_2(0)_{\text{amp}}$ depends on the current gain of the output stage. It is assumed that a BJT output stage is current driven, thus resulting in $\alpha_{20} = -\beta_{ac_o}$. When the output stage is a FET, the current gain $\alpha_2(\omega) = -\omega_T/\omega$ and can thus be very high at low frequencies like ω_l. It can thus be expected that the current gain of the output stage is limited by the output resistance of the input stage at ω_l: $\alpha_{20} = -r_{oi}g_{m1_o} = -r_{oi}A_2$.

In case of parallel feedback at the input (e.g., a current amplifier), the constraint $(R_s + R_t) \gg r_{\pi_i}$ usually holds for the BJT input stage. The contribution that the input stage makes to the second-order nonlinearity of the amplifier depends on the type of output stage, and is given by

$$\begin{aligned} \frac{a'_{12}}{A_i^2\alpha_{20}^2} \approx & \quad \frac{n_f kT}{q}\frac{1}{2I_{cQ_i}^2\beta_{ac_o}^2}\left[\frac{\beta_{ac_i}}{(R_s+R_t)} + \frac{q}{n_f kT}I_{cQ_i}(1-x)\right] \\ & \qquad (\text{BJT output} - \text{stage}) \\ & \qquad \text{and} \\ \frac{a'_{12}}{A_i^2\alpha_{20}^2} \approx & \quad \frac{n_f kT}{q}\frac{1}{8\beta_{\text{FET}_o}U_{AF_i}^2 I_{dQ_o}}\left[\frac{\beta_{ac_i}}{(R_s+R_t)} + \frac{q}{n_f kT}I_{cQ_i}(1-x)\right] \\ & \qquad (\text{FET output} - \text{stage}). \end{aligned} \tag{6.28}$$

The current gain of the output stage is β_{ac_o}. U_{AF_i} and β_{ac_i} are the Early voltage and the current gain of the input BJT, respectively, and β_{FET_o} is the transconductance factor of the output FET. Parameter x is the ratio of $g_{\pi 2}$ and g_{m2}/β_{ac} (see Chapter 3).

Large values of R_s and feedback resistance R_t (or the equivalent resistance of the feedback network) are beneficial for a low value of $a'_{12}/(A_i^2\alpha_{20}^2)$. However, the uncertainty in the exact value of $a'_{12}/(A_i^2\alpha_{20}^2)$ then increases, because the influence of the $(1-x)$ term increases also. For a BJT biased in the mid-current region it is expected that $0.97 \leq x \leq 1.03$, as has been argued in Chapter 3. In the special case that $R_s + R_t \to \infty$, Equation (6.28) reduces to $(1-x)/(2I_{cQi}\beta_{ac_o}^2)(n_f kT)/(q)$ and $(1-x)I_{cQi}/(8\beta_{\text{FET}_o}U_{AF_i}^2 I_{dQ_o})(n_f kT)/(q)$, respectively, and may therefore reach low values. It is expected that Equation (6.28) gives pessimistic results, since some (small) linearizing effects have been disregarded in deriving the approximation.

In case of series feedback at the input, it usually follows from noise considerations that $r_{\pi_i} \gg R_s//R_{\text{equivalentfeedback}}$. For the contribution that the input stage makes to the second-order nonlinearity of the amplifier, it is now found

$$\begin{aligned} \frac{a'_{12}}{A_i^2\alpha_{20}^2} \approx & \quad \frac{1}{2I_{cQi}\beta_{ac_o}^2} \qquad (\text{BJT output} - \text{stage}) \\ & \qquad \text{and} \\ \frac{a'_{12}}{A_i^2\alpha_{20}^2} \approx & \quad \frac{I_{cQi}}{8\beta_{\text{FET}_o}U_{AF_i}^2 I_{dQ_o}} \quad (\text{FET output} - \text{stage}). \end{aligned} \tag{6.29}$$

As can be seen, the input stage contributes more to second-order nonlinearity of the amplifier in case of series feedback at the input than in case of parallel feedback at the input.

For a cascoded FET input stage, it holds

$$\begin{aligned} \frac{a'_{12}}{A_i^2\alpha_{20}^2} &\approx \frac{I_{dQ_i}}{16\beta_{\mathrm{FET}_o}(\beta_{ac_i}U_{AF_i})^2} \quad (\mathrm{FET}-\mathrm{BJT}-\mathrm{cascode}) \\ &\text{and} \\ \frac{a'_{12}}{A_i^2\alpha_{20}^2} &\approx \frac{\lambda_i^4}{64\beta_{\mathrm{FET}_i}\beta_{\mathrm{FET}_o}}\frac{I_{dQ_i}^2}{I_{dQ_o}} \quad (\mathrm{FET}-\mathrm{FET}-\mathrm{cascode}). \end{aligned} \tag{6.30}$$

β_{FET_i} and λ_i are the transconductance factor and the channel length modulation factor of the input FET, respectively.

Term $a'_{12}/(A_i^2\alpha_{20}^2)$ is inversely proportional to α_{20}^2. When this term is too large it can thus be reduced by increasing the current gain of the output stage. This may be accomplished by, e.g., selecting or designing a transistor with a larger current gain. A BJT output stage should thus have a high β_{ac_o}, preferably as high as possible. In case of a FET output stage, U_{AF_i}, β_{FET_o} and β_{FET_i} should have values as high as possible.

The output stage should be biased at a larger current than the input stage. The other way around will increase $a'_{12}/(A_i^2\alpha_{20}^2)$ in case of a FET output stage. Increasing I_{cQ_i} will be beneficial when both input and output stage are implemented with a BJT.

Typically, a FET input stage will show a smaller value of $a'_{12}/(A_i^2\alpha_{20}^2)$ than a BJT input stage.

B. Second-order nonlinear dependencies of the output stage

The ratio $a'_{22}/(A_2^2\alpha_{20})$ of a single output stage can be written as

$$\begin{aligned} \frac{a'_{22}}{A_2^2\alpha_{20}} &\approx \frac{n_f kT}{q}\frac{1}{2I_{cQ_o}^2}\left[\frac{I_i}{\Upsilon}+\frac{q}{n_f kT}\frac{I_{cQ_o}}{\beta_{ac_o}}(1-x)\right] \quad (\mathrm{BJT}) \\ &\text{and} \\ \frac{a'_{22}}{A_2^2\alpha_{20}} &= \frac{1}{8I_{dQ_o}\sqrt{\beta_{\mathrm{FET}}I_{dQ_o}}}\frac{I_i}{\Upsilon} \quad (\mathrm{FET}), \end{aligned} \tag{6.31}$$

with

$$\begin{aligned} \mathrm{BJT\ input-stage}: &\quad I_i = I_{cQ_i}, \quad \Upsilon = U_{AF_i} \\ \mathrm{BJT}-\mathrm{BJT}-\mathrm{cascode}: &\quad I_i = I_{cQ_i}, \quad \Upsilon = \beta_{ac_i}U_{AF_i} \\ \mathrm{FET}-\mathrm{BJT}-\mathrm{cascode}: &\quad I_i = I_{dQ_i}, \quad \Upsilon = \beta_{ac_i}U_{AF_i} \\ \mathrm{FET}-\mathrm{FET}-\mathrm{cascode}: &\quad I_i = I_{dQ_i}, \quad \Upsilon = \frac{2}{\lambda^2}\sqrt{\frac{\beta_{\mathrm{FET}}}{I_{dQ_i}}}, \end{aligned}$$

when a current driven output stage is assumed.

Comparable equations for I_i and Υ can be found when a differential stage is used as input stage. I_i in that case, may be replaced by $I_{T_i}/2$ (halve the tail current of the input stage) for instance.

The second-order nonlinearity factor a'_{22} of differential output stages can be approximated by Equations (4.38) and (4.45), under the conditions given in Chapter 4. In case of a differential BJT output stage, $a'_{22}/(A_2^2\alpha_{20})$ is found to be

$$\frac{a'_{22}}{A_2^2\alpha_{20}} \approx \frac{2}{I_{cQ1_o}\beta_{ac_o}} \frac{1}{\frac{q}{n_f kT}\frac{I_{cQ1_o}}{I_i}\frac{\Upsilon}{\beta_{ac_o}} + 1 + \frac{\delta}{\upsilon}} \frac{\upsilon}{\upsilon+\Lambda}\left(1+\delta\frac{\Lambda}{\upsilon}\right) \times \left[\frac{\upsilon^2\left(1+\frac{R_{l1}}{r_{o1}}\right)^2 - \left(1+\frac{R_{l2}}{r_{o2}}\right)^2}{\left[\upsilon\left(1+\frac{R_{l1}}{r_{o1}}\right) + \left(1+\frac{R_{l2}}{r_{o2}}\right)\right]^2}\right]^2, \tag{6.32}$$

and in case of a differential FET output stage

$$\frac{a'_{22}}{A_2^2\alpha_{20}} \approx \frac{(1+\delta\upsilon)^3}{8I_{dQ_1}\sqrt{\beta_{\mathrm{FET}_1}I_{dQ_1}}\delta\upsilon\sqrt{\delta\upsilon}} \frac{I_i}{\Upsilon} \frac{1+\Lambda\upsilon[1+\lambda_1 I_{dQ_1}(R_{l1}+R_{l2})]}{\Lambda\upsilon(1+R_{l1}\lambda_1 I_{dQ_1})} \times \frac{\upsilon\sqrt{\delta\upsilon}(1+\lambda_1 R_{l1} I_{dQ_1})^2 - (1+\Lambda\lambda_1\upsilon R_{l2} I_{dQ_1})^2}{\left[1+\Lambda\lambda_1\upsilon R_{l2} I_{dQ_1} + \sqrt{\delta\upsilon}(1+\lambda_1 R_{l1} I_{dQ_1})\right]^2} \frac{\delta}{\sqrt{\delta\upsilon}} \frac{\Lambda\upsilon}{\Lambda\upsilon+1}, \tag{6.33}$$

is found. Currents I_{cQ1_o} and I_{dQ1_o} are the bias currents of the first (left) transistor of the differential stage (see Fig. 4.5(a), Chapter 4). For the differential BJT output stage holds $\upsilon = I_{cQ2_o}/I_{cQ1_o}$, $\delta = \beta_{ac2_o}/\beta_{ac1_o}$, and $\Lambda = U_{AF2_o}/U_{AF1_o}$; for the differential FET stage holds $\upsilon = I_{dQ2_o}/I_{dQ1_o}$, $\delta = \beta_{\mathrm{FET}_2}/\beta_{\mathrm{FET}_1}$, and $\Lambda = \lambda_2/\lambda_1$. I_i and Υ have the same meaning as stated before.

All the equations in this subsubsection show that $a'_{22}/(A_2^2\alpha_{20})$ decreases with increasing bias current of the output stage. They also show that the bias current of the output stage should in general be larger than the bias current of the input stage.

Similar to the input stage, $a'_{22}/(A_2^2\alpha_{20})$ is inversely dependent on the current gain of the output stage. The same conclusions regarding the transistor parameters can thus be drawn. Cascoding the input stage also reduces $a'_{22}/(A_2^2\alpha_{20})$ of a differential output stage, since Υ will increase in that case.

Since both β_{FET} and I_{dQ} are in the order of magnitude of $10^{-6} - 10^{-3}$, it is expected that $a'_{22}/(A_2^2\alpha_{20})$ in case of a single FET output stage is typically larger than $a'_{22}/(A_2^2\alpha_{20})$ in case of a single BJT output stage. Typically, it may thus be expected that a BJT output stage causes a lower E_{s,ω_l} than a FET output stage.

When it is found that $a'_{22}/(A_2^2\alpha_{20})$ can not be made small enough to meet the E_{s,ω_l} demand, a single output stage may be replaced by a differential output stage. As long as $r_{o1}, r_{ds1} \gg R_{l1}$ and $r_{o2}, r_{ds2} \gg R_{l2}$, respectively, this will result in a much smaller value of $a'_{22}/(A_2^2\alpha_{20})$ than in case of a single output stage. Cascoding the differential output stage could be a possibility to ensure this. In case of perfect balance $a'_{22}/(A_2^2\alpha_{20})$ even equals zero.

It depends on the amount of imbalance (i.e., the values of υ, δ, and Λ) whether a differential FET or a differential BJT output delivers the largest value of $a'_{22}/(A_2^2\alpha_{20})$. For equal amounts of imbalance, it is found that typically a differential FET output stage will generate the largest value of $a'_{22}/(A_2^2\alpha_{20})$.

Hence, a differential BJT output stage should be favored over a differential FET stage under these assumptions.

The observation made in [60] that the contribution an active device can make to the loop gain is of more importance for low distortion than its inherent nonlinearity, is endorsed by the equations presented here, since second-order distortion will typically be caused by the output stage because $\frac{a'_{12}}{A_i^2\alpha_{20}^2} \ll \frac{a'_{22}}{A_2^2\alpha_{20}}$. The same is true for EMI as long as the output stage is dominating the second-order nonlinearity. Although this observation follows directly from the discussion so far, it can be considered fairly important since it is in contradiction with the common believe that a more 'linear' active device will automatically result in more linear behavior of the negative-feedback amplifier.

As long as $\frac{q}{n_f kT}\frac{I_{T_o}}{2}\frac{r_{oi}}{\beta_{ac}} \gg \frac{\upsilon+\delta}{\upsilon}$, $D_2(0)_{\text{amp}}$ will decrease more or less inversely proportional to $I_{T_o}^2$ (I_{T_o} being the tail current of the differential stage) when the output stage dominates the second order nonlinearity. When the condition is not satisfied, $D_2(0)_{\text{amp}}$ will decrease proportionally to I_{T_o}. In case of a differential FET output stage it is found $D_2(0)_{\text{amp}}$ will decrease proportionally to $I_{T_o}\sqrt{I_{T_o}}$.

Note that in general, cascoding the output stage has as advantage that the detrimental effect of g_x (Chapter 3) is made ineffective. This may specifically be effective in case of parallel feedback at the output, since in that case large voltage swings may occur across the collector-base/emitter and drain-source junction, respectively.

C. Active part implementation

An active part consisting of an input and output stage may be implemented by one of the combinations listed in Table 6.3. Local feedback in the active part

Table 6.3: Possible combinations of a dual-stage active part.

Input stage:	Output stage:
differential BJT	single BJT
differential BJT	single FET
single BJT	differential BJT
single BJT	differential FET
differential FET	single FET
differential FET	single BJT
single FET	differential FET
single FET	differential BJT
differential BJT	differential FET
differential FET	differential BJT

of the negative-feedback amplifier should be avoided, which is possible with the proper choice of one of these combinations.

The choice for the kind of input or output stage may be based on the kind of feedback used. A differential input stage may be convenient in case of series feedback at the input. Both signal source and feedback network can be connected in a straightforward manner to the bases/gates of the input stage. Offset voltages at the input are conveniently low. That S_{u_n} is twice as large as in the case of a single transistor may not be that harmful. The noise constraints can usually still be met. E_{s,ω_l} is determined by the output stage when $\omega_c \ll \omega_k$; when $\omega_c \gg \omega_k$, the differential input stage determines E_{s,ω_l}.

A differential output stage is the best choice when we have series feedback at the output. Using a single transistor would result in a form of local feedback at the output, which should be avoided.

In case of parallel feedback at the output, the choice for a single transistor or differential pair is not that obvious. Both can be used to satisfy the driving and bandwidth demands. The choice should thus be based on the value of E_{s,ω_l} when $\omega_c \ll \omega_k$. If the demands on E_{s,ω_l} are met with a single transistor, this implementation can be used. Otherwise the differential implementation should be used.

Parallel feedback at the input may result in both a single transistor and a differential pair implementation of the input stage. Under assumption that the noise constraints can be met with either implementation, the choice is based on E_{s,ω_l} in case $\omega_c \gg \omega_k$. If the demands on E_{s,ω_l} can be met with a single transistor, this is the obvious choice, otherwise the differential implementation of the input stage should be used.

The choice for FET or BJT input stage has to be made on basis of the SER demands. Here, it is proposed to determine the preliminary choice on basis of noise calculations. From this follows either the use of a BJT or FET. Next, E_{s,ω_l} can be approximated and checked at very high frequencies ($\omega_c \gg \omega_0$). If E_{s,ω_l} is found to be too large in case of a BJT implementation (single or differential), a FET input stage may now considered (single or differential) since they usually result in a smaller a'_{12}/A_i when the bias current of the FET(s) is not too low. Noise is expected to increase, so it should be checked whether the SER demands are met.

The preferred output stage is implemented with BJTs as the previous discussions have shown. Obviously, when only FET technology is at the designer's disposal the FET should be used. As a result it may follow that a differential implementation of the FET output stage is required, while a single BJT output stage would suffice.

6.3.1 Generally valid design rules

Some generally valid design rules follow from the equations given in Table 6.2 and the discussion in the previous sections. They hold for both EMI and distortion behavior.

1. The kind of feedback at the output has a large impact on E_{s,ω_l}. Series feedback at the output is the preferred kind of feedback, since it will typ-

ically result in the lowest $E_{s,\omega_l}(\omega_0)$ (because $\chi_{1,max}$ is the lowest in this case, see Subsections 5.3.1 and 6.2.4). If it does not matter whether the load is voltage or current driven, series feedback at the output should be chosen.

2. The contribution to E_{s,ω_l} of the input stage is inversely proportional to α_{20}^2 and the contribution of the output stage is inversely proportional to α_{20} (see Section 6.3). The low frequency current gain of the output stage should therefore be high.

3. Typically, a BJT output stage will result in a lower E_{s,ω_l} than a FET output stage. At such high frequencies ($\omega_c \gg \omega_k, \omega_0$) that the input stage determines E_{s,ω_l}, typically a FET input stage will be more beneficial for a low E_{s,ω_l} than a BJT input stage. See Section 6.3.

4. Amplifiers with parallel feedback at the output suffer from the load resistance (R_l) (see Subsection 5.2.4 and Section 6.3). The lower R_l is with respect to the value of the feedback network, the higher the value of E_{s,ω_l}. For a given E_{s,ω_l} and R_l, the maximum value of the feedback network can be determined. A too low impedance of the feedback network may, however, increase E_{s,ω_l}. The output transistor may for instance have to be biased in the high-current region. A trade-off has now to be made between the impedance of the feedback network and the bias current of the output transistor.

5. High amplification factors negatively affect E_{s,ω_l} (see Section 6.3; Table 6.2). It is harder to design for low E_{s,ω_l} when, e.g., $\mu = 10$ than when $\mu = 100$ under assumption of equal $A_1\alpha_{20}\beta$.

6. The parallel connection of the source resistance and the feedback network should have a value as large as possible in case of parallel feedback at the input (see Section 6.3; Table 6.2). Since the source resistance is usually large, this means that the feedback network should be designed for large values. This is also beneficial for low noise performance (see Section 5.2.3).

7. In case of a FET input stage, the contribution to E_{s,ω_l} of the input stage is inversely proportional to A_i^3, and the contribution of the output stage is inversely proportional to A_i (see Section 6.3).

8. $D_2(0)_{\text{amp}}$ can be decreased by increasing the bias currents. Increasing the bias current of the output stage is most beneficial since this decreases the contribution of the output stage and may also decrease the contribution of the input stage to $D_2(0)_{\text{amp}}$ (see Section 6.3).

9. The bias current of the output stage should be larger than the bias current of the input stage (see Section 6.3).

10. In case of a BJT as output stage, a device with a large β_{ac} should be favored over a device with a lower value of β_{ac}. The current gain of a FET

is characterized by a pole in the origin. Its value is dependent of the ratio of the FETs transit frequency (ω_T) and the frequency of ω_l. Therefore a FET with a high ω_T should favored over a FET with a lower value of ω_T. See Section 6.3.

6.3.2 Differential input stage

Although it is typically unlikely that a differential input stage would determine $E_{s,\omega_l}(0)$ and $E_{s,\omega_l}(\omega_0)$, yet, its second-order nonlinear behavior will be investigated in more detail in this subsection. Although the design conclusions given in Chapter 4 still hold, it was found that Equations (4.38) and (4.45) may result in relatively large errors when applied to the differential input stage in case of series feedback at the input[6]. The feedback action and network both have an effect on the difference between $|E_{in1}|$ and $|E_{in2}|$, thus influencing the total second-order nonlinear behavior of the differential input stage. Note that this effect does not occur in the differential output stage. Equations (4.38) and (4.45) are in this case accurate enough for the first design steps.

It is possible to derive a complete superposition model for a negative-feedback amplifier with differential input and single or differential stage output. However, here it is chosen to derive equations from a simpler model, since slightly less accurate equations are good enough to get an impression of the second-order nonlinear behavior of the differential input stage. The first stage in Fig. 6.3 (Page 194) can be substituted by the model of a differential stage of Fig. 4.7 (page 117), and ξ_{12} and ξ_{22} are substituted by feedback factors β_{i1} and β_{i2}, respectively. E_{s2} is replaced by the output stage signal. Finally, to ease the calculation, we assume the total transconductance from the differential stage to be approximated by $A_i \approx A_{i1}A_{i2}/(A_{i1} + A_{i2})$. A_{i1} and A_{i2} are the transconductances of both transistors of the differential stage. This approximation is usually accurate enough for design, especially when the output resistance of the differential stage is large compared to the input resistance of the output stage (see Subsections 4.5.1 and 4.5.2).

In case of a differential input stage, the input signals can now be approximated by

$$E_{in1} = E_s \frac{\xi_{i1}(1 - A_i\alpha_2\beta_{i2} - A_{i2}\kappa_{22}) + \xi_{i2}(A_i\alpha_2\beta_{i1} + A_{i2}\kappa_{22})}{1 - (A_{i1}\kappa_{11} + A_{i2}\kappa_{22}) - A_i\alpha_2\beta(1 - A_{i1}\kappa_{21} - A_{i2}\kappa_{12})} \tag{6.34}$$

and

$$E_{in2} = E_s \frac{\xi_{i1}(-A_i\alpha_2\beta_{i2} + A_{i1}\kappa_{11}) - \xi_{i2}(-1 - A_i\alpha_2\beta_{i1} + A_{i1}\kappa_{11})}{1 - (A_{i1}\kappa_{11} + A_{i2}\kappa_{22}) - A_i\alpha_2\beta(1 - A_{i1}\kappa_{21} - A_{i2}\kappa_{12})}. \tag{6.35}$$

β_{i1} and β_{i2} are the feedback factors to both transistors. κ_{11}, κ_{12}, κ_{21}, and κ_{22} are the local feedback factors originating from the impedance of the tail current source, as discussed in Chapter 4.

[6]This may also be the case when the amplifier has a differential output stage too. See Appendix D for an accurate model for negative-feedback amplifiers having differential input and differential output stages..

Further, it holds

$$\begin{aligned} E_d = E_{in1} - E_{in2} &= E_s \xi_i \frac{1 - (A_{i1}\kappa_{11} + A_{i2}\kappa_{22})}{1 - (A_{i1}\kappa_{11} + A_{i2}\kappa_{22}) - A_i\alpha_2\beta(1 - A_{i1}\kappa_{21} - A_{i2}\kappa_{12})} \\ &\equiv E_s \frac{\xi_i}{1 - A_i\alpha_2\beta} = E_s\chi_i, \end{aligned} \tag{6.36}$$

and $\xi_i = \xi_{i1} - \xi_{i2}$.

Under the assumption that $-\xi_{i1}\beta_{i1} + \xi_{i2}\beta_{i2} \ll \beta(\xi_{i1} + \xi_{i2})$ and $\kappa_{11} \approx \kappa_{21}, \kappa_{12} \approx \kappa_{22}$ χ_{i1} and χ_{i2} can be approximated by

$$\begin{aligned} \chi_{i1} \approx &\chi_i \left(\frac{-A_{i2}\kappa_{22}}{1 - (A_{i1}\kappa_{11} + A_{i2}\kappa_{22})} + \frac{\xi_{i1} - A_i\alpha_2\beta(\xi_{i1} + \xi_{i2})}{\xi_i(1 - (A_{i1}\kappa_{11} + A_{i2}\kappa_{22}))} \right) \\ &\text{and} \\ \chi_{i2} \approx &\chi_i \left(\frac{A_{i1}\kappa_{11}}{1 - (A_{i1}\kappa_{11} + A_{i2}\kappa_{22})} + \frac{\xi_{i2} - A_i\alpha_2\beta(\xi_{i1} + \xi_{i2})}{\xi_i(1 - (A_{i1}\kappa_{11} + A_{i2}\kappa_{22}))} \right). \end{aligned} \tag{6.37}$$

Transfers $|\chi_{i1}|$ and $|\chi_{i2}|$ should be as equal as possible. In case of FETs, however, considerable differences may occur at low frequencies due to the fact that $|\xi_{i2}|$ is much smaller than $|\xi_{i1}|$. In case of BJTs it is expected that the differences between $|\chi_{i1}|$ and $|\chi_{i2}|$ are less pronounced.

The second-order nonlinearity of the input stage, a'_{12}, is now approximated by

$$\begin{aligned} a'_{12} \approx &- \chi_{i1}^2 \left[a_{12} + b_{12} \left(A_{i1}\gamma_{11,\omega_l} + A_{i2}\gamma_{21,\omega_l} \frac{\nu_{2,\omega_l}}{\nu_{1,\omega_l}} \right) \right] \frac{A_{i2}}{A_{i1} + A_{i2}} + \\ &\chi_{i2}^2 \left[a_{22} + b_{22} \left(A_{i1}\gamma_{12,\omega_l} \frac{\nu_{1,\omega_l}}{\nu_{2,\omega_l}} + A_{i2}\gamma_{22,\omega_l} \right) \right] \frac{A_{i1}}{A_{i1} + A_{i2}}, \end{aligned} \tag{6.38}$$

under the assumption of adequate loop gain, e.g., $-A_i\alpha_2\beta \geq 10$. Coefficients b_{11} and b_{12} are zero in case of a FET differential stage and have non-zero values in case of a BJT differential stage.

Single-ended loading of a BJT differential stage results in significantly differing values of ξ_{i1}, ξ_{i2} and κ_{11}, κ_{22}. Transfers $|\chi_{i1}|$ and $|\chi_{i2}|$ will therefore also differ. On top of that, $|\nu_{1,\omega_l}|$ and $|\nu_{2,\omega_l}|$ differ substantially, thus increasing the value of $|a'_{12}|$. Differential loading may reduce the difference in values in these variables and, hence, make $|\chi_{i1}|$, $|\chi_{i2}|$, and $|\nu_{1,\omega_l}|$, $|\nu_{2,\omega_l}|$ more equal. This will result in a smaller value of $|a'_{12}|$.

Equations (6.37) and (6.38) can be used to approximate the contribution of the input stage to $E_{s,\omega_l}(\omega_c)$, specifically when $\omega_c > \omega_0$ and $\omega_c > \omega_k$. It can be expected that this contribution is negligible at low frequencies, at which the output stage will typically dominate.

In case $\omega_c \gg \omega_0, \omega_k$, it is expected that feedback, both from the κ-s and β, is completely ineffective. The equivalent feedback resistance causes $|E_{in2}|$ to be

much smaller than $|E_{in1}|$. Now, χ_{i1} will be almost equal to χ_i. For the BJT differential stage it is now found

$$a'_{12} \approx \frac{1}{2}\left(\frac{q}{n_f kT}\right)^2 I_{cQ_1} \frac{\upsilon}{1+\upsilon}\frac{\upsilon\delta}{\delta+\upsilon}\frac{\left(1+\delta\frac{R_v}{r_{o1}}\right)}{1+\frac{R_s+R_x}{r_{\pi_1}+r_{\pi_2}}}, \tag{6.39}$$

with R_x being equal to R_t for the transadmittance amplifier and $R_x = R_2//(R_1+R_l)$ in case of a voltage amplifier. R_v equals r_{o2} in case of differential loading and $R_v \approx r_{o2}//(R_s+r_{\pi 1})//(R_x+r_{\pi 2})$ in case of single-ended loading of the first transistor (Q_1) (see Fig. 4.5). If it is assumed that $\upsilon = \delta = 1$ and that $R_s + R_x \ll r_{\pi_1} + r_{\pi_2}$, this equation reduces to

$$a'_{12} \approx \frac{1}{4}\left(\frac{q}{n_f kT}\right)^2 I_{cQ_1}. \tag{6.40}$$

For the FET differential stage at very high frequencies follows

$$a'_{12} \approx \beta_{\mathrm{FET}_1}\frac{\sqrt{\upsilon\delta}}{1+\sqrt{\upsilon\delta}}. \tag{6.41}$$

Again, when it is assumed that $\upsilon = \delta = 1$, this equation reduces to

$$a'_{12} \approx \frac{1}{2}\beta_{\mathrm{FET}_1}. \tag{6.42}$$

It may thus be concluded that at very high frequencies when there is no effective series feedback action anymore (and the second transistor (Q_2, M_2) of the differential stage is made ineffective), the second-order nonlinearity of a differential stage is about halve the value of the second-order nonlinearity of a single transistor.

Note that in case of parallel feedback at the input there is no feedback resistance that causes $|E_{in2}|$ to have a significantly lower value than $|E_{in1}|$. At very high frequencies χ_{i1} and χ_{i2} can be approximated by $\chi_{i1} \approx \chi_i(C_{in2}+C_T)/(C_{in1}+C_{in2}+C_T)$ and $\chi_{i2} \approx \chi_i(C_{in1})/(C_{in1}+C_{in2}+C_T)$, respectively. C_{in1} and C_{in2} are the input capacitances of both transistors and C_T is the capacitance of the tail current source. Using (6.38), the nonlinearity of the differential input stage can be approximated.

When the designer is interested in a more accurate model for analysis of $E_{s,\omega_l}(\omega_c)$, he is referred to Appendix D. The appendix presents a model of a dual stage negative-feedback amplifier with differential input and differential output stages. It can also be used in case of a unbalanced output stage by making the transfers of one of the output devices zero.

Although this model is accurate, it does not lend itself for design purposes due to the large equations. As a first design step the methods proposed in this chapter are recommended, after which a detailed analysis may be performed using the model of Appendix D.

6.4 Technology considerations

The choice for BJT or FET input stage is in principle based on noise considerations and the choice of output stage is based on nonlinearity considerations. Both input and output stage should contribute as much as possible to the LP product. After all, the LP product should be high enough to meet bandwidth, distortion, and EMI constraints. As was shown, ω_T equals the maximal contribution one transistor can make.

Modern BJTs may have an ω_T as high as 94 Grad/s to 280 Grad/s [105]. Discrete BJTs with an ω_T between 600 Mrad/s and 56 Grad/s are commonly available (e.g., [126][151]). A BJT should preferably combine a high ω_T with a high β_{ac} and a high Early voltage U_{AF}. The BJT should be selected or designed and biased for these criteria. The current gain can be maximized by minimizing the base width and maximizing the ratio of emitter to base doping densities in homojunction BJTs [57]. Typically, β_{ac} lies between 100 and 1000 [57] (discrete BJTs show comparable figures for β_{ac} (e.g., [126][151])). The Early voltage, however, is inversely proportional to the base width and is typically 15 to 100 V for integrated-circuit BJTs [57]. A trade-off between β_{ac} and U_{AF} could be made. It is recommended to design the BJT for a high β_{ac} and to accept a possible decrease of U_{AF}. A too low U_{AF} can easily be compensated for by cascoding the BJT.

Preferably, the mid-current region should cover a large current region. Specifically currents in the low-current region negatively affect the nonlinearity of the BJT, as is argued in Chapter 3. To lower the boundary current $I_{cQ_{min}}$, the base-emitter leakage saturation current I_{se} should be small with respect to saturation current I_s. A high current gain is also beneficial for a low value of $I_{cQ_{min}}$.

The specific resistivity of the base (r_B) (that may vary from less than 10 Ω up to 500 Ω [57]) may have an adverse effect both on the small-signal (and transient) responses and on the noise performance of a negative-feedback amplifier (see Chapter 5) [3]. For a low r_B, the periphery of the emitter that is adjacent to the base contact can be maximized by, e.g., applying multiple base and emitter stripes [57].

When the ω_T (and β_{ac}) demand can not be met using conventional (homojunction) BJTs, heterojunction BJTs can be considered. Heterojunction BJTs use differing semiconductor materials for the base and emitter regions [57]. It is possible to decrease the emitter doping and increase the base doping compared to the homojunction BJT. An increase in ω_T while r_B remains constant and an increase in U_{AF} can now be obtained [57]. Heterojunction BJTs with an ω_T higher than $3{\cdot}10^{12}$ rad/s, and a β_{ac} between 65 and 115 have been reported[7] [152][153].

A FET should combine a high β_{FET} and high ω_T. The transit frequency is approximated by $\omega_T \approx 1.5\mu_n/L^2(U_{gs}-U_t)^2$ [57], and $\beta_{\mathrm{FET}} \sim W/L$ (see Chapter 3). Both ω_T and β_{FET} will thus increase with decreasing channel length (L).

[7] Note that the low breakdown voltages (ca. 1.5 V) reported in [152][153] limit the use of these heterojunction BJTs in the amplifiers that follow from the design method described in this work.

For the latter, it is beneficial when the width (W) of the FET is larger than L. For example, very high values of ω_T ($119{\cdot}10^9$rad/s$-1{\cdot}10^{12}$ rad/s) have been reported for short channel MOSFETs (L: 50 nm$-$250 nm; W: 330 μm$-$65 μm) [108]. Although no figures of $\beta_{\rm FET}$ are given in the paper, it is estimated from the figures given that $\beta_{\rm FET}$ should be in the order of several (tens of) A/V^2. In very high frequency applications, a short channel is therefore often chosen. Cascoding the FET increases the low value of the drain-source (output) resistance, cancels the nonlinear effects of channel length modulation (CLM), and by choosing a not too high drain-source bias voltage, the contribution of hot electrons to the drain current can be kept small.

As was discussed in Chapter 3, CLM increases with decreasing L and secondary effects like hot electrons are more likely to be a problem in short channel MOSFETs. A trade-off between $\beta_{\rm FET}$, ω_T and the detrimental effects of too short channels can thus be made. When the amplifier is intended for moderate frequencies, e.g., several (tens of) MHz, longer channel devices can be chosen. For example, a typical CMOS process with 3 μm minimal allowed gate length that is used to realize a MOSFET with L= 5.4 μm, may result in $\beta_{\rm FET}$= 1 mA/V^2, an ω_T= 779 Mrad/s (U_{dsQ}= 5V and I_{dsQ}= 10 μA), and a CLM factor λ= $66.7{\cdot}10^{-3}$ [1/V] [57].

JFETs are often used in discrete design. A large variety of JFETs are available. For example, $\beta_{\rm FET}$ may range from 0.4 mA/V^2 to 75 mA/^{2}, λ may range from $2.7{\cdot}10^{-3}$ to $15{\cdot}10^{-3}$ [1/V], and ω_T may range up to[8] 600 Mrad/s (e.g., [154][151]).

6.5 Overview of the proposed design method

In Chapter 5 and the previous sections of this chapter, rules for designing negative-feedback amplifiers with a specified SER were presented. The effects of the interconnect dimensions and the frequency dependency of the disturbance on the SER were not taken into account. Firstly, the frequency dependency of the disturbance and its effects on the negative-feedback amplifier are discussed. Secondly, a procedure is proposed that incorporates both interconnect and negative-feedback amplifier design.

6.5.1 Disturbance and envelope detection in a second-order amplifier

Second-order behavior of the transfer $A_t(f)$ (gain) often occurs in application specific amplifiers. Therefore, disturbance and envelope detection in a second-order amplifier is discussed in this subsection. For reasons of simplicity, an electrically-short interconnect is assumed. Hence, the disturbance as a function of frequency will increase at a slope of + 20 dB/dec. (see Chapter 2). The transfers of the disturbance and the envelope detection of a Butterworth compensated second-order amplifier are depicted in Fig. 6.6.

[8] Datasheets present I_{dss} and U_p from which $\beta_{\rm FET} = I_{dss}/U_p^2$ is calculated. It may (just like λ) also be taken from the numerous SPICE models provided by the semiconductor industry.

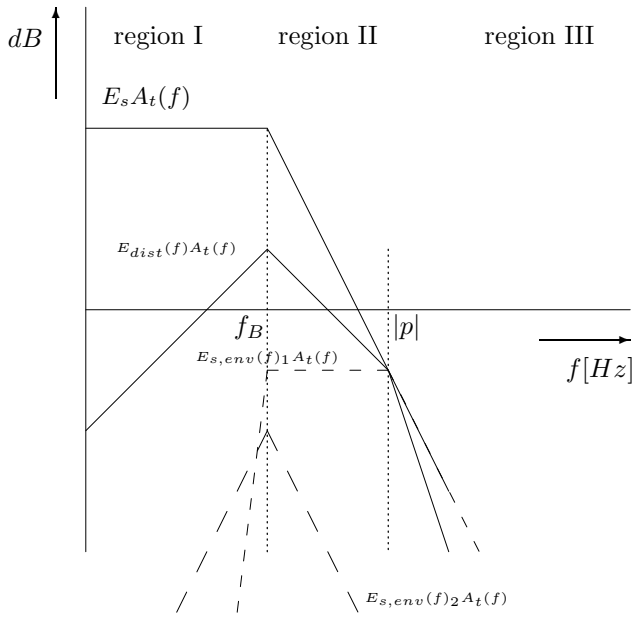


Figure 6.6: Transfers $20\log|E_sA_t(f)|$, $20\log|E_{dist}(f)A_t(f)|$, and $20\log|E_{s,env}(f)A_t(f)|$ of a second-order Butterworth compensated amplifier. It is assumed that the EM field couples to an electrically-short interconnect. Frequency f_B is upper frequency of the amplifier bandwidth and pole $|p|$ is a (parasitic) pole located at a frequency much higher than the bandwidth.

Transfer $E_{dist}(f)A_t(f)$ gives the output signal of the amplifier due to the disturbance. Transfers $E_{s,env}(f)_1A_t(f)$, and $E_{s,env}(f)_2A_t(f)$ are two possible outputs due to envelope detection of the disturbance. $E_{s,env}(f)_1A_t(f)$ may be found in amplifiers with a voltage output (An amplifier with the parameters given in Table 6.1, Row 2 shows this kind of response.). Section 7.2 presents an example of an amplifier design with envelope detection properties according to $E_{s,env}(f)_1A_t(f)$, as depicted in Fig. 6.6. $E_{s,env}(f)_2A_t(f)$ is a transfer that may be found in amplifiers with a current output (Table 6.1, Row 3). Figure 6.5 on page 203 depicts comparable envelope detection behavior of a dual-stage negative-feedback amplifier. Three regions of amplifier behavior can be distinguished, and will be discussed.

A. Amplifier behavior in region I

The linear transfer $E_sA_t(f)$ is constant up to the upper edge of the bandwidth represented by f_B. $E_{dist}(f)A_t(f)$ increases with 20 dB/dec and shows a maximum at f_B. $E_{s,env}(f)_1A_t(f)$ will increase with 80 dB/dec ($E_{dist}(f)^2\chi_1(f)^2 \sim 40+40$ dB) and $E_{s,env}(f)_2A_t(f)$ increases with 40 dB/dec up to the bandwidth

of the amplifier (since $\chi_1(f)$ is flat).

B. Amplifier behavior in region II

$E_s A_t(f)$ decreases at a rate of 40 dB/dec and $E_{dist}(f)A_t(f)$ decreases at a rate of 20 dB/dec. $E_{s,env}(f)_1 A_t(f)$ is flat because $E_{dist}(f)^2$ increases with 40 dB/dec, while $\chi_1(f)^2$ decreases with 40 dB/dec. The maximal detection can be calculated by determining the values of $E_{dist}(f)^2$ and $\chi_1(f)^2$ at f_B. Because f_B represents a corner frequency, the actual maximum of $E_{env}(f)_1 A_t(f)$ will be about 6 dB larger than the value calculated at frequency f_B.

The slope of $E_{dist}(f)^2$ is 40 dB/dec, resulting in a decrease of $E_{s,env}(f)_2 A_t(f)$ of 40 dB/dec, since for frequencies higher than the bandwidth the slope of $\chi_1(f)^2$ is -80 dB/dec. Maximal envelope detection occurs at frequency f_B.

C. Amplifier behavior in region III

In this region $E_s A_t(f)$ decreases at a rate of 60 dB/dec. $E_{dist}(f)A_t(f)$ decreases with 40 dB/dec. For frequencies higher than $|p|$, $E_{s,env}(f)_1 A_t(f)$ decreases with 40 dB/dec. and $E_{s,env}(f)_2 A_t(f)$ with 80 dB/dec. It is thus expected that errors due to envelope detection will rapidly decrease in magnitude in this region.

D. Discussion

A SER determined by both noise and envelope detection may be expected in regions II and III. Both interconnect and amplifier can be (re)designed in such a way that the SER requirements in either region II or III (in which it is minimal) are met.

Near the upper edge of the bandwidth (the transition from region I to region II) E_{dist} is maximal and therefore its degrading effect on the SER will be maximal too. Note that now E_{dist} is larger than $E_{s,env}$. Often, one tends to neglect this. This is understandable, since the band for which $E_{s,env}(f)$ is relatively large is usually (much) wider than bandwidth B, and therefore there is a greater probability that an interfering signal occurs across such a wide frequency band. This may be true in the specific case of plane wave interference that often occurs at frequencies higher than the moderate amplifier bandwidth. For these amplifiers it is best to design for a SER determined by noise and envelope detection.

Amplifier and interconnect combinations with a response depicted by $E_{s,env}(f)_1 A_t(f)$ should be designed for meeting the SER requirements by taking the noise behavior and the envelope detection behavior between f_B and $|p|$ ($\approx$ the envelope detection behavior at f_B) into account. For other responses, the amplifier and interconnect should designed in such a way that the SER is determined by noise and maximal envelope detection at frequency f_B. When the SER requirements are met at that frequency, they are automatically met in regions II and III.

E. Disturbance in case of an electrically-long interconnect

In case of an electrically-long interconnect, the first anti-resonance point may cause a large amplitude of E_{dist}. Except perhaps in case of extremely wide band amplifiers, the first resonance point will not occur in region I. This will be assumed in this work.

When the first anti-resonance point is at a frequency in region III or in region II in case of $E_{s,env}(f)_2A_t(f)$, the proposed method for designing for a specific SER at frequency f_B is probably still valid. However, when the first anti-resonance point occurs in region II in case of an envelope detection behavior given by $E_{s,env}(f)_1A_t(f)$, the amplifier should be designed for a specific SER at the frequency of that anti-resonance point.

The higher anti-resonance points will usually be lower in amplitude than the first one, due to the damping factor of the interconnect. At these frequencies also the effect of (parasitic) poles located at frequencies (much) higher than f_B will most probably be noticeable, further reducing the amplitude of the detected envelope.

6.5.2 Proposed design procedure

The design procedure proposed here is based on simplification, hierarchy and orthogonality. It can be split up in distinguishable steps. Each step can be further split up and orthogonalized. Each step starts at a simple level, then the complexity and accuracy of the models used will increase. The design procedure is demonstrated in Chapter 7.

The proposed design procedure is depicted in Fig. 6.7 and it is discussed using this figure. At the specification level, at least the source and load, the bandwidth, the EM environment, and the required signal-to-error ratio, SER_{req}, have to be specified. From the source and load specification the type of negative-feedback amplifier follows, i.e., the domain (i.e., voltage or current) of the input and output are determined. Then, a noise calculation has to be carried out so that the signal-to-noise ratio (SNR) can be determined. The SNR has to be larger than the SER_{req}. When this is not the case, it follows that the specified SER_{req} is not realistic since it is not theoretically possible. If possible, the SER_{req} should be reduced so that it is lower than the SNR again. Otherwise, the design process is stopped since it is impossible to meet the specifications.

Next, the allowed error level due to EM coupling is determined. In order to cope with uncertainties in parameter values like, e.g., EM field strength, an extra margin can be introduced. From the discussion given in Subsection 5.2.1 it follows that $DF = SNR - SER_{\text{req}} - NF_n - c$. The noise figure ($NF$) introduced in that subsection has been split-up into a part determined by the noise (NF_n) and a part determined by EMI, the disturbance factor (DF). Note that the equation for DF gives its maximal allowed value in dB. Ideally, DF equals NF_n as was argued Subsection 5.2.1. Constant c gives an extra margin of, e.g., 3 dB or 6 dB. With DF known, it is possible to determine the maximal dimensions of the interconnect, and calculate if shielding is necessary (see Chapter 2).

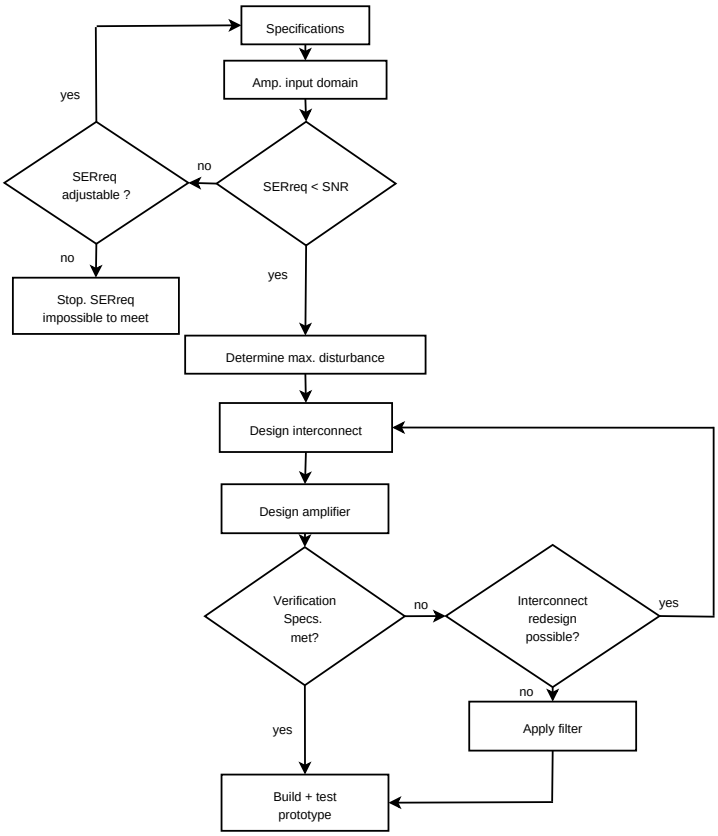


Figure 6.7: Flow diagram of the design of an amplifier with interconnect.

Using the specifications, the knowledge about the SNR, NF_n, and DF, the negative-feedback amplifier can now be designed. During the design process, the specifications are verified with calculations and simulations with more elaborate models[9]. It is possible that at this stage it turns out that the EMI specifications are difficult to meet. One can now choose to redesign the interconnect so that the EMI specifications are easier to meet, i.e., a design iteration occurs, or one may choose to apply a filter at the input of the amplifier. An overview of the

[9]The disturbance can, e.g., now be calculated using the small-signal model of the amplifier with the actual value of its input impedance. This causes differences in the value of E_{dist} with respect to the ideal case and should be checked. For moderate loop gains of 10–20, Z_{in} may however be expected to be that large/low that errors in the estimation of E_{dist} are below 10% as simulations show. These moderate loop gain values are usually easily obtained. Higher loop gains will show less deviation. In case of voltage processing amplifiers Z_{in} may at frequencies (much) higher than the bandwidth even become lower than Z_s. The effect of this on E_{dist} should be checked. An iteration between disturbance estimation and amplifier design may be necessary, i.e., orthogonality is lost.

design process of negative-feedback amplifiers is presented in Subsection 6.5.3.

Finally, when all specifications are met, a prototype can be built and tested.

6.5.3 Overview of negative-feedback amplifier design

The design method proposed in this work consists of 10 distinguishable steps. In this Subsection, we give a short overview of the method using Figure 6.8. Taking the specifications of the signal source and load, the required SER, the interconnect, and the EM environment as a starting point, Step 1 is to determine what kind of quantity the amplifier has to process, i.e., voltage or current.

Step 2 is to estimate $E_{dist}(\omega_c)$ using the methods presented in Chapter 2. The reason why this is done in Step 2 and not in Step 1, is that the quantity to be processed of the intended signal should be known. $E_{dist}(\omega_c)$ is then calculated for the same quantity as the intended signal.

In Step 3 the type of feedback is determined and designed. When the load permits both voltage and current drive, series feedback at the output should be favored over parallel feedback since this will result in lower EMI susceptibility. If voltage drive is mandatory, it may be hard to meet the SER_{req} in case of high $E_{dist}(\omega_c)$. In that case, effort has to be made to reduce $E_{dist}(\omega_c)$, e.g., by redesigning the interconnect or applying some filtering at the input.

Next, in Step 4, the input stage is designed for optimal noise performance. From the noise calculations follow the type of transistor, BJT or FET and its bias current. The noise performance determines SER_{max} which should, obviously, be larger than SER_{req}. It may be possible to implement the transimpedance and transadmittance amplifier or the voltage or current follower with a single stage. This can be checked at this stage of the design process. When both load driving requirements and the noise specifications can be met, it can be checked if the LP product of the single stage implementation (LP_1) is large enough to meet both bandwidth and EMI specifications. If this is the case, it is possible to design a single stage amplifier. Section 7.2 in Chapter 7 presents such a design.

Often, it is found that a dual-stage implementation of the nullor is required. The output stage is designed for the load requirements in Step 5. The bias current should be high enough to drive the load over the entire bandwidth for both the intended amplified signal $E_s A_t(\omega_0)$ and the disturbing signal $E_{dist}(\omega_0)A_t(\omega_0)$.

In Step 6 the bandwidth is determined. The equation $\omega_o = \sqrt[n]{LP_1\omega_{T2}}$ may be solved for ω_{T2}. A transistor can now be designed or selected that shows the required ω_{T2} at the required bias current.

The minimal value of the LP product that is required for meeting the SER_{req} is checked in Step 7. Since the amplifier can be expected to show maximal EMI susceptibility at the upper edge of the bandwidth, the minimal value of the LP product is determined at ω_0. The calculations are done under assumption of phantom zero frequency compensation. A_t is usually compensated for a Butterworth characteristic.

It may be found that the SER_{req} demand is already satisfied. Otherwise, the required LP product for meeting SER_{req} may be calculated. In case that an

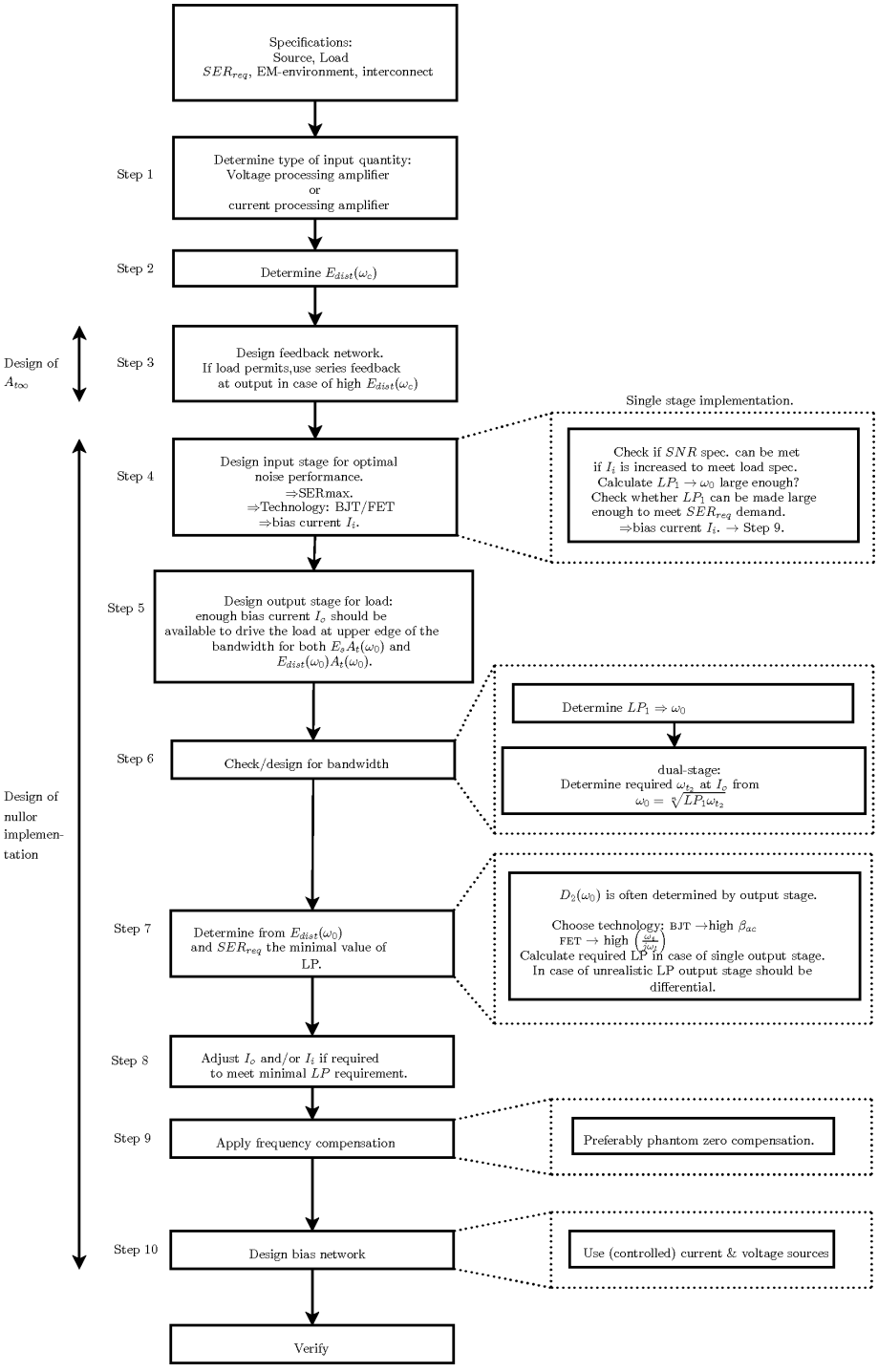


Figure 6.8: Overview of the proposed systematic design strategy for negative-feedback amplifiers with a specified SER.

unrealistically large value of the LP product is found, the output stage may be realized with a differential stage, since the output stage will often determine the second-order nonlinearity of the amplifier at ω_0.

The bias current of the output stage, and possibly also the input stage, may be increased in order to increase the LP product. This is done in design Step 8, that may be skipped if SER_{req} has already been met.

In Step 9, frequency compensation is applied. This is preferably done by means of phantom zero compensation. Butterworth[10] compensation ($\zeta = \frac{1}{2}\sqrt{2}$ in case of a second-order behavior) is beneficial for EMI behavior near the upper edge of the bandwidth. Frequency compensation is extensively dealt with in [3].

Finally, in Step 10 the bias network is designed. It should be designed in such a way that it does not negatively affect the LP product, nor may it cause BJT stages to become voltage driven instead of current driven. Designing the bias circuitry is not treated extensively in this work, but is treated in [3].

Extensive simulations (and measurements) have to be performed to check the final amplifier design. Of course, simulations are usually also done during the presented design steps.

When there is a large voltage swing across the collector of the output transistor, it may be found that EMI and distortion are larger than expected. This is caused by the 'cross term transconductance' (Chapter 3), g_x, which can be made ineffective by preventing the large voltage swing by cascoding the transistor.

6.6 Design example of a voltage amplifier

Consider a voltage source with source resistance $R_s = 500\ \Omega$ and signals in a band of 100 Hz−4 MHz. Signal voltage levels of up to maximally 88 mV peak occur up to about 500 kHz. Signal levels above this frequency are limited to maximally 3 mV.

Disturbing voltages with a maximal amplitude of 2 mV may be expected. EMI induced voltage $u_{s,\omega_l}(\omega_c)$ of the same order of magnitude as the noise voltage is allowed (Steps 1 and 2). The load is ideally voltage driven and a maximal peak voltage of 4 V is allowed. Its electrical equivalent consists of a resistance of 3 kΩ shunted by a capacitance of 330 pF.

The transfer is voltage to voltage and therefore series-parallel feedback is required (Step 3). An amplification factor of maximally 50 times follows from the input and output values.

The amplifier should be realized with discrete components and the npn transistor type BS847(BS) and the pnp transistor type BC857 are available (the BS847 are two matched BC847 transistors in one package, the BC857 is its pnp dual [126]).

The bias current of the input stage follows from noise considerations. With[11]

[10] or Bessel ($\zeta = \frac{1}{2}\sqrt{3}$ in case of a second-order behavior, for a maximally flat phase response in the pass band) compensation.

[11] Note that the noise performance can be improved by choosing $R_1//R_2$ to be smaller, e.g., a little smaller than R_s. This increases the load on the output transistor.

R_1= 38k3 and R_2= 866 Ω, A_t =45.23 and minimal voltage noise is obtained when the transistors (BS847(BS)) of the differential input stage are biased at a current of about 690 μA , giving I_T= 1380 μA. The total equivalent noise voltage is $\overline{u_{n,eq}}$= 10.5 μV (Step 4).

The bias current of the output stage should both satisfy the load driving conditions and the $u_{s,\omega_l}(\omega_0)$ constraint. The demand that results in the largest value of I_{cQo} should be used as the bias current of the output BJT (Step 5). From the output requirements it follows that the output stage should be biased at a collector current of 2 mA. To limit adverse effects of the output voltage ($\hat{u}_{bc}$) on the linearity of the output stage, a large U_{ceQ} of 5V has been chosen, resulting in $|U_{bcQ}| \approx 4.3V$. A single stage implementation of the output stage is used in this example. For convenience in the first design steps, the input stages have been given the same U_{ceQ}, which also reduces the offset.

A first order estimation of the poles follows from the hybrid-π parameters: U_{AF_i} = 82 V, ω_{t_i} = 697.4 Mrad/s, β_{ac_i} = 325 and ω_{t_o} = 923.6 Mrad/s, $\beta_{ac_o} = 304$.

The load causes a pole $p_l \approx -\frac{1}{R_l C_l}\frac{R_1+R_2+R_l}{R_1+R_2} = -1.09$ Mrad/s. The input stage introduces a pole at $p_i \approx -\frac{\omega_{t_i}}{\beta_{ac_i}}\frac{2r_\pi(R_1+R_2)}{R_s(R_1+R_2)+R_1R_2} \approx -38.9$Mrad/s, and the output stage a pole at $p_o \approx -\frac{\omega_{t_o}}{\beta_{ac_o}} = -3.0$ Mrad/s. The LP product is approximated by $LP \approx \frac{q}{4n_fkT} I_T \left(\frac{R_2}{R_1+R_2}\frac{\omega_{t_o}}{C_l}\right) = 8.25 \cdot 10^{14}$, resulting in $\omega_0 \approx 28.7$ Mrad/s ($\approx$ 4.6MHz) (Step 6). There is, however, a problem. Pole $|p_i|$ is only approximately 1.4 times larger than ω_0. It will therefore affect both bandwidth [2] and χ. As stated earlier, the effect of the non-dominant p_i can be approximated by considering its effect on damping factor ζ. Damping factor ζ will decrease, whether the amplifier is frequency compensated by a phantom zero or not.

When we assume the amplifier to be frequency compensated with a phantom zero (z) at -22.6 Mrad/s, ζ will equal $\frac{1}{2}\sqrt{2}$ when the effect of p_i is neglected. Due to p_i, however, it appears that $|z|$ is shifted to a higher frequency resulting in an effective damping of $\zeta' = 0.338$.

From Table 6.2, Equation (6.27), the considerations given in Section 6.2.4, and incorporating the frequency dependency of the output stage, for $u_{s,\omega_l}(\omega_0)$ is found

$$
\begin{aligned}
|u_{s,\omega_l}(\omega_0)| \approx & u_s^2 m \left(\frac{R_1+R_2+R_l}{R_2R_l}\right)^2 \frac{1}{4\zeta^2}\left[\frac{\omega_o}{p_o p_l}\sqrt{\omega_0^2+(p_o+p_l)^2}\right]^2 \times \\
& \left(\frac{1}{\frac{q}{n_fkT}\frac{I_T}{4}} + \frac{R_s+R_2//(R_1+R_l)}{\beta_{ac_i}}\right)\frac{n_fkT}{q}\frac{1}{2I_{cQo}^2}\times \\
& \left(\frac{I_T}{2U_{AF_i}} + \frac{q}{n_fkT}\frac{I_{cQo}}{\beta_{ac_o}}(1-x)\right)\frac{1}{1+\left(\frac{\omega_0}{p_o}\right)^2}.
\end{aligned}
\tag{6.43}
$$

Note that the LP product is incorporated in this equation (Step 7).

Using the value of ζ' instead of ζ in Equation (6.43), and the disturbing voltage of 2 mV, we find for $|u_{s,\omega_l}(\omega_0)|$ values between 0.12 μV and 6.83 μV,

under that assumption $\upsilon = 1$ and x has a value between 1.03 and 0.97. This within specifications since it $|u_{s,\omega_l}(\omega_0)|$ is of the same order of magnitude as $\overline{u_{n,eq}}$.

When $x = 1$, $|u_{s,\omega_l}(\omega_0)| \approx 3.47\mu$V is found. SPICE simulations[12] using NXP models of the BJTs [126] showed a value of $|u_{s,\omega_l}(\omega_0)| \approx 2.37\mu$V. The first order estimation is accurate enough. Of course, accuracy in the estimation of $|u_{s,\omega_l}(\omega_0)|$ can be improved by deriving more accurate equations for the necessary asymptotic gain model parameters from the small signal model of the amplifier. This can be done in the analysis part of the amplifier being designed.

Step 8 is skipped since the SER_{req} is already met. Frequency compensation is accomplished by adding a shunt capacitance of 1.155pF in parallel with feedback resistor R_1 (Step 9). Implementing the bias network (Step 10) is skipped in this example.

Figure 6.9 shows the circuit diagram of the voltage amplifier that was used in the simulations. The total SER is approximately 75.9 dB for signals up to 500

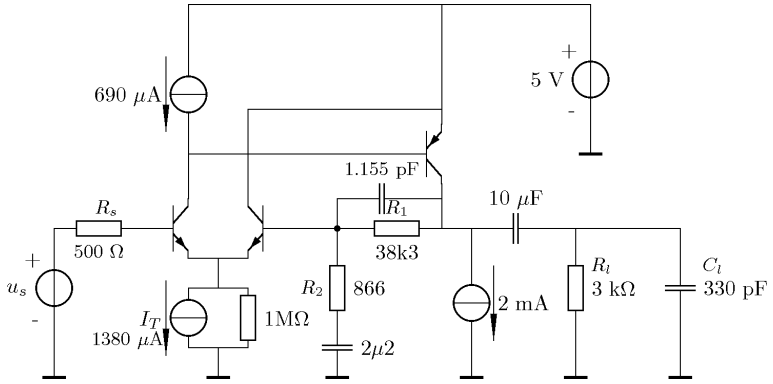


Figure 6.9: Voltage amplifier: μ= 45.23, B=100Hz−4.6MHz, $\overline{u_{n,eq}}$= 10.5 μV, $|u_{s,\omega_l}(\omega_0)| \approx 0.12\mu - 6.83\mu V$. In case x =1, $|u_{s,\omega_l}(\omega_0)| \approx 3.47\mu$V.

kHz and about 47.3 dB for frequencies higher than 500kHz. The SER at higher frequencies can be improved by applying overcompensation.

For illustration purposes $u_{s,\omega_l}(\omega_c)$ at frequencies ω_c much lower than $|p_o|$ is also approximated. $D_2(\omega_c) \approx D_2(0)$ and $u_{s,\omega_l}(\omega_c) \approx u_{s,\omega_l}(0)$ in this case. For $u_{s,\omega_l}(0)$ it is found

$$u_{s,\omega_l}(0) \approx u_s^2 m \left(\frac{n_f kT}{q}\right)^2 \left(\frac{R_1 + R_2 + R_l}{R_2 R_l}\right)^2 \frac{1}{2\frac{I_{cQi_1}}{2} I_{cQ_o}^2} \times \left[\frac{I_{cQi}}{U_{AFi}} + \frac{q}{n_f kT} \frac{I_{cQo}}{\beta_{ac_o}}(1-x)\right].$$

[12]Simulations must be made with care. The run time should be made large and the time step small. This leads to long simulation times and large data-files. Also, simulation data should be stored when the amplifier is in steady state.

Since in a single ended differential stage the transconductance is proportional to half the current, and the output resistance can be approximated by (worst case) the output resistance of one BJT, we have $I_{cQi1}/2$ in the term outside of the brackets and I_{cQi1} inside the brackets.

When the Early voltage goes to infinity, the equation for $u_{s,\omega_l}(0)$ reduces to

$$u_{s,\omega_l}(0) \approx u_s^2 m \left(\frac{n_f kT}{q}\right) \left(\frac{R_1 + R_2 + R_l}{R_2 R_l}\right)^2 \frac{1}{\beta_{ac_o}} \frac{1}{I_{cQi_1}} \frac{1}{I_{cQ_o}} (1 - x).$$

Performing reliable simulations of $u_{s,\omega_l}(0)$ is troublesome[13]. One has to use long simulation times and small maximal time steps in transient simulation to obtain the necessary resolution. Still, with u_s being 2 mV, the 'Fourier transformation noise floor' with peak values larger than 1 μV, was much larger than the expected $|u_{l,\omega_l}(0)|$ range[14] of -94.1 nV up to 94.1 nV in case we assume $U_{AF_i} \to \infty$. Therefore, the simulation has been performed with u_s being 20 mV, resulting in $u_{l,\omega_l}(0)$ having a value between -9.4 μV and 9.4 μV ($U_{AF_i} \to \infty$) and -4.5μV and 14.3μV ($U_{AF_i} = 82$ V) (when $x = 1$, $|u_{s,\omega_l}(0)| \approx 0.11\mu$V and $u_{l,\omega_l}(0) \approx 4.9\mu$V, respectively). Simulation gives $|u_{l,\omega_l}(0)| = 9.30$ μV, which is within the calculated range.

Further, it was necessary to cascode the output stage, a voltage-controlled current source with g_m equal to that of the output stage connected as current follower was used, to avoid an increase of $u_{l,\omega_l}(0)$ due to the effect of g_x. In the uncascoded case, $u_{l,\omega_l}(0)$ was about 108.3 μV.

6.7 Conclusions

This chapter presented a systematic design approach for application specific negative-feedback amplifiers. Noise, distortion, bandwidth and also EMI performance were discussed.

Noise and EMI determine the signal-to-error ratio (SER) of the amplifier. Noise determines the maximal SER, which should always be higher than the required SER. The difference $\text{SER}_{\max} - \text{SER}_{\text{req}}$ gives a measure for the error that may be generated by EMI. The latter can best be of the same order of magnitude as the noise.

Equations were presented that enable the designer to calculate noise, bandwidth, the required loop gain poles product, and the bias current of the transistors to meet both the SER_{req} and the bandwidth.

EMI has extensively been dealt with. It has been shown that negative-feedback amplifiers with series feedback at the output suffer much less from EMI than amplifiers with parallel feedback at the output. If possible, series feedback at the output should thus be favored over shunt feedback at the output.

It was found that in case of a dual-stage negative-feedback amplifier, the output stage should have a large current amplification factor, α_{20}, for low EMI

[13] With '0' being f_c= 10 kHz and f_l=1kHz.
[14] With $0.97 \leq x \leq 1.03$.

behavior. A large α_{20} is so beneficial, that a device with a high α_{20} should be favored over one with a lower α_{20}, even if the latter device is more linear than the first.

As a starting point, it is for convenience advised to apply differential stages in case of series feedback. Series feedback at the input thus results in a differential stage at the input and a differential stage as output stage follows in case of series feedback at the output.

Parallel feedback at either the input or output stage may result in a single stage implementation of that input or output stage. If calculations show that EMI behavior is too bad, the single stage implementation can be replaced by a differential stage implementation.

Frequency compensation should be applied to the amplifier in order to obtain a Butterworth (or Bessel) characteristic. Uncompensated amplifiers will show overshoot in the desired transfer and also in EMI susceptibility near the upper edge of the bandwidth.

Finally, since EMI is (among other terms) determined by the second-order nonlinearity of the amplifier, the measures taken to decrease EMI are also expected to be beneficial for low second harmonic distortion.

Chapter 7

Realizations

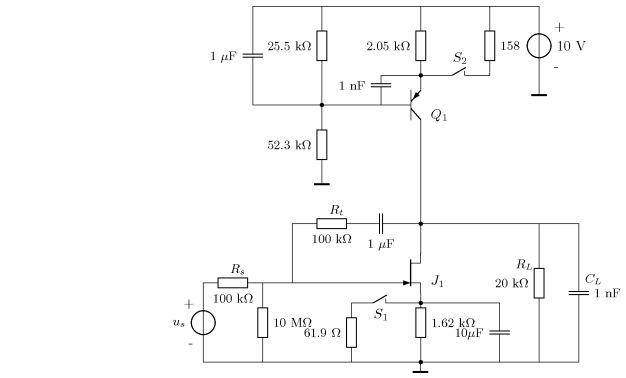
Modified hybrid-π models of active devices and a design method for negative-feedback amplifiers with specified signal-to-error ratio (SER) have been presented in the previous chapters. This chapter presents some designs of negative-feedback amplifiers using the models and the method developed in those chapters, to demonstrate and verify the design method. Therefore, application specific amplifiers with low EMI susceptibility are designed for relatively low interfering frequencies to ease EMI measurements.

Section 7.1 presents a single stage JFET transimpedance amplifier of which its only purpose is to demonstrate the dependence of EMI on loop gain and the pole locations. It is not designed for a specific SER. The systematic design of a negative-feedback cascode amplifier with specified SER is demonstrated in Section 7.2. Finally, in Section 7.3, the systematic design of a multiple stage transadmittance amplifier is presented. It is designed for a harsh electromagnetic environment. Disturbing input voltages with an amplitude of 1 V and a modulation depth of 1 result in an equivalent input voltage of only a few microvolts, which is of the same order of magnitude as the equivalent noise voltage.

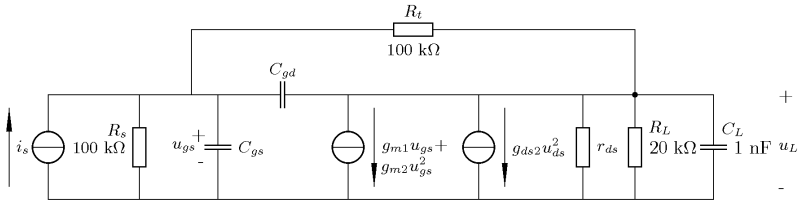
7.1 AM detection effects in a single-stage transimpedance amplifier

To verify the theory described in the previous chapters, a single-stage transimpedance amplifier (TIA) was designed and built[1]. It is used to demonstrate the effects of the pole and zero positions of $\xi(s)$ and the effect of the LP product on the AM detection effect, not as an example of an amplifier with very good AM detection properties. The amplifier was therefore designed to have a moderate LP product. As a result, the AM detection properties can be measured at relatively low frequencies, which is easier to do than at high frequencies because parasitic capacitances and inductances do not have to be accounted for.

[1] This section was published in [116]



(a) transimpedance amplifier



(b) small-signal model of the transimpedance amplifier

Figure 7.1: The designed transimpedance amplifier. Input current is generated by means of a voltage source and a 100kΩ resistor. Bias current I_{dQ} is 1 mA with switches open, 10 mA with switches closed.

A JFET (J309) is used as the active device in the amplifier. Figure 7.1(a) shows the circuit diagram. The amplifier can be biased at a drain current of 1 mA or 10 mA by a current source. With switches S_1 and S_2 open the drain current is 1 mA, with the switches closed it is 10 mA. The current source is built with a BJT decoupled for high frequencies by capacitors, so that the BJT does not disturb the demodulation action of the amplifier. The source signal is a current that is generated using a voltage source and a series resistor of 100kΩ. The small-signal model of the amplifier is shown in Figure 7.1(b). The output impedance of the current source is much larger than $r_{ds}//R_l$ and is therefore disregarded.

The small-signal parameters have been determined using SPICE. The actual JFET used agreed well with the typical values of the SPICE model. Both measurements and simulations show g_{m1} being equal to 4.4 mA/V and 13.9 mA/V in case of I_{dQ} being equal to 1 mA and 10 mA, respectively; g_{m2} is approximately 4.7 mA/V^2. The pinch-off voltage is about -2V. Simulated values of C_{gs}, C_{gd}, and r_{ds} are approximately 4 pF, 3 pF and 71.4 kΩ, respectively, in the case of $I_{dQ} = 1$ mA, and approximately 5 pF, 3 pF and 7.14 kΩ, respectively, in the

case of $I_{dQ} = 10$ mA.

The transfers β and ξ and their associated poles and zeros were calculated. They are given in Table 7.1. Pole p_l is due to load capacitance C_l and pole p_i is

Table 7.1: Overview of the poles and zeros of β and ξ in case $|p_l| < |p_i|$

	DC value[Ω]	p_l(rad/s)	p_i(rad/s)	z(rad/s)
β_{1mA}	$-7.25 \cdot 10^3$	$-68.89 \cdot 10^3$	$-2.92 \cdot 10^6$	$-3.45 \cdot 10^6$
ξ_{1mA}	$53.62 \cdot 10^3$	$-68.89 \cdot 10^3$	$-2.92 \cdot 10^6$	$-73.79 \cdot 10^3$
β_{10mA}	$-2.56 \cdot 10^3$	$-194.66 \cdot 10^3$	$-2.46 \cdot 10^6$	$-3.12 \cdot 10^6$
ξ_{10mA}	$51.28 \cdot 10^3$	$-194.66 \cdot 10^3$	$-2.46 \cdot 10^6$	$-199.42 \cdot 10^3$

due to C_{gs}. As was stated in Chapter 5, the zero in ξ is so close to p_l that they tend to cancel each other.

$A_{t\infty}$ is -100kΩ. With I_{dQ} equal to 1mA, the loop gain $A\beta_0$ equals -31.90, resulting in a transimpedance A_t of 99.7 dB[Ω] and a bandwidth of about 280 kHz. Increasing the drain current to 10 mA results in: $A\beta_0$ being -35.58, A_t being 99.8 dB[Ω] and a bandwidth of approximately 450 kHz[2]. In both cases there is a 40 dB/decade roll off, as can be seen in Figure 7.2(a). Measurements agreed with these figures.

For the demodulation action $\chi(s)^2$ is of importance. As could be expected from the fact that $|p_l|$ is located at a lower frequency than $|p_i|$, there will be a peak in the transfer. The maximum value of $\chi(s)^2$ occurs at a frequency of 409 kHz and 664 kHz for I_{dQ} being equal to 1 mA and 10 mA, respectively.

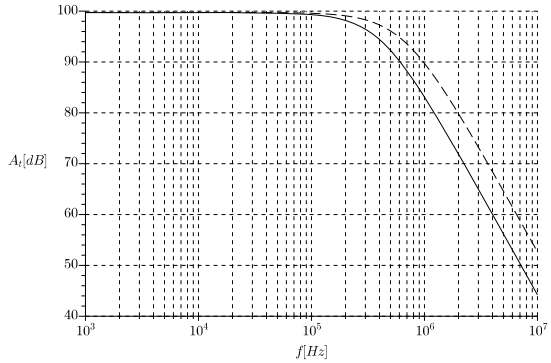
Increasing the drain current to 10 mA increases the $A\beta_0$ and the LP product. The resulting decrease in χ^2 reduces the AM detection effect by about 2.6 dB. The decreased ratio of g_{m2} and g_{m1} results in a further decrease of approximately 10.0 dB. The total decrease is approximately 12.6 dB.

When input pole $|p_i|$ is located at a lower frequency than $|p_l|$, the increase of $\chi(s)^2$ can be avoided or reduced and therefore the AM detection reduces. To force $|p_i|$ to a lower frequency, a 270 pF capacitor is placed in parallel with c_{gs}. Load capacitor C_l has to decrease to 22 pF now in order to keep the LP product constant. The values of both capacitors are calculated such that $|p_i|_{new} \approx |p_l|_{old}$ and $|p_l|_{new} \approx |p_i|_{old}$. The new transfers are summarized in Table 7.2. Note that the $A_t(s)$ remains the same as in the previous case (see Figure 7.2(a)).

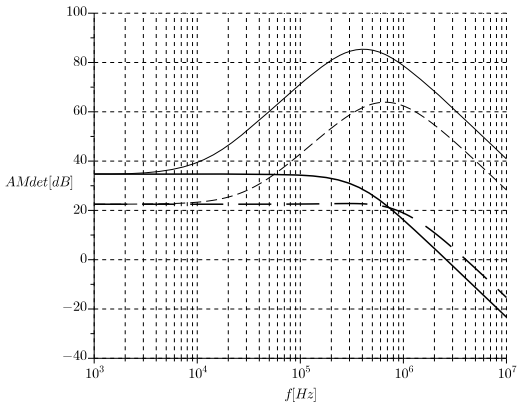
It must be noted that selecting or designing a JFET with a large C_{gs} will have the same effect. In fact, the latter is advised. A FET with a large width has both a large C_{gs} and a larger g_{m1}, and thus a larger contribution to the LP product.

We can identify four cases, being $|p_l| > |p_i|$ or $|p_l| < |p_i|$ with I_{dQ} being equal to 1 mA, and both pole combinations for I_{dQ} being equal to 10 mA. A Bode diagram can be used to compare the equivalent current source $\hat{i}_{s,f_l}(f_c)$

[2]The bandwidth is lower than predicted by $\omega_0 = \sqrt{(1 - A\beta_0)p_i p_l}$, ($\omega_0/(2\pi) \approx 409$ kHz and 666kHz, respectively.) due to the Miller effect. Note that the χ_{max} is still located at about $\omega_0/(2\pi)$, as is expected.



(a) Linear transfers $20\log|A_t(s)|$ for I_{dQ}= 1 mA (line) and I_{dQ}= 10 mA (dashed). Bandwidths are approximately 280 kHz and 450 kHz, respectively.



(b) Transfers of the AM detection behavior $20\log|\text{AM}_{det}(f_c)|$, in case $|p_l| < |p_i|$ for I_{dQ}= 1 mA (thin line) and I_{dQ}= 10 mA (thin dashed line) and in case $|p_l| > |p_i|$ for I_{dQ}= 1 mA (thick line) and I_{dQ}= 10 mA (thick dashed line).

Figure 7.2: Linear transfers and AM detection behavior of the transimpedance amplifier.

($f_c = \frac{\omega_c}{2\pi}$ and $f_l = \frac{\omega_l}{2\pi}$) in these four cases more easily, and to be able to quickly estimate the magnitude of the equivalent signal source for a given input signal and modulation depth. It is made using Equation (5.24). The product of $\hat{i}_s^2$, m and $AM_{det}(f_c)$ results in $\hat{i}_{s,f_l}(f_c)$.

In Figure 7.2(b), the transfers of the demodulation characteristic $20\log|AM_{det}(f_c)|$ are given for the four cases. It is assumed that the carrier

Table 7.2: Overview of the poles and zeros of β and ξ in case $|p_l| > |p_i|$

	DC value[Ω]	p_l(rad/s)	p_i(rad/s)	z(rad/s)
β_{1mA}	$-7.25 \cdot 10^3$	$-2.97 \cdot 10^6$	$-67.44 \cdot 10^3$	$-3.45 \cdot 10^6$
ξ_{1mA}	$53.62 \cdot 10^3$	$-2.97 \cdot 10^6$	$-67.44 \cdot 10^3$	$-2.97 \cdot 10^6$
β_{10mA}	$-2.56 \cdot 10^3$	$-2.74 \cdot 10^6$	$-194.94 \cdot 10^3$	$-3.12 \cdot 10^6$
ξ_{10mA}	$51.28 \cdot 10^3$	$-2.74 \cdot 10^6$	$-194.94 \cdot 10^3$	$-2.74 \cdot 10^6$

wave is modulated with a f_l =1 kHz. The thin line and the thin dashed line show $AM_{det}(f_c)$ in case $|p_l| < |p_i|$ for I_{dQ} being equal to 1 mA and 10 mA, respectively. The thick line and the thick dashed line show $AM_{det}(f_c)$ in case $|p_l| > |p_i|$ while I_{dQ} equals 1 mA and 10 mA, respectively.

The complete measurement set-up is shown in Figure 7.3. The function

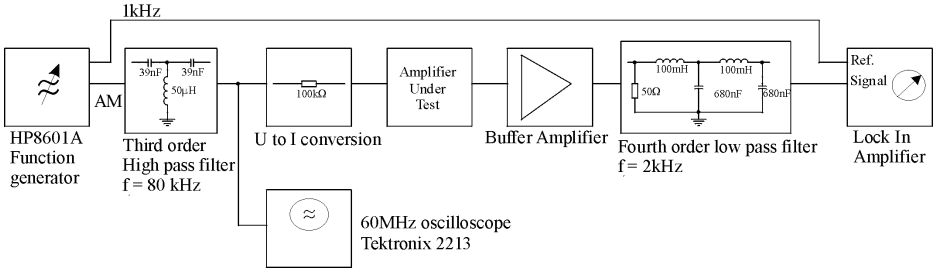


Figure 7.3: Measurement set-up. To get maximal performance, all filters, the buffer amplifier (bandwidth= 50 MHz) and the lock-in amplifier were specifically designed for the set up.

generator produces the AM signal. Spurious 1 kHz signals from the modulation are filtered out by means of a passive filter. The output of the amplifier under test is buffered by a linear amplifier with a 50 MHz bandwidth that was specifically designed for this purpose. The output from the latter amplifier is passively low-pass filtered and then measured by a lock-in amplifier which was also designed for this set-up.

The demodulation characteristics of the amplifier were measured with an input signal of 10 μA that was modulated by an 1 kHz sinusoid with a modulation depth, m, of 30 % (presented in Figure 7.4). Current $\hat{i}_{s,f_l}(f_c)$ is the magnitude of the equivalent current source as a function of the frequency. The thin solid line is the calculated value for I_{dQ} of 1 mA; the thin dashed line represents the calculated value in the case where I_{dQ} is 10 mA. The poles $|p_l| < |p_i|$. The thick solid and thick dashed lines represent the calculated value of $\hat{i}_{s,f_l}(f_c)$ for the cases I_{dQ} is 1 mA and I_{dQ} is 10 mA respectively, when $|p_l| > |p_i|$. The crosses and pluses in this figure are the measured values, which are in good agreement

with the theoretical calculation[3].

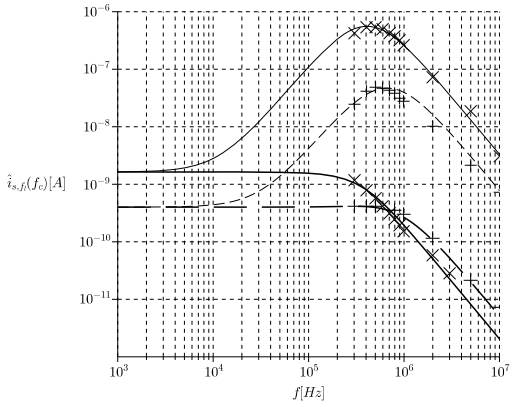


Figure 7.4: Amplitude of the equivalent current source $\hat{i}_{s,f_l}(f_c)$ at the input of the amplifier, $\hat{i}_s = 10\mu A$ and $m = 30\%$. Thin solid line: I_{dQ} equals 1 mA; thin dashed line I_{dQ} equals 10 mA in case $|p_l| < |p_i|$. Thick solid line: I_{dQ} equals 1 mA; thick dashed line I_{dQ} equals 10 mA in case $|p_l| > |p_i|$. The crosses and pluses are the measured values.

The measured value of $\hat{i}_{s,f_l}(f_c)$ was determined by measuring the demodulated component in the output voltage and dividing it by A_t at 1 kHz.

As Figure 7.4 clearly shows, the AM detection of an amplifier can be decreased at the cost of larger power consumption; for I_{dQ} equal to 10 mA the curves are well below the ones for I_{dQ} equal to 1 mA. A decrease in the AM detection peak is also seen when comparing the thin solid lines ($I_{dQ} = 1$ mA) and the thin dashed lines ($I_{dQ} = 10$ mA).

The measurements were performed at relatively low frequencies where parasitic capacitances and inductances could not affect the result. Therefore, a discrepancy between the calculated and measured demodulation component can occur at higher frequencies than were used here. The exact frequency where this discrepancy might occur depends on the circuit lay-out. Incorporating these parasitic impedances in the calculation reduces the possible discrepancies.

[3]In general, it is better to cascode a FET to reduce the detrimental effect of g_{ds2}, as was discussed in Chapter 3. Both measurements and evaluation of the effects of g_{ds2}, using a comparable method as discussed in appendix B, show that its effect may indeed be neglected for this amplifier at the presented frequencies of interest.

7.2 Design of a transimpedance amplifier with specified SER

The method to design a transimpedance amplifier with a specified SER in high field strengths is demonstrated by designing such an amplifier for a given signal source and load[4]. Table 7.3 summarizes the specifications of the source, load, signal transfer, and EM environment. All specifications chosen are realistic and may occur in practice.

Table 7.3: Specifications of the transimpedance amplifier example.

Source	Max. signal	10 μA
	Signal bandwidth	10 Hz $\cdots$ 1 MHz
	Impedance	100 kΩ // 1 pF
Load	Max. signal	1 V
	Impedance	10 kΩ // 100 pF
Transfer	Response type	Butterworth (Maximally flat pass band)
	Signal-error-ratio	$\geq$ 70 dB
EM-environment	field type	plane wave (far field)
	frequency band	1MHz$-$100MHz
	amplitude	30 V/m
	modulation depth	1

The envelope of the plane waves[5] shows low-frequency variations that are in the amplifiers' pass band. The maximum variation in the envelope corresponds to an amplitude modulation with a modulation index of 1, as stated in Table 7.3. Such an EM environment may very well occur in practice. Industrial, scientific and medical equipment (ISM), e.g., used for heating, diathermy, electrosurgery, or radio transmitters may radiate EM fields with high field strengths and low-frequency envelope variations. In some ISM bands (13.5 MHz, 27.0 MHz and 40.7 MHz) the amount of power that may be radiated is unrestricted in some countries [38]. EM field strength levels between 10 V/m and 30 V/m can therefore readily occur in the vicinity of radiating equipment. Equipment in an industrial environment and life supporting medical systems should be immune to EM fields up to at least 10 V/m [38][23].

The consequences of high susceptibility in a harsh EM environment (i.e., a too low SER) of the negative-feedback amplifier (as part of a larger system) may vary from life threatening situations in medical environments [21][22] and in aviation, to inconvenience when telephones receive AM radio broadcasts [10]. Maintaining

[4]The main part of this section has been published in [155].

[5]The electric and magnetic fields of the EM wave are perpendicular to each other and perpendicular to the directions of propagation (see Section 2.6).

sufficient SER in high EM field strength levels is thus important, especially in possible life threatening situations. Here, a minimal SER of 70 dB is expected to prevent these detrimental effects.

The relatively low frequency of 100 MHz, has been specifically chosen as the upper design limit. This relieves the measurement difficulties that can be expected at higher frequencies where board lay-out properties play a significant role. The method presented in this work is, nonetheless, also applicable to frequencies in the GHz range as used by cellular phones.

We will assume that both the negative-feedback amplifier and the load are shielded from interfering fields, but the interconnect between source and amplifier will not be shielded. To ease the calculation of EM coupling, the interconnect is assumed to consist of two wires that have a fixed distance to each other (comparable with two wires of a ribbon cable), and that EM-interaction with the shield does not occur. We will assume a called two-wire line [42] with a length of 0.1 m, a distance between the wires of 1.27 mm, an inductance of 92.7 nH, and a measured capacitance of 2.36 pF.

The intended signal is smallest at the input of the amplifier, where noise and EMI have the largest detrimental effect. Both noise and EMI effects are therefore transferred to an equivalent source at the input of the amplifier.

If it is assumed that the equivalent noise power and equivalent EMI power are uncorrelated, the SER is simply the ratio of the signal power and the sum of both EMI and noise power.

7.2.1 Determining the disturbing current

Under the specified conditions, the disturbing current at the input of the transimpedance amplifier can now be approximated by $i_{dist,tot} = j\omega C_d dE \sin\theta$ (see Chapter 2 or [42]), where ω is the angular frequency, C_d is the capacitance of the two-wire, d the distance between the conductors, E is the electric field strength, θ is the angle between the E-field and the two-wire, and $j = \sqrt{-1}$. When the orientation of the E-field is perpendicular to the two-wire ($\theta = 90°$), $i_{dist,tot}$ is maximal. Note that for frequencies higher than 100 MHz, the contributions of the magnetic field component and inductance L_d have to be taken into account as well.

In EMC engineering it is customary to assume the worst case scenario, i.e., maximal field coupling. This also makes sense from a design point of view, so in this section maximal $i_{dist,tot}$ is assumed ($\theta = 90°$).

To demonstrate the validity of the lumped circuit model for the specified maximum frequency of the interfering plane waves, Figure 7.5 shows the graph of $i_{dist,tot}$ determined by both the lumped circuit model and by the transmission line method (see Subsections 2.6.1 and 2.6.2 or [42][68]). Both graphs are in good agreement up to the frequency (≈240 MHz) where the two-wire is not electrically short anymore.

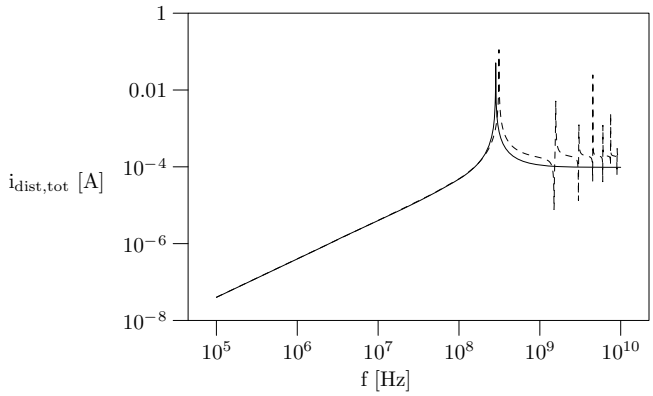


Figure 7.5: Total disturbing current at the input of the transimpedance amplifier as a function of frequency calculated with a lumped circuit model (solid line) and as predicted by transmission line theory (dashed line). At a frequency of about 240 MHz, the lumped circuit model becomes less accurate because the two-wire is not electrically short anymore. Resonance and anti-resonance points can be identified in the transmission line model based $i_{dist,tot}$ calculation that do not occur in the simple model. The lumped circuit model completely loses validity at approximately 1 GHz.

7.2.2 Design approach

From the source and load specifications (as summarized in Table 7.3) it follows that a transimpedance of 100 kΩ realizes 1 V across the load for a source current of 10 μA. This transimpedance can, e.g., be implemented by a negative-feedback amplifier with a feedback resistor of 100 kΩ.

Since noise will always be generated (i.e., also when there is no interference), it will determine the maximal obtainable SER and is therefore considered before EMI. The maximal allowable EMI now follows from the required SER and the noise behavior. Noise and EMI are extensively dealt with in the next subsections.

For elaborate treatment of the other design steps, we refer to Chapter 5 and [3]. They are only briefly discussed here.

7.2.3 Noise

For the transimpedance amplifier with a bipolar input stage, the equivalent input noise power is given by:

$$\overline{i_{n,eq}^2} = 4kTf_h\left\{\frac{1}{R_s}+\frac{1}{R_t}+\left(r_B+\frac{1}{2g_{m1}}\right)\left[\left(\frac{1}{R_s}+\frac{1}{R_t}\right)^2+\frac{1}{3}\left(2\pi f_h C_x\right)^2\right]+ \frac{g_{m1}}{2\beta_{dc}}\left[\left(1+r_B\left(\frac{1}{R_s}+\frac{1}{R_t}\right)\right)^2+\frac{1}{3}\left(r_B 2\pi f_h C_x\right)^2\right]\right\}, \tag{7.1}$$

under the assumption that the signal source generates noise equivalent to the thermal noise of the real part of its admittance. In this equation, f_h is the upper cutoff frequency. Because of the large bandwidth required (1 MHz), the influence of the lower-frequency corner of the bandwidth and the influence of flicker-noise can be neglected. For modern BJTs the frequency at which the flicker-noise equals the white noise is usually a few Hz [3]. Furthermore, R_s is the source resistance, C_x is formed by the source capacitance, C_s, and the capacitance of the two-wire line (C_d) in parallel. R_t is the feedback resistor, r_B is the base resistance, and β_{dc} is the dc current gain of the transistor.

For low noise power, it immediately follows from (7.1) that the BJT should have a high value of β_{dc} and, preferably, a low value of r_B. Also, (7.1) is valid under the assumption that the current noise contribution of the BJT is dominated by the base current. This is allowed when $\beta_{ac} \gg 1$ and $f_h \ll f_t/\sqrt{\beta_{ac}}$ [3], f_t being the transit frequency; conditions that usually can be met easily.

7.2.4 Calculation of the required transconductance

When we design for equal contributions of both noise power and EMI power to the SER, the most optimal design regarding the SER results. After all, when a lot of design effort is put in low noise design while EMI dominates the SER, this effort is wasted. Similarly, design effort and power is wasted when EMI is designed to be much lower than the noise. Therefore, EMI should have at most the same order of magnitude as the noise. For this EMI power, the minimal required transconductance of the active part is determined.

The disturbing current generated by the non-constant envelope of the interfering electromagnetic field shows the same amplitude variations as the electromagnetic field. Like noise, the resulting envelope detection (EMI) caused by the disturbing current can be represented by one equivalent current source at the input of the negative-feedback amplifier, given by (see Chapter 5):

$$i_{s,env}(\omega_c) = i_{dist,tot}(\omega_c)^2 \chi(\omega_c)^2 m D_2 \frac{1}{\xi_{\omega_l}}. \tag{7.2}$$

The angular frequency of the disturbing current is ω_c. χ is the transfer from the disturbing current to the input of the BJT, i.e., the transfer from $i_{disturb,tot}$ to u_{be}. ξ_{ω_l} is the low-frequency term of the transfer from signal source i_s to u_{be} and m is the modulation depth. For a transimpedance amplifier, ξ_{ω_l} also determines the transfer from source ${g_{\pi 2}u_{be}}^2$ to u_{be}, when $r_B \ll R_s//(R_t + R_L)$. D_2 is the second-order nonlinearity term, which is a measure for the second-order nonlinear behavior of the negative-feedback amplifier. Here, $D_2 = g_{m2}/g_{m1} - g_{\pi 2}\xi_{\omega_l}$.

To prevent the Miller effect, a BJT-BJT cascode stage is chosen for the amplifier implementation. Figure 7.6 depicts the following hybrid-π diagram of the transimpedance amplifier. Although the exact values of the circuit elements of the cascode are not yet known, some conclusions can be drawn using Table 7.3: load capacitance C_L will most probably be much larger than $C_{\mu CB}$, C_π, $C_{\mu 1}$

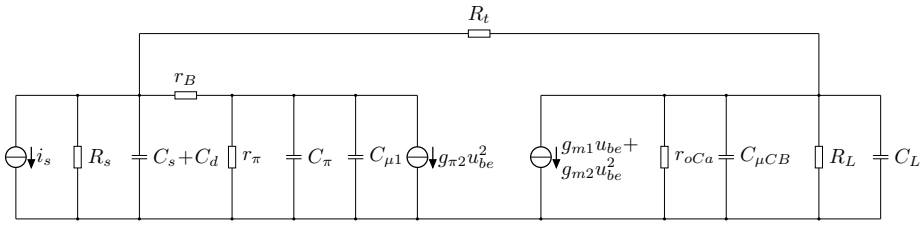


Figure 7.6: Hybrid-π signal diagram of the transimpedance amplifier.

and $C_s + C_d$; there will be two poles determining the bandwidth, with pole p_L affected by C_L and R_L located at a lower frequency than pole p_i affected by the input capacitance formed by C_π, $C_{\mu 1}$, $C_s + C_d$, and R_s shunted by R_t and r_π. Expressions for the poles will be given later.

Transfer $\xi(\omega_c)$ will have a zero located at approximately the same frequency as p_L and therefore shows a single pole transfer. The loop gain often shows two dominant poles in application-specific amplifiers. $\chi(\omega_c)$ is given by the ratio of $\xi(\omega_c)$ and the loop gain. When $\omega_c > |p_L|$, $\chi(\omega_c)$ will increase with increasing frequency up to some maximum value at ω_{max} after which it will decrease again. As a result $i_{s,env}$ will show the same behavior.

Fig. 7.7 shows the transfer $\chi(\omega_c)$, current $i_{dist,tot}(\omega_c)$ and the resulting equivalent envelope detection source $i_{s,env}(\omega_c)$ in one figure. It shows how the slopes of $i_{s,env}(\omega_c)$ depend on $i_{dist,tot}(\omega_c)$ and the slopes of $\chi(\omega_c)$. Between

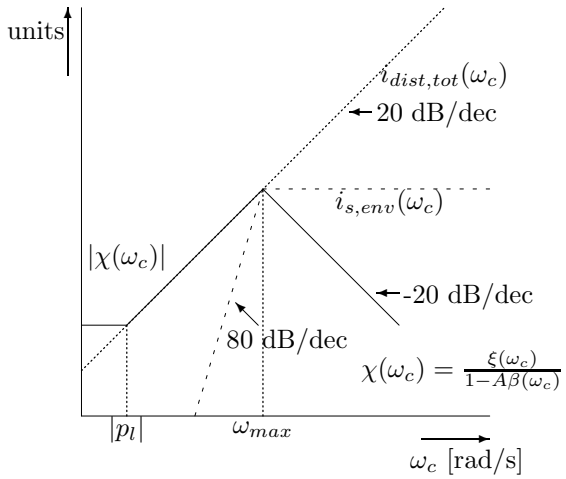


Figure 7.7: The transfers $|\chi|$ (solid line), $|i_{dist,tot}|$ (dotted line), and $|i_{s,env}|$ (dashed line) as a function of frequency. The maximum frequency used in this figure is in the 'differentiating' region of $i_{dist,tot}$. Note that the flat region of $|i_{s,env}|$ is due to out-of-band disturbance and thus the region of interest.

$|p_L|$ and ω_{max}, $i_{s,env}$ increases with a slope of 80 dB/dec and it stabilizes at a constant value for frequencies higher than ω_{max}. Furthermore, ω_{max} will occur near the upper corner frequency of the bandwidth ω_0. Note that the flat region of $|i_{s,env}|$ is due to out-of-band disturbance, and is thus the region of interest.

The maximum value of χ_{max} occurs at a frequency, ω_{max}, approximately equal to the upper limit of the bandwidth, $\omega_0 = \sqrt{(1 - A\beta_0)p_i p_L}$, and can be determined from (see Chapter 5)

$$\chi_{max} \approx \frac{\chi_0}{2\zeta}\sqrt{\frac{\omega_0^2 + p_L^2}{p_L^2}}. \tag{7.3}$$

χ_0 and $A\beta_0$ are still unknown. To develop an equation that can be solved, Figure 7.6 has to be considered.

Output resistance $r_{o,CA}$ can be expected to have a value much greater than R_L and can therefore be neglected. For now, it is assumed that r_B can be neglected because it is much smaller than r_π. When this is not the case, its effect can be evaluated in a later design phase. Feedback factor β_0 is determined from Fig. 7.6 and $A = g_{m1}$. With $r_\pi = \frac{\beta_{ac}}{g_{m1}}$ it follows for the loop gain

$$A\beta_0 = -\beta_{ac}\frac{R_s R_L}{r_\pi R_s + (r_\pi + R_s)(R_L + R_t)}. \tag{7.4}$$

Also, from Figure 7.6 for ξ_0 it follows directly that:

$$\xi_0 = \frac{r_\pi R_s (R_t + R_L)}{R_s(r_\pi + R_t + R_L) + r_\pi(R_t + R_L)}. \tag{7.5}$$

The 'DC' transfer χ_0 is approximately $\xi_0/(-A\beta_0)$ when $-A\beta_0$ is much larger than one. It is now possible to simplify this expression to a form where, apart from g_{m1}, no hybrid-π parameters appear

$$\chi_0 \approx \frac{R_t + R_L}{R_L}\frac{1}{g_{m1}}. \tag{7.6}$$

Envelope variations usually occur at a low frequency. As an approximation, ξ_{ω_l} is approximately equal to ξ_0 can be used in Equation (7.2). For D_2 it is found that

$$D_2 = \frac{q}{2n_f kT}\frac{1}{1 + \frac{R_v}{r_\pi}} = \frac{q}{2n_f kT}\frac{\beta_{ac}}{\beta_{ac} + g_{m1}R_v}, \tag{7.7}$$

in which $R_v = R_s//(R_t + R_L)$.

Substituting Equations (7.6), (7.7), and (7.3) (ζ equals $-(p_L + p_i)/(2\omega_0)$), into (7.2) and solving for g_{m1} results in:

$$\begin{aligned} g_{m1} &= \frac{-\beta_{ac}}{2R_v} + \frac{1}{2i_{s,env}R_v}\sqrt{i_{s,env}\beta_{ac}\left(i_{s,env}\beta_{ac} + 4E\right)} \\ &\text{and} \\ E &= i_{dist,tot}^2 R_v m \frac{R_t + R_L}{R_L}\left(\frac{p_i}{p_L}\right)\frac{\omega_0^2 + p_L^2}{(p_L + p_i)^2}\frac{q}{2n_f kT}. \end{aligned} \tag{7.8}$$

The required transconductance can be calculated from this equation if one uses the desired bandwidth as the value for ω_0 and a first-order approximation for p_L and p_i. This first-order approximation for p_L follows from Fig. 7.6 by neglecting the influence of r_π, which is allowed because the shunt $r_\pi // R_s$ is in series with the large-valued resistor R_t. Pole p_L is thus approximately equal to $-1/(R_L C_L)\frac{(R_L+R_t)}{R_t}$. Under the condition that R_s and R_t are much larger than r_π, and C_π is larger than C_x, p_i can be approximated by $-\omega_t/\beta_{ac}$. Pole p_i thus follows from the transistor properties. As a first-order approximation of β_{ac}, the maximal forward current gain β_f (as specified in SPICE models), can be used.

7.2.5 Implementation of the BJT transimpedance amplifier

To quickly realize a prototype transimpedance amplifier, it was designed and built using discrete BJTs. From the large number of BJTs that satisfy the design constraints, the BC548B npn transistor, was chosen.

A. Noise calculation

From the noise equation derived earlier, viz. Equation (7.1), the optimal bias current for the transistor is determined to be approximately 10 μA for the BC548B. The noise contribution of the BJT is negligible compared to the noise contributions of R_s and R_t. The resulting equivalent noise power is $\overline{i^2_{n,eq}} = 354 \cdot 10^{-21}\mathrm{A}^2$. The resulting SNR is 84.5 dB, which is the largest obtainable SER.

B. Output capability

In order to deliver a signal of 1 V peak to the load, a current of 637 μA is required. When this current has to be delivered to the load, one has to make sure that enough current keeps flowing through the output stage to avoid an unacceptable decrease in transit frequency f_t. Biasing the output stage at approximately 1.5 times the current to be delivered is a good strategy [3], resulting in a minimal bias current of 1 mA.

C. EMI

To compensate for component spread and uncertainties in the exact value of $i_{dist,tot}$, the design SER of 73 dB is assumed, so there is a margin of 3 dB. With 73 dB SER, the total equivalent input error power ($i^2_{n,eq}$ plus $i^2_{s,env}$) equals $5 \cdot 10^{-18}\ A^2$. If it is assumed that both components equally contribute to the 'error power', a value for $i_{s,env}$ of 1.58 nA is obtained.

Since $i_{dist,tot}$ equals $j\omega C_d dE$, it follows that the allowed maximal value of $i_{dist,tot}$ at ω_0 is 567 nA. However, a bandwidth of 1.1 MHz is designed for to be on the safe side again. Using Equation (7.8) with the corresponding $i_{dist,tot}$ of 621 nA, it is now found that g_{m1} should have a value of 48.5 mA/V to satisfy the EMI demands, which corresponds to an I_{cQ} of 1.3 mA (the Early effect has been disregarded). This value of I_{cQ} is located in the mid-current region. A β_f of 294 and an ω_t of 628 Mrad/s follow for the BC548B.

D. Discussion

The I_{cQ} determined from the above EMI considerations is only a little higher than required for the output capability. Hence, in order to meet the required EMI specifications, the power consumption does not increase excessively. There is, however, a large discrepancy between the values of I_{cQ} for minimal noise performance and that required for EMI performance.

Biasing the cascode at a current of 1.3 mA instead of 10 μA changes the noise behavior of the BJT. The contribution of the BJT to the equivalent noise power increases and will now be of the same order of magnitude as the noise from R_s and R_t, which is still acceptable. The equivalent noise current power $\overline{i_{n,eq}^2}$ equals $1.94 \cdot 10^{-18}$ A^2, resulting in a SER of 73.5 dB.

E. SER analysis and amplifier implementation

Biasing the BJT cascode at a collector current I_{cQ} of 1.3 mA and a collector-emitter voltage of 2 V results in the values of the modified hybrid-π parameters tabulated in Table 7.4. They were determined using SPICE to determine the linear values and Equations (3.7) and (3.9) to determine the second-order values of the modified hybrid-π model. The simulated value of g_{m1} is slightly larger than the value obtained with Equation (3.6). This is because SPICE has taken the Early effect into account.

Table 7.4: Hybrid-π parameters, I_{cQ}= 1.3 mA, U_{ceQ}= 2 V

r_B = 26.5 Ω	β_{ac}= 286
r_π =5.79 kΩ	r_o=48k4 Ω
$g_{\pi 2}$ =3.30 mA/V^2	C_π =70.2 pF
g_{m1} =49.3 mA/V	C_μ =2.4 pF
g_{m2} =945 mA/V^2	f_t =108 MHz

The loop gain is equal to -23.4, which results in an accuracy of the transimpedance of 99.6 dB[Ω]; just 0.4 dB[Ω] less than in the ideal case. Poles p_L and p_i can be found at $-1.06 \cdot 10^6$ rad/s and $-2.54 \cdot 10^6$ rad/s, respectively. The bandwidth ω_0, as predicted by the LP product, is $8.13 \cdot 10^6$ rad/s (1.29 MHz) and ζ equals 0.22. Note that the bandwidth specifications cannot be met with a non-cascode single stage. Due to the Miller effect, the bandwidth in this case is limited to approximately 460 kHz.

χ_{max} reaches a high value at approximately ω_0 due to the low value of ζ. The minimal SER to be expected near ω_0 amounts to 70 dB, which is just within specifications. After frequency compensation to obtain a Butterworth characteristic, however, no overshoot will occur and therefore χ_{max} will decrease, resulting in a larger SER.

For a Butterworth characteristic a phantom zero [3] was introduced by shunting R_t with a capacitance C_{ph} of 1.18 pF. Now, ζ equals 0.69 and ω_{max} equals $8.07 \cdot 10^6$ rad/s, which is indeed very close to ω_0 ($8.13 \cdot 10^6$ rad/s).

χ_{max} is determined to be 1,211 Ω. This results in a corresponding value of $i_{s,env}$ equal to 224 pA at ω_0. For frequencies just above ω_0, the slope of $\chi(\omega_c)$ (see Fig. 7.7) has not reached -20 dB/dec yet. This slope is reached after approximately an octave. In the frequency band $[\omega_0$–$2\omega_0]$, $\chi(\omega_c)$ decreases by about 3 dB and $i_{dist,tot}$ increases by 6 dB, resulting in an increase of 6 dB in $i_{s,env}$. As a result, $i_{s,env}$ is approximately 450 pA for frequencies larger than $2\omega_0$. The SER to be expected thus equals 76.1 dB.

The required SER is easily reached after frequency compensation. The designer could consider reducing I_{cQ} in order to reduce power consumption. As a consequence, $i_{s,env}$ will increase and $i_{n,eq}$ will decrease, but the required SER can still be reached. A trade-off between power consumption and SER is thus possible. We will not elaborate on this here.

Figure 7.8(a) shows the final schematic of the transimpedance amplifier. A current source realized with a pnp BJT (BC556A) biases the cascode at a collector current of 1.3 mA. The resistors required for establishing the desired base-emitter and collector-emitter voltages are chosen such that LP product of the transimpedance is virtually not reduced. SPICE simulations show a transimpedance of 99.6 dB[Ω], a bandwidth of 1.29 MHz ($8.11{\cdot}10^6$ rad/s) and an $\overline{i_{n,eq}}$ of 1.55 nA. These figures are very close to the calculated values (no deviation in transimpedance, 0.5 % deviation in bandwidth and 10 % deviation in $\overline{i_{n,eq}}$).

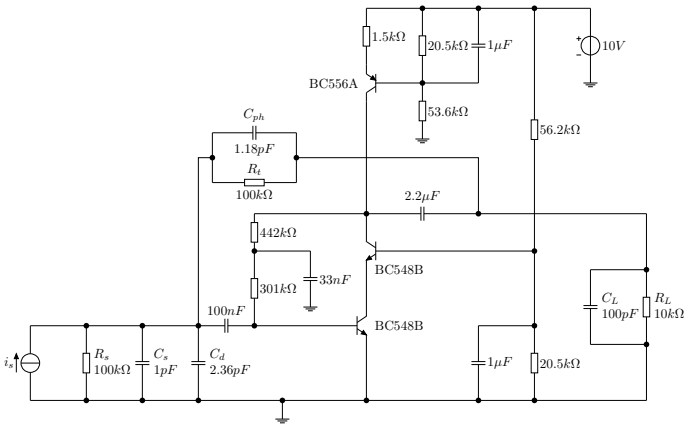
The effects of the non-zero input impedance of the transimpedance amplifier on $i_{dist,tot}$ can now be evaluated. As stated before, the effect is expected to be minor; the inaccuracy of the amplifier transfer function is just 0.4 dB[Ω]. Such a low value of the inaccuracy implies an input impedance much smaller than the impedance formed by Z_s and the two-wire line.

Using the accurate transmission line equations, the effect of the non-zero input impedance has been evaluated. It was found that over the frequency range of interest, the accuracy of the approximated value of $i_{dist,tot}$ is within 90 % (i.e., the inaccuracy is less than 1 dB), which is considered acceptable.

7.2.6 Measurements

The transimpedance amplifier as depicted in Figure 7.8(a) has been built and tested. The transimpedance was measured to be 99.6 dB[Ω] and the bandwidth 1.1 MHz. Compensation is realized by a C_{ph} of 1 pF. It should be noted that due to component spread in C_{ph} and the parasitic capacitance of R_t, the actual total compensation capacitance was approximately 1.6 pF. This was accounted for in the calculation of $i_{s,env}$ in Figure 7.8(b).

Generating an electromagnetic plane wave of 30 V/m and ensuring that this plane wave is received by the transimpedance amplifier, may be a tedious task. As shown in Section 7.2.1, the disturbance current is dominated by a capacitance and the electric field component. Therefore, it was chosen to capacitively couple the disturbing signal to the amplifier. Simulating field to wire coupling by coupling an equivalent signal via a conductance to the amplifier is a valid and generally used method for frequencies at which transmission line effects are minimal [156].



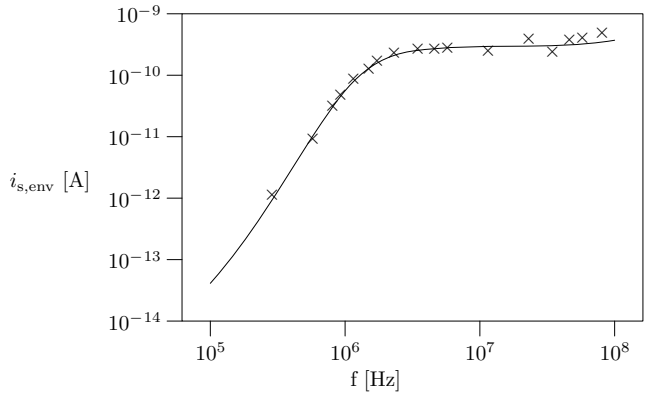


Figure 7.8: Schematic of the transimpedance amplifier, Fig. 7.8(a), and the amplitude of the equivalent envelope detection source at the input of the amplifier as a function of frequency, Fig. 7.8(b). The line in Fig. 7.8(b) is calculated. The crosses are actual measurements. The amplifier is frequency compensated to obtain a Butterworth characteristic. Note that the out-of-band measurements of interest are located above 1 MHz. The in-band detection components are shown for completeness.

The electric field component has been replaced by a voltage from a signal generator and the capacitance by a coupling capacitor equal to that of the (removed) two-wire line. The voltage was chosen such that i_{dist} at 1 MHz amounted to the required 568 nA. Due to the differentiating character of the coupling capacitance, i_{dist} increases with increasing frequency.

The measured and calculated values of $i_{s,env}$ are shown in Figure 7.8(b). The

measured values are in close agreement with the calculations and (as expected) no overshoot appears in both calculation and in measurement. Note that the out-of-band measurements of interest are located above 1 MHz. The in-band detection components are shown for completeness.

The calculated equivalent current $i_{s,env}$ flattens out at a maximum value of about 428 pA. This is close to the approximated value of 450 pA.

7.2.7 Discussion

This amplifier was designed to meet a certain SER specification for interfering fields up to 100 MHz. That does not imply that there are no other design solutions nor that this is the best one possible. For example, it can be expected that both noise and EMI requirements can be met by a (CMOS) FET implementation of the amplifier also. However, a more complicated, multistage solution will probably be required to meet the bandwidth specification due to the low LP product of a single stage FET (cascode) implementation.

Here, we have chosen to demonstrate that severe EMI requirements can be met with enough loop gain and a BJT cascode that is more nonlinear than a FET (cascode).

Extending the specification for the interference from 100 MHz to 1 GHz or higher, two extra effects have to be taken into account in the design process. Firstly, transmission line theory shows resonances in $i_{dist,tot}$ at frequencies higher than 1GHz. Secondly, r_B and $C_s + C_d + C_{ph}$ (in series with $C_\pi + C_{\mu 1}$) introduce a non-dominant pole in $\chi(\omega_c)$ at approximately 1.4 GHz. Its effect on the disturbance is that of a first-order low-pass filter. High-frequency maxima will thus be attenuated, leaving the maximum at ca. 340 MHz as the EMI determining value of $i_{dist,tot}$. A new, higher value of g_{m1} (and hence $A\beta_0$) will be needed. Our simple cascode amplifier may not meet the specifications and a different implementation could be required.

7.3 Multiple-stage transadmittance amplifier

Finally, the method to design a dual-stage negative-feedback amplifier with specified SER has to be checked and applied in an example. An application was chosen in which EMI susceptibility has to be low.

Equipment for magnetic resonance imaging (MRI) generates high levels of high frequency interfering signals during imaging. The main interfering high frequency signal is located at the Larmor frequency: $\omega_L = \gamma B_0$ [157][158]. γ is the gyromagnetic constant and is approximately 42.5 MHz, and B_0 is the flux of the static magnetic field. For a field strength of 3 T commonly used nowadays, ω_L is about 127.5 MHz. During imaging this frequency may be amplitude modulated [158]. If one wants to measure a bio-potential (e.g., electrocardiogram (ECG)), the SER of bio-potential amplifiers may be impaired by pick-up of the high frequency disturbance.

Measurements and discussions with MRI users in the Academic Medical Centre in Amsterdam showed that bio-potential amplifiers suffer from both high frequency interference and in-band interference caused by 'slice selection'. Each type of interference may severally impair ECG quality on its own [159], and hence, both types of interference should be adequately 'suppressed'. However, because the most important part of this work deals with out-of-band interference, it was chosen to concentrate on the high-frequency interference and to disregard in-band interference for the time being. See Subsection 7.3.11 for a possible solution for dealing with the in-band interference of the MRI.

The high frequency interference will generate both a differential-mode and a common-mode disturbance at the input of the amplifier. The common-mode disturbance is expected to be larger than the differential-mode disturbance, since the common-mode loop is larger than the differential-mode loop due to coupling (of the interconnect) to the environment (see Chapter 2). When the input of the amplifier is unbalanced, maximal common-mode to differential-mode conversion occurs. The resulting total disturbance (being the sum of the differential mode disturbance and the disturbance due to common-mode to differential-mode conversion) is maximal in this case. To demonstrate that it is possible to design negative-feedback amplifiers resilient to large high frequency disturbances, it was decided to design an amplifier with an unbalanced input.

Systems for bio-potential recordings often use instrumentation amplifiers (balanced negative-feedback voltage amplifiers) to suppress 50 Hz (or 60 Hz) common-mode mains interference, e.g., [18][160][161]. However, since MRI systems are used in screened rooms, 50 Hz interference was expected to be of minor importance. Hence, an unbalanced amplifier will suffice.

It was decided that a simple, one-channel system would be designed that had to meet two requirements. Firstly, it should be capable of measuring an ECG signal. Secondly, the system should be so immune that an interfering signal at 127.5 MHz with an amplitude equal to what was measured in the MRI would result in an equivalent detected envelope signal of the same order of magnitude as the noise. Note that the most important goal of the design is to demonstrate the design of an amplifier that has low EMI susceptibility. The proposed system may be regarded as an experimental set-up that may be developed into a multi-channel MRI-compatible bio-potential measuring system in the future. Such a multi-channel system is, however, beyond the scope of this work.

7.3.1 System design

The system is split into two parts: a battery powered front-end and a back-end that delivers the signal to the A/D-card of a computer (see Figure 7.9). The front-end consists of a pre- and post-amplifier. The electrical signal is converted to light by a LED. The light is transported through a plastic fiber to the back-end.

The preamplifier has to process the input voltage and it should be immune enough to the disturbing voltage at its input. Since a transadmittance amplifier is typically less susceptible to EMI than a voltage amplifier (see Chapters 5 and 6), a transadmittance amplifier is chosen as preamplifier. Its design will be

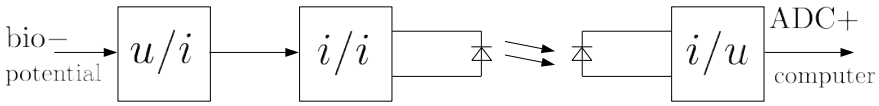


Figure 7.9: System design of the measurement system. The bio-potential is measured and converted to a current by a transadmittance amplifier. The current is amplified and converted to light by a current amplifier with optical feedback. Using a plastic fiber, light is transported to the back-end, which converts the signal to a data stream that can be displayed and stored on a computer.

extensively discussed in the following subsections. The post-amplifier thus has to process a current at its input and it has to deliver a current to the LED. Thus, a current amplifier is used as post-amplifier.

Optical feedback is used in the current amplifier to reduce distortion due to nonlinearities (e.g., due to junction heating [162]) in the current to light conversion in the LED. The light signal that is received at the back-end site does not suffer from an unacceptable level of distortion that may impair the quality of the ECG.

The receiver consists of a PIN photodiode (PIN photodiodes show excellent linearity [162][163]) that converts light into a current and a transimpedance amplifier that, finally, converts this current into a voltage that is processed further by a computer. This part of the system is straightforward, and its design is not discussed further.

An advantage of an isolated, battery-powered, front-end is that it ensures safety (a person under test cannot be connected to the mains in case of a faulty situation). Moreover, the small front-end can be placed near the patient, while the back-end may be in another room. For example, the patient resides in the MRI bore, while the back-end may be placed outside the Faraday cage enclosing the MRI-system.

To avoid interference from reaching the electronics directly, both electronics from the front- and back-ends have copper enclosures.

7.3.2 Specifications

The design of any amplifier system starts with specifying the source and load. Table 7.5 presents the signal source specifications.

The 3.2 cm^2 electrode with a mean impedance of 50 kΩ at frequencies lower than the pole is used in the design. It should be noted that the electrode impedance is subject to spread. Impedance variations of up to 30 % are common [165].

With a high-quality, low-noise system for bio-potential measurement [166] [161], a total noise (system plus electrodes) of about 1 μV_{rms} is expected [164]. However, more noise was measured (about 3 μV_{rms}). Possible explanations for this are electro-chemical reactions at the electrode-skin interface that generate

Table 7.5: Signal source specifications [18][161][164][165].

Biopotential specifications		
Signal	Max. voltage [mV]	Bandwidth [Hz]
ECG	5	400

Electrode (Ag-AgCl) specifications (3M, Red Dot)		
Size [cm^2]	Mean impedance [Ω]	Comment
3.2	50 k	Impedance shows a first-order behavior with a pole between 0.1 and 100Hz. No DC-current allowed through the electrodes. Up to 300 mV offset possible.
2.0	100k	

noise [164].

The system to be designed should have comparable noise specifications. Out-of-band interference caused by the HF pulses at the Larmor frequency may generate envelope detected voltages which are, preferably, about the same magnitude as the voltage noise and not larger. This level of detected voltage is acceptable, since the same amount of mains disturbance levels are considered acceptable in practice [160].

A. Interconnect

A two-wire line will be used to connect the electrodes to the input of the amplifier. The two-wires will pick-up interference from the MRI and transport it to the input of the amplifier. One side of the interconnect is connected to the preamplifier and the other side is connected via two 10 kΩ 'safety resistors' to the electrodes. The 10 kΩ resistors are considered nowadays to be more or less mandatory to prevent thermal burns due to induction in case of fault situations in the MRI.

Chapter 2 shows that the dimensions of the interconnect have to be small in order to decrease the amount of differential disturbance. The two-wire line therefore consists of two copper wires, taken from a ribbon cable, with a radius of about 0.1 mm, a distance between the wires of approximately 0.6 mm and has a length of 307 cm. The length can not be taken much smaller, since it should be able to cross the distance from the electrodes on somebody's chest in the bore of an MRI to the front-end outside of the bore.

The measured self-inductance, capacitance and resistance of the two-wire line is shown in Table 7.6. The measured self-inductance remains about the same with frequency. The capacitance shows a decrease of about 16% and the resistance a decrease of 25 % with increasing frequency. At higher frequencies, the capacitance measurement is probably affected negatively by metal objects in the surroundings.

Using Kaden's equation for the self-inductance of a two-wire line (Table 2.1),

Table 7.6: Measured two-wire line parameters. (LCR-meter PM6304 Philips/Fluke)

$f_{measure}$ [Hz]	Self-inductance [μH]	Capacitance [pF]	Resistance [Ω]
1k	2	139	3.2
10k	2	127	2.4
100k	1.9	117	2.4

results in a self-inductance of 664 nH/m, i.e., a total of 2.04 μH. Measured and calculated self-inductance are in good agreement. A resistance of about 1.37 Ω/m follows from the equation for the resistance, and therefore the total resistance is approximately 2.7 Ω, which is also accurate enough. A capacitance of 16.7 pF/m is found from Kaden's equation for a two-wire line with ε_r equal to one. However, ε_r is larger than one because of the wires insulation. The calculated value of C (ε_r of 2.7) is 45.1 pF/m, resulting in a total capacitance of 139 pF, which is about the same as measured.

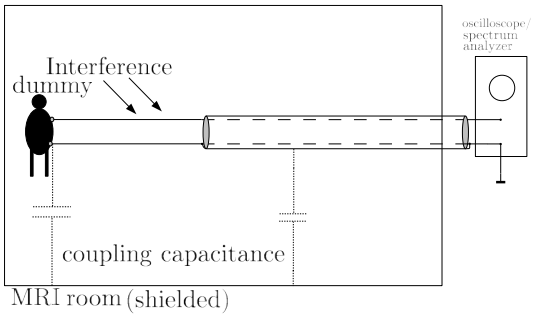
For the design, L_s equals 2.04 μH and C_s equals 139 pF are assumed. The wire resistance can be neglected with respect to the electrode impedance and the 'safety resistors' because it is small by comparison.

7.3.3 Measurements of 3T MRI induced interference

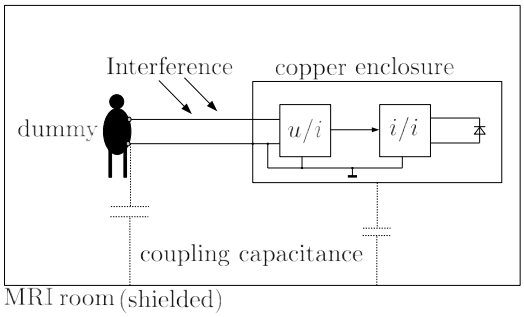
To get an idea of the disturbance that may be picked-up by the two-wire line, measurements were done in a 3 T MRI (Philips Intera scanner). Electrodes were placed on a dummy (a water filled jar) and were connected to the two-wires (see Fig. 7.11(a)). The largest distance between the electrodes was approximately 17 cm.

It should be noted that the measurements will only give an indication of the amplitude of the disturbance that can be expected in real cases. Real tissue, differences in distance between electrodes and differences in the length of the interconnect that is actually 'illuminated' in the MRI bore, etc., will cause differences from the values measured with the dummy. On top of that, extra uncertainty is introduced because measurement equipment can not be placed in the MRI room because of the large magnetic field.

Figure 7.10(a) shows a simplified drawing of the measurement set-up. The two-wire line will be the main receptor of the interference since it will go into the MRI bore. A shielded two-wire transmission line, which does not go into the MRI bore, is connected to the two-wire line. The latter is used to transport the disturbance out of the MRI room. The shielded transmission line used has a characteristic impedance of about 75 Ω and its length is approximately 13 m. Reflections occurring due to (characteristic) impedance mismatch will affect the measured interference level and add to the uncertainty. The disturbance has been measured both in the time domain and in the frequency domain.



(a) Interference is picked-up by the two-wire line and transported to the measurement equipment by a shielded transmission line.



(b) Interference is picked-up by the two-wire line and transported to the front-end of the system.

Figure 7.10: Simplified drawings of the measurement set-up and of the bio-potential measurement system. Interference is (mainly) picked-up by the two-wire line and transported to either an oscilloscope or spectrum analyzer (Fig. 7.10(a)), or to the input of the transadmittance amplifier (Fig. 7.10(b)). Note that common-mode to differential-mode conversion occurs in both cases.

Note that a common-mode loop exists formed by the two-wire line, the (distributed) coupling capacitances, and measurement equipment. It is not possible to present exact values of the coupling capacitances since they depend on the distance between the interconnects and the nearest conductive area, which may vary in practical cases. A value of several (tens of) picofarads may be expected (see Table 2.1).

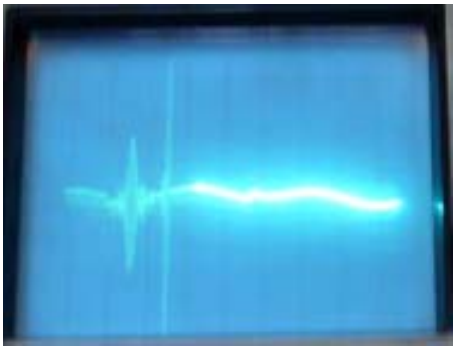
The measurement equipment has an unbalanced input, resulting in a maximal common-mode to differential-mode converted disturbance. A comparable common-mode loop and common-mode to differential-mode conversion exists when the system (to be designed) is realized as shown in Figure 7.10(b).

Measurements with a (Tektronix 454A) 150MHz oscilloscope (Z_{in} equals 1 MΩ//15pF) have been performed in order to characterize the pulses in the time domain. The MRI performed the 'echo planar imaging (EPI)' sequence,

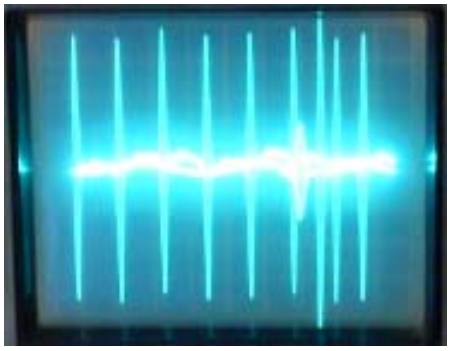
since this was regarded to be a sequence that caused a lot of interference[6]. Fig. 7.11(b) gives an impression of the EPI sequence. It can be seen that the maximum (peak) value of the interference is approximately 2V. The pulses can therefore be regarded as having an amplitude of 1V and a modulation depth (m) of 1.

Fig. 7.11(c) shows another sequence (gradient spin echo). The gradient pulses show a peak value of about 2 V, with occasionally a maximum of ca. 2.6 V, and a repetition frequency of about 167 Hz in this case. Again we can assume an amplitude of about 1 V and an m equal to 1.

(a) Dummy.



(b) Echo planes imaging sequence.



(c) Gradient spin echo sequence.

Figure 7.11: Dummy used for measuring 3 T MRI high frequency pulses and two kinds of sequences. Oscilloscope settings: 0.5 V/div, 5 ms/div.

The EPI induced disturbance was also monitored with a Hameg (HM5006) spectrum analyzer (50 Ω input impedance). The input attenuation was set to 30 dB and the frequency scanwidth varied between 0.1 MHz/div and 50 MHz/div, depending on the frequency range of interest. The filter bandwidth was chosen to be 20 kHz or 200 kHz accordingly, to assure accurate measurements.

[6]Dr. ir. A.J. Nederveen, Academic Medical Centre, private communication.

Due to the non-continuous character of the signals, see Fig. 7.11(c), some averaging occurs in the spectrum analyzer. The measured values are therefore a bit lower than the actual peak values. This may, however, not be the case in the lower frequency range (Table 7.7, first row), since these signals were also measured without a sequence being made. Table 7.7 gives an example of some of the measured values. Note that the spectrum analyzer measures the power in

Table 7.7: Disturbance measured with the spectrum analyzer (see Fig. 7.10(a)). The second row presents the input voltage (calculated from the measured input power in dB), the third column shows the (estimated) values if the input impedance would be the same as that of the oscilloscope. The fourth column shows the multiplication factor used, which follows from Figure 7.12(b). The disturbance at 127.5 MHz is pulsed (as far as we could determine, this was not the case at the other frequencies). Therefore, averaging occurs during the measurement. The value between the brackets at 127.5 MHz is the measured value without taking averaging into account; averaging is taken into account in the value without brackets.

frequency [MHz]	approx. measured peak voltage [mV]	approx. corrected peak voltage [mV]	multipl. factor
10	0.2	7	35.5 (31 dB)
30	0.2	15.9	89.1 (39 dB)
50	0.2	1.6	7.9 (18 dB)
100	0.4	1.1	2.8 (9 dB)
127.5	14	(220) 880	15.8 (24 dB)
170	0.4	0.5	1.2 (1.6 dB)
350-360	4	1.5	1 (-0.26 dB)
460-500	2.8	0.8	0.6 (-4.2 dB)

dB, which has to be converted to a voltage so it can be compared to the voltage measured by the oscilloscope. The corresponding peak voltage of the measured power values are calculated and presented in the second column of the table. The disturbance amplitudes measured with the oscilloscope and the spectrum analyzer differ, specifically at the most important frequency (127.5 MHz). This is due to the differences in input impedance and some averaging.

In order to check the measurements, the disturbance that would be measured with the spectrum analyzer when it would have an input impedance of 1MΩ//15pF, is calculated. It is expected that the disturbance found in this way has approximately the same value as the one measured with the oscilloscope. The third column presents the values that would be measured in that case; the fourth column shows the multiplication factor that was used. The disturbance at 127.5 MHz shows a corrected value between brackets, and one without brackets. The first shows the corrected value without taking averaging into account, the latter the corrected value taking averaging into account, also. What kind of

correction has been applied, is discussed next.

Although the EM environment in the MRI bore is very difficult to model, it is possible to estimate the differences in disturbance levels between the low impedance (50 Ω) and the high impedance (1MΩ//15pF) using the models and equations presented in Subsections 2.6.2 and Section 2.7. Note that these models are simplified approximations of the electromagnetic coupling that may occur in the MRI bore. They can, however, be used to check if the large difference between the high and low input impedances are plausible.

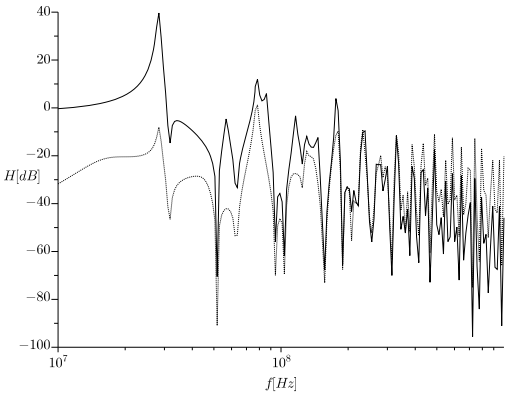
The earlier mentioned models and equations were used to estimate the transfer of the EM field to the total disturbance, being the sum of the differential-mode disturbance and the disturbance resulting from common-mode to differential-mode conversion. Plots of the transfer (H) are shown in Fig. 7.12 and are normalized in such a way that low frequency value of H depicted by the solid line corresponds to 0 dB. Figure 7.12(a) shows that the disturbance in case of a high input impedance (1 MΩ// 15 pF) (solid line) is higher than in case of a low input impedance (50 Ω) (dotted line). At 127.5 MHz this difference is about 24 dB (see Fig. 7.12(b)). On top of that should be noted that the spectrum analyzer measures continuously, while the (127.5 MHz) disturbance is pulsed. The measured value is averaged. From the measured pulses, it was estimated that the peak value should be a about a factor four higher (12 dB). If we take the measured value of 14 mV from the spectrum analyzer and multiply this with 63 (36 dB), a value of 0.88 V_{peak} is found[7]. This is indeed of the same order of magnitude as the value measured with the oscilloscope. The calculation shows that the large difference in measured values between the oscilloscope and the spectrum analyzer are plausible.

The shielded transmission line for signal transport will not be used in the final system. Its effect will be a frequency dependent attenuation and reflections affecting the magnitude of the disturbance. The first effect, however, is so low that it may be neglected in the frequency range of interest. Reflections may attenuate the disturbance at certain frequencies. At other frequencies hardly any attenuation occurs, so the maximum disturbance will be delivered to the load. Evaluation at 127.5 MHz showed that the transmission line used for signal transport hardly attenuates the signal at 127.5 MHz.

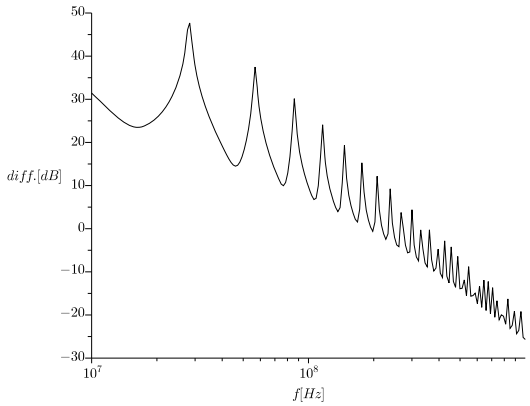
In the lower frequency range, a relatively high (constant envelope) disturbance of about 0.13 V_{peak} can be expected (see the thick lines in Figs. 7.11(b) and 7.11(c)). The disturbance between 10 MHz and 127.5 MHz, and at frequencies higher than 127.5 MHz, are lower than at 127.5 MHz (see Table 7.7) and will therefore have less effect. On top of that, these disturbances are not modulated (as far as could be determined), reducing their detrimental effect to a DC shift that is easily compensated. The non-constant envelope disturbance at 127.5 MHz will therefore most probably have the most detrimental effect.

Both measurements with the oscilloscope and with the spectrum analyzer

[7]Note that a difference of 25 dB instead of 24 dB would have resulted in almost exactly 1 V_{peak} of disturbance. Because of the simplified models, it is reasonable to assume that this one dB more disturbance may occur in practical cases.



(a) Simulated total disturbance in the two-wire line normalized to 0 dB. The solid line shows the transfer when the load is a 1 MΩ//15 pF impedance and the dotted line shows the transfer in case of a 50 Ω load.



(b) The difference between the total disturbance in case of the high impedance load (1 MΩ//15 pF) and the low impedance load (50 Ω). The difference is 24 dB at 127.5 MHz.

Figure 7.12: Estimated transfer of interference (common-mode and differential-mode) to a disturbance voltage across a load of 1 MΩ//15 pF and a load of 50 Ω.

(after correction) show corresponding magnitudes of the dominating disturbing voltage at 127.5 MHz. Therefore, we confirm a signal of about 1 V_{peak} (and m of 1) from these measurements. The amplifier to be designed will most probably have an input impedance comparable to that of the oscilloscope. The amount

of disturbing voltage at the input of the amplifier can thus be expected to be about the same[8]. No clipping is allowed to occur in the amplifier due to this disturbance in the amplifier to be designed. Moreover, the resulting detected envelope should have the same order of magnitude as the noise.

7.3.4 Magnitude of the required transfers

It is beneficial when the transadmittance has a larger value in the signal passband than for signals higher than the passband. Since the passband is low frequency, some kind of bandwidth limiting is probably needed.

A transadmittance of 1 S was chosen; i.e., an amplitude of 5 mV corresponds to a current of 5 mA through the LED. The total transfer is to be divided over the transadmittance amplifier and the current amplifier. A large transadmittance (of the transadmittance amplifier) may result in a relatively small loop gain that may affect the accuracy of the transfer in the passband and perhaps EMI susceptibility. Therefore, a transadmittance equal to -10 mS was chosen. The current amplifier should have a gain of 100 with a bandwidth of 400 Hz, which is feasible.

7.3.5 Design of the feedback network

A transadmittance of -10 mS is required with a bandwidth of about 400 Hz. Since it can be expected that a transadmittance amplifier will easily reach larger bandwidths, the bandwidth has to be limited. A way to accomplish this is shown in Figure 7.13. The transadmittance, γ, in the passband is given by

$$\gamma = -\frac{R_1 + R_2 + R_3}{R_1 R_3}, \tag{7.9}$$

while it reduces to $\gamma = -1/(R_1//R_3)$ for frequencies larger than the bandwidth. The bandwidth is determined by R_2 and C. With R_1 equal to 5.1 kΩ, R_2 equal to 162 kΩ, and R_3 equal to 3.3 kΩ, γ equals -10.1 mS in the passband and -0.5 mS for frequencies sufficiently higher than the passband.

The signal bandwidth is probably smaller than the bandwidth that follows from the LP product. Thus, B will be used to denote the signal bandwidth and ω_0 to denote the bandwidth of the amplifier.

[8]Simulations show that the exact value of the input impedance of the negative-feedback amplifier to be designed does not matter much as long as it is of the same order of magnitude as the impedance of the oscilloscope.

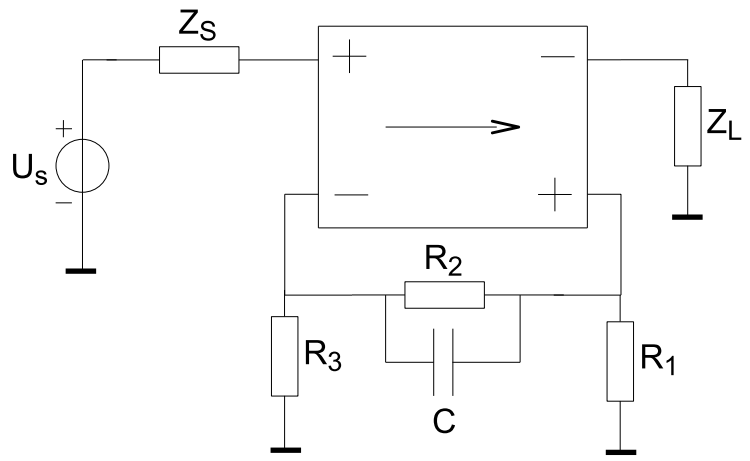


Figure 7.13: Transadmittance amplifier with high transadmittance in the pass-band (γ= -10 mS) and low transadmittance at higher frequencies (γ= -0.5 mS).

7.3.6 Noise calculation and input stage bias current

The following equation holds for the spectral voltage noise density (at low frequencies) of the transadmittance amplifier in Fig. 7.13.

$$\begin{aligned} S_{u_{n,eq}} =& S_{u_n} + S_{i_n}\left[R_s + R_3\left(\frac{R_1+R_2}{R_1+R_2+R_3}\right)\right]^2 + \\ & 4kT\left[R_s + (R_1+R_2)\left(\frac{R_3}{R_1+R_2+R_3}\right)^2 + R_3\left(\frac{R_1+R_2}{R_1+R_2+R_3}\right)^2\right]. \end{aligned} \tag{7.10}$$

R_s is the source resistance, S_{u_n} and S_{i_n} are the spectral voltage and spectral current noise densities of the input stage (see Chapter 5), respectively. The effect of capacitance C is disregarded.

The noise specification can be met with both a BJT and a FET differential stage. In case of a BJT input stage, a bias current of several tens of micro-amperes up to a few hundred micro-amperes (depending on the BJT) follows from the noise calculations, since R_s is large. It is expected that a cascoded JFET stage may require a larger drain current to meet the noise specifications. As a consequence, the JFET will contribute more to the loop gain than the BJT, which is beneficial for accuracy, distortion, and EMI. Therefore, a differential JFET input stage is chosen.

The equivalent input noise power $\overline{u_{n,eq}^2}$ is given by

$$\overline{u_{n,eq}^2} = qI_{gQ}B\left(R_s + R_3\left(\frac{R_1+R_2}{R_1+R_2+R_3}\right)\right)^2 + 4kT\left\{B\left[R_s + (R_1+R_2)\left(\frac{R_3}{R_1+R_2+R_3}\right)^2 + R_3\left(\frac{R_1+R_2}{R_1+R_2+R_3}\right)^2\right] + \frac{c}{g_{m1}}f_l \ln\left(\frac{f_H}{f_L}\right)\left[2 + \frac{1}{6}(2\pi f_H C_{iss})^2\left(R_s + R_3\left(\frac{R_1+R_2}{R_1+R_2+R_3}\right)\right)^2\right]\right\}. \tag{7.11}$$

The gate current is I_{gQ}, B is the bandwidth ($f_H - f_L$), and f_H and f_L are the upper and the lower corner frequencies, respectively. The flicker noise corner frequency is f_l. It is incorporated in the equation because of the relatively small bandwidth.

The differential JFET will generate acceptably low noise levels ($\overline{u_{n,eq}} \approx 1.1\ \mu$V) when g_{m1} is about 40 μA/V^2. The transconductance can be increased in a straightforward manner to further increase the contribution that the stage will make to the loop gain. This will decrease both noise and EMI susceptibility.

A dual JFET of type U406 [154] was selected and biased at an[9] I_{dQ} of 2 mA. The transconductance g_{m1} is now expected to have a value of about 3.6 mA/V, resulting in $\overline{u_{n,eq}}$ being approximately 0.42 μV.

7.3.7 Output stage

The minimal bias current is taken to be 1.5 times the signal current through the load ($\hat{i}_l$), to avoid clipping distortion (see Subsection 5.2.4 and [3]). A bias current approximately equal to 2 mA ($\hat{u}_{dist,max}|\gamma|\cdot 1.5$) is found, when a maximal disturbance voltage of 2.6 V with a frequency lower than ω_0 at the amplifier input is assumed. This is a worst case assumption. To prevent voltage clipping in the output stage, $|U_{ceQ}| > \hat{i}_l Z_t + U_{ceMIN} > 2.9$ V. An $|U_{ceQ}|$ of 5 V is taken in the first design steps.

Local feedback at the output stage can be avoided by using a differential stage. The output stage is implemented with PNP BJTs of type BC857 [126]. This BJT type combines a large β_{ac} (approximately 277) with a high f_t (approximately 144 MHz).

7.3.8 Linear transfers

A cascoded differential JFET input and BJT output implementation of the nullor results in $-A_i\alpha_{20}\beta_0$ being approximately 55.3 in the passband. This results in an accuracy of 98.2 % in transadmittance, which is acceptable.

[9] This is a trade-off between the chance of I_{dQ} being larger than the drain current in saturation (typically 3 mA, maximally 10 mA, and minimally 0.5 mA [154]) and the contribution the JFET can make to the loop gain.

Transadmittance γ equals -0.5 mS between $\omega_a \approx 1/(C(R_1 + R_3))$ and ω_0, while $-A_i\alpha_{20}\beta_0$ is increased to approximately 1k. Transfer ξ_{i0} is about 1, resulting in χ_{10} of about $0.9{\cdot}10^{-3}$.

The output stage will introduce a pole p_o at approximately -2.9 Mrad/s ($-\omega_{To}/\beta_{aco}$). The source and two-wire line impedances are so low that they can be neglected at frequencies higher than ω_a. An input pole (p_i) is thus created by the input capacitance of the FET stage and R'_t (being the parallel connection of R_1 and R_3); p_i is about -122 Mrad/s. The expected bandwidth (ω_0) is approximately 596 Mrad/s (95 MHz).

Transfer ξ_1 has a pole p_i, but also a pole (p_{tw}) estimated by $-1/(2R_{\text{safety}}C_s)$ when the electrode impedance is neglected. Pole p_{tw} is located at about -360 krad/s. This pole is non-dominant and will not affect signals in the passband, but it will attenuate low-frequency interference.

The two-wire line is electrically long for interference higher than approximately 10 MHz. Transmission line equations are used to describe signal transport by the two-wire line to the input of the amplifier. Now, no pole p_{tw} occurs in ξ_{i1} due to the two-wire line. Several resonances and anti-resonances can be identified, however, that cause the interference to decrease or increase with frequency. The amplitude of the main interfering frequency to be expected at the input of the amplifier has been measured and is known. For reasons of simplicity we use the measured data and disregard pole p_{tw} in the further (EMI) analysis.

As a result we have a ξ_{10} of one and a pole, p_i for the transfer of the interference. Considering $\chi_{1,max}$, we find $\chi_{1,max}$ to be about 0.13 in the case of a frequency-compensated amplifier, and even about 0.92 in the case of an uncompensated one. With a peak disturbance $\hat{u}_{\text{dist.}}$ of 2.6 V, a differential input voltage of 0.34 V and 2.39 V, respectively, can be expected. The latter differential voltage is large enough to cause clipping in the amplifier. When the amplifier is ideally compensated, no clipping occurs. However, when compensation is less ideal, or a non-dominant pole occurs at too low a frequency, the risk of the differential input voltage becoming so large that clipping (or periodically forward biasing of the gate-source junction) still occurs, is too large. Transfer $\chi_{1,max}$ should therefore decrease significantly, by decreasing ω_0.

It was found that both p_i and p_o had to be shifted to a lower frequency. Pole p_o was shifted to -572 krad/s by adding a 4.7 pF Miller capacitance to the output stage. Adding 235 pF to the input of the differential JFET stage and 'decoupling' the two-wire line with a resistor, R_{shift}, of 6.8 kΩ, shifts pole p_i to approximately -1.96 Mrad/s. Fig. 7.14(a) shows the design.

Transfer $\chi_{1,max}$ is approximately $37.5{\cdot}10^{-3}$ after frequency compensation and ω_0 is about 33.5 Mrad/s (5.3 MHz). No clipping will occur with this value of $\chi_{1,max}$. Unfortunately, however, a non-dominant pole and a zero affect the ideal second-order behavior. Overcompensation is necessary to prevent $\chi_{1,max}$ from deviating too much from the previously calculated value. A compensation capacitance, C_{ph} (8 pF), has to be connected between R_{shift} and the reference (see Fig. 7.14(a)) in order to introduce a phantom zero with appropriate value[10]

[10] A common place to introduce a phantom zero is in the feedback network [3]. Here, how-

(near -18 Mrad/s). As a result we now have a $\chi_{1,max}$ of about $30{\cdot}10^{-3}$ and and an ω_0 of approximately 26.4 Mrad/s (4.2 MHz).

Note that although the combination of R_{shift} and C_{ph} looks like a low-pass filter, its effect is not that of a low-pass filter. The transfer from the signal source u_s to the input of the amplifier is determined by poles p_i and p_o. Since p_i is determined by the 240 pF input capacitance, the additional 8 pF from C_{ph} hardly affects p_i, so no low-pass filtering occurs. The effect of C_{ph} is that for frequencies higher than the phantom zero, the attenuation in the feedback loop (β) is reduced, forcing the system poles into (approximately) Butterworth positions. The transfers will not be much affected by R_{shift} and C_{ph} for frequencies higher than ω_0. Simulations show that χ_1, χ_2, and γ are indeed only about 4.4 dB less in the compensated case than in the uncompensated case at 127.5 MHz.

7.3.9 EMI behavior of the transadmittance amplifier

Using the simplified equations presented in Chapter 6, it is found that the transadmittance amplifier will meet the EMI specifications without difficulty. However, both differential input and output stages will affect each others' nonlinear behavior in a complicated way (see Appendix D). Equivalent voltage source u_{s,ω_l} may be higher than follows from the simplified equations, so it should also be checked with the elaborate equations of Appendix D. The result is depicted by the solid (perfectly matched FETs) and dotted lines (10 % mismatch) in Figure 7.16.

It can be seen that up to about 4 MHz u_{s,ω_l} increases due to the fact that χ_1 becomes so high that the input stage determines u_{s,ω_l}. The influence of the input stage rapidly decreases for frequencies higher than 4 MHz. For frequencies higher than about 30 MHz, the output stage contributes more to the nonlinearity than the input stage, but the contribution of the input stage cannot be neglected.

Simulations and calculations show that the design will meet the specifications; $u_{s,\omega_l} \approx 76$ nV at a frequency of 127.5 MHz.

7.3.10 Measurements

Figure 7.14(a) shows the simplified diagram of the transadmittance amplifier. The required common-mode bias circuitry is omitted for clarity. The realized amplifier on its printed circuit board is depicted in Figure 7.14(b)

Table 7.8 shows the measured specifications. The total system gain is 1786 instead of the specified 1000. The current gain of the optically fed back amplifier in the front-end was found to be too large, 178.6 instead of 100, due to excessive optical attenuation. This can be corrected in either the optical or electrical domain. However, since this gain is not critical for this system, it was decided to leave it unaltered.

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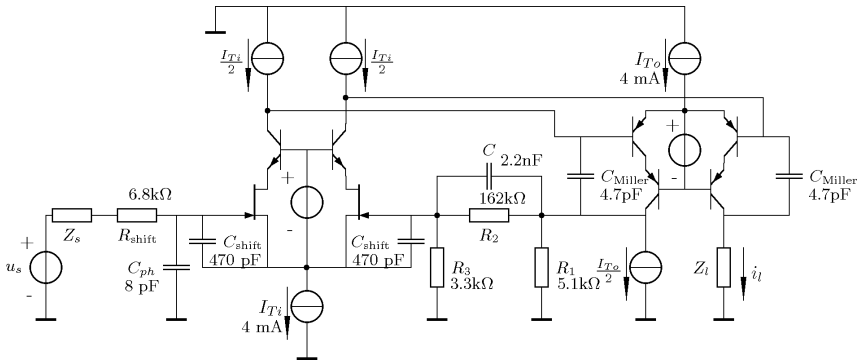
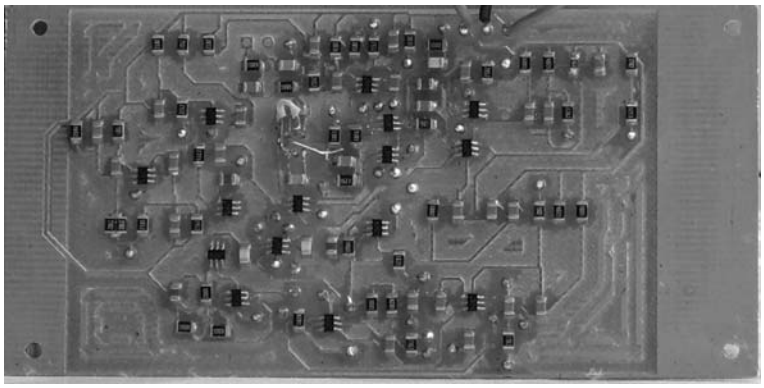
ever, it was found that a phantom zero in the feedback network was ineffective because the (inevitable) accompanying pole was located near the phantom zero, making it ineffective. A phantom zero at the input is effective because the accompanying pole is located at a much higher frequency (approximately -156 Mrad/s).



(a) Simplified schematic of the transadmittance amplifier. R_{shift}, C_{shift} and C_{Miller} are necessary to realize a reasonable value of χ_1 so that clipping is avoided. C_{ph} introduces a phantom zero, frequency compensating the amplifier. R_{shift} and C_{ph} do *not* filter the input signal.



(b) The transadmittance amplifier on a printed circuit board (PCB), including common-mode bias circuitry. Note that the PCB can be improved from an EMC point of view.

Figure 7.14: The realized transadmittance amplifier.

The transadmittance(s) and bandwidth(s) correspond well to the calculated values. The noise is, however, about twice as large as was calculated. This is due to the current amplifier generating a relatively large current noise, caused by the transfer from the current to optical domain and vice-versa in the feedback. When this current noise is transferred to the input of the transadmittance amplifier, it is found that it adds almost the same noise as the transadmittance amplifier itself, explaining the 3 dB increase in the measured noise.

To demonstrate the ability to measure ECGs, the author's ECG has been measured with the system, which is depicted in Fig. 7.15.

Figure 7.16 shows the calculated, simulated, and measured values of u_{s,ω_l} as a function of frequency. The measurements were performed with the set-up shown

Table 7.8: Specifications of the final system

Power supply:	± 15 V	Conditions
Current consumption Transadmittance amp.: Total system:	 ca. 12 mA ca. 70 mA	
Transadmittance:	-9.9 mS	160 mHz−442 Hz
Bandwidth:	-505 μS	9.6 kHz−4 MHz
Noise: (no electrodes but with 2·10 kΩ safety resistors)	≈ 0.9 μV	
Total system gain:	1786 [V/V]	

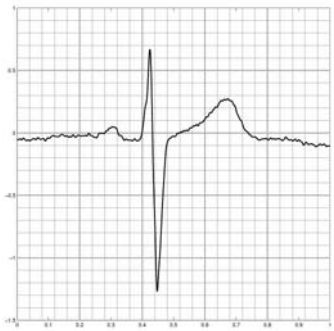


Figure 7.15: ECG measured with the system described in this section. The horizontal axis is the time (1 s), the vertical axis the output voltage (-1.5−1 V).

in Fig. 7.3, with the u to i converter, the buffer amplifier, and the fourth-order low-pass filter removed. The function generator, however, now was a Rhode & Schwarz SMS 2 and the oscilloscope a HP54610A (500 MHz). All measurements are normalized to a disturbing input voltage of 1 V_{peak} and a modulation depth (m) of 1.

Calculations and simulations showed that replacing the interconnect and safety resistors by the function generator do not significantly affect the pole locations and amplifier behavior. Therefore $u_{s\omega_l}(\omega_c)$ is not affected. EMI behavior of the amplifier with interconnect, safety resistors and electrodes is thus expected to be equal to that of the amplifier in the measurement set-up.

Both solid and dotted lines are calculated. Note that the second-order nonlinearity of the output stage also depends on how accurately $g_{\pi 2}$ of the output stage equals g_{m2}/β_{ac}. The solid line shown in Fig. 7.16 holds in case x equals 0.995, matched transistors and equal biasing of the differential stages.

By deliberately introducing some unbalance, the nonlinearities of the input FETs and output BJTs may add up to a lower total second-order nonlinearity

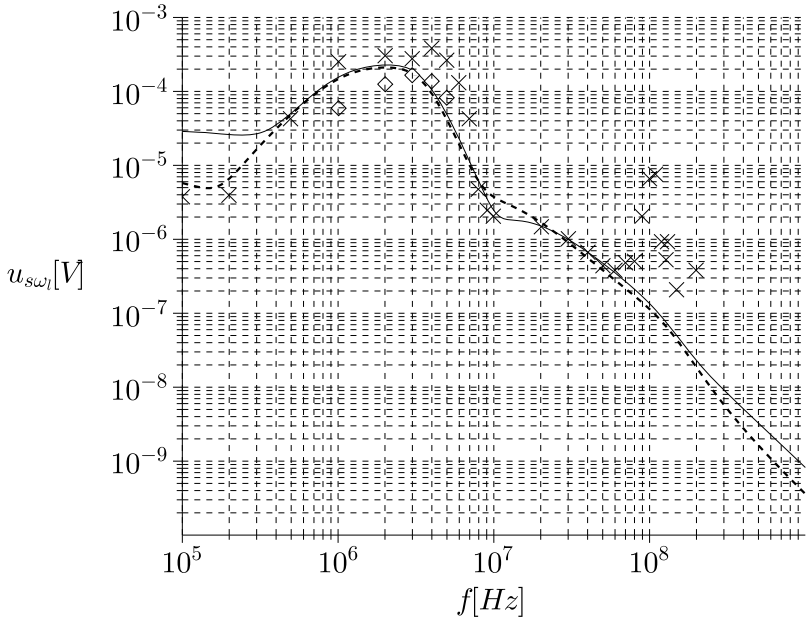


Figure 7.16: Equivalent voltage source $u_{s\omega_l}$ as function of the frequency. Disturbance: 1V, m=1. Both solid and dotted lines are calculated, the diamonds are simulation results and the crosses are measurement results. Note the resonance occurring near 100MHz. The solid line depicts the response in case of matched transistors and biasing (x=0.995). The dotted line represents the case of 10 % mismatch between the FETs and both output transistors having slightly different values of x (0.999 and 1.008, respectively). See text for discussion.

than in case of exactly equal transistors. In case of the dotted line, both output transistors have slightly different values of x: x equals 0.999 and 1.008, respectively, and the second-order nonlinearity of the FETs differ by 10 %. Now, the low-frequency calculation corresponds better to the measurements. The designer should, however, not deliberately design for this effect since it depends too much on parameter values that are subject to spread.

It can be seen that slight differences in biasing and transistor parameters have a considerable effect on u_{s,ω_l}. In order to get an idea of possible responses, we can draw lines for several values of x, mismatches in biasing, and transistor parameters. Here, we do not elaborate on that.

The input stage causes u_{s,ω_l} to have a relatively large value up to about 4MHz due to the zero that occurs in χ_1. It can be seen that both measurements

and simulations[11] of the complete amplifier, thus including bias circuitry, show a roll off of u_{s,ω_l} at a slightly higher frequency than the calculations. The latter is based on hybrid-π models and first-order approximations of the bias source impedances. It is reasonable to attribute the differences between measurement, simulation and calculations to this. On top of that, transistor parameters may deviate to some extent from their SPICE model parameters, and finally the biasing may be slightly different (e.g., corresponding more to the case that results in the dotted line). Considering this, specifically in the range 8 MHz−60 MHz, measurements and calculations agree to within 1.4 dB (solid line).

At about 100 MHz a resonance occurs in the measurement that is not accounted for in the calculation. It was found that the resonance was due to a non-optimal printed circuit board design, the assembly of the interconnect in the enclosure, and the enclosure itself. It was, e.g., possible to decrease or increase u_{s,ω_l} by 'playing around' with metal plating in the enclosure. It is therefore reasonable to assume that a more carefully realized system will show no resonance, or a resonance with a much lower peak. Nonetheless, the system does meet the design requirement: u_{s,ω_l} was measured to be about 0.5 μV at 127.5 MHz.

7.3.11 Resolving in-band interference problems

When trying to measure bio-potentials in an MRI system, two types of in-band interference can be distinguished

- Interference due to movement of wires caused by breathing.
- Interference caused by 'gradient pulses' used for slice selection.

Screening to reduce interference is difficult. Metal screens may interfere with the imaging system, and cause distorted images. Conductive coating may be tested, since its conductivity is much less than a metal, the image distortion may be less. This approach may reduce capacitive coupling, but inductive coupling remains. More research on this topic has to be performed.

Another method to reduce interference may be by using balancing[12]. When a second amplifier is used that is not connected to the electrodes, but does receive the same amount of disturbance (e.g., by connecting its interconnect in a small loop around the electrodes) it will generate the same in-band disturbance at its output as the bio-potential measuring amplifier. Both in-band disturbances can be subtracted, leaving only the bio-potential. A reduction of the in-band gradient to about 20% of its magnitude was observed using this approach [159]. This may be not enough, but it should be possible to improve this figure. More research has to be performed on this topic as well.

[11] Note that no simulation results are presented at frequencies higher than 7 MHz. Even with contemporary computers, simulation time and file size become so long that it is impractical to perform accurate simulations at higher frequencies.

[12] Note that using a balanced input amplifier will reduce common-mode to differential mode conversion of the (out-of-band) disturbance. The total disturbance reduces and u_{s,ω_l} will become even smaller.

7.4 Conclusions

Three examples to demonstrate the models of active devices and the design method presented in the earlier chapters are presented in this chapter.

Firstly, the dependence of EMI on the loop gain and the location of the dominant poles of a negative-feedback amplifier, as discussed in Chapter 5, was demonstrated by calculations and measurements on a JFET transimpedance amplifier.

Secondly, the systematic design of a transimpedance amplifier with specified EMI behavior was presented. The transimpedance amplifier was designed to have a transimpedance of 100 kΩ, a bandwidth of 1 MHz, and a minimal signal-to-error ratio of 70 dB, resulting from both noise and interference, while being subjected to (the equivalent disturbance of) a plane wave of 30 V/m with a modulation depth equal to one.

The expected amount of disturbing signal at the input of the amplifier due to an interfering electromagnetic plane wave was approximated using the methods presented in Chapter 2.

The bipolar junction transistor cascode (see Chapter 4) was used as nullor implementation. The required transconductance to reach the specifications was calculated, from which the biasing of the cascode followed. Measurements were in good agreement with calculations and simulations, and thus support the method presented in the previous chapters.

Finally, a dual stage transadmittance amplifier was designed for a bio-potential measurement system. It used cascoded differential input and output stages for low second-order nonlinearity and high loop gain. The amplifier was designed to have an equivalent EMI source voltage of the same order of magnitude as the equivalent noise voltage (1 μV) while being subjected to an input disturbance voltage of 1V at 127.5 MHz and a modulation depth of 1. This kind of disturbance may be found in 3 Tesla magnetic resonance imaging systems.

It was found that the system met the specifications. An ECG was successfully measured and the measured equivalent EMI voltage was about 0.5 μV at 127.5 MHz (despite the occurrence of an unmodelled system resonance, which increased EMI susceptibility at about 100 MHz).

The design may be regarded a first step towards the development of an MRI-immune bio-potential measurement system. Only the in-band interference problems still have to be solved.

Chapter 8

Conclusions and recommendations

This chapter presents the overall conclusions in Section 8.1 and the original contributions made in this thesis in Section 8.2. Finally, some recommendations for future research are given in Section 8.3.

8.1 Conclusions

Just like any other electronic circuit, negative-feedback amplifiers are subject to noise, speed and signal power limitations. On top of that, susceptibility to electromagnetic interference (EMI) hampers the information processing done by the negative-feedback amplifier (and other types of electronics) even further. In this work, it is assumed that EMI causes a disturbance at the input of the negative-feedback amplifier, since it is the most susceptible place and the disturbance is usually easy to attenuate at other places by filtering or shielding.

Chapter 1 shows that EMI from out-of-band signals (i.e., signals with a frequency much larger than the bandwidth of the amplifier) may result in a DC shift and detection of the low frequency envelope variations (envelope or 'AM' detection) of the high frequency interference, caused by even-order nonlinearities in the active devices. Noise, distortion and EMI introduce errors in the signal transfer and thus reduce the signal-to-error ratio (SER). It is therefore necessary to take these three error sources into account (and minimize them) in the design of negative-feedback amplifiers. EMI in particular may cause the SER to become unacceptably low.

In this work, the design of the interconnect from signal source to the negative-feedback amplifier, the (shielding) enclosure, and the amplifier are orthogonalized. Firstly, the interconnect and enclosure are designed for low electromagnetic coupling, under the assumption that the interconnect is loaded by an ideal amplifier. Secondly, the amplifier is designed for a sufficiently high SER. In principle, the interconnect design is not changed during design of the amplifier. Verifica-

tion that both interconnect and the implementation of the amplifier meet the specifications can then be checked by simulation.

Chapter 2 presents equations that enable the designer to determine the maximal dimensions of the interconnects and/or whether shielding is required. The necessary knowledge to design negative-feedback amplifiers with a sufficiently high SER is presented in the subsequent chapters.

Nonlinear behavior of the bipolar junction transistor (BJT) and field-effect transistor (MOSFET, JFET, and MESFET) is investigated in Chapter 3. Modified hybrid-π models of both types of transistors are presented. They enable both linear and second-order nonlinear analysis and design.

Nonlinear behavior is strongly dependent on the impedances connected to the transistor. For low distortion, both types of transistors are preferably loaded by impedances much lower than their output impedances. In case of FETs, the load impedance is preferably so much smaller than the output resistance of the FET that cascoding of the FET is recommended. The BJT is preferably current driven. The larger the impedance of the signal source, the smaller the nonlinearity of the BJT. The actual value of the second-order nonlinearity becomes harder to determine with increasing source impedance and the uncertainty in its value (and therefore in the second-harmonic distortion and EMI) also increases. However, this drawback is easily accounted for in the design process of the amplifier.

Since BJTs and FETs often behave rather poorly regarding the accuracy of their transfers, high-frequency behavior and/or nonlinearity, special combinations of active devices have been developed by designers: the cascode stage and the differential stage. They are investigated in Chapter 4.

Cascode stages usually show improved high-frequency behavior, since the Miller-effect is reduced. Nonlinear behavior of a BJT cascode stage (a common-emitter (CE) stage loaded by a common-base stage) is comparable to the nonlinear behavior of the CE stage. The nonlinear behavior of a FET cascode is, however, improved with respect to the nonlinear behavior of a CS stage. The cascode effectively reduces the detrimental effect of the nonlinear output resistance of the FET.

Even-order nonlinearity is absent in differential stages, and thus second-harmonic distortion and EMI (ideally) do not occur. In reality some even-order nonlinearity still remains, which can be determined using a newly developed model. Apart from accurately describing the linear and second-order nonlinear behavior of the differential stage, the effects of, e.g., bias current imbalance and transistor mismatch can also be analyzed with this model. Using this model, it has been shown that second-order nonlinearity can be minimized by ensuring that the impedance of the tail current source (connected to the emitter and source nodes, respectively) is as large as possible. At high frequencies, it should still be an order of magnitude larger than the input impedances of the differential stage.

Second-order nonlinearity is lowest when differential stages are differentially driven and loaded. Every imbalance in loading or driving impedances increases the second-order nonlinearity and therefore EMI susceptibility. Moreover, suscep-

tibility to EMI increases with frequency up to the upper edge of the bandwidth of the differential stage, after which it decreases again.

Simplified equations are derived for the new differential stage model, from which simple circuit models followed. These can be used in the first stages of design. The circuit models exchange simplicity for accuracy.

Chapters 5 and 6 present a systematic design approach for application specific negative-feedback amplifiers with specified SER. It enables the designer to calculate noise, bandwidth, EMI, the required loop gain poles (LP) product, and the bias current of the transistors used in the amplifier in order to meet the SER requirement.

The type of feedback has a large influence on EMI. Negative-feedback amplifiers with series feedback at the output typically suffer much less from EMI than amplifiers with parallel feedback at the output. If possible, series feedback at the output should thus be favored over parallel feedback at the output.

Both distortion and EMI are determined by the second-order nonlinearity and the LP product of the amplifier. Second-order nonlinearity may be reduced by using current driven (possibly cascoded) BJTs, cascoded FETs and differential stages. A large enough LP product can be assured by proper design or selection of the transistors (high transit frequency, ω_T) and proper biasing of these transistors. Moreover, in the case of a dual-stage negative-feedback amplifier, the output stage should have a large (low-frequency) current amplification factor (α_{20}) for low EMI behavior. A large α_{20} is so beneficial that a device with a high α_{20} should be favored over one with a lower α_{20}, even if the latter device is more linear than the first.

The dependance of EMI on the loop gain and the location of the (dominant) poles of a negative-feedback amplifier is demonstrated by calculations and measurements on a JFET transimpedance amplifier in Chapter 7. The same chapter also presents two systematically designed and realized negative-feedback amplifiers with specified SER.

Firstly, the design of a transimpedance amplifier with a transimpedance of 100 kΩ, a bandwidth of 1 MHz, and a minimal SER of 70 dB (due to both noise and interference) when subjected to (the equivalent disturbance of) a plane wave of 30 V/m has been demonstrated. Measurements were in good agreement with calculations and simulations.

Secondly, a dual-stage transadmittance amplifier has been designed for a biopotential measurement system. It uses cascoded, differential input and output stages for low second-order nonlinearity and high loop gain. The amplifier was designed to have an equivalent EMI voltage source of the same order of magnitude as the equivalent noise voltage (1 μV), while being subjected to an input disturbance voltage of 1V at 127.5 MHz, with a modulation depth of 1. This kind of disturbance may be found in 3 T magnetic resonance imaging systems.

The system met the specifications. An ECG was successfully measured and (despite an unmodelled system resonance increasing EMI susceptibility at about 100 MHz) the measured equivalent EMI voltage was about 0.5 μV at 127.5 MHz. The design may be regarded as a first step towards the development of an MRI

immune bio-potential measurement system.

8.2 Summary of contributions

The contributions made in this thesis are summarized as follows:

1. Development of modified hybrid-π models of the BJT, the MOSFET, the JFET, and the MESFET. The modified hybrid-π models enable small-signal linear and second-order nonlinear (EMI) analysis.

2. Development of modified hybrid-π models of cascoded transistor stages. Analysis of the EMI properties of the BJT-BJT, the FET-BJT, the BJT-FET, and the FET-FET cascode.

3. A new model of the differential stage that enables accurate linear, nonlinear and EMI analysis. The model can also take the effects of component mismatch and unequal biasing into account. A simplified model for EMI analysis and design is also presented.

4. A method to systematically design negative-feedback amplifiers with specified EMI behavior (partially published in [116], [155], [167], and [168]).

5. The design of a BJT-BJT cascode based transimpedance amplifier with a 70 dB signal to error ratio in (the equivalent of) a 30 V/m EM field [155].

6. Development of a (bio-potential) measurement system immune to RF pulses similar to those generated by a 3T MRI. The most important subsystem is formed by a dual-stage negative-feedback amplifier.

Publications resulting from other research: [144] and [169].

8.3 Recommendations

The number of amplifying stages is limited to two in this work. Three amplifying stages may sometimes be necessary too. Therefore, the design of triple-stage negative-feedback amplifiers with specified signal to error ratio (low EMI susceptibility) would be a logical continuation of the research presented here. Although they often tend to be unstable, negative-feedback amplifiers with more than three amplifying stages may also be investigated.

The simplified models of differential (input and output) stages presented in this work (Chapters 4 and 6) are accurate and simple enough for design purposes. More accurate figures of EMI susceptibility in the analysis phase are obtained from the model presented in Appendix D. The latter model is, however, still simplified. A future subject of investigation may be aimed at obtaining a model with less simplification and checking if the increased accuracy is worth the increase in complexity.

This work concentrates on amplifiers using direct, passive, negative feedback. Comparable design strategies as presented in this work can be developed for amplifiers using indirect feedback or active feedback. Developing strategies for designing low EMI susceptible amplifiers using indirect negative feedback is recommended, since indirect negative feedback is often used in low-voltage circuits. Active (common-mode) feedback may, e.g., be found in bio-medical designs (e.g., driven right leg) [161]. When a bio-potential measurement system has to be developed that properly functions both in clinical situations and in an MRI, active feedback may have to be applied (to increase the common-mode rejection ratio at the mains frequency). Therefore, measures for designing low EMI susceptible amplifiers using active feedback should be investigated as well.

Appendix A

Shielding

Conductive enclosures give attenuation of interfering electromagnetic fields (EM fields) by current flow in the enclosure caused by the EM fields themselves, i.e., eddy currents. The induced currents generate EM fields of opposite signs, so the resulting EM fields at the inside of the enclosure are smaller than the incident EM field.

When the behavior of a shield is considered, it follows that conductive planes, cylinders and spheres[1] present different shielding factors for magnetic and electric fields. The shielding factors depend on the wavelength and the distance between the emitter and the shield. Two cases can be identified:

- the distance is smaller than $\frac{\lambda}{2\pi}$ (near field)
- the distance is larger than $\frac{\lambda}{2\pi}$ (far field)

In the first case (near field) the wave impedance of the electromagnetic wave depends on whether the electric field is dominating, i.e., the emitter is a short electric dipole, or the magnetic field is dominating, i.e., the emitter is a short magnetic dipole. With a short electric dipole the wave impedance is $Z_{wE} = Z_w/(k_0 r)$ and in case of a short magnetic dipole $Z_{wH} = Z_w k_0 r$ [41], with $k_0 = 2\pi/\lambda$ being the wave number and r the distance from the emitter to the shield. In the second case (far field) the electromagnetic wave is a plane wave and the wave impedance is $Z_w = \sqrt{\mu_0/\varepsilon_0} = 120\pi\Omega$.

A conductive enclosure provides attenuation of the interfering EM fields by generating eddy currents. These eddy currents and the resulting shielding effect can most easily be determined by considering the magnetic field. In case of electric field coupling in the near field, the electric field can be converted to an equivalent magnetic field using $H_E = E/Z_{wE} = E\omega r/\mu_0$, with ω being the angular frequency of the electric field. H_E is zero when $\omega = 0$ and H_E increases

[1] Although in practice spherical enclosures will seldom be used, the considerations and equations that will be presented for the sphere also give reasonable approximations for other types of enclosures with the same volume [75][82].

with frequency. Hence, high shielding factors for E fields are easily obtained at low frequency because H_E is small.

The magnetic field H induces eddy currents in the shield. The eddy current is directed such that the resulting magnetic field opposes the incident magnetic field. At low frequencies, the skin effect does not occur and the eddy current is homogenous across the cross section of the shield. As a result, a magnetic field is generated at the inside of the enclosure. Shielding of magnetic fields therefore hardly exists at low frequencies. With increasing frequency the 'AC'-resistance and the internal inductance of the shield start to increase and, hence, the eddy currents are not homogenous across the cross section of the enclosure any more. Less current will flow at the inside of the enclosure or shield, and therefore the magnetic field that will be generated at the inside of the shield will become smaller with frequency. For even higher frequencies, the skin effect causes the eddy currents to flow in a thin sheet at the outside of the shield. Virtually no current flows at the inside of the shield and, hence, the shielding factor is large.

When the frequency becomes that high that its wavelength becomes comparable to the dimensions of the enclosure, resonances may start to occur and as a result electromagnetic fields may be generated inside the enclosure, thus hampering the shielding factor.

A.1 Calculating the shielding factor for magnetic fields

The shielding factor for magnetic fields for both $r < \frac{\lambda}{2\pi}$ and $r > \frac{\lambda}{2\pi}$ can be calculated with [75]

$$\begin{aligned} a_s = \frac{H_{ext}}{H_{int}} &= \cosh kd + \frac{1}{a}\left(K + \frac{b}{K}\right)\sinh kd, \\ k &= \frac{1+j}{\delta}, \\ K &= \frac{1}{\mu_r} k r_0, \\ \delta &= \sqrt{\frac{2\rho}{\mu_0 \mu_r \omega}}, \end{aligned} \tag{A.1}$$

with d being the thickness of the shield and r_0 being the radius of the enclosure, or in case of two parallel plates, the distance between those plates. Constants a and b depend of the kind of shield. In case of two infinite parallel plates, $a = 1$ and $b = 0$. For conductive cylinders $a = 2$ and $b = 1$, and for conductive spheres $a = 3$ and $b = 2$ [75]. As follows from equation A.1, a_s is indeed low at low frequencies and increases with frequency.

Simpler engineering approximations of (A.1) are helpful in design. They can be derived for two special cases, for low frequencies and for high frequencies. At low frequencies, the skin depth δ is larger than the material thickness (d); at high frequencies, $\delta < d$. When we use $\cosh(kd) \approx 1$ and $\sinh(kd) \approx kd$ in

case $d < \delta$, and $\cosh(kd) \approx \sinh(kd) \approx 0.5e^{kd}$ in case $d > \delta$ [75], we find the following approximations

$$20\log|a_s| \approx \begin{cases} 20\log\sqrt{1+\left(\frac{d}{a}\frac{2r_0}{\mu_r\delta^2}\right)^2} & d<\delta \quad (\text{'low frequencies'}) \\ 20\log\left(e^{\frac{d}{\delta}}\cdot\left(\frac{r_0}{a\sqrt{2}\mu_r\delta}\right)\right) & d>\delta \quad (\text{'high frequencies'}). \end{cases} \tag{A.2}$$

For very low frequencies, k reduces to zero and only the magneto-static shielding remains. This equals $a_s = 1 + \frac{b}{a}\mu_r\frac{d}{r_0}$ [75][82]. Magneto-static shielding thus requires conductors with a large relative permeability, μ_r, a small enclosure, and thick walls.

When λ becomes comparable to, or smaller than, the dimensions of the shield, resonances may occur. These can be taken into account with an extra term, a_m [75]

$$a_m = \frac{3\sqrt{1+(k_0r_0)^2}|\sin k_0r_0 - k_0r_0\cos k_0r_0|}{(k_0r_0)^3}. \tag{A.3}$$

This equation of a_m is valid for a sphere. Resonances that reduces a_m occur at frequency $f_{rH} = 0.715\frac{c}{r_0}, 1.227\frac{c}{r_0}, \cdots$ [75], with c being the speed of light in vacuum. The total magnetic shielding for an arbitrary frequency is now

$$S_H = 20\log|a_s| + 20\log|a_m| \tag{A.4}$$

Figure A.1 shows, as an example, a plot of S_H (dotted line) for a copper sphere with a radius of 1m and a thickness, d, of 0.1 mm.

Factor $20\log|a_s|$ gives rise to extremely large attenuation values for frequencies higher than 10 MHz in this example. In practice such a large attenuation value is not reached, since the necessary openings for interconnect feed through limit the reachable attenuation. Kaden proposes to use an upper limit of 12 Np, i.e., 104 dB [75], since larger attenuations are hardly verifiable by measurements [82]. This upper limit is used when calculating S_H and S_E in Fig. A.1.

For a cylinder an equation for a_m is given in [75]. This equation is too elaborate to present here. Here, it suffices to state that resonances that hamper the shielding can be expected at $f_{rH} = 0.61\frac{c}{r_0}, 1.117\frac{c}{r_0}, 1.619\frac{c}{r_0}, \cdots$.

A.2 Calculating the shielding factor for electric fields

The electric field shielding can be determined by using the equation for a_s (A.1) and adding a term that describes the electric field shielding at both low frequencies and at high frequencies (resonances). The extra term that describes both for a sphere, a_E, is given by [75]

$$a_E = \frac{3\sqrt{1-(k_0r_0)^2+(k_0r_0)^4}|((k_0r_0)^2-1)\sin k_0r_0 + k_0r_0\cos k_0r_0|}{(k_0r_0)^5}. \tag{A.5}$$

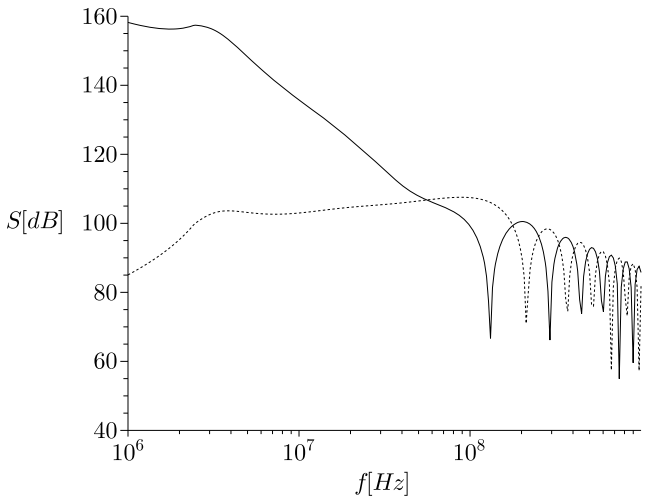


Figure A.1: Shielding factors in dB as a function of frequency for a copper, spherical, enclosure with enclosure wall thickness d= 0.1mm and radius r_0= 1 m. The solid line is S_E and the dotted line is S_H. Note the differences in shielding at both low and high frequencies.

The total electric field shielding for an arbitrary frequency is now

$$S_E = 20 \log |a_s| + 20 \log |a_E|. \tag{A.6}$$

Figure A.1 shows a plot (solid line) of S_E for the same sphere with a radius of 1 m and a thickness of 0.1 mm. Resonances that hamper the shielding for electric fields[2] are found at $f_{rE} = 0.437\frac{c}{r_0}, 0.974\frac{c}{r_0}, 1.483\frac{c}{r_0}, \cdots$ [75].

Kaden [75] also presents equations for a_E for a cylinder. a_E differs for the cases that the H field is parallel with the cylinder, a_{Ep}, and when H is perpendicular to the cross-section of the cylinder, a_{Epp} . These equations are also to elaborate to present here. Again, it suffices to state that resonances that hamper the shielding can be expected at $f_{rEp} = 0.383\frac{c}{r_0}, 0.879\frac{c}{r_0}, 1.377\frac{c}{r_0}, \cdots$ and $f_{rEpp} = 0.293\frac{c}{r_0}, 0.849\frac{c}{r_0}, 1.359\frac{c}{r_0}, \cdots$, respectively.

[2]In case of a cube the first resonance frequency is found at $f_{rE} = 0.866\frac{c}{a}$, with a being the length of the cube [82].

Appendix B

Single stage nullor implementation

Since a single transistor is a three terminal network, not all amplifier configurations are possible with a single stage implementation of the nullor. The only possible configurations are parallel-parallel feedback (transimpedance amplifier), series-series feedback (transadmitance amplifier), unity gain voltage feedback, and unity gain current feedback. The latter two are also called voltage follower and current follower, respectively.

B.1 Some additional design considerations

In case of series-series and parallel-parallel feedback, it may be found that using a single stage representation of the nullor results in a too low loop gain and, hence, more stages have to be used. When unity feedback is applied, the loop gain usually suffices to obtain adequate accuracy of the signal transfer. Often, single stage negative-feedback amplifiers are therefore unity gain amplifiers.

Both as first amplifier in a cascade of negative-feedback amplifiers and as a first stage of a negative-feedback amplifier, a unity gain amplifier has a detrimental effect on the noise behavior. Apart from the noise consideration, applying local negative feedback in a (global) negative-feedback amplifier has (or may have) an adverse effect on the nonlinear behavior. These are usually good reasons to avoid using unity gain feedback amplifiers in global feedback amplifiers.

An exception can be the current follower. When the current follower is used to cascade a common-emitter or common-source stage (i.e., cascode), this results in a nearly unilateral behavior of that stage, thus improving its high-frequency behavior. The nonlinear behavior is determined by the common-emitter or common-source stage, while the contribution of the current follower to the total nonlinearity is negligible compared to the nonlinearity of that common-emitter or common-source stage. In case of a common source stage the adverse effects

of the nonlinear output conductance are eliminated by avoiding the occurrence of a signal voltage across the drain-source terminals.

A current follower realized with a FET, however, also has a nonlinear output conductance. Its influence, and therefore the usability of a FET as current follower, has to be considered in more detail, to verify if its contribution to the nonlinearity is really negligible.

B.2 Common gate stage

The common name for a current follower realized with one FET is the common-gate (CG) stage. Its second-order nonlinear behavior can be analyzed with the superposition model[1] presented in Chapter 5 (page 171) or [116]. The model is shown again in Fig. B.1, for convenience.

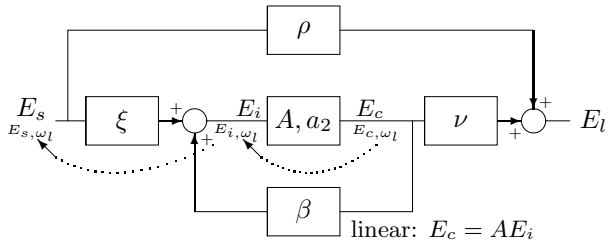


Figure B.1: Superposition model. Dotted lines show the transfers from the demodulated signal to an equivalent signal source at the input.

Applying this model to the CG stage gives as result that the direct transfer from signal source to load, ρ, is exceptionably large. This is due to the fact that $\rho = R_s/(R_s + r_{ds} + R_l)$. Since a CG stage is a current follower, source resistance R_s is expected to have a large value, while load resistance R_l will be (much) lower than r_{ds}. The output resistance of a FET, r_{ds}, may be much lower than R_s also. As a result ρ may already approach one.

It is therefore recommended to calculate the transfers using the equations that follow from the superposition principle and not to use the asymptotic gain model equations. Although the error obtained by using the asymptotic gain model equations for the linear transfer is small, the errors in the second-order nonlinear behavior are significant.

The linear transfer from signal source to load is given by

$$A_t = \rho + \nu\xi\frac{A}{(1 - A\beta)}. \tag{B.1}$$

[1] The superposition model is called asymptotic gain model when $A\beta \to \infty$

The transfer from signal source to the input of the nonlinear controlled source is the familiar equation

$$E_{in} = E_s \frac{\xi}{(1 - A\beta)} = E_s \chi. \tag{B.2}$$

The contribution of the nonlinear output conductance ($g_{ds2} u_{ds}^2$) can be taken in to account by determining the equivalent of u_{ds} in the model shown in Fig. B.1. Voltage u_{ds} equals drain voltage u_d minus source voltage u_s. In the superposition model, u_s equals E_{in} and u_d equals $E_{in} A\nu Z_l + E_s \rho Z_l$, where Z_l is the load impedance. When voltage u_{ds} is translated to superposition model terms, it can be called E_Δ, being the signal across the controlled source. For E_Δ thus follows

$$E_\Delta = E_s \left(Z_l \left(A\chi\nu + \rho \right) - \chi \right). \tag{B.3}$$

It now follows that the second-order nonlinearity component at the output of the controlled source consists of a directly generated term due to a_2, a directly generated term due to b_2 (nonlinearity at the output) and a term at ω_l due to the earlier second-order term that was fed back to the input and amplified again

$$E_{c\omega_l}(\omega_c) = E_{in}(\omega_c)^2 m_2 + E_\Delta(\omega_c)^2 m b_2 + E_{c\omega_l} A\beta_{\omega_l}. \tag{B.4}$$

Here, b_2 equals the second-order nonlinear output conductance g_{ds2}. The other parameters have their usual meaning. Transferring $E_{c\omega_l}$ to an equivalent signal source ($E_{s,eq}$) at the input of the negative-feedback amplifier results in

$$E_{s,eq}(\omega_c) = E_s^2 m \frac{1}{A\xi_{\omega_l}} \left(\chi(\omega_c)^2 a_2 + \left(Z_l \left(A\chi(\omega_c)\nu(\omega_c) + \rho(\omega_c) \right) - \chi(\omega_c) \right)^2 b_2 \right) \tag{B.5}$$

The ω_l component in the load is usually calculated by multiplying $E_{s,eq}(\omega_c)$ with $A_t(\omega_c)$. For the CG this would result in a too pessimistic result. After all, due to the relatively large value of ρ, it dominates A_t while it does not contribute to the nonlinearity.

Because in this work $E_{s,eq}(\omega_c)$ is defined as the equivalent input signal giving the correct value of $E_{l\omega_l}(\omega_c)$ after multiplication with A_t, $E_{s,eq}(\omega_c)$ is rewritten to comply with this definition.

$$\begin{aligned} E_{s,eq}(\omega_c) = & E_s^2 m \frac{1}{A\xi_{\omega_l}} \left(1 - \frac{\rho(\omega_c)}{A_t(\omega_c)} \right) \times \\ & \left(\chi(\omega_c)^2 a_2 + \left(Z_l \left(A\chi(\omega_c)\nu(\omega_c) + \rho(\omega_c) \right) - \chi(\omega_c) \right)^2 b_2 \right) \end{aligned} \tag{B.6}$$

When the FET is biased in the saturation region, b_2 is negative and usually $|b_2|$ is much smaller than a_2. The total second-order nonlinearity term in (B.6) is the $\cdots a_2 + \cdots b_2$ term. In the remainder of the discussion $\cdots a_2$ and $\cdots b_2$ are called the a_2' and b_2' term, respectively, for short.

From equation (B.6) follows that the contribution of b_2' to the total second-order nonlinearity is proportional to load impedance Z_l^n. Exponent n is at least

2, but since a low Z_l tends to lower χ, ν and ρ, n may become larger in some cases and certain frequency ranges.

The total second-order nonlinearity term between the brackets is dominated by the positive value of a_2' for low values of Z_l. For increasing values of Z_l the b_2' term starts to increase in importance. Since b_2' and a_2' have opposite signs, the total second-order nonlinearity term may become zero. When Z_l is increased further, the b_2' term starts to dominate and second-order nonlinear behavior of the CG stage rapidly increases.

The zero value of the second-order nonlinearity term seems interesting, but one should realize that the zero value is only reached in a small frequency band and is subject to parameter spread between FETs, which may be considerable. On top of that, it is found that for those values of the parameters in equation B.6 that result in zero second-order nonlinearity, the inaccuracy of the linear transfer is quite large; about two times as large as in case of low values of Z_l.

When both linear and second-order nonlinear behavior of the CG stage are considered, it is found that the value of the signal source impedance, Z_s, and the load impedance Z_l are of importance. Z_s and Z_l strongly affect the loop gain poles (LP) product. The LP product can be made large by ensuring that $Z_s \gg r_{ds}$ and $r_{ds} \gg Z_l$. When the LP product is large, the second-order nonlinearity term is dominated by the a_2' term since the b_2' term is negligibly small.

In conclusion, the second-order nonlinearity is determined by a_2' when the CG stage is properly designed for a high LP product. The high LP product ensures a low value of χ and therefore $E_{s,eq}$ can reach very low values in this case. $E_{s,eq}$ may even reach values as low as (tens of) nano amperes for reasonable values of E_s.

Appendix C

Derivation of differential stage equations

In this appendix, equations for both linear and second-order nonlinear behavior for EMI analysis at relatively low frequency are derived for the BJT and the FET differential stage. The simplified hybrid-π models of the differential stage presented in Chapter 4 are based on this appendix.

Figure C.1 shows a low-frequency approximation of a FET differential stage. It is driven by two voltage sources (u_{s1} and u_{s2}) with their respective source resistances R_{s1} and R_{s2}. The differential stage is loaded by the resistances R_{l1} and R_{l2}. R_T is the resistance of the current source connected to the source-source node.

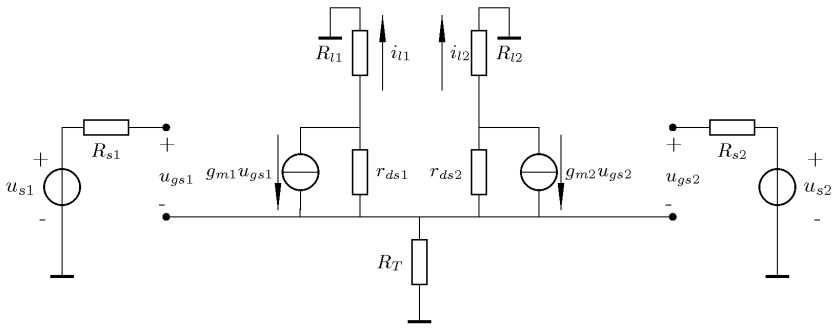


Figure C.1: Low-frequency FET differential stage small signal model.

From Figure C.1 and Equations (4.12) and (4.13) it is found that u_{gs1} and

u_{gs2} are given by

$$\begin{aligned} u_{gs1} =& u_{s1}\frac{1+g_{m2}r_p\left(1+\frac{R_{l1}}{r_{ds1}}\right)}{1+\left(g_{m1}\left(1+\frac{R_{l2}}{r_{ds2}}\right)+g_{m2}\left(1+\frac{R_{l1}}{r_{ds1}}\right)\right)r_p} \\ & - u_{s2}\frac{g_{m2}r_p\left(1+\frac{R_{l1}}{r_{ds1}}\right)}{1+\left(g_{m1}\left(1+\frac{R_{l2}}{r_{ds2}}\right)+g_{m2}\left(1+\frac{R_{l1}}{r_{ds1}}\right)\right)r_p} \end{aligned} \tag{C.1}$$

and

$$\begin{aligned} u_{gs2} =& - u_{s1}\frac{g_{m1}r_p\left(1+\frac{R_{l2}}{r_{ds2}}\right)}{1+\left(g_{m1}\left(1+\frac{R_{l2}}{r_{ds2}}\right)+g_{m2}\left(1+\frac{R_{l1}}{r_{ds1}}\right)\right)r_p} \\ & + u_{s2}\frac{1+g_{m1}r_p\left(1+\frac{R_{l2}}{r_{ds2}}\right)}{1+\left(g_{m1}\left(1+\frac{R_{l2}}{r_{ds2}}\right)+g_{m2}\left(1+\frac{R_{l1}}{r_{ds1}}\right)\right)r_p}, \end{aligned} \tag{C.2}$$

with

$$r_p = \frac{r_{ds1}r_{ds2}R_T}{R_T(r_{ds1}+r_{ds2}+R_{l1}+R_{l2})+(r_{ds1}+R_{l1})(r_{ds2}+R_{l2})}. \tag{C.3}$$

For signal current i_{l1} in the load R_{l1} can be found

$$i_{l1} = -\frac{g_{m1}g_{m2}r_p}{1+\left(g_{m1}\left(1+\frac{R_{l2}}{r_{ds2}}\right)+g_{m2}\left(1+\frac{R_{l1}}{r_{ds1}}\right)\right)r_p}\left[u_{s1}\left(1+\frac{1}{\mu_2'}\right)-u_{s2}\left(1+\frac{1}{\mu_1}\right)\right], \tag{C.4}$$

with $\mu_1 = g_{m1}r_{ds1}$, $r_{ds2}' = \frac{r_{ds2}R_T}{r_{ds2}+R_{l2}+R_T}$, and $\mu_2' = g_{m2}r_{ds2}'$. The voltage across R_{l1} is found by multiplying i_{l1} by R_{l1}.

For i_{l2} follows

$$i_{l2} = \frac{g_{m1}g_{m2}r_p}{1+\left(g_{m1}\left(1+\frac{R_{l2}}{r_{ds2}}\right)+g_{m2}\left(1+\frac{R_{l1}}{r_{ds1}}\right)\right)r_p}\left[u_{s1}\left(1+\frac{1}{\mu_2}\right)-u_{s2}\left(1+\frac{1}{\mu_1'}\right)\right], \tag{C.5}$$

with $\mu_2 = g_{m2}r_{ds2}$, $r_{ds1}' = \frac{r_{ds1}R_T}{r_{ds1}+R_{l1}+R_T}$, and $\mu_1' = g_{m1}r_{ds1}'$. Again, the voltage across R_{l2} is found by multiplying i_{l2} by R_{l2}.

The differential output current ($i_l = i_{l1} - i_{l2}$) and differential output voltage are found to be given by

$$\begin{aligned} i_l =& -\frac{2g_{m1}g_{m2}r_p}{1+\left(g_{m1}\left(1+\frac{R_{l2}}{r_{ds2}}\right)+g_{m2}\left(1+\frac{R_{l1}}{r_{ds1}}\right)\right)r_p} \\ & \left[u_{s1}\left(1+\frac{1}{2g_{m2}\frac{r_{ds2}R_T}{r_{ds2}+R_{l2}+2R_T}}\right)-u_{s2}\left(1+\frac{1}{2g_{m1}\frac{r_{ds1}R_T}{r_{ds1}+R_{l1}+2R_T}}\right)\right] \end{aligned} \tag{C.6}$$

and

$$\begin{aligned} u_l =& -\frac{g_{m1}g_{m2}r_p}{1+\left(g_{m1}\left(1+\frac{R_{l2}}{r_{ds2}}\right)+g_{m2}\left(1+\frac{R_{l1}}{r_{ds1}}\right)\right)r_p} \\ & \left[u_{s1}\left(\left(1+\frac{1}{\mu_2'}\right)R_{l1}+\left(1+\frac{1}{\mu_2}\right)R_{l2}\right)-u_{s2}\left(\left(1+\frac{1}{\mu_1}\right)R_{l1}+\left(1+\frac{1}{\mu_1'}\right)R_{l2}\right)\right]. \end{aligned} \tag{C.7}$$

The detection terms are given by

$$
\begin{aligned}
i_{l1,\omega_l} =& m \left(\frac{g_{m1} g_{m2} r_p}{1 + \left(g_{m1} \left(1 + \frac{R_{l2}}{r_{ds2}} \right) + g_{m2} \left(1 + \frac{R_{l1}}{r_{ds1}} \right) \right) r_p} \right)^3 \times \\
& \left(\left[\left(1 + \frac{R_{l2}}{r_{ds2}} \right) (u_{s2} - u_{s1}) + u_{s2} \frac{1}{g_{m1} r_p} \right]^2 \frac{a_{22}}{g_{m2}^3} \left(1 + \frac{1}{\mu_1} \right) - \right. \\
& \left. \left[\left(1 + \frac{R_{l1}}{r_{ds1}} \right) (u_{s1} - u_{s2}) + u_{s1} \frac{1}{g_{m2} r_p} \right]^2 \frac{a_{12}}{g_{m1}^3} \left(1 + \frac{1}{\mu_2'} \right) \right)
\end{aligned}
\tag{C.8}
$$

and

$$
\begin{aligned}
i_{l2,\omega_l} =& m \left(\frac{g_{m1} g_{m2} r_p}{1 + \left(g_{m1} \left(1 + \frac{R_{l2}}{r_{ds2}} \right) + g_{m2} \left(1 + \frac{R_{l1}}{r_{ds1}} \right) \right) r_p} \right)^3 \times \\
& \left(\left[\left(1 + \frac{R_{l1}}{r_{ds1}} \right) (u_{s1} - u_{s2}) + u_{s1} \frac{1}{g_{m2} r_p} \right]^2 \frac{a_{12}}{g_{m1}^3} \left(1 + \frac{1}{\mu_2} \right) - \right. \\
& \left. \left[\left(1 + \frac{R_{l2}}{r_{ds2}} \right) (u_{s2} - u_{s1}) - u_{s1} \frac{1}{g_{m1} r_p} \right]^2 \frac{a_{22}}{g_{m2}^3} \left(1 + \frac{1}{\mu_1'} \right) \right).
\end{aligned}
\tag{C.9}
$$

Balanced gate-source voltages and low values of i_{l1,ω_l} and i_{l2,ω_l} can be obtained by ensuring that μ_1, μ_2, μ_1', and μ_2' are as equal as possible and that $g_{mx} r_p \gg 1$. This can be accomplished by using matched FETs and assuring that $r_{ds1} \gg R_{l1}$, $r_{ds2} \gg R_{l2}$, and $R_T \gg r_{ds1}, r_{ds2}$. The equations given in Subsection 4.5.2 are simplified, slightly less accurate, equations based on the equations and assumptions presented here.

Figure C.2 shows the low-frequency model of a differential BJT stage. Using

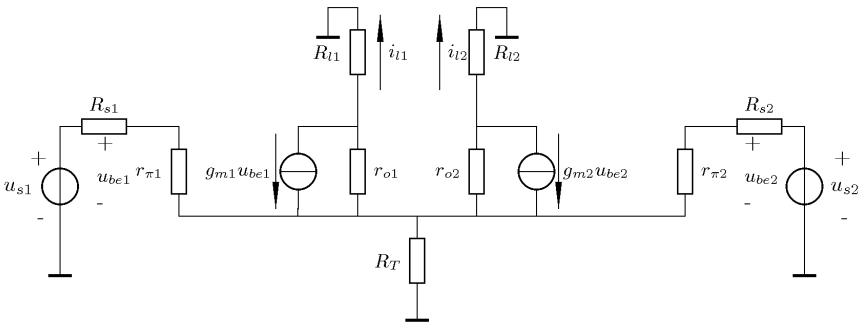


Figure C.2: Low-frequency BJT differential stage small signal model.

this figure and Equations (4.12) and (4.13), it follows for u_{be1} and u_{be2}

$$\begin{aligned} u_{be1} =& \frac{g_{m2} r_p \left(1 + \frac{R_{l1}}{r_{o1}}\right)}{1 + \left(g_{m1}\left(1 + \frac{R_{l2}}{r_{o2}}\right)\left(1 + \frac{R_{s2}}{r_{\pi 2}}\right) + g_{m2}\left(1 + \frac{R_{l1}}{r_{o1}}\right)\left(1 + \frac{R_{s1}}{r_{\pi 1}}\right)\right) r_p} \\ & \left(u_{s1}\left\{1 + \frac{R_{s2} + r_{\pi 2}}{\beta_{ac2} r_{o2}}\left(1 + \frac{r_{o2} + R_{l2}}{r_{o1} + R_{l1}}\left(1 + \frac{r_{o1} + R_{l1}}{R_T}\right) + \frac{r_{o2} + R_{l2}}{R_{s2} + r_{\pi 2}}\right)\right\}\right. \\ & \left. - u_{s2}\left\{1 + \frac{1}{\beta_{ac2}}\left(1 + \frac{R_{l2}}{r_{o2}}\right)\right\}\right) \end{aligned} \tag{C.10}$$

and

$$\begin{aligned} u_{be2} =& \frac{g_{m1} r_p \left(1 + \frac{R_{l2}}{r_{o2}}\right)}{1 + \left(g_{m1}\left(1 + \frac{R_{l2}}{r_{o2}}\right)\left(1 + \frac{R_{s2}}{r_{\pi 2}}\right) + g_{m2}\left(1 + \frac{R_{l1}}{r_{o1}}\right)\left(1 + \frac{R_{s1}}{r_{\pi 1}}\right)\right) r_p} \\ & \left(-u_{s1}\left\{1 + \frac{1}{\beta_{ac1}}\left(1 + \frac{R_{l1}}{r_{o1}}\right)\right\} + \right. \\ & \left. u_{s2}\left\{1 + \frac{R_{s1} + r_{\pi 1}}{\beta_{ac1} r_{o1}}\left(1 + \frac{r_{o1} + R_{l1}}{r_{o2} + R_{l2}}\left(1 + \frac{r_{o2} + R_{l2}}{R_T}\right) + \frac{r_{o2} + R_{l2}}{R_{s1} + r_{\pi 1}}\right)\right\}\right), \end{aligned} \tag{C.11}$$

respectively. With β_{ac1} and β_{ac2} being the current gain of the first (left) and second (right) BJT, respectively, and

$$\begin{aligned} r_p =& \frac{r_{\pi 1} r_{\pi 2} r_{o1} r_{o2} R_T}{w + (R_{l2} + r_{o2})\left[R_T (R_{l1} + r_{o1})(R_{s1} + r_{\pi 1}) + x\right]} \\ x =& (R_{s2} + r_{\pi 2}) \cdot \left[(R_{l1} + r_{o1})(R_{s1} + r_{\pi 1}) + R_T (R_{l1} + r_{o1})(R_{s1} + r_{\pi 1})\right] \\ w =& R_T (R_{l1} + r_{o1})(R_{s1} + r_{\pi 1})(R_{s2} + r_{\pi 2}). \end{aligned} \tag{C.12}$$

For the signal currents i_{l1} and i_{l2} the following equations are found.

$$\begin{aligned} i_{l1} =& \frac{g_{m1} g_{m2} r_p}{1 + \left(g_{m1}\left(1 + \frac{R_{l2}}{r_{o2}}\right)\left(1 + \frac{R_{s2}}{r_{\pi 2}}\right) + g_{m2}\left(1 + \frac{R_{l1}}{r_{o1}}\right)\left(1 + \frac{R_{s1}}{r_{\pi 1}}\right)\right) r_p} \times \\ & \left(-u_{s1}\left\{\frac{1}{1 + \frac{R_p}{R_p + r_{o2} + R_{l2}} \frac{r_{o2} + R_{l2}}{r_{o1} + R_{l1}}}\left[1 + \right.\right.\right. \\ & \left.\left.\frac{R_{s2} + r_{\pi 2}}{\beta_{ac2} r_{o2}}\left(1 + \frac{r_{o2} + R_{l2}}{r_{o1} + R_{l1}}\left(1 + \frac{r_{o1} + R_{l1}}{R_T}\right) + \frac{r_{o2} + R_{l2}}{R_{s2} + r_{\pi 2}}\right)\right] + \right. \\ & \left.\frac{1}{1 + \frac{R_p}{R_p + r_{o1} + R_{l1}} \frac{r_{o1} + R_{l1}}{r_{o2} + R_{l2}}} \frac{R_p}{R_p + r_{o1} + R_{l1}}\left(1 + \frac{1}{\beta_{ac1}}\left(1 + \frac{R_{l1}}{r_{o1}}\right)\right)\right\} + \\ & u_{s2}\left\{\frac{1}{1 + \frac{R_p}{R_p + r_{o2} + R_{l2}} \frac{r_{o2} + R_{l2}}{r_{o1} + R_{l1}}}\left(1 + \frac{1}{\beta_{ac2}}\left(1 + \frac{R_{l2}}{r_{o2}}\right)\right) + \right. \\ & \frac{1}{1 + \frac{R_p}{R_p + r_{o1} + R_{l1}} \frac{r_{o1} + R_{l1}}{r_{o2} + R_{l2}}} \frac{R_p}{R_p + r_{o1} + R_{l1}} \\ & \left.\left. \times \left[1 + \frac{R_{s1} + r_{\pi 1}}{\beta_{ac1} r_{o1}}\left(1 + \frac{r_{o1} + R_{l1}}{r_{o2} + R_{l2}}\left(1 + \frac{r_{o2} + R_{l2}}{R_T}\right) + \frac{r_{o2} + R_{l2}}{R_{s1} + r_{\pi 1}}\right)\right]\right\}\right) \end{aligned} \tag{C.13}$$

and

$$
\begin{aligned}
i_{l2} = & \frac{g_{m1}g_{m2}r_p}{1+\left(g_{m1}\left(1+\frac{R_{l2}}{r_{o2}}\right)\left(1+\frac{R_{s2}}{r_{\pi 2}}\right)+g_{m2}\left(1+\frac{R_{l1}}{r_{o1}}\right)\left(1+\frac{R_{s1}}{r_{\pi 1}}\right)\right)r_p}\times \\
& \left(u_{s1}\left\{\frac{1}{1+\frac{R_p}{R_p+r_{o2}+R_{l2}}\frac{r_{o2}+R_{l2}}{r_{o1}+R_{l1}}}\frac{R_p}{R_p+r_{o2}+R_{l2}}\right.\right. \\
& \times\left[1+\frac{R_{s2}+r_{\pi 2}}{\beta_{ac2}r_{o2}}\left(1+\frac{r_{o2}+R_{l2}}{r_{o1}+R_{l1}}\left(1+\frac{r_{o1}+R_{l1}}{R_T}\right)+\frac{r_{o2}+R_{l2}}{R_{s2}+r_{\pi 2}}\right)\right]+ \\
& \left.\frac{1}{1+\frac{R_p}{R_p+r_{o1}+R_{l1}}\frac{r_{o1}+R_{l1}}{r_{o2}+R_{l2}}}\left(1+\frac{1}{\beta_{ac1}}\left(1+\frac{R_{l1}}{r_{o1}}\right)\right)\right\}- \\
& u_{s2}\left\{\frac{1}{1+\frac{R_p}{R_p+r_{o2}+R_{l2}}\frac{r_{o2}+R_{l2}}{r_{o1}+R_{l1}}}\frac{R_p}{R_p+r_{o2}+R_{l2}}\left(1+\frac{1}{\beta_{ac2}}\left(1+\frac{R_{l2}}{r_{o2}}\right)\right)+\right. \\
& \frac{1}{1+\frac{R_p}{R_p+r_{o1}+R_{l1}}\frac{r_{o1}+R_{l1}}{r_{o2}+R_{l2}}}\left[1+\right. \\
& \left.\left.\left.\frac{R_{s1}+r_{\pi 1}}{\beta_{ac1}r_{o1}}\left(1+\frac{r_{o1}+R_{l1}}{r_{o2}+R_{l2}}\left(1+\frac{r_{o2}+R_{l2}}{R_T}\right)+\frac{r_{o2}+R_{l2}}{R_{s1}+r_{\pi 1}}\right)\right]\right\}\right),
\end{aligned}
\tag{C.14}
$$

with R_p being the resistance formed by $R_T//(R_{s1}+r_{\pi 1})//(R_{s2}+r_{\pi 2})$.

Finally, for $i_{l1\omega_l}$ and $i_{l2\omega_l}$, the following two large equations are found.

$$
\begin{aligned}
i_{l1\omega_l} =& m\left(\frac{g_{m1}r_p\left(1+\frac{R_{l2}}{r_{o2}}\right)g_{m2}r_p\left(1+\frac{R_{l1}}{r_{o1}}\right)}{1+\left(g_{m1}\left(1+\frac{R_{l2}}{r_{o2}}\right)\left(1+\frac{R_{s2}}{r_{\pi 2}}\right)+g_{m2}\left(1+\frac{R_{l1}}{r_{o1}}\right)\left(1+\frac{R_{s1}}{r_{\pi 1}}\right)\right)r_p}\right)^3 \\
&\left(-\left(u_{s1}\left[1+\frac{R_{s2}+r_{\pi 2}}{\beta_{ac2}r_{o2}}\left(1+\frac{r_{o2}+R_{l2}}{r_{o1}+R_{l1}}\left(1+\frac{r_{o1}+R_{l1}}{R_T}\right)+\frac{r_{o2}+R_{l2}}{R_{s2}+r_{\pi 2}}\right)\right]\right.\right. \\
&\left.\left.-u_{s2}\left(1+\frac{1}{\beta_{ac2}}\left(1+\frac{R_{l2}}{r_{o2}}\right)\right)\right)^2\frac{a_{12}}{\left(g_{m1}r_p\left(1+\frac{R_{l2}}{r_{o2}}\right)\right)^3}r_{o1}R_y\times\right. \\
&\left(\frac{r_{o2}+R_{l2}}{r_{o1}+R_{l1}}+\frac{R_p+r_{o2}+R_{l2}}{R_P}+\right. \\
&\frac{1}{g_{m1}r_p\left(1+\frac{R_{l1}}{r_{o1}}\right)}\frac{r_{\pi 2}R_v}{(R_{s1}+r_{\pi 1})(R_v+R_{s2}+r_{\pi 2})+R_v(R_{s2}+r_{\pi 2})}\times \\
&\left.\left\{\frac{r_{o2}}{r_{o1}}+\frac{\beta_{ac1}}{\beta_{ac2}}\frac{R_v+R_{s2}+r_{\pi 2}}{R_v}\frac{R_P+R_{l2}+r_{o2}}{R_P}\right\}\right)+ \\
&\left(-u_{s1}\left(1+\frac{1}{\beta_{ac1}}\left(1+\frac{R_{l1}}{r_{o1}}\right)\right)+\right. \\
&\left.u_{s2}\left[1+\frac{R_{s1}+r_{\pi 1}}{\beta_{ac1}r_{o1}}\left(1+\frac{r_{o1}+R_{l1}}{r_{o2}+R_{l2}}\left(1+\frac{r_{o2}+R_{l2}}{R_T}\right)+\frac{r_{o2}+R_{l2}}{R_{s1}+r_{\pi 1}}\right)\right]\right)^2\times \\
&\frac{a_{22}}{\left(g_{m2}r_p\left(1+\frac{R_{l1}}{r_{o1}}\right)\right)^3}r_{o2}R_y\left(1+\frac{r_{o1}+R_{l1}}{r_{o2}+R_{l2}}\frac{R_P+r_{o2}+R_{l2}}{R_P}+\right. \\
&\frac{r_{\pi 1}R_v}{(R_{s2}+r_{\pi 2})(R_v+R_{s1}+r_{\pi 1})+R_v(R_{s1}+r_{\pi 1})}\frac{1}{g_{m2}r_p\left(1+\frac{R_{l2}}{r_{o2}}\right)}\times \\
&\left.\left.\left\{\frac{r_{o1}}{r_{o2}}\frac{R_P+r_{o2}+R_{l2}}{R_P}+\frac{\beta_{ac2}}{\beta_{ac1}}\frac{R_v+R_{s1}+r_{\pi 1}}{R_v}\right\}\right),
\end{aligned}
\tag{C.15}
$$

with

$$
R_y=\frac{R_P}{(r_{o1}+R_{l1})(R_P+r_{o2}+R_{l2})+R_P(r_{o2}+R_{l2})} \tag{C.16}
$$

and

$$
\begin{aligned}
i_{l2\omega_l} =& m\left(\frac{g_{m1}r_p\left(1+\frac{R_{l2}}{r_{o2}}\right)g_{m2}r_p\left(1+\frac{R_{l1}}{r_{o1}}\right)}{1+\left(g_{m1}\left(1+\frac{R_{l2}}{r_{o2}}\right)\left(1+\frac{R_{s2}}{r_{\pi 2}}\right)+g_{m2}\left(1+\frac{R_{l1}}{r_{o1}}\right)\left(1+\frac{R_{s1}}{r_{\pi 1}}\right)\right)r_p}\right)^3 \\
&\left(\left(u_{s1}\left[1+\frac{R_{s2}+r_{\pi 2}}{\beta_{ac2}r_{o2}}\left(1+\frac{r_{o2}+R_{l2}}{r_{o1}+R_{l1}}\left(1+\frac{r_{o1}+R_{l1}}{R_T}\right)+\frac{r_{o2}+R_{l2}}{R_{s2}+r_{\pi 2}}\right)\right]\right.\right. \\
&\left.\left.-u_{s2}\left(1+\frac{1}{\beta_{ac2}}\left(1+\frac{R_{l2}}{r_{o2}}\right)\right)\right)^2\frac{a_{12}}{\left(g_{m1}r_p\left(1+\frac{R_{l2}}{r_{o2}}\right)\right)^3}r_{o1}R_y\times \right. \\
&\left(1+\frac{r_{o2}+R_{l2}}{r_{o1}+R_{l1}}\frac{R_P+r_{o2}+R_{l2}}{R_P}+\right. \\
&\frac{r_{\pi 2}R_v}{(R_{s1}+r_{\pi 1})(R_v+R_{s2}+r_{\pi 2})+R_v(R_{s2}+r_{\pi 2})}\frac{1}{g_{m1}r_p\left(1+\frac{R_{l1}}{r_{o1}}\right)}\times \\
&\left.\left\{\frac{r_{o2}}{r_{o1}}\frac{R_P+r_{o2}+R_{l2}}{R_P}+\frac{\beta_{ac1}}{\beta_{ac2}}\frac{R_v+R_{s2}+r_{\pi 2}}{R_v}\right\}\right)- \\
&\left(-u_{s1}\left(1+\frac{1}{\beta_{ac1}}\left(1+\frac{R_{l1}}{r_{o1}}\right)\right)\right. \\
&\left.+u_{s2}\left[1+\frac{R_{s1}+r_{\pi 1}}{\beta_{ac1}r_{o1}}\left(1+\frac{r_{o1}+R_{l1}}{r_{o2}+R_{l2}}\left(1+\frac{r_{o2}+R_{l2}}{R_T}\right)+\frac{r_{o2}+R_{l2}}{R_{s1}+r_{\pi 1}}\right)\right]\right)^2\times \\
&\frac{a_{22}}{\left(g_{m2}r_p\left(1+\frac{R_{l1}}{r_{o1}}\right)\right)^3}r_{o2}R_y\left(\frac{r_{o1}+R_{l1}}{r_{o2}+R_{l2}}+\frac{R_p+r_{o2}+R_{l2}}{R_P}+\right. \\
&\frac{1}{g_{m2}r_p\left(1+\frac{R_{l2}}{r_{o2}}\right)}\frac{r_{\pi 1}R_v}{(R_{s2}+r_{\pi 2})(R_v+R_{s1}+r_{\pi 1})+R_v(R_{s1}+r_{\pi 1})} \\
&\left.\left\{\frac{r_{o1}}{r_{o2}}+\frac{\beta_{ac2}}{\beta_{ac1}}\frac{R_v+R_{s1}+r_{\pi 1}}{R_v}\frac{R_P+R_{l2}+r_{o2}}{R_P}\right\}\right),
\end{aligned}
\tag{C.17}
$$

with $R_v = R_T//(r_{o1}+R_{l1})//(r_{o2}+R_{l2})$.

The equations presented here are too elaborate for design purposes. Under the reasonable assumption that $g_{mx}r_p \gg 1$, $\beta_{ac1}, \beta_{ac2} \gg 1$, and $r_{o1}, r_{o2} \gg R_{l1}, R_{l2}$, they reduce to the more manageable, but slightly less accurate, equations in Subsection 4.5.1.

C.1 A note on the CD-CG and the CC-CB stages

The common drain-common gate stage (CD-CG stage) and the common collector-common base stage are often used as 'non-inverting' versions of the common source (CS) and common emitter (CE) stages, respectively. Both CD-CG and CC-CB stage are imbalanced differential stages; the signal source is connected to the CD or CC stage, while the load is connected to the CG or CB stage. In case of a CC-CB stage, now follows from Subsection 4.5.1 for the transconductance from

differential input voltage to load current[1]

$$g_{mt} = \frac{g_{m1}g_{m2}\left(2+\frac{R_{l2}}{r_{o2}}\right)}{g_{m1}\left(1+\frac{R_{l2}}{r_{o2}}\right)+g_{m2}}\frac{r_{o2}}{r_{ot}}\frac{r_{ot}}{r_{ot}+R_{l2}}, \tag{C.18}$$

which reduces to $g_{mt} \approx (g_{m1}g_{m2})/(g_{m1}+g_{m2})$ when $r_{o2} \gg R_{l2}$.

Since both CD-CG and CC-CB stages are (imbalanced) differential stages, the second-order nonlinearity will be lower than that of the CS and CE stage, respectively. The detection component in the output current can be approximated by:

$$i_{l,\omega_l} = -u_d^2 m a_2'(0)\frac{r_{ot}}{r_{ot}+R_{l2}} \tag{C.19}$$

and

$$\begin{aligned} a_2'(0) = &\left(\frac{g_{m2}}{g_{m1}\left(1+\frac{R_{l2}}{r_{ds2}}\right)+g_{m2}}\right)^3\left\{a_{12}-a_{22}\left(\frac{g_{m1}}{g_{m2}}\right)^3\left(1+\frac{R_{l2}}{r_{ds2}}\right)^2\right\}\times \\ &\left(\frac{r_{ds1}}{r_{dst}}+\left(1+\frac{R_{l2}}{r_{ds2}}\right)\frac{r_{ds2}}{r_{dst}}\right), \end{aligned} \tag{C.20}$$

in case of a CD-CG stage, and

$$\begin{aligned} a_2'(0) = &\frac{r_{\pi 1}}{R_s+r_{\pi 1}+r_{\pi 2}}\left(\frac{r_{\pi 1a}}{r_{\pi t}}\right)^2\left\{a_{12}-a_{22}\left(\frac{g_{m1}}{g_{m2}}\right)^3\left(1+\frac{R_{l2}}{r_{o2}}\right)^2\right\}\times \\ &\left(\frac{r_{o1}}{r_{ot}}+\frac{\beta_{ac2}}{\beta_{ac1}}\frac{r_{o2}}{r_{ot}}\right), \end{aligned} \tag{C.21}$$

in case of a CC-CB stage.

The CD-CG stage will be analyzed in more detail in the next subsection. Here, the CC-CB stage is further dealt with.

It can be seen that under current drive, $R_s \gg r_{\pi 1}+r_{\pi 2}$, $a_2'(0)$ approaches zero (even in case of imbalanced transistors and biasing). However, the equations in this section are derived under the assumption that R_T is much larger than R_s, and that the loading of r_{o1} and r_{o2} on the source is negligible. In practice, both R_T and the loading effect of r_{o1} and r_{o2} will limit the linearizing effect of R_s. For $R_s \gg r_{\pi 1}+r_{\pi 2}$, a reasonable under limit of $a_2'(0)$ is given when the value $R_s//R_T//r_{o1}//(r_{o2}+R_l)$ is used for R_s in equation (C.21). This is under the condition that $R_T \gg r_{o1}, r_{o2}$. When the latter condition is violated, equation (C.21) gives too optimistic results.

Under voltage drive conditions, $R_s \ll r_{\pi 1}+r_{\pi 2}$, $a_2'(0)$ can only approach zero when the term between the curly brackets approaches zero. Apart from R_s, $a_2'(0)$ is affected by load resistance R_{l2}. Second-order nonlinearity term $a_2'(0)$ increases for increasing values of R_{l2}. When its value is negligibly low with respect to r_{o2} its effect vanishes. However, equation (C.21) is a simplified

[1]The presented equation is valid for the FETs also; r_{o2} should be replaced by r_{ds2} in that case (see Subsection 4.5.2).

approximation. In case of matching transistors and equal biasing, the following observations about the accuracy can be made.

The inaccuracy of $a_2'(0)$ is small when $R_{l2} \geq r_{o2}/20$, and a higher inaccuracy (order of magnitude is correct) is obtained when $R_{l2} < r_{o2}/20$. For very small values of R_l, e.g., $R_{l2} < r_{o2}/1000$, the inaccuracy increases further and the order of magnitude is not correct anymore. This is caused by approximating the $(1+1/\beta_{acx}(1+R_{lx}/r_{ox}))$ coefficients of u_{s1} and u_{s2} in equations (C.10) and (C.11) with one. Although the coefficients only depart slightly from 1, their influence starts to affect the value of $a_2'(0)$ in case R_l has very low values. The inaccuracy at very low levels of R_{l2} is, however, only of academic interest. In practice the slight unideal matching and inequality of the biasing of the transistors causes causes $a_2'(0)$ to be valid again, even for very low values of R_{l2}, since the unequal values of the hybrid-π parameters are larger than the afore mentioned departure of one of the coefficients of u_{s1} and u_{s2} in equations (C.10) and (C.11).

The second-order nonlinear behavior of both CD-CG and CC-CB stages is frequency dependent. In order to get an impression of the frequency dependency of a_2', $a_2'(\omega_c)$ of the CD-CG stage is investigated next. For the CC-CB stage comparable results are expected.

A. Second-order nonlinearity term $a_2'(\omega_c)$ of a CD-CG stage

Figure C.3 presents a current driven CD-CG stage, which will be analyzed using the equations and models of Section 4.4. When the various transfers are

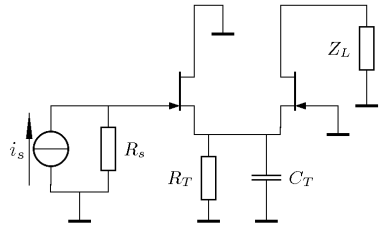


Figure C.3: Large signal model of the CD-CG stage.

determined, we find for (very) low frequencies: $\kappa_{11} = \kappa_{21} = -\frac{r'_{ds1}(r_{ds2}+R_l)}{r'_{ds1}+r_{ds2}+R_l}$, $\kappa_{22} = \kappa_{12} = -\frac{r'_{ds2}(r_{ds1}+R_l)}{r'_{ds2}+r_{ds2}+R_l}$, $\xi_{11} = R_s$, $\xi_{21} = 0$, $\nu_1 = \frac{r'_{ds1}}{r'_{ds1}+r_{ds2}+R_l}$, and $\nu_2 = -\frac{r'_{ds2}}{r_{ds1}+r'_{ds2}+R_l}$, with $r'_{ds1} = r_{ds1}//R_T$ and $r'_{ds2} = r_{ds2}//R_T$. From these equations follows that under the assumption of r_{ds1} and r_{ds2} being much higher than R_l, κ_{11} and κ_{22} are determined by the parallel connection of R_T, r_{ds1} and r_{ds2}, i.e., $r_p = R_T//r_{ds1}//r_{ds2}$.

The various transfers are determined by two poles

$$p_1 \approx -\frac{1}{R_s\left(C_{gs1}+\frac{C_{gd1}(C_{gs2}+C_T)}{C_{gd1}+C_{gs2}+C_T}\right)} \quad \text{and} \tag{C.22}$$

$$p_2 \approx -\frac{1}{r_p\left(C_{gs2}+C_T+\frac{C_{gs1}C_{gd1}}{C_{gs1}+C_{gd1}}\right)}. \tag{C.23}$$

Transfers κ_{11} and κ_{22} have zeros located at

$$z_{k11} = -\frac{1}{R_s C_{gd1}}, \quad z_{k22} = -\frac{1}{R_s(C_{gs1}+C_{gd1})}, \tag{C.24}$$

and for the zeros in ξ_{11} and ξ_{22}, respectively, are found

$$z_{\xi 11} = -\frac{1}{r_p(C_{gs2}+C_T)}, \quad z_{\xi 22} = 0. \tag{C.25}$$

Input voltages u_{gs1} and u_{gs2} can now be determined using equations (4.7) and (4.8). The resulting equations can be simplified further because some poles and zeros will cancel. Also, the $1-(A_1\kappa_{11}(s)+A_2\kappa_{22}(s))$ term in the denominator results in two closed loop poles. The exact location of these poles may be determined using the familiar mathematics. The resulting expressions for the two closed loop poles can be approximated by

$$p_l \approx -\frac{1}{R_s\left(C_{gd1}+\frac{C_{gs1}C_{gs2}}{C_{gs1}+C_{gs2}}\right)} \tag{C.26}$$

and

$$p_h \approx -\left(g_{m1}\frac{C_{gd1}}{C_{gs1}+C_{gd1}}+g_{m2}\right)\frac{C_{gd1}+C_{gs2}+C_T}{\left(\frac{C_{gs1}C_{gd1}}{C_{gs1}+C_{gd1}}+C_{gs2}+C_T\right)^2}. \tag{C.27}$$

Pole p_l represents the pole at the lowest frequency and p_h represents the pole at the highest frequency.

The voltages u_{gs1} and u_{gs2} are thus found to be approximated by:

$$u_{gs1} \approx i_s R_s \frac{1+g_{m2}r_p}{1+(g_{m1}+g_{m2})r_p}\frac{\left(1-\frac{s}{(1+g_{m2}r_p)p_2}\right)}{\left(1-\frac{s}{p_l}\right)\left(1-\frac{s}{p_h}\right)} \tag{C.28}$$

and

$$u_{gs2} \approx -i_s R_s \frac{g_{m1}r_p}{1+(g_{m1}+g_{m2})r_p}\frac{\left(1+s\frac{C_{gs1}}{g_{m1}}\right)}{\left(1-\frac{s}{p_l}\right)\left(1-\frac{s}{p_h}\right)}. \tag{C.29}$$

The expressions for u_{gs1} and u_{gs2} show that in case $g_{mx}r_p \gg 1$ the voltages are determined by $g_{m2}/(g_{m1}+g_{m2})$ and $g_{m1}/(g_{m1}+g_{m2})$, respectively, at low frequencies. For equal biasing and matched devices, the voltages are then, except for the sign, equal. At higher frequencies, at which the effect of the zeros become noticeable, u_{gs1} and u_{gs2} start to differ.

The detection component in the output current can be determined using Equation (4.10). Under the previously mentioned assumption it can be approximated by

$$\begin{aligned} i_{l,\omega_l}(\omega_c) \approx & m\Bigg[u_{gs1}(\omega_c)^2 a_{12}\frac{r'_{ds1}}{r'_{ds1}+r_{ds2}}\frac{(1+2g_{m2}r_p)}{1+(g_{m1}+g_{m2})r_p} \\ & - u_{gs2}(\omega_c)^2 a_{22}\frac{r'_{ds2}}{r_{ds1}+r'_{ds2}}\frac{(1+2g_{m1}r_p)}{1+(g_{m1}+g_{m2})r_p}\Bigg] \approx i_s^2 R_s^2 m\times \\ & \left(\frac{g_{m1}r_p}{1+(g_{m1}+g_{m2})r_p}\right)^3\Bigg[\left(\frac{\left(1-\frac{s}{(1+g_{m2}r_p)p_2}\right)}{\left(1-\frac{s}{p_l}\right)\left(1-\frac{s}{p_h}\right)}\right)^2 a_{12}\frac{g_{m2}r_p(1+g_{m2}r_p)^2}{(g_{m1}r_p)^3} \\ & - \left(\frac{\left(1+s\frac{C_{gs1}}{g_{m1}}\right)}{\left(1-\frac{s}{p_l}\right)\left(1-\frac{s}{p_h}\right)}\right)^2 a_{22}\Bigg]. \end{aligned} \tag{C.30}$$

In case g_{m1} and g_{m2} are approximately equal and when also holds that $R_T \gg r_{ds1}, r_{ds2}$, the second-order nonlinearity for approximating EMI reduces to

$$\begin{aligned} a_2(\omega_c) \approx & \frac{1}{8}\Bigg[\left(\frac{\left(1-\frac{s}{(1+g_{m2}r_p)p_2}\right)}{\left(1-\frac{s}{p_l}\right)\left(1-\frac{s}{p_h}\right)}\right)^2 \frac{g_{m2}}{g_{m1}}\frac{(1+g_{m2}r'_{ds})^2}{(g_{m1}r'_{ds})^2}a_{12} - \\ & \left(\frac{\left(1+s\frac{C_{gs1}}{g_{m1}}\right)}{\left(1-\frac{s}{p_l}\right)\left(1-\frac{s}{p_h}\right)}\right)^2 a_{22}\Bigg], \end{aligned} \tag{C.31}$$

with r'_{ds} being $r_{ds1}//r_{ds2}$. Equation (C.31) shows that $a_2(\omega_c)$ will usually decrease in value at relatively low frequencies due to the effect of p_l. At higher frequencies, it may increase in value because both zeros are typically located at higher frequencies also, e.g., $(1+g_{m2}r_p)p_2$ may be located near p_h and $\frac{C_{gs1}}{g_{m1}}$ may be of the same order of magnitude as the transit frequency, ω_T. The expected effect of these zeros and p_h are (two) points of inflection, with $a_2(\omega_c)$ still getting smaller with increasing frequency.

Note that the (approximate) equations presented in this appendix can be used in the early stages of amplifier design. For more accurate analysis in later stages of the design, a more elaborate model that takes negative feedback into account, e.g., the one presented in Appendix D, should be used.

Appendix D

Differential input and output stage negative-feedback amplifier

This appendix presents a model of a negative-feedback amplifier with both differential input and output stages. The model may be used when increased accuracy in determining $E_{s,\omega l}(\omega_c)$ is needed. It is based on the model of a dual stage negative-feedback amplifier as presented in Chapter 6 and on the simplified model of the differential stage (Fig. 4.7) as presented in Chapter 4. It therefore holds under the same conditions as these models. Figure D.1 shows the model.

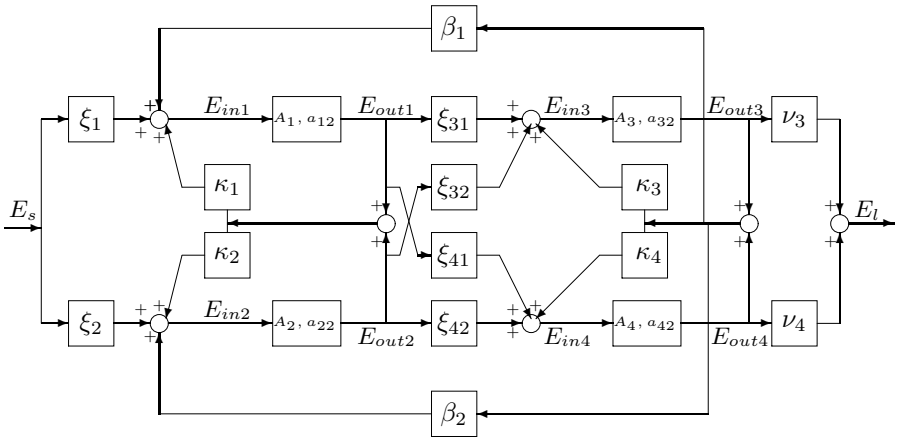


Figure D.1: Simplified model of a negative-feedback amplifier with differential input and differential output stage.

ξ_1 and ξ_2 are the transfers from the signal source to the inputs, u_{be1} and u_{be2} respectively u_{gs1} and u_{gs2}, of the differential input stage. β_1 is the feedback path from the output signal of the differential output stage to the input of first transistor of the input stage. β_2 represents the comparable feedback action to the second transistor of the input stage (Fig. 4.5(a) on page 111 shows which is transistor one and which is transistor two.). Transfers κ_1 and κ_2 represent the feedback action in the differential input stage; κ_3 and κ_4 represent the feedback action in the differential output stage. ξ_{31} and ξ_{32} are the transfers from the output of transistor 1 and transistor 2, respectively, to the input of transistor 3 of the differential output stage. ξ_{41} and ξ_{42} are the transfers from the same transistors to the input of transistor 4 of the differential output stage. ν_3 and ν_4 are the transfers from transistors 3 and 4 to the load signal. All transfers may be determined as described in Chapters 4 and 5. The A_x and a_{xx} terms are the linear and second-order nonlinear transconductances of the transistors.

From Fig. D.1, the frequency dependent linear transfers $\chi_{i1} - \chi_{i4}$ are derived

$$\chi_{i1} = \frac{1}{N}\Big\{\xi_1(1-(A_3\kappa_3+A_4\kappa_4)) + A_2\Big[\kappa_1\xi_2-\kappa_2\xi_1+ A_3[\xi_{32}(\beta_1\xi_2-\beta_2\xi_1)+\kappa_3(\kappa_2\xi_1-\kappa_1\xi_2)] + A_4[\xi_{42}(\beta_1\xi_2-\beta_2\xi_1)+\kappa_4(\kappa_2\xi_1-\kappa_1\xi_2)]\Big]\Big\}, \tag{D.1}$$

$$\chi_{i2} = \frac{1}{N}\Big\{\xi_2(1-(A_3\kappa_3+A_4\kappa_4)) + A_1\Big[\kappa_2\xi_1-\kappa_1\xi_2+ A_3[\xi_{31}(\beta_2\xi_1-\beta_1\xi_2)+\kappa_3(\kappa_1\xi_2-\kappa_2\xi_1)] + A_4[\xi_{41}(\beta_2\xi_1-\beta_1\xi_2)+\kappa_4(\kappa_1\xi_2-\kappa_2\xi_1)]\Big]\Big\}, \tag{D.2}$$

$$\begin{aligned}\chi_{i3} =& \frac{1}{N}\Big\{A_2\xi_2[\xi_{32}+A_4(\xi_{42}\kappa_3-\kappa_4\xi_{32})] \\ &+ A_1\Big[A_2\Big\{A_4\Big(\xi_1[\beta_2(\xi_{41}\xi_{32}-\xi_{42}\xi_{31})+\kappa_2[\kappa_4(\xi_{31}-\xi_{32})+\kappa_3(\xi_{42}-\xi_{41})]] \\ &+ \xi_2[\beta_1(\xi_{42}\xi_{31}-\xi_{41}\xi_{32})+\kappa_1[\kappa_4(\xi_{32}-\xi_{31})+\kappa_3(\xi_{41}-\xi_{42})]]\Big)+ \\ &(\xi_{31}-\xi_{32})(\kappa_1\xi_2-\kappa_2\xi_1)\Big\}+\xi_1[\xi_{31}+A_4(\xi_{41}\kappa_3-\kappa_4\xi_{31})]\Big]\Big\},\end{aligned} \tag{D.3}$$

and

$$\begin{aligned}\chi_{i4} =& \frac{1}{N}\Big\{A_2\xi_2[\xi_{42}+A_3(\xi_{32}\kappa_4-\kappa_3\xi_{42})] \\ &+ A_1\Big[A_2\Big\{A_3\Big(\xi_1[\beta_2(\xi_{42}\xi_{31}-\xi_{41}\xi_{32})+\kappa_2[\kappa_3(\xi_{41}-\xi_{42})+\kappa_4(\xi_{32}-\xi_{31})]] \\ &+ \xi_2[\beta_1(\xi_{41}\xi_{32}-\xi_{42}\xi_{31})+\kappa_1[\kappa_4(\xi_{31}-\xi_{32})+\kappa_3(\xi_{42}-\xi_{41})]]\Big)+ \\ &(\xi_{42}-\xi_{41})(\kappa_2\xi_1-\kappa_1\xi_2)\Big\}+\xi_1[\xi_{41}+A_3(\xi_{31}\kappa_4-\kappa_3\xi_{41})]\Big]\Big\},\end{aligned} \tag{D.4}$$

with

$$\begin{aligned} N =& 1-(A_3\kappa_3+A_4\kappa_4)+A_1[-\kappa_1+A_3(\kappa_1\kappa_3-\beta_1\xi_{31})+A_4(\kappa_1\kappa_4-\beta_1\xi_{41})] \\ &+A_2[-\kappa_2+A_3(\kappa_2\kappa_3-\beta_2\xi_{32})+A_4(\kappa_2\kappa_4-\beta_2\xi_{42})] \\ &+A_1A_2(\beta_1\kappa_2-\beta_2\kappa_1)[A_3(\xi_{31}-\xi_{32})-A_4(\xi_{42}-\xi_{41})]. \end{aligned} \tag{D.5}$$

$E_{i1}-E_{i4}$ can be calculated from $E_s\chi_{i1}-E_s\chi_{i4}$. All transfers, except for the transconductances A_1-A_4 are dependent on ω_c.

The equivalent input signal can be approximated by

$$\begin{aligned} E_{s,\omega_l}(\omega_c) = E_s^2 m\frac{\beta_{1\omega_l}+\beta_{2\omega_l}}{\xi_{1\omega_l}+\xi_{2\omega_l}}\times \\ \left(\chi_{i1}^2(g_{\pi 1a}+a_{12a})+\chi_{i2}^2(g_{\pi 2a}+a_{22a})+\chi_{i3}^2(g_{\pi 3a}+a_{32a})+\chi_{i4}^2(g_{\pi 4a}+a_{42a})\right). \end{aligned} \tag{D.6}$$

The second-order nonlinear terms $g_{\pi xa}$ represent the effects of the nonlinear input impedances of BJTs, calculated to the *output (E_l)*. The effects of the nonlinear transconductances of the active devices, calculated to the *output (E_l)* are depicted by the a_{x2a} terms.

Finally, the a_{x2a} and $g_{\pi xa}$ terms are given by

$$\begin{aligned} a_{12a} = \frac{a_{12}}{N}\Bigg[A_3\Bigg[&-(\xi_{31\omega_l}-A_2\kappa_{2\omega_l}\xi_{3a})\nu_{3\omega_l} \\ &+A_4\left[[\xi_{ao}A_2\beta_{2\omega_l}+\kappa_{4\omega_l}(\xi_{31\omega_l}-A_2\kappa_{2\omega_l}\xi_{3a})-\kappa_{3\omega_l}(\xi_{41\omega_l}-A_2\kappa_{2\omega_l}\xi_{4a})](\nu_{3\omega_l}-\nu_{4\omega_l})\right]\Bigg] \\ &-A_4\left(\xi_{41\omega_l}-A_2\kappa_{2\omega_l}\xi_{4a}\right)\nu_{4\omega_l}\Bigg], \end{aligned} \tag{D.7}$$

with

$$\begin{aligned} \xi_{ao} =& \xi_{42\omega_l}\xi_{31\omega_l}-\xi_{41\omega_l}\xi_{32\omega_l}, \\ \xi_{3a} =& \xi_{31\omega_l}-\xi_{32\omega_l}, \\ \xi_{4a} =& \xi_{41\omega_l}-\xi_{42\omega_l}, \end{aligned} \tag{D.8}$$

and

$$\begin{aligned} N =& -1+A_3\kappa_{3\omega_l}+A_4\kappa_{4\omega_l}+ \\ &A_1\left[\kappa_{1\omega_l}+A_3(\xi_{31\omega_l}\beta_{1\omega_l}-\kappa_{1\omega_l}\kappa_{3\omega_l})+A_4(\xi_{41\omega_l}\beta_{1\omega_l}-\kappa_{1\omega_l}\kappa_{4\omega_l})\right] \\ &+A_2\left[\kappa_{2\omega_l}+A_3(\beta_{2\omega_l}\xi_{32\omega_l}-\kappa_{2\omega_l}\kappa_{3\omega_l})+A_4(\beta_{2\omega_l}\xi_{42\omega_l}-\kappa_{2\omega_l}\kappa_{4\omega_l})\right]+ \\ &+A_1A_2(\kappa_{2\omega_l}\beta_{1\omega_l}-\kappa_{1\omega_l}\beta_{2\omega_l})\left[A_3(\xi_{32\omega_l}-\xi_{31\omega_l})+A_4(\xi_{42\omega_l}-\xi_{41\omega_l})\right], \end{aligned} \tag{D.9}$$

$$\begin{aligned} a_{22a} = \frac{a_{22}}{N}\Bigg[A_3\Bigg[&-(\xi_{32\omega_l}+A_1\kappa_{1\omega_l}\xi_{3a})\nu_{3\omega_l} \\ &+A_4\left[[\xi_{ao}A_1\beta_{1\omega_l}-\kappa_{4\omega_l}(\xi_{32\omega_l}+A_1\kappa_{1\omega_l}\xi_{3a})+\kappa_{3\omega_l}(\xi_{42\omega_l}+A_1\kappa_{1\omega_l}\xi_{4a})](\nu_{4\omega_l}-\nu_{3\omega_l})\right]\Bigg] \\ &-A_4\left(\xi_{42\omega_l}+A_1\kappa_{1\omega_l}\xi_{4a}\right)\nu_{4\omega_l}\Bigg], \end{aligned} \tag{D.10}$$

$$a_{32a} = \frac{a_{32}}{N}\Bigg[[1-(A_1\kappa_{1\omega_l}+A_2\kappa_{2\omega_l})]\,[(A_4\kappa_{4\omega_l}-1)\nu_{3\omega_l}-A_4\kappa_{4\omega_l}\nu_{4\omega_l}]+ A_4\Bigg([(\xi_{41\omega_l}-\xi_{4a}A_2\kappa_{2\omega_l})A_1\beta_{1\omega_l}+(\xi_{42\omega_l}+\xi_{4a}A_1\kappa_{1\omega_l})A_2\beta_{2\omega_l}]\,(\nu_{3\omega_l}-\nu_{4\omega_l})\Bigg)\Bigg], \tag{D.11}$$

$$a_{42a} = \frac{a_{42}}{N}\Bigg[[1-(A_1\kappa_{1\omega_l}+A_2\kappa_{2\omega_l})]\,[(A_3\kappa_{3\omega_l}-1)\nu_{4\omega_l}-A_3\kappa_{3\omega_l}\nu_{3\omega_l}]+ A_3\Bigg([(\xi_{31\omega_l}-\xi_{3a}A_2\kappa_{2\omega_l})A_1\beta_{1\omega_l}+(\xi_{32\omega_l}+\xi_{3a}A_1\kappa_{1\omega_l})A_2\beta_{2\omega_l}]\,(\nu_{4\omega_l}-\nu_{3\omega_l})\Bigg)\Bigg], \tag{D.12}$$

$$\begin{aligned} g_{\pi 1a} =& \frac{g_{\pi 1}}{N}\Bigg[\gamma_{11\omega_l}A_1\Bigg[\xi_{ao}A_2\beta_{2\omega_l}A_3A_4(\nu_{3\omega_l}-\nu_{4\omega_l})+ \\ & A_3(\xi_{31\omega_l}-A_2\kappa_{2\omega_l}\xi_{3a})[A_4\kappa_{4\omega_l}(\nu_{3\omega_l}-\nu_{4\omega_l})-\nu_{3\omega_l}] \\ & -A_4(\xi_{41\omega_l}-A_2\kappa_{2\omega_l}\xi_{4a})[A_3\kappa_{3\omega_l}(\nu_{3\omega_l}-\nu_{4\omega_l})+\nu_{4\omega_l}]\Bigg] \\ & +\gamma_{21\omega_l}A_2\Bigg[\xi_{ao}A_1\beta_{1\omega_l}A_3A_4(\nu_{4\omega_l}-\nu_{3\omega_l})+ \\ & A_3(\xi_{3a}A_1\kappa_{1\omega_l}+\xi_{32\omega_l})\,[A_4\kappa_{4\omega_l}(\nu_{3\omega_l}-\nu_{4\omega_l})-\nu_{3\omega_l}] \\ & -A_4(\xi_{42\omega_l}+\xi_{4a}A_1\kappa_{1\omega_l})[\nu_{4\omega_l}+A_3\kappa_{3\omega_l}(\nu_{3\omega_l}-\nu_{4\omega_l})]\Bigg] \\ & +\gamma_{31\omega_l}A_3\Bigg[A_4(\nu_{4\omega_l}-\nu_{3\omega_l})\times \\ & [(\xi_{4a}A_2\kappa_{2\omega_l}-\xi_{41\omega_l})A_1\beta_{1\omega_l}-(\xi_{4a}A_1\kappa_{1\omega_l}+\xi_{42\omega_l})A_2\beta_{2\omega_l}] \\ & +[1-(A_1\kappa_{1\omega_l}+A_2\kappa_{2\omega_l})][A_4\kappa_{4\omega_l}(\nu_{3\omega_l}-\nu_{4\omega_l})-\nu_{3\omega_l}]\Bigg] \\ & +\gamma_{41\omega_l}A_4\Bigg[A_3(\nu_{3\omega_l}-\nu_{4\omega_l})\times \\ & [(\xi_{3a}A_2\kappa_{2\omega_l}-\xi_{31\omega_l})A_1\beta_{1\omega_l}-(\xi_{3a}A_1\kappa_{1\omega_l}+\xi_{32\omega_l})A_2\beta_{2\omega_l}] \\ & +[1-(A_1\kappa_{1\omega_l}+A_2\kappa_{2\omega_l})][A_3\kappa_{3\omega_l}(\nu_{4\omega_l}-\nu_{3\omega_l})-\nu_{4\omega_l}]\Bigg]\Bigg], \end{aligned} \tag{D.13}$$

$$
\begin{aligned}
g_{\pi 2a} =& \frac{g_{\pi 2}}{N}\Bigg[\gamma_{12\omega_l} A_1\Bigg[\xi_{ao} A_2 \beta_{2\omega_l} A_3 A_4 (\nu_{3\omega_l} - \nu_{4\omega_l}) + \\
& A_3(\xi_{31\omega_l} - A_2\kappa_{2\omega_l}\xi_{3a})[A_4\kappa_{4\omega_l}(\nu_{3\omega_l} - \nu_{4\omega_l}) - \nu_{3\omega_l}] \\
& - A_4(\xi_{41\omega_l} - A_2\kappa_{2\omega_l}\xi_{4a})[A_3\kappa_{3\omega_l}(\nu_{3\omega_l} - \nu_{4\omega_l}) + \nu_{4\omega_l}]\Bigg] \\
& + \gamma_{22\omega_l} A_2\Bigg[\xi_{ao} A_1 \beta_{1\omega_l} A_3 A_4 (\nu_{4\omega_l} - \nu_{3\omega_l}) + \\
& A_3(\xi_{3a} A_1\kappa_{1\omega_l} + \xi_{32\omega_l})\left[A_4\kappa_{4\omega_l}(\nu_{3\omega_l} - \nu_{4\omega_l}) - \nu_{3\omega_l}\right] \\
& - A_4(\xi_{42\omega_l} + \xi_{4a} A_1\kappa_{1\omega_l})[\nu_{4\omega_l} + A_3\kappa_{3\omega_l}(\nu_{3\omega_l} - \nu_{4\omega_l})]\Bigg] \\
& + \gamma_{32\omega_l} A_3\Bigg[A_4(\nu_{4\omega_l} - \nu_{3\omega_l})\times \\
& [(\xi_{4a} A_2\kappa_{2\omega_l} - \xi_{41\omega_l}) A_1\beta_{1\omega_l} - (\xi_{4a} A_1\kappa_{1\omega_l} + \xi_{42\omega_l}) A_2\beta_{2\omega_l}] \\
& + [1 - (A_1\kappa_{1\omega_l} + A_2\kappa_{2\omega_l})][A_4\kappa_{4\omega_l}(\nu_{3\omega_l} - \nu_{4\omega_l}) - \nu_{3\omega_l}]\Bigg] \\
& + \gamma_{42\omega_l} A_4\Bigg[A_3(\nu_{3\omega_l} - \nu_{4\omega_l})\times \\
& [(\xi_{3a} A_2\kappa_{2\omega_l} - \xi_{31\omega_l}) A_1\beta_{1\omega_l} - (\xi_{3a} A_1\kappa_{1\omega_l} + \xi_{32\omega_l}) A_2\beta_{2\omega_l}] \\
& + [1 - (A_1\kappa_{1\omega_l} + A_2\kappa_{2\omega_l})][A_3\kappa_{3\omega_l}(\nu_{4\omega_l} - \nu_{3\omega_l}) - \nu_{4\omega_l}]\Bigg]\Bigg],
\end{aligned}
\tag{D.14}
$$

$$
\begin{aligned}
g_{\pi 3a} =& \frac{g_{\pi 3}}{N}\Bigg[\gamma_{13\omega_l} A_1\Bigg[A_3\Bigg[(\xi_{31\omega_l} - \xi_{3a} A_2\kappa_{2\omega_l})[A_4\kappa_{4\omega_l}(\nu_{3\omega_l} - \nu_{4\omega_l}) - \nu_{3\omega_l}] + \\
& \xi_{ao} A_2\beta_{2\omega_l} A_4(\nu_{3\omega_l} - \nu_{4\omega_l})\Bigg] + A_4(\xi_{4a} A_2\kappa_{2\omega_l} - \xi_{41\omega_l})\times \\
& [A_3\kappa_{3\omega_l}(\nu_{3\omega_l} - \nu_{4\omega_l}) + \nu_{4\omega_l}]\Bigg] + \\
& \gamma_{23\omega_l} A_2\Bigg[A_3\Bigg[(\xi_{32\omega_l} + \xi_{3a} A_1\kappa_{1\omega_l})[A_4\kappa_{4\omega_l}(\nu_{3\omega_l} - \nu_{4\omega_l}) - \nu_{3\omega_l}] + \\
& \xi_{ao} A_1\beta_{1\omega_l} A_4(\nu_{4\omega_l} - \nu_{3\omega_l})\Bigg] + A_4(\xi_{4a} A_1\kappa_{1\omega_l} + \xi_{42\omega_l})\times \\
& [A_3\kappa_{3\omega_l}(\nu_{4\omega_l} - \nu_{3\omega_l}) - \nu_{4\omega_l}]\Bigg] + \\
& \gamma_{33\omega_l} A_3\Bigg[A_4\left[(\xi_{4a} A_2\kappa_{2\omega_l} - \xi_{41\omega_l}) A_1\beta_{1\omega_l} - (\xi_{4a} A_1\kappa_{1\omega_l} + \xi_{42\omega_l}) A_2\beta_{2\omega_l}\right]\times \\
& (\nu_{4\omega_l} - \nu_{3\omega_l}) + \{1 - (A_1\kappa_{1\omega_l} + A_2\kappa_{2\omega_l})\}[A_4\kappa_{4\omega_l}(\nu_{3\omega_l} - \nu_{4\omega_l}) - \nu_{3\omega_l}]\Bigg] + \\
& \gamma_{43\omega_l} A_4\Bigg[A_3\left[(\xi_{3a} A_2\kappa_{2\omega_l} - \xi_{31\omega_l}) A_1\beta_{1\omega_l} - (\xi_{3a} A_1\kappa_{1\omega_l} + \xi_{32\omega_l}) A_2\beta_{2\omega_l}\right]\times \\
& (\nu_{3\omega_l} - \nu_{4\omega_l}) + \{1 - (A_1\kappa_{1\omega_l} + A_2\kappa_{2\omega_l})\}[A_3\kappa_{3\omega_l}(\nu_{4\omega_l} - \nu_{3\omega_l}) - \nu_{4\omega_l}]\Bigg]\Bigg],
\end{aligned}
\tag{D.15}
$$

and

$$
\begin{aligned}
g_{\pi 4a} =& \frac{g_{\pi 4}}{N}\Bigg[\gamma_{14\omega_l} A_1\Bigg[A_3\Bigg[(\xi_{31\omega_l} - \xi_{3a}A_2\kappa_{2\omega_l})[A_4\kappa_{4\omega_l}(\nu_{3\omega_l} - \nu_{4\omega_l}) - \nu_{3\omega_l}]+ \\
& \xi_{ao}A_2\beta_{2\omega_l}A_4(\nu_{3\omega_l} - \nu_{4\omega_l})\Bigg] + A_4(\xi_{4a}A_2\kappa_{2\omega_l} - \xi_{41\omega_l})\times \\
& [A_3\kappa_{3\omega_l}(\nu_{3\omega_l} - \nu_{4\omega_l}) + \nu_{4\omega_l}]\Bigg] \\
& + \gamma_{24\omega_l}A_2\Bigg[A_3\Bigg[(\xi_{32\omega_l} + \xi_{3a}A_1\kappa_{1\omega_l})[A_4\kappa_{4\omega_l}(\nu_{3\omega_l} - \nu_{4\omega_l}) - \nu_{3\omega_l}]+ \\
& \xi_{ao}A_1\beta_{1\omega_l}A_4(\nu_{4\omega_l} - \nu_{3\omega_l})\Bigg] + A_4(\xi_{4a}A_1\kappa_{1\omega_l} + \xi_{42\omega_l})\times \\
& [A_3\kappa_{3\omega_l}(\nu_{4\omega_l} - \nu_{3\omega_l}) - \nu_{4\omega_l}]\Bigg]+ \\
& \gamma_{34\omega_l}A_3\Bigg[A_4\left[(\xi_{4a}A_2\kappa_{2\omega_l} - \xi_{41\omega_l})A_1\beta_{1\omega_l} - (\xi_{4a}A_1\kappa_{1\omega_l} + \xi_{42\omega_l})A_2\beta_{2\omega_l}\right]\times \\
& (\nu_{4\omega_l} - \nu_{3\omega_l}) + \{1 - (A_1\kappa_{1\omega_l} + A_2\kappa_{2\omega_l})\}[A_4\kappa_{4\omega_l}(\nu_{3\omega_l} - \nu_{4\omega_l}) - \nu_{3\omega_l}]\Bigg]+ \\
& \gamma_{44\omega_l}A_4\Bigg[A_3\left[(\xi_{3a}A_2\kappa_{2\omega_l} - \xi_{31\omega_l})A_1\beta_{1\omega_l} - (\xi_{3a}A_1\kappa_{1\omega_l} + \xi_{32\omega_l})A_2\beta_{2\omega_l}\right]\times \\
& (\nu_{3\omega_l} - \nu_{4\omega_l}) + \{1 - (A_1\kappa_{1\omega_l} + A_2\kappa_{2\omega_l})\}[A_3\kappa_{3\omega_l}(\nu_{4\omega_l} - \nu_{3\omega_l}) - \nu_{4\omega_l}]\Bigg]\Bigg].
\end{aligned}
\tag{D.16}
$$

The elaborate equations do not lend themselves very well for design purposes, but may be used during analysis after the first design step is concluded. This has, e.g., been done during the design of the transadmittance amplifier presented in Chapter 7. The lines presenting the equivalent voltage source at the input of the amplifier in Figure 7.16 has been calculated using the model and equations of this appendix.

An even more accurate model may be derived when the differential stages are based on the model presented in Fig. 4.6. This will result in even more elaborate equations, while the obtained extra accuracy may be questionable. This may be the subject of future research.

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List of Abbreviations and Symbols

Abbreviations

AC	Alternating Current
AM	Amplitude Modulation
ASK	Amplitude Shift Keying
BJT	Bipolar Junction Transistor
(W)CDMA	(Wideband) Code Division Multiple Acces
DSB	Double Side Band modulation
(DS)CDMA	(Direct Sequence) Code Division Multiple Access
CLM	Channel Length Modulation
DC	Direct Current
DECT	Digital Enhanced Cordless Telecommunications
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
FDD	Frequency Division Duplex
(O)FDM	(Orthogonal) Frequency Division Multiplexing
FDMA	Frequency Division Multiple Access
FET	Field Effect Transistor
FM	Frequency Modulation
(G)FSK	(Gaussian) Frequency Shift Keying
GSM	Global System for Mobile Communications
IEC	International Electrotechnical Committee
JFET	Junction Field-Effect Transistor
(W)LAN	(Wireless) Local Area Network
MESFET	Metal-Semiconductor Field-Effect Transistor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
(G)MSK	Gaussian Minimum Shift Keying
PCB	Printed Circuit Board
PM	Phase Modulation
PSK	Phase Shift Keying
SER	signal-to-error ratio
SNR	signal-to-noise ratio
SSB	Single Side Band modulation

TIA	Transimpedance amplifier
TDD	Time Division Duplex
TDM	Time Division Multiplexing
TDMA	Time Division Multiple Access
QAM	Quadrature Amplitude Modulation
UMTS	Universal Mobile Telecommunications System
UWB	Ultra Wide Band
VSB	Vestigial Side Band modulation

Symbols

I, i	Current	[A]
U, u	Voltage	[V]
P, p	Power	[W]

Electromagnetic field coupling:

α	attenuation constant of transmission line	[Np/m]
β	phase constant of transmission line	[radians/m]
δ	skin depth	[m]
γ	propagation constant of transmission line $\sqrt{ZY} = \alpha + j\beta$	[-]
λ	wavelength	[m]
σ	conductance	[S]
ρ	resistance	[Ω]
ε_0	permittivity of free space: $8.85 \cdot 10^{-12}$	[C^2/N·m^2]
ε_r	relative permittivity of a medium	[-]
μ_0	permeability of free space: $4\pi \cdot 10^{-7}$	[Tm/A]
μ_r	relative permeability of a medium	[-]
c	Speed of Light	[m/s]
E	Electric Field	[V/m]
H	Magnetic Field	[A/m]
k_0	wave number	[1/m]
Z_w	wave impedance : $\sqrt{\frac{\mu_0}{\varepsilon_0}} = 120 \cdot \pi$	[Ω]
Z_0	characteristic impedance of transmission line $\sqrt{\frac{R+j\omega L}{G+j\omega C}}$	[Ω]
v	phase velocity: $\frac{1}{\sqrt{\mu_0 \mu_r \varepsilon_0 \varepsilon_r}}$	[m/s]
S	Shielding Factor	[-]

Negative-feedback amplifier design and active devices:

α	current gain of an active stage	[-]
α_{20}	low-frequency current gain of the second stage (output stage)	[-]
β	feedback factor	[-] or [Ω]
β_{FET}	FET transconductance factor	[A/V^2]
β_f	Forward Current Amplification Factor	[-]
β_{dc}	'direct current' current gain of the BJT	[-]
β_{ac}	small signal current gain of the BJT	[-]
$\mathcal{E}_n$	normalized truncation error	
λ	channel length modulation factor (first-order characterization)	[-]
χ	transfer from source to input of active device	[-] or [Ω]
χ_{max}	maximal value of χ	[-] or [Ω]
ω_c	(angular) carrier frequency	[rad/s]
ω_k	(angular) frequency at which input stage determines $D_2(\omega_c)$	[rad/s]
ω_l	(angular) frequency of the envelope variation	[rad/s]
ω_{max}	angular frequency at which χ_{max} occurs	[rad/s]
ω_0	amplifier bandwidth	[rad/s]
ω_T	(angular) transit frequency	[rad/s]
ζ	damping factor	[-]
γ	transfer of the second order current from the voltage controlled current source at the input of a BJT to the base-emitter voltage	[Ω]
κ	feedback factor in the differential stage	[-] or [Ω]
ξ	transfer from signal source to the input of a controlled (current) source	[-] or [Ω]
ν	loading factor of amplifier output	[-] or [Ω]
ρ	direct signal transfer from source to load	[-], [Ω], [S]
A_t	Asymptotic Gain	[-], [Ω], [S]
A_1	linear gain (e.g., transconductance) of the first amplifier stage and the first transistor (Q_1, M_1) of the differential stage, respectively	
A_2	linear gain (e.g., transconductance) of the second amplifier stage and the second transistor (Q_2, M_2) of the differential stage, respectively	
a_{12}	second-order nonlinearity of the first amplifier stage and the first transistor (Q_1, M_1) of the differential stage, respectively	[A/V^2]
a_{22}	second-order nonlinearity of the second amplifier stage and the second transistor (Q_2, M_2) of the differential stage, respectively	[A/V^2]

$a'_{21}(0)$	low-frequency second-order nonlinearity factor giving the detection current in the first transistor (Q_1, M_1) of the differential stage	[A/V^2]
$a'_{22}(0)$	low-frequency second-order nonlinearity factor giving the detection current in the second transistor (Q_2, M_2) of the differential stage	[A/V^2]
$a'_2(0)$	low-frequency second-order nonlinearity factor giving the total detection current in the differential stage	[A/V^2]
b_{12}, b_{22}	second-order nonlinearity factor of the input of the BJTs in differential stages and in dual-stage amplifiers	[A/V^2]
C_{je}	junction capacitance between base and emitter	[F]
C_{de}	depletion capacitance between base and emitter	[F]
C_{jc}	junction capacitance between base and collector	[F]
C_{js}	junction capacitance between collector and substrate (npn)	[F]
C_{bs}	junction capacitance between base and substrate (lateral pnp)	[F]
C_{bx}	small-signal capacitance between collector and base terminal	[F]
C_{μ}	small-signal capacitance between collector and r_B	[F]
C_{π}	small-signal capacitance between base and emitter	[F]
$C_{\pi t}$	small-signal input capacitance of the BJT differential stage	[F]
C_{gsov}	overlap capacitance between gate and source	[F]
C_{gdov}	overlap capacitance between gate and drain	[F]
C_{bd}	depletion capacitance between bulk and drain	[F]
C_{gs}	gate-source capacitance	[F]
C_{gst}	small-signal input capacitance of the FET differential stage	[F]
C_{ox}	gate oxide capacitance per unit area	[F]
C_{gd}	gate-drain capacitance	[F]
$CM(s)$, $CM(0)$	the common-mode signal at the input of the differential stage	[V]
D_2	second-order nonlinearity term of a negative-feedback amplifier	[1/V]
E_{in}	signal at the input of an active part	[V] or [A]
E_l	Load signal	[V] or [A]
E_s	Source signal	[V] or [A]
E_{s,ω_l}	equivalent signal source that represents the envelope detection effect	[V] or [A]
$G_{\Delta L}$	channel length modulation factor (higher-order characterization)	[-]
G_{vsat}	velocity saturation factor	[-]
G_{mob}	mobility reduction factor	[-]
$g_{\pi 2}$	Second-order nonlinear input conductance of the BJT	[A/V^2]
g_{ds1}	Linear output conductance of the FET	[S]
g_{ds2}	Second-order nonlinear output conductance of the FET	[S]
g_{m1}	Linear transconductance	[A/V]
g_{mt}	linear transconductance of the differential stage	[A/V]
g_{m2}	Second-order nonlinear transconductance	[A/V^2]
g'_{m2}	Total second-order nonlinear transconductance with linearizing effect of base resistances taken into account	[A/V^2]

g_x	cross conductance ($di_c/(du_{be}dU_{ce})$ and $di_d/(du_{gs}dU_{ds})$ of the BJT and FET	[A/V^2]
$\overline{i_{n,eq}}$	equivalent current noise source at the input of an amplifier	[A]
k	Boltzmann's constant: $1.38{\cdot}10^{-23}$	[J/K]
L	channel length (FET)	[m]
LP product	loop gain poles product	[rad/s]^{1or2}
m	modulation index	[-]
q	Electron charge: $1.60{\cdot}10^{-19}$	[C]
p_i	pole determined by the capacitance of the input stage and the resistances connected to it	[rad/s]
p_o	pole determined by the (transit) frequency of the output stage	[rad/s]
p_l	pole determined by the load capacitance and the resistances connected to it	[rad/s]
r_π	small-signal input resistance of the BJT	[Ω]
$r_{\pi t}$	small-signal input resistance of the BJT differential stage	[Ω]
r_B	semiconductor material resistance of the base	[Ω]
r_{dst}	small-signal output resistance of the FET differential stage	[Ω]
r_o	small-signal output resistance of the BJT	[Ω]
r_{oCa}	output resistance of the cascode stage	[Ω]
r_{ot}	small-signal output resistance of the BJT differential stage	[Ω]
T	Absolute temperature	[K]
$\overline{u_{n,eq}}$	equivalent voltage noise source at the input of an amplifier	[V]
U_{beQmin}	base-emitter voltage corresponding to the lower boundary of the mid-current region	[V]
U_{beQmax}	base-emitter voltage corresponding to the upper boundary of the mid-current region	[V]
$U_{ds,max}$	maximal drain-source voltage for which the simplified FET equations can be used	[V]
U_{dssat}	saturation voltage of the FET	[V]
$U_{gs,max}$	maximal gate-source voltage for which the simplified FET equations can be used	[V]
U_p	JFET pinch-off voltage	[V]
U_t	threshold voltage of the FET	[V]
W	channel width (FET)	[m]

Summary

The information transfer capacity of negative-feedback amplifiers (and electronic circuits in general) is limited by three fundamental limitations being noise, bandwidth, and signal power. Electromagnetic interference (EMI) from other electronic circuits is not a fundamental limitation, but it also hampers the information transfer. EMI may have such detrimental effects that malfunctioning of the electronic circuit occurs. This may result in loss of information, or worse, possibly dangerous situations. That is a reason why susceptibility to EMI is regulated by law.

This work focuses on reducing the errors from the fundamental limitations and EMI in negative-feedback amplifiers, since amplification is such a basic function that it is almost always used in an electronic system. It is assumed that interference is coupled to the input of the negative-feedback amplifier (since this is the most susceptible place in a well-designed amplifier) and generates a disturbance. Errors can be caused by the disturbance from in-band and out-of-band interference.

In-band disturbance can not be distinguished from the intended signal and is processed accordingly. The only way to minimize this kind of error is to reduce the efficiency of the coupling mechanism to the amplifier input. This is usually accomplished by careful design of the interconnects (e.g., small dimensions, shielding) and enclosure(s).

EMI from out-of-band signals, i.e., signals with a frequency (much) higher than the bandwidth of the amplifier, may result in a DC shift and detection of the in-band low frequency envelope variations (envelope or 'AM' detection) of the high frequency interference, caused by even-order nonlinearities in the active devices. The error introduced by the DC shift may be of less importance, specifically when DC is not in the information band of the intended signal. Envelope detection is expected to cause the main problem, since this will often be a signal in the pass band. However, measures to reduce envelope detection will usually be beneficial for reducing DC shifts as well.

Typically, the measures to reduce in-band disturbance are less effective at the (usually) high frequencies of the out-of-band disturbance. An amplifier that does not suffer from in-band disturbance may very well suffer from out-of-band disturbance. This work therefore concentrates on reducing the detrimental effect of out-of-band disturbance, i.e., envelope detection.

The signal-to-error ratio (SER) can be regarded as a figure of merit for the signal handling performance of an amplifier for a given input signal and electromagnetic environment. It is therefore necessary to take the error sources into account (and minimize them) in the design process of the negative-feedback amplifier. This automatically implies that the magnitude of the various error sources must be calculated (or at least estimated).

A systematic design approach for application specific negative-feedback amplifiers with specified SER is proposed in this work. It enables the designer to calculate noise, bandwidth, EMI, the required loop gain poles product, and the bias current of the transistors, respectively, in order to meet the SER requirement. The design starts when the signal source, the load of the amplifier, the electromagnetic (EM) environment, and the required signal-to-error ratio (SER_{req}) are known.

From the signal source and load specifications, the type of negative-feedback amplifier follows. Next, a noise calculation has to be carried out so that the (maximal) signal-to-noise ratio (SNR) can be determined. The SNR has to be larger than the SER_{req}. When this is not the case, it follows that the specified SER_{req} is not realistic since it is not theoretically possible. If possible, the SER_{req} could be reduced so that it is lower than the SNR again. If not, the design process is stopped since it is impossible to meet the specifications.

The allowed error level from out-of-band (and in-band) disturbance follows from the difference of SNR and SER_{req}. This level affects both the design of the interconnect(s) and enclosure(s) and the design of the negative-feedback amplifier.

The design of the interconnect from signal source to the negative-feedback amplifier, the (shielding) enclosure, and the amplifier are orthogonalized. Firstly, the interconnect (+ enclosure) is designed for the allowed out-of-band disturbance, under assumption that the interconnect is loaded by an ideal amplifier. Equations are therefore presented that enable the designer to calculate the maximal dimensions of the (shielded) interconnect. This results in a low disturbance signal. Secondly, the amplifier is designed for low noise and low envelope detection. In principle, the interconnect design is not changed during the design of the amplifier. Both interconnect and the implementation of the amplifier can then be checked for functioning according to specifications by simulation.

The type of negative-feedback amplifier, its expected noise behavior and the amount of disturbance are known at this stage of the design. Next, the feedback network is designed, followed by the design of the active part. Only global feedback should be applied, since the distortion behavior generally worsens when local feedback is applied too.

Envelope detection properties strongly depend on the type of negative-feedback used. Under assumption of a typical load impedance with a capacitive behavior at high frequencies, it is found that series feedback at the output typically results in less susceptible amplifiers than parallel feedback at the output. When the designer has free choice, amplifiers with series feedback at the output (transadmittance and current amplifier) should therefore be favored over amplifiers with

parallel feedback at the output (transimpedance and voltage amplifier).

The type of input stage transistor and its biasing follows from the noise calculation. The output stage is designed for the load requirements. Its bias current should be high enough to drive the load over the entire bandwidth for both the intended amplified signal and the disturbing signal. For both input and output stage hold that the transistors should remain in the active forward region at all times.

At this point, the bandwidth can be determined, which follows from the loop gain poles (LP) product. Measures to optimize the bandwidth will in general positively affect distortion and envelope detection too.

The envelope detection properties of a negative-feedback amplifier depend on the second-order nonlinearity of its active part and the LP product. In fact, it is inversely proportional to the square of the LP product and linearly dependent on the second-order nonlinearity. Designing for low envelope detection properties comes down to ensuring a low second-order *nonlinearity* and high enough *loop gain*. Although harmonic distortion is not the main subject of this work, it should be noted that measures taken for low envelope detection properties are beneficial for second-harmonic (and in some cases third-harmonic) distortion also.

Nonlinear behavior is strongly dependent on the environment of the transistor. Both the bipolar junction transistor (BJT) and the field-effect transistor (FET) are preferably loaded by an impedance much lower than their output impedances. In case of FETs the load impedance is preferably so much smaller than its output impedance that cascoding of the FET is recommended. The BJT is preferably current driven. The larger the impedance of the signal source, the smaller the nonlinearity of the BJT. However, the actual value of the second-order nonlinearity becomes harder to determine and the uncertainty in its value increases with increasing source impedance. This drawback is easily accounted for in the design process of the amplifier.

Since BJTs and FETs often behave rather poorly regarding the accuracy of their transfers, high-frequency behavior and/or nonlinearity, special combinations of active devices are used: the cascode stage and the differential stage. Cascode stages usually show improved high-frequency behavior since the Miller-effect is reduced. Nonlinear behavior of a BJT cascode stage is comparable to the nonlinear behavior of the common-emitter stage. The nonlinear behavior of a FET cascode is, however, improved with respect to the nonlinear behavior of a common-source stage. The cascode effectively cancels the detrimental effect of the nonlinear output resistance of the FET. Using cascode stages in the active part of the negative-feedback amplifier may thus be beneficial for both bandwidth and nonlinear behavior.

Even-order nonlinearity is absent in differential stages and thus second-harmonic distortion and EMI (ideally) do not occur. In reality some even-order, frequency dependent, nonlinearity still remains. Second-order nonlinearity is lowest when differential stages are differentially driven and loaded. Every imbalance due to transistor mismatch, biasing, loading or driving impedances,

increases the second-order nonlinearity and therefore EMI. Second-order nonlinearity can be kept low by ensuring that the impedance of the tail current source (connected to the emitter and source nodes, respectively) is as large as possible. At high frequencies it should still be an order of magnitude larger than the input impedances of the differential stage. It can be expected that the differential stage will then show (much) lower second-order nonlinearity than a single transistor, while it contributes the same to the loop gain as the single transistor. This can be advantageously used in amplifier design.

The minimal value of the *loop gain* poles product that is required for meeting the SER_{req} has to be calculated. Since the amplifier can be expected to show maximal EMI susceptibility at the upper edge of the bandwidth, the minimal value of the LP product is determined at that frequency. The calculations are done under assumption of phantom zero frequency compensation for a maximal flat magnitude (Butterworth) characteristic. The expressions for the LP product and the second-order nonlinearity relate transistor parameters like bias current and current gain to envelope detection behavior. These thus follow straightforwardly from a calculation.

It usually follows that transistors with a high transit frequency and high current gain should be used. Also, a high bias current is usually necessary. It may follow from the calculations that the bias current of (one of) the stages should be increased.

The bias current of the input stage is determined by the noise requirements. Therefore, it is recommended to increase the current of the output stage. Moreover, the output stage should have a large current amplification factor (α_{20}) for low EMI behavior. A large α_{20} is so beneficial, that a device with a high α_{20} should be favored over one with a lower α_{20}, even if the latter device is more linear than the first. When the envelope detection specifications are still just not met, the bias current of the input stage can be increased. The possible detrimental effect on noise (in case of a BJT) should be checked.

In case of a very harsh EM environment, it can be found that an impossibly large LP product is required. Now, a completely differential implementation of the active part can be chosen and/or an input filter can be designed in such a way that noise and stability requirements are not violated.

The final design step is designing the bias network. It should be designed in such a way that it does not negatively affect the LP product, nor may it cause BJT stages to become voltage driven instead of current driven.

Some amplifiers have been built to check the presented method. The dependance of EMI on the loop gain and the location of the dominant poles of a negative-feedback amplifier, is demonstrated by calculations and measurements on a JFET transimpedance amplifier. To demonstrate the design method, two negative-feedback amplifiers with specified SER were designed and realized.

Firstly, the design of a transimpedance amplifier with a transimpedance of 100 kΩ, a bandwidth of 1 MHz, and a minimal SER of 70 dB (due to both noise and interference) when subjected to (the equivalent disturbance of) a plane wave of 30 V/m has been demonstrated. Measurements are in good agreement with

calculations and simulations.

Secondly, a dual-stage transadmittance amplifier has been designed for a bio-potential measurement system. It uses cascoded differential input and output stages for low second-order nonlinearity and high loop gain. The amplifier was designed to have an equivalent EMI voltage source of the same order of magnitude as the equivalent noise voltage (1 μV), while being subjected to an input disturbance voltage of 1V at 127.5 MHz, with a modulation depth of 1. This kind of disturbance may be found in 3 Tesla magnetic resonance imaging system.

The system met the specifications. An ECG was successfully measured and (despite an unmodelled system resonance increasing EMI susceptibility at about 100 MHz) the measured equivalent EMI voltage is about 0.5 μV at 127.5 MHz. The design may be regarded as a first step towards the development of an MRI-immune bio-potential measurement system.

Samenvatting

De informatieverwerkende capaciteit van tegengekoppelde versterkers (en van elektronische schakelingen in het algemeen) wordt beperkt door drie fundamentele grenzen: ruis, bandbreedte en signaalvermogen. Elektromagnetische Interferentie (EMI) veroorzaakt door andere elektronische systemen is dan wel geen fundamentele begrenzing, maar het heeft ook een nadelig effect op de informatieverwerkende capaciteit. EMI kan zelfs tot gevolg hebben dat de elektrische schakeling niet meer goed werkt. Als gevolg hiervan kan er informatie verloren gaan, of er kunnen zelfs gevaarlijke situaties ontstaan. Dit is een reden waarom er wettelijke eisen aan het EMI gedrag van elektronische systemen worden gesteld.

Versterking is een elektronische basisfunctie en wordt daarom in bijna elk elektronisch systeem toegepast. Daarom ligt de focus van dit werk op het verkleinen van de fouten ten gevolge van de fundamentele beperkingen en EMI in tegengekoppelde versterkers. We gaan er vanuit dat elektromagnetische interferentie ingekoppeld wordt op de ingang van de versterker en daar een storend signaal opwekt. De ingang is namelijk de plek waar een goed ontworpen versterker het gevoeligst is voor EMI. De fouten ten gevolge van het storende signaal kunnen worden onderverdeeld in binnen-de-band en buiten-de-band-verstoring.

Het is onmogelijk om binnen-de-band-stoorsignalen te onderscheiden van het gewenste signaal. Het wordt daarom op dezelfde manier verwerkt als dat gewenste signaal. Het verminderen van de effectiviteit van de inkoppeling van stoorsignalen is de enige manier om dit type fout te beperken. De effectiviteit van de inkoppeling is te beperken door de interconnect (verbindingen: draden, sporen e.d.) en de behuizing goed te ontwerpen, door bijvoorbeeld te zorgen voor kleine afmetingen en afscherming.

Buiten-de-band stoorsignalen zijn signalen met een frequentie (veel) hoger dan de bandbreedte van de versterker. Zij veroorzaken fouten zoals verschuivingen van de gelijkstroominstelling (biaspunt) van actieve componenten en detectie van variaties van de omhullende (omhullende- of 'AM'-detectie) van het hoogfrequente stoorsignaal. Dat wordt veroorzaakt door de even orde niet-lineariteit van de actieve componenten. Een fout in het biaspunt maakt vaak niet zoveel uit, vooral niet als gelijkstroom of -spanning niet in de informatieband van het gewenste signaal zit. De fouten ten gevolge van omhullende detectie zijn van groter belang, omdat die zich over het algemeen wel binnen-de-band bevinden. De maatregelen die genomen kunnen worden om omhullende detectie te beperken

zijn echter ook effectief om biaspunt verschuiving te beperken.

Goed ontworpen behuizingen en interconnects zijn niet altijd voldoende om de hoogfrequent buiten-de-band-stoorsignalen genoeg te beperken. Daarom kan het gebeuren dat een versterker niet gevoelig is voor
binnen-de-band-stoorsignalen, maar wel voor buiten-de-band-stoorsignalen. We concentreren ons daarom voornamelijk op het beperken van fouten veroorzaakt door de buiten-de-band-stoorsignalen: omhullende detectie.

De verhouding van het gewenste signaal en de fouten (SER), is een kwaliteitsparameter die aangeeft hoe goed het signaal nog van de fouten te onderscheiden is, bij een gegeven ingangssignaal en elektromagnetische omgeving. De SER dient groter te zijn dan een bepaalde minimale waarde. Tijdens het ontwerp van de versterker moet er voor gezorgd worden dat de fouten een maximum waarde niet overschrijden. Dat betekent natuurlijk automatisch dat de grootte van de fouten berekend moet kunnen worden, exact of benaderd.

In dit proefschrift wordt een systematische ontwerpmethode voor het ontwerpen van tegengekoppelde versterkers met een gespecificeerde SER gepresenteerd. Het stelt de ontwerper in staat om ruis, bandbreedte, EMI gedrag en de benodigde 'loop gain poles product' (LP product) en de instelstroom van de transistoren van de versterker te bepalen, zodat deze aan de SER-eis zal voldoen. Het ontwerp begint met het bepalen van de specificaties van de signaalbron, de belasting, het elektromagnetische (EM) milieu en de vereiste minimale SER: SER_{req}.

Het type tegengekoppelde versterker volgt uit de specificaties van de signaalbron en de belasting. Daarna wordt er een ruisbereking gemaakt, zodat de maximale signaal-ruis verhouding (SNR) bepaald kan worden. De SNR moet groter zijn dan de SER_{req}. Als dit niet het geval is, moet het ontwerpproces of stopgezet worden omdat SER_{req} theoretisch niet mogelijk is, of SER_{req} moet verlaagd worden (indien mogelijk).

De grootte van de toelaatbare fout t.g.v. buiten-de-band (en binnen-de-band) stoorsignalen volgt nu uit het verschil van SNR en SER_{req}. De toelaatbare fout beïnvloedt zowel het ontwerp van de interconnect(s), dat van de behuizing(en) als dat van de tegengekoppelde versterker.

Het ontwerp van de interconnect van de signaalbron naar de versterker, de (afschermende) behuizing en de versterker worden georthogonaliseerd. Eerst worden de interconnect en de behuizing ontworpen en wel zo dat de stoorsignalen het maximaal toelaatbare niet overschrijden. Dit gebeurt onder de aanname dat de interconnect belast wordt met een ideale versterker. Daarna wordt de versterker zo ontworpen dat deze voldoet aan SER_{req} voor de eerder bepaalde maximale waarde van de stoorsignalen aan zijn ingang. In principe wordt de interconnect niet gewijzigd tijdens het ontwerp van de versterker. Wanneer zowel interconnect (en behuizing) als de versterker zijn ontworpen, kan door middel van simulaties en metingen bepaald worden of het geheel aan de specificaties voldoet.

De mate van omhullende detectie hangt sterk af van het type tegenkoppeling dat toegepast wordt. Wanneer we uitgaan van een typische belastingsimpedantie met een capacitief gedrag bij hoge frequenties, dan blijkt dat serie-aankoppeling

aan de uitgang over het algemeen versterkers oplevert die minder gevoelig zijn voor EMI dan versterkers met parallel-aankoppeling aan de uitgang. Als de ontwerper de vrije keus heeft in het bepalen van het type versterker, dan kan hij dus beter kiezen voor een versterker met serie-aankoppeling aan de uitgang (transadmittantie- en stroomversterker) dan voor een versterker met parallel-aankoppeling aan de uitgang (transimpedantie- en spanningsversterker).

Het type tegengekoppelde versterker, zijn verwachtte ruisgedrag en de hoeveelheid storing zijn nu bekend. Nu volgt het ontwerp van het tegenkoppelnetwerk, waarna het actieve deel van de versterker ontworpen wordt. Hierbij geldt dat alleen globale tegenkoppeling toegepast dient te worden. Als ook lokale tegenkoppeling toegepast wordt, zal namelijk over het algemeen het vervormingsgedrag van de versterker verslechteren.

Het type transistor van de ingangstrap en zijn biasing volgt uit een ruisberekening. De uitgangstransistor, ongeacht het type, moet zo ingesteld worden dat hij voor frequenties over de hele bandbreedte in staat is om voldoende stroom aan de belastingsimpedantie te leveren, zowel voor het gewenste ingangssignaal als voor het stoorsignaal. Bovendien geldt voor zowel de ingangs- als de uitgangstrap dat beiden onder deze omstandigheden in de zogenaamde 'forward active region' blijven.

Nu is het punt bereikt dat uit het LP-product de bandbreedte bepaald kan worden. De methodes om de bandbreedte te optimaliseren (frequentiecompensatie) zullen over het algemeen ook een positief effect hebben op de vervorming en de omhullende detectie.

De mate van omhullende detectie die in een versterker optreedt, hangt af van de tweede orde niet-lineariteit van het actieve deel en van het LP-product. De detectie is namelijk omgekeerd evenredig met het kwadraat van het LP-product en evenredig met de tweede orde niet-lineariteit. Ontwerpen voor weinig omhullende detectie komt dus neer op het zorgen voor een lage tweede orde *niet-lineariteit* en voldoende *loop gain*. Harmonische vervorming wordt in dit proefschrift niet uitvoerig behandeld, maar merk op dat de maatregelen die getroffen worden om omhullende detectie te beperken, ook tweede harmonische vervorming (en in bepaalde gevallen derde harmonische vervorming) beperken.

Het *niet-lineaire* gedrag van een transistor wordt sterk bepaald door zijn omgeving. Zowel de bipolaire junctie transistor (BJT) als de veldeffecttransistor (FET) worden bijvoorkeur door een impedantie veel lager dan hun uitgangsimpedantie belast (current load). In het geval van de FET is de aanbevolen belastingsimpedantie over het algemeen zo laag dat deze bij voorkeur gecascodeerd wordt. De BJT wordt bij voorkeur in het stroomdomein aangestuurd. Hoe hoger de impedantie van de signaalbron, hoe lager de niet-linariteit van de BJT. De exacte waarde van de tweede orde niet-lineariteit wordt moeilijker te bepalen met toeneemde bronimpedantie, omdat de onzekerheid in die waarde ook toeneemt. Hiermee blijkt echter makkelijk rekening gehouden te kunnen worden tijdens het ontwerp.

BJTs en FETs vertonen vaak een matige nauwkeurigheid in hun overdracht, hoogfrequent gedrag en/of een matige tweede orde niet-lineariteit. Dit maakt het

ontwerp van de versterker moeilijker. Daarom worden vaak speciale combinaties van transistoren, de cascode trap en de differentieeltrap, gebruikt.

Cascode trappen hebben een verbeterd hoogfrequent gedrag omdat het Miller -effect wordt beperkt. BJT cascodes vertonen een zelfde niet-lineariteit als de gemeenschappelijke emitter schakeling. Het niet-lineaire gedrag van een FET-cascode is beter dan die van een FET in gemeenschappelijke source schakeling. De cascode neutraliseert het nadelige effect van de niet-lineaire uitgangsweerstand van de FET. Het is dus goed voor de bandbreedte en het niet-lineaire gedrag van de versterker om cascode trappen in het actieve deel toe te passen.

In het ideale geval treedt er geen even orde niet-lineariteit op in differentieeltrappen. Tweede harmonische vervorming en omhullende detectie zullen dus niet optreden. Ten gevolge van ongelijkheden tussen de gebruikte transistoren, verschillen in hun biasing en verschillen in belasting- en stuurimpedanties, zal er toch een, frequentie afhankelijke, tweede orde niet-lineariteit optreden.

De tweede orde niet-lineariteit is minimaal wanneer de differentieeltrap differentieel aangestuurd en belast wordt. Elke onbalans in de biasing, de stuur- of belastingsimpedanties vergroot de tweede orde niet-lineariteit en daardoor de omhullende detectie. De tweede orde niet-lineariteit kan klein gehouden worden door er voor te zorgen dat de uitgangsimpedantie van de stroombron, die aan het emitter of source knooppunt aangesloten is, zo groot mogelijk te houden. Ook bij hoge frequenties moet die impedantie nog steeds een orde van grootte groter zijn dan de ingangsimpedantie van de differentieeltrap. In dat geval zal de differentieeltrap een (veel) kleinere tweede orde niet-lineariteit bezitten dan een enkelvoudige transistor, terwijl het evenveel bijdraagt aan de lusversterking. Hier kan goed gebruik van gemaakt worden bij het versterkerontwerp.

Het minimale *loop gain* poles product dat nodig is om aan de SER_{req} te voldoen moet berekend worden. Omdat verwacht kan worden dat maximale gevoeligheid voor EMI zal optreden bij het hoog kantelpunt van de bandbreedte, moet de minimale waarde van het LP-product bij die frequentie berekend worden. De berekeningen worden gedaan onder aanname van 'phantom zero frequency compensation' voor een maximaal vlakke magnitude (Butterworth) karakteristiek. De formules voor het LP-product en de tweede orde niet-lineariteit relateren transistor parameters zoals de instelstroom en de stroomversterking aan de omhullende detectie. De benodigde waarden van beiden kunnen dus simpelweg berekend worden. Doorgaans volgt uit de berekeningen dat transistoren met een hoge 'transit frequency' en een hoge stroomversterking gebruikt moeten worden. Een relatief hoge instelstroom blijkt geregeld nodig te zijn. Het zou kunnen dat uit de berekeningen volgt dat de instelstroom van (een van de) versterkertrappen verhoogd moet worden.

De instelstroom van de ingangstrap volgt uit de ruisberekeningen. Daarom wordt aangeraden om de stroom van de uitgangstrap te verhogen. De uitgangstrap dient bovendien een hoge (laagfrequent) stroomversterkingsfactor (α_{20}) te bezitten voor een laag detectiegedrag. Een grote α_{20} is zo voordelig, dat men beter een transistor met een hoge α_{20} kan toepassen dan een met een lage α_{20}, zelfs als die minder niet-lineair is.

Wanneer na het vergroten van de uitgangsstroom de omhullende detectie nog steeds iets te groot is, kan men de instelstroom van de ingangstransistor vergroten. In geval van een BJT ingangstrap kan dit het ruisgedrag verslechteren. Het moet dus gecontroleerd worden in hoeverre verhogen van de stroom toegestaan is. Het heeft immers geen zin om de omhullende detectie te verlagen met als gevolg dat de ruis zoveel toeneemt dat niet meer aan SER_{req} voldaan wordt.

In het geval van zeer sterke storende elektromagnetische velden kan uit de berekeningen volgen dat een onpraktisch of onmogelijk hoog LP-product nodig is. Er kan dan een volledig differentiële implementatie van het actieve deel en/of een laagdoorlaatfilter aan de ingang van de versterker ontworpen worden. Door het voorafgaande ontwerpwerk aan de versterker, kan het filter aan de ingang nu zo ontworpen worden dat het ruisgedrag en de stabiliteit van de versterker niet (te) nadelig beinvloed worden.

De laatste ontwerpstap is het ontwerpen van het bias netwerk. Dat moet zo ontworpen worden dat het LP-product niet nadelig beïnvloed wordt. Tevens mag het bias netwerk niet tot gevolg hebben dat BJT trappen spanningsgestuurd worden in plaats van stroomgestuurd.

Om de in dit proefschrift gepresenteerde methode te testen, is een drietal versterkers gebouwd. Dat het detectiegedrag afhangt van de lusversterking en de dominante polen, wordt gedemonstreerd door middel van berekeningen en metingen aan een transimpedantieversterker met een JFET als actief component. Daarnaast zijn twee versterkers met een gespecificeerde SER ontworpen en gebouwd.

De eerste versterker is een transimpedantieversterker met een transimpedantie van 100 kΩ, een bandbreedte van 1 MHz, en een minimale SER t.g.v. ruis en omhullende detectie van 70 dB. Het storende signaal aan de ingang van de versterker komt overeen met een elektromagnetisch veld (vlakke golf) van 30 V/m dat op de ingang instraalt. De metingen en de berekeningen komen goed overeen.

De tweede versterker is een tweetraps transadmittantieversterker, die ontworpen is voor een systeem om bio-potentialen te meten. Het actieve deel bestaat uit differentiële, gecascodeerde, ingangs- en uitgangstrappen voor een lage tweede orde niet-lineariteit en een hoge lusversterking. De versterker is zo ontworpen dat een equivalente 'detectie spanningsbron' aan de ingang dezelfde orde van grootte heeft als de equivalente ruisbron (1 μV), wanneer er buiten-de-band stoorsignalen van 1V op 127,5 MHz met een modulatiediepte van 1 aanwezig zijn. Dit soort stoorsignalen kunnen in een 3 Tesla MRI-systeem aangetroffen worden.

Het systeem voldoet aan de specificaties. Er kon succesvol een ECG mee gemeten worden en (ondanks dat een niet-gemodelleerde resonantie in het systeem de EMI gevoeligheid rond de 100 MHz vergrootte) de gemeten equivalente 'detectie spanningsbron' was ongeveer 0.5 μV op 127,5 MHz. Dit systeem mag beschouwd worden als een eerste stap in de richting van de ontwikkeling van een MRI-compatibel systeem om bio-potentialen te meten.

Acknowledgements

When I was working as a designer of (analog) electronics for bio-medical instrumentation at the Academic Medical Center, I discovered that amplifiers may behave as AM radios when subjected to electromagnetic interference (EMI). I wanted to understand this phenomenon and also learn how to design negative-feedback amplifiers that suffer from AM detection much less than the amplifiers I designed at that time. Therefore, I contacted the specialists from the micro-electronics department of Delft University of Technology. However, it appeared that a design methodology for EMI resilient (special purpose) negative-feedback amplifiers did not exist. So, there was an opportunity to develop such a design methodology and I decided to try to do that.

Although the exact date on which I started my research is not very clear to me anymore, I guess that I spent about 10 years doing research in my free time, outside my day job. The first few years I did this without being connected to a technical university, but in 2004 I became a part-time PhD student at the micro-electronics department of Delft University of Technology. Such an endeavor takes a big toll on your (social) life and perhaps on your health, since there is a large imbalance in intellectual exertion and relaxation. Especially the last couple of years were stressful. Therefore, I am glad that this PhD adventure will finally be completed after defending my thesis; I now know what I wanted to know.

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M.J. van der Horst
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Biography

Marcel Johan van der Horst was born in Amsterdam, the Netherlands, on January 4^{th}, 1970. He received the ing. (bachelor's) degree in electrical engineering from (the predecessor of) the Hogeschool van Amsterdam in 1992. After that, he completed postgraduate courses on electromagnetic compatibility and systematic design of analog circuits. Combining study, research, and work, he started a part-time Ph.D. program at the Electronics Research Laboratory of Delft University of Technology, resulting in this thesis.

From 1995 up to September 2008 he was employed as designer of biomedical instrumentation by the Academic Medical Center in Amsterdam, the Netherlands. Since September 2008 he is working as a lecturer at the Hogeschool van Amsterdam.