Interface Electronics for a CMOS Electrothermal Frequency-Locked-Loop

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***Abstract*—This paper describes a new implementation of a CMOS electrothermal frequency-locked-loop (FLL), whose output frequency is determined by the temperature-dependent phase shift of an electrothermal filter (ETF). The FLL maintains a constant phase shift in the ETF, and as a result drives it with a signal whose frequency is a well-defined function of temperature. Compared to a previous implementation, the FLL described here has significantly more loop gain, less electrical phase-spread, and is more suitable for full integration. Measurements on 16 samples (from one batch) show that the temperature dependence of the FLL's output frequency agrees very well with the known thermal properties of bulk silicon. The untrimmed spread of this frequency is less than $\pm 0.45\%$ (3σ) from -40°C to 100°C, which corresponds to a temperature-sensing inaccuracy of less than $\pm 0.7\,^{\circ}$C (3σ).**

***Index Terms*—Electrothermal filter, frequency-locked-loop, synchronous demodulator, temperature sensor.**

I. Introduction

TODAY, most integrated temperature sensors are based on the temperature dependence of the base-emitter voltage of a bipolar transistor [1]–[4]. This dependence is affected by process spread, which limits the inaccuracy of such sensors to about $\pm 2\,^{\circ}$C. By calibrating and trimming individual sensors, their inaccuracy can be reduced to less than $\pm 0.1\,^{\circ}$C (3σ) over the military temperature range [4]. However, this is at the expense of increased manufacturing costs.

An alternative way of realizing an integrated temperature sensor is by measuring the temperature-dependent thermal diffusivity of bulk silicon [5]–[7]. This can be done by measuring the temperature-dependent phase shift of an electrothermal filter (ETF), which consists of a heater and a temperature sensor implemented in close proximity in the substrate of a chip. Due to the finite rate at which heat diffuses through the substrate, the output of the temperature sensor will be delayed with respect to the electrical power dissipated in the heater. This delay is determined by the temperature-dependent thermal diffusivity of the substrate, and by the filter's geometry. The former is essentially process independent [8], [9], while variations in the latter are caused by lithographic inaccuracy and can be mitigated by making the filter's dimensions sufficiently large. Therefore, the delay of an ETF can be used as the basis for an accurate temperature sensor: untrimmed inaccuracies of between $0.5\,^{\circ}$C and $0.7\,^{\circ}$C (3σ) have been achieved over the industrial temperature range ($-40\,^{\circ}$C to $105\,^{\circ}$C) [7], [9], [10].

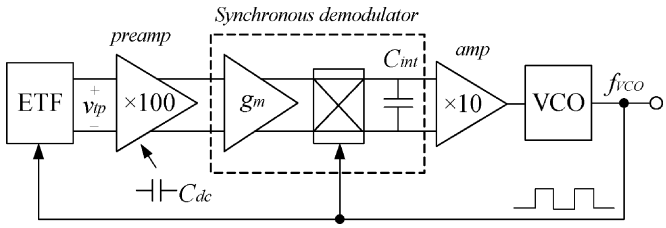

Fig. 1. Block diagram of an electrothermal FLL [7].

In [7], a temperature-to-frequency converter was realized by incorporating an ETF in a frequency-locked loop (FLL). This maintains a constant phase shift in the ETF, and therefore, drives it at a temperature-dependent frequency. As shown in Fig. 1, the FLL consists of an ETF, a preamplifier, a synchronous demodulator (transconductance g_m, chopper and integrating capacitor $C_{\rm int}$) and a voltage-controlled oscillator (VCO). The VCO drives the ETF with a square-wave, and its phase-shifted output is first amplified and then synchronously demodulated. The output of the demodulator is then amplified again and used to tune the VCO. Due to the integrating action of $C_{\rm int}$, the VCO's frequency $f_{\rm VCO}$ will stabilize when the chopper's DC output is zero, which corresponds to a phase shift of 90° in the ETF.

In [7], however, some critical analog components of the FLL were realized off-chip, such as the VCO, the instrumentation amplifier and two capacitors. This paper presents an improved FLL architecture that does not require off-chip capacitors, and thus can be fully integrated.

In the next section, the operating principles of electrothermal FLLs are described in more detail. Then in Section III, the design of the improved architecture is discussed. This is followed, in Section IV, by a description of its circuit-level implementation. The measurement results are presented and discussed in Section V. Finally, the paper ends with an outlook and some conclusions.

II. Operating Principles of Electrothermal FLLs

The heart of an electrothermal FLL is an electrothermal filter (ETF). The ETF used here (Fig. 2) is essentially the same as that described in [7]: the distance $s = 20\ \mu$m, the heater is an n^+-diffusion resistor with a nominal resistance of $1\ \mathrm{k}\Omega$, and the temperature sensor is a thermopile that consists

Manuscript received November 16, 2007; revised February 18, 2008.

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Digital Object Identifier 10.1109/JSSC.2008.922405

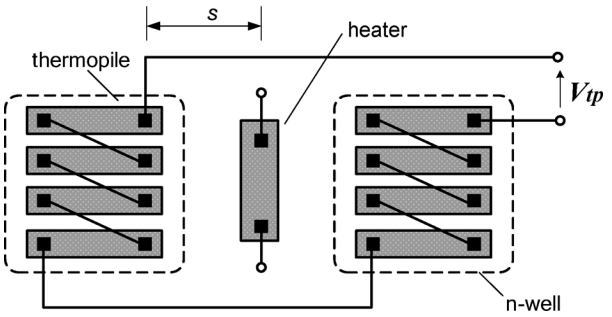

Fig. 2. Schematic layout of an electrothermal filter.

of 20 Al/p$^+$-diffusion thermocouples and has an estimated sensitivity of 10 mV/K.

The filter's phase shift ϕ can be expressed as

$$\phi \propto \sqrt{\frac{\omega}{2D}} \tag{1}$$

where ω is the frequency of the heater's output power, and D is the temperature-dependent thermal diffusivity of the substrate. When incorporated in an electrothermal FLL, the ETF's phase shift will be fixed at 90°, and so from (1), the VCO's frequency $f_{\rm VCO}$ will be proportional to D.

Over the industrial range, the temperature dependence of D can be approximated by a power-law function of absolute temperature, i.e., $D = T^{-n}$, where T is the absolute temperature and $n \sim 1.8$ over the industrial temperature range [6], [7], [11]. As a result, $f_{\rm VCO}$ can be expressed as

$$f_{\rm VCO} \propto \frac{1}{T^n}. \tag{2}$$

Therefore, $f_{\rm VCO}$ is a function of absolute temperature, which, for this ETF, will vary from about 70 kHz to 170 kHz over the industrial temperature range [7].

III. Interface Electronics: Design Considerations

Since silicon is a good thermal conductor, the amplitude of the thermopile's output signal is quite small: having an amplitude of only about 1 mV at a heater power dissipation of 10 mW [7]. The thermopile also generates thermal noise, and so the FLL's bandwidth must be minimized in order to maximize its temperature-sensing resolution.

Noting that a synchronous demodulator (Fig. 1) behaves like a narrowband filter centered on $f_{\rm VCO}$, the FLL's noise bandwidth BW may be expressed as

$$\mathrm{BW} \propto \frac{g_{m,\rm eq}}{C_{\rm int}} \tag{3}$$

where $C_{\rm int}$ is the integrating capacitor and $g_{m,\rm eq}$ is the equivalent transconductance of the front-end, i.e., the combination of the preamplifier and the transconductor shown in Fig. 1.

In [7], a 1 μF off-chip integrating capacitor was used to obtain a temperature sensing resolution of 0.04 °C in a 0.5 Hz noise bandwidth. In order to achieve the same bandwidth with a smaller, on-chip, capacitor, $g_{m,\rm eq}$ will have to be drastically reduced. This can be done by eliminating the preamplifier and appropriately dimensioning the transconductor. It also has the added advantage of eliminating the other external capacitor $C_{\rm dc}$, which was also part of the preamplifier [7]. But eliminating the preamplifier also means that the chopper's DC output becomes smaller, making the loop more sensitive to any offset introduced after the chopper. However, such offset can be reduced by chopping the entire front-end [7].

The front-end should also ensure that the FLL's output frequency is determined solely by the ETF's phase shift. This means that the transconductor's bandwidth should be large enough to ensure that its process-dependent phase shift is much smaller than the 90° phase shift in the ETF. Substituting the power law approximation for D in (1) and differentiating, we obtain

$$\frac{d\phi}{\phi} = \frac{n}{2}\frac{dT}{T}. \tag{4}$$

So for a worst-case temperature error of ±0.5 °C over the industrial temperature range (−40 °C to 105 °C), the transconductor's phase spread should be less than 0.2°.

Finally, the FLL's loop gain should be large enough to ensure that process-dependent variations are not a significant source of error. Based on the results of [7], this means that the gain of the front-end should be greater than some 130 dB.

IV. Implementation of Interface Electronics

A block diagram of the new FLL architecture is shown in Fig. 3. It is functionally equivalent to the Fig. 1 architecture. The main differences are that the preamp has been eliminated, and that the passive integrator has been replaced by an opamp integrator. The elimination of the preamp simplifies the front-end, reducing its power dissipation and lowering its electrical phase shift. The use of the opamp integrator significantly boosts the on-chip loop gain, and so no external gain is required. The integrator is buffered by two source followers, each biased at a 50 μA quiescent current.

As shown in Fig. 4, the input transconductor is a telescopic operational transconductance amplifier (OTA), whose bandwidth was maximized by minimizing the parasitic capacitances at its output nodes. Therefore, all the transistors connected to these nodes are of minimum size. For the same reason, the input of the common-mode feedback circuit is connected to the virtual ground of the opamp, i.e., to the output of the $f_{\rm VCO}$ chopper, rather than to the output of the OTA. Simulations over process and temperature corners show that the OTA's phase-spread is less than 0.2° over the industrial temperature range. Moreover, the phase spread within one batch will typically be an order of magnitude smaller.

The opamp integrator uses two 25 pF on-chip capacitors. As a tradeoff between signal level and noise bandwidth, the g_m of the OTA was chosen to be 100 μS, which corresponds to an FLL noise bandwidth of about 30 Hz. The integrator's opamp uses a folded-cascode topology with a typical DC gain of 96 dB. Together with the gain of the OTA, the result is a total front-end gain of about 150 dB.

At the input of the integrator, the chopper's charge-injection mismatch will result in a residual offset current that is proportional to $f_{\rm VCO}$ [12]. To solve this problem and to cancel the opamp's own offset, extra choppers were added around the

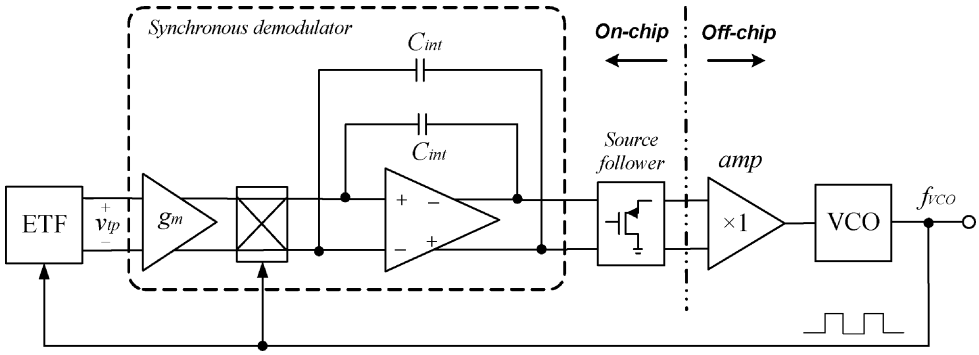

Fig. 3. Simplified block diagram of the implemented electrothermal FLL.

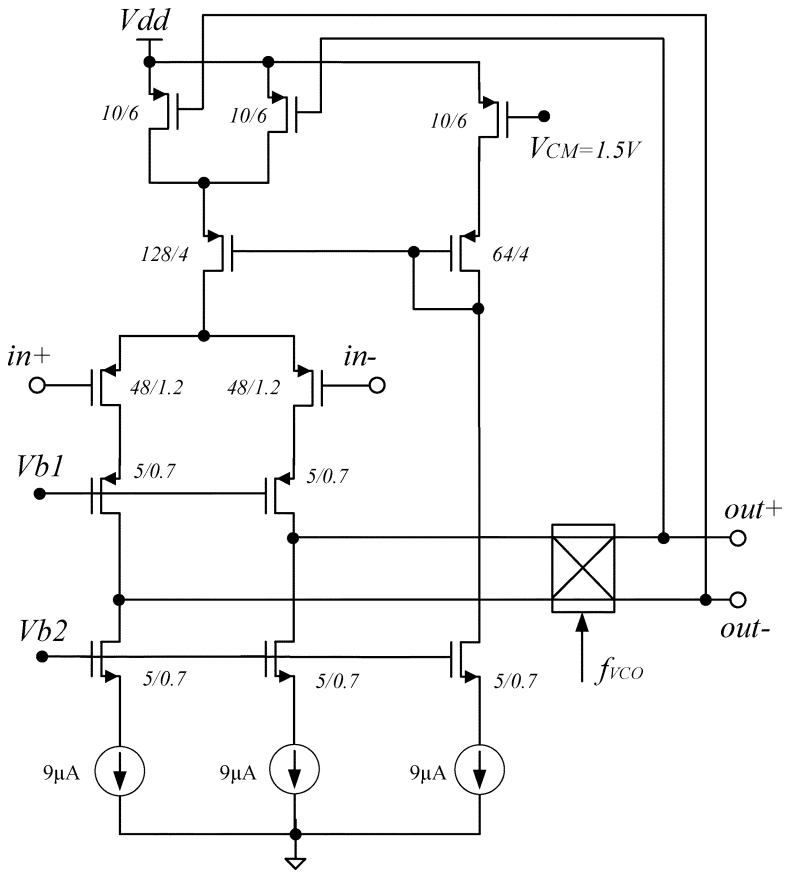

Fig. 4. Circuit implementation of the input transconductor.

opamp (Fig. 5). These choppers are operated at a lower frequency $f_{\rm VCO}/a$ ($a = 256$), and as a result, the residual offset current will be reduced by a factor of a.

To maintain the correct polarity of the integrated current, a digital chopper inverts the phase of the dissipated heat in the ETF at the same frequency $f_{\rm VCO}/a$. Similarly, negative feedback around the integrator is maintained by an extra chopper, which chops the output current of the opamp's differential input pair [13].

The offset of the OTA and the opamp will both give rise to ripple at the output of the integrator. The OTA's offset gives rise to a DC output current, which is then modulated by the $f_{\rm VCO}$ chopper. This, in turn, gives rise to triangular ripple at the integrator's output with a frequency of $f_{\rm VCO}$ (Fig. 6). The opamp's offset appears as a small voltage difference between its two input terminals. Due to the action of the $f_{\rm VCO}$ chopper, this voltage appears as a square-wave across the OTA's output, which will charges and discharges the parasitic capacitances present there. After demodulation by the $f_{\rm VCO}$ chopper, the result is a net DC current flowing into the integrator [14]. This current will be chopped by the $f_{\rm VCO}/a$ chopper, and will again appear at the integrator's output as triangular ripple, but at the lower frequency $f_{\rm VCO}/a$ (Fig. 6). Finally, the opamp's offset is also chopped by the $f_{\rm VCO}/a$ chopper, and so gives rise to square-wave ripple with a frequency of $f_{\rm VCO}/a$ at the integrator's output (Fig. 6).

Since the driving signals of the various choppers are all derived from $f_{\rm VCO}$, its duty cycle must be exactly 50% in order to achieve perfect offset cancellation. This means that the VCO's input should be kept constant throughout one complete chop-

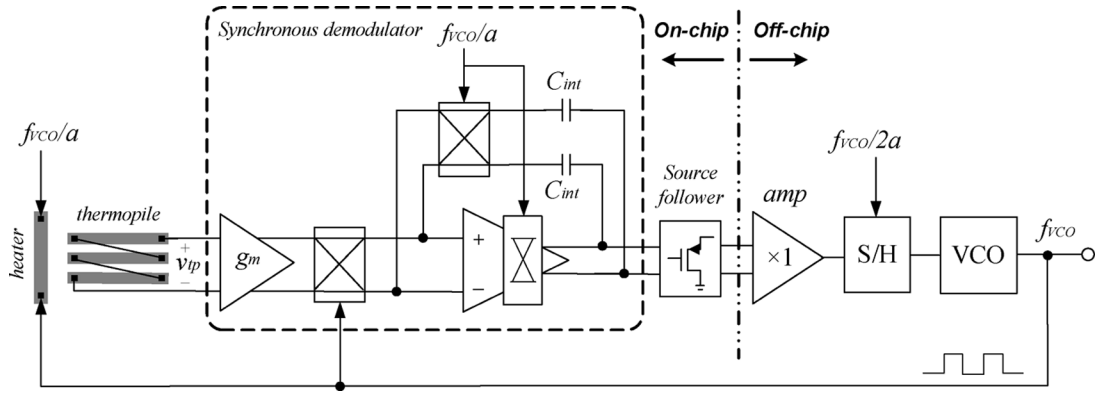

Fig. 5. Complete block diagram of the implemented electrothermal FLL.

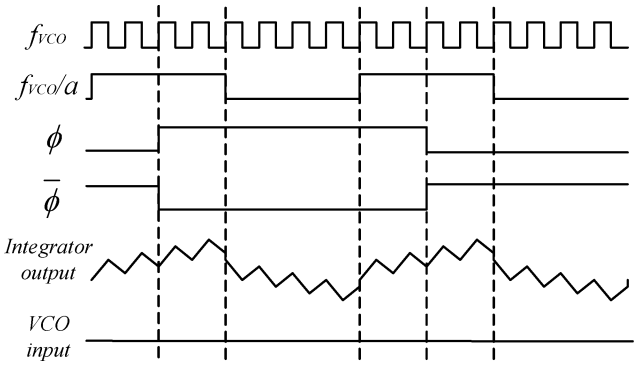

Fig. 6. Timing diagram of the sample-and-hold.

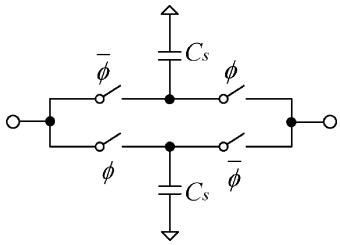

Fig. 7. Implementation of the S/H shown in Fig. 5.

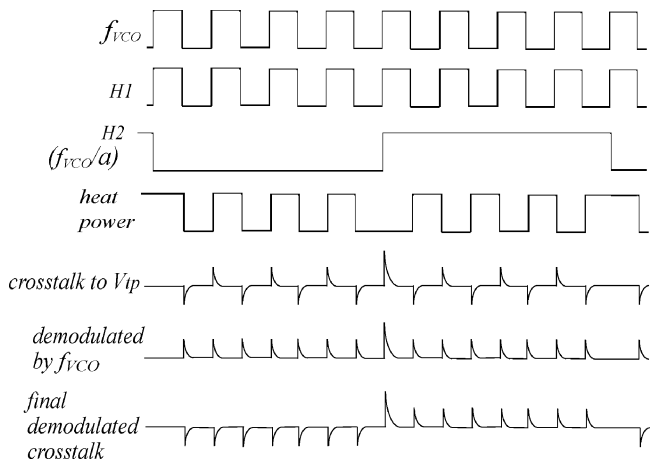

Fig. 8. Timing diagram of the crosstalk.

ping cycle, i.e., one period of $f_{\rm VCO}/a$. In other words, the AC ripple at the output of the integrator must be eliminated. In [7], this was done by implementing a large integrator time-constant with the help of a large (1 μF) external capacitor. However, this approach does not lend itself to integration. Another approach, and the one used here, is to employ a sample-and-hold (S/H) circuit as a notch-filter [14]–[16].

As shown in Figs. 5–7, an off-chip sample-and-hold (S/H) circuit at the output of the integrator was implemented using two capacitors and some switches. When driven at $f_{\rm VCO}/2a$, the S/H effectively removes the ripple present at the output of the integrator (Fig. 6). Such a S/H circuit can be readily implemented on chip [14]–[16]. This leaves the VCO as the major remaining off-chip component. However, the required tuning range, i.e., 70 kHz to 170 kHz is quite low, and such a VCO can readily be implemented in standard CMOS technology [17], [18].

Another source of error is crosstalk (via parasitic capacitances) between the heater drive voltages and the thermopile output. To eliminate this error, a simplified implementation of heater drive inversion [7], was used. As shown in Fig. 5, the terminals of the heater are driven by square-waves with frequencies $f_{\rm VCO}$ and $f_{\rm VCO}/a$. Consequently, the polarity of the heater drive voltages is inverted at a frequency of $f_{\rm VCO}/a$, and so is the polarity of the crosstalk (spikes) after demodulation by the $f_{\rm VCO}$ and $f_{\rm VCO}/a$ choppers (Fig. 8). The amplitude of the residual crosstalk is therefore reduced by a factor of a. A further advantage of this heater drive strategy is that it periodically inverts the polarity of the generated heat power (Fig. 8), and thus directly implements the required $f_{\rm VCO}/a$ digital chopper.

V. Measurement Results

The ETF, the synchronous demodulator, and the source followers were realized in a standard 0.7 μm CMOS process (Fig. 9). The entire chip has an area of 2.3 mm^2. The on-chip electronics (excluding the heater) dissipates 1 mW from a 5 V supply, of which roughly 50% is dissipated in the source follower. For flexibility, the S/H, the VCO, the instrumentation amplifier and the digital logic were implemented off-chip. Because the on-chip gain of the synchronous demodulator is sufficiently large, the gain of the instrumentation amplifier was set to unity, i.e., it is just used as a differential-to-single-ended converter.

At high temperatures, both the S/H switches and the protection diodes at the VCO input exhibit significant leakage currents (2 μA worst-case), which cause errors in the voltages stored on the sampling capacitors $C_{\rm s}$ (Fig. 7). To minimize these errors,

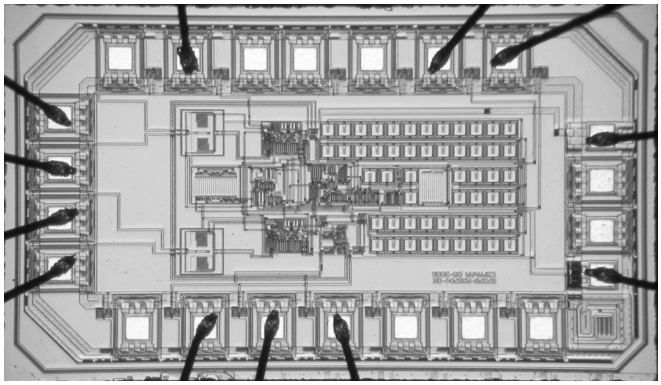

Fig. 9. Chip photo of the electrothermal FLL.

relatively large (10 μF) sampling capacitors were used. However, by integrating the VCO and the switches, such leakage currents can be drastically reduced, thus allowing the sampling capacitors to be made small enough (a few tens of picofarads) for on-chip integration. The implemented S/H effectively suppresses the ripple at the output of the integrator, which has a typical amplitude of several tens of millivolts. The residual ripple, as observed on an oscilloscope, is dominated by noise.

Measurements were made on 16 samples from one batch. As in [7], each sample was mounted in a ceramic DIL-16 package, and placed in an oven. Their temperature was then measured by a reference platinum thermometer, which was calibrated to within 20 mK at the Dutch Institute of Metrology. Measurements show that $f_{\rm VCO}$ has the expected $1/T^n$ dependence, where T is the absolute temperature in Kelvin, and $n \approx 1.8$ (Fig. 10). As in [7], the small systematic deviation between the pure power law model and the measured data (Fig. 11) was modeled by a fifth-order polynomial. Based on this model, the extrapolated value of $f_{\rm VCO}$ at 300 K is 103 kHz, which is about 2% larger than the value obtained in [7]. However, the value of n is now in much better agreement with the value expected from the known properties of bulk silicon [11]. This improvement, as well as the slightly larger value of $f_{\rm VCO}$ at 300 K, is probably due to the greater loop gain and reduced electrical phase spread of this FLL implementation.

At a heater power dissipation of 5 mW, the spread in $f_{\rm VCO}$ is less than $\pm 0.45\%$ (3σ) from $-40\,^\circ$C to $100\,^\circ$C. At lower heater powers, the spread increases. This is probably due to the fact that the ETF's output is then smaller, and so residual offset at the input of the integrator becomes the dominant source of error. The measured spread corresponds to a temperature inaccuracy of less than $\pm 0.7\,^\circ$C (3σ) (Fig. 12). This is in good agreement with earlier work [7], [10]. The FLL's output jitter corresponds to a temperature-sensing resolution of about $0.08\,^\circ$C (rms). The FLL's performance is summarized in Table I.

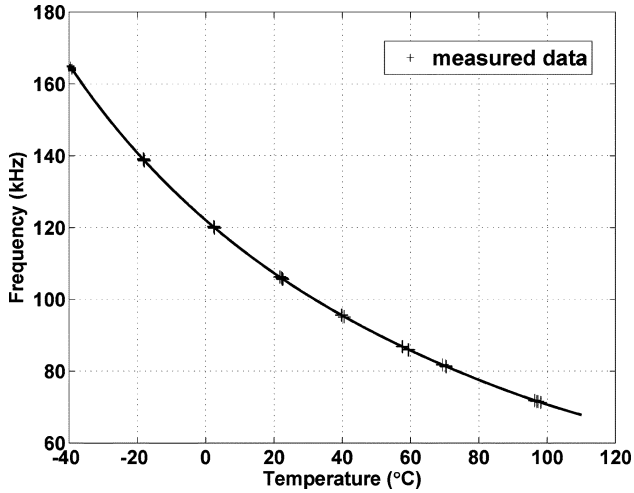

Fig. 10. Measured frequency versus temperature characteristic (16 samples from one batch) and a $1/T^n$ fit.

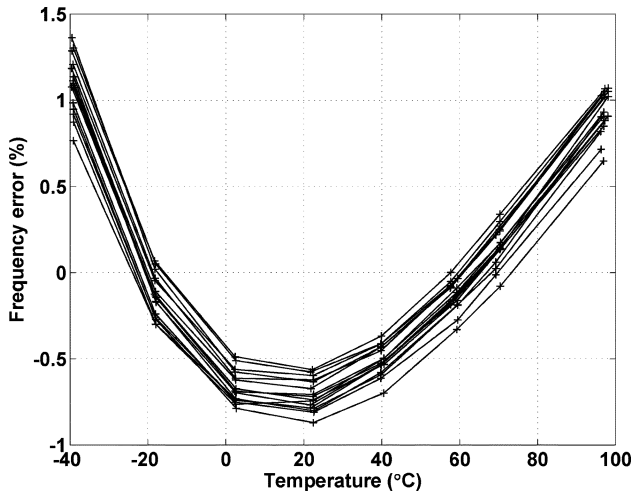

Fig. 11. Deviation of measured FLL characteristic from ideal $1/T^n$ fit.

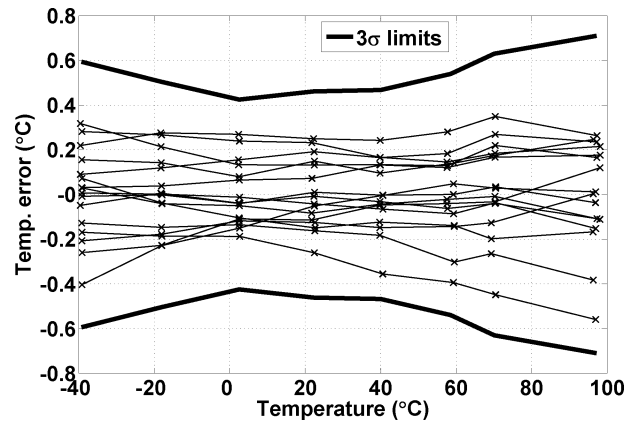

Fig. 12. Measured temperature error of 16 samples from one batch, with 3σ limits (bold lines).

VI. Outlook

In a fully integrated electrothermal FLL, the differential-to-single-ended conversion realized by the instrumentation amplifier can be eliminated. Ripple at the integrator's output can be removed by a differential S/H [16] which then drives a VCO with a differential input. Also, the source followers will no longer be required, and the resulting power savings (about 0.5 mW) will more than offset the extra power required by the VCO [17], [18]. As a result, the total power dissipated by the interface electronics should remain approximately the same, i.e., about 1 mW.

TABLE I
PERFORMANCE SUMMARY

Off-chip components	S/H, Differential amplifier, VCO
Electrical phase-spread	0.2 degree
On-chip steady-state gain	150dB
Required off-chip voltage gain	Not required
Noise bandwidth	30Hz
Error caused by noise (rms)	0.08°C
Temperature dependency of f_{VCO}	$f_{VCO} \propto 1/T^{1.8}$
Inaccuracy (3σ)	±0.7°C from 16 samples
Temperature range	−40°C to 100°C
Power dissipation of interface	1mW
Power dissipation of heater	5mW

VII. CONCLUSION

A new implementation of an electrothermal frequency-locked-loop (FLL) has been presented. The FLL is designed such that its output frequency is determined by an electrothermal filter. As a result, the temperature dependence of this frequency is determined by the temperature-dependent thermal diffusivity of bulk silicon, which, due to its high purity, is very well-defined. The measured device-to-device spread of the FLL's output frequency is less than $\pm 0.45\%$ (3σ) from $-40\,^{\circ}\mathrm{C}$ to $100\,^{\circ}\mathrm{C}$, which corresponds to an untrimmed inaccuracy of less than $\pm 0.7\,^{\circ}\mathrm{C}$ (3σ). Furthermore, the measured temperature dependence agrees very well with the known properties of bulk silicon. Compared to an earlier implementation [7], the electrothermal FLL presented here has significantly more loop gain, less electrical phase-spread, and is more suitable for full integration in standard CMOS technology. However, further work is required to reach the final goal: a fully integrated electrothermal FLL.

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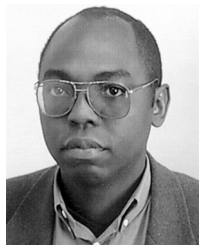

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