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DOI
10.23919/VLSIC.2017.8008555

Publication date
2017

Document Version
Final published version

Published in
Digest of Technical Papers - 2017 Symposium on VLSI Circuits

A Compact Sensor Readout Circuit with Combined Temperature, Capacitance and Voltage Sensing Functionality

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Abstract

This paper presents an area- and energy-efficient sensor readout circuit, which can precisely digitize temperature, capacitance and voltage. The three modes use only on-chip references and employ a shared zoom ADC based on SAR and ΔΣ conversion to save die area. Measurements on 24 samples from a single wafer show a temperature inaccuracy of ±0.2 °C (3σ) over the military temperature range (-55°C to 125°C). The voltage sensing shows an inaccuracy of ±0.5%. The sensor also offers 18.7-ENOB capacitance-to-digital conversion, which handles up to 3.8 pF capacitance with a 0.76 pJ/conv.-step energy-efficiency FoM. It occupies 0.33 mm^2 in a 0.16 μm CMOS process and draws 4.6 μA current from a 1.8 V supply. ***Keywords:*** temperature sensing, voltage sensing, capacitance-to-digital conversion.

Introduction

Capacitance and voltage sensing are often required in industrial and environmental measurements, calling for precision readout circuits that can digitize capacitance and voltage, and the associated references. Temperature variation, which typically affects the sensor, the circuit and the references, also needs to be accounted for, calling for accurate temperature sensing. This paper introduces a triple-mode readout circuit with on-chip references that combines these functionalities in one compact circuit capable of performing capacitance-to-digital (CDC), temperature-to-digital (TDC) and voltage-to-digital (VDC) conversion.

Sensor's architecture

Fig. 1 shows an overview of the readout circuit. It is composed of a shared incremental zoom ADC, on-chip reference voltages (V_{BE} and ΔV_{BE}) generated using substrate BJTs, and an on-chip reference capacitor (C_{REF}). The ADC uses a switched-capacitor (SC) architecture, which can be configured as a SAR or a ΔΣ [3, 4]. The ΔΣ loop filter (LF) is composed of two SC-integrators built around energy-efficient current-reuse OTAs. The first stage of the ΔΣ LF can perform as a charge amplifier, which together with a capacitive DAC (CDAC) implements the SAR. As in [3, 4], in TDC mode, the ADC converts $X_T=V_{BE}/\Delta V_{BE}$, whose value changes from ~28 to ~8 over the military range. X_T then translates to temperature by using $D_{out,TDC}=A\cdot(\alpha/(\alpha+X_T))-B$, where A, B, and α are calibration parameters. Converting X_T is done in a 2-step SAR-ΔΣ fashion, where the SAR step finds the integer part of X_T, and the ΔΣ step digitizes its fractional part [3, 4].

Similar to the TDC mode, in the CDC mode (Fig. 2), a SAR step finds the integer number of CDAC elements (N_{SAR}), closest to the input capacitance. This is done by comparing charges proportional to $V_{DD}\cdot C_{in}$ and $V_{DD}\cdot C_{REF}\cdot N$, where N=1:32 is implemented using the 32-element CDAC (Fig. 3). In the ΔΣ step, $N_{SAR}\cdot C_{REF}$ is subtracted from the input (Fig. 2) capacitance; thus, the ΔΣ loop balances the residual charge ($=V_{DD}\cdot(C_{in}-N_{SAR}\cdot C_{REF})$) against the reference charges $V_{DD}\cdot C_{REF}$, and $-V_{DD}\cdot C_{REF}$. The input capacitance can then be interpreted by combining the two results as $C_{in}=(N_{SAR}+2\cdot\mu_{\Delta\Sigma})\cdot C_{REF}$, where $\mu_{\Delta\Sigma}$ is the average value of the bitstream (bs) in the ΔΣ step. DEM logic shuffles the position of CDAC elements, and thus removes the non-linearity due to mismatch between these elements.

In VDC mode, the circuit uses a three-step (SAR1-SAR2-ΔΣ) conversion (Fig. 4). SAR1 [SAR2] finds the integer number of V_{BE}s [ΔV_{BE}s] closest to the input voltage Vin [$(V_{in} - M_{SAR1})$]. To do so, in SAR1 [SAR2] the charges proportional to $V_{in}\cdot C_{REF}$ [$(V_{in}-M_{SAR1}\cdot V_{BE})\cdot C_{REF}$], and $V_{BE}\cdot C_s\cdot M_1$ [$\Delta V_{BE}\cdot C_{REF}\cdot M_2$] are compared, where M_1 = 1:5 [M_2 = 1:32] are CDAC ratios. In the third step, the ΔΣ balances the charges proportional to $V_{in}\cdot C_s-(M_{SAR}\cdot V_{BE} + N_{SAR}\cdot\Delta V_{BE})\cdot C_{REF}$ against reference charges $-\Delta V_{BE}\cdot C_{REF}$, and $+\Delta V_{BE}\cdot C_{REF}$. The input voltage can then be interpreted as $(M_{SAR1}\cdot X_T+M_{SAR2}+2\cdot\mu_{\Delta\Sigma})\cdot\Delta V_{BE}$, where X_T is the TDC output.

Experiments

The circuit has been realized in a 0.16 μm CMOS process (Fig. 5). It occupies 0.33 mm^2 and draws 4.6 μA from a 1.8 V supply. The BJT-core and the ADC consume 2.8 μA and 1.8 μA, respectively. The logic for implementing the *sinc*^{2} decimation filter and digital processing are realized off-chip. At a sampling clock of 35 kHz, the TDC mode achieves 4 mK_{rms} resolution in a 100 ms conversion time. With the same conversion rate, the VDC and CDC modes achieve resolutions of 12 μV_{rms} and 2 aF_{rms} (Fig. 6), respectively.

A MEMS pressure sensor has been applied as a variable capacitance for the CDC measurement. The pressure of a vacuum chamber was slowly increased, while the CDC's output was continuously recorded (Fig. 7). This measurement was repeated with a fixed 2 pF additional capacitor in parallel to the sensor to demonstrate a different capacitance range.

Measurements of 24 samples of the sensor packaged in ceramic show a 3σ-inaccuracy of ±0.2 °C after single-temperature trimming (Fig. 8, left). The inaccuracy in the VDC mode's reference (which is based on approximating ΔV_{BE} as a linear function of the TDC output) is less than ±0.1% (Fig. 8, middle). In the current implementation, the untrimmed VDC inaccuracy is less than 0.5% (Fig. 8, right). This can be attributed to the mismatch of C_{REF} and C_s (which is not included in the DEM process). Fig. 9 compares the performance of this work with the state-of-the-art. This work represents a considerable improvement in energy-efficiency compared to prior multi-mode circuits [1, 6], and compares favorably to state-of-the-art stand-alone CDCs [2, 5], and TDCs [4].

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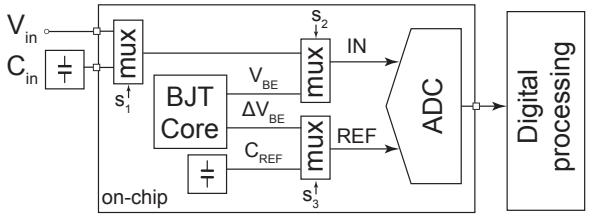

Fig. 1 Overview of the readout circuit. S_1, S_2, and S_3 are selected based on the sensor's mode

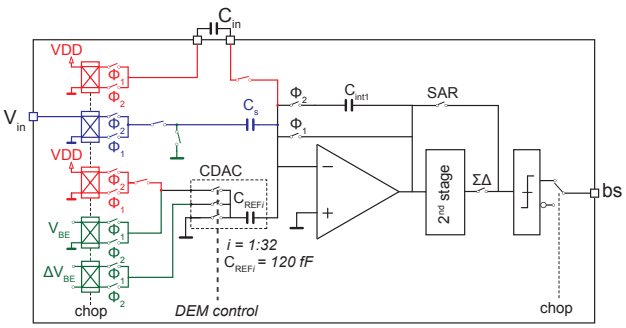

Fig. 3 Simplified circuit diagram of the sensor. TDC: green, CDC: blue and green, CDC: red.

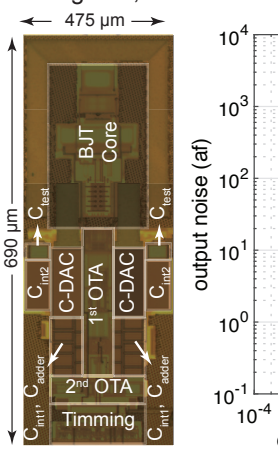

Fig. 5 Chip micrograph

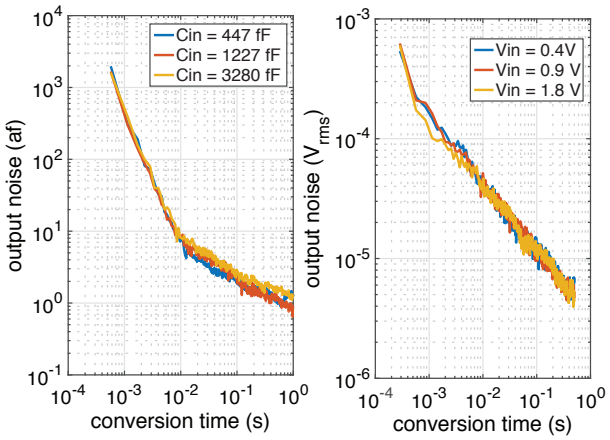

Fig. 6 Measured resolution vs conversion time. Left: capacitance sensing. Right: voltage sensing.

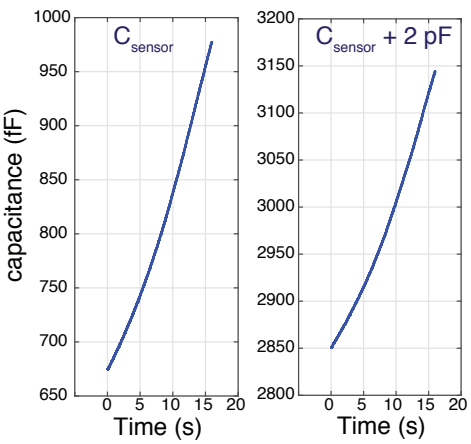

Fig. 7 Measured capacitance of a pressure sensor exposed to slowly-varying pressure

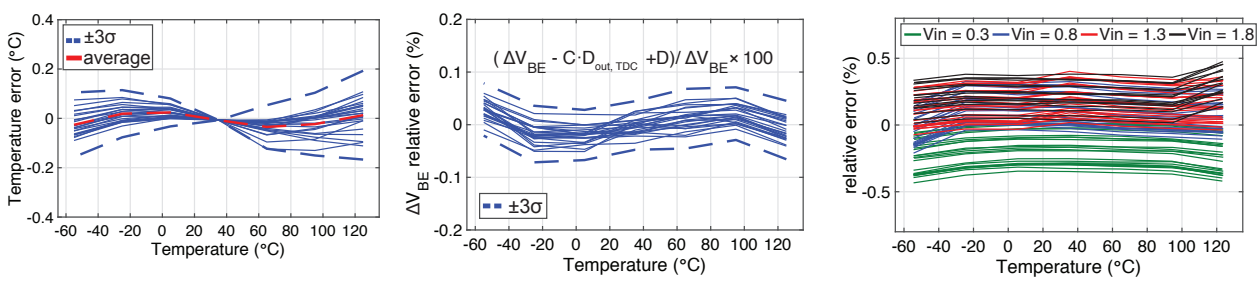

Fig. 8 Temp. error, ΔV_{BE} relative error using a linear estimation, and voltage sensing relative error for 24 samples

Item	Method	capacitance				temperature			voltage		$T_{conv.}$	supply current	supply voltage	area
		res. (aF)	range (pF)	ENOB[a]	res. FoM[b] (pJ/step)	range (°C)	±3σ-inacc. (°C)	res. FoM[c] (pJ°C²)	relative inacc.[d] (%)	range (V_{pp})	(ms)	(µA)	(V)	(mm²)
[6]	ΔΣ	20	8	19.1	6700	-40 – 125	±0.5	NA	0.1	5	200	700	2.7 – 5.2	-
[2]	SAR-ΔΣ	156	24	15.4	0.18	-	-	-	-	-	0.23	24	1.4	0.46
[5]	iterative discharge	12e3	10e3	8	0.14	-	-	-	-	-	0.019	1.84	1	0.002
[1]	ΔΣ	-	-	-	-	-40 – 105	NA	1875	0.012[e]	5	200	85	2.5 – 5.5	4.8
This work	SAR-ΔΣ	2.5	3.8	18.7	0.76	-55 – 125	±0.2	8	0.5	1.8	100	4.6	1.6 – 2	0.33

Fig. 9 Comparison table

[a] ENOB = (1/6.02)·(20·log(range / (2√2 · res.)) – 1.76)
[b] FoM = (power · $T_{conv.}$) / (2^{ENOB})
[c] FoM = (Energy per conversion) · (res^2)
[d] RI = 100 · (inaccuracy) / (range)
[e] Temperature drift only