Ultra-Low-Noise Cryogenic Multilevel Memristors for Sub-100 µV Spin Qubit Biasing

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***Abstract*—We demonstrate interface-enhanced memristors (OxReRAM) tailored for cryogenic spin-qubit control. By engineering a sparse filament network, our devices achieve eight nonvolatile resistance levels with an ultra-low read noise rate of around 0.3 %. When embedded in a cryogenic gain stage with $R_L = 30\,\mathrm{k}\Omega$ and $V_{\mathrm{in}} = 0.3\,\mathrm{V}$, it will deliver a ±1 V output range and sub-100-µV resolution using only six memristors per channel. This single-line biasing architecture will reduce wires, paving the way for large-scalce quantum processors.**

I. Introduction

Semiconductor quantum dots (QDs) now exhibit gate fidelities exceeding 99 % and coherence times from milliseconds to seconds, establishing them as leading platforms for fault-tolerant quantum processors [1], [2]. However, scaling from tens to thousands of qubits demands tens to hundreds of independent, ultra-low-noise DC biases per qubit for controlling potentials without overloading the dilution refrigerator cooling power or wiring capacity [3], [4]. For nowadays standard approach, each qubit requires $\sim$10 control electrodes, barrier, plunger, and screening gates, each routed through individual low-pass filters and cryogenic DACs at 4.2 K, then driven by high-speed links from 300 K controllers, as shown in Fig. 1(a). This $\mathcal{O}(N)$ wiring load imposes prohibitive heat leaks, cable bulk, and system complexity [3], [5], [6]. Malinowski *et al.* introduced the WISE architecture, embedding switch matrices on-chip to share waveform generators across many electrodes, reducing room-temperature DAC counts by an order of magnitude while still relying on multiple high-bandwidth feeds and analog filters [3]. A more radical solution leverages cryogenic nonvolatile memories: Mouny *et al.* demonstrated a memristor-based programmable gain amplifier (PGA) that replaces each DAC–filter pair with a single shared bias line and on-chip memristors crossbars at 4 K, collapsing feedthroughs to $\mathcal{O}(1)$ [4]. These works establish the feasibility of sub-µW, sub-µV-noise amplification at millikelvin temperatures. There, a common DC bias V_{in} and a serial/RF interface program memristor conductances in the feedback of *Cryo-CMOS* operational amplifier (OpAmp), yielding up to ten independent, sub-100-µV-resolved outputs per channel (see Fig. 1(b)). Meanwhile, the problem is that the read noise rate is around 1 % which is still not feasible for sub-100-µV step of gate voltage control. Complementary monolithic 65 nm CMOS studies have validated AD8605 amplifiers down to 1.2 K and TiO_2 memristor programming with 10 mV steps, enabling $\sim 10^6$ channels within a 1.5 W 4 K budget [7] while the problem is still there that the resolution is 10 mV which is still far from sub-100-µV precision. Nonetheless, key challenges remain [8]: achieving ultra-low programming read noise rate at 4.0 K and balancing the trade-offs among number of programming levels, read noise rate and output-voltage resolution. In this work, we propose, for the first time, modified interface-enhanced Pt/Ti/HfO_2/Pt memristors (M-PtHT) optimized for 4 K operation with eight-level programmability. Mounted on a *Cryo-PCB* test board, we evaluate resistance reliability, including retention and read noise rate. We demonstrate a read noise rate of around 0.3 %, and when integrated into a cryogenic PGA ($R_L = 30\,\mathrm{k}\Omega$, $V_{\mathrm{in}} = 0.3\,\mathrm{V}$), it will guarantee a ±1 V range of output voltage with <100 µV resolution using minimum 6 memristors in corssbar arrays. These results confirm memristor-PGA technology as a compact, scalable approach for next-generation quantum processors.

II. Resutls and Discussions

A. Cryo-Memristor-based Control Circuitry and Resolution Simulation

Figure 2 illustrates the cryogenic memristor-*PGA* for quantum-dot biasing and its simulated resolution. In Fig. 2a, a single 0.3 V DC bias passes through $R_L = 30\,\mathrm{k}\Omega$ into a *Cryo-CMOS OpAmp* whose feedback is an N_m-device memristor crossbar array (*CBA*). Programming each conductance G_i sets

$$R_{CBA} = \Big(\sum_i G_i\Big)^{-1}, \quad V_{\mathrm{out}} = V_{\mathrm{in}}\,\frac{R_{CBA}}{R_L} \approx 1\ \mathrm{V}$$

covering ±1 V without individual DACs. The QD cross-section (Fig. 2b) shows source/drain reservoirs, two barrier gates, and a plunger gate, all requiring sub-100-µV precision. Defining resolution $\delta V = (V_{\max} - V_{\min})/N_s^{N_m}$ with a 1 V range, Fig. 2c plots δV versus states N_s for $N_m = 4, 6, 8, 9$. Six-device arrays with five states yield $\delta V < 100\,\mu\mathrm{V}$, demonstrating that small *CBAs* meet qubit-biasing needs while reducing wiring to a single bias line and programming link.

B. Fabrication and Electrical Characterization of (M-)/PtHT Memristors

Figure 3 summarizes device structure, switching physics, test waveforms, I–V cycling, and fabrication flow. In PtHT devices (Fig. 3a,b), negative bias drives oxygen vacancies away from the HfO_2/Pt interface, rupturing filaments and switching to a high-resistance state. The M-PtHT variant adds a 1 nm interfacial Pt layer (Fig. 3c,d), which suppresses

stochastic vacancy drift at the Ti/HfO_2 interface, sharpening state separation and reducing variability.

We apply a bipolar staircase waveform (20 mV steps, 50 ms hold/delay, ±1.0/–1.5 V stop voltages; Fig. 3(e) to program eight levels, then record ten consecutive I–V loops (Fig. 3(f). Both stacks exhibit stable LRS/HRS switching, with M-PtHT showing an expanded memory window. All devices are fabricated on Si/SiO_2 using PVD for HfO_2, and EBE for Ti adhesion and Pt layers, with optical inspection ensuring pad integrity (Fig. 3g).

At 300 K, a Keysight B1500A applies a 3.5 V electroforming pulse followed by ten SET/RESET cycles (±1.0/–1.5 V) to assess variability. Multi-level programming uses variable RESET stops, and retention is measured under 0.2 V reads every 35 ms over 800 s to quantify drift and read noise rate. Cryogenic tests on wire-bonded chips mounted on a KiCad PCB board in a 4.0 K cryostat repeat the same protocols (Fig. 4), confirming device robustness under cycling and retention test.

C. Reliability under 300 K and 4.0 K

Figure 5 summarizes endurance cycling (a) and seven-level retention for both PtHT and M-PtHT memristors (b-d) at room temperature (300 K) and cryogenic (4.0 K) conditions. PtHT devices are subjected to over 3 $\times 10^3$ SET/RESET cycles with a read bias of 0.2 V. The LRS (orange) and HRS (purple) remain well separated, demonstrating robust switching and negligible degradation. After programming seven distinct resistance levels (R1–R7) at 300 K, each level is monitored under 0.2 V bias for 800 s. The levels remain drift-limited spread but few states collisions, especially for higher resistance states. Under cryogenic operation, M-PtHT devices exhibit even tighter level clustering, higher number of resistance states and alleviated drift and read noise over 800 s, confirming their suitability for long-term QD gate biasing with descent stability. Therefore, these results validate that the Pt-based devices deliver sufficient endurance cycle for resistive switching, multilevel retention, and cryogenic reliability required for programmable, on-chip DC-bias generation in scalable quantum processors.

D. Statistical Variability of Multi-Bit Resistance States

Figure 6 quantifies the standard deviation of programmable resistance levels in PtHT and M-PtHT devices at 300 K and 4.0 K. Cumulative distribution functions (CDFs) of resistance levels are evaluated in Fig. 6(a) for PtHT at 300 K and it shows broad distributions for each level (20 kΩ–180 kΩ), with clear separation but substantial overlap at higher states. Meanwhile, M-PtHT at 300 K in Fig. 6(b) exhibits tighter clustering (10 kΩ–70 kΩ), indicating reduced read noise. Fig. 6(c) of M-PtHT at 4.0 K demonstrates the narrowest distributions, confirming cryogenic suppression of ionic motion and drift. Standard Deviation vs. Mean Resistance plotting σ against mean R for PtHT (orange), M-PtHT at 300 K (purple), and M-PtHT at 4.0 K (red) reveals distinct trends: PtHT follows an exponential scaling $\sigma = 2.9\,R^2$ (COD=0.993), reflecting increasing read noise at high resistance. M-PtHT at 300 K and 4.0 K follow linear relationships $\sigma = 0.031\,R$ (COD=0.9996) and $\sigma = 0.003\,R$ (COD=0.993), respectively, indicating voltage-programming noise remains proportional to the state value and is suppressed at cryogenic temperatures. Fig. 6(e) show expanded M-PtHT linearity for M-PtHT at 300 K, highlighting their sub-percent slopes (read noise rate). These results confirm that the M-PtHT stack achieves the lower-noise, multilevel stability, necessary for sub-100-μV bias generation in quantum-dot control circuits as simulated results in Fig. 2(d). In PtHT, read noise is dominated by stochastic trap capture, emission and local Joule-heating in nanometric filament constrictions. Because $R \propto 1/A$, small cross-section fluctuations ΔA induce $\Delta R \propto R^2$, yielding quadratic scaling. With a 1 nm Pt interlayer (M-PtHT), vacancy migration is homogenized across many conductive paths; numerous uncorrelated ΔR events aggregate Gaussian-like, so σ scales linearly with R. Cryogenic cooling reduces trap kinetics, lowering the linear noise coefficient while preserving proportional dependence (Fig. 6(f)).

III. Conclusion

We have demonstrated interface-enhanced Pt/HfO_2/Ti/Pt memristors that deliver eight distinct resistance states with approximately 0.3 % read noise rate. Minimal 6 memristors being integrated into a cryogenic PGA with $R_L = 30\,\mathrm{k\Omega}$ and $V_{\mathrm{in}} = 0.3\,\mathrm{V}$, can guarantee a ±1 V range and <100 μV resolution per channel. This approach collapses wiring complexity to a single bias feed and serial interface, enabling scalable, high-precision control for next-generation quantum processors.

References

[1] J. J. Pla, K. Y. Tan, J. P. Dehollain, W. H. Lim, J. J. Morton, F. A. Zwanenburg, D. N. Jamieson, A. S. Dzurak, and A. Morello, "High-fidelity readout and control of a nuclear spin qubit in silicon," *Nature*, vol. 496, no. 7445, pp. 334–338, 2013.

[2] C. J. Ballance, T. P. Harty, N. M. Linke, M. A. Sepiol, and D. M. Lucas, "High-fidelity quantum logic gates using trapped-ion hyperfine qubits," *Physical review letters*, vol. 117, no. 6, p. 060504, 2016.

[3] M. Malinowski, D. Allcock, and C. Ballance, "How to wire a 1000-qubit trapped-ion quantum computer," *PRX Quantum*, vol. 4, no. 4, p. 040313, 2023.

[4] P.-A. Mouny, Y. Beilliard, S. Graveline, M.-A. Roux, A. El Mesoudy, R. Dawant, P. Gliech, S. Ecoffey, F. Alibart, M. Pioro-Ladrière *et al.*, "Memristor-based cryogenic programmable dc sources for scalable in situ quantum-dot control," *IEEE Transactions on Electron Devices*, vol. 70, no. 4, pp. 1989–1995, 2023.

[5] F. A. Zwanenburg, A. S. Dzurak, A. Morello, M. Y. Simmons, L. C. Hollenberg, G. Klimeck, S. Rogge, S. N. Coppersmith, and M. A. Eriksson, "Silicon quantum electronics," *Reviews of modern physics*, vol. 85, no. 3, pp. 961–1019, 2013.

[6] D. M. Zajac, A. J. Sigillito, M. Russ, F. Borjans, J. M. Taylor, G. Burkard, and J. R. Petta, "Resonantly driven cnot gate for electron spins," *Science*, vol. 359, no. 6374, pp. 439–442, 2018.

[7] P.-A. Mouny, R. Dawant, P. Dufour, M. Valdenaire, S. Ecoffey, M. Pioro-Ladrière, Y. Beilliard, and D. Drouin, "Towards scalable cryogenic quantum dot biasing using memristor-based dc sources," *Cryogenics*, vol. 142, p. 103910, 2024.

[8] A. D. O'Connell, M. Ansmann, R. C. Bialczak, M. Hofheinz, N. Katz, E. Lucero, C. McKenney, M. Neeley, H. Wang, E. M. Weig *et al.*, "Microwave dielectric loss at single photon energies and millikelvin temperatures," *Applied Physics Letters*, vol. 92, no. 11, 2008.

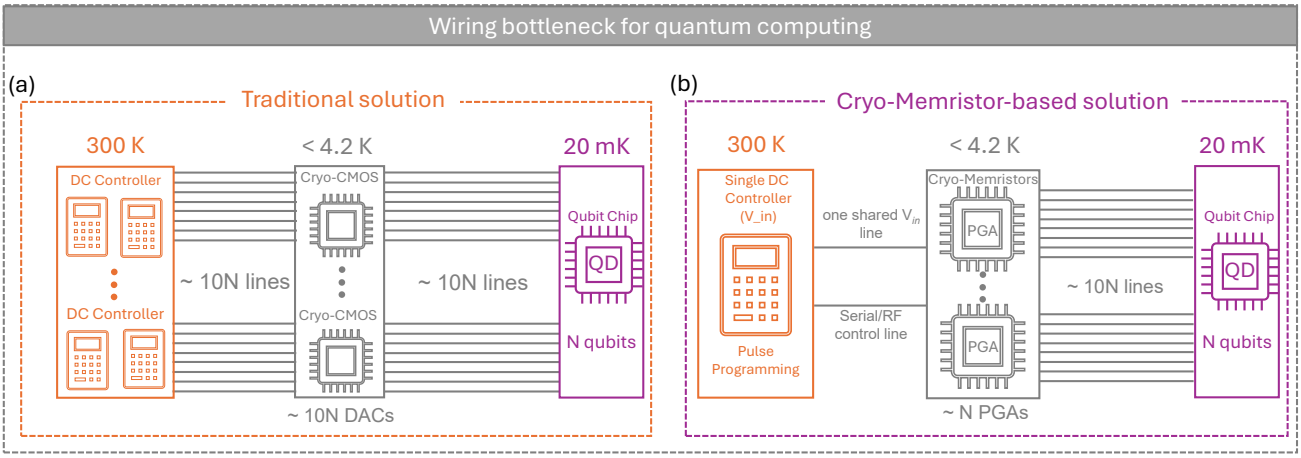

Fig. 1. Schematic comparison of control wiring for large-scale quantum processors. (a) Traditional solution: Each of N qubits at 20 mK uses $\sim 10N$ DC electrodes, routed through low-pass filters into $\sim 10N$ *Cryo-CMOS* DACs (< 4.2 K), each driven by its own high-speed digital link from 300 K. This requires $\mathcal{O}(N)$ digital and coax lines, creating thermal load and cabling complexity. (b) Cryo-Memristor-based solution: A single shared bias line V_{in} and one serial/RF link from 300 K feed on-chip memristor -based Programmable Gain Amplifiers (PGAs) at 4.2 K, which locally synthesize $\sim 10N$ electrode voltages. Wiring scales as $\mathcal{O}(1)$, reducing heat load and enabling scalable qubit integration.

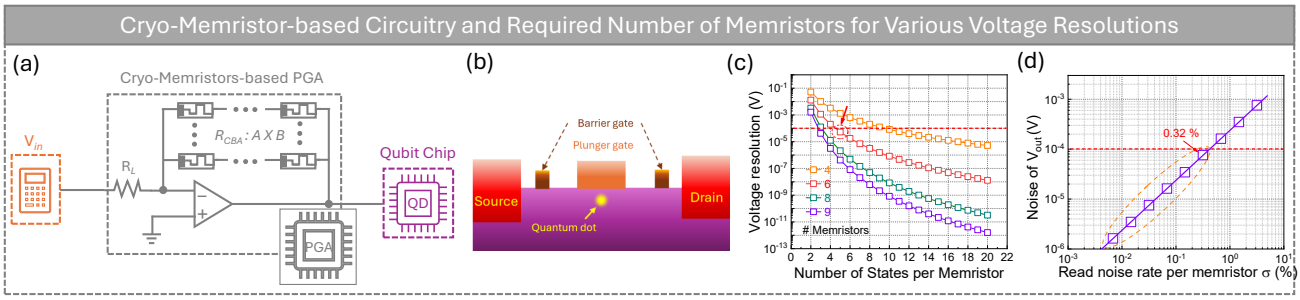

Fig. 2. Cryo-Memristor-based control circuitry for quantum dot devices and its performance. **(a)** Schematic configuration of the spin qubit control: a single room-temperature DC bias V_{in} is applied through load resistor R_L (30 kΩ) to on-chip memristor crossbar arrays (*CBA*) with A × B size in feedback around a *Cryo-CMOS* operational amplifiers (*OpAmp*), generating multiple individually tuned outputs for quantum-dot gates. **(b)** Cross-section schematic of a lateral quantum dot, showing barrier and plunger gates that require precise DC biases. **(c)** Simulated voltage resolution versus states per memristor for arrays of 4–9 devices, demonstrating sub-100-μV resolution with modest array size (e.g. 6 memristors with 5 states), given the V_{in}= 0.3 V, to make sure the V_{out} is ranging from 0.1 V to 1.0 V. **(d)** The Monte Carlo simulation to show how single-device read-noise rates (0.003 %–3 %) translate into output-voltage noise $\sigma(V_{\text{out}})$ for a 6 × 5-state memristors PGA, where less than 0.32 % read noise rate per memristor is required to make sure the noise of V_{out} is less than the V_{out} resolution.

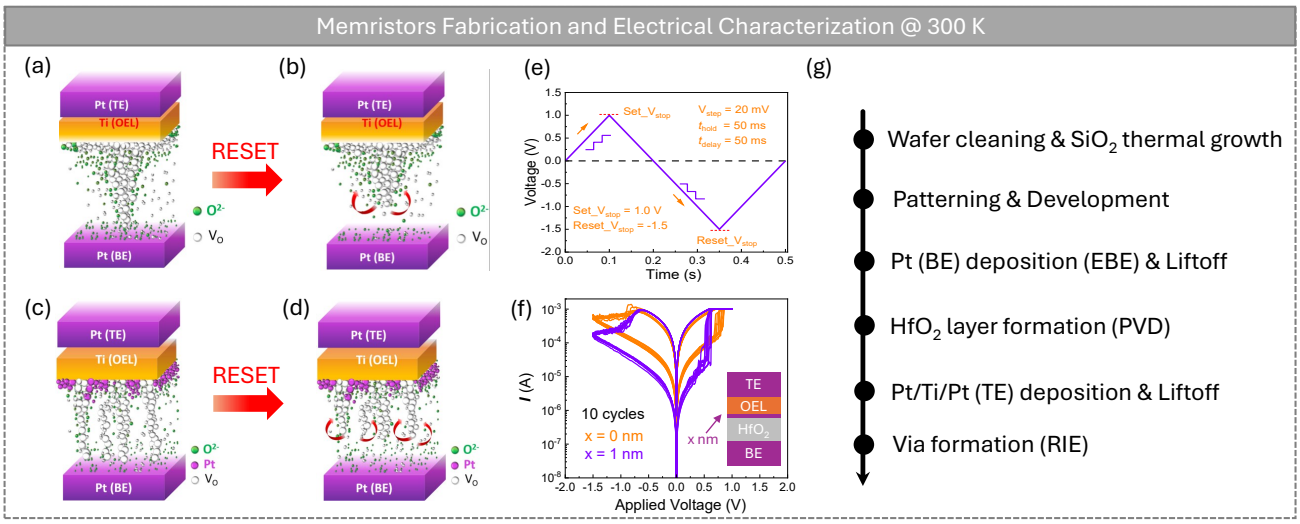

Fig. 3. Fabrication process and electrical characterization of the Pt/Ti/HfO_2/Pt (PtHT) memristor. **(a,b)** RESET mechanism: oxygen vacancies migrate away from the HfO_2/Pt interface under a negative voltage on top electrodes (TE) while bottom electrodes (BE) are grounded, rupturing the multiple conductive filaments. **(c,d)** Modified memristors PtHT (M-PtHT with 1 nm of innert interfacial metal layer) : vacancy drift at the Ti/HfO_2 interface similarly disrupts the filament. **(e)** Bipolar voltage waveform used for set/reset cycling schemes. **(f)** Ten consecutive I–V loops demonstrating stable switching between low- and high-resistance states for PtHT and M-PtHT. **(g)** Device fabrication flowchart: EBE: Electron Beam Evaporator; PVD: Physical Vapor Deposition; RIE: Reactive Ions Etching.

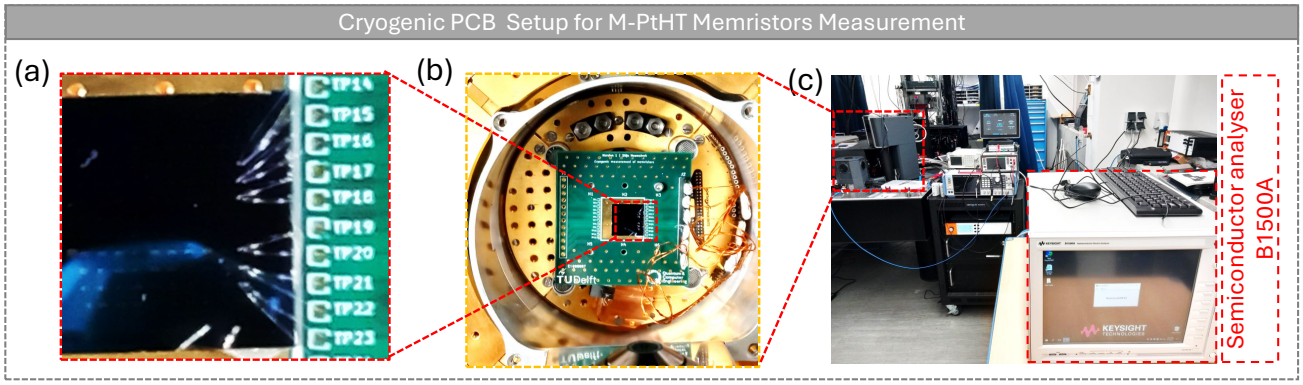

Fig. 4. Cryogenic measurement setup for M-PtHT memristors: (a) M-PtHT memristor chip on test PCB; (b) Mounted on 4 K stage with wire bonds; (c) External Keysight B1500A semiconductor analyzer controlling and reading via cryostat feedthroughs.

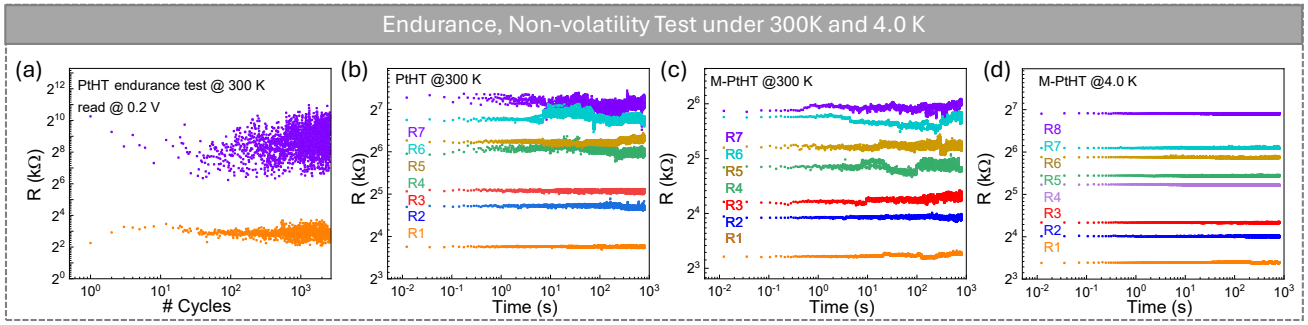

Fig. 5. Endurance and multi-bit retention of PtHT and memristor-integrated PtHT (M-PtHT) devices at room temperature and cryogenic conditions. **(a)** Endurance test of PtHT devices at 300 K with read bias 0.2 V, showing stable low- and high-resistance states over $> 10^3$ cycles. **(b)** Seven-level retention of PtHT at 300 K: each resistance level R1–R7 remains distinct and drift-limited over 800 s. **(c)** M-PtHT at 300 K similarly retains seven programmed levels with minimal overlap. **(d)** M-PtHT at 4.0 K demonstrates robust multi-level retention under cryogenic operation, confirming suitability for quantum-dot gate biasing.

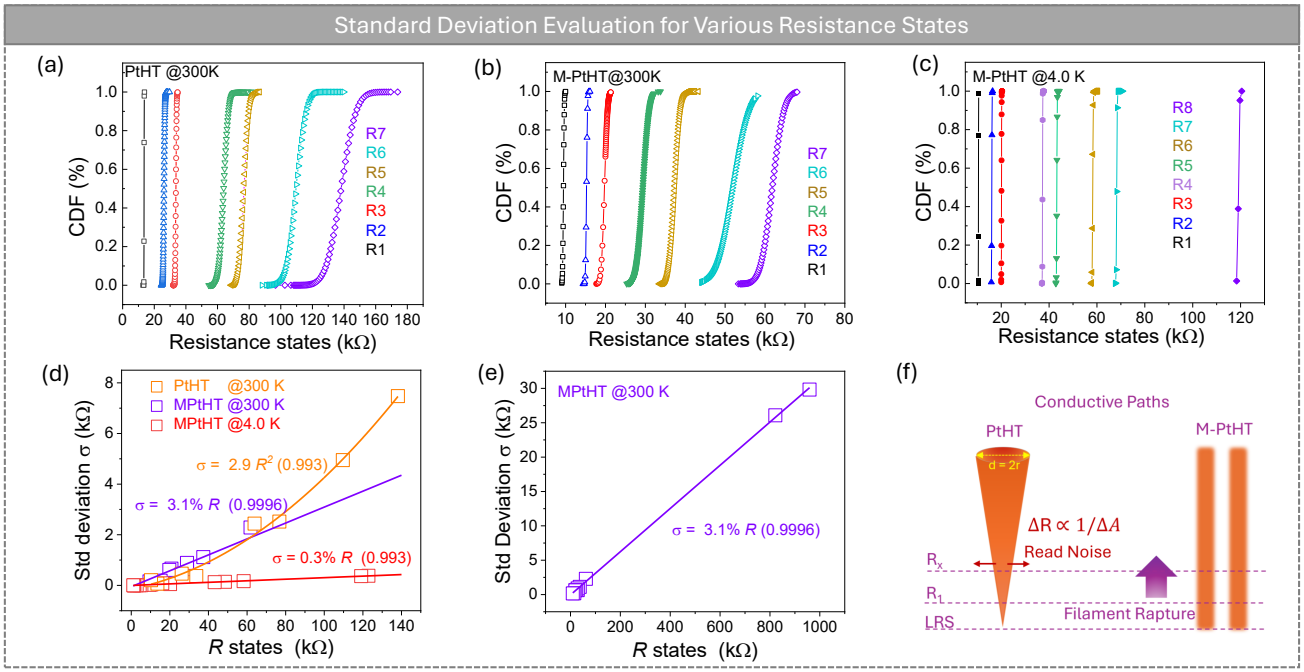

Fig. 6. Statistical variability of multi-bit resistance states in PtHT and M-PtHT memristors. **(a–c)** CDFs of seven programmed levels R1–R7 at 300 K in PtHT (a), 300 K in memristor-integrated M-PtHT (b), and 4.0 K in M-PtHT (c), showing tighter clustering in the M-PtHT devices. **(d)** Standard deviation σ versus mean resistance: PtHT at 300 K (orange) exhibits an exponential increase, fitted by $\sigma = 2.9\,R^2$, whereas M-PtHT at 300 K (purple) and 4.0 K (red) follow linear trends with slopes of 3.1% and 0.3%, respectively. **(e)** Expanded M-PtHT linearity and it fits for M-PtHT at 300 K. **(f)** Schematic illustration of the read noise difference for PtHT and M-PtHT.