Energy Efficient and Compact RF High-Power Amplifiers

David Angel CALVILLO CORTÉS

Energy Efficient and Compact RF High-Power Amplifiers

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A mis padres, mi esposa y mi amada familia.

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INTRODUCTION

Communications have been essential for the development of our society since the very beginning of our existence. Modern information and communication technology (ICT) is at the core of today's knowledge-based society and economy. The need of the human nature to communicate has significantly stimulated innovation and invigorated the telecommunications industry. The exponential increase of popularity for personal communications, internet and, lately, the so-called "internet-of-things" (which is a term utilized to denote advanced connectivity of devices, systems, and services beyond machine-to-machine communications, including a variety of protocols, domains, and applications yet to be developed) is a genuine driver of this industry that is affecting everyone's life in one way or another.

Since its beginning, the history of the communications industry has been linked with electronics. Although, as early as 1865, the existence of electromagnetic waves was predicted by Maxwell's theory of electromagnetism, it was not until 1887 that Hertz demonstrated practically that such radio waves could travel over distance. It took decades after this before technology would actually enable the development of practical wireless communications whereby the transmitter has been always considered a key element. The history of transmitters and amplifiers can be broadly divided into four eras [1, 2]. In the early days from 1895 to the mid 1920s, radio-frequency (RF) power was generated by rudimentary spark, arc, and alternator techniques. Later, following the invention of the thermionic "triode" in 1907, vacuum tube transmitters were dominant from the late 1920s until the mid 1970s. The commercial introduction of silicon bipolar transistors by the end of the 1960s initiated a new era, and discrete solid-state RF power devices of many types were commonplace and replaced vacuum tubes in most applications. From the late 1980s and 1990s, innovative solid state devices based on compound semiconductors such as GaN, SiC, and InP appeared which added new transistor options for the power amplifiers applied in these transmitters. All of these technological innovations along with information theory developments and extensive computational improvements have facilitated the exponential use of mobile communications and its market. However, along with these tremendous technical advances, power consump-

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tion and their inescapable environmental footprint have significantly increased, which demands attention in order to improve the energy efficiency of communication systems.

This chapter provides the motivation, objectives, and outline of this thesis. As an element of the motivation and contextualization of this work, the modern cellular networks are first briefly described followed by a discussion of the current "energy cost" of wireless communications. In this aspect, the RF power amplifiers have been established as one of the most power-hungry components of communications systems [3–5] and, as such, techniques to making them more energy efficient are the core subject of this thesis. In view of this, the influence of the actual modulated signal (i.e., the signal to be transmitted) on the power amplifier performance is explained together with a brief overview of the primary efficiency-enhancement techniques proposed in the field. The objectives of the research in this thesis are subsequently provided as well as the outline of the succeeding chapters.

1.1. MODERN CELLULAR NETWORKS

The earliest radio stations were merely radiotelegraphy systems and, following the invention of the electronic detection and amplification, other forms of wireless communication ensued such as radio and TV broadcasting and personal communications. The modern-day and almost ubiquitous mobile-phone system is based on cellular networks as proposed by Bell Labs, which was first outlined at the end of the 1940s [6] and refined over the next two decades [7, 8]. Illustrated in Fig. 1.1, this system re-uses the scarce frequency spectrum in a coverage area by dividing it into cells that use slightly different frequencies or channel sets (e.g., f_A to f_G in Fig. 1.1a [8]) to communicate from a

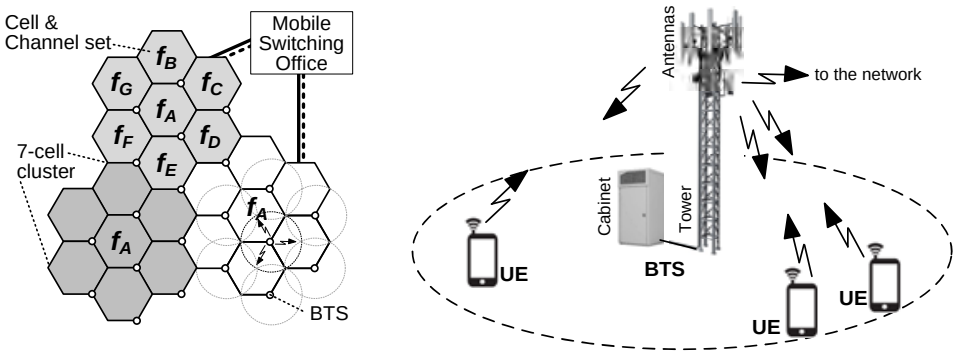

Figure 1.1: Cellular network concept: a) frequency re-use through spatial separation using cells, and b) single cell with a radio base station serving different users.

fixed station to mobile users. Conventionally, these geographical areas are depicted as hexagons with cell sites located at alternate corners, each containing a base transceiver station (BTS, also referred to as radio base station or simply base station). Typically, each base station incorporates three directional antennas sectored 120° apart that radiate inwards each cell within a (rhomboid-like) sector, serving the users' equipment (UE) or mobile devices located within that sector while other cell sites provide for the other sectors of the cells. In order to reduce interference, adjacent cells transmit on different frequencies with an established re-use pattern, for example, Fig. 1.1a illustrates a re-use pattern of seven [8]. Likewise, Fig. 1.1b illustrates a simplistic view of a conventional macro-cell in which the base station comprises mainly a cabinet (an air-conditioned weather-proof enclosure housing radio access equipment) and a tower (a mast supporting the feeder co-axial cables and the antennas) that communicate with several users within its own coverage range. The average power of the communications link determines each cell, which can range from a few meters (femto/pico-cells) to a few tens of kilometers (macro-cells) cell radius. In general, the actual mobile networks are evolving towards heterogeneous architectures comprising base stations of various sizes (macro-, micro-, pico- and femto-cells), a greater quantity of cell sectors and other techniques that aim at increasing capacity and system performance.

Wireless communication standards have evolved over time and continue to do so (regarded as generational changes, from 1G to 4G+) as the number of mobile-phone users and services increases. The earliest systems (prior to actual standardization) began in the USA as early as 1947 with the "Mobile Telephone Service" (MTS) that eventually evolved into the "Improved MTS" (IMTS) in 1965. A little later, other systems also appeared in other countries such as the Autoradiopuhelin (ARP) or "car radio phone" in Finland, however, the number of users was limited and the standards varied widely. The official first generation of standards, or "1G", was initiated in the late 1970s with the current cellular network concept and exploited analog modulation and frequency division multiple access (FDMA) techniques. Primary examples include the Advance Mobile Phone System (AMPS) in the USA, the Nippon Telegraph and Telephone (NTT) network in Japan, and the Nordic Mobile Telephone (NMT) in Northern Europe. By the early 1990s, "2G" systems appeared that were driven by considerably increasing numbers of users. This system introduced digital modulations as well as both time (TDMA) and code division multiple access (CDMA). The principle 2G standards are (where the first three use TDMA for user separation) the European Global System for Mobile Communications (GSM), the Japanese Personal Digital Cellular (PDC), and the North-American IS-136 or Digital-AMPS (D-AMPS) and IS-95 or cdmaOne. GSM introduced innovative digital services such as the short message service (SMS) and became immensely popular worldwide. Later, in the early 2000s, GSM networks introduced packet switching methods to increase data rates and digital services including the multimedia messaging service (MMS) and (basic) internet access and, after further improvements, subsequently became the General Packet Radio Service (GPRS), the Enhanced Data rates for GSM Evolution (EDGE), and the Enhanced GPRS (EGPRS) which are considered "2.5G", "2.75G" and "2.9G" standards, respectively. In an effort to facilitate the transition to "3G" systems, also in the early 2000s, the International Telecommunication Union (ITU) coordinated the efforts of government, industry, and the private sector in the development of a global

set of standards, referred to as the International Mobile Telecommunications-2000 (IMT-2000) specifications. 3G systems are required to provide peak data rates of at least 200 kbits/s. They must also provide a variety of services in addition to voice telephony such as several types of internet access, video calls, and mobile TV. The most important 3G systems include the Universal Mobile Telecommunications System (UMTS), in which the most widespread radio interface is Wideband-CDMA (W-CDMA) and is standardized by the 3G Partnership Project (3GPP); and the (less popular) CDMA2000 system that is standardized by the 3G Partnership Project 2 (3GPP2). By 2008, the ITU also established the requirements for "4G" systems in the IMT-Advanced specifications that require data rates of hundreds of Mbits/s and allow additional data-intensive applications such as mobile broadband internet access and new services such as high-definition television. Two main standards are considered 4G: the Long Term Evolution-Advanced (LTE-A) and the Worldwide Interoperability for Microwave Access (WiMAX). Currently, market forces are requesting even greater data rates than 1Gbits/s in wireless channels, affording the possibility for what is beginning to be termed "5G" systems that, at this time, do not yet have an official standard.

1.2. THE ENERGY COST OF WIRELESS COMMUNICATIONS

The enormous demand for data is increasing the energy consumption of ICT devices and infrastructure worldwide, leaving behind significant economic and environmental footprints. Telecommunications operator (fixed and mobile) networks wield a substantial aggregate energy consumption of approximately 260 TWh per year (2012) [9], representing about 1.3% of the total worldwide electricity expenditures [10]. This energy consumption has been rapidly increasing over recent years at almost 10% or higher per year (2007-2012) [5,9], primarily due to an expanding demand for coverage and capacity. Since only a minimal amount of this energy is derived from renewable energy sources, there is a significant environmental footprint from ICTs which are responsible for about 2% of the greenhouse gas emissions worldwide (similar to the entire aviation industry) [11]. From the total carbon dioxide emissions of ICT devices, mobile and fixed-line telecommunications are accountable for 9% and 15% (2007) [12], respectively, although it is expected that mobile telecommunications will dominate by 2020 [11]. Global communication networks have expanded to support billions of users with currently more mobile (more than six billion) than fixed subscriptions (less than two billion), and traffic within those networks has been increasing twofold every year. This is predominantly due to an increase in mobile "broadband" custumers that, in 2010, represented 15% of the subscriber base and is expected to reach 100% by 2020 [5]. Therefore, as the demand for mobile broadband services is expected to continue to rapidly increase, according to recent reports, "keeping network energy consumption flat, or even reducing it, will be a major objective for operators over the next decade in order to stay profitable" [5]. Specifically for wireless infrastructure systems, the current energy costs constitute 10-15% of the total network operating expenses (OPEX) in mature markets and can amount up to 50% in developing markets [5]. Therefore, addressing the energy efficiency of the actual

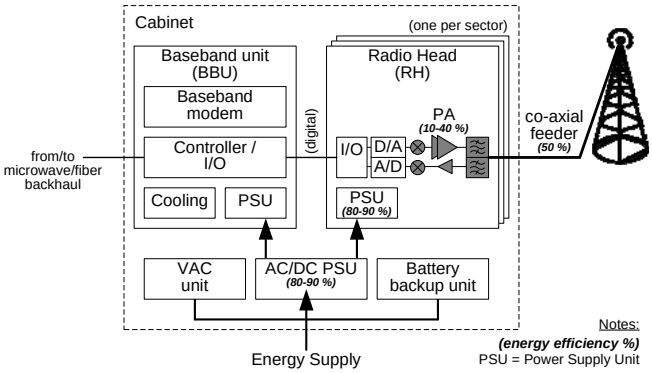

Figure 1.2: Functional components of a typical 3-sector 3G/4G macro-cell base station with an indication of the energy efficiency of its key components.

wireless infrastructures (and mobile devices) is vital.

In order to accomplish more energy-efficient wireless communications infrastructures, several key areas have already been identified involving both software and hardware solutions [4, 5] and ranging from network modernization, optimization, and improved management up to the actual base station energy efficiency. In fact, it is estimated that approximately 75-80% of all mobile network energy expenditure (including cell sites, mobile telephone switching offices, data centers, and retail locations) is due to the radio access equipment at the base stations [3,5,9]. In particular, the power amplifier is directly responsible for almost 65-70% and indirectly (in regard to power supplies and air cooling) up to about 85-90% of the total power consumption in the base station while only about 5% of this total energy actually reaches the on-air radio waves [3–5]. Fig. 1.2 depicts the main functional components of a typical 3-sector 3G/4G macro-cell radio base station together with an indication of the energy efficiency of its key components. Similarly, in user mobile phones, the power amplifier is also one of the most power-hungry elements. Therefore, from a hardware perspective, improving the efficiency of the power amplifier block is one of the most effective measures to decrease the overall energy consumption of wireless communications.

1.3. THE EFFICIENCY CHALLENGE IN RF POWER AMPLIFIERS

With the evolution of cellular wireless standards, the on-air signals themselves are also experiencing significant transformations [13]. The characteristics of those signals are ultimately responsible for the performance and cost of the fundamental hardware, particularly the power amplifier. While 2G signals are low-order and possess low peak-to-average power ratios (PAPR), the higher data rates in 3G+ systems are accomplished with higher-order and larger PAPR (and even wider band) signals. In addition to increasing the peak power requirements for specific average power (or conversely, reducing the av-

erage power for a given peak power capability), large PAPR signals significantly affect the *average* energy efficiency of the power amplifier. This is due to traditional designs being most efficient only at the peak power levels while those signals incite them to operate in "average" at much lower output power levels where they are significantly less efficient. In addition, the higher-order of these more complex modulations increases the linearity requirements of the radio access equipment, especially again, the power amplifier. While a minimum amount of linearity is strictly specified by communications standards (employing several figures-of-merit for in-band and out-of-band linearity), the minimum energy efficiency is not specified but substantially affects the economics and environmental footprint of the communication systems, as discussed earlier.

Fig. 1.3 illustrates in detail the impact of modulated signals on the average efficiency and linearity of amplifiers by utilizing, as an example, a classical single-branch amplifier (e.g. class-B) and a W-CDMA test signal [14]. Fig. 1.3a plots the instantaneous output power P_{out} and ideal drain-efficiency η_{DE} versus the input power P_{in} of this amplifier along with a sample of the time-domain modulated signal (squared and scaled with a vertical time axis). Note that, for linear amplification, all signal levels must remain inside the linear region of the amplifier (including the infrequent peaks) whereby, consequently, the "average" signal stays in deep power back-off (depending on the PAPR) with a corresponding, much lower average efficiency $\eta_{DE,avg}$ than what is maximally possible for the instantaneous signal (i.e., $\eta_{DE,max}$). In Fig. 1.3a two cases are indicated: the linear (marked with ①) and the nonlinear case (marked with ②). In the first case, the signal is maintained within the linear response of the amplifier while, in the second case, it is allowed to experience limited compression in order to increase the average efficiency. An alternative visualization of this (provided only for the first case) is by employing the probability density function (PDF) of the signal superimposed with a plot of η_{DE} versus P_{out}, as illustrated in Fig. 1.3b. Fig. 1.3c provides the spectrum of the output signal in both cases where it can be appreciated that the nonlinear case incites spectral regrowth (in the depicted example that exceeds the minimum adjacent channel leakage power ratio $ACLR1$ specified by the 3GPP [15]). In summary, Fig. 1.3 illustrates the lower average efficiency (compared with the peak efficiency) realizable for signals with large PAPR as well as the existing trade-off between (average) efficiency and linearity in a classical single-branch amplifier.

1.4. EFFICIENCY ENHANCEMENT TECHNIQUES

Despite the differences in technologies and applications, the need to ameliorate the energy efficiency of traditional single-branch power amplifiers is actually several decades old. Various efficiency enhancement techniques have been proposed over time [1, 16] with a variety of inherent advantages and disadvantages. In general, these techniques increase the instantaneous efficiency at back-off and afford the opportunity to facilitate greater average efficiencies while maintaining linearity. Currently, the most important efficiency enhancement techniques are based on either supply-voltage modulation, such as "envelope elimination and restoration" (EER)/polar and "envelope tracking"

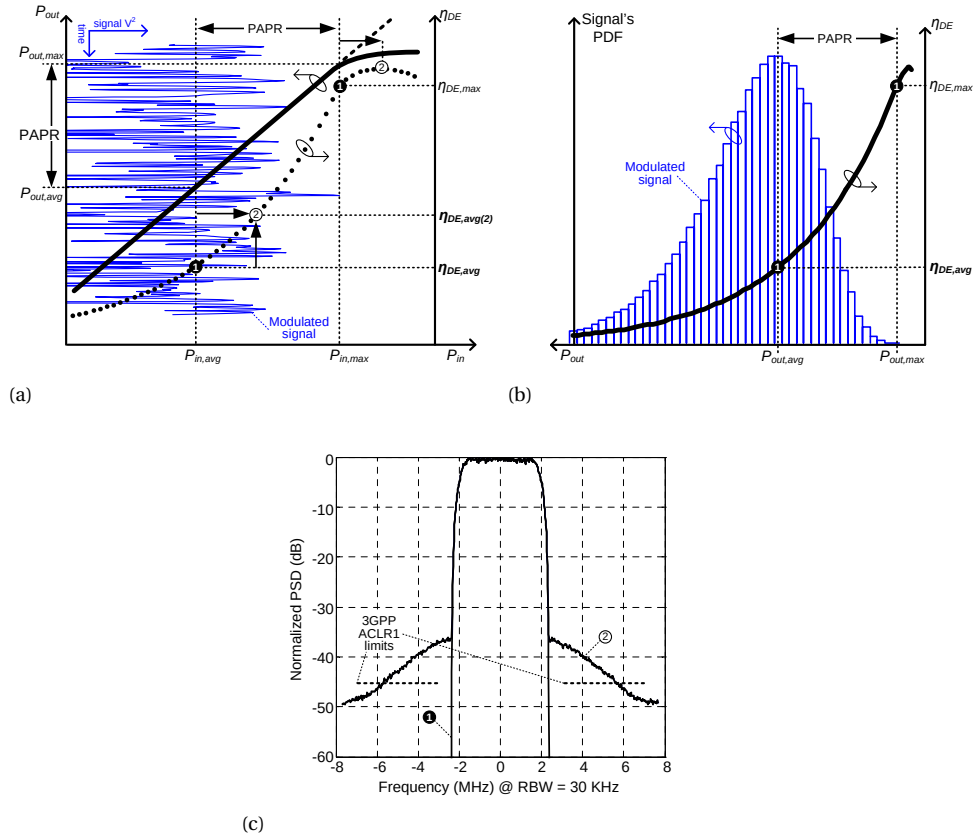

Figure 1.3: Efficiency and linearity trade-off in classical single-branch amplifiers with large PAPR signals: a) P_{out} and η_{DE} versus P_{in} with superimposed time-domain modulated signal (W-CDMA), b) η_{DE} versus P_{out} with superimposed signal's PDF, and c) corresponding spectra of a linear and nonlinear amplified signal.

(ET) [16, 17], or based on load modulation, such as Doherty [18] and outphasing [19, 20] as depicted in Fig. 1.4. Although a comprehensible description of these techniques, as well as others, can be found elsewhere [16, Ch. 10], a brief overview is provided here.

Transmitters with supply-voltage modulation vary dynamically the DC voltage of the RF amplifying stage according to the envelope of the modulated signal. This reduces the power dissipation when the signal has small levels and hence improves the average efficiency of the amplifying stage. There are two distinct versions of this approach: the envelope tracking amplifier and the EER/polar amplifier [17]. While the first version suitably operates the RF device as a current source, and the supply only "tracks" the envelope to improve efficiency, the second version operates the device nonlinearly and reconstructs the envelope at RF by tightly modulating the DC supply. Due to the less complex RF amplifying stage, these amplifiers can afford good efficiencies and large operational RF bandwidth [21, 22]. However, they require a difficult-to-implement energy-efficient sup-

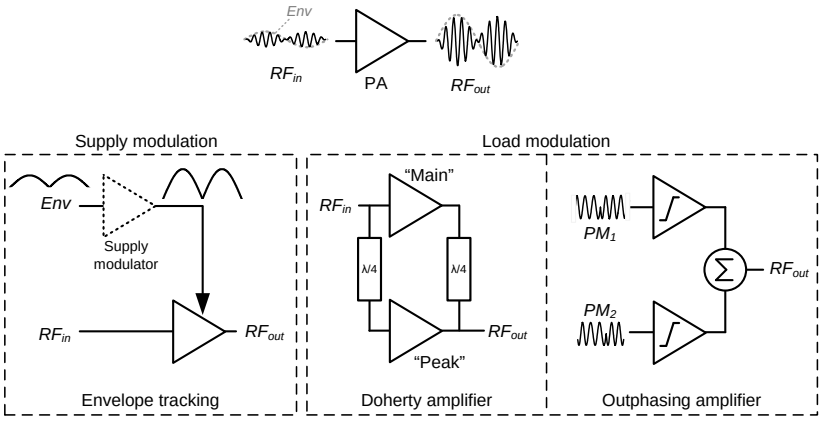

Figure 1.4: The most popular high-efficiency amplifier concepts: envelope tracking, Doherty and outphasing amplifier.

ply modulator that, in practice, severely restricts the instantaneous modulation bandwidth. Although the design of such a supply modulator is improving [23], it continues to be a very important issue for the upcoming modulation schemes that tend to occupy wider bandwidths.

The most popular amplifier topologies based on load modulation are the Chireix outphasing amplifier and the Doherty amplifier. These were proposed in the mid-1930s by H. Chireix [19] and W.H. Doherty [18], respectively, to improve the efficiency of shortwave broadcast stations. They are both based on what is now known as active load-pull which basically indicates that the behavior of each constitutive amplifying branch is affected (via its load) by the amplifier in the other branch. However, the basic operation and control of both the Doherty and the outphasing amplifiers are different, as detailed later in Chapter 3.

The Doherty amplifier is currently the preferred workhorse in base station power amplifiers and comprises (in its simplest form) two amplifying branches, i.e., the "main" and the "peak". The main amplifier operates continuously while the peak amplifier operates only at peak power levels (when working, the latter keeps the main amplifier in saturation and saves power when turned off). The Doherty concept is a cost-effective technique with good efficiency [24], however, traditionally suffers from a narrow operational RF bandwidth (due to the applied design techniques and impedance inverter) and the requirement for linear PAs in the branch amplifiers. Although the first issue is being actively addressed [25,26], the latter requirement often results in a lower achievable peak efficiencies.

The outphasing amplifier has a radically different approach to efficient power amplification by enabling linear amplification utilizing nonlinear components (also referred to as LINC [27]). In principle, it employs two highly efficient, yet nonlinear, branch amplifiers that are driven by phase-modulated signals ($PM_{1,2}$ in Fig. 1.4). Following its vector addition, amplitude modulation is subsequently accomplished by the precise

control of the differential phase between these signals. While high efficiency is accomplished due to the nonlinear amplifying branches, which is different from Doherty and supply-voltage modulation, the linearity of the outphasing amplifier does not rely on the constitutive individual PAs but, rather, on the integrity of the required amplitude to phase conversion [16, Ch. 10.4] which can currently be accurately controlled at baseband. Although the outphasing amplifier has generally been less popular, it has recently been regaining much attention due to its potential superior efficiency and linearity performance as well as to advances in high-speed and low-power digital signal processing. In addition, it can be broadband [28, 29], reconfigurable/multi-mode [30, 31] and can potentially bridge the gap between the high power analog and digital domains enabling higher integration [28, 32]. Because of its potential and historical insufficient practical and competitive implementations, this technique forms a central element in this thesis, and subsequent chapters will delve further into its design and implementation aspects.

Along with the development of efficient amplifier concepts, the active devices themselves have also improved. Over the last decade, the silicon laterally diffused metal-oxide-semiconductor transistor (Si LDMOS) has been the primary technology of choice for RF high-power amplifiers, notably in radio base stations, due to its ruggedness and competitive price [33]. However, recently, this dominance is being challenged by wide-bandgap semiconductors such as gallium-nitride high-electron-mobility transistors (GaN HEMTs) [34] whose material properties such as increased breakdown voltages and junction temperatures (that translate in greater power densities) have enabled RF amplifiers with even higher performance levels. In this thesis, GaN HEMT is the technology of choice to target the highest possible performance for the aimed circuit demonstrators.

1.5. THESIS OBJECTIVES

The focus of this thesis is on improving the energy efficiency and physical form-factor of high-power amplifiers for base station applications. In particular, there are two primary research objectives addressed in this thesis:

- Development of low-cost design techniques intended for physically compact high-power amplifiers with improved efficiency and bandwidth performance. These include the design of passive elements, package-integration, and CMOS drivers for advanced power amplifier functionalities.

- Advance the state-of-the-art in outphasing power amplifiers to improve efficiency while meeting stringent linearity requirements.

Regarding the first objective, reducing the physical size and weight of power amplifiers enables more energy-efficient radio access equipment by bringing the amplifiers closer to the radiating antenna elements (and thus significantly reduces the high losses due to the traditionally used co-axial feeders, as illustrated in Fig. 1.2), enabling new system configurations utilizing "remote radio heads" and "smart antennas". Regarding the second objective, practical outphasing amplifier implementations for base stations have

been rather limited in performance and the rather limited number of published results indicates the opportunity for making new contributions in this field. Hence, there is an important academic and industrial interest for publishing and demonstrating the efficiency performance of outphasing amplifiers as a future alternative for power amplification in wireless infrastructure applications.

1.6. THESIS OUTLINE

The following chapters of this thesis can be grouped into two parts that discuss several aspects in regard to the main objectives described above. They are organized as outlined in Fig. 1.5.

The first part comprises Chapters 2 to 4. Following the brief introduction given earlier in Section 1.4, Chapter 2 reviews the fundamentals of outphasing amplifiers in more detail and briefly describes recent developments published in literature. Chapters 3 and 4 provides a detailed system-level perspective for the most popular highly-efficient amplifiers based on load modulation. In particular, Chapter 3 describes the design and efficiency performance of both Chireix outphasing and Doherty amplifiers with both class-B and class-E branch amplifiers when utilizing signals with large PAPR like W-CDMA. Chapter 4 complements this system-level analysis with a discussion on bandwidth expansion in the branch signals of those amplifiers, in particular the ideal outphasing amplifier.

The second segment of this thesis comprises Chapters 5 to 8 which are focused on compact power amplifier design and implementation. Chapter 5 describes the design of low-loss and high-current inductive passive elements for high-power amplifiers, specifically inductors and transformers, employing low-cost bondwire technologies. This forms the foundation for integrating the power amplifier inside an otherwise standard transistor package. Chapter 6 presents the design, implementation, and measurements of two switch-mode power amplifier examples intended for package-integration. These amplifiers are based on GaN HEMTs operating in class-E with broadband performance. Chapter 7 consolidates the design techniques described in earlier chapters and delineates the design, implementation, and measurements of a state-of-the-art GaN HEMT Chireix outphasing amplifier implemented inside an otherwise standard transistor package. This amplifier demonstrates, in practice, the achievement of the two primary objectives of this thesis. Chapter 8 presents the design of high-voltage CMOS drivers for switch-mode high-power amplifiers based on wide-bandgap compound semiconductors such a GaN HEMT. As demonstrated by the practical examples referred to in this chapter, the inclusion of CMOS to directly drive GaN HEMTs opens up several opportunities to improve overall amplifier performance and facilitates even greater integration levels for next generation amplifiers.

Finally, Chapter 9 summarizes the main conclusions of this thesis and provides recommendations for further research.

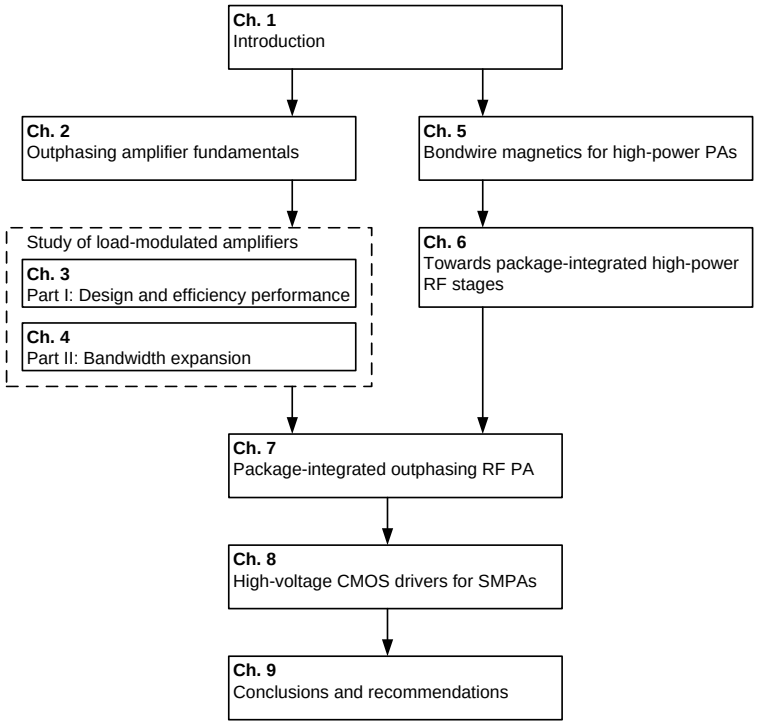

Figure 1.5: Outline of this thesis.

2

OUTPHASING AMPLIFIER FUNDAMENTALS

2.1. INTRODUCTION

The original outphasing transmitter concept [19] encodes arbitrary amplitude and phase modulation on a carrier wave by using only phase modulation, as depicted in the equivalent phasor representation of Fig. 2.1. The main idea of this technique is that a complex modulated signal can be decomposed into two constant envelope signals whose differential and common phases contain the original amplitude and phase information, respectively. If these two signals are combined (after individual RF up-conversion and amplification), the resulting signal is an amplified envelope-equivalent replica of the original input signal.

This technique was originally proposed by H. Chireix [19] in the 1930's to improve the efficiency and linearity of AM-broadcast transmitters. Later, it was also termed "LINC" (linear amplification using non-linear components) [27] because highly-efficient although

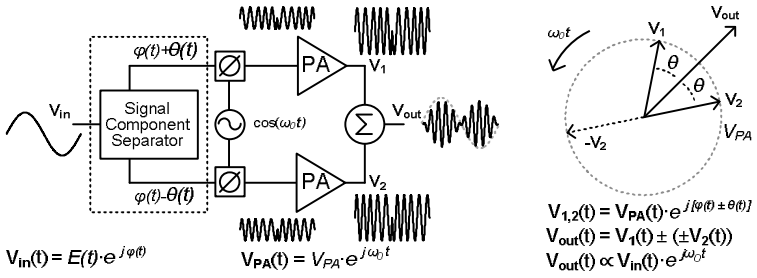

Figure 2.1: Outphasing amplifier concept [19, 20] and equivalent phasor representation.

non-linear amplifiers can be used while still providing linear amplification.

This chapter describes the fundamentals of the outphasing amplifier. First, basic aspects are described such as ideal outphasing modulation and efficiency performance. Then, different outphasing combining strategies are reviewed from published literature. Finally, for completeness, a short discussion on the main non-idealities of this amplifier is also provided. Next chapter will focus on other specific aspects of the design of this amplifier topology when using different classes of operation for the branch amplifiers.

2.2. OUTPHASING MODULATION

The basic outphasing modulation principle can be analytically described as follows. At a carrier frequency ω_0, a complex modulated signal $S_{in}(t)$, with envelope $E(t)$ and phase $\varphi(t)$ is proportional to the vector addition of two constant-amplitude signals $S_{1,2}(t)$ according to

$$S_{in}(t) = E(t) \cdot \cos\left(\omega_0 t + \varphi(t)\right) \tag{2.1}$$

$$S_{out}(t) = [S_1(t) + S_2(t)] \propto S_{in}(t) \tag{2.2}$$

$$S_{1,2}(t) = \cos\left(\omega_0 t + \varphi(t) \pm \theta(t)\right) \tag{2.3}$$

where $S_{out}(t)$ represents the output of an outphasing transmitter and $S_{1,2}(t)$ are the (normalized) phase-modulated signals at the output of the two branch amplifiers of this transmitter[1]. $\theta(t)$ is called the *outphasing angle* and for the ideal case of (2.1)-(2.3) it is given by $\theta(t) = \arccos\left(\overline{E(t)}\right)$. In fact, (2.2) is a special case of the following trigonometric identities[2]:

$$\cos\left(\omega_0 t + \varphi(t) + \theta(t)\right) \pm \cos\left(\omega_0 t + \varphi(t) - \theta(t)\right) = 2 \cdot \begin{matrix}\cos \\ \sin\end{matrix}(\theta(t)) \cdot \begin{matrix}\cos \\ \sin\end{matrix}\left(\omega_0 t + \varphi(t)\right) \tag{2.4}$$

These equations indicate that the equal-magnitude signals $S_{1,2}(t)$ can be added or subtracted (i.e., vector summed) in order to control the magnitude of the resultant signal through the outphasing angle $\theta(t)$. Therefore, according to (2.4), this angle is then given by

$$\theta(t) = \begin{cases} \arccos\left(\overline{E(t)}\right), & \text{for additive combining} \quad (2.5a) \\ \arcsin\left(\overline{E(t)}\right), & \text{for substractive combining} \quad (2.5b) \end{cases}$$

[1] If $S_{in}(t)$ is a baseband signal, then it is first split into two signals that are then RF up-converted to become $S_{1,2}(t)$.

[2] Further combinations are possible if any $S_{1,2}(t)$ are sine instead of cosine phasors.

or, equivalently by (where the choice of the sine function, instead of cosine, is arbitrary)

$$\theta(t) = \arcsin\left(\overline{E(t)}\right) + \theta_{offset} \tag{2.6}$$

$$\theta_{offset} = \begin{cases} -\pi/2, & \text{for additive combining} \quad (2.7a) \\ 0, & \text{for subtractive combining} \quad (2.7b) \end{cases}$$

Since $S_{1,2}(t)$ in (2.3) are constant-envelope signals, they can be viewed as the outputs of highly efficient switching power amplifiers. Despite the nonlinear nature of these amplifiers, $S_{out}(t)$ in (2.2) is a perfectly linear amplified replica of $S_{in}(t)$ if $\theta(t)$ properly encodes $E(t)$. So ideally, and different from Doherty and envelope tracking transmitters, the linearity of the outphasing transmitter does not depend on the constitutive branch amplifiers themselves but rather on the integrity of the branch signal decomposition or amplitude to phase conversion [16, Ch. 10.4], represented here by (2.6) and (2.7), which can be done accurately at baseband.

In addition, the outphasing modulation is not limited to only two vectors. In principle, for equal-magnitude vectors, any even number of vectors can control the amplitude of the resultant with infinite dynamic range. For example, the outphasing operation with 4 vectors can be described using the following expression (which uses (2.4) twice):

$$\begin{aligned} &\cos\left(\omega_0 t + \phi_1(t)\right) + \cos\left(\omega_0 t - \phi_1(t)\right) + \cos\left(\omega_0 t + \phi_2(t)\right) + \cos\left(\omega_0 t - \phi_2(t)\right) \\ &\qquad = 4 \cdot \underbrace{\cos\left(\frac{\phi_1(t) + \phi_2(t)}{2}\right)\cos\left(\frac{\phi_1(t) - \phi_2(t)}{2}\right)}_{\text{Amplitude control}} \cdot \cos(\omega_0 t) \end{aligned} \tag{2.8}$$

where $\varphi(t)$ was ignored and only additive combining was considered for simplicity. In this case there are two outphasing angles $\phi_{1,2}(t)$ and linear amplification is accomplished when both $\phi_{1,2}(t)$ map properly $\overline{E(t)}$ (i.e. $\phi_{1,2}(t) = f_{1,2}(\overline{E(t)})$, which has many solutions). Recently, a specific example of a 4-way outphasing system using a non-isolating power combiner was proposed in [35,36] and was demonstrated at RF in [37–39]. Having additional outphasing vectors can lead in principle to higher efficiencies at the cost of increased complexity (in both power combining and signal processing) [36]. This thesis, however, concentrates in two-way outphasing amplifiers and its practical implementations.

2.3. EFFICIENCY AND POWER FACTOR

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The efficiency of an outphasing amplifier depends on mainly three aspects: the power combiner, the operating class of the branch amplifiers and the specific driving signals. Different choices on these aspects lead to distinct outphasing amplifiers with different efficiency performances. This section proposes a generalization of the analytical expression for drain-efficiency in ideal outphasing amplifiers regardless of their operating class. This expression is derived from basic principles and justifies formally the subsequent analysis of several power combiners separated from the branch amplifiers.

The *total* drain-efficiency η_{DE_N} for N sources such as power amplifiers (PAs) combining their powers in a lossless manner can be defined as the ratio of the *total* RF power $\sum P_{out_n}$ at the fundamental frequency to the *total* DC power $\sum P_{DC_n}$ of the sources, this is

$$\eta_{DE_N} = \frac{\sum_{n=1}^{N} P_{out_n}}{\sum_{n=1}^{N} P_{DC_n}} \tag{2.9}$$

where the sub-index $_n$ refers to the n-source. In turn, each P_{out_n} can be defined in terms of fundamental currents and voltages, or even admittances (or impedances), as

$$P_{out_n} = \frac{1}{2}\mathbf{Re}\{\mathbf{V_n} \cdot \mathbf{I_n^*}\} = \frac{1}{2}|\mathbf{V_n}|^{\mathbf{2}} \cdot \mathbf{Re}\{\mathbf{Y_n}\} \tag{2.10}$$

$$P_{DC_n} = V_{DC_n} \cdot I_{DC_n} = \left(\frac{V_{DC_n}}{|\mathbf{V_n}|}\frac{I_{DC_n}}{|\mathbf{I_n}|}\right) \cdot |\mathbf{V_n}|^{\mathbf{2}} \cdot |\mathbf{Y_n}| \tag{2.11}$$

where the sub-index $_\mathbf{n}$ refers to the fundamental voltage, current or admittance of each n-source. In the ideal outphasing PA concept, the amplitude of the sources are considered identical and therefore, from (2.9)-(2.11), η_{DE_N} can be simplified to

$$\eta_{DE_N} = \eta_S \cdot PF_N \tag{2.12}$$

$$\eta_S = \frac{1}{2}\frac{|\mathbf{V_n}|}{V_{DC_n}}\frac{|\mathbf{I_n}|}{I_{DC_n}} \tag{2.13}$$

$$PF_N = \frac{\sum_{n=1}^{N} \mathbf{Re}\{\mathbf{Y_n}\}}{\sum_{n=1}^{N} |\mathbf{Y_n}|} \tag{2.14}$$

This is, in the ideal case, η_{DE_N} can be seen as the multiplication of two factors: a *net power factor* PF_N[3] and another factor η_S which can be regarded as an *apparent efficiency*[4]. Splitting η_{DE_N} into such two factors merely aims at developing design intuition and at analyzing separately the influence of the branch amplifiers and the power combiner in the complete outphasing amplifier. Although PF_N influences η_{DE_N} in (2.12), it shall rather be treated only as a "figure-of-merit" of the power combining process [36]. Meanwhile, η_S relates to the efficiency of the branch amplifiers and shall be regarded only as an "apparent" efficiency because it does not consider any phase difference between the delivered voltage and current. The "real" efficiency is given by η_{DE_N} which

[3] The same expression for PF_N in (2.14) was derived in [36] from loss and source utilization concepts.
[4] This name is just an analogy to the concept of *apparent power*.

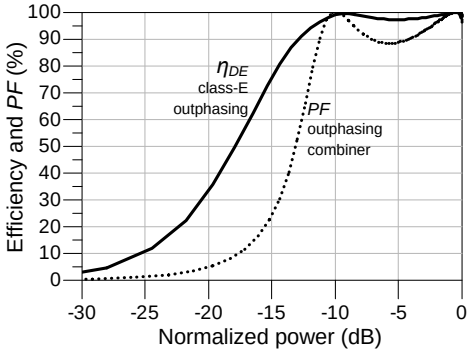


Figure 2.2: Efficiency and power factor for an ideal class-E outphasing amplifier (Chireix compensation at 10 dB back-off).

considers such a phase difference in the PF_N term that multiplies η_S. The factor η_S is actually determined by the specific PA class (and its loading conditions) and, in this context, it can enhance ($\eta_S > 1$) or worsen ($\eta_S < 1$) the total η_{DE_N} with respect to PF_N, as explained next.

The maximum theoretical efficiency of the ideal linear amplifier classes A, AB, B and C depends only on their conduction angle α [16, Ch. 3.2]. For them, η_S is therefore constant and a function of α because their fundamental voltage amplitude equals the DC voltage supply ($|\mathbf{V_n}| = V_{DC_n}$) and their fundamental current is proportional to the DC current ($|\mathbf{I_n}|/I_{DC_n} = f(\alpha)$[5]). Therefore, the η_{DE} of an outphasing amplifier with ideal class-B branch amplifiers is just a $\frac{\pi}{4}$-scaled version of the net power factor of its combiner since $\eta_{S,\text{class B}} = \frac{\pi}{4}$ [20, 36]. However, there are cases and specific conditions where the η_{DE_N} of an amplifier can in fact be larger than the PF_N of its own combiner. For example, the η_S of an ideal class-E amplifier is not necessarily constant since it depends on its (instantaneous) load, primarily due to the $|\mathbf{I_n}|/I_{DC_n}$ term (since $|\mathbf{V_n}|/V_{DC_n}$ remains constant)[6]. For an specific class-E termed "load-insensitive" [28], described in detail later in Subsection 7.2.2 [29, Sec. II-C], $\eta_{S,\text{class E}}$ varies during the outphasing load excursion such that $\eta_{S,\text{class E}} \approx 1$ at 0 dB while $\eta_{S,\text{class E}} > 1$ at deeper back-off levels (e.g., after 10 dB). This effectively enhances the overall amplifier's η_{DE} as depicted in Fig. 2.2. Although no formal explanation was provided previously, this enhanced outphasing PA efficiency was first indicated by [40] which reported a notably higher efficiency at deep back-off levels when using class-E PAs compared to class-B.

[5] From [16, Eqs. (3.2) - (3.3)], $|\mathbf{I_n}|/I_{DC_n} = f(\alpha) = \frac{\alpha - \sin(\alpha)}{2\cdot\sin(\alpha/2) - \alpha\cdot\cos(\alpha/2)}$. Therefore, for class-B amplifiers $\alpha = \pi$ and hence $|\mathbf{I_n}|/I_{DC_n} = \frac{\pi}{2}$.

[6] Since a complete analytical expression for $\eta_{S,\text{class E}}$ is rather complex and not the goal of this thesis, it is only used here for a qualitative discussion.

2.4. OUTPHASING WITH ISOLATING COMBINERS

In the outphasing amplifier, the output power from the individual branch amplifiers can be combined by using either an isolating or a non-isolating combiner. This choice leads to many different practical approaches to outphasing amplifiers with various levels of performance and complexity. This section will briefly review first outphasing PAs using (lossy) isolating power combiners and then outphasing PAs with (lossless) non-isolating power combiners.

Outphasing amplifiers using isolating power combiners are generally referred to as "linear amplification using non-linear components" or simply LINC amplifiers [27]. Since these combiners "isolate" both branch amplifiers from each other, the impedances seen by them are constant during the outphasing modulation. This in principle preserves linearity [41] but compromises efficiency because the isolation comes at the cost of adding a lossy element to the combining network. Fig. 2.3 illustrates two examples using voltage sources to represent the branch amplifiers with two different power combiners, namely, the Wilkinson combiner and the quadrature hybrid combiner. For these two cases, the input port isolation is accomplished when the characteristic impedance of the transmission lines and the isolating resistor R_{iso} are properly dimensioned, as specified in the figure.

When using isolating combiners, the isolating resistor R_{iso} consumes all the power that is not delivered to the final load. In fact, the efficiency of this combining strategy reduces linearly with back-off power. This can be seen after calculating the dissipated power P_{iso} and the desired output power P_{out} from the circuits in Fig. 2.3. For example, for the Wilkinson combiner in Fig. 2.3a these are

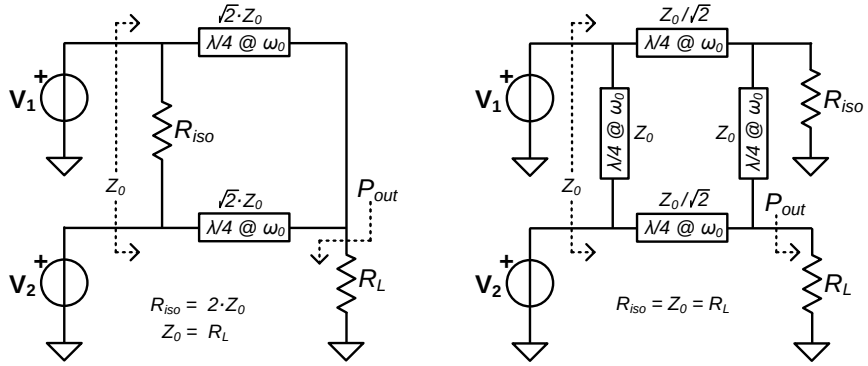
$$P_{out} = P_{out,max} \cdot \cos^2(\theta(t)) \tag{2.15}$$

$$P_{iso} = P_{out,max} \cdot \sin^2(\theta(t)) \tag{2.16}$$

and therefore a normalized efficiency η_{iso}, representing the instantaneous ratio from output power and total power (independent to the efficiency of the branch amplifiers), can be given as

$$\eta_{iso} = \frac{P_{out}}{P_{out} + P_{iso}} = \cos^2(\theta(t)) = \frac{P_{out}}{P_{out,max}} \tag{2.17}$$

Note that when using these isolating and lossy combiners, the power factor is always unity and of little use. Instead, the efficiency of those combiners can be described by η_{iso}. It is also interesting to realize that the efficiency described by (2.17) is much lower at all levels of back-off when compared with the one of a simpler stand-alone class-B amplifier (also normalized, i.e. $\overline{\eta_{DE,B}} = \eta_{DE,B}/(\pi/4)$). This is because the latter has a squared-root relationship with back-off power (since the DC-power reduces also with back-off) instead of the linear relationship given by (2.17). These two cases are depicted in Fig. 2.5.



(a) (b)

Figure 2.3: Outphasing with isolating power combiners: a) with a Wilkinson combiner, b) with a hybrid combiner.

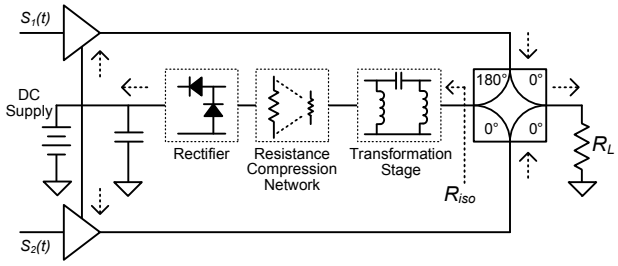


Figure 2.4: Outphasing with power recovery (from [42] © 2009, IEEE.).

A few techniques have been developed to overcome the severe efficiency degradation at back-off when using these isolating combiners, which are described next. Although interesting, they all have important drawbacks and have not proven yet to be better, from the efficiency point of view, than other outphasing amplifiers using non-isolating combiners, which in turn will be described afterward.

2.4.1. OUTPHASING WITH POWER RECOVERY

The efficiency of the LINC amplifier can be improved if the power dissipated in R_{iso} could be recovered. The work in [43] proposed a power recycling technique in which the isolation resistor R_{iso} of the hybrid combiner in Fig. 2.3b is replaced with an RF-DC converter to recover the otherwise wasted power P_{iso} back to the DC-power supply, as depicted in Fig. 2.4. The former (2.17) can be modified to account for a given energy recovery efficiency η_{rec}, resulting in the following expression [42]

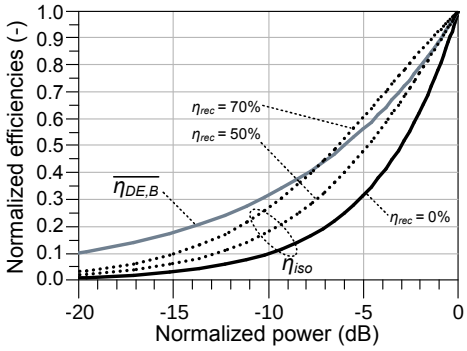


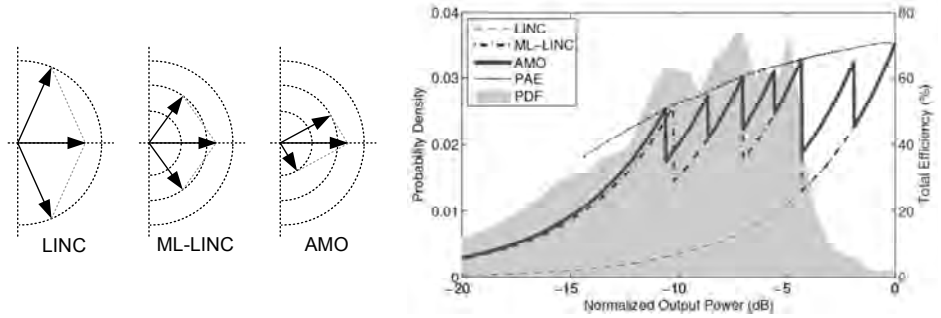
Figure 2.5: Efficiency versus back-off of the outphasing amplifier with power recovery [42]. The normalized drain-efficiency of a stand-alone class-B amplifier ($\overline{\eta_{DE,B}}$) is plotted for reference.

$$\eta_{iso} = \frac{P_{out}}{P_{out} + \left(1 - \eta_{rec}\right) P_{iso}} \tag{2.18}$$

Fig. 2.5 illustrates this equation for η_{iso} versus back-off power for several η_{rec} efficiencies (0 , 50 and 70%) along with the normalized efficiency for a stand-alone class-B amplifier for comparison. Practical implementations of this technique suffer from losses and other effects that limit its actual effectiveness. For example, the implementation in [43] achieves about 50% of energy recovery at 1.96 GHz. A more recent implementation described in [42] improves the RF-DC conversion by adding a resistance-compressed rectifier, shown at the middle of Fig. 2.4. This latter topology reduces the impedance variation seen in practice at the isolation port (which in turn reduces the isolation between the branch amplifiers and therefore degrades both efficiency and linearity of the entire amplifier) by using a resistance compression network [44]. The work in [42] demonstrated about 70% of energy recovery but only at 48 MHz.

2.4.2. MULTILEVEL LINC AMPLIFIERS

The multilevel LINC amplifier [45–47] improves the efficiency of the basic LINC amplifier by incorporating a simplified supply modulator for performing a discrete envelope tracking. In this amplifier, the supply voltage of the branch amplifiers can be switched between multiple discrete levels in order to track the envelope and hence reduce the power losses at back-off. If the supply levels are equal at all times for the two branches, this technique is simply referred to as ML-LINC [46]. A variant of this architecture allows unequal DC-supply levels for the individual branches [45, 47] and is mostly known as “asymmetric multilevel outphasing” (AMO) [45, 48–50]. These multilevel LINC amplifiers are compared in Fig. 2.6 (reproduced from [45]). By making independent changes in the DC supplies of each branch amplifier (limited in practice to either adjacent or equal



(a) (b)

Figure 2.6: Comparison of several multilevel LINC amplifiers (LINC, ML-LINC and AMO): a) baseband vector representation, and b) practical efficiencies including the effect of supply voltage back-off on the *PAE* and the PDF of a WLAN signal for reference (from [45] © 2009, IEEE.).

levels), the AMO technique results in smaller outphasing angles and hence higher efficiency when compared to using only the isolating combiner, as can be observed in Fig. 2.6b. Different from a truly polar/envelope tracking system that requires a (normally inefficient) wideband and linear PA for controlling the supply, these architectures employ more efficient DC-DC converters.

2.5. OUTPHASING WITH NON-ISOLATING COMBINERS

When a non-isolating power combiner is employed, the two branch amplifiers interact with each other during the outphasing operation and hence their *dynamic* loads are dependent on each other. During operation, this load is modulated according to the outphasing angle and hence power is controlled. If this active load modulation is properly utilized, it can lead to significant efficiency improvements. As described in Section 2.3, the efficiency can be assessed by means of the net power factor in (2.14). For an ideal two-way outphasing amplifier, the power factor is given by

$$PF = \frac{\mathbf{Re}\{\mathbf{Y_1}\} + \mathbf{Re}\{\mathbf{Y_2}\}}{|\mathbf{Y_1}| + |\mathbf{Y_2}|} \tag{2.19}$$

where the fundamental admittance load $\mathbf{Y_{1,2}}$ seen by each branch amplifier is *dynamic* with modulation. During the outphasing modulation, the modulated loads $\mathbf{Y_{1,2}}$ present an unwanted and varying reactive loading that reduces the power factor of the combiner and hence the overall amplifier's efficiency at back-off. In a seminal paper [19], Chireix proposed adding a pair of opposite and fix reactive elements between the sources and the combiner in order to minimize such unwanted reactance. This in turn increases efficiency by increasing the net power factor of the combiner. Since then, this is the most

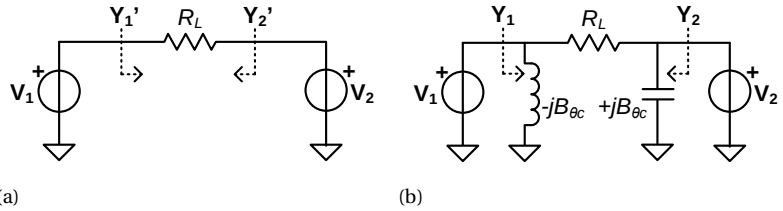


Figure 2.7: Outphasing power combiner with voltage sources: a) basic voltage-source combiner, b) voltage-source combiner with Chireix compensation.

commonly used efficient implementation of outphasing amplifiers that are referred to as Chireix outphasing amplifiers due to his proposed compensation. Next is a description of the basic combiners of this type and their practical implementations.

2.5.1. FUNDAMENTAL CHIREIX COMBINERS

The most basic non-isolating power combiners with Chireix compensation are depicted in Figs. 2.7 and 2.8, when the branch amplifiers are assumed to behave as voltage and current sources, respectively.

Assuming that the voltage sources of the circuit in Fig. 2.7 are phase-modulated vectors $v_{1,2}(t) = V_{PA} \cdot e^{\pm j\theta(t)}$ with arbitrary amplitude V_{PA}, then the *dynamic* admittance load $\mathbf{Y_{1,2}}$ seen by each voltage source is given by [16, 20]

$$\mathbf{Y_{1,2}}(\theta(t)) = G(\theta(t)) \pm j\left[B(\theta(t)) - B_{\theta c1,2}\right] \tag{2.20}$$

$$G(\theta(t)) = \left(\frac{1}{R_{PA}}\right)\sin^2(\theta(t)) \tag{2.21}$$

$$B(\theta(t)) = \left(\frac{1}{R_{PA}}\right)\frac{\sin(2\cdot\theta(t))}{2} \tag{2.22}$$

$$B_{\theta c1,2} = B\left(\theta_{c1,2}\right) \tag{2.23}$$

where $R_{PA} = \frac{R_L}{2}$ is the load seen by each voltage source (or amplifier) at full power, $G(\theta(t))$ and $B(\theta(t))$ are the real and imaginary parts of the *dynamic* complex (admittance) load, respectively, $\theta_{c1,2}$ and $B_{\theta c1,2}$ are the Chireix compensating angles and susceptances for branch 1 and 2, respectively. The output power across the floating resistor R_L is given by

$$P_{out}(t) = \frac{V_{PA}^2}{R_{PA}}\sin^2(\theta(t)) \tag{2.24}$$

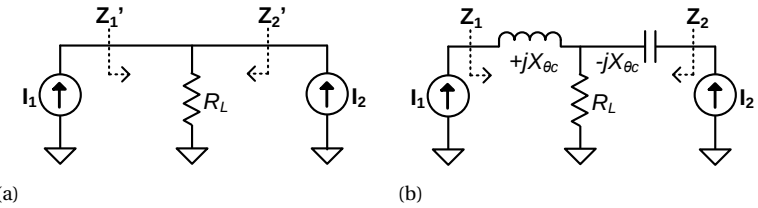


Figure 2.8: Outphasing power combiner with current sources: a) basic combiner, and b) with Chireix compensation.

and therefore maximum power is attained when the voltage sources $v_{1,2}(t)$ are out of phase, this is $\theta(t)|_{P_{out,max}} = \frac{\pi}{2}$, as can be also appreciated by a simple inspection of the circuit in Fig. 2.7. This combiner is actually an example of a "subtractive" combining network according to (2.5), and therefore $\theta(t)$ is given by (2.6) and (2.7b).

The circuit in Fig. 2.8 is the dual of the circuit in Fig. 2.7. This current-based combiner is an example of an "additive" combining network and therefore maximum power will be reached when the phase-modulated current vectors $i_{1,2}(t) = I_{PA} \cdot e^{\pm j\theta(t)}$ are in phase, this is $\theta(t)|_{P_{out,max}} = 0$. In this case, $\theta(t)$ is given by (2.6) and (2.7a), and the *dynamic* impedance load $\mathbf{Z_{1,2}}$ seen by each current source is given by

$$\mathbf{Z_{1,2}}(\theta(t)) = R(\theta(t)) \mp j\left[X(\theta(t)) - X_{\theta c1,2}\right] \tag{2.25}$$

$$R(\theta(t)) = R_{PA} \cdot \cos^2(\theta(t)) \tag{2.26}$$

$$X(\theta(t)) = R_{PA} \cdot \frac{\sin(2 \cdot \theta(t))}{2} \tag{2.27}$$

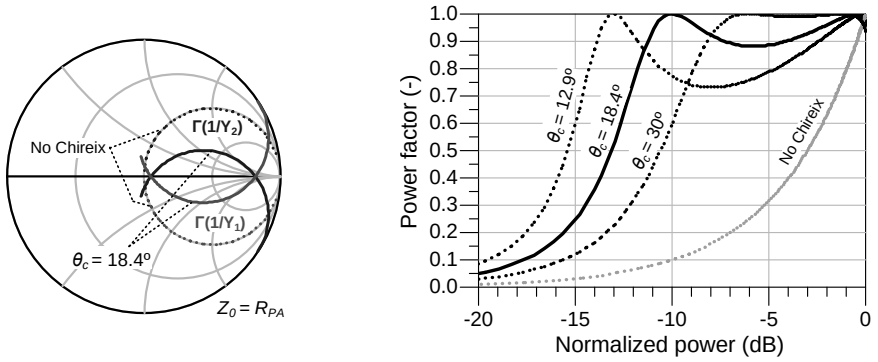
$$X_{\theta c1,2} = X\left(\theta_{c1,2}\right) \tag{2.28}$$

where now $R_{PA} = 2 \cdot R_L$ which is also the load seen by each current source at full power, $R(\theta(t))$ and $X(\theta(t))$ are the real and imaginary parts of the *dynamic* complex (impedance) load, respectively, and $X_{\theta c1,2}$ are the Chireix compensating reactances for branch 1 and 2, respectively. The output power across the shunt resistor R_L is given by

$$P_{out}(t) = I_{PA}^2 \cdot R_{PA} \cdot \cos^2(\theta(t)) \tag{2.29}$$

2.5.2. CHIREIX COMPENSATION

The Chireix compensation elements $B_{\theta c1,2}$ and $X_{\theta c}$ minimize the effects of the unwanted dynamic reactive load-modulation $B(\theta(t))$ and $X(\theta(t))$ seen by each branch voltage and current source, respectively, due to the outphasing mechanism. At certain back-off power levels, or equivalently "outphasing angles", $B_{\theta c}$ nulls $B(\theta(t))$ in (2.20) and $X_{\theta c}$ nulls $X(\theta(t))$



(a) (b)

Figure 2.9: Illustration of the efficiency improvement by adding the Chireix compensation: a) load-$\Gamma\left(1/\mathbf{Y_{1,2}}\right)$ loci in the Smith chart and b) power factor versus normalized output power without and with compensation at 6, 10 and 13 dB back-off (or, equivalently, at 12.9°, 18.4° and 30°).

in (2.25), maximizing the power factor and hence the efficiency. This improvement is illustrated in Fig. 2.9 for the circuit in Fig. 2.7b. In Fig. 2.9a, the dynamic load-$\Gamma\left(1/\mathbf{Y_{1,2}}\right)$ loci is depicted without and with compensation (at 10 dB back-off power or equivalently at a compensating angle of about 18.4°) in the impedance Smith chart. Furthermore, Fig. 2.9b shows the corresponding power factor versus normalized output power for several compensation conditions. From these figures, it can be visualized that bringing the load-$\Gamma\left(\mathbf{1/Y_{1,2}}\right)$ loci near the real axis by means of $B_{\theta c1,2}$ increases the power factor at back-off. The specific Chireix compensating angles θ_c (or directly the corresponding elements $B_{\theta c}$) are chosen to maximize the *average* efficiency of the amplifier under operation with a given *modulated* signal. This maximization considers the specific characteristics of the signal of interest such as its probability density function (PDF) and sets the compensation accordingly.

2.5.3. PRACTICAL IMPLEMENTATIONS OF CHIREIX COMBINERS

The previous Chireix combiners in Fig. 2.7 and Fig. 2.8 are normally implemented either with transmission lines or with transformers. In general, it is preferable to have the final load single-ended and that branch amplifiers themselves behave as voltage sources.

Transmission line-based outphasing combiners [40, 51–53] employ a pair of quarter wavelength transmission lines (QWTL) that connect the two branch amplifiers to a single-ended load, as depicted in Fig. 2.10. The Chireix compensation are lumped or distributed elements [51, 53] or even incorporated in the combiner itself [40, 52]. Note that the circuit in Fig. 2.10 is an "additive" combining network, similar to the network depicted previously in Fig. 2.8b, and therefore maximum power is reached when the source vectors are in phase, $\theta(t)|_{P_{out,max}} = 0$. In this case, however, such vectors are "volt-

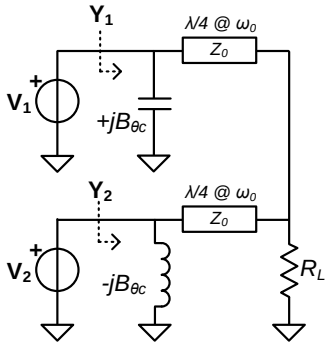


Figure 2.10: Chireix outphasing with transmission lines-based power combiner.

age sources" $v_{1,2}(t) = V_{PA} \cdot e^{\pm j\theta(t)}$ and the Chireix elements are shunted because of the impedance inversion caused by the QWTLs. For this combiner, the dynamic admittance $\mathbf{Y_{1,2}}$ is given by

$$\mathbf{Y_{1,2}}(\theta(t)) = G(\theta(t)) \mp j\left[B(\theta(t)) - B_{\theta c1,2}\right] \tag{2.30}$$

$$G(\theta(t)) = \left(\frac{1}{R_{PA}}\right) \cdot \cos^2(\theta(t)) \tag{2.31}$$

$$B(\theta(t)) = \left(\frac{1}{R_{PA}}\right) \cdot \frac{\sin(2 \cdot \theta(t))}{2} \tag{2.32}$$

$$B_{\theta c1,2} = B\left(\theta_{c1,2}\right) \tag{2.33}$$

$$P_{out}(t) = \frac{V_{PA}^2}{R_{PA}} \cdot \cos^2(\theta(t)) \tag{2.34}$$

where $R_{PA} = \frac{Z_o^2}{2 \cdot R_L}$ is the load seen by each voltage source at full power and Z_o is the characteristic impedance of the QWTLs. Notice that (2.30)-(2.34) are similar to (2.25)-(2.29) as expected from additive combining networks, except for the duality between impedance and admittance.

The main drawback from the QWTL-based outphasing combiner in Fig. 2.10 is the bandwidth restriction caused by the QWTLs. This restriction is much more severe than the one due to the Chireix compensation elements themselves [54]. Therefore, wideband combiner implementations are based on the original floating load network shown in Fig. 2.7b. In practice, this is implemented based on transformers [28–30, 54–56] and have reported in fact larger RF bandwidths, especially at deep back-off power levels [28, 29]. Fig. 2.11 illustrate two equivalent examples of these transformer-based outphasing combiners. From simple inspection, it can be appreciated that this circuit is a "subtractive" power combining network, and therefore it is described by the same equations (2.20)-(2.24) given earlier for the circuit in Fig. 2.7. In this case, however, the load seen by each

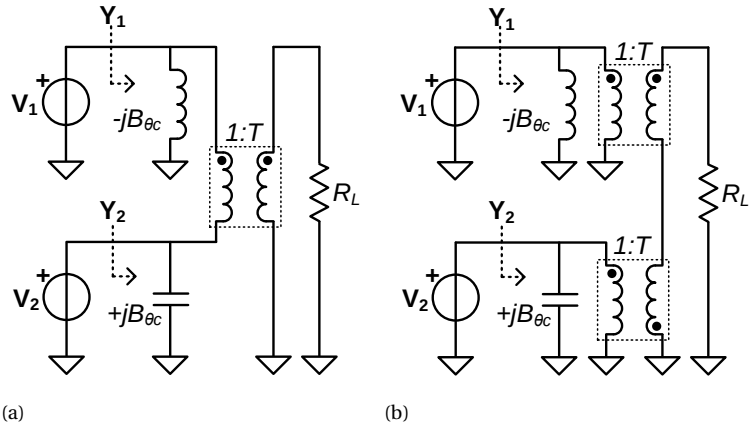


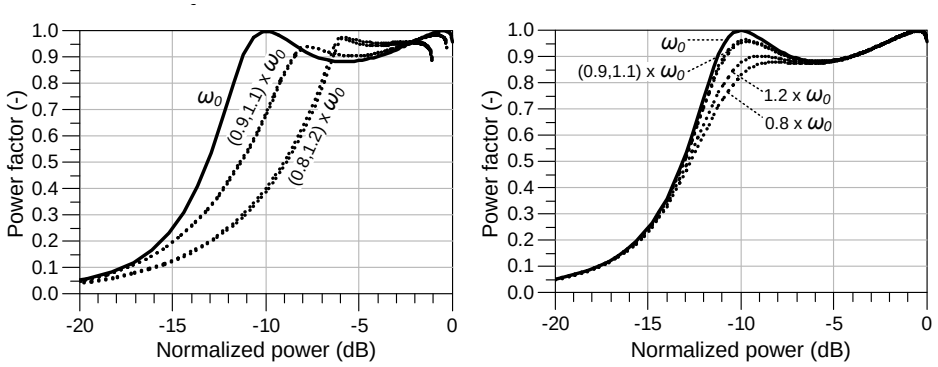
Figure 2.11: Wideband Chireix outphasing combiner using transformers: a) one transformer, b) two transformers [29].

voltage source at full power is given by $R_{PA} = \frac{1}{T^2}\left(\frac{R_L}{2}\right)$, where T is the transformer's turns ratio.

The RF operating bandwidth of the previous combiners can be examined using the net power factor in (2.19), as illustrated in Fig. 2.12. This figure shows the PF versus back-off power of the previous a) QWTL-based and b) transformer-based combiners in Fig. 2.10 and Fig. 2.11, respectively, from 0.8× to 1.2× the design frequency ω_0. For both cases, the Chireix compensation is at 10 dB back-off power and they have the same R_L and R_{PA}. Comparing the power factor responses in Fig. 2.12a with Fig. 2.12b, it becomes clear that the QWTL-based combiner is indeed more restricted in bandwidth than the transformer-based combiner.

Another transformer-based combiner using distributed elements was proposed in [28] in order to broaden up the bandwidth of the traditional QWTL-based outphasing combiner. This outphasing combiner, depicted in Fig. 2.13, is based on two coupled transmission lines (similar to a Marchand balun) and mimics the behavior of the two lumped-element transformers shown previously in Fig. 2.11b. At the central frequency, this combiner behaves just like the one previously depicted in Fig. 2.11b and is described by the same equations (2.20)-(2.24). In this case, however, the Chireix compensating elements are not explicitly shown as individual lumped elements in Fig. 2.13 but such compensation is accomplished by the unequal lengths of the coupled lines. Those lengths are adjusted such that opposite (shunt-like) reactances appear at the proper inputs of the combiner depending on the compensating angle, just like the standard Chireix compensation elements. The particular components of the combiner in Fig. 2.13 are designed according to [28][7]:

[7] The equations provided here are slightly different than the original ones in [28] and use explicitly a magnetic coupling term that is more intuitive for design.



(a) QWTL-based combiner.

(b) Transformer-based combiner.

Figure 2.12: Power factor of a) the QWTL-based and b) the transformer-based outphasing combiners with compensation at 10 dB back-off power versus frequency for $0.8 \times \omega_0 \leq \omega \leq 1.2 \times \omega_0$.

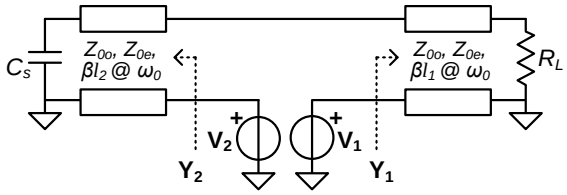


Figure 2.13: Outphasing combiner based on coupled-line transformers (i.e. Marchand balun-like) [28].

$$\beta l_{1,2} = \arctan\left(\frac{2}{\pm B_{\theta c} \cdot (Z_{0e} + Z_{0o})}\right) \tag{2.35}$$

where $\beta l_{1,2}$ are the electrical lengths of the coupled lines that account for the Chireix-like compensation elements $\pm B_{\theta c}$. Z_{0e} and Z_{0o} are the even-mode and odd-mode impedances of the coupled-line elements. The odd-mode impedance Z_{0o} can be calculated based on the impedance transformation from output to inputs according to

$$Z_{0o} = \frac{R_L}{1+k} = \frac{2k^2 \cdot R_{PA}}{1+k} \tag{2.36}$$

$$Z_{0e} = Z_{0o}\left(\frac{1+k}{1-k}\right) \tag{2.37}$$

in which $R_{PA} = \frac{1}{k^2}\left(\frac{R_L}{2}\right)$ is the load seen by each voltage source at full power and k is the magnetic coupling of the coupled-line "transformers", which in turn is given by

$$k = \frac{Z_{0e} - Z_{0o}}{Z_{0e} + Z_{0o}} \tag{2.38}$$

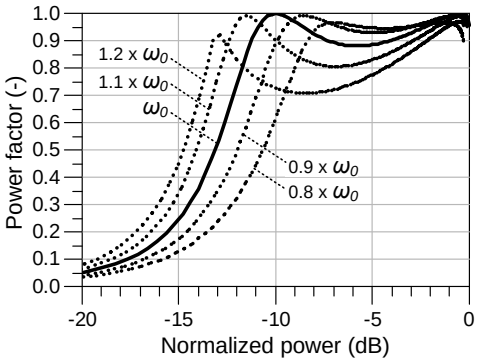


Figure 2.14: Net power factor of the coupled-line transformers outphasing combiner [28] versus back-off from 0.8× to 1.2× the design frequency ω_0, considering $k = 0.8$ and initial compensation at -10 dB back-off.

and is maximized with larger ratios of Z_{0e}/Z_{0o}. The capacitor C_s in Fig. 2.13 is required to tune out the leakage inductance resulting from imperfect coupling (i.e. $k < 1$) from both coupled-lines [28]:

$$C_s = \frac{1}{2\omega_0}\left(\frac{1}{Z_{0o}} + \frac{1}{Z_{0e}}\right)\cot\left(\beta l_2\right) \tag{2.39}$$

As an example with $k = 0.8$ and compensation at -10 dB back-off, Fig. 2.14 depicts the power factor of this combiner versus back-off power from 0.8× to 1.2× the design frequency ω_0. Comparing Fig. 2.14 with Fig. 2.12, it can be appreciated that this combiner is also wideband although it has an asymmetrical frequency response compared to the transformer-based combiner.

It shall be noted that, from (2.35), βl_2 seems negative but in practice it is non-negative because (2.35) is actually modified to provide a given amount of negative susceptance B_E (i.e. a shunt inductor) to (miss-)tune out the output capacitance C_{out} of the devices. For example, the branch amplifiers employed in [28] operate in class-E and therefore (2.35) is actually given by

$$\beta l_{1,2}|_{\text{class E}} = \arctan\left(\frac{2}{B_E \pm B_{\theta c}\cdot(Z_{0e}+Z_{0o})}\right) \tag{2.40}$$

where $B_E \approx 1.69\cdot\omega_0\cdot C_{out}$ (and $R_{PA}|_{\text{class E}} \approx \frac{0.585}{\omega_0\cdot C_{out}}$) is needed for the desired class-E operation.

2.6. OTHER ADD-ON EFFICIENCY-ENHANCEMENT TECHNIQUES FOR OUTPHASING

In addition to the outphasing combining strategies described previously, this section briefly describes other techniques that can be employed to further enhance the back-off

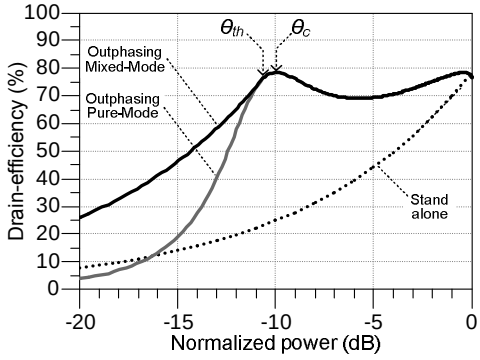


Figure 2.15: Drain-efficiency of pure-mode and mixed-mode class-B outphasing amplifiers versus back-off power (the case of stand-alone class-B is added for reference). The corresponding threshold angle θ_{th} to switch from pure-mode outphasing to linear-mode is just beyond (in back-off) the Chireix compensation angle θ_c.

efficiency performance of the outphasing amplifiers. The first technique is about introducing amplitude modulation to the otherwise phase-modulated-only driving signals in order to improve the efficiency at deep back-off levels. The second technique is about increasing the number of outphasing vectors beyond two in order to minimize the unwanted reactive load modulation in order to improve the efficiency at lower levels of back-off.

2.6.1. MIXED-MODE OUTPHASING OPERATION

All the previous outphasing topologies, with both isolating and non-isolating combiners, use constant-amplitude amplified signals and therefore output power level is controlled only by means of phase modulation. This is, of course, the basic principle of the outphasing amplifier and can be referred to as the “pure-mode” outphasing operation. However, keeping the input drive power constant at all output power levels compromises total-efficiency at back-off due to the limited gain of the actual active devices at RF. Several authors have proposed adding some form of amplitude control at the input signals in order to boost total-efficiency. This is referred to as “mixed-mode” outphasing operation and is especially useful when dealing with high-PAR modulated signals.

The works in [57] and [58] proposed adding a linear input amplitude control on a LINC architecture "above" a certain threshold, keeping the traditional outphasing modulation for the lower power levels. Although they showed some improvement, it was rather limited and only with respect to the already poorer performance expected from using an isolating combiner. The work in [59] employed a non-isolating combiner and experimentally added both amplitude and (differential) phase control at the driving signals looking to maximize efficiency at all different back-off levels. Later, the work in [51] also demonstrated a high-performance outphasing amplifier using a non-isolating combiner and proposed switching to pure "amplitude" control "below" a certain amplitude

level threshold (or equivalently, a certain outphasing angle threshold θ_{th}) just beyond the Chireix compensation point (i.e., θ_c). The class-B amplifiers used in [51] are in "pure" outphasing mode at the upper power levels and in “linear-mode” at the lower power levels where the loading is purely real. Switching to input amplitude control at back-off reduces the otherwise very reactive loading conditions at deeper back-off levels and results in a much softer efficiency roll-off compared to the pure-mode Chireix outphasing (this roll-off is actually the same as for the case of a linear class-B amplifier). This is shown in Fig. 2.15, which depicts the maximum theoretical drain-efficiency of class-B amplifiers versus back-off power for three cases: a) in stand-alone, b) with pure-mode outphasing, and c) with mixed-mode outphasing. The maximum performance of the class-B amplifier in mixed-mode outphasing can only be achieved with the proper input drive profiles that include both amplitude and phase control, as detailed in [60] and elaborated further in the next chapter.

2.6.2. N-WAY OUTPHASING COMBINERS

As mentioned at the beginning of this chapter, the outphasing modulation is not limited to the use of only two vectors. In fact, one of the first practical 4-way outphasing systems was proposed in [35, 36] using a 2-stage resistance compression network (RCN). An RCN is a class of matching networks that can be used to reduce the variation in effective resistance seen by tuned RF inverters as loading conditions change and can also be used for the same purpose in load-modulated (multi-path) RF power amplifiers [44]. Fig. 2.16 depicts the 4-way circuit described in [36] although other implementations are possible [38, 61]. The two reactances X_1 and X_2 in the two-stage RCN in Fig. 2.16a can be selected to provide a load sensitivity compression of $1:\left(\frac{b_1^2}{k_1}\right)\left(\frac{b_2^2}{k_2}\right)$ (or simply $1:\left(\frac{b_1^2}{k_2}\right)$) after the selection of R_L and an arbitrary parameter $k_2 > 1$ (which is normally small, for example $k_2 = 1.05$ will produce a RCN with a 1:11.4 compression) as follows [36]:

$$X_2 = \frac{2 \cdot R_L}{k_2 + 1} \tag{2.41}$$

$$X_1 = \frac{X_2}{b_2} \tag{2.42}$$

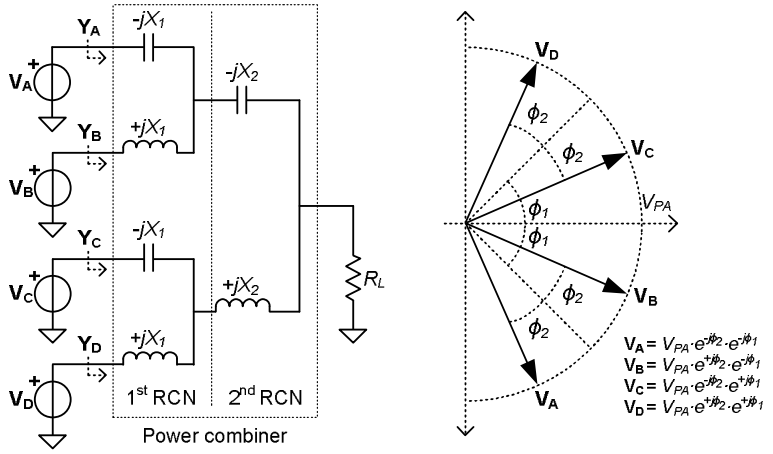
$$b_{1,2} = k_{1,2} + \sqrt{k_{1,2}^2 - 1} \tag{2.43}$$

$$k_1 = b_2^2 \tag{2.44}$$

The four sources in Fig. 2.16a are controlled by a pair of outphasing angles (ϕ_1, ϕ_2) with the relationships shown in the vector diagram of Fig. 2.16b. It can be shown [62] that the load voltage is given by

$$V_{RL} = j\frac{R_L}{X_1}\left(V_B - V_A + V_D - V_C\right) \tag{2.45}$$

and therefore the total power delivered to R_L by any pair (ϕ_1, ϕ_2) is given by



(a) Basic circuit schematic.

(b) Phasor relationship between the sources.

Figure 2.16: Four-way outphasing combiner using a two-stage resistance compression network [35, 36].

$$P_{out} = 4\left(\frac{V_{PA}^2}{2\cdot R_{PA}}\right)\sin^2(\phi_2)\cos^2(\phi_1) \tag{2.46}$$

where $R_{PA} = \frac{X_1^2}{4\cdot R_L}$ is the resistive load at the maximum power, which occurs when $(\phi_1 = 0, \phi_2 = \pi/2)$. Minimum power is reached when $\phi_{1,2} = 0$. As indicated by (2.46), and previously by (2.8) in Section 2.2, there are two degrees of freedom and therefore a variety of laws can be followed for controlling the power with the pair of phases (ϕ_1, ϕ_2) [62]. These laws can then be functions of a normalized commanded power $P_{cmd} = P_{out}/P_{out,max}$ and the dynamic load seen by the sources depends on the specific profile of such laws.

A control law that minimizes the effective input susceptance seen by the branch amplifiers was proposed in [62]. The work in [63] further elaborated on this control law by proposing an arbitrary power normalization. Here, this so-called "optimum susceptance" control law is described by using a more intuitive normalization (with respect to $P_{out,max}$ in (2.46)):

$$\phi_1 = \arccos\left(\sqrt{\frac{\gamma^2}{16\cdot P_{cmd}} + P_{cmd}}\right) \tag{2.47}$$

$$\phi_2 = \arctan\left(\frac{4}{\gamma\cdot P_{cmd}}\right) \tag{2.48}$$

where $\gamma = \frac{X_1}{R_L}$ is an intermediate variable. In principle, (2.47) and (2.48) are valid within the range $\frac{1}{2}\left(1-\sqrt{1-\gamma^2/4}\right) \le P_{cmd} \le \frac{1}{2}\left(1+\sqrt{1-\gamma^2/4}\right)$, providing a "linear" re-

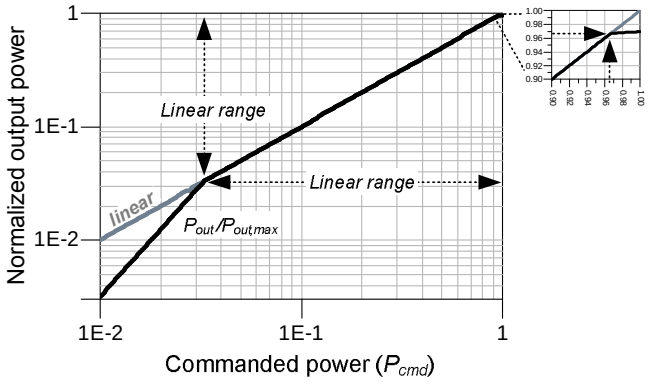
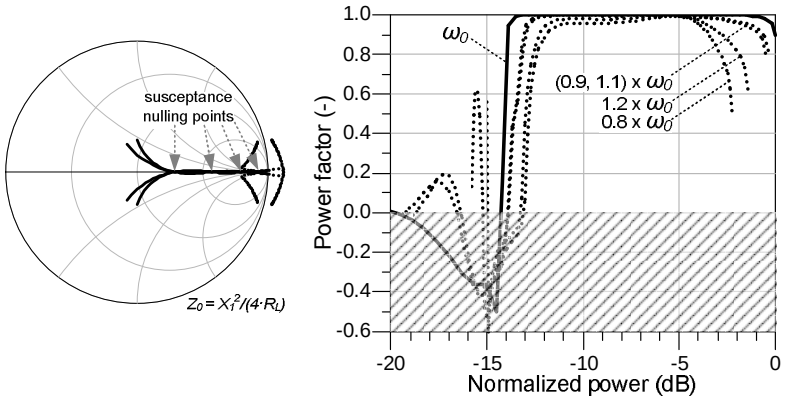


Figure 2.17: Normalized (limited) linear power control range for the four-way outphasing system using the "optimum susceptance" control law.

sponse between the actual P_{out} and the commanded P_{cmd}, as depicted in Fig. 2.17. This range directly enables only $10 \cdot \log 10\left(\frac{2+\sqrt{4-\gamma^2}}{2-\sqrt{4-\gamma^2}}\right)$-dB of linear power dynamic range. In the choice of k_2, there is a trade-off between dynamic range and worst-case input susceptance in which larger k_2 values result in increased dynamic ranges at the cost of higher susceptance magnitudes [62]. Fig. 2.18 plots the efficiency performance of a 4-way combiner with $k_2 = 1.05$: Fig. 2.18a depicts in the Smith chart the load-$\Gamma\left(1/\mathbf{Y_{A,B,C,D}}\right)$ loci seen by each source of Fig. 2.16 at the nominal frequency; while Fig. 2.18b plots the net power factor of the combiner versus frequency (from 0.8× to 1.2× the nominal frequency ω_0). It can be appreciated in Fig. 2.18a that the susceptive loading of this combiner is greatly reduced in comparison to the case of the traditional Chireix outphasing amplifier in Fig. 2.9a. This is due to the added sources that bring along extra susceptance-nulling points. As a consequence of this, Fig. 2.18b shows a very high and flat net power factor at the nominal frequency but only for about 14 dB of back-off after which it rapidly decays (for other frequencies this range is even lower as shown in the figure). This limited dynamic range is not enough for communications applications, so extra control schemes are necessary to extend it such as predistortion and input drive back-off [38]. In addition, as noticed in both Fig. 2.18a and Fig. 2.18b, the dynamic resistive loading at very low powers can become negative, rising instability concerns. Practical implementations of this combiner have been demonstrated at 27.12 MHz [64] and at 2.14 GHz [37, 38]. Despite the great theoretical performance of this topology, the actual efficiency performance of the prototypes demonstrated so far are significantly lower than other simpler 2-way Chireix implementations [28, 65], including the one described later in Chapter 7.



(a) (b)

Figure 2.18: Load modulation and net power factor for the four-way outphasing combiner: a) load-$\Gamma\left(1/\mathbf{Y_{1,2}}\right)$ loci in the Smith chart and b) power factor versus back-off and frequency for $0.8 \times \omega_0 \leq \omega \leq 1.2 \times \omega_0$.

2.7. OUTPHASING NON-IDEALITIES

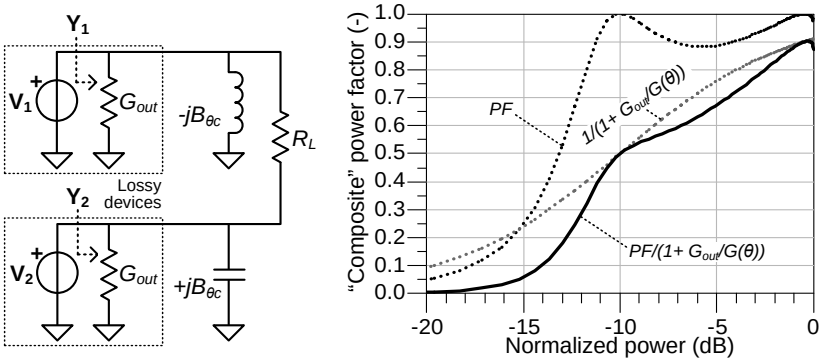
The maximum attainable performance of a practical outphasing amplifier is constrained by several factors at both device-level and system-level, which are briefly discussed in this section. At the device-level, these constrains are mainly related to undesired transistor non-idealities such as finite output conductance and finite power gain (especially at RF). At the system-level, the main concerns are related to branch imbalances and bandwidth expansion of the branch signals [8].

2.7.1. FINITE OUTPUT CONDUCTANCE

Practical transistor devices, as well as matching and combining networks have losses. For simplicity, these losses can be modeled as a single conductance G_{out} in parallel with the load seen by each device [51, 66], as shown in the Chireix combiner of Fig. 2.19a. These losses limit the effectiveness of the efficiency enhancement of the outphasing modulation. At deeper back-off levels, the outphasing-modulated load increases and G_{out} becomes significant, dissipating more power and causing efficiency degradation. The resulting drain-efficiency $\eta_{DE_N,G_{out}}$ that accounts for this effect can be derived following the same generalization for N sources in Section 2.3, this is

$$\eta_{DE_N,G_{out}} = \frac{\sum_{n=1}^{N} P_{out_n} - \sum_{n=1}^{N} P_{losses_n}}{\sum_{n=1}^{N} P_{DC_n}} \tag{2.49}$$

[8] Another issue relates to the actual branch signal generation, but this is discussed in the next chapter.



(a) (b)

Figure 2.19: Effects due to finite output conductance G_{out} in a Chireix outphasing combiner: a) schematic with lossy devices and b) example of (normalized) efficiency degradation for the case of $G_{out} = 10\,[G(\theta(t))]_{max}$. Because a) only contains AC sources, the results in b) are normalized and hence are equivalent to a "composite" power factor that includes the effect of G_{out}.

where the numerator represents the *total* fundamental RF power delivered to the actual output load R_L (in Fig. 2.19) and P_{out_n} is the total fundamental RF power generated by the amplifier including P_{losses_n}, where P_{losses_n} represents the power lost due to G_{out}. P_{out_n} and P_{DC_n} were given previously in Section 2.3 by (2.10) and (2.11), respectively, while $P_{losses_n} = \frac{1}{2}|\mathbf{V_n}|^2 \cdot G_{out}$. Assuming identical sources (and correspondingly identical G_{out} per source) (2.49) can be simplified to

$$\eta_{DE_N,G_{out}} = \eta_{DE_N} \cdot \left(1 - \frac{N \cdot G_{out}}{\sum_{n=1}^{N} \mathbf{Re}\{\mathbf{Y_n}\}}\right) \tag{2.50}$$

which for the common case of a two-way outphasing system at the center frequency can be further simplified to[9]

$$\eta_{DE,G_{out}} = \eta_{DE} \cdot \left(1 - \frac{G_{out}}{\mathbf{Re}\{\mathbf{Y_{1,2}}\}}\right) \approx \eta_{DE} \cdot \left(\frac{1}{1 + G_{out}/G(\theta(t))}\right) \tag{2.51}$$

where η_{DE_N} and η_{DE} are the normal drain efficiencies for N and 2 sources, respectively, as given by (2.12)-(2.19). Note that in this case, as can be observed in Fig. 2.19a, $\mathbf{Re}\{\mathbf{Y_n}\}$ includes both the finite output conductance G_{out} as well as the normal outphasing modulation term $G(\theta(t))$, this is $\mathbf{Re}\{\mathbf{Y_n}\} = G_{out} + G(\theta(t))$. Therefore, the second term in (2.50) and (2.51) represents the efficiency degradation due to G_{out}. Fig. 2.19b illustrates an example of this efficiency degradation for the case when $G(\theta(t))|_{max} = 10 \times G_{out}$. In this example, $G(\theta(t))$ starts being $10 \times G_{out}$ at full power while its gets to

[9] The same expression for $\eta_{DE,G_{out}}$ in 2.51 was derived previously in [51, Eq. 17]. The derivation provided here is only for the sake of completeness.

the same value of G_{out} at 10 dB back-off, resulting in a drain-efficiency which is 91% and 50% of the original lossless case at those conditions, respectively.

The efficiency degradation due to G_{out} in outphasing can be significant in some transistor technologies and needs to be considered with care. For example, sub-micron CMOS technologies have higher values of G_{out} (or conversely, lower output impedances) due to a stronger channel-length modulation than the longer channel technologies. Therefore, in these cases, a more efficient outphasing amplifier would require longer channels at the output stage or other output-impedance boosting techniques, indicating a trade-off between speed and efficiency. As another example, the outphasing amplifier can profit more from GaN HEMTs than from Si LDMOS transistors due to the increased power densities (and hence reduced G_{out}) of the first one (among other benefits).

2.7.2. FINITE POWER GAIN

High-power transistors also suffer from limited power gains G_P at GHz frequencies, ranging between 10-20 dB. As with almost all amplifiers, low power gains affect the "total"-efficiency η_{TOT} at back-off. This efficiency metric accounts for the total input power $\sum P_{in}$ as follows[10]

$$\eta_{TOT} = \frac{P_{out}}{P_{DC} + \sum P_{in}} \tag{2.52}$$

and is easy to show that it is related to the drain-efficiency η_{DE} according to

$$\eta_{TOT} = \eta_{DE}\left(\frac{1}{1+\eta_{DE}/G_{TOT}}\right) \tag{2.53}$$

$$G_{TOT} = \frac{P_{out}}{\sum P_{in}} \tag{2.54}$$

where G_{TOT} is the total amplifier power gain while G_P is the power gain of each transistor in the branch amplifiers. The profile of G_{TOT} with back-off depends on the specific driving profile of the branch amplifiers [51, 60], as will be shown in the next chapter. In the "pure" outphasing mode described earlier, G_{TOT} reduces linearly with back-off since the input power remains constant. Fig. 2.20 exemplifies this by showing the measured η_{DE}, η_{TOT} and G_{TOT} for a pure-mode outphasing amplifier prototype with 13.2 dB-gain GaN devices at 2.3 GHz [29] (this is amplifier is further described in Chapter 7). Therefore, with a modulated signal, the resulting average total-efficiency will be lower than the average drain-efficiency and if the power gain is low, then this difference can be significant. In the other hand, in "mixed" outphasing mode, a finite gain is less problematic because of the input amplitude control at back-off preserves G_{TOT} [51, 60], as shown in the next chapter.

[10] "Power-added" efficiency, $PAE = \frac{P_{out}-\sum P_{in}}{P_{DC}}$, is another widely used efficiency metric that accounts for the input power but is used more commonly for single-stage amplifiers.

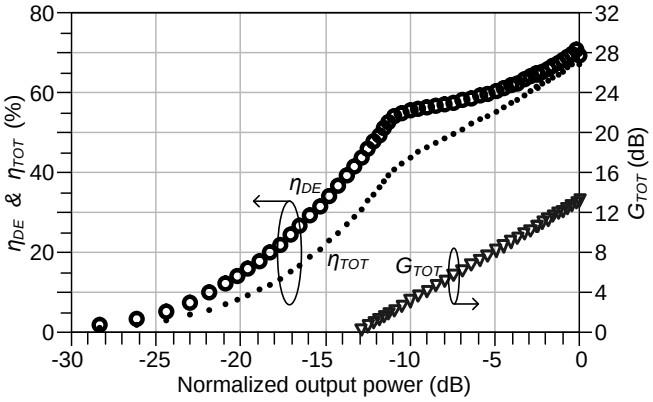


Figure 2.20: Example of measured efficiencies (η_{DE}, η_{TOT}) and total power gain (G_{TOT}) versus back-off for a practical pure-mode outphasing amplifier with 13.2 dB-gain GaN devices at 2.3 GHz [29]. G_{TOT} peaks at 13.2 dB and reduces linearly with back-off.

2.7.3. BANDWIDTH EXPANSION OF THE BRANCH SIGNALS

For the ideal outphasing modulation described earlier in Section 2.2, an alternative representation of the (normalized) outphasing branch signals $S_{1,2}(t)$ at baseband is given in Fig. 2.21a. As can be observed, these signals can be expressed as the summation of two signals in quadrature [67] according to

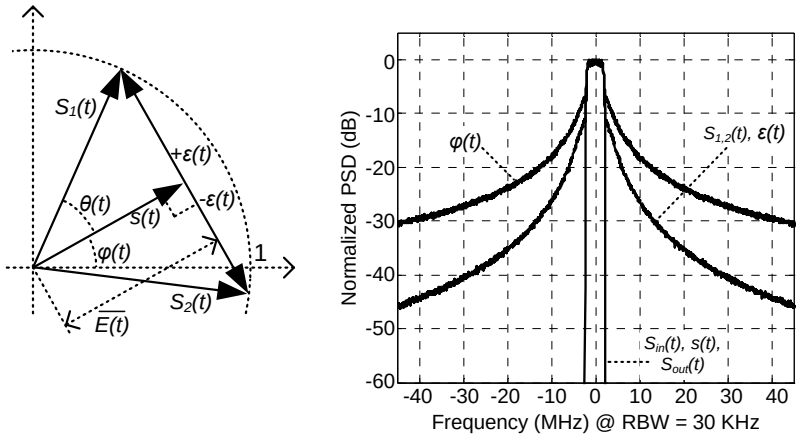
$$S_{1,2}(t) = e^{j(\varphi(t)\pm\theta(t))} = s(t) \pm \varepsilon(t) \tag{2.55}$$

$$s(t) = \overline{E(t)} \cdot e^{j\varphi(t)} \tag{2.56}$$

$$\varepsilon(t) = j \cdot s(t) \cdot \sqrt{\frac{1}{|s(t)|^2} - 1} \tag{2.57}$$

where $s(t)$ is the in-phase component (which is simply the normalized version of the original modulated signal $S_{in}(t)$ with envelope $E(t)$ and phase $\varphi(t)$), and $\varepsilon(t)$ is the quadrature component. Zero-crossings in the modulated signal $S_{in}(t)$ are responsible for instantaneous phase discontinuities and ultimately bandwidth expansion in $S_{1,2}(t)$ [68]. Fig. 2.21a shows the spectral power density of the different signals for the case of a W-CDMA test signal. Note that while $s(t)$ is band-limited, $\varepsilon(t)$ is not because of (2.57) and the zero-crossings of $S_{in}(t)$.

The branch signals $S_{1,2}(t)$ can be generated in different ways by a variety of circuits and the extended bandwidth in those signals imposes different requirements in those circuits compared to more conventional transmitters. One method is to create $S_{1,2}(t)$ by generating the phases $\varphi(t)$ and $\theta(t)$ directly using PLL-based phase modulators but these would require very large bandwidths which are difficult to achieve. The issue here is that the original phase signal $\varphi(t)$ can jump abruptly up to 2π radians when $S_{in}(t)$ crosses



(a) Vector representation. (b) Power spectral density.

Figure 2.21: Illustration of bandwith expansion in the branch signals.

the origin and it does not have a well-defined bandwidth [68]. A more popular method is to generate $S_{1,2}(t)$ digitally at baseband, followed by quadrature up-conversion to RF. This would require extra power due to the four DACs and to the higher sampling rates compared to conventional transmitters. Another approach proposes to generate $S_{1,2}(t)$ in the baseband analog domain in order to reduce power [69] by utilizing only two DACs and less oversampling (this comes at the expense of reduced flexibility in adapting the required transfer functions for proper operation, as will be described in the next chapter). More recently, phase modulators based on delay-based approaches have been proposed as a feasible way for wider band digital modulation [70]. All of these possibilities are important considerations when designing complete outphasing transmitters aimed for the best trade-offs between efficiency, linearity and bandwidth.

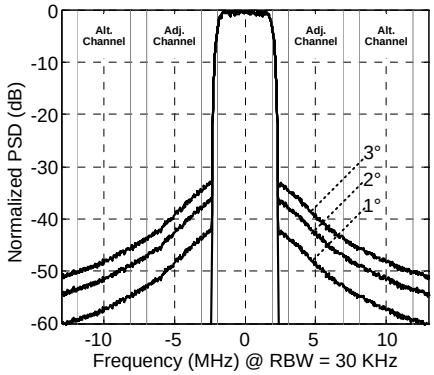
2.7.4. BRANCH IMBALANCES

Since the basic outphasing principle relies on vector summation, the performance of the outphasing amplifier is sensitive to amplitude and phase imbalances in the amplifying branches. The following is an expression for the reconstructed output signal $\hat{S}_{out}(t)$ after accounting for amplitude and phase imbalances, Δ_{AM} and Δ_{PM}, in one of the branches with respect to the other [41, Sec. 2.5.2]:

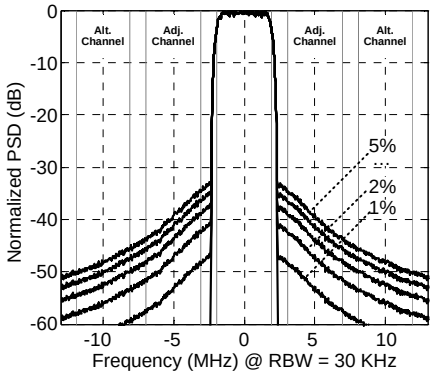
$$\hat{S}_{out}(t) = S_1(t) + S_2(t) \cdot (1 + \Delta_{AM})\, e^{j\Delta_{PM}} \tag{2.58}$$

Using (2.55) into (2.58) leads to the following expression

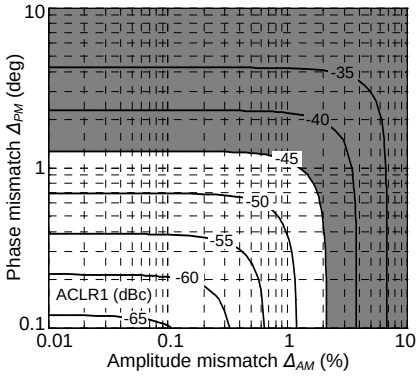
$$\hat{S}_{out}(t) = \left[1 + (1 + \Delta_{AM})\, e^{j\Delta_{PM}}\right] \cdot s(t) + \left[1 - (1 + \Delta_{AM})\, e^{j\Delta_{PM}}\right] \cdot \varepsilon(t) \tag{2.59}$$



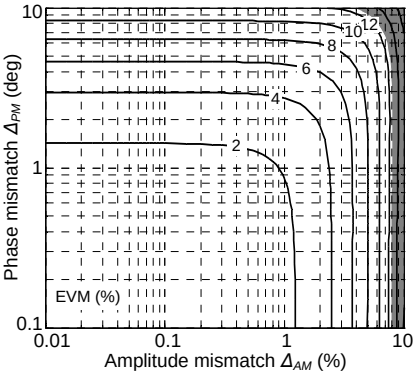
(a) Spectral regrowth due to Δ_{PM}.



(b) Spectral regrowth due to Δ_{AM}.



(c) *ACLR1* (dBc).



(d) *EVM* (%).

Figure 2.22: Effects of amplitude and phase mismatches on in-band and out-of-band distortion of the output signal (gray are in c) and d) are out-of-specs regions for 3GPP)

which for small amplitude and phase impairments ($\Delta_{AM} \to 0$ and $\Delta_{PM} \to 0$) can be approximated by [41, Sec. 2.5.2]

$$\hat{S}_{out}(t) \approx 2 \cdot s(t) - \left(\Delta_{AM} + j \cdot \Delta_{PM}\right) \cdot \varepsilon(t) \tag{2.60}$$

Then, according to (2.60), the power spectrum of $\hat{S}_{out}(t)$ is thus the weighted sum of the desired spectrum of $s(t) = \overline{S_{in}(t)}$ and the undesired spectrum of $\varepsilon(t)$. Therefore, above certain limits for both Δ_{AM} and Δ_{PM}, $\hat{S}_{out}(t)$ will show unacceptable out-of-band spectral regrowth (or higher levels of adjacent channel leakage power ratio, *ACLR1*) and in-band distortion (e.g. higher levels of error vector magnitude, *EVM*) depending on the specific modulation standard [71]. While phase imbalances can be corrected by phase shifts during the branch signal generation at baseband, amplitude imbalances will limit the achievable dynamic range [72] and will require extra mitigation techniques. A prac-

tical example of balancing the two branches in an outphasing amplifier is given in the next chapter.

Fig. 2.22 illustrate the effects of both amplitude and phase imbalances in the branches when using a W-CDMA signal [14]. Specifically, Fig. 2.22a and Fig. 2.22b show the spectral regrowth due to only a small phase and only a small amplitude imbalance, respectively. In addition, Fig. 2.22c and Fig. 2.22d show the corresponding *ACLR1* and *EVM*[11] levels due to the combined effect of both amplitude and phase mismatches. The white area in both Fig. 2.22c and Fig. 2.22d indicate levels that meet the 3GPP compliance specifications for base stations with this signal [15]: $ACLR1 < -45$ dBc (and $ACLR2 < -50$ dBc, not shown in the figures) and $EVM < 12.5$ %. It can be appreciated that the more strident constrain is due to *ACLR1*, resulting in maximum permissible imbalances of $\Delta_{AM} < 1\%$ and $\Delta_{PM} < 1^\circ$ (other practical impairments can actually reduce these limits even further).

2.8. CONCLUSIONS

This chapter reviewed fundamental aspects of the outphasing amplifier, including basic modulation principles, a review of different isolating and non-isolating power combining strategies published in recent literature, and some important non-idealities. A key aspect of this amplifier is its high-efficiency performance and a formal justification of the so-called "net power factor" as a figure-of-merit for the power combiner was provided and discussed. It was concluded that although it indeed quantifies properly the maximum efficiency performance of traditional outphasing amplifiers using class-B branch amplifiers, it does not accurately predict the full potential when using other branch amplifier types like class-E which can even provide higher efficiencies at deep back-off. This important aspect will be demonstrated by detailed simulations in the following chapter and can be appreciated as well in the actual results of the practical implementation described later in Chapter 7.

In addition to this, in this chapter other recent add-on techniques like "mixed-mode" operation and multi-way outphasing were briefly described. These two techniques aim at improving the efficiency of outphasing amplifiers by either introducing amplitude control to the outphasing signals and by adding extra outphasing vectors, respectively. Since the interest of this thesis is in simpler and effective efficiency enhancement techniques, the case of the "mixed-mode" approach will be further detailed in the next chapter along with other specific two-way outphasing amplifiers.

[11] Here, EVM is calculated for every k-th sample (not symbol) on the actual signal $Z(k)$ with respect to a reference signal $R(k)$ previously normalized with respect to their own root-mean-square levels: $EVM = 100\% \times \sqrt{\frac{\sum|Z(k)-R(k)|^2}{\sum|R(k)|^2}}$. However, a proper computation of EVM is performed with the actual symbols, requiring an ideal demodulation-modulation followed by several error minimization processes [15, Appendix E], and leads to lower levels. The "sample-wise" EVM used here can be considered a "worse case EVM" which is much easier to perform and does not require details of the specific signal under test.

3

STUDY OF LOAD-MODULATED AMPLIFIERS I: DESIGN AND EFFICIENCY PERFORMANCE

3.1. INTRODUCTION

Most text books and current literature (e.g. [16, Ch. 10]) that describe load modulation for the efficiency enhancement of power amplifiers treat active devices simply as ideal AC sources with unbounded maximum ratings for their current or voltage capabilities. With this high-level abstraction, the evaluation of the different amplifier topologies focuses on the interaction of such sources with their power combining networks, while their achievable "drain" efficiency performance is estimated assuming a specific operating class for their branch amplifiers. Although this simplified approach is useful for a high-level understanding of the general and ideal operation of the different amplifier topologies, practical active devices exhibit several physical limitations and non-idealities that can cause deviations from the original assumptions. Some of the limitations include finite breakdown voltages, current handling capabilities and power gain, while device non-idealities include finite output impedances, conduction losses, non-linear elements among others. In addition, the applied drive profiles for the branch amplifiers strongly impact the performance and operation of the overall amplifier architecture, requiring more detailed consideration and analysis. This chapter and the following provide a comprehensible system-level analysis for several load-modulated power amplifiers, including Doherty and outphasing topologies. This chapter focuses on system-level design and (instantaneous and average) efficiency performance and aims at identi-

Section 3.2 and subsection 3.5.1 of this chapter were published by: **D.A. Calvillo-Cortes** and L.C.N. de Vreede, "Analysis of Pure- and Mixed-Mode Class-B Outphasing Amplifiers," in IEEE Latin American Symposium on Circuits and Systems (LASCAS) proceedings, Feb. 2014.

fying the optimum operation and drive conditions when practical device constraints in the constitutive branch amplifiers are taken into account. The following chapter deals with bandwidth expansion of the driving signals, another important consideration for multi-input load-modulated amplifiers.

This chapter starts by describing an idealized large-signal transistor model that will be used to study the different amplifier topologies and that can account for limited power gain, current handling and voltage breakdown, among other device constrains. After this, the basic operation of class-B and class-E amplifiers is reviewed using this large-signal device model as they both will be employed as branch amplifiers in the Doherty and outphasing amplifiers. Special attention is given to the class-E switch-mode branch amplifier since its inherently higher efficiency makes it the candidate of choice in subsequent chapters of this thesis, leading to several practical designs in Chapters 6 and 7. Next, the symmetric and the asymmetric Doherty amplifier configurations are described and evaluated in terms of their maximum *instantaneous* drain- and total-efficiency when using class-B for both the main and peak branch amplifiers. Doherty amplifiers are currently the most popular choice in base stations and are used here to benchmark the performance of the other amplifier topologies in this chapter. Subsequently, several outphasing amplifiers are analyzed in detail, using both class-B and class-E branch amplifiers. For the outphasing PA with class-B branch amplifiers, three specific drive profiles / operating modes are considered: the classical over-driven phase-modulated branch signals, a more adequate drive profile that accounts for the transconductance nature of the transistors and a modified drive profile for "mixed-mode" operation. For the outphasing PA with class-E branch amplifiers, a phase-only drive profile is studied with two amplitude levels, namely, 60%-overdrive and onset-overdrive. The aim of these experiments is to analyze the effect of reducing the driving power in an effort to enhance the total-efficiency of the amplifier line-up. Once the most important load-modulated amplifier configurations have been reviewed, their ideal *average* efficiency performance is evaluated when considering a modulated signal with a Rayleigh-distributed envelope, using both analytical computations based on harmonic/balance simulations as well as with envelope simulations provided last. Overall, the evaluation of the different amplifiers in this chapter underlines the importance of combining optimum device matching techniques with optimum drive profiles of the different branch amplifiers. In addition, it provides a clear performance comparison on the different amplifier topologies with a generalized device model and common modulated signals.

3.2. A SIMPLIFIED LARGE-SIGNAL TRANSISTOR MODEL FOR PA STUDIES

3.2.1. PROPERTIES OF THE MODEL

The design of practical RF power amplifiers require comprehensible transistor models from the actual device manufacturers or directly from measured load-pull data [33, 34].

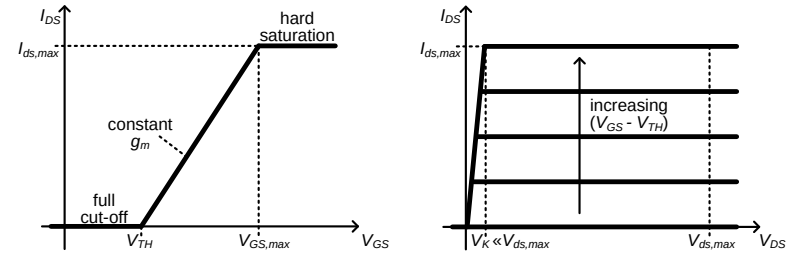


Figure 3.1: DC curves for the ideal strongly nonlinear device model.

However, for the purpose of this chapter, a simpler large-signal device model is employed for the active devices that allows including the effect of some of their main physical constraints such as limited current handling, voltage breakdown and power gain. This approach aims at being more comprehensible that the otherwise used assumption of perfect voltage/current source behavior representing the active devices while being still analytically tractable. It includes sufficient detail to capture important behavioral aspects in entire amplifier architectures in terms of drain and total efficiencies.

The DC current-voltage behavior of this transistor model is depicted in Fig. 3.1. The transistors are modeled as "ideal strongly nonlinear transconductance devices" with constant transconductance g_m and negligible knee-voltage V_K [16, Ch. 4] [73]. Between the threshold voltage[1] V_{TH} and $V_{GS,max}$, the voltage-to-current transfer function is perfectly linear while strong nonlinearities are represented by the hard cut-off ($V_{GS} < V_{TH}$) and the hard saturation ($V_{GS} > V_{GS,max}$) transitions as shown in Fig. 3.1a. Note in Fig. 3.1b that for simplicity, I_{ds} is assumed to be independent of V_{DS} which implies that the output conductance is zero. Also note that although the drain-source breakdown voltage behavior is not explicitly modeled in Fig. 3.1b, a maximum allowable voltage swing $V_{ds,max}$ is indicated and is avoided during the use of this model. For the purpose of this chapter, these are useful simplifications of the actual behavior of practical transistors that instead exhibit both softer saturation and softer cut-off transitions in addition to weak nonlinearities in the large-signal transconductance function [16, Ch. 2].

3.2.2. MODEL FORMULATION

The previous transistor behavior is modeled using an ideal voltage-controlled current-source I_{ds} that is a function of an overdrive gate-source voltage $V_{gs} = V_{GS} - V_{TH}$ and is described with the following piecewise linear formulation[2]:

[1] This chapter focuses in FET transistors, as implied by the notation (e.g. Si LDMOS and GaN HEMT).

[2] The abrupt transitions in (3.1) can lead to convergence issues in certain simulations. In such cases, (3.1) can incorporate (i.e., be multiplied by) functions to soften the corners, for example "$\times \left[\frac{1}{2} + \frac{1}{2}\tanh\left(\alpha \cdot \left(V_{ds} - \beta\right)\right)\right]$" with large α and very small β [34]. Other functions like "$\times \left[1 - \exp\left(-V_{ds}/\left(V_K/5\right)\right)\right]$" (modified from [74] and

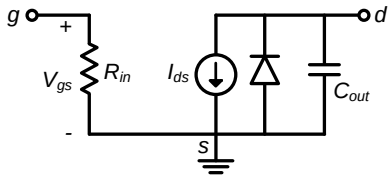


Figure 3.2: Simplified large-signal transistor model for system-level amplifier simulations. The voltage-controlled current-source I_{ds} is defined in (3.1).

$$I_{ds}(t) = \begin{cases} 0, & \text{for } V_{gs}(t) < V_{TH} \quad (3.1a) \\ g_m \cdot V_{gs}(t), & \text{for } V_{TH} \le V_{gs}(t) < V_{gs,max} \quad (3.1b) \\ g_m \cdot V_{gs,max}, & \text{for } V_{gs}(t) \ge V_{gs,max} \quad (3.1c) \end{cases}$$

where it can be noticed that the current I_{ds} saturates at $I_{ds,max} = g_m \cdot V_{gs,max}$ for $V_{gs} \ge V_{gs,max}$ and $V_{gs,max} = V_{GS,max} - V_{TH}$. For simplicity and without any loss of generality, this model is simplified by setting V_{TH} to zero and $V_{gs,max}$ to one. In this case, g_m would represent the equivalent device transconductance for a normalized overdrive voltage $\overline{V_{gs}} = V_{gs}/V_{gs,max}$.

In addition to the previous linear transconductance transfer function, the model includes an output capacitance, an input resistance and a (optional) reverse-biased diode, as depicted in Fig. 3.2. For simplicity, the input capacitance is neglected from the model (e.g. it can be assumed to be resonated out by a matching circuitry) and the device is considered unilateral. The ideal reversed diode prevents the drain-source voltage swings on having (very) negative polarities[3]. The output capacitance C_{out} represents all capacitance at the transistor output, including the drain-source capacitance C_{ds} and the gate-drain capacitance C_{gd} and it is considered constant (i.e. its practical dependency on terminal voltages is neglected). The input resistance R_{in} in Fig. 3.2 is used to define the effect of a finite operating power gain G_P as explained shortly. Although nonlinearities can be introduced to the transistor model (such as a third order polynomial description of I_{ds} to represent weak AM-AM nonlinearities [16, Ch. 4] and a nonlinear output capacitance [74] for AM-PM distortion), these are not considered here for simplicity.

3.2.3. SELECTION OF MODEL PARAMETERS

At RF frequencies, practical active devices exhibit limited power gains. In particular, the operating power gain $G_P = \frac{P_{out}}{P_{in}}$ defines the relation between output power P_{out} and

valid for $V_{ds} > 0$) can also soften corners and allow using a finite knee-voltage if required.

[3] The presence of this diode, which represents the parasitic diode between drain-bulk in MOSFETs, does not influence the normal waveforms in most amplifier classes since they have positive polarities. However, in switch-mode amplifiers like class-E, this diode prevents eventual negative-polarity voltage swings that would be allowed if those devices are idealized unbounded switches (like in a purely mathematical analysis).

input power P_{in}. This is a very important consideration in power amplifiers since efficiency is quantified not only by the drain-efficiency $\eta_{DE} = \frac{P_{out}}{P_{DC}}$ but also by the total-efficiency $\eta_{TOT} = \frac{P_{out}}{P_{DC}+P_{in}}$ to take into account P_{in} in addition to the DC power P_{DC}. In this model, a finite G_P (which is a commonly known parameter of RF transistors) is incorporated by means of R_{in} in Fig. 3.2, which dissipates the input power (alternatively, R_{in} can be seen as the driving losses after the transistor has been conjugate-matched at its input). Therefore, assuming class-B operation as reference, $R_{in,B}$ can be defined in terms of G_P according to:

$$R_{in,B} = \frac{G_P \cdot V_{gs,max}^2 \cdot R_{opt,B}}{V_{DD,B}^2} \tag{3.2}$$

$$R_{opt,B} = \frac{V_{DD,B}}{I_{ds,max}/2} = \frac{2 \cdot V_{DD,B}}{g_m \cdot V_{gs,max}} \tag{3.3}$$

where $R_{opt,B}$ is the familiar optimum load for class-B and $V_{DD,B}$ is the DC-supply. Later in this chapter, for the class-E amplifiers a (overdriven) sinusoidal drive will be used and as such, the input power will also be dissipated by the same $R_{in,B}$ in order to represent the same device (with the same G_P) and to allow direct comparisons with class-B amplifiers. In practice, however, true switch-mode class-E amplifiers can be driven directly by squared waves coming from dedicated digital drivers that can improve their effective gain and switching behavior [28, 75].

3.3. STAND-ALONE BRANCH AMPLIFIER OPERATION

Although stand-alone class-B and class-E amplifiers are well-known and described elsewhere [16,76,77], they are briefly described in this section because they will be employed later for the branch amplifiers of several Doherty and outphasing amplifiers. In particular, special attention is given to class-E because it has important subtleties and due to its higher efficiency will be also employed in subsequent chapters of this thesis.

3.3.1. CLASS-B BRANCH AMPLIFIERS

The circuit schematic in Fig. 3.3 represents an ideal class-B amplifier. The quarter-wavelength line in Fig. 3.3 acts as a DC-feed and provides the required even harmonics shorts needed for class-B operation (note that for the ideal class-B amplifier, I_{ds} is an even function and thus the odd harmonic terms are inherently very low [16, Fig. 3.2], making the need for odd harmonics shorts less stringent). As discussed previously, the input is assumed to be conjugate-matched and hence the operating power gain is set by means of the R_{in} defined according to (3.2). Assuming a 20 dB-gain device, i.e.

$G_P = 20$ dB[4], Fig. 3.4 plots the familiar drain- and total-efficiency curves as well as power gain and output power (normalized with respect to the maximum linear power) versus the normalized overdrive voltage $\overline{V_{gs}}$. At $\overline{V_{gs}} = 1$ the expected maximum "linear" drain-efficiency of 78.5% is reached while slightly higher efficiencies are possible by driving the active device into saturation where the power gain compresses. In addition, Fig. 3.5 depicts the well-known load-line as well as the voltage and current waveforms at the maximum (linear) class-B efficiency condition of 78.5%.

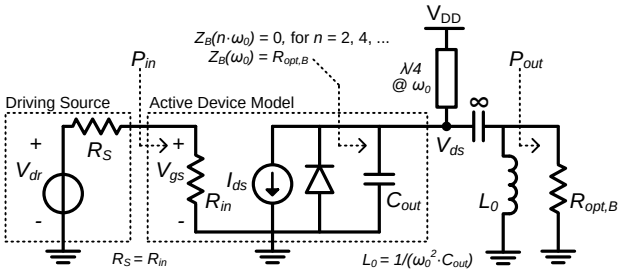


Figure 3.3: Schematic of the stand-alone class-B branch amplifier showing the simplified large-signal transistor model as described earlier.

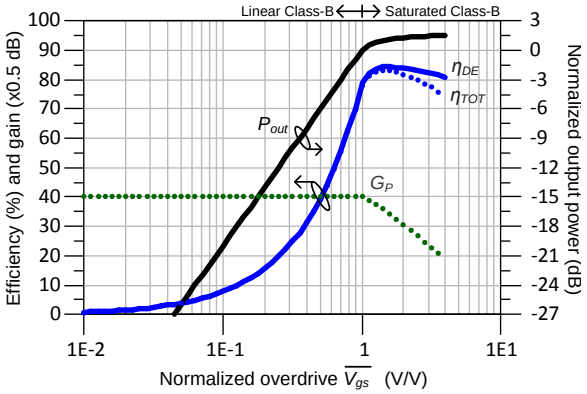
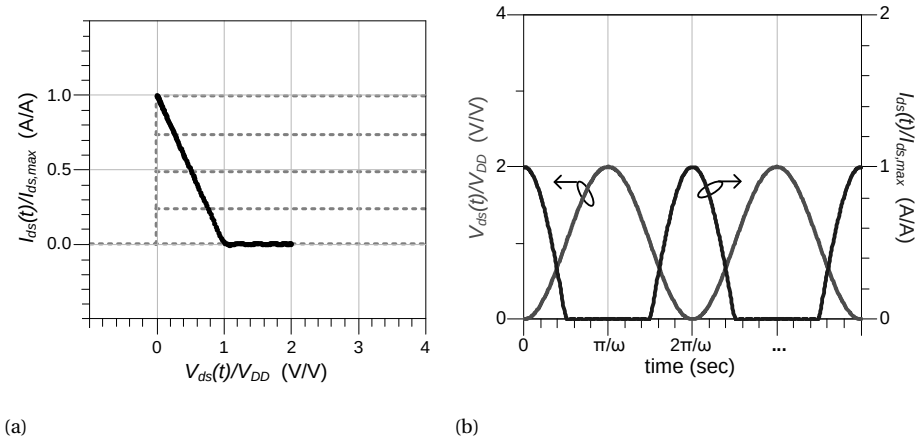


Figure 3.4: Harmonic-balance simulation results of the class-B amplifier in Fig. 3.3 versus normalized input drive $\overline{V_{gs}}$: shown are the drain- and total-efficiency, output power (normalized with respect to the maximum linear power) and power gain.

[4] This choice will be used in the rest of this chapter for both class-B and class-E branch amplifiers since it is a typical value in the low GHz range for high-power RF transistors.



(a) (b)

Figure 3.5: Response of the class-B amplifier in Fig. 3.3 when η_{DE} = 78.5% in Fig. 3.4: a) normalized load-line, b) normalized voltage and current waveforms.

3.3.2. CLASS-E BRANCH AMPLIFIERS

The class-E amplifier deserves a more detailed discussion as it is the basis of several practical amplifiers discussed here and also in subsequent chapters. This amplifier is categorized as a switch-mode amplifier (SMPA) where, ideally, the transistor operates as an on-off switch. It is designed such that the current and voltage waveforms do not overlap, maximizing energy efficiency with a theoretical limit of 100%. Different from g_m-based amplifiers, such as the previous class-B and all other classes from A, AB, to C, the class-E amplifier is designed based on equations originally derived from time-domain analysis under the idealized assumption that the active device acts as a perfect switch instead of as a transconductance device. Another notable difference in class-E is that the load network -and not the active device- determines the response of the voltage/current waveforms in response to the switching action of its transistor, making this amplifier highly nonlinear (i.e., its output amplitude is not controlled linearly by its input amplitude).

Although class-E was first introduced by G. D. Ewing in the mid-60s [78], its name was coined by the Sokal's a decade later [79, 80]. After a classical paper in the late 1970s by F. H. Raab describing its idealized operation [81], many more theoretical and practical works have appeared in literature covering different aspects and details of this amplifier. The more recent works in [82] and [77, Chs. 5-8] provide a good and comprehensible overview of this amplifier as well as of previous works. This section aims at concisely describing the design of these class-E amplifiers when specially targeted for the branches in outphasing amplifiers. First, the standard description based on ideal switches will be presented. Then, some refinements will be discussed in order to shift from the ideal switch to a more practical transconductance device, as used in the model of the active

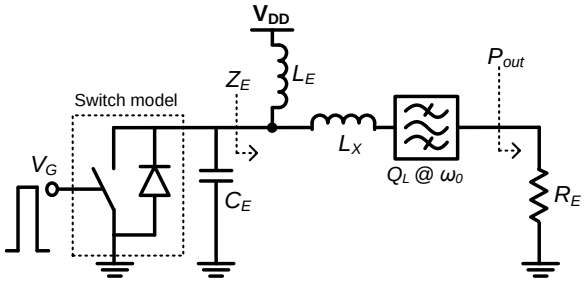


Figure 3.6: Schematic of the stand-alone class-E amplifier assuming an ideal switch model for the transistor.

devices in this chapter.

THE IDEAL SWITCH MODEL DESCRIPTION

In general, class-E amplifiers can be designed and/or operated in the so-called "optimum" or "sub-optimum" modes depending on their specific loading conditions [79,81]. The so-called "optimum" mode has been traditionally used to refer to the well-known condition of simultaneous zero-voltage ($V_{ds}(\pi/\omega_0) = 0$) and zero-voltage-derivative ($\frac{dV_{ds}}{dt}(\pi/\omega_0) = 0$) across the drain-source terminals of the intrinsic switch at the turn-on moment ($t = \pi/\omega_0$). However, only the first condition is responsible for the ideal efficiency of 100% while the second is useful in practice as it reduces the sensitivity of the circuit to the spread of component values [79]. If at the turn-on moment either the voltage and/or the voltage-derivative are non-zero, then the amplifier is said to be in a "sub-optimum" mode [81]. Two distinct conditions of this last mode are discussed in more detail in [83] and [84] for the particular case of non-zero voltage (called “variable-voltage”) and non-zero voltage-derivative (called “variable-slope”), respectively[5].

Fig. 3.6 depicts a general schematic for a class-E amplifier when the active device is assumed as a perfect switch[6]. In the figure, the fundamental load for this amplifier is indicated by Z_E while the ideal bandpass filter has a "high enough" loaded quality factor Q_L such as the output current is assumed sinusoidal at the switching frequency. Regardless of the specific operating mode, the class-E load network in Fig. 3.6 can take several forms because for a given set of design goals (e.g. supply voltage, operating frequency, and output capacitance) there is still one degree-of-freedom in the network [82]. One

[5] Actually, it has been recognized recently [85] that the term "optimum mode" has been a misnomer and should be referred to as "nominal mode" instead. This is because this nominal mode is truly optimum from an efficiency point of view only when all circuit components have negligible losses which is a much idealized assumption (although still used here for simplicity). Conversely, "sub-optimum mode" should be referred to as "off-nominal mode" [85]. This sub-optimum/off-nominal class-E mode is actually more useful when dealing with practical non-ideal switches (e.g. with finite on/off-resistance and/or limited breakdown voltage) and in certain conditions of load modulation as will be seen later.

[6] The effect of the reverse diode is normally not included in the time-domain mathematical analysis of class-E amplifiers. However, it is included here to explicitly indicate its presence in practical devices and to avoid unrealistic negative voltage excursions that are sometimes predicted by unconstrained mathematical models of this amplifier. In addition, in outphasing transmitters, it helps to maintain efficiency at deep back-off power levels.

way to express this design freedom is by the use of the design parameter "q", defined by M. Acar *et al.* in [82] as

$$q = \frac{1}{\omega\sqrt{L_E \cdot C_E}} \tag{3.4}$$

This parameter q determines how much the resonance frequency of the LC-tank, created by the shunt capacitance C_E and the DC-feed inductance L_E, deviates from the operating frequency ω. Therefore, the optimum (for 100% efficiency) class-E fundamental load Z_E in Fig. 3.6 and the maximum output power are functions of q, according to

$$Z_E = j\omega \cdot L_E || \left[R_E + j\omega \cdot L_X\right] \tag{3.5}$$

$$P_{out,E} = K_P\left(q\right) \cdot V_{DD,E}^2 / R_E \tag{3.6}$$

in which

$$R_E = \frac{K_C\left(q\right)}{\omega \cdot C_E} \tag{3.7}$$

$$L_E = R_E \frac{K_L\left(q\right)}{\omega} \tag{3.8}$$

$$L_X = R_E \frac{K_X\left(q\right)}{\omega} \tag{3.9}$$

where the $K_\square\left(q\right)$-functions represent a set of useful normalizations employed during the time-domain solution of the generalized class-E output network [82]. Once q is selected, the terms $K_\square\left(q\right)$ become constants and therefore the circuit elements R_E, L_E and L_X can be readily found for a given C_E and ω. An analytical solution as well as a polynomial-based approximation for the $K_\square\left(q\right)$ set in "optimum/nominal" mode is provided in [82]. For convenience, Table 3.1 summarizes the results for three distinctive cases of interest: the RF-choke, the parallel-circuit and the load-insensitive class-E amplifiers.

The classical "RF-choke" class-E PA [79, 81] corresponds to the case when $q = 0$ and therefore $Z_{E_{choke}} = R_{PA} + j\omega L_X$ since $L_E = \infty$ for $q = 0$. The "parallel-circuit" class-E PA [86] results when $q \approx 1.4$ and hence $Z_{E_{parallel}} = R_{PA} || j\omega L_E$ since $L_X = 0$ for $q \approx 1.4$. When $q \approx 1.3$, the class-E PA can be made "load-insensitive" by design [28] and this feature can be favorably exploited in outphasing amplifiers, as will be detailed later in Subsection 7.2.2. Although L_X is non-zero in this specific condition, in practical situations it can be neglected with minimum detriment on performance and therefore the load network becomes $Z_{E_{insensitive}} \approx R_{PA} || j\omega L_E$ and resembles the one of the parallel-circuit, sharing similar broadband characteristics [87]. As noticed from Table 3.1, the peak voltage $V_{ds,pk}$ and peak current through the switch $I_{ds,pk}$ are very weak functions of q and roughly about 3.6 and 2.7 times the supply voltage and current, respectively.

Table 3.1: DESIGN EQUATIONS FOR DIFFERENT CLASS-E AMPLIFIERS WITH IDEAL SWITCHES.

Design equations [82]	**RF-choke** [79, 81]	**Parallel-circuit** [86]	**Load-insensitive** [28]
q	0	1.41	1.3
$K_L(q) = \omega \cdot L_E / R_E$	$\rightarrow \infty$	0.732	1.01
$K_C(q) = \omega \cdot C_E \cdot R_E$	0.184	0.685	0.585
$K_P(q) = P_{out,E} \cdot R_E / V_{DD,E}^2$	0.577	1.365	1.29
$K_X(q) = X_E / R_E$	1.152	0	0.26
$V_{ds,pk} / V_{DD,E}$	3.562	3.647	3.6
$I_{ds,pk} / I_{DD,E}$	2.862	2.647	2.7
f_{max}	$\sim \frac{I_{ds,max}}{56 \cdot C_E \cdot V_{DD,E}}$	$\sim \frac{I_{ds,max}}{33 \cdot C_E \cdot V_{DD,E}}$	$\sim \frac{I_{ds,max}}{37 \cdot C_E \cdot V_{DD,E}}$

3

THE PRACTICAL TRANSCONDUCTANCE MODEL DESCRIPTION

The previous discussion and equations for the design of class-E amplifiers are valid directly under the assumption of ideal switches. However, practical switching transistors are not ideal switches (especially at microwave frequencies) but rather transconductance devices aiming at operating as switches. In this case, the class-E amplifier can be better depicted as the circuit in Fig. 3.7 which employs the transistor model described earlier in Section 3.2. The same design equations (3.4)-(3.9) are applicable as long as some considerations are made related to the limitations of the practical transistor switches, in particular with respect to their maximum voltage swing ($V_{ds,max}$), current ($I_{ds,max}$) and operating frequency (ω_{max}). Although other non-idealities such as finite "on" and "off" resistances affect the maximum achievable efficiency [77], these loss mechanisms are neglected here for simplicity.

The maximum allowable voltage swing is mainly constrained by the drain-source breakdown voltage of the practical transistor switch. Since such voltage swing is about 3.6 times the DC-supply voltage as indicated in Table 3.1, the latter must be properly scaled down in order to prevent exceeding the breakdown limit.

The maximum drain current $I_{ds,max}$ in a practical device imposes some constraints on the capacitor C_E and the operating frequency ω in order to maximize both efficiency and output power for a given technology and transistor size. From (3.6) and $K_C(q)$ in Table 3.1, the output power can also be expressed as

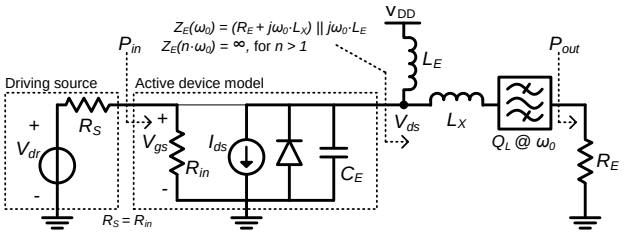


Figure 3.7: Schematic of the stand-alone class-E branch amplifier using the transconductance large-signal transistor model described at the beginning of this chapter.

$$P_{out,E} = \frac{K_P(q)}{K_C(q)}\omega \cdot C_E \cdot V_{DD,E}^2 \tag{3.10}$$

which saturates at a finite value imposed by a maximum allowed frequency ω_{max} and a given C_E (which is preferably implemented fully by the C_{out} of the device). Among other factors, this frequency is determined by the maximum current $I_{ds,max}$ through the switching transistor, which during operation must be able to sink the required peak current $I_{ds,pk}$ determined by the load network in order to preserve the current and voltage waveforms (depicted later in Fig. 3.10). A relationship between $I_{ds,pk}$, C_E and ω can be derived from the assumption of maximum efficiency as follows. For the ideal 100% efficiency, the DC power is equal to the RF power and hence

$$P_{DC,E} = I_{DD,E} \cdot V_{DD,E} = P_{out,E} \tag{3.11}$$

$$I_{DD,E} = \frac{K_P(q)}{K_C(q)}\omega \cdot C_E \cdot V_{DD,E} \tag{3.12}$$

and by using $I_{ds,pk}/I_{DD,E} = \gamma$, where $\gamma \approx 2.7$ according to Table 3.1, then

$$I_{ds,pk} = \gamma \cdot \frac{K_P(q)}{K_C(q)}\omega \cdot C_E \cdot V_{DD,E} \tag{3.13}$$

This last result shows the relationship between the (ideal) maximum operating frequency ($\omega = \omega_{max}$) of the class-E amplifier with the maximum current through the transconductance-based switch ($I_{ds,pk} = I_{ds,max}$), which after substituting these terms can be expressed as[7]

$$\omega_{max} = \frac{I_{ds,max}}{\gamma \cdot C_E \cdot V_{DD,E}} \frac{K_C(q)}{K_P(q)} \tag{3.14}$$

This is, ω_{max} is the maximum operating frequency at which the shunt capacitance C_E can be completely discharged due to current restrictions in the switching device. At higher frequencies, a switch current $I_{ds,pk}$ larger than $I_{ds,max}$ would need to be sunk and if not, then losses would arise degrading the efficiency. If the operating frequency is lower than ω_{max}, then the switching transistor is simply sub-utilized ($I_{ds,pk} < I_{ds,max}$) leading to lower output power[8]. At ω_{max}, maximum output power is generated while the ideal efficiency is maintained. In the ideal 100% efficiency conditions, this maximum output power is simply given by

$$\left(P_{out,E}\right)_{max} = V_{DD,E} \cdot I_{ds,max}/\gamma \approx \frac{V_{ds,max} \cdot I_{ds,max}}{9.7} \tag{3.15}$$

An important implication of (3.14) is that ω_{max} is mainly constrained by the device technology (since the breakdown voltage, and hence $V_{DD,E}$, as well as the ratio

[7] [88] derived the expression of ω_{max} for the particular case of $q = 0$ (RF-choke class-E) and [86] for $q = 1.41$ (parallel-circuit class-E), while (3.14) is the generalization for all q's.

[8] In these conditions, adding an external capacitance can restore the output power. This is equivalent to reducing ω_{max} by such an external capacitance.

$I_{ds,max}/C_E$ are constants if C_E is implemented fully by the C_{out} of the device) with a weaker dependency on the selection of q. Simplified expressions of (3.14) for the three cases of interest of q are shown at the bottom of Table 3.1. In theory, however, it is still possible to operate the device at higher frequencies but with lower yet reasonable efficiencies by redesigning the load network. For example [77]: up to $2.5 \times \omega_{max}$, the efficiency can be higher than with class-F3 operation (i.e. three controlled harmonics); and up to $3.1 \times \omega_{max}$, the efficiency can be similar to the one of class-B.

DRIVING CONDITIONS FOR THE TRANSCONDUCTANCE MODEL

The transconductance device shown in Fig. 3.7 can act as a switch if it is (over) driven with a sinusoidal wave or driven directly with a squared drive with sufficient amplitude (e.g. coming from a dedicated switching driver). For proper switching action, the active device must transition quickly from the cut-off region to the deep-triode region. However, real transistors have finite transition times that can become a significant portion of the RF cycle. These finite times are mainly due to the time delay at the input of the transistor (determined by the channel charge process) and can cause some losses because of a short transition through the active state region [77]. Fortunately, it has been demonstrated that for class-E, trapezoidal waveforms with significant transition times can cause minor degradation of efficiency (e.g. a degradation of 1% for on-off/off-on transitions of about 5% the RF cycle each [77]). In the device model adopted in this chapter, the frequency limitations due to the input time constants are neglected and the driving is considered sinusoidal (to ease comparisons with class-B amplifiers employing the same device model), as illustrated in Fig. 3.8. This figure shows two driving cases of interest that will be used later in Section 3.5.2: a 60% amplitude overdrive condition (that minimizes the on-off/off-on transition times to about 11% of the RF cycle and hence increases drain-efficiency), and a reduced-amplitude condition at the onset of overdrive (that reduces input power in order to increase the total-efficiency at the expense of reduced drain-efficiency). Note that the latter case represents the same driving conditions as for the class-B amplifier at maximum linear output power.

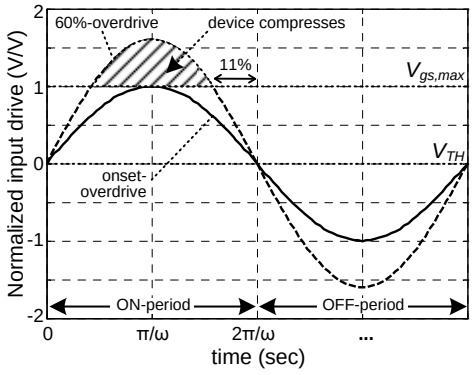


Figure 3.8: Sinusoidal driving for class-E transconductance amplifiers.

SIMULATION RESULTS FOR THE TRANSCONDUCTANCE MODEL

Using the same 20 dB-gain transconductance device of Section 3.2 (recall that in this model, the operating power gain is defined for class-B using $R_{in,B}$ in (3.2) and is maintained here), Fig. 3.9 shows the efficiency, power gain and output power[9] responses versus normalized sinusoidal input voltage $\overline{V_{gs}}$ for the circuit in Fig. 3.7. Also, Fig. 3.10 shows the load-line and the familiar voltage and current waveforms of the class-E amplifier when η_{DE} approaches 100% in Fig. 3.9. The particular results in both Fig. 3.9 and Fig. 3.10 correspond to the "load-insensitive" ($q = 1.3$) class-E amplifier at ω_{max}.

Observe in Fig. 3.9 that even though the active device is not an ideal switch, the expected high efficiency of class-E is reached at $\overline{V_{gs}} \gg 1$, which represents an overdriven sinusoidal. At the specific condition of 60% overdrive, $\eta_{DE} \approx 95\%$ and $\eta_{TOT} \approx 91\%$ with an effective power gain of about 14.5 dB, performing fairly close to the ideal class-E but now with a limited-gain device. Overall, this condition has a 3 dB lower gain and 1.5 dB lower output power with respect to the same device in class-B when using the same breakdown voltage limit[10].

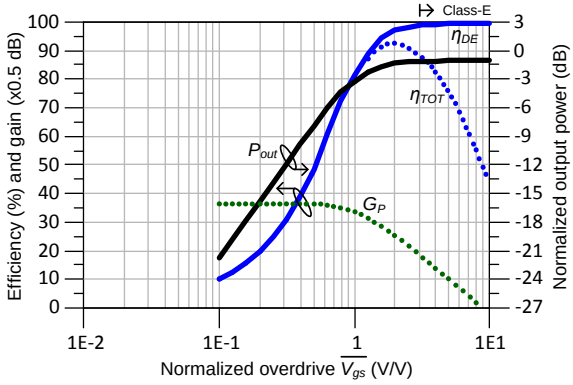


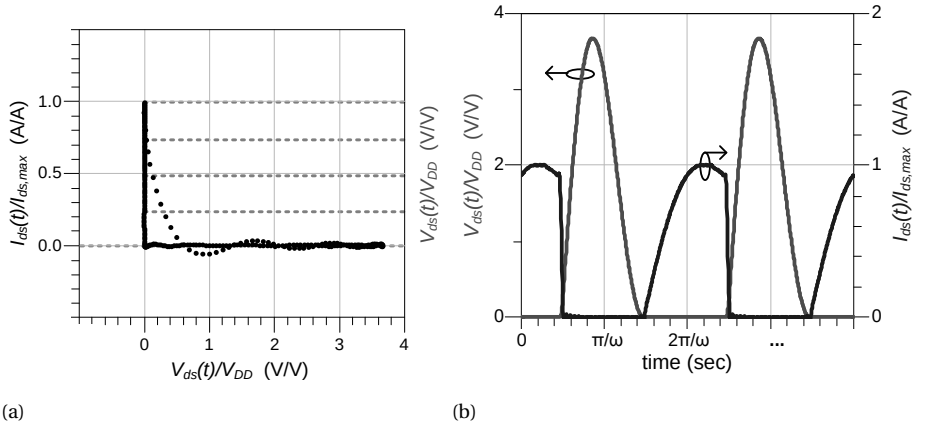
Figure 3.9: Harmonic-balance simulation results of the class-E amplifier in Fig. 3.7 versus normalized input drive $\overline{V_{gs}}$: shown are drain- and total-efficiency, output power (normalized with respect to the maximum linear power of the previous class-B amplifier, for reference) and power gain.

[9] The output power in class-E is also normalized with respect to the maximum linear power in class-B for reference and for comparison.

[10] For completeness, it is interesting to calculate the difference in output power between an ideal class-E amplifier (i.e. with a very large overdrive condition) and an ideal class-B amplifier (at the onset of overdrive), employing the same device constraints of $V_{ds,max}$ and $I_{ds,max}$. In terms of those parameters, the maximum (linear) output power in class-B is given by

$$\left(P_{out,B}\right)_{max} = \frac{V_{DD,B}^2}{2 \cdot R_{opt,B}} = \frac{V_{ds,max} \cdot I_{ds,max}}{8} \tag{3.16}$$

which is about 0.9 dB higher than the one of class-E given in (3.15). Note that this value is the saturated output power level indicated in Fig. 3.9.



(a) (b)

Figure 3.10: Response of the class-E amplifier in Fig. 3.7 when $\eta_{DE} \approx 100\%$ in Fig. 3.9: a) normalized load-line, b) normalized voltage and current waveforms.

3.4. DOHERTY AMPLIFIERS

The Doherty amplifier [18] (DPA) is used in this chapter as a benchmark to compare the results for the outphasing amplifiers in terms of efficiency performance. Although a comprehensible treatment of this amplifier can be found elsewhere [16, 89], Fig. 3.11 depicts a general schematic of this amplifier able to represent both "symmetric" and "asymmetric" DPA implementations. For the "symmetric" DPA, both the main and the peaking devices have the same size (i.e., $r = 1$ in Fig. 3.11) and the efficiency peaks at 6 dB back-off. In turn, for the "asymmetric" DPA, the peaking device is larger by "r" times than the main device in order to move the efficiency peak at deeper back-off levels. In this chapter, a 1:2 devices size ratio (i.e., $r = 2$) is considered for the asymmetric DPA because this sets the back-off efficiency at about 9.5 dB which is similar to the case of the outphasing amplifiers of the next section.

The ideal operation of the Doherty amplifiers is considered when using class-B for both the main and peaking branch amplifiers, as depicted at the center of Fig. 3.11, and the turn-off of the peaking amplifier is accomplished by using separate dedicated drive profiles for both amplifiers. As describer earlier in Subsection 3.3.1, R_{opt} (given by (3.3)) is the optimum load for these class-B amplifiers and the quarter-wavelength lines act as a DC-feed and provide even harmonic shorts. The output capacitance C_{out} of the devices can be absorbed by the so-called impedance inverter when using a quasi-lumped quarter-wavelength transmission line [26] with line impedance $Z_{tr} = R_{opt}$ (as long as $C_{out} < \frac{1}{Z_{tr} \cdot \omega_0}$). For the asymmetric DPA case, the transistor model for the peaking device need to be scaled by r[11] and therefore the transconductance are g_m and $r \times g_m$ for the

[11] In this case, the output capacitance of the peaking device is assumed to be also perfectly compensated for by the quasi-lumped transmission line. Here for simplicity, as shown in Fig. 3.11, such capacitor is not scaled by r.

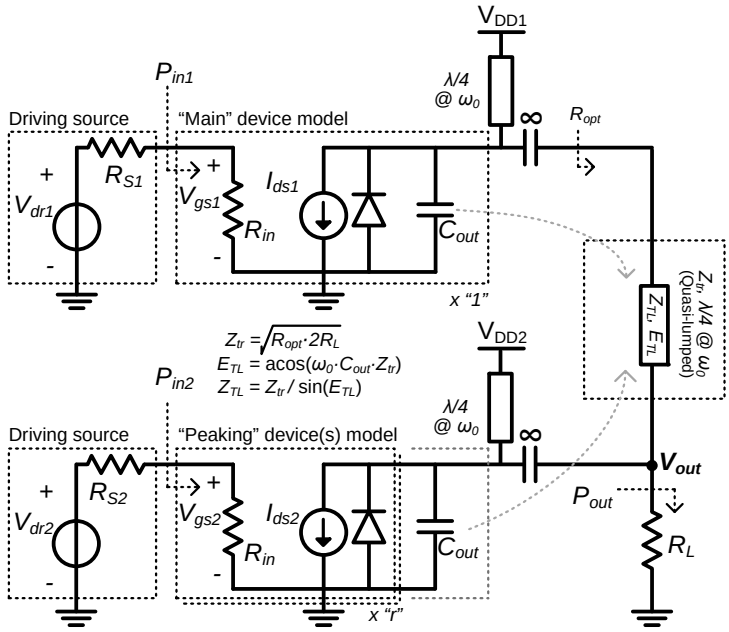


Figure 3.11: Schematic of the class-B Doherty amplifier with $1:r$-devices size ratio.

main and the peaking devices, respectively. The final load is given by $R_L = R_{opt}/(1+r)$.

The ideal normalized drive profiles for both devices $V_{gs,\text{main}}$ and $V_{gs,\text{peak}}$ (V_{gs1} and V_{gs2} in Fig. 3.11, respectively) are given according to

$$V_{gs,\text{main}}(t) = \overline{V_{in}(t)} = \overline{E(t)} \cdot e^{j\varphi(t)} \tag{3.17}$$

$$V_{gs,\text{peak}}(t) = \begin{cases} 0, & \text{for } |\overline{V_{in}(t)}| < \frac{1}{1+r} \\ \left[\left(\frac{1+r}{r}\right) \cdot \overline{E(t)} - \frac{1}{r}\right] \cdot e^{j(\varphi(t)-\pi/2)}, & \text{for } |\overline{V_{in}(t)}| \geq \frac{1}{1+r} \end{cases} \tag{3.18}$$

where $V_{in}(t)$ is the original complex modulated signal with normalized envelope $\overline{E(t)}$ and phase $\varphi(t)$. Note that $V_{gs,\text{main}}$ is simply a replica of $\overline{V_{in}(t)}$. In turn, $V_{gs,\text{peak}}$ is a piece-wise defined function with respect to the magnitude of $V_{in}(t)$. For $|\overline{V_{in}(t)}| \geq \frac{1}{1+r}$, the magnitude of $V_{gs,\text{peak}}$ is a scaled and level-shifted version of the magnitude of $\overline{V_{in}(t)}$ while the phase of $V_{gs,\text{peak}}$ is a $-90°$ shifted version of the phase of $V_{in}(t)$ to compensate for the quarter-wavelength inverter.

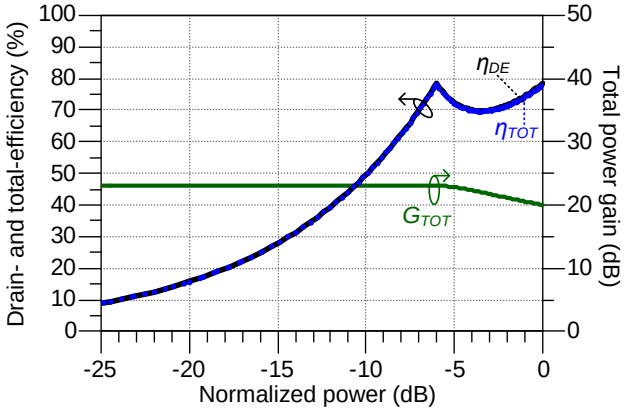
The simulation results for the instantaneous efficiencies (η_{DE} and η_{TOT}) of both the symmetric and asymmetric DPA are depicted in Fig. 3.12 when using the 20 dB-gain transistor model of this chapter. In this figure, η_{TOT} practically overlaps η_{DE} due to the use of high-gain devices[12]. Additionally, this figure plots the total-gain G_{TOT} of the am-

[12] In fact, this is also true for the simulations of all the other class-B outphasing operating modes that will be shown later in this section. In [60], however, these simulations are given for 10 dB-gain devices and there η_{TOT} distinguishes more clearly from η_{DE}.

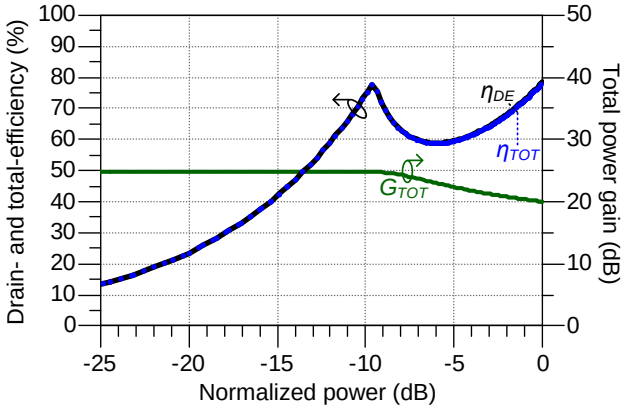
plifier that is defined according to

$$G_{TOT} = \frac{P_{out}}{\sum P_{in}} \tag{3.19}$$

where the total input power is given by $\sum P_{in} = P_{in1} + P_{in2}$. Later, in Section 3.6, the average efficiencies $\eta_{DE,av}$ and $\eta_{TOT,av}$ resulting for the two Doherty amplifier cases are examined under signals with different PAPR levels.



(a) Symmetric class-B Doherty amplifier.



(b) Asymmetric (1:2) class-B Doherty amplifier.

Figure 3.12: Envelope simulation results of the class-B Doherty amplifier in a) symmetric operation and b) asymmetric operation (1:2-devices size ratio).

3.5. OUTPHASING AMPLIFIERS

The outphasing amplifier can employ highly nonlinear but efficient branch amplifiers in order to allow simultaneously an efficient and linear amplifier architecture [19, 27]. Historically, class-B was the first practical choice for the branch amplifier implementation in outphasing architectures [20] even though switch-mode amplifiers like class-E could make a better choice [40]. For long, the use of class-E in outphasing amplifiers was considered to be non-trivial [41]. It was until recently that practical outphasing amplifiers using class-E successfully appeared in literature [28,40,65]. Later, Chapter 7 will describe in detail one of these implementations [29, 65].

In this section, the design of outphasing amplifiers using both class-B and class-E branch amplifiers will be detailed using the simplified transistor model described previously. For the class-B branch amplifier implementations, three different outphasing operating modes will be considered: *saturated* class-B and *linear* class-B with pure-phase control (although the first one is a suboptimal implementation, both are referred to as "pure-mode" outphasing) and *linear* class-B with output phase and amplitude control (referred to as "mixed-mode" outphasing) [51, 59]. When dealing with class-E branch amplifiers, only pure-phase control will be considered with two slightly different amplitude levels for the driving signals of the branch amplifiers in order to improve the achievable total-efficiency.

3.5.1. OUTPHASING WITH CLASS-B BRANCH AMPLIFIERS

A general schematic for the outphasing amplifier using class-B is depicted in Fig. 3.13. As described earlier, the quarter-wave transmission lines at the devices' drain act as DC-feed and provide even harmonic shorts. The power combiner is formed by two quasi-lumped quarter wave transmission lines in order to absorb the active devices' C_{out}. The branch amplifiers are driven by voltage sources $V_{dr1,2}$ with finite output impedance R_S, which is assumed to be conjugate-matched to the active devices' inputs ($R_S = R_{in}$). These sources directly set $V_{gs1,2} = \left(\frac{R_{in}}{R_S+R_{in}}\right) V_{dr1,2}$, which in turn determine the specific operating mode of the amplifier. The shunt elements $\pm jB_{\theta c}$ are the Chireix compensating elements for efficiency enhancement.

For the class-B outphasing amplifier, two different operating modes have been proposed in literature: pure-mode (phase-only) and mixed-mode (phase and amplitude). The pure-mode is the original and basic outphasing modulation control where the outphasing amplifier's output power is controlled by means of only phase [19,27]. In mixed-mode [51, 59], the input driving signal changes from (pure-mode) outphasing operation to amplitude modulation in deep back-off in order to increase efficiency. Specifically, this means that amplitude control replaces phase control beyond a certain level of back-off, or equivalently, beyond a certain outphasing threshold angle θ_{th} [51]. This dedicated control avoids device operation with very reactive loading conditions while saving input drive power. In turn, this combination improves significantly both drain- and total-

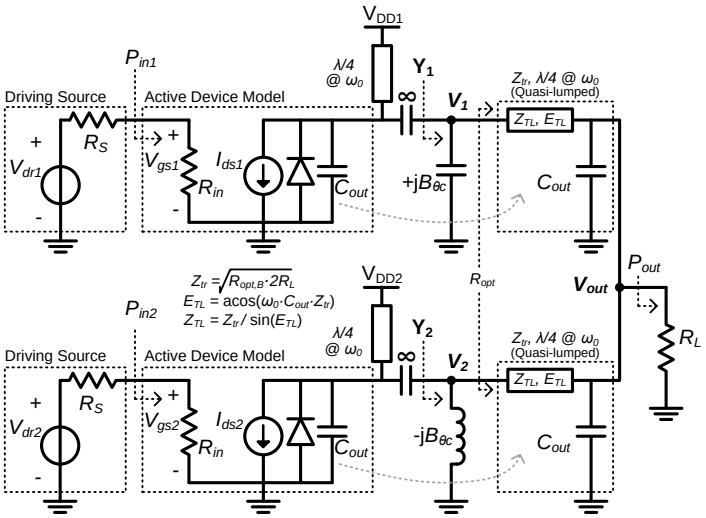


Figure 3.13: Schematic of the class-B Chireix outphasing amplifier with a transmission line-based combiner.

efficiency but requires linear branch amplifiers (i.e. amplifiers whose output amplitude is controllable by its input amplitude) that are sufficiently efficient (e.g. class-B). Therefore, a mixed-mode outphasing amplifier operates its branch amplifiers first in pure-outphasing mode from peak-power up to a certain back-off level given by θ_{th}, and then in their normal "linear-mode" at deeper back-off levels. Both the Chireix compensation angle θ_c and the mixed-mode's threshold angle θ_{th} are set to maximize efficiency for the complex modulated signal of interest [51]. Even though [59] and [51] introduced the idea of "mixed-mode" operation, these works did not provide the explicit analytical expressions for the required driving signals when using transconductance devices. Therefore, these equations are derived here for the case of ideal class-B branch amplifiers.

The ideal instantaneous drain-efficiency versus back-off for both the "pure-mode" and the "mixed-mode" class-B outphasing amplifier is illustrated in Fig. 3.14 [51]. For comparison, this figure also includes the ideal efficiency for the asymmetrical (1:2) Doherty amplifier of the previous section. In Fig. 3.14, the efficiency of the class-B outphasing amplifiers was maximized at around 10 dB back-off (with $\theta_c = 71.6°$ and $\theta_{th} = 73.2°$). Note in the figure that the efficiency of the mixed-mode amplifier is the highest at all back-off levels and that it is a combination of the "pure-mode" outphasing efficiency up to θ_{th} and the normal "linear-mode" class-B efficiency beyond θ_{th}.

The behavior of both the pure-mode and the mixed-mode outphasing amplifiers is described by the (normalized and baseband-equivalent) amplified branch signals $\overline{V_{1,2}}$ in Fig. 3.13, which can be expressed as [51]

$$\overline{V_{1,2}(t)} = \begin{cases} e^{j[\varphi(t) \pm \theta(t)]}, & \text{for } \theta(t) \leq \theta_{th} \quad (3.20a) \\ \alpha(t) \cdot e^{j[\varphi(t) \pm \theta_{th}]}, & \text{for } \theta(t) > \theta_{th} \quad (3.20b) \end{cases}$$

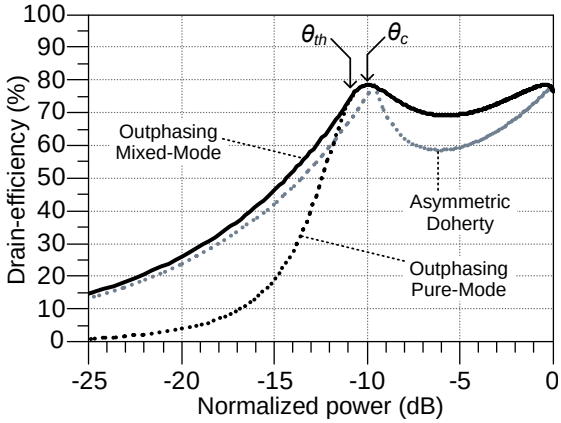


Figure 3.14: Instantaneous drain-efficiency for several ideal class-B amplifiers versus normalized power back-off: stand-alone class-B, asymmetrical Doherty and outphasing in both pure-mode and mixed-mode operation.

where $\theta(t)$ is the outphasing angle and $\alpha(t)$ is the amplitude control coefficient for mixed-mode, both given by

$$\theta(t) = \arccos(\overline{E(t)}) \tag{3.21}$$

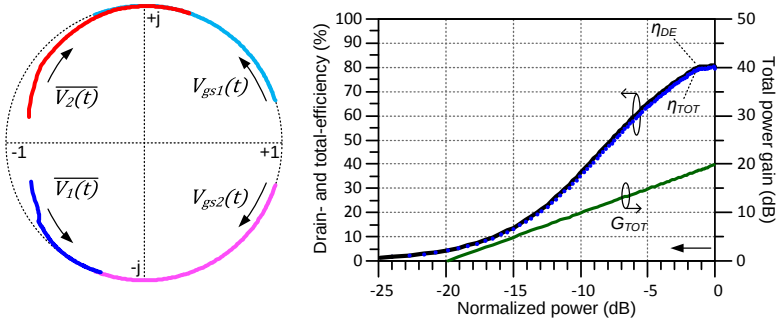
$$\alpha(t) = \overline{E(t)} / \cos(\theta_{th}) \tag{3.22}$$

in which $\varphi(t)$ and $\overline{E(t)}$ are the original phase and (normalized) envelope information, respectively. Note that since the circuit in Fig. 3.13 uses "additive" combining, (3.21) and (3.22) are expressed in terms of cosine functions as indicated previously in Section 2.2. In addition, note in (3.20) that the "pure" outphasing mode is described by either (3.20a), or by (3.20) after setting $\theta_{th} > \pi/2$ since $0 \leq \theta(t) \leq \pi/2$ from (3.21).

In order to achieve the expected behavior described in (3.20) at the $\boldsymbol{V_{1,2}}$ nodes of Fig. 3.13, specific profiles must be provided by the driving signals $V_{gs1,2}$ because of the transconductance nature of the active devices as explained next.

SATURATED CLASS-B

If the driving signals $V_{gs1,2}(t)$ are simply phase-modulated without any consideration on the actual transconductance nature of the active devices from input to output, then the class-B branch amplifiers will not perform ideally and will even eventually be driven in saturation due the increasing complex load at back-off and the lack of amplitude control. This is illustrated in Fig. 3.15. Fig. 3.15a depicts both the normalized driving signals $V_{gs1,2}(t)$ and the resulting $\overline{V_{1,2}(t)}$ signals at the $\boldsymbol{V_{1,2}}$ nodes of Fig. 3.13, where it can be observed that only the first ones are perfectly phase-modulated. This breaks the initial assumption of voltage-source behavior from the branch amplifiers and therefore a significantly degraded efficiency performance is observed in Fig. 3.15b that provides the resulting η_{DE}, η_{TOT} and G_{TOT} versus power back-off. Although the efficiency performance versus back-off is better than the one of a stand-alone class-B amplifier as shown



(a) (b)

Figure 3.15: Harmonic-balance simulations of the *saturated* class-B outphasing amplifier: a) driving $V_{gs1,2}(t)$ and resulting $\overline{V_{1,2}(t)}$ signals in the complex plane, and b) simulated G_{TOT}, η_{DE} and η_{TOT} versus power back-off.

in Fig. 3.15b, this *pseudo* pure-mode operation with direct phase-modulation results in a worse efficiency performance than would occur if the transconductance transfer function of the device is really taken into account as described in the next two cases. Additionally, in Fig. 3.15b it can be observed that G_{TOT} decreases linearly with back-off since the drive power is kept constant for all power levels.

LINEAR CLASS-B

The proper drive profile of the branch amplifiers in Fig. 3.13 should consider the transconductance nature of the active devices that link the $V_{1,2}(t)$ signals, at the $\boldsymbol{V_{1,2}}$ nodes, with the driving voltages $V_{gs1,2}$. These relationships can be obtained using (3.1) and the expressions that model the outphasing operation in (3.20a), resulting in

$$V_{1,2}(t) = \frac{-I_{ds1,2}(t)}{Y_{1,2}(\theta(t))} = \frac{-g_m \cdot V_{gs1,2}(t)}{Y_{1,2}(\theta(t))} \tag{3.23}$$

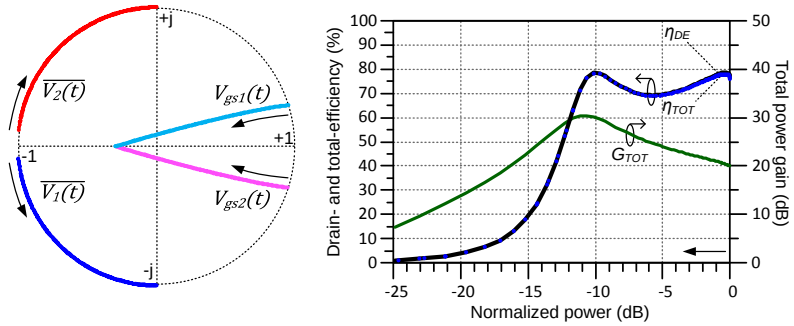
where $Y_{1,2}(\theta(t))$ is the dynamic outphasing fundamental load admittance seen by the active devices in Fig. 3.13. The admittances $Y_{1,2}$ were given previously in Subsection 2.5.3 by (2.30)-(2.33) and are repeated here for convenience ($R_{PA} = R_{opt,B}$):

$$Y_{1,2}(\theta(t)) = G(\theta(t)) \mp j\left[B(\theta(t)) - B_{\theta c1,2}\right] \tag{3.24}$$

$$G(\theta(t)) = \left(\frac{1}{R_{opt,B}}\right) \cdot \cos^2(\theta(t)) \tag{3.25}$$

$$B(\theta(t)) = \left(\frac{1}{R_{opt,B}}\right) \cdot \frac{\sin(2 \cdot \theta(t))}{2} \tag{3.26}$$

$$B_{\theta c} = B(\theta_c) \tag{3.27}$$



(a) (b)

Figure 3.16: Harmonic-balance simulations of the *linear* class-B outphasing amplifier: a) driving $V_{gs1,2}(t)$ and resulting $\overline{V_{1,2}(t)}$ signals in the complex plane, and b) simulated G_{TOT}, η_{DE} and η_{TOT} versus power back-off..

Therefore, the drive profile that ensures the active devices to remain in *linear* class-B (i.e. at maximum output swing but still in the linear region) while in pure-mode outphasing is given by (assuming unitary $V_{gs,max}$)

$$V_{gs1,2}(t) = \overline{Y_{1,2}(\theta(t))} \cdot e^{j[\varphi(t) \pm \theta(t)]} \tag{3.28}$$

where the normalization $\overline{Y_{1,2}(\theta(t))} = Y_{1,2}(\theta(t)) \cdot R_{opt,B}$ is needed to cancel out g_m in (3.23) ($R_{opt,B} = \frac{2 \cdot V_{DD}}{g_m \cdot V_{gs,max}}$ from (3.3) [13]). Note that the driving signals in (3.28) are no longer phase-modulated signals but rather include the amplitude-modulated unitless factor "$\overline{Y_{1,2}(\theta(t))}$" that is responsible for the current-to-voltage transformation that make the transconductance devices act as voltage sources at the $\boldsymbol{V_{1,2}}$ nodes in Fig. 3.13, as required.

Fig. 3.16 shows the harmonic-balance simulations of the class-B outphasing amplifier in Fig. 3.13 with the pure-mode control described in (3.28). Fig. 3.16a illustrates the driving signals $V_{gs1,2}(t)$ along with the corresponding resulting (and normalized) $V_{1,2}(t)$ signals. Note in this figure that, thanks to the specific profiles of $V_{gs1,2}(t)$, $\overline{V_{1,2}(t)}$ are indeed phase-modulated signals as described by (3.20a)[14]. Fig. 3.16b provides the resulting η_{DE}, η_{TOT} and G_{TOT} versus power back-off. First, it can be observed that now the efficiency performance is indeed as expected from the ideal outphasing amplifier. In addition, it can be observed that the G_{TOT} has a distinct profile due to the amplitude-modulation component of the input drive signal: it starts at 20 dB at peak power (as expected from the individual device's gain), then increases 10 dB more before reducing again at deep back-off levels. The initial gain increase is due to the (linear, for reference) increase of the load impedance with back-off while maintaining $V_{1,2}(t)$ constant with a

[13] As can be appreciated in Fig. 3.13, $R_{opt,B}$ is also given by $R_{opt,B} = \frac{Z_{tr}^2}{2R_L}$, but this expression is used to calculate Z_{tr} for a given R_L, or vice versa.

[14] As appreciated in Fig. 3.16a, the phases of $V_{gs1,2}(t)$ are not zero at peak power (i.e. when $\theta(t) = 0$) due to the Chireix compensation elements (i.e. the finite $B_{\theta c}$ term within $\overline{Y_{1,2}}$ in 3.28).

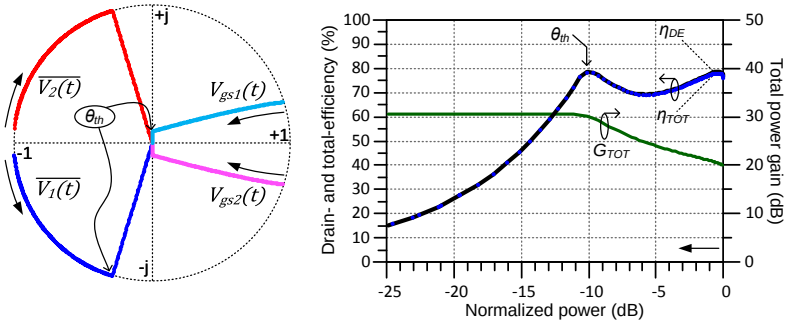


Figure 3.17: Harmonic-balance simulations of the *linear* class-B outphasing amplifier in "mixed-mode": a) driving $V_{gs1,2}(t)$ and resulting $\overline{V_{1,2}(t)}$ signals in the complex plane, and b) simulated G_{TOT}, η_{DE} and η_{TOT} versus power back-off.

(linear) reduction of input drive V_{gs}, see (3.23) and Fig. 3.16a, causing a faster (squared) drop in total input power than in output power (linear drop). The subsequent reduction in gain is due to the increasing amplitude of V_{gs} (left half-plane in Fig. 3.16a) while trying to keep $V_{1,2}(t)$ constant despite the increasing reactive loading at deeper back-off levels.

LINEAR CLASS-B WITH MIXED-MODE CONTROL

The "mixed-mode" outphasing operation indicated in (3.20) can be accomplished with the following drive profiles while maintaining the class-B branch amplifiers in their *linear* regime:

$$V_{gs1,2}(t) = \begin{cases} \overline{Y_{1,2}(\theta(t))} \cdot e^{j[\varphi(t) \pm \theta(t)]}, & \text{for } \theta(t) \le \theta_{th} \quad (3.29a) \\ \dfrac{\overline{E(t)}}{\cos(\theta_{th})} \cdot \overline{Y_{1,2}(\theta_{th})} \cdot e^{j[\varphi(t) \pm \theta_{th}]}, & \text{for } \theta(t) > \theta_{th} \quad (3.29b) \end{cases}$$

Note that, ignoring $\varphi(t)$, (3.29b) is simply a straight line function of $\overline{E(t)}$ that connects (3.29a) at $\theta(t) = \theta_{th}$ to the origin of the complex plane, just like (3.20b) and (3.22).

Fig. 3.16 shows the harmonic-balance simulations of the class-B outphasing amplifier in Fig. 3.13 with the mixed-mode control described in (3.29). Specifically, Fig. 3.17a illustrates the driving signals $V_{gs1,2}(t)$ in (3.29) along with the resulting (and normalized) $V_{1,2}(t)$ signals, while Fig. 3.16b provides the resulting η_{DE}, η_{TOT} and G_{TOT} versus power back-off. Note in this case that beyond the back-off point set by θ_{th} (at about 73°, or equivalently at 11 dB back-off as shown), the $\overline{V_{1,2}(t)}$ signals in Fig. 3.17a are indeed amplitude-modulated and, as a result, the efficiency shown in Fig. 3.17b is significantly improved at deep back-off with respect to the pure-mode due to the less reactive loading of the active devices and such amplitude control. As a direct consequence of this, after its initial increase, G_{TOT} remains constant at deeper back-off levels beyond θ_{th}.

3.5.2. OUTPHASING WITH CLASS-E BRANCH AMPLIFIERS

A general schematic for the outphasing amplifier using class-E for the branch amplifiers is depicted in Fig. 3.18. This circuit employs subtractive combining by means of an ideal transformer-based power combiner and shunt Chireix compensating elements $\pm jB_{\theta c}$ for efficiency enhancement. The branch amplifiers are designed as "load-insensitive" class-E ($q \approx 1.3$ in Subsection 3.3.2 and Table 3.1) in order to absorb the active devices' output capacitance (i.e., $C_{out} = C_E$ operating at ω_{max}) and because, as its name suggests, the ideal efficiency performance for this specific amplifier class does not degrade significantly with the (ohmic) load modulation of the outphasing modulation [28, 29]. A comprehensible treatment of the load-insensitive class-E branch amplifier is given later in Subsection 7.2.2. In Fig. 3.18, the harmonic terminations required for the class-E branch amplifiers are provided by a common bandpass filter which is shifted towards the load. This filter can be as simple as an LC-filter with high-Q_L (in this case $Q_L = 10$) or more complex for extended bandwidths. For the analysis in this section, the inputs are assumed to be conjugate-matched and the active devices are operated in their saturated and most efficient region with input control signals that are simply phase-modulated:

$$V_{gs1,2}(t) = \overline{V_{gs}} \cdot e^{j[\varphi(t) \pm \theta(t)]} \tag{3.30}$$

where $\overline{V_{gs}}$ (see Fig. 3.4) represents the amplitude drive level. Two representative conditions that keep the branch amplifiers sufficiently saturated and with high efficiency are considered here: 60%-overdrive (i.e., $\overline{V_{gs}} = 1.6$) and onset-overdrive (i.e. $\overline{V_{gs}} = 1$). While the first condition maximizes drain-efficiency, the second one maximizes total-efficiency.

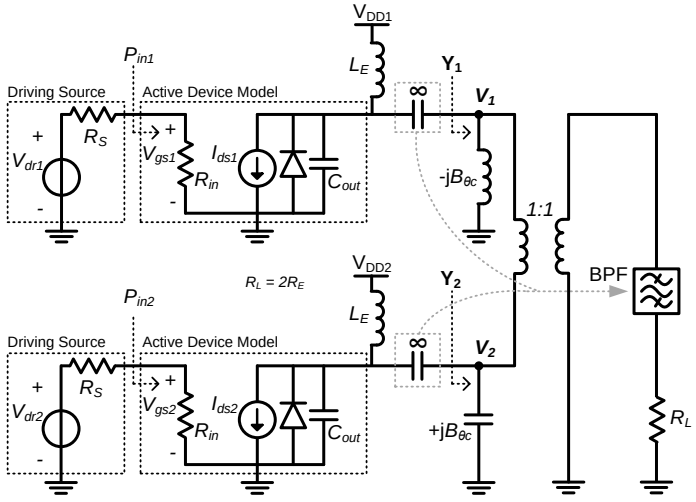


Figure 3.18: Schematic of the class-E Chireix outphasing amplifier with a transformer-based power combiner.

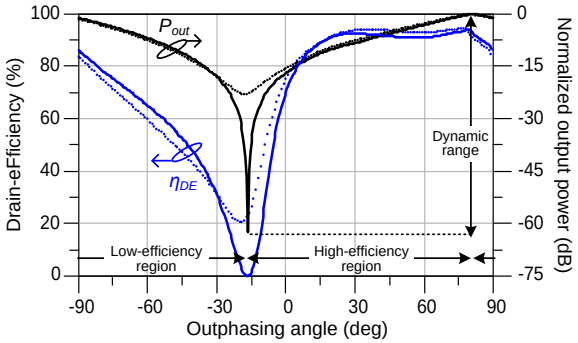


Figure 3.19: Instantaneous efficiency and power response of the amplifier in Fig. 3.18 versus outphasing angle. The dotted and solid lines correspond to the responses before and after branch amplitude equalization, respectively.

As described previously in Subsection 2.7.4, the outphasing branch amplifiers need to be accurately balanced in terms of both amplitude and phase in order to allow linear amplification. While phase imbalances can be corrected with (static) phase offsets in the driving signals, any amplitude imbalance will limit directly the maximum controllable power range and hence will affect linearity (i.e., will cause in-band distortion and out-of-band spectral regrowth [71,72]). For the class-B branch amplifiers of the previous section this is less of an issue because, ideally, these amplifiers react equally to both signs of the complex-valued dynamic load admittance $Y_{1,2}(\theta(t))$ from the outphasing action. On the contrary, amplitude imbalances are expected for the class-E branch amplifiers since, even in ideal conditions, they react differently to the opposite dynamic susceptance in $Y_{1,2}(\theta(t))$, delivering slightly different power levels that manifest themselves as "amplitude" imbalances at back-off. Therefore, in the presence of amplitude imbalances, the combined power cannot be perfectly nulled at the out-phased condition and explicit counter-measures need to be applied. As an illustration, Fig. 3.19 shows the instantaneous power and efficiency response to an entire 180-degree sweep of the outphasing angle for the amplifier in Fig. 3.18. The dotted and solid lines correspond to the responses before and after branch amplitude balancing or equalization, respectively. Balancing the amplitudes of the branches can be done in different ways, for example via small independent duty-cycle adjustments for digital drives or via a small differential DC-supply adjustment between the branches for analogue drives. For simplicity, the latter option was used here, recognizing that the efficiency performance of class-E amplifiers is not very sensitive to the supply voltage. The solid traces in Fig. 3.19 show that with balancing the power dynamic range improves significantly (e.g. to more than 60 dB) with minor efficiency degradation[15].

Note also in Fig. 3.19 that two very distinctive efficiency regions at back-off power levels can be appreciated due to the employed 180-degree sweep of the outphasing an-

[15]The simulated amplifiers in this section have not been extensively optimized because the goal is to demonstrate general trends on performance. Still, for this example, the Chireix compensation angle was adjusted for large PAPR signals.

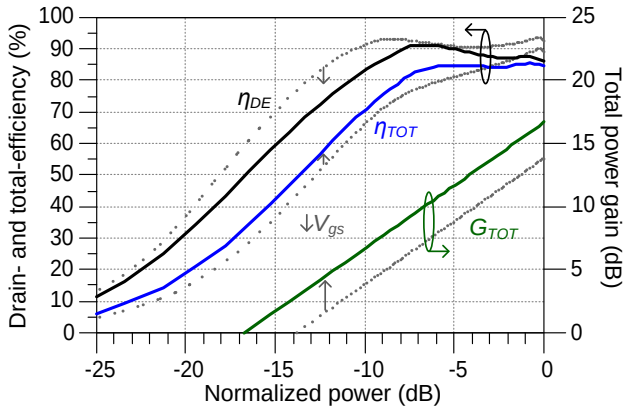


Figure 3.20: Harmonic-balance simulation results of the class-E outphasing amplifier, showing instantaneous efficiencies and total power gain versus normalized power. The dotted and solid-thick lines correspond to the 60%-overdrive and onset-overdrive conditions, respectively, illustrating the effect of reducing the drive amplitude.

gle. However, only one of them is desired in terms of high-efficiency performance, while the other should be entirely avoided. The desired region of operation corresponds to the positive angles of θ (after accounting for the phase offset seen in Fig. 3.19) for the established Chireix compensation elements shown in Fig. 3.18 since in the ideal outphasing modulation $0 \leq \theta \leq \frac{\pi}{2}$ (see (2.5) in Section 2.2). The other region (called "low-efficiency" region in Fig. 3.19) reverses the sign of the Chireix compensation and leads to inefficient operation. The required phase discrimination must be done by the “signal component separator" (SCS) that provides each branch with the proper driving signals after processing the original complex modulated signal.

Using the 20-dB gain devices of this chapter, Fig. 3.20 shows the simulated instantaneous efficiencies η_{DE} and η_{TOT}, as well as the total-gain of the class-E outphasing amplifier of Fig. 3.18 for the two amplitude drive levels corresponding to onset-overdrive (solid thick lines) and 60%-overdrive (dotted lines) conditions. First, note that due to the finite-gain transconductance of the device and the constant drive power ((3.30)), G_{TOT} reduces linearly with back-off. Second, it can be observed that the maximum drain-efficiency is less than the ideal 100% because of the finite amplitude sinusoidal drive as anticipated in Subsection 3.3.2. For the 60%-overdrive condition, the total-gain G_{TOT} peaks at 14 dB (as expected from Fig. 3.9) and the instantaneous efficiencies are excellent (about 80% and 65% for the drain- and total-efficiency up to about 12 and 10 dB back-off, respectively[16]). It is very important to realize that this efficiency performance (especially the roll-off at back-off) cannot actually be explained solely by the net power factor of the ideal transformer combiner but rather by the interaction of such combiner and the class-E amplifiers, as previously explained in Section 2.3 by (2.12)-(2.14). Although the onset-overdrive or reduced drive condition will compromise the maximum η_{DE} compared to the 60%-overdrive case, the G_{TOT} will increase and hence the η_{TOT} will

[16]Devices with lower gain will of course yield lower total-efficiencies.

improve significantly. With respect to the 60%-overdrive condition, the onset-overdrive condition increases G_{TOT} by about 3 dB causing at 10 dB back-off an increment of about 4%-points in η_{TOT} (but a decrement of 8%-points in η_{DE}) which are significant because they will be reflected directly in the average total-efficiency for a modulated signal of similar PAR level, as will be shown in the next section.

3.6. AVERAGE EFFICIENCY COMPARISONS OF LOAD-MODULATED AMPLIFIERS

Although in the previous sections the *instantaneous* efficiency performance versus back-off power was provided for the different amplifier topologies, their actual practical performance with modulated signals is evaluated in terms of *average* efficiency, as briefly introduced earlier in Section 1.3. The average drain and total efficiencies, $\eta_{DE,avg}$ and $\eta_{TOT,avg}$, are given by [90]

$$\eta_{DE,avg} = \frac{P_{out,avg}}{P_{DC,avg}} \tag{3.31}$$

$$\eta_{TOT,avg} = \frac{P_{out,avg}}{P_{DC,avg} + \sum P_{in,avg}} \tag{3.32}$$

and depend on the probability density function PDF of the actual modulated signal. Since different modulated signals have different PDFs [13], the comparison of the average efficiency performance of the amplifiers described in this chapter needs to be done using the same type of signal. Here, a Rayleigh-distributed envelope has been chosen because this is representative for the signals used in modern base-station power amplifiers. Fig. 3.21 shows the instantaneous drain-efficiency of three amplifier topologies described earlier, together with a Rayleigh PDF with 10.5 dB PAPR that represents a W-CDMA test signal.

The Rayleigh PDF is described analytically by [90]

$$PDF_{Rayleigh}(V) = 2V\xi \exp\left(-V^2\xi\right) \tag{3.33}$$

where ξ is the signal's PAPR in linear units and V is the normalized envelope voltage. The average drain-efficiency in (3.31) can be calculated using the following expression [51, 90]

$$\eta_{DE,avg} = \frac{\int_{V_{min}}^{V_{max}} P_{out}(V) \cdot PDF(V) \cdot \mathrm{d}V}{\int_{V_{min}}^{V_{max}} P_{DC}(V) \cdot PDF(V) \cdot \mathrm{d}V} \tag{3.34}$$

where $P_{out}(V)$ and $P_{DC}(V)$ are instantaneous functions with respect to the envelope $V_{min} \leq V \leq V_{max}$ with $V_{min} \to 0$ (the output power dynamic range is given by

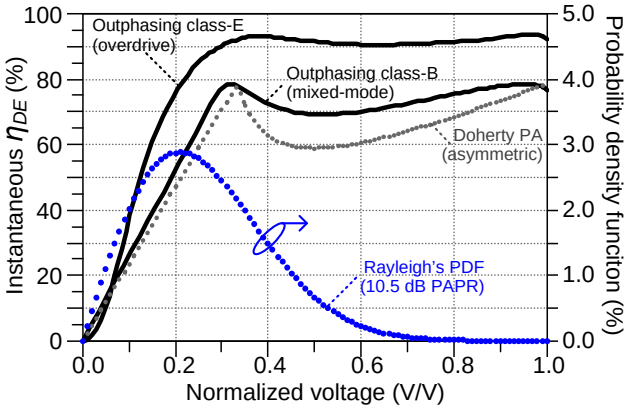


Figure 3.21: Three examples of instantaneous efficiency performance (versus normalized output voltage) from the amplifiers studied in this chapter together with a Rayleigh's PDF representing a W-CDMA test signal.

$20 \cdot \log[V_{max}/V_{min}]$). However, a more convenient expression for computation can use directly the instantaneous efficiency $\eta_{DE}(V)$ and the signal's $PDF(V)$ functions. Since $\eta_{DE}(V) = P_{out}(V)/P_{DC}(V)$ and the output power is proportional to the square of the instantaneous voltage or envelope $P_{out}(V) \propto V^2$, then (3.34) can be more conveniently expressed as

$$\eta_{DE,avg} = \frac{\int_{V_{min}}^{V_{max}} V^2 \cdot PDF(V) \cdot \mathrm{d}V}{\int_{V_{min}}^{V_{max}} \left[V^2/\eta_{DE}(V)\right] \cdot PDF(V) \cdot \mathrm{d}V} \tag{3.35}$$

Similarly, $\eta_{TOT,avg}$ can be expressed as

$$\eta_{TOT,avg} = \frac{\int_{V_{min}}^{V_{max}} V^2 \cdot PDF(V) \cdot \mathrm{d}V}{\int_{V_{min}}^{V_{max}} \left[V^2/\eta_{TOT}(V)\right] \cdot PDF(V) \cdot \mathrm{d}V} \tag{3.36}$$

Fig. 3.22 shows the result of computing both (3.35) and (3.36) for all the Doherty and outphasing amplifiers described in this chapter, employing several values of PAPR. Note, however, that the amplifiers were not optimized for those different PAPR values but rather the targeted high-efficiency operation was at 10 dB back-off (except for the symmetric Doherty PA, whose efficiency peaks at 6 dB back-off). Nevertheless, the efficiency trends in Fig. 3.22 are meaningful and give a clear view on what can be accomplished with the given amplifier concepts. In general, it can be observed in this figure that the outphasing amplifiers can reach higher efficiencies than the Doherty amplifiers. Within the outphasing PAs, the highest drain-efficiency corresponds to the use of class-E branch amplifiers although such advantage is reduced significantly when accounting for the input drive power in the total-efficiency. Note that by reducing the drive power, like in the onset-overdrive class-E case or in the mixed-mode class-B case, the total-efficiency for

the outphasing architectures is maintained high for signals with very large PAPRs. For the particular case of a PAPR level of 10.5 dB, Table 3.2 summarizes the computed average efficiencies for all the amplifier topologies described in this chapter. Additionally, these computations were verified by envelope simulations using a realistic 3GPP Test Model 1 signal [15] (a W-CDMA signal with the same 10.5 dB PAPR level [14]) and the results are also summarized in Table 3.2. Details on these latter simulations are given in the next section.

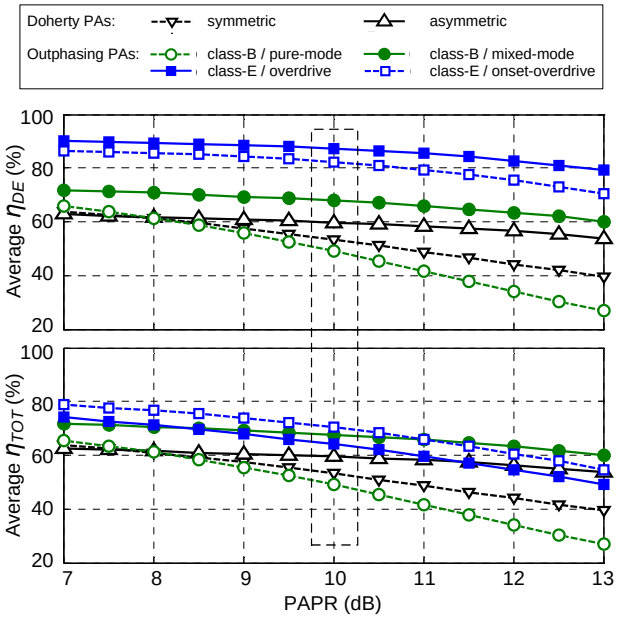


Figure 3.22: Average efficiency computation results for several Doherty and outphasing amplifiers using a Rayleigh-distributed envelope with several levels of PAPR.

Table 3.2: AVERAGE EFFICIENCY OF SEVERAL PA ARCHITECTURES USING CLASS-B AND CLASS-E BRANCH AMPLIFIERS*.

Power Amplifier Architecture	**Branch amplifier**	$\eta_{DE,avg}$ (%, computed)	$\eta_{TOT,avg}$ (%, computed)	$\eta_{DE,avg}$ (%, simulated*)	$\eta_{TOT,avg}$ (%, simulated*)
Pure-mode outphasing (60%-overdrive)	Class-E	86.4	61.8	85.7	61.2
Pure-mode outphasing (onset-overdrive)		80.7	68.0	79.5	66.6
Mixed-mode outphasing	Class-B	66.9	66.8	65.9	65.8
Asymmetric (1:2) Doherty		59.0	58.9	58.8	58.7
Symmetric Doherty		50.9	50.8	50.9	50.8
Pure-mode (linear) outphasing		45.1	45.0	42.7	42.7
Pure-mode (saturated) outphasing		30.9	29.8	33.9	35.3
Stand-alone		27.0	27.0	26.4	26.4

*Assuming 20-dB power gain devices and a 10.5 dB PAR W-CDMA test signal.

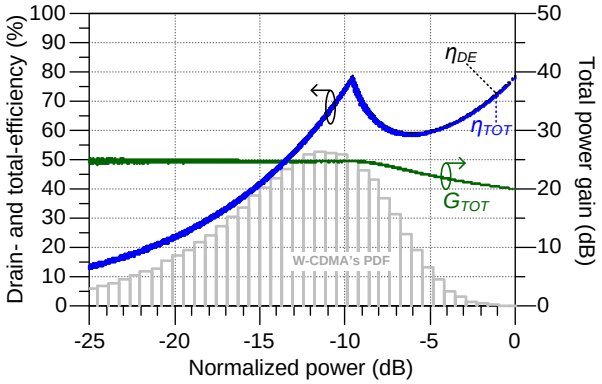
3.7. VERIFICATION WITH ENVELOPE SIMULATIONS

In order to verify the calculated results of the previous section, envelope simulations of the amplifiers in this chapter can be accomplished by replacing the harmonic-balance frequency-domain sources by time-domain sources (that perform ideal up-conversions of baseband data). In this chapter, this was performed using Agilent ADS and a dataset source containing the proper voltage waveforms required for each branch amplifier. These waveforms were obtained after processing in ADS Ptolemy and MATLAB the modulated baseband signal according to the exact analytical driving functions described for each branch amplifier in Section 3.4 and Section 3.5. The modulated signal used in this chapter consist of an entire radio frame (10 milliseconds with an oversampling factor of 4) of a 10.5 dB PAPR W-CDMA signal that is used as a test signal for 3GPP amplifiers [14].

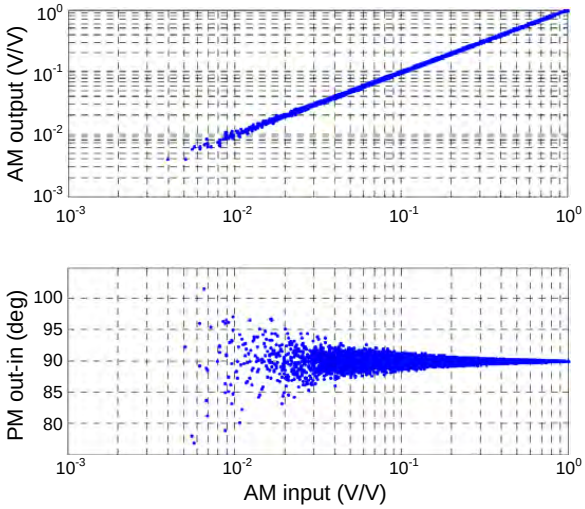
Figures 3.23 to 3.25 illustrate representative results for the envelope simulations of the class-B Doherty and outphasing amplifiers. The results for class-E outphasing amplifiers are detailed in the next section. Figures 3.23a and 3.24a provide instantaneous efficiencies and total gains versus back-off power while figures 3.24b and 3.24b give AM-AM and AM-PM responses for the asymmetric DPA and the mixed-mode outphasing amplifier, respectively. The corresponding spectra of these amplifiers is plotted in Fig. 3.25. As expected, note that the envelope simulation results for the efficiency follow the harmonic-balance simulations shown earlier. This is an indication that the signal processing of the branch signals was done properly. Even though these envelope simulations require significantly more computational resources, they are useful also to analyze some linearity and bandwidth aspects of the different amplifiers.

DYNAMIC PERFORMANCE VERIFICATION OF THE CLASS-E OUTPHASING PA

Compared to the previous amplifier concepts, the correct dynamic operation of the class-E outphasing amplifier with modulated signals requires an extra step even in the ideal case. In Section 3.5.2 it was mentioned that this amplifier requires an explicit balancing of the amplitudes of the two branch amplifiers in order to allow for sufficient dynamic range and this was illustrated previously in Fig. 3.19. In that same figure, it can be observed that there is a phase offset (of about $-17°$ in the figure) and that even after accounting for it, the so-called "high-efficiency" region is not exactly in the ideal outphasing angle range $0 \leq \theta \leq \frac{\pi}{2}$. In fact, the ideal function $\overline{E} = \sin\left(\theta - \theta_{offset}\right)$ expected for this amplifier ((2.6) and (2.7) in Section 2.2) does not accurately represents the actual amplitude behavior versus phase as obtained with the schematic of Fig. 3.18. This is depicted in Fig. 3.26 which shows the "ideal" function $\overline{E} = \sin\left(\theta - \theta_{offset}\right)$ as well as the "real" function representing the actual envelope behavior of the amplifier versus outphasing angle (from Fig. 3.19). This is an important consideration that needs to be handled by the signal modulator (i.e. signal component separator) in order to preserve the linearity of the entire outphasing amplifier.

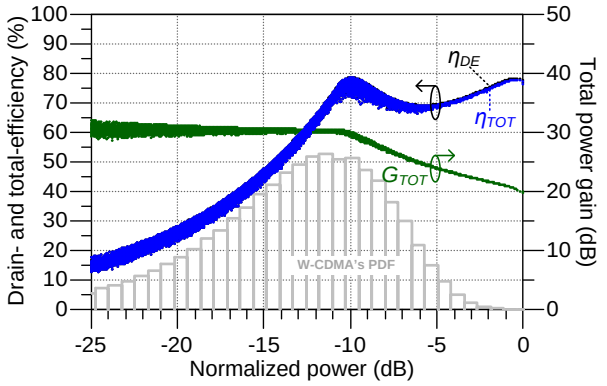


(a) Instantaneous efficiencies and total gain.

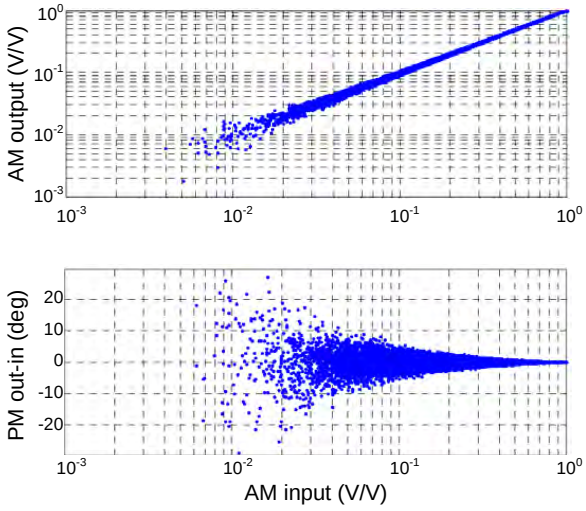


(b) AM-AM and AM-PM curves.

Figure 3.23: Envelope simulation results of the class-B asymmetric Doherty amplifier: a) instantaneous efficiencies and total gain versus normalized power (output W-CDMA's PDF plotted for reference), and b) AM-AM and AM-PM curves.



(a) Instantaneous efficiencies and total gain.



(b) AM-AM and AM-PM curves.

Figure 3.24: Envelope simulation results of the class-B outphasing amplifier in "mixed-mode": a) instantaneous efficiencies and total gain versus normalized power (output W-CDMA's PDF plotted for reference), and b) AM-AM and AM-PM curves.

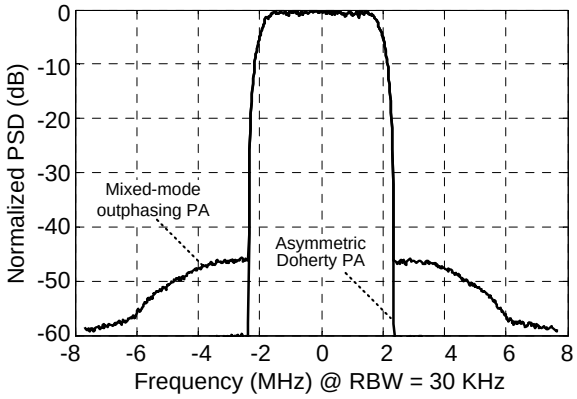


Figure 3.25: Output spectrum of the assymetric Doherty and mixed-mode outphasing PAs.

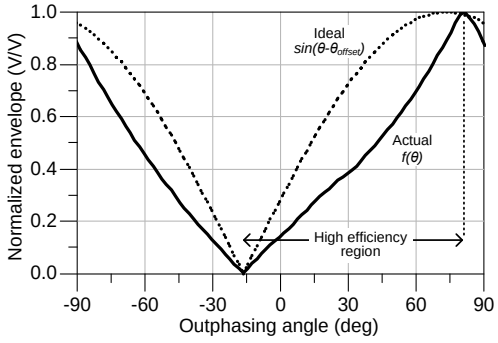


Figure 3.26: Ideal (sinusoidal function) and practical (actual amplifier behavior) envelope amplitude control versus outphasing angle.

The task of the signal component separator is to decompose the input complex modulated signal according to the actual response of the amplifier. In practice, this can be easily done at baseband by mapping such a response with a complex-valued look-up table (LUT) that contains the information of the output amplitude and phase versus outphasing angle. This is, the SCS needs to process the original envelope $E(t)$ and phase $\varphi(t)$ in order to generate the phase-modulated baseband branch signals $S_{1,2}(t)$ according to

$$S_{1,2}(t) = e^{j(\varphi(t)\pm\theta'(t)-AMPM(t))} \tag{3.37}$$

where

$$\theta'(t) = \mathrm{LUT}_{\theta}\left(\overline{E(t)}\right) \tag{3.38}$$

$$AMPM(t) = \mathrm{LUT}_{phase}\left(\overline{E(t)}\right) \tag{3.39}$$

If this process is done properly, then the output will be linear. As an example, Fig. 3.27 shows the results of the envelope simulations for the class-E outphasing amplifier with 60%-overdrive after the above correction has been applied. Note that these results are the same as for the harmonic-balance simulations shown previously in Fig. 3.20. In turn, Fig. 3.28 compares the AM-AM, AM-PM and spectrum of this amplifier before and after such correction. Observe that the lack of proper mapping between output power and phase control leads to spectral regrowth which can be corrected by the SCS after a straightforward characterization of the instantaneous response of the actual amplifier (equivalent to a memoryless digital predistortion). A practical demonstration to show the effectiveness of this simple memoryless linearization will be given later in Chapter 7 using a practical implemented outphasing prototype.

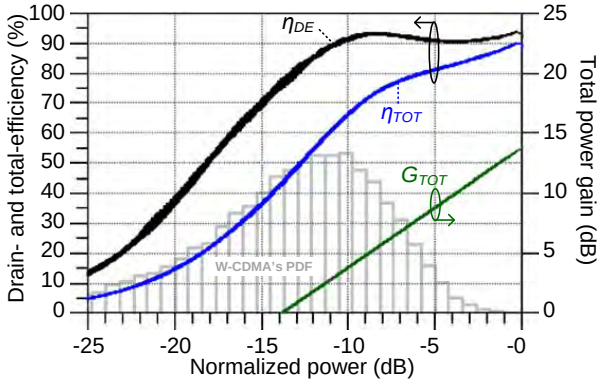
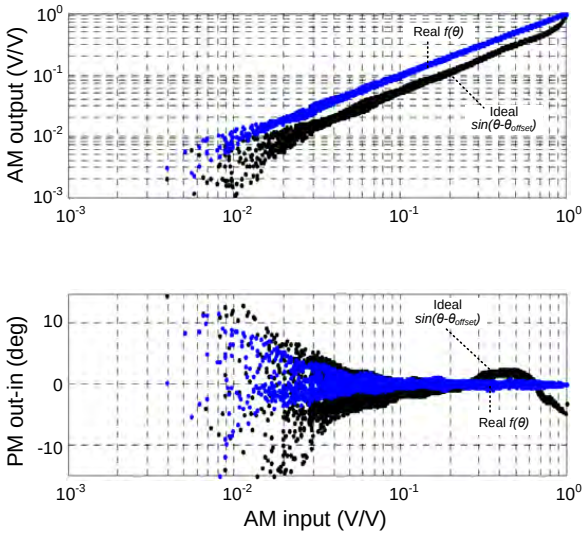
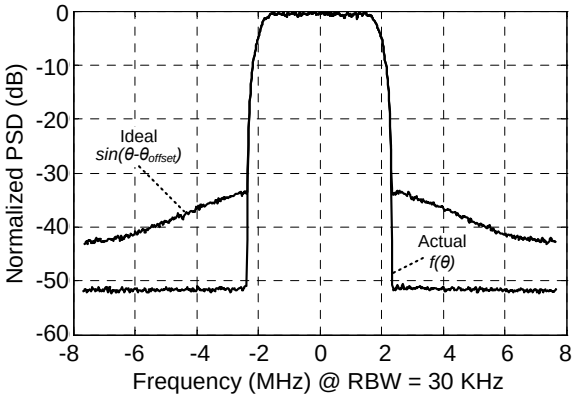


Figure 3.27: Envelope simulation results of the class-E outphasing amplifier: instantaneous efficiencies and total gain versus normalized power (output W-CDMA's PDF plotted for reference).



(a) AM-AM and AM-PM curves.



(b) Output spectra.

Figure 3.28: Effect of improper signal decomposition by the SCS in the class-E outphasing amplifier: a) AM-AM and AM-PM responses and b) output spectrum using input drive signal conditioning based on the "ideal" phase relations as well as the "actual" phase relations after the proper look-up table correction.

3.8. CONCLUSIONS

This chapter provided a system-level study of the most appealing power amplifier concepts that utilize load-modulation for the linear and energy-efficient amplification of complex modulated communication signals with large PAPR. The studied amplifier concepts include Doherty and outphasing and employ class-B and class-E operation for

their branch amplifiers. To enable a detailed and unified discussion, as first step an idealized large-signal transistor model was introduced and described. This simple model allows accounting for several performance limitations found in practical devices, such as finite power gains, finite breakdown voltages and current handling constrains. Using this model, the design of the branch amplifiers was detailed, with emphasis on the class-E amplifier. Next, symmetric and asymmetric Doherty amplifiers utilizing class-B operation were described in order to use their efficiency performance potential as benchmark. Then, a detailed description is given for the design and efficiency performance of various outphasing amplifier configurations with class-B and class-E branch amplifiers in combination with specific input drive conditions. The average efficiency performance of all these amplifiers was compared assuming a Rayleigh-envelope distribution for the amplified signal and these results were verified by envelope simulations using a realistic 10.5 dB PAPRW-CDMA test signal.

Following this approach, it was demonstrated that the efficiency potential of outphasing amplifiers is typically higher than of two-way Doherty amplifiers when dealing with signals with a high PAPR (e.g. 10-12 dB). In addition, it was also shown that the required input power and drive profile for a particular amplifier concept has a high impact on the achievable total-average efficiency. In view of this, use of mixed-mode control, or other means to reduce the input drive proved to be very important. This is most visible by considering the rather spectacular drain-efficiency of a class-E (pure-mode) outphasing amplifier which, when including the required input power, yields in the end a similar average overall efficiency as a mixed-mode class-B outphasing amplifier with optimum input drive-profile.

Besides their efficiencies, class-B and class-E outphasing amplifiers have also other important differences. Contrary to the class-E case, the ideal driving for the class-B outphasing amplifier when using voltage-source-like combiners is not a pure phase-modulated signal as traditionally considered. In fact, although purely phase-modulated signals can certainly be employed (as shown in Subsection 3.5.1) and the efficiency performance is better than a stand-alone class-B amplifier, such performance is far from optimum as summarized in Table 3.2. The optimum drive for class-B outphasing PAs requires a specific amplitude control that depends on the applied combining network (i.e. it shall include its specific compensation) as indicated by (3.28). This makes the optimum driving profile for class-B outphasing amplifiers sensitive to the actual hardware configuration and therefore more complicated.

In conclusion, although the overall total efficiencies are in the same order for mixed-mode class-B and pure-mode class-E outphasing, the latter allows a significantly simpler drive profile and as such is offers the potential to drive it from “standard” digital circuitry. For these reasons we will focus in this thesis work on outphasing concepts that utilize class-E branch amplifiers. Next chapter will review the bandwidth expansion considerations for the driving signals of the different amplifier concepts with a special attention to class-E outphasing.

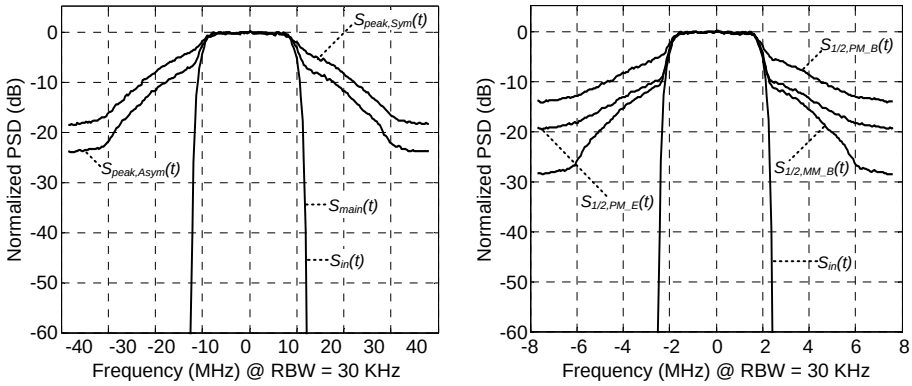
4

STUDY OF LOAD-MODULATED AMPLIFIERS II: BANDWIDTH EXPANSION

4.1. INTRODUCTION

An important consideration in the study of load-modulated amplifiers is that of the bandwidth expansion of the controlling signals of the constitutive branch amplifiers. These signals require non-linear transformations applied to the original and band-limited baseband signal $S_{in}(t) = E(t) \cdot e^{j\varphi(t)}$, resulting in a much larger phase and amplitude modulation signal bandwidths as the complex signal trajectory approaches or crosses the origin of the IQ plane [68]. Two well-known functions that cause bandwidth expansion are the Cartesian-to-polar coordinates transformation required in envelope tracking amplifiers [68] and the amplitude-to-phase conversion in outphasing amplifiers [41] (possibly requiring also a prior Cartesian-to-polar coordinates transformation). However, branch signal bandwidth expansion is not exclusive to these two amplifier concepts but it is rather general to multi-input amplifiers, including also the peaking branch of the ideal Doherty amplifiers.

In this chapter, a brief discussion is provided in regards to the bandwidth expansion of the driving signals of the load-modulated amplifiers treated in the previous chapter, with a special focus on the pure-mode outphasing amplifier. This chapter starts with reviewing the bandwidth expansion of the driving signals for the previously discussed load-modulated amplifiers using the envelope simulations with the W-CDMA signal described in the previous chapter. In addition, a comparison of their spectra is performed using other three complex modulated signals with different near-origin signal trajectories. After this, the specific case of the pure-mode outphasing amplifier is further analyzed. Here, a simulation experiment is performed in which the branch signals' band-



(a) Peaking branch of Doherty amplifiers.

(b) Both branches of outphasing amplifiers.

Figure 4.1: Bandwidth expansion in a) the peaking branch signal in the ideal Doherty amplifier (symmetric and asymmetric cases), and b) both branch signals of several outphasing amplifiers: class-B in pure-mode ("PM-B"), class-B in mixed-mode ("MM-B") and class-E in pure-mode ("PM-E").

width is limited and the oversampling ratio of the original baseband signal is varied in order to study these two parameters on the overall output signal performance in terms of ACLR and EVM. In particular, the reconstructed signal of the outphasing amplifier is checked with the presence of limiters in the amplifying branches in order to resemble ideal switch-mode branch amplifiers. Finally, conclusions on the bandwidth expansion of the branch signals are given.

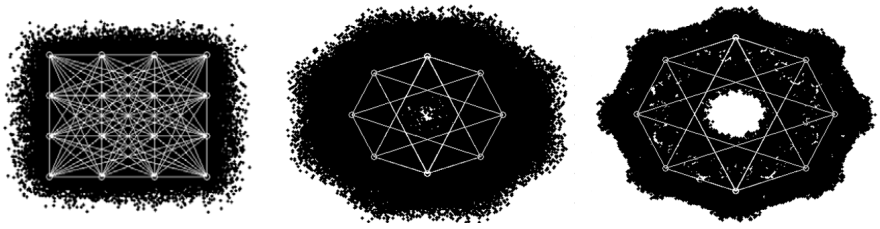
4.2. BANDWIDTH EXPANSION IN LOAD-MODULATED AMPLIFIERS

As described earlier, non-linear transformations of band-limited signals lead to bandwidth expansion. For example, the instantaneous frequency of the original signal's phase component $\varphi(t)$ can be expressed in terms of the original in-phase and quadrature components $I_{in}(t)$ and $Q_{in}(t)$, respectively, according to[1]

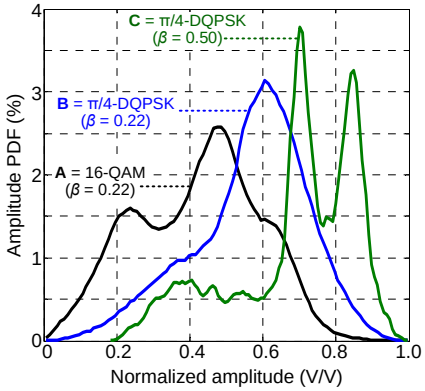
$$\frac{d}{dt}\varphi(t) = \frac{d}{dt}\left(\text{atan2}\left[\frac{Q_{in}(t)}{I_{in}(t)}\right]\right) = \frac{I_{in}(t)\cdot\frac{d}{dt}Q_{in}(t) + Q_{in}(t)\cdot\frac{d}{dt}I_{in}(t)}{I_{in}(t)^2 + Q_{in}(t)^2} \tag{4.1}$$

where it can be noticed that near-origin signal trajectories will lead to large frequency deviations. In fact, if the signal trajectory goes through the origin ($I_{in}(t) \to 0$ and $Q_{in}(t) \to 0$) large instantaneous phase deviations will occur $\Delta\varphi \to 2\pi$, causing frequency deviations Δf that go asymptotically to infinite (i.e. to half the sampling frequency in discrete signals, or $\Delta f \to \pm f_s/2$) [68]. Such bandwidth expansion can be observed in all

[1] Altough $\text{atan}(Q/I) = \text{atan2}(Q/I)$, the four-quadrant inverse tangent function "atan2()" is preferred over the two-quadrant function "atan()" in (4.1) because $\varphi(t)$ lies in the interval $(\pi, -\pi]$.



(a) 16-QAM ($\beta = 0.22$) (b) $\pi/4$-DQPSK ($\beta = 0.22$) (c) $\pi/4$-DQPSK ($\beta = 0.50$)



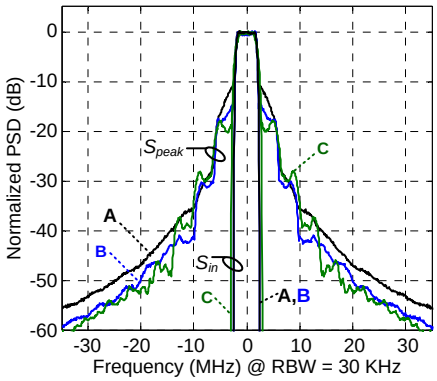
(d) Amplitude's PDF.

Figure 4.2: Complex modulated signals with different near-origin trajectories: 16-QAM and $\pi/4$-DQPSK: a to c) constellations (before and after oversampling and filtering), and d) amplitude's PDF.

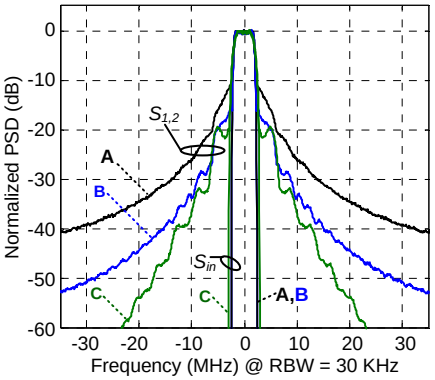
the load-modulated amplifier concepts studied in the previous chapter by simply plotting the spectra of their driving signals. Fig. 4.1 illustrate this by using the results of the envelope simulations described earlier in Section 3.7 that employed a W-CDMA test signal which has zero-crossings. Fig. 4.1a shows the signal bandwidth expansion as found for the peaking branch in the symmetric and asymmetric Doherty PAs, while Fig. 4.1b shows the signal bandwidth expansion as found for the branches signals in the various outphasing amplifier implementations. Note that although not equally, the branch signal's bandwidth expands for all the amplifiers (the limited bandwidth span is due to the limited oversampling of 4 used in the simulations).

4.3. EFFECT OF NEAR-ORIGIN SIGNAL TRAJECTORIES

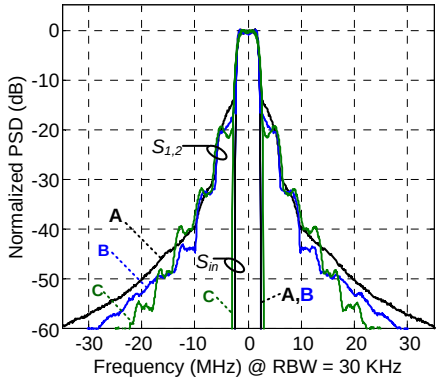
The work in [68] studied the effect of near-origin trajectories of the complex modulated signals on the bandwidth expansion in envelope-tracking amplifiers using W-CDMA signals that have zero-crossings. It realized, however, that 96% of the time the complex



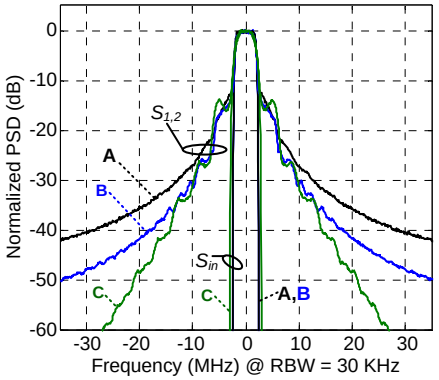
(a) Asymmetric Doherty amplifier.



(b) Class-B outphasing in pure-mode.



(c) Class-B outphasing in mixed-mode.



(d) Class-E outphasing (pure-mode).

Figure 4.3: Branch signal's bandwidth expansion for the different amplifiers and the different modulated signals depicted in Fig. 4.2: a) peaking branch in Doherty PAs, b) to d) both branches in outphasing amplifiers.

W-CDMA trajectory is sufficiently distant from the origin and the resulting frequency modulation is contained in a very narrow band. Therefore it proposed to avoid the zero-crossings by processing the original modulated signal using a dedicated algorithm in order to decrease the bandwidth expansion of the polar modulator. In this section, a similar study is performed in order to analyze the effect of near-origin signal trajectories in the bandwidth expansion of Doherty and outphasing amplifiers, by using simply several modulated signals with different near-origin signal trajectories.

For this purpose, three complex modulated signals were selected. The first one is a 16-QAM with a square-root-raised-cosine filter (SRRC), very similar to the one used in W-CDMA but without the dedicated spreading and scrambling. The second and third signals are $\pi/4$-DQPSK signals with SRRC filtering using different roll-off factors β: 0.22 (same as for the first signal) and 0.50 (slightly wider bandwidth), respectively. Contrary to the case of the 16-QAM signal, the original constellation of the $\pi/4$-DQPSK signals does

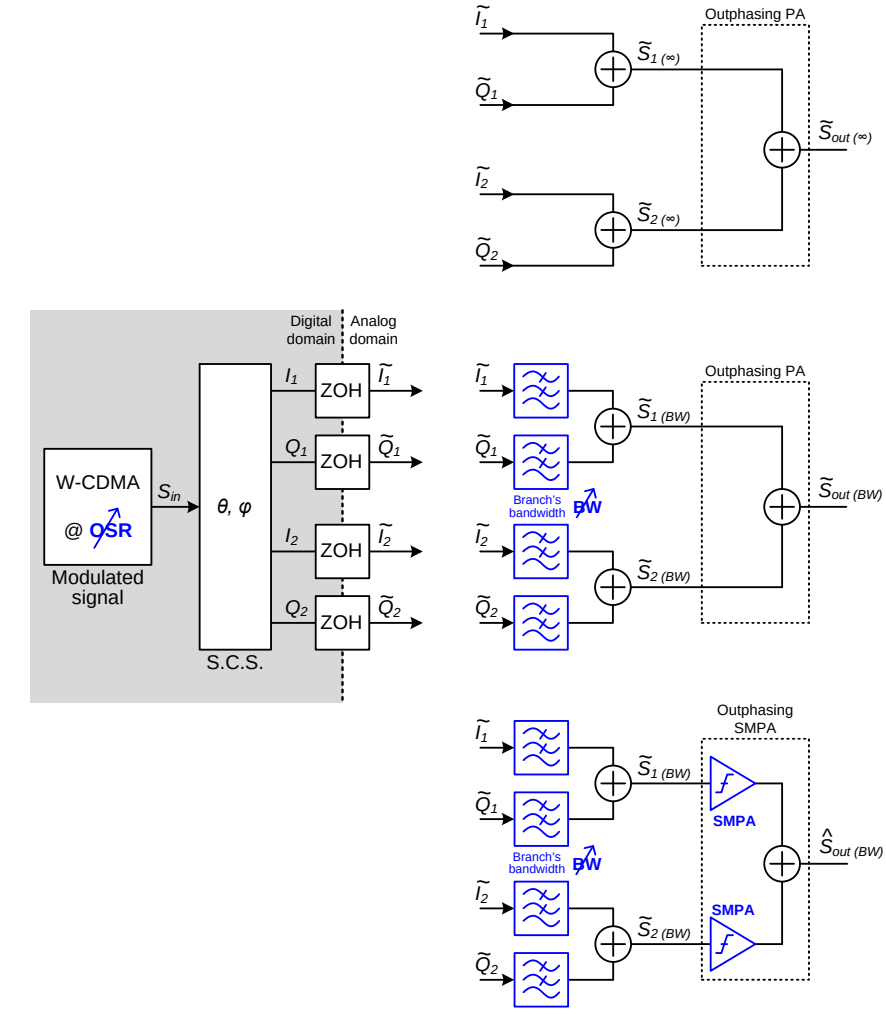
not have zero-crossings as required for this experiment. Even though the filter's roll-off factor affects the occupied bandwidth of the signals, it has a greater effect on the near-origin trajectories for the $\pi/4$-DQPSK signal after filtering. The IQ time-domain representations along with the original constellations of these signals are depicted in Figs. 4.2a to 4.2c. Here, the important characteristic of these signals is that their near-origin trajectories is clearly different (see the center part of Figs. 4.2a to 4.2c), as illustrated by their amplitude's PDF provided in Fig. 4.2d (see the bottom-left corner).

With these three modulated signals and the analytical expressions given earlier in Sections 3.4 and 3.5, the driving signals for the branch amplifiers of the Doherty and outphasing amplifiers were generated. Their resulting spectra are given in Fig. 4.3. Although not plotted, the results of the symmetric DPA peaking branch are very similar to the ones of the asymmetric DPA in Fig. 4.3a. Note that although in all cases there is bandwidth expansion, the asymmetric DPA and the mixed-mode outphasing amplifiers suffer less from the zero-crossings in the modulated signals (using as an arbitrary reference the -40 or -50 dBc power level). In addition, note that the signals with trajectories farther from the origin lead to significantly lower bandwidth expansion in the pure-mode outphasing amplifier cases (class-B and class-E). This is presumably due to the absence of very small amplitude levels that would otherwise result in relatively large phase changes, and hence bandwidth expansion.

4.4. BANDWIDTH EXPANSION IN THE IDEAL OUTPHASING AMPLIFIER

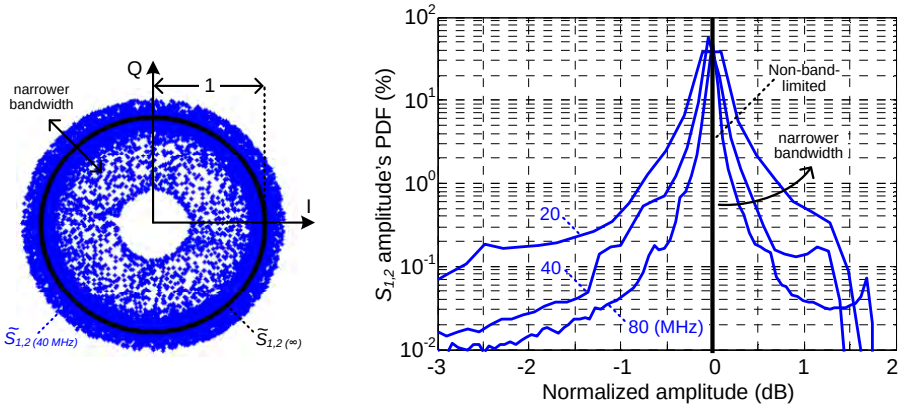
The previous section showed that the pure-mode outphasing amplifiers have the largest bandwidth expansion in its branch signals, e.g. as observed in Fig. 4.3d. However, such expansion is normally quantified arbitrary to about 10-16X the original signal's bandwidth [41, 51, 91], depending on the specific assumptions considered. For example, a common arbitrary definition for the expanded bandwidth is the one contained when the normalized signal power exceeds -40 dBc (i.e., the bandwidth where the signal power is at least 0.01% of the peak power). Then, based on this definition, the bandwidth of the $S_{1,2}(t)$ signals occupies up to about 60 MHz for a W-CDMA signal with a 3.84 MHz chip rate frequency [51] (this corresponds to a 16X expansion factor as depicted in Fig. 4.3d for the trace labeled "A"). Using the same -40 dBc bandwidth limit, the work in [91, Eq. (28)] estimated analytically the bandwidth expansion factor for a 16-QAM signal to about 13 [sic] [recte 10]. However, as shown in the previous section, different modulated signals with roughly the same bandwidth (such as "B" and "C" in Fig. 4.3d) can lead to different occupied bandwidths for $S_{1,2}(t)$ depending on their near-origin signal trajectories for the same amplifier and same arbitrary power limit. What is certain, is that the branch signals $S_{1,2}(t)$ will simply occupy all the available bandwidth, which is limited in baseband domain by the sampling frequency as discussed previously. However, if considered properly, this bandwidth expansion is not as large as traditionally considered as explained next.

As described earlier in Subsection 2.7.3 by the alternative branch signal representa-



(a) (b)

Figure 4.4: Simulation setup for analyzing the effect of band-limiting and over-sampling ratios on the quality of the recombined output outphasing signal: a) baseband signal representation, b) the three analyzed cases (infinite and finite bandwidths, and the latter including a limiter).

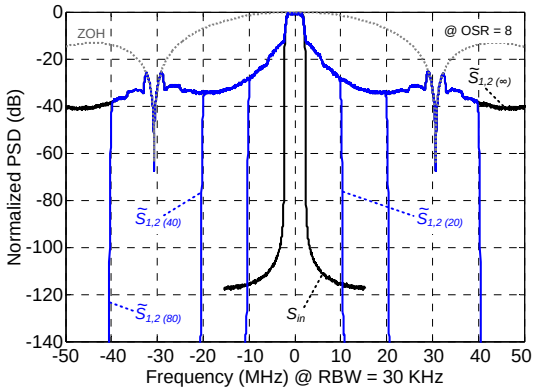


(a) Normalized IQ representation. (b) Amplitude's PDF for different branch bandwidths.

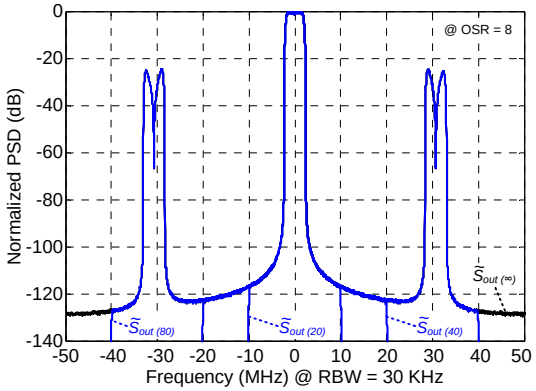
Figure 4.5: Outphasing branch signals before and after band-limiting: a) normalized IQ representation and b) amplitude's PDF for different branch bandwidths.

tion given by (2.55) to (2.57), the in-phase component $s(t)$ of the phase-modulated signals $S_{1,2}(t)$ simply contains a scaled replica of the original signal $S_{in}(t)$ while the quadrature component $\varepsilon(t)$ is required to maintain their constant amplitude (depicted earlier in Fig. 2.21a). Thus, the expanded bandwidth of $S_{1,2}(t)$ is due to the contribution of $\varepsilon(t)$ while the original information is still contained in $s(t)$. As such, the phase-only nature of $S_{1,2}(t)$ is due to $\varepsilon(t)$ at the expense of bandwidth expansion. A scaled replica of $S_{in}(t)$ can be perfectly recovered after the out of phase combination of $S_{1,2}(t)$. However, if $S_{1,2}(t)$ are band-limited, then their amplitude will exhibit some variation (losing their pure phase-modulated nature) but $S_{in}(t)$ will still be recoverable at the output although with some distortion (i.e. degraded ACLR and EVM) depending on the specific recombination process. This can be demonstrated by the simulation experiment in this section.

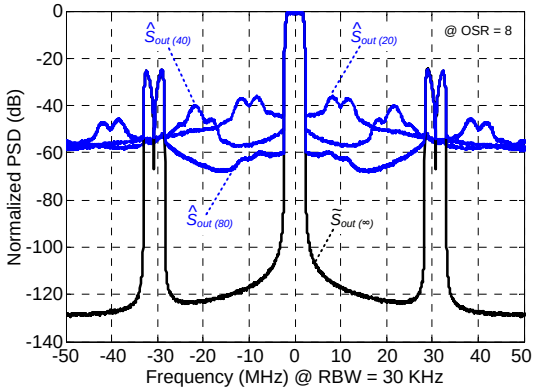
Fig. 4.4 shows a simulation setup developed in MATLAB for analyzing the impact of both band-limiting the branch signals and employing different over-sampling ratios (OSR) of the original signal on the linearity of the output outphasing signal, as measured in terms of spectral re-growth or ACLR and EVM. Fig. 4.4a depicts a baseband signal generator (in this case of a 16-QAM signal) with a selectable OSR, followed by the ideal outphasing signal component generator. Zero-order-hold (ZOH) operators are used to model ideal digital-to-analog converters and hence represent "analog" signals with discrete time and discrete amplitude signals in the simulations (quantization noise is kept very small by utilizing 64-bit double precision floating-point numbers in the simulator). Fig. 4.4b illustrate the three cases considered here: the ideal case of infinite bandwidth (top), the case of limited bandwidth for the branch signals (middle) and the case of using a limiter (representing an ideal branch SMPA) for the second case (bottom). For the latter two cases, the analog bandwidth of the amplifying branches can be varied using a low-pass filter, implemented here as a high-order and linear-phase FIR with Blackman-Harris window, located prior to the branch amplifier.



(a) Input and branch signals.



(b) Output signals with linear amplification (middle case in Fig. 2.21).

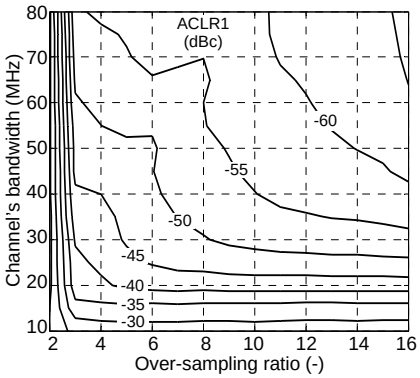


(c) Output signals with saturated amplification by SMPAs (bottom case in Fig. 2.21).

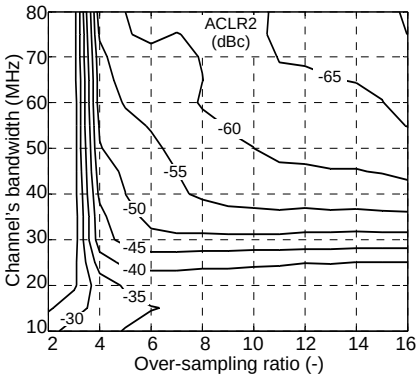
Figure 4.6: Examples of simulated spectra of the branch and output signals in the setup depicted in Fig. 2.21 for different branch bandwidths: a) input and branch signals, b) output signals with linear amplification (middle case in Fig. 2.21) and c) output signals with saturated amplification by SMPAs (bottom case in Fig. 2.21).

Several combinations of OSR and branch bandwidths were simulated since different combinations will cause different degrees of distortion in the output signal. From all the simulated cases, examples of the analog-represented branch signals $\tilde{S}_{1,2}(t)$ are depicted in Fig. 4.5 for different branch bandwidths. As described, $\tilde{S}_{1,2}(t)$ are perfect phase-modulated signals if infinite bandwidth is considered. Otherwise, they will exhibit larger amplitude variations with smaller branch bandwidths. Fig. 4.5a illustrates the normalized IQ representation of a non-band-limited and a band-limited branch signal, the latter corresponds to the "fuzzy" circle. Alternatively, this can be illustrated by the amplitude's PDF of these signals as given in Fig. 4.5b. Note on this figure that the amplitude of the band-limited signals spread around the original's amplitude level (given in dB with respect to the non-band-limited case). The simulated spectra of the three band-limited signals of Fig. 4.5b are provided in Fig. 4.6a along with the original baseband signal (and an indication of the sinc response of the ZOH operator). In turn, the corresponding spectra of the output signals are given in Fig. 4.6b for the second (middle) case of Fig. 4.4b. For the case of utilizing branch SMPAs (bottom case in Fig. 4.4b), the corresponding spectra of the output signals are given in Fig. 4.6c. Note in Fig. 4.6b that regardless of the bandwidth, the output is still a clean and linear replica of the input as long as the signals are combined linearly without further distortion. So, even though band-limiting will cause envelope variations in the branch signals, the output will not be affected if these signals are combined perfectly in the outphasing amplifier. However, note in Fig. 4.6c that if a non-linear operator is applied to these branch signals, such as the limiter that represents the SMPAs, the output will be distorted in certain degree creating spectral re-growth and reducing EVM. In this last case, the branch signals located between the limiter and the combiner will exhibit again large bandwidths and, as long as they remain within the outphasing amplifier and are amplified equally, this is not a big concern.

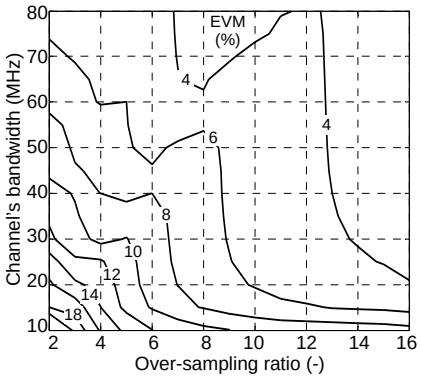
The simulation results for out-of-band (ACLR1 and ACLR2) and in-band distortion (EVM) caused by the different branch bandwidths and original signal's OSR are depicted in Fig. 4.7. Although not considered here, other parameters affect these results [41, Ch. 2], such as quantization errors, branch imbalances and filter types, among others. Although there is no distortion for infinite channel bandwidths, as depicted earlier in Fig. 4.6b, there is some distortion depending on the branch bandwidth and the over-sampling ratios. The important conclusion of the results provided in Fig. 4.7 is that reasonable low levels of over-sampling and channel bandwidth suffice to comply with the distortion requirements of the outphasing amplifier (such as -45/-50 dBc $ACLR1/2$ and 12.5% EVM requirements in 3GPP systems [15]), regardless of the otherwise arbitrary definition of bandwidth expansion of 10X or more.



(a) ACLR1 (dBc).



(b) ACLR2 (dBc).



(c) EVM (%).

Figure 4.7: Simulation results for the distortion of the output signal after saturated amplification (bottom case in Fig. 4.4b) for different over-sampling ratios and branch bandwidths: a) ACLR1 and b) ACLR2 levels, and c) corresponding (sample-wise) EVM.

4.5. CONCLUSIONS

This chapter discussed some bandwidth expansion considerations of the branch signals of the ideal load-modulated amplifiers treated in the system-level study started in the previous chapter. A special focus was also given for the outphasing amplifier. It was shown that bandwidth expansion occurs in all the amplifiers, including both Doherty and outphasing amplifiers. For the first case, this bandwidth expansion happens in the "peaking" branch while in the outphasing case it occurs in both branches. Also, it was shown that modulated signals with different trajectories near the origin lead to different degrees of bandwidth expansion. This is due to the non-linear transformations needed

to create the branch amplifier signals and is regardless of the original signal's occupied bandwidth. This effect is more profound in pure-mode outphasing amplifiers than in the amplifiers that use amplitude modulation in their drive signals, such as the DPAs and the mixed-mode outphasing amplifier.

For the particular case of the pure-mode outphasing amplifier, the effect of branch bandwidths and the original signal's over-sampling ratios on the distortion of the overall output was analyzed. This analysis considered the use of switch-mode PAs represented by ideal limiters. The simulation results indicated that band-limiting the branch signals does not distort per se the output outphasing signal but rather introduces some amplitude variation. If SMPAs are used in the PA branches, then the phase-modulation of these signals are restored while their bandwidth is expanded again (which can be harmless if inside the outphasing amplifier and provided that both paths are identical). The net effect of bandwidth limitations is some distortion in the overall output after outphasing combining. However, reasonably low branch bandwidths and over-sampling ratios can suffice to comply with in-band and out-of-band linearity specifications. This is a more objective way to quantify bandwidth expansion in outphasing amplifiers than done traditionally when using an arbitrary power level definition.

5

BONDWIRE MAGNETICS FOR COMPACT HIGH-POWER AMPLIFIERS

5.1. INTRODUCTION

Wire bonding is a mature and cost-effective technique to create electrical interconnects between integrated circuits and their packages. This low-cost and versatile bondwire-based technology can also be used to realize compact magnetic structures such as inductors, transformers or even other complex structures different than interconnects [92]. Bondwire interconnections are formed by thin metal wires (gold and aluminum are common materials), which are mechanically and electrically connected to bonding pads on chips and in packages using a wire-bonding tool which is automated for mass production or for accurate prototyping. The two main wire-bonding process technologies are ultrasonic wedge-wedge (normally used for aluminum wires connecting to aluminum or gold pads) and thermosonic ball-stitch (normally used for gold wires to different pad materials) bonding. A brief description of these processes can be found in [92]. The photograph in Fig. 5.1 exemplifies the case of ultrasonic wedge-wedge bonding process using aluminum wires in an automatic wire-bonding machine (only the bond wedge and wire clamp of the machine is visible in the photograph).

In many semiconductor devices, bondwires are typically considered as parasitic elements (normally inductive) which degrade RF circuit performance. However, in high-power RF transistors, bondwire arrays are normally used as low-loss inductive elements to form partial impedance-matching networks inside the transistor packages. As it will

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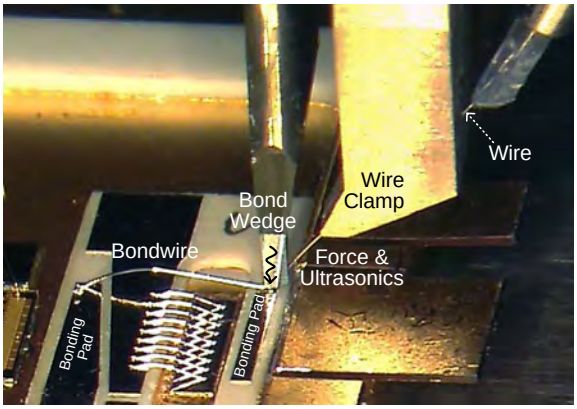


Figure 5.1: Photograph exemplifying the ultrasonic wedge-wedge wire-bonding process during the manufacturing of one of the amplifier prototypes in this thesis.

be described soon, several geometric properties of the wires (including their cross section, their number in parallel arrangements and the loops they create) determine their equivalent inductive behavior. Most of these parameters can be adjusted by automatic wire-bonding machines. However, there are currently very limited simulation tools that can accurately predict the actual wire loop after a bonding process and therefore ad hoc experiments are still needed in order to optimize some process recipes for the loop shapes [92].

This chapter describes the design and modeling of bondwire-based magnetic components such as inductors and novel transformer structures, which are key elements in the implementation of the packaged-integrated RF high-power amplifiers in subsequent chapters. This chapter starts by reviewing basic concepts of (self- and mutual-) inductance with a focus on the case of bondwires. Then, the design of simple inductors based on arrays of bondwires is described. Next, a novel bondwire-based transformer is presented which is also based on parallel bondwire connections. This transformer differs from the conventional series (multi-turn) connection of inductive bondwire loops that has been described in previous works [93–98]. The subsequent section describes a prototype implementation of the proposed transformer along with its main RF measurements. In addition, further practical demonstration of the usefulness of the techniques described in this chapter can be appreciated with the practical compact highly-efficiency and high-power amplifier designs described in the next two chapters.

5.2. BASICS OF INDUCTANCE

Inductance is a relevant property to any conductor or physical circuit in which a time-variant current flows. Changing currents in a conductor creates varying magnetic fields that "induce" proportional voltages in both the conductor itself (self-inductance) and,

via magnetic flux linkage, in nearby conductors (mutual-inductance). Although a comprehensible treatment of electromagnetic theory applied to the inductance can be found elsewhere [99, 100], here some basic concepts are reviewed to better support the understanding of the bondwire cases discussed later.

5.2.1. INDUCTANCE FUNDAMENTAL CALCULATIONS

For ideal circuit elements, the self-inductance and mutual-inductance not associated with ferromagnetic materials are only dependent on the physical geometry of the circuit loop [101]. Under quasi-static conditions (i.e. small physical loop dimensions compared with the wavelength of the electromagnetic fields), the inductance can be defined analytically as a proportionality factor that relates the magnetic flux Ψ_{ij} in a i-th loop owing to the varying current I_j in a j-th loop, this is [100]

$$L_{ij} \equiv \frac{\Psi_{ij}}{I_j} = \frac{\int_{S_i} \overrightarrow{B_j} \cdot \mathrm{d}\overrightarrow{S_i}}{I_j} \text{ for } I_k = 0 \text{ with } k = 1, 2... \text{ and } k \neq j \tag{5.1}$$

where $\overrightarrow{B_j}$ is the magnetic flux density vector and $\mathrm{d}\overrightarrow{S_i}$ is the elemental area on the surface S_i (oriented normally to S_i according to the right-hand rule). In (5.1), L_{ij} are the self-inductances for $i = j$ while $M_{ij} = L_{ij}$ are the mutual-inductances for $i \neq j$. In terms of the loop geometry, and assuming a uniform distribution of the current I_j over a constant cross section area a_j along the j-th loop, (5.1) can also be expressed as [100]

$$L_{ij} = \frac{1}{a_i \cdot a_j} \int_{a_i} \int_{a_j} L_{\mathrm{f}ij} \mathrm{d}a_i \mathrm{d}a_j \tag{5.2}$$

$$L_{\mathrm{f}ij} = \frac{\mu}{4\pi} \oint_{C_i} \oint_{C_j} \frac{\mathrm{d}\vec{l}_i \mathrm{d}\vec{l}_j}{r_{ij}} \tag{5.3}$$

where μ is the permeability of the medium, $\mathrm{d}\overrightarrow{l_{i,j}}$ are the elemental vectors tangent to the contour paths $C_{i,j}$ directed in accordance with the currents $I_{i,j}$, $\mathrm{d}a_{i,j}$ are the differential elements of the cross section areas $a_{i,j}$, and $r_{ij} = \left|\overrightarrow{r_i} - \overrightarrow{r_j}\right|$ is the distance between every pair of points on the i, j-th loops, respectively. Fig. 5.2 provides an illustration of these quantities.

Equation (5.3) is known as Neumann's inductance formula for closed loops and represents the inductance when the loops are considered filamentary (i.e. of negligible cross section). Neumann's equation describes compactly the geometric nature of mutual-inductance as the average value of $\frac{1}{r_{ij}}$ between every pair of points on the loops weighted by $\cos(\vartheta)$, where ϑ is the local angle between the points in the loop [99]. A well-known consequence of this is that points lying on segments mutually perpendicular do not contribute to the mutual-inductance. In addition, this idea of averages is also present in (5.2) which illustrates that averages are taken over the conductor cross sections [100].

It shall be noted that in the calculation of the self-inductance by (5.1), the magnetic flux Ψ_{ii} accounts for two portions of the magnetic field, one external and another one

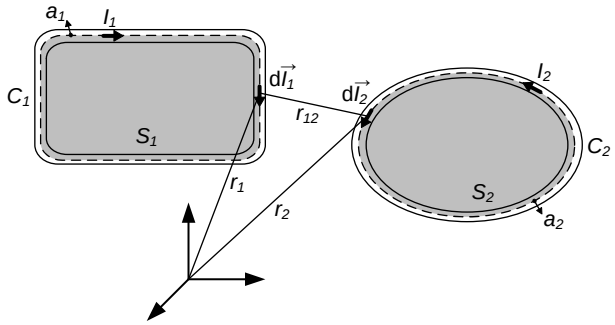


Figure 5.2: Diagram illustrating the currents and geometries of two coupled loops (from [100] © 2008, Wiley.).

internal to the conducting wire. These two contribute to the so-called external (L_{ext}) and internal (L_{int}) inductances, respectively, and the total inductance is the sum of both. However, the internal inductance can be normally neglected because it is normally very small compared with the external inductance in typical loop dimensions[1] and it vanishes at high frequencies when the skin effect is well developed. So, at high frequencies (up to the point where the quasi-static assumption still holds), the total self-inductance is basically equal to the external inductance defined by the wire loop. This means that for equal-shaped wires forming different loops, the corresponding inductances will differ. Therefore, for adequate predictability of the inductance, the return current path in open loops should be well defined and taken into account.

The strength of the mutual-inductance between a pair (i, j) of circuit loops can be expressed using a figure-of-merit called (magnetic) coupling factor k_m which is simply the ratio between the mutual-inductance and the geometric mean of the self-inductances of the loops (notice that $M_{ij} = M_{ji}$ because the integration in (5.3) can be performed in any order), this is

$$k_m = \sqrt{\frac{M_{ij} \cdot M_{ji}}{L_{ii} \cdot L_{jj}}} = \frac{M_{ij}}{\sqrt{L_{ii} \cdot L_{jj}}} \tag{5.4}$$

which is bounded by $|k_m| < 1$, where $|k_m| = 1$ represents that the two circuit loops are coupled perfectly (e.g. in an ideal transformer).

5.2.2. INDUCTANCES FOR ROUND-WIRE CONDUCTORS

The analytical expressions for the inductance of general wire loops (i.e. the solutions to (5.1)) are unduly complicated except for some very simple and idealized cases. There

[1] For example, for straight round wires, the internal inductance per-unit-length is $L'_{int} = \frac{\mu}{8\pi}$ and this is only 50pH/mm which is normally very small compared to the external inductance formed by the loop of those wires.

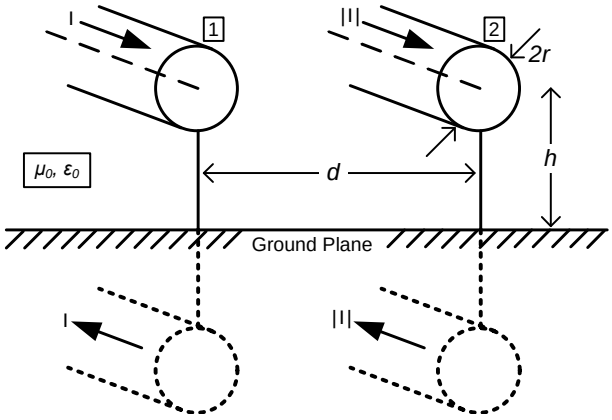


Figure 5.3: Diagram illustrating the currents and geometries of two straight and round-wire coupled conductors.

are numerous formulas and methods for computing the approximate behavior of self-inductance and mutual-inductance of close loops by solving (5.1) by magnetic fields solutions using the Biot-Savart law or by Neumann's equation [101, 102]. Since bondwires form non-closed loops, the resulting open loops can be treated using the concept of partial inductance [100, 102]. This means that complex shaped loops can be segmented into smaller linear pieces such that its total inductance is the algebraic sum of the individual partial inductances of those pieces.

As can be appreciated in (5.2) and (5.3), the inductance in a bondwire basically depends on the geometry of the loop formed with the ground, its cross section area and other conductors nearby which could be coupled. For a basic understanding of the main parameters influencing inductance in bondwires, it is instructive to analyze the idealized case of a couple of parallel round-wire conductors of radius r_w, separated by center-to-center distance d, and placed at a distance h above a large return ground plane as illustrated in Fig. 5.3. At high frequencies, the self-inductance and mutual-inductance *per-unit-length* of *each* of the two wires in the figure (assumed infinitely long) are given by [103, Ch. 4.2] [100], independent of their interconnection (i.e. independent on the relative current direction between both wires):

$$L'_{11} = L'_{22} = \frac{\mu_0}{2\pi}\cosh^{-1}\left(\frac{h}{r_w}\right) \approx \frac{\mu_0}{2\pi}\ln\left(\frac{2h}{r_w}\right) \text{ for } h \gg r_w \tag{5.5}$$

$$M'_{12} \approx \frac{\mu_0}{2\pi}\ln\left(1+\left(\frac{2h}{d}\right)^2\right) \tag{5.6}$$

Then, from fundamental circuit theory, if the identical conductors in Fig. 5.3 are joined in parallel (i.e. equal currents flow in the same direction in both wires), the *equivalent total* inductance is given by the parallel of the individual equivalent inductances according to

$$L'_{eq} = \frac{L'_{11} + M'_{12}}{2} \tag{5.7}$$

Similarly, if more wires are joined in parallel, there will be a mutual-inductance between every pair and the equivalent total inductance equation will be an expanded version of the previous one that will include the added mutual-inductance terms (which are not equal due to the different distances) divided by the number of wires.

The last three simple expressions show general trends of the inductance of (sets or arrays of) bondwires, represented simplistically by the parallel wires in Fig. 5.3. To increase (or alternatively, decrease) both the self-inductance and mutual-inductance of the bondwires, the flux of the loops should be increased (or alternatively, reduced). For a given wire radius, this is accomplished by controlling the area of the loop via the length of the wire and its height from the ground plane as indicated by (5.5) and (5.6). In addition, the spacing distance d affects the mutual-inductance as indicated in (5.6). (5.7) also indicates that the equivalent inductance of several bondwires in parallel do not scale linearly with their number due to their magnetic coupling. It shall be noted that the derivation of the expressions (5.5) and (5.6) underlie the assumption of uniform current distribution along the peripheries of the wires. This assumption restricts the accuracy of those expressions when the separation of the wires between ground or between them is not large compared to the radius.

It is interesting to recall that the product of the inductance per-unit-length L' and the capacitance per-unit-length C' of any (homogeneous) transmission line in a homogeneous medium is a constant related to the propagation velocity v_p in the medium (defined by the permittivity ϵ and permeability μ), given by $L'C' = \frac{1}{v_p^2} = \frac{1}{\epsilon \cdot \mu}$. This means that once either L' or C' is known, the other element can be readily calculated using the previous equation and hence the lossless transmission line is fully characterized, with characteristic impedance $Z_o = \sqrt{\frac{L'}{C'}}$. When analyzing a bondwire set such as Fig. 5.3 terminated with an impedance Z_t, the resulting network can have either an inductive behavior if $Z_o > Z_t$ or a capacitive behavior if $Z_o < Z_t$ [104]. However, the bondwire set itself will behave inductively up to its own resonance frequency, where the capacitance to ground start to dominate[2].

In practice, the inductance expressions in (5.5) and (5.6) do not provide sufficient accuracy for the design of practical inductive components based on bondwires shapes, even when using concepts such as the average height of the bondwire arc above the ground plane for complex loop shapes [105]. In addition, other important high frequency effects such as non-uniform current densities due to proximity effects, surrounding environment (metals and dielectrics) interactions, etc., are not accounted for by those expressions. For this reason, after a basic understanding on the basic geometrical characteristics of inductance as described previously, it is more practical to rely on accurate simulation methods. Bondwire models exist in circuit simulators such as Agilent ADS that are based on basic loop shape geometries and materials, such as the

[2] Using distributed analysis of a shorted distributed LC line of length ℓ, the first resonance frequency occurs at $\omega = \frac{\pi}{2 \cdot \ell \cdot \sqrt{L' \cdot C'}}$ which is $2/\pi$ times lower than predicted by circuit theory that neglects any spacial variation in the fields [99].

Mouthaan's wire-curved-array model [104]. However, more general and accurate models can be obtained using finite-element-methods in full-wave 3D electromagnetic simulation tools, such as Ansoft HFSS [105, pp. 133]. This second option is preferred here due to its greater versatility and accuracy (the inherent increase of computational resources required can be reduced significantly by judicious choices on the simplification of the structures) as will be clear in the next sections.

5.2.3. LOSSES AND CURRENT-HANDLING OF BONDWIRES

The main loss mechanism in an electrically short bondwire is the ohmic losses. Note that the losses associated to induced Eddy currents are much lower for bondwires than for monolithic inductors due to the much larger separation from the ground. At low frequencies the conductive losses are simply related to the DC resistance of the conductors due to their material properties and their physical dimensions. At high frequencies, the skin effect decreases the effective cross section area of the conductors and thus the AC resistance increases. Since the skin depth δ at frequency f is given by

$$\delta = 1/\sqrt{\pi \cdot f \cdot \mu \cdot \sigma} \tag{5.8}$$

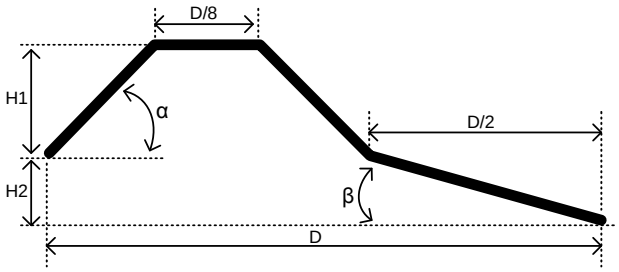
for a material with conductivity σ, then the AC resistance per-unit-length R'_{AC} of a single round-wire of radius r_w is

$$R'_{AC} = \frac{1}{\pi \cdot \sigma \left(r_w^2 - (r_w - \delta)^2\right)} \approx \frac{1}{2\pi \cdot \sigma \cdot r_w \cdot \delta} \tag{5.9}$$

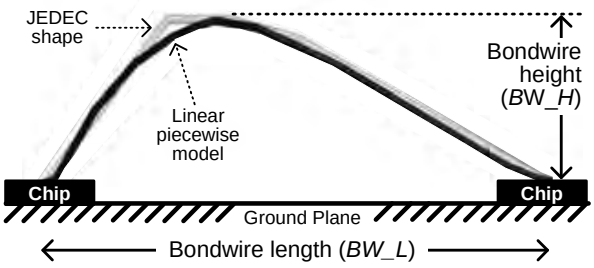
For example, for 50μm-diameter aluminium and gold wires at 2.1 GHz, R'_{AC} is about 102 and 110 mΩ/mm per wire, respectively. When current is flowing through the conductor, the losses due to R'_{AC} are converted into heat. When significant current is passing through the conductor wire, the temperature can rise up too much. The current level at which the wire can melt is known as fusing current [106] and sets a hard limit for the current-handling capability for the wires. For example, a 5 mm-long and 50μm-diameter AlMg wire has a fusing current of about 0.7 A at 1.8 GHz, while gold wires can support about 25% higher currents [106]. Even though parallel connection of wires will reduce losses and increase the current-handling capability, conservative limits are recommended to avoid this failure mechanism.

5.3. DESIGN AND MODELING OF BONDWIRE INDUCTORS

Bondwires have excellent inductive properties that combined with their low losses and high current-handling capabilities make them very attractive for the implementation of high-quality magnetic components in matching networks for high-power applications.



(a) 5-point JEDEC model [107].

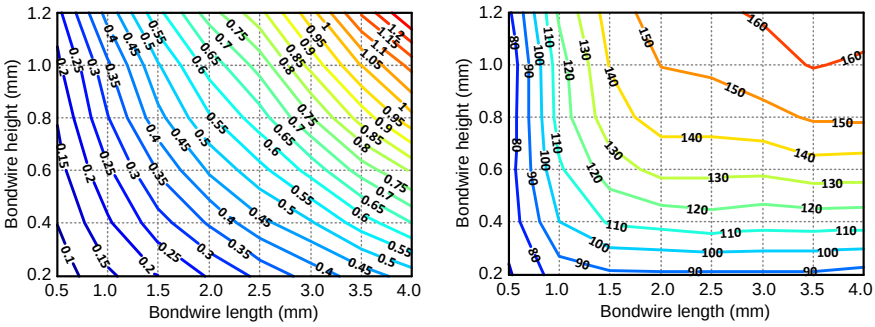


(b) Arbitrary model.

Figure 5.4: Piece-wise geometrical models for bondwire shapes.

Additionally, their small electrical dimensions and their sufficiently high resonance frequencies allow operation up to a few gigahertz while still allowing the use of a lumped model approximation.

In general, bondwire arrays can be accurately simulated with the aid of full-wave 3D electromagnetic (EM) tools [95] as long as their shapes are well known. However, for the design of an inductive bondwire section with a specific predefined electrical performance, there are several design variables that can be used to achieve the aimed behavior such as the number of paralleled bondwires, their pitch, their length (BW_L) and their height (BW_H) from the ground plane. Other variables such as the wire material and wire diameter are normally fixed for a given bonding process. The minimum number of paralleled wires can be determined in terms of the current-handling requirements as described in previously and the acceptable losses of the section. Still, for determining the remaining design variables, normally several simulation iterations and some practical experimentation are needed to arrive at the required parameters. This process can be simplified with the use of standardized geometrical models for bondwire loop shapes such as the 5-point JEDEC bondwire model [107] shown in Fig. 5.4a. This simplified piece-wise linear model has only five independent parameters (three distance parameters D, $H1$ and $H2$, and two positive angles α and β) and is available in many simulation tools. Because of its simplicity and generality is useful for design purposes. Fig. 5.4b depicts an arbitrary piece-wise linear shape for a bondwire bonded to two semiconductor dies with its equivalent JEDEC model indicating an acceptable geometrical



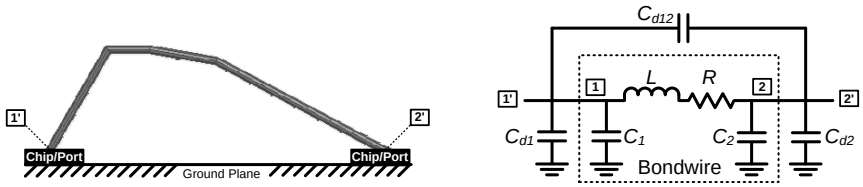
(a) Self inductance (nH). (b) Quality factor (-).

Figure 5.5: Example of an inductance design chart created in MATLAB from HFSS simulations for 8 parallel aluminum bondwires (further details are given in the text): a) selft inductance and b) quality factor.

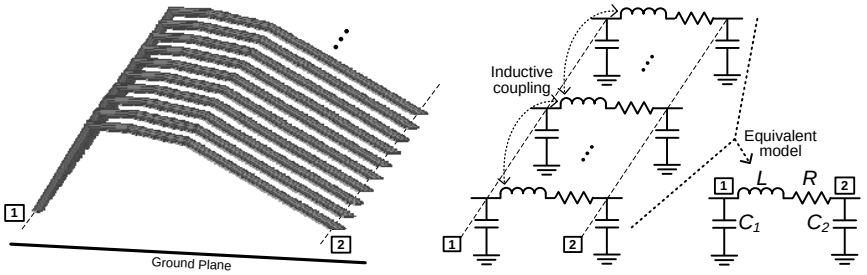
match. Such arbitrary piece-wise linear models are more useful for analyzing already constructed wires but contain too many degrees of freedom for design purposes. This is because most automatic wire-bonding machines have currently limited capabilities for reproducing exact bondwire shapes and therefore practical experimentation using simpler parameters such as their horizontal length BW_L (or even their arc length) and vertical height BW_H is normally required. These ad hoc experiments normally start from predetermined loop shape recipes.

Appropriate EM simulations in the form of design charts, or similar, can greatly simplify this design process. These charts can be created by fixing some variables such as the number of bondwires in parallel, their pitch, the wire material and diameter while sweeping other variables such as the bondwire length and height with the aid of the simple 5-point JEDEC bondwire model. An example of these design charts is given in Fig. 5.5 that shows the simulated (and de-embedded) equivalent inductance, as well as the corresponding quality factor, of an array of 8 aluminum wires with 50μm-diameter (using 10 facets) at 100μm above the ground plane (which is the height of a normal semiconductor die such as a MOS capacitor) and 300μm-pitch. This chart was created by collecting the results from multiple simulations in Ansoft HFSS, controlled from a dedicated MATLAB script that creates automatically the corresponding JEDEC shapes (similar to Fig. 5.4) for each value of BW_L and BW_H within the realizable ranges. Note that for the considered bondwire parameters, a 1:10 range of inductance values can be realized and that indeed very high quality factors can be obtained. Regarding the simulation and de-embedding procedure for the bondwire structures whose results are given in Fig. 5.5, a few extra details are relevant and given next.

HFSS is a commercial electromagnetic solver from Ansoft, Inc. based on the finite element method. It first computes fields and then scattering parameters from an arbitrary 3D object with multiple ports. After the 3D geometry and its boundary conditions have been defined, an initial mesh is created in order to solve the electromagnetic fields and compute the corresponding scattering parameters. After each simulation run, the mesh



(a) Lateral view representation (left) and equivalent schematic (right).



(b) Lateral tilted view representation (left) and equivalent schematic (right).

Figure 5.6: Compact model of 2-port bondwire inductor structures: a) before and b) after de-embedding.

is redefined in order to reach the minimum predetermined simulation accuracy (based on a general error criterion from the scattering parameters). In this process, several parameters affect both the accuracy and the computation time of the HFSS simulations, such as the objects discretization, the box dimensions, the boundary conditions, etc. These parameters must be experimentally determined such that an acceptable compromise between accuracy and computation time is accomplished.

In order to extract the equivalent inductance from the simulated structures in HFSS, the compact model shown in Fig. 5.6 is assumed. The inner pi-network in Fig. 5.6a (alternatively, also a T-network can be used) can fairly represent an electrically short 2-port bondwire inductor. The external and surrounding capacitors C_{d1}, C_{d2} and C_{d12} represent parasitic capacitance due to artificial ports in the simulation bench if any. The internal elements L, R and $C_{1,2}$ represent the actual equivalent inductance, its losses and its parasitic capacitance to ground. Therefore, if strip ports of non-negligible capacitance to ground are used in the simulation (e.g. to interconnect several bondwires in parallel in order to avoid defining individual ports for each bondwire and hence to reduce simulation complexity as in Fig. 5.6b) these ports need to be de-embedded from the results in order to move the reference planes from ports 1'-2' to ports 1-2, as shown in Fig. 5.6a. This is easily done by performing two separate simulations: one with the entire structure and its ports (Y_{all}) and the other with only the ports (Y_{par}). Then, the Y-parameters of the actual (internal) bondwire structure (Y_{DUT}) is simply given by $Y_{DUT} = Y_{all} - Y_{par}$. From the resulting Y_{DUT}, the compact model illustrated in Fig. 5.6b can be obtained directly using the known equations summarized in Table 5.1. Those equations were used to create the design chart showed previously in Fig. 5.5.

Table 5.1: COMPACT MODEL EQUATIONS FOR 2-PORT INDUCTORS FROM $Y = Y_{DUT}$ MATRIX.

Parameters	Equations
Inductance	$L = \mathrm{Im}\{-1/Y_{12}\}/\omega$
Resistance	$R = \mathrm{Re}\{-1/Y_{12}\}$
Quality factor	$Q_L = \omega \cdot L/R = -\mathrm{Im}\{Y_{12}\}/\mathrm{Re}\{Y_{12}\}$
Capacitance to ground	$C_i = \mathrm{Im}\{Y_{ii} + Y_{12}\}/\omega$

5.4. DESIGN AND MODELING OF BONDWIRE TRANSFORMERS

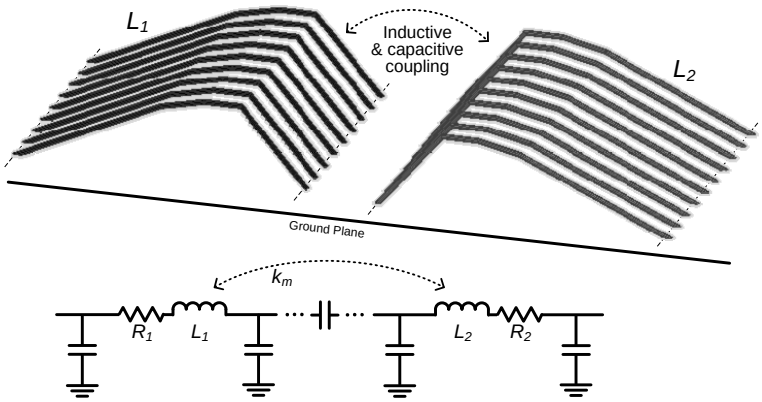
As expected from Neumann's equation in (5.3), the circuit loops of two arrays of bondwires in close proximity will be magnetically coupled as depicted in Fig. 5.7a[3]. Maximizing the overlapping area of the two loops will enhance such magnetic coupling creating effectively a transformer, as illustrated in Fig. 5.7b. This structure will resemble an ordinary 2-port transformer if one end of each bondwire array is grounded, for example either by a large capacitor (AC ground) or by a metallic bar (DC ground). In this case, the resulting simple compact model will be as shown in the same Fig. 5.7b (the dot convention used indicates the direction where the currents are flowing into on each side)[4]. Notice that this is the intrinsic model for the bondwire transformer, where any parasitic capacitance has been already de-embedded as explained previously for the case of the bondwire inductors.

Previous works on bondwire-based transformers were only aimed at multi-turn loops (i.e. bondwire-based sections connected in series) for both conductors [93–98]. On the contrary, the novel transformer concept presented here in Fig. 5.7b is based on parallel connections of the bondwires in each side, effectively forming a single-turn primary-winding transformer. Although the secondary side of the transformer can have multiple turns, for practical implementation reasons also a single turn is preferred on this winding [109]. As for the case of the bondwire inductors, this parallel-bondwire transformer provides significant benefits in terms of low losses, large current-handling capabilities, low-cost and is easily scalable (i.e., its so-called magnetizing inductance is scalable), providing a good design flexibility for high-power RF transistors and amplifiers.

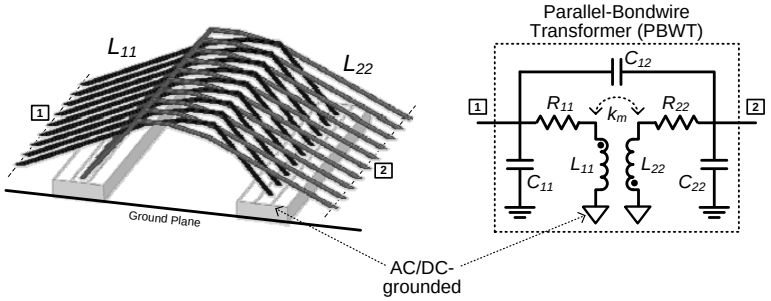
The self-inductances $L_{11,22}$ and mutual-inductance M_{12} (or equivalently, k_m according to (5.4)) as well as the lossy elements $R_{11,22}$ in the 2-port compact model shown in Fig. 5.7b can be directly obtained with a (de-embedded) 2-port Z_{DUT}-matrix with the simple equations given in Table 5.2. At low frequencies, the inductive behavior is dom-

[3] For the case of Fig. 5.7a, the mutual coupling (perhaps weak) is between wire sections of the two bondwire arrays that are non-aligned with respect to the current direction.

[4] A more comprehensible bondwire transformer model can be obtained using a 4-port network definition. The self-inductances, resistances and capacitance to ground of each conductor can be obtained using the same expressions as for the case of simple inductors as given in Table 5.1. Then, by using adequate common- and differential-mode 2-port parameters definitions (expressed compactly with the so-called 4-port mixed-mode parameters like in [108]), the mutual capacitive and inductive coupling can be obtained after the previous variables for each individual inductor are known. However, due to the construction of bondwire transformer itself in Fig. 5.7b, 4-port measurements are difficult to perform and hence this modeling approach is not considered here.



(a) Lateral tilted view representation (top) and equivalent schematic (bottom).



(b) Lateral tilted view representation (left) and equivalent schematic (right).

Figure 5.7: Bondwire transformers: a) coupled bondwire arrays, and b) compact model of 2-port bondwire transformers.

inant and the parasitic capacitance $C_{11,22}$ and C_{12} can be neglected. However, at higher frequencies, that capacitance will cause resonance, modifying the otherwise relatively flat behavior of the magnetic quantities simply extracted using Table 5.2.

In Table 5.2, the *magnetic coupling factor* k_m is more properly referred to as the *mutual reactive coupling factor* k_{lm} to indicate that k_{lm} equals k_m only at low frequencies, deviating at high frequencies due to the parasitic capacitance in the transformer [110]. In addition to the quality factors Q_L of each conductor, the maximum available gain G_{MAX} figure-of-merit is employed to quantify the transformer losses[5] in a realistic and meaningful manner [110]. This is because G_{MAX} quantifies the energy transfer efficiency under ideal conditions (a simultaneous complex conjugate matching at both input and output) which can be accomplished in practice if the reactive components of the transformer are absorbed by the surrounding circuitry.

[5] In dB, the losses are calculated with $10 \cdot \log 10\left(1/G_{MAX}\right)$.

Table 5.2: COMPACT MODEL EQUATIONS AND FIGURES-OF-MERIT FOR 2-PORT TRANSFORMERS FROM~ $Z = Z_{DUT}$ MATRIX.

Parameters and figures-of-merit		**Equations**
Self-inductance	(at port-i)	$L_i = \mathrm{Im}\{Z_{ii}\}/\omega$
Resistance		$R_i = \mathrm{Re}\{Z_{ii}\}$
Quality factor of self-inductance		$Q_{L_i} = \mathrm{Im}\{Z_{ii}\}/\mathrm{Re}\{Z_{ii}\}$
(Mutual reactive) Coupling factor	(between port-i and -j)	$k_{\mathrm{Im}(i,j)} = \sqrt{\frac{\mathrm{Im}\{Z_{ij}\}\cdot\mathrm{Im}\{Z_{ji}\}}{\mathrm{Im}\{Z_{ii}\}\cdot\mathrm{Im}\{Z_{jj}\}}}$
Maximum available gain		$G_{MAX(i,j)} = \left\lvert\frac{Z_{ji}}{Z_{ij}}\right\rvert\left(\kappa_{(i,j)} - \sqrt{\kappa^2_{(i,j)} - 1}\right)$ $\kappa_{(i,j)} = \frac{2\cdot\mathrm{Re}\{Z_{ii}\}\cdot\mathrm{Re}\{Z_{jj}\} - \mathrm{Re}\{Z_{ij}\cdot Z_{ji}\}}{\lvert Z_{ij}\cdot Z_{ji}\rvert}$

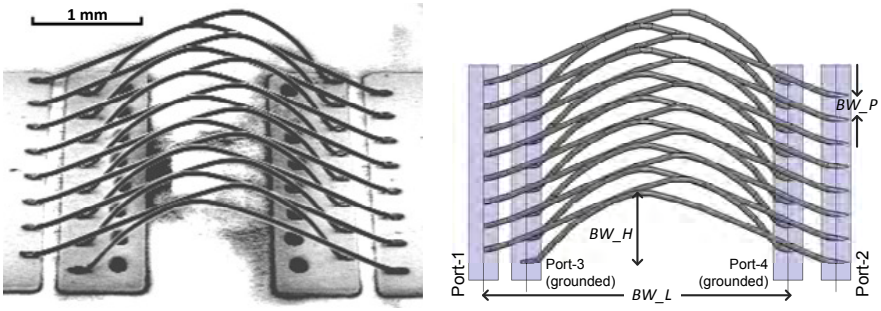
5.5. PRACTICAL IMPLEMENTATION OF A PARALLEL-BONDWIRE TRANSFORMER

In order to demonstrate the feasibility of the proposed parallel-bondwire transformer concept, the design and characterization of one prototype is described in detail in this section. In the following two chapters this kind of transformer will be used in the practical implementation of two compact and high-power RF amplifiers.

5.5.1. TRANSFORMER DESIGN AND IMPLEMENTATION

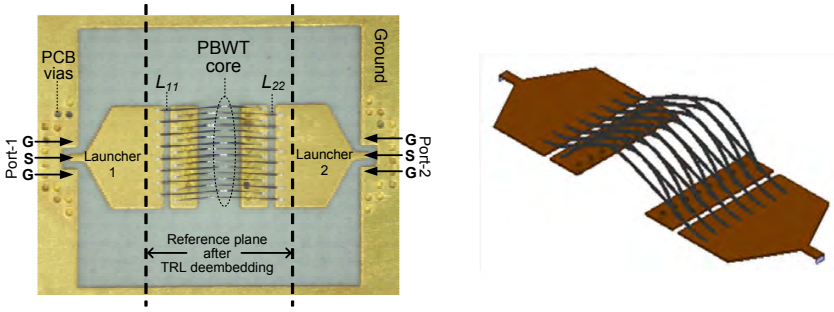
In general, a parallel bondwire-transformer (PBWT) can be implemented in various ways with different turn ratios and winding schemes as outlined in [109]. The prototype described here is a symmetric single-turn transformer with 8 parallel bondwires in both primary and secondary windings. Fig. 5.8a shows a scanning electron microscope (SEM) photograph of the fabricated prototype, placed on a PCB fixture designed for characterizing purposes. Note in this implementation that the return path is formed by the wide bonding pad, the vias (shown at the center of the picture) and finally the ground plane. In a practical application, the windings of this transformer can land on power transistor dies, MOS capacitors dies, etc., as part of compact matching networks. Fig. 5.8b depicts a 3D reconstruction model in HFSS of the fabricated prototype used for EM simulations as will be described shortly.

The height and length of the bondwires in the PBWT, as well as the number of bondwires in parallel, can be chosen such that a desired magnetizing inductance is realized depending on the needs for a particular application. Here, the transformer prototype was designed to obtain a magnetizing inductance in the order of 0.6 nH and a magnetic coupling factor larger than 0.7, with an operating frequency around 2.1 GHz. To achieve this goal, the BW_L and BW_H of the wires in the transformer in Fig. 5.8 were deter-



(a) Size-calibrated SEM photograph. (b) 3D model for EM simulations in HFSS.

Figure 5.8: Fabricated parallel bondwire-transformer prototype.



(a) Photograph. (b) 3D model for EM simulations in HFSS.

Figure 5.9: PCB test fixture for the RF measurements of the PBWT prototype.

mined based on full-wave electromagnetic simulations of simplified bondwire shapes. The bondwires pitch (BW_P) on every array was set to 300μm (i.e. 150μm between neighboring wires) as a compromise between easy manufacturability and high magnetic coupling, although smaller pitches can still be pursued. Aluminum wires with 50μm-diameter were used for the PBWT prototype and were placed using an automatic wire bonder.

Since the electrical behavior of a bondwire structure is affected by the location of the ground plane, the thickness of the fixture substrate in this experiment was chosen such that it approximates the thickness of a typical transistor or capacitor die. Consequently, this prototype and its de-embedding structures were implemented on a special gold-plated double-sided "thin" PCB using 4mil-thick Rogers 4350B substrate, supported mechanically by a 1 mm-thick copper plate bonded on the backside. A photograph of the PCB test structure, including the actual transformer, is provided in Fig. 5.9a. The fixture was designed to be contacted with 500μm-pitch ground-signal-ground (GSG) RF probes.

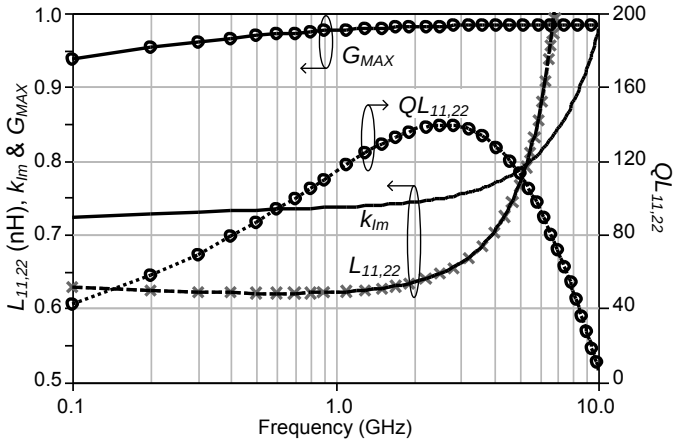


Figure 5.10: EM simulation results of the PBWT core.

5.5.2. TRANSFORMER SIMULATED PERFORMANCE

To establish a detailed performance evaluation of the realized transformer prototype, the size-calibrated SEM microphotograph of the implemented bondwire structure shown in Fig. 5.8a was used to determine the exact loop shape of the actual bondwires. This information was used in HFSS to create a very accurate 3D model of the implemented bondwire transformer core, as shown in Fig. 5.8b. In addition, in order to compare the actual measurement results obtained from the realized transformer with respect to the simulation predictions, another 3D model was also generated in HFSS including a reproduction of the actual test fixture connections in Fig. 5.9a, as shown in Fig. 5.9b.

The PBWT without test fixture connections was first simulated as a 4-port device from 0.1 to 10 GHz. Then, by grounding the inner ports 3 and 4 (see Fig. 5.8b), the performance parameters of the transformer core were calculated using the expressions in Table 5.2. The simulation results for the PBWT "core" (which is the actual device of interest) are given in Fig. 5.10. At 2.1 GHz, its two self-inductances are 0.64 nH with a quality factor of 138, while the reactive coupling factor is 0.75 and the G_{MAX} is as high as 0.98 (or equivalently, a loss of 0.09 dB). As observed, the self-resonance frequency is larger than 10 GHz and the reactive coupling factor is very close to the magnetic coupling factor at 2.1 GHz.

5.5.3. TRANSFORMER RF MEASUREMENTS

RF measurements on the implemented PBWT were performed using an Agilent PNA-X N5242A network analyzer. The PBWT core and the main parasitic components of its PCB test fixture are depicted in Fig. 5.11. The signal launchers are represented by the matrices $T_{A,B}$ in Fig. 5.11. First, the measurement setup was calibrated at the RF probe tip refer-

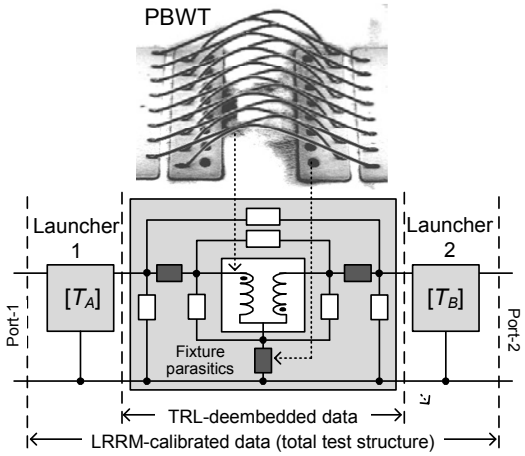
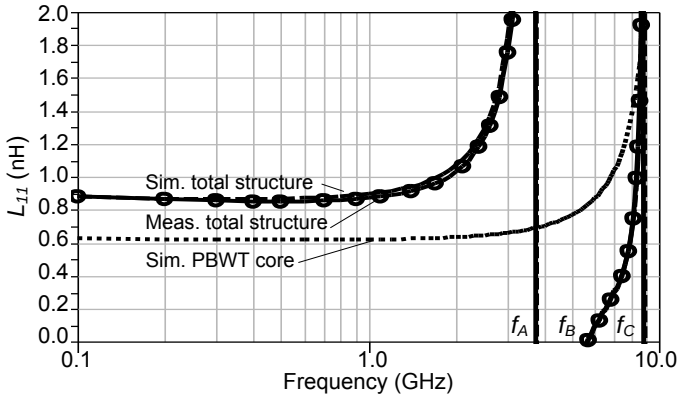


Figure 5.11: PBWT core and the main parasitic components of its PCB test fixture.

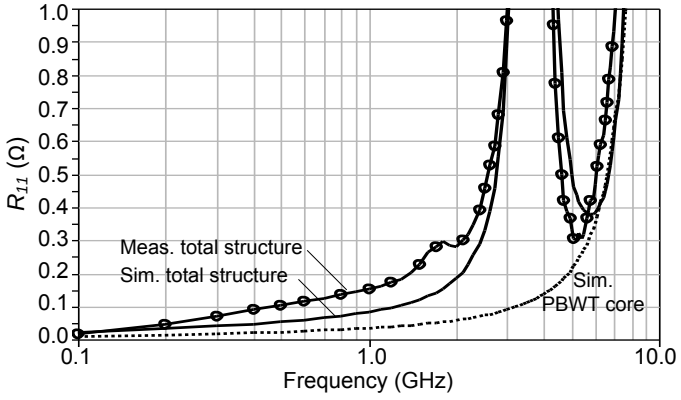
ence plane using the LRRM calibration method with a commercial impedance substrate. Next, the PBWT including the PCB signal launchers was measured, and some results are shown in Fig. 5.12 (called "Meas. total test structure"). In addition, the simulated results of the two HFSS models of the PBWT (i.e. the one including signal launchers and the one with only the core) are also plotted in Fig. 5.12 (called "Sim. total test structure" and "Sim. PBWT core", respectively). An excellent agreement between measured and simulated data of the PBWT including signal launchers can be observed, validating the chosen microphotograph-based 3D-EM modeling approach. The resonances observed in Fig. 5.12 at the frequencies f_A and f_B, are dominated by the capacitive loading of the PCB signal launchers, while f_C is dominated by the PBWT self-resonance frequency (observe in Fig. 5.10 that the simulated PBWT core only resonates slightly above f_C).

As a second step, a multi-line TRL de-embedding method was applied in order to move the reference planes up to the bond pads of the PBWT (see Fig. 5.9a and Fig. 5.11). This step removes the coplanar-to-microstrip launcher that connects to the bonding pads of the PBWT. The resulting self-inductance and mutual reactive coupling factor of the PBWT prototype are given in Fig. 5.13. Also here, an excellent agreement between the de-embedded measurement data (called "Meas. TRL-deemb.") and the HFSS simulated results (called "Sim. TRL-deemb.") of the transformer can be appreciated. At 2.1 GHz, the measured self-inductances, reactive coupling factor and self-resonance of the PBWT without launchers are 0.59 nH, 0.71 and 6.8 GHz, compared to 0.63 nH, 0.70 and 7.0 GHz obtained from the related HFSS simulations, respectively.

As expected from the simulations in Fig. 5.10, the losses of the PBWT are very low and the measurement results are given in Fig. 5.14. For the PBWT structure including signal launchers, at 2.1 GHz the measured G_{MAX} (LRRM calibrated) is 0.95 with an associated loss of only 0.22 dB. Note that this is very close to the related simulated HFSS results (G_{MAX} = 0.96, 0.18 dB loss). Further de-embedding could remove the remaining parasitic elements, such as PCB vias and bond pads (see Fig. 5.11), bringing the



(a) Self-inductance.



(b) Equivalent series resistance.

Figure 5.12: Measured and simulated self-inductance and resistance of the PBWT prototype at port-1.

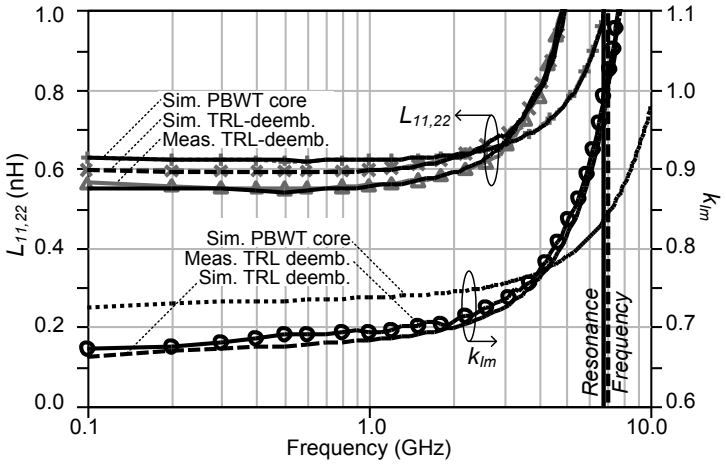


Figure 5.13: Measured (after TRL de-embedding) and simulated (after TRL de-embedding and for the core alone) self-inductance and mutual reactive coupling factor of the PBWT prototype.

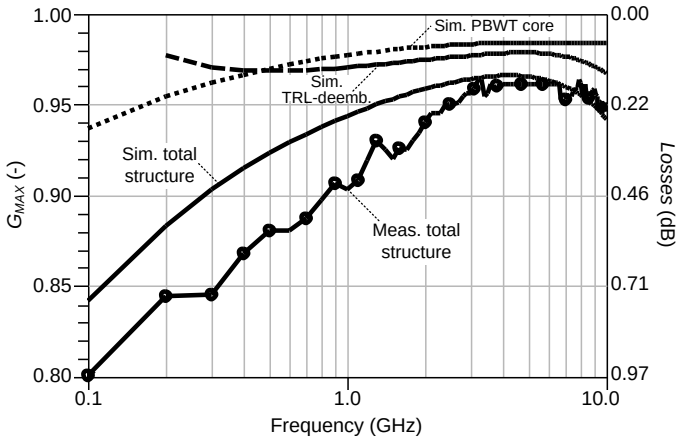


Figure 5.14: Maximum available gain and losses for the PBWT prototype with launchers (measured and simulated), the PBWT without launchers (simulated) and the PBWT core-only (simulated).

measurement reference plane to the actual PBWT core and therefore reducing the losses associated with the measurement. However, the losses are already very small such that in practice this becomes very challenging. Instead, Fig. 5.14 shows simulation results when removing the effect of the launchers, when G_{MAX} increases to 0.97 (0.13 dB of losses), and reproduces the results of only the PBWT core in Fig. 5.10, where G_{MAX} is as high as 0.98 (or equivalently, a loss of 0.09 dB).

5.6. CONCLUSIONS

This chapter reviewed important aspects in the design of compact and low-cost magnetic structures based on bondwires such as inductors and transformers. Since these structures employ several bondwires in parallel, they provide significant benefits in terms of low losses and large current-handling capabilities which are especially important for high-power RF transistors and amplifiers. The practical demonstration focused on the novel single-turn parallel-bondwire transformer aimed for high-power applications. This RF transformer differs from previous works that have focused on series connected multi-turn bondwire-transformer structures. It was shown that the RF performance of this new bondwire-transformer can be accurately predicted and modeled using 3D EM simulations. In addition, RF measurements indicated state-of-the-art performance in terms of low losses and high magnetic coupling for a compact RF transformer. The discussed bondwire-based components are key elements in the implementation of compact and high-performance amplifier implementations, as the ones described in the next chapters.

6

TOWARDS PACKAGE-INTEGRATED HIGH-POWER RF STAGES

6.1. INTRODUCTION

For wireless infrastructure applications, high-power amplifiers fully integrated in a package [75, 111–114] are an appealing approach to achieve improved RF performance, low form factors and lower system costs. In a package-integrated PA, the reduced dimensions and electrical delays can provide increased RF bandwidth while the efficiency can be enhanced by providing proper harmonic loading right at the transistor die [75, 115] or even at the transistor unit cell [112]. Also, having DC bias decoupling inside the package helps to reduce the long term memory effects and hence eases predistortion [116].

This relative new direction in high power amplifier implementation (e.g. [75, 111–114]) requires more sophisticated simulations and design techniques, due to increased design complexity and tighter implementation constrains. This is especially important when aiming to work with the low-cost bondwire technologies described in the previous chapter. However, the potential benefits of such an integrated approach can compensate for the difficulties. Note that the implementation constrains for package-integrated PAs are mainly due to the restricted physical space and the limited design space for the passive components. Inside the package, those components are typically shunt low-density and high-density metal-oxide-semiconductor capacitor dies (MOSCAP), series bondwire inductors and the package itself (whose leads can be considered as low-density ca-

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pacitors or short transmission lines) [105]. Also, passive integration and miniature PCBs can be used (e.g. to build transmission lines and/or metal-insulator-metal capacitors, MIMCAPs, in high-ϵ_r substrates [112–114]).

This chapter discusses specific design and implementation aspects aimed at the designing of low-cost package-integrated PAs. Two practical examples of compact GaN high-power amplifiers using class-E are demonstrated. The two compact PA implementation examples use different bondwire-based output matching networks. These designs are evaluated for their predicted physics-based performance versus actual measured data when attention is given to implementation deviations and tolerances when using bondwires.

6.2. DESIGNING PACKAGE-INTEGRATED PA MODULES

In conventional RF PAs, the design typically starts with a packaged transistor (potentially including some impedance pre-matching) and focuses on the design of the external matching networks (that aims at providing proper fundamental and harmonics loading conditions), biasing and power combining using transmission lines on a relative large PCB (compared to the package size). In contrast, a package-integrated PA design starts from the bare transistor die and aims at implementing all the PA network functions inside a (compact) transistor package, using mainly conventional low-cost in-package components such as bondwires and MOS/MIM pre-match capacitors of restricted realizable values. In addition, as discussed in the previous chapter, low-loss and high-power inductors and transformers can be designed from bondwire structures. Together with pre-match capacitors, the bondwire structures can enable advanced harmonic impedance manipulation right at the devices reference plane, ultimately leading to higher performance. For example, [115] demonstrates that by proper internal pre-matching design, the peak efficiency of a packaged GaN HEMT can be desensitized with respect to the second harmonic load, allowing the designer to only focus on synthesizing externally the fundamental load and hence facilitating high-efficiency over broadband. Another very recent example is given in [75] that demonstrates a packaged CMOS-GaN class-E amplifier implementation in which a single-stage *LC*-ladder is used to implement the required bandpass harmonics filtering inside the package, leading to state-of-art efficiency performance.

The design of package-integrated PAs needs to consider practical limits not only on component values but also in network topologies, a tighter restriction than for conventional PCB-based RF PAs. To handle these constrains, some iterations are needed between the design of the individual components and the design of the actual amplifier topology, as illustrated in Fig. 6.1. In addition, package-integrated PAs require 3D electromagnetic (EM) tools for simulating their bondwires and the surrounding package while the power transistor bars and other components (e.g. MIM/MOSCAPs, external PCB, SMD components, etc.) need to be handled by models in the standard circuit simulators. In addition, when designing the overall bondwire-based matching networks, proper design segmentation needs to be applied to minimize the computational

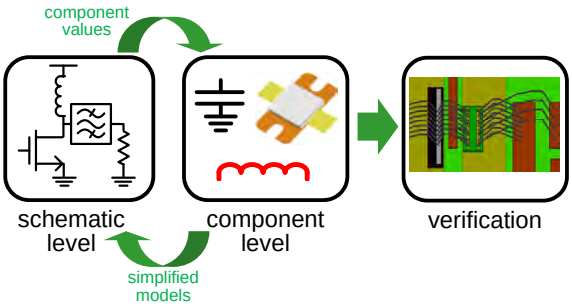


Figure 6.1: Package-integrated PA design flow. The realizable individual components influences the PA topology and co-simulations between standard circuit simulators and 3D EM simulators are needed to confirm the actual design performance.

requirements of the 3D EM solver while preserving all relevant EM interactions [117]. For example, although it is tempting to treat each bondwire inductance in the design as an independent section, one should be aware that due to their 3D nature and their close proximity, some of these sections can couple. This is a much stronger EM interaction than what can be typically found in classical transmission line implementations and can seriously affect the PA stability and performance if not properly considered during the design phase. Interdigitated bondwire arrays (e.g. at the gate and/or drain contacts of the transistor die, as depicted in the example at the right in Fig. 6.1) must always be designed together as a single structure in order to account for the coupled inductances, like a transformer [118]. After the design of all the matching sections is concluded, a complete 3D EM model must be created in order to validate the overall PA design.

The next sections describe two practical examples of the design, implementation and measurements of two broadband class-E power amplifiers using bare GaN HEMT dies and aiming for package integration. The effect of bondwire tolerances in those designs will be discussed at the end.

6.3. COMPACT PA DESIGN 1: A 65 W CLASS-E PA OPERATING AT 1.7-2.3 GHZ

This section describes the design, implementation and measurements of the first example of a very compact PA aimed for package-integration: a highly efficient, 65 W wideband GaN class-E power amplifier. Optimum class-E loading conditions are achieved using a wideband design and implementation approach which is described first. Both input (IMN) and output matching networks (OMN) are implemented with bondwire inductors and MOS/MIM capacitors. The resulting amplifier operates from 1.7 to 2.3 GHz with a transducer power gain (G_T) of 12.3±0.9 dB. It provides an output power (P_{out}) of

The work in Section 6.3 was done by Kanjun Shi (while at Delft University of Technology) together with the author of this thesis, and published in [119].

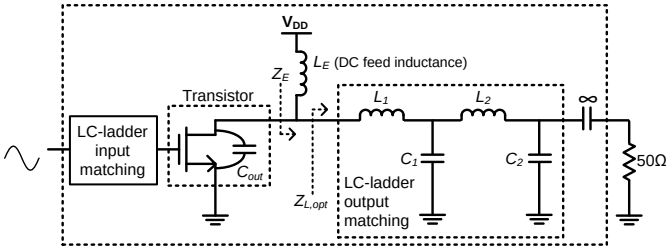


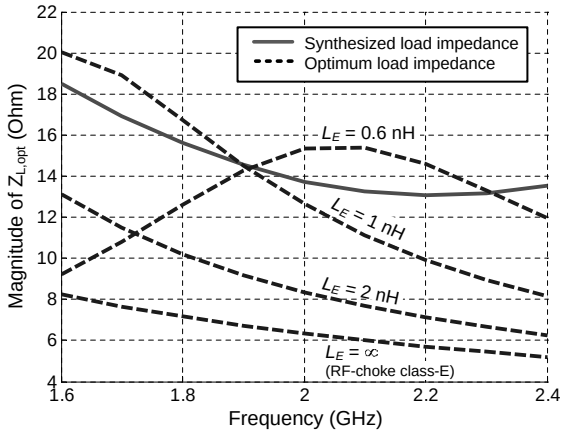
Figure 6.2: Basic schematic of the first class-E compact PA design, using a finite DC feed inductance L_E.

42 to 65 W with a drain-efficiency (η_{DE}) from 68 to 75% and a power-added efficiency (PAE) from 63 to 72%. The total effective area of the amplifier, including bias arrangements, input and output matching networks to 50Ω, is only 2-by-2 cm^2.

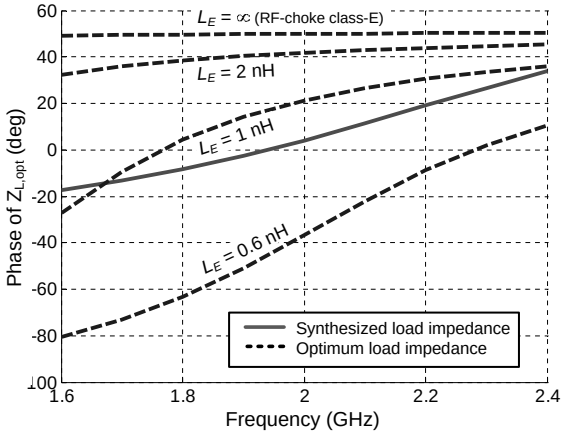
6.3.1. WIDEBAND CLASS-E PA DESIGN

It is known that the traditional RF-choke class-E PA [79] is a narrow-band amplifier and its high-efficiency bandwidth is roughly inversely proportional to the Q_L of the output network for moderate to large values of Q_L [120]. As described previously in Subsection 3.3.2, this classical amplifier employs an RF-choke, a series reactance (X_E) and a LC-series resonator prior to its real load (R_L) in order to accomplish the so-called optimum class-E loading conditions [81]. Under these conditions, the parasitic drain capacitance of the switching transistor (C_{out}) is completely discharged before the device is turned-on, avoiding any capacitive switching loss and leading to the theoretical 100% efficiency of this PA class. However, the above circuit conditions only apply at the design frequency, where the LC-resonator passes the fundamental signal "untouched" to the load, while all higher harmonics are blocked. In fact, when deviating from the design frequency, both the shunt capacitive susceptance ($B = \omega \cdot C_{out}$) and the net load reactance X_E will vary, yielding violation of those optimum class-E loading conditions [120]. While B is simply proportional to the frequency, X_E also depends on the Q_L of the output circuit as well as the operating frequency. For low values of Q_L, the efficiency degradation is mainly caused by the variation of the effective load reactance with frequency. For large values of Q_L, the output circuit effectively tends to decouple the load when the operating frequency starts to significantly differ from the design (or center) frequency.

To overcome the bandwidth limitations associated with the traditional class-E topology, in this first PA design, the class-E output configuration depicted in Fig. 6.2 is utilized. This wideband class-E topology uses a finite feed inductor, an LC "low-pass" ladder filter topology [121] and a DC blocking capacitor. Besides blocking the higher harmonics, this LC-ladder network converts the external 50Ω load to the desired class-E loading, at the device plane, over the frequency range of interest. The combination of a finite DC feed inductance L_E with an LC-ladder output matching network provides more flexibility in the PA design to achieve a large operating bandwidth. In fact, L_E can be employed to



(a)



(b)

Figure 6.3: Optimum (dashed lines) and synthesized (solid lines) class-E load impedance $Z_{L,opt}$ for the first PA design with different feed inductance values: a) magnitude and b) phase.

control the frequency behavior of the optimum PA load impedance $Z_{L,opt}$. In Fig. 6.3, the optimum load impedance over frequency, at the reference plane indicated in Fig. 6.2, is shown for different L_E values (dashed lines). These results were obtained after ideal load-pull simulations in Agilent ADS using a large-signal transistor model of the actual bare die device used in this amplifier.

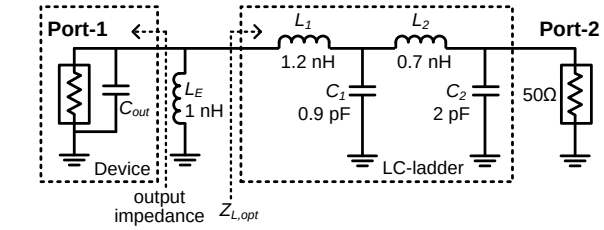
The output matching network of the PA was implemented by the *LC*-ladder network that is shown in Fig. 6.4a. That network tends to provide an input impedance that goes from capacitive to inductive with increasing frequencies. Consequently, the amplifier feed inductance value should be chosen such that both the input impedance of that *LC*-ladder network and the optimum load trajectory $Z_{L,opt}$ are closely matched over the frequency band of interest, which for this design is from 1.7 to 2.3 GHz. In Fig. 6.3, it is shown that a feed inductance of around 1 nH yields this desired condition, where the solid line represents the input impedance provided by the synthesized *LC* network of Fig. 6.4a. Fig. 6.4b shows the resulting "filter performance" of the output load network. Maximum insertion loss in the fundamental band is 0.4 dB (at the lower end) while the filter provides at least 3.3 dB and 11.7 dB suppression to the 2nd and 3rd harmonic band, respectively. This provides the amplifier with sufficient harmonic suppression to maintain high efficiency. Note that the *LC* ladder network combined with the finite feed inductance of Fig. 6.4a fulfilled both the fundamental matching as well as the harmonic filtering function needed for the wideband class-E operation.

The input of the PA is also broadband matched with another *LC* ladder network. The proposed matching networks were implemented inside a transistor package by employing bondwire-based inductors and pre-match capacitors, as explained next.

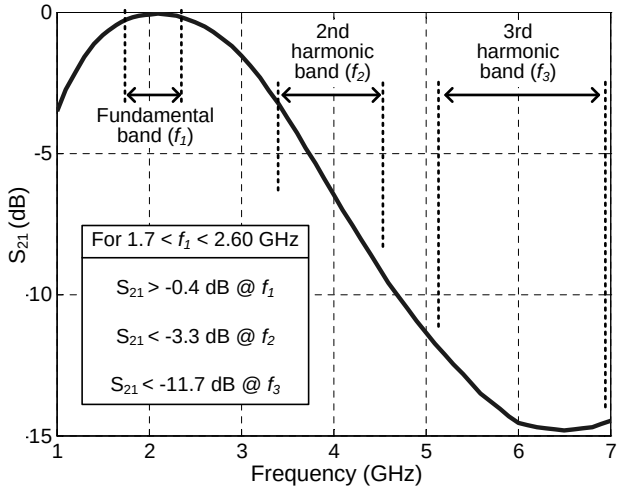
6.3.2. COMPACT PA IMPLEMENTATION

A demonstrator for this compact wideband class-E PA was designed using a 14.4 mm gate periphery GaN HEMT bare die (CGH60060D GaN HEMT from Cree, Inc.). It was fabricated on a gold-plated 2-layer PCB with 4 mil-thick Rogers 4350B substrate, supported by a 1 mm-thick copper backside plate. The transistor die was mounted on top of a 1 mm-thick CuW flange placed at the middle of the PCB. Fig. 6.5 shows the photograph of the PA prototype. The final effective area of this proposed PA is only 2-by-2 cm^2, including all 50Ω input and output matching networks and bias arrangements, as shown in Fig. 6.5.

Fig. 6.6 shows a cross-section view representation of the output matching network and the PCB substrate along with a representative schematic (indicating component values and the main parasitic magnetic coupling K_p at the output side). Inductors in the RF path were implemented with bondwires. Capacitors in the output matching network were implemented as MIM capacitors using the two metal layers of the 4 mil-thick PCB. The gate/drain feed inductances were implemented with a combination of bondwires and microstrip lines, terminated with shunt capacitors. The shunt capacitors in the input matching network are standard MOS die capacitors, which are normally used as pre-match capacitors for packaged power transistors.



(a)



(b)

Figure 6.4: Filter response of the first amplifier output network including C_{out} and L_E: a) equivalent schematic (port-1 is the real part of the transistor output impedance and port-2 is the system 50Ω impedance), b) "filter" gain.

The RF inductors consisted of several equal-shape 50μm diameter aluminum bondwires in parallel. As described previously in Chapter 5, the inductance offered by a bondwire-based structure depends on a number of variables such as the number of paralleled bondwires, their loop shape, the distance to the ground plane, etc. For a set of paralleled bondwires with a given pitch, the bondwire height (BW_H) and length (BW_L) indicated in Fig. 6.6 can be considered the main design parameters for determining the inductance value of the structure. Additionally, the design of every bondwire inductor set must prevent exceeding the fusing current limit of its individual bondwires [106]. For this design, the specific loop shapes of each bondwire inductors were carefully designed to implement the required inductance values and the structures were implemented using automatic bonding machines. HFSS was employed to design each bondwire inductor as well as to verify the entire design. Fig. 6.7 depicts the entire 3D EM model used for the final verification along with a photograph of the corresponding RF section from the actual prototype. During the final design verification, a multi-port

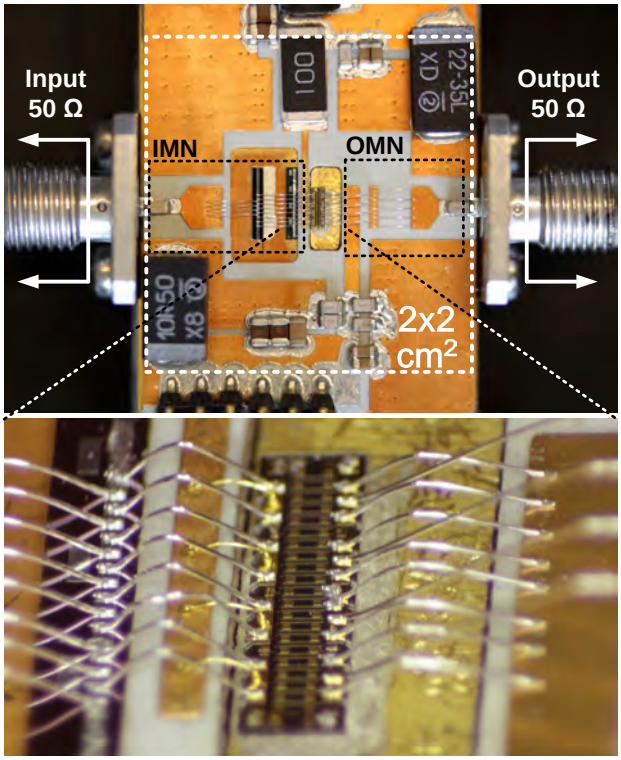


Figure 6.5: Photograph of the first implemented class-E power amplifier prototype with a magnified view centered on the GaN HEMT.

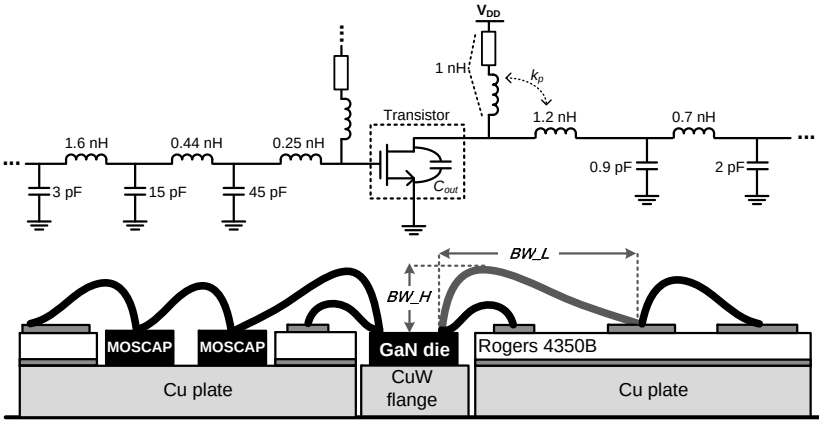


Figure 6.6: Cross section view representation of the implemented output matching network of the first prototype along with a representative schematic.

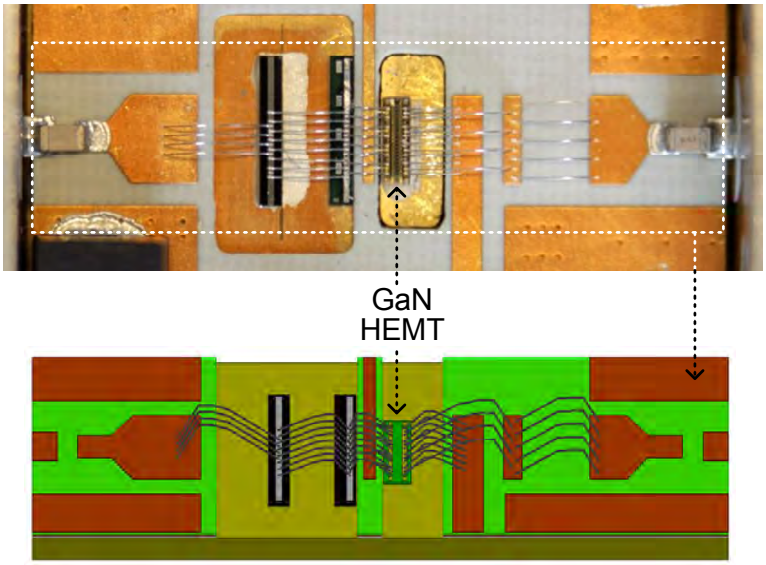


Figure 6.7: Close-up photograph and corresponding 3D EM model in HFSS of the first amplifier's RF section used for final design verification in Agilent ADS.

S-parameters box was obtained from the 3D model in HFSS and was imported into Agilent ADS for running the simulations using the large-signal transistor model and other components models such as various SMD capacitors for AC coupling and de-coupling.

6.3.3. MEASUREMENT RESULTS

To characterize the prototype performance, pulsed RF measurements (10% duty-cycle, 100μsec) were carried out using an in-house active load-pull system [122]. The measured results for a supply voltage of 35 V are shown in Fig. 6.8. This supply voltage guarantees that the GaN device operates below its breakdown voltage and the fusing current of the bondwires is not exceeded over the entire frequency band. The amplifier is driven up to 4 dB compression using 35 dBm of available power from the driving source, yielding a switch-like class-E operation. It can be observed in Fig. 6.8 that from 1.7 to 2.3 GHz, the PA has an output power of 42 to 65W with drain-efficiency and *PAE* between 68 to 75% and 63 to 72%, respectively. In the same frequency range, the transducer power gain remains at 12.3±0.9 dB. These results are summarized in Table 6.1, on page 125, along with other published GaN class-E PA designs operating above 1 GHz and with more than 5 W output power. This amplifier achieves good efficiency performance, comparable with others in the table, but with larger bandwidth and a very compact area. Additionally, the design and implementation approach of this work offers the possibility to integrate the complete 50Ω matched and fully biased PA into a single transistor package.

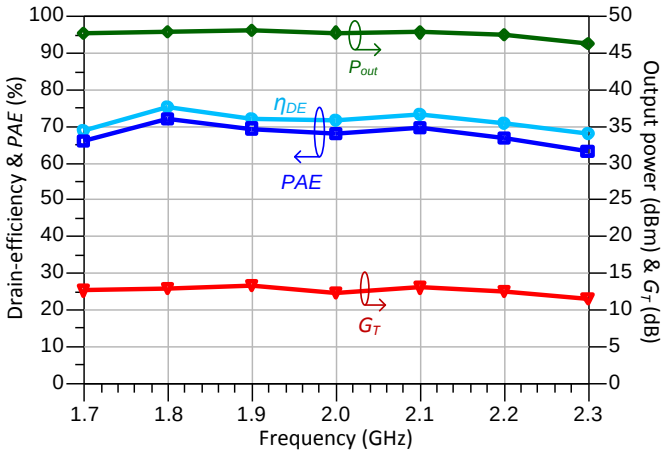


Figure 6.8: Measured RF performance of the first class-E compact PA design.

6.4. COMPACT PA DESIGN 2: A 70 W CLASS-E PA OPERATING AT 1.7-2.6 GHZ

This section describes the design, implementation and measurements of a second compact PA design also aimed for package-integration. This is also a wideband and highly efficient GaN class-E power amplifier but with a different output matching network that is power-scalable. In this case, the large bandwidth performance is achieved by employing directly the so-called "class-E with parallel-circuit" loading conditions [86] using a very compact all-lumped element implementation. The fundamental loading is realized by the magnetizing inductance of the bondwire-based transformer described previously in Section 5.4, which is connected directly at the transistor drain. The PA input and output matching networks are entirely implemented with bondwire inductors and MOS/MIM capacitors. The amplifier provides an output power from 44 to 72 W with a drain-efficiency from 64 to 71%, a *PAE* from 60 to 69% and a transducer power gain of 12.9±1.1dB over 39% bandwidth (1.75-2.60 GHz). The total area of the PA, including bias arrangements, 50Ω input and output matching networks, is 2.9-by-1.7 cm^2.

6.4.1. WIDEBAND CLASS-E PA DESIGN

The wideband output network for the class-E PA in this case is designed according to the "class-E with parallel-circuit" [86] conditions. As described previously in Subsection 3.3.2, the class-E loading conditions Z_E can be implemented in various ways due to the free-to-choose DC feed inductance L_E [82], while various fundamental-tuned filter topologies can be used to present the open condition to the harmonics. In the so-called

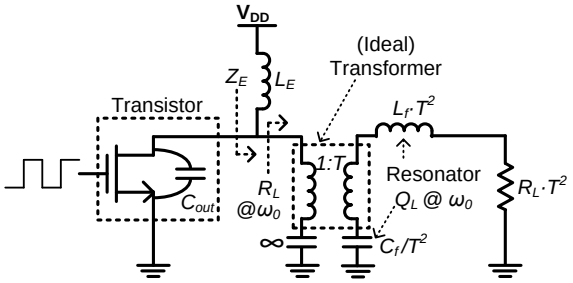


Figure 6.9: Basic schematic of the second wideband class-E power amplifier design using a transformer.

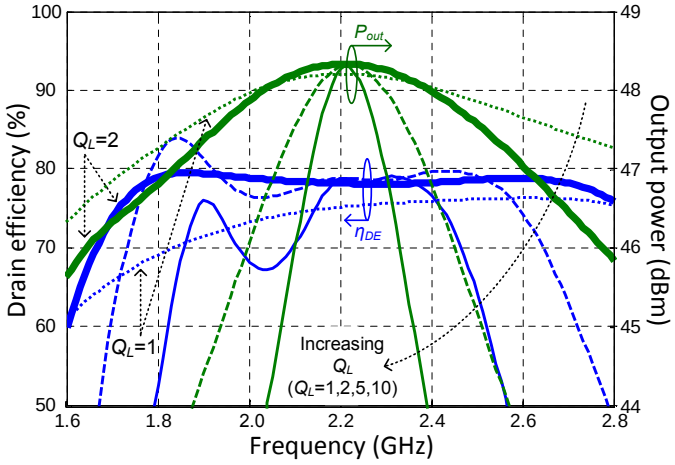


Figure 6.10: Simulated effect of filter Q_L on drain-efficiency and output power for the transformer-based class-E PA with parallel-circuit (see Fig. 6.9).

"class-E with parallel-circuit" [86] L_E is chosen finite and there is no additional reactance X_E needed in series with the filter. This kind of implementation has important benefits over the traditional RF-choke class-E amplifier: it is simpler, its optimum real load impedance is higher (or, equivalently, more power can be obtained for the same load) and it is more broadband in nature.

The first two advantages are due to the fact that X_E can be made zero, while the broadband performance also depends on the quality factor Q_L of the filter. For this second PA, an alternative implementation of the class-E with parallel-circuit is employed by using a transformer, as depicted in Fig. 6.9. In this topology, an *LC* filter is used and it can be placed either at the primary or at the secondary side of the transformer (after proper impedance scaling). For very compact designs aimed for package integration, the use of the parallel-bondwire transformer [118] proves to be useful and facilitates true power-scaling in a natural way, as it will be explained soon.

In class-E PA designs there is a trade-off between efficiency and bandwidth. When the filter Q_L is high, the PA is narrowband and its efficiency is high. For very low values

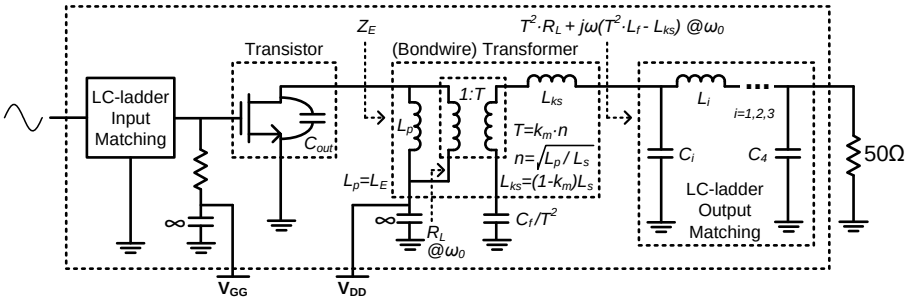


Figure 6.11: Schematic of the implemented transformer-based class-E PA. The input side consists of an *LC*-ladder matching and a precautory stability network. The output side consists of a parallel-bondwire transformer followed by an *LC*-ladder matching network.

of Q_L, the PA is wideband but its efficiency is reduced by the losses related to the imperfect harmonic termination. For example, as mentioned before, the high-efficiency bandwidth of the RF-choke class-E is roughly inversely proportional to Q_L [120]. However, for the class-E with the parallel output circuit such a trade-off is greatly relaxed. In fact, in this later case, even for moderate values of Q_L, the bandwidth can be made broad with almost no efficiency degradation [123]. As a practical demonstration of this fact, Fig. 6.10 shows the simulated performance over frequency for the square-wave driven GaN circuit of Fig. 6.9 for different values of Q_L (1, 2, 5 and 10). These simulations use the large-signal transistor model of the actual GaN HEMT used for this design, as well as realistic parameters for the designed bondwire-based transformer. Reducing Q_L from 10 to 2 increases the bandwidth of the PA with no penalty on efficiency, while reducing it further for example to $Q_L = 1$ such increase comes at the cost of reduced efficiency. For this reason, in this PA design a $Q_L = 2$ was chosen to maximize the PA bandwidth.

The complete schematic of the implemented class-E PA is illustrated in Fig. 6.11. At the output side, the parallel-bondwire RF transformer is connected at the transistor drain and its electrical model is depicted in the figure for clarity. The transformer magnetizing inductance L_p is designed to be equal to the required L_E, while any leakage inductance is absorbed by the filter inductance L_f (scaled at the secondary side of the transformer). Both sides of the transformer are AC-grounded, the primary side by a large de-coupling capacitor and the secondary side via the filter capacitance C_f (also scaled due to its location). A broadband *LC*-ladder output matching network transforms the 50Ω system impedance to the optimum load R_L plus any remaining reactance (if any) required by the *LC* filter. At the input side, another *LC*-ladder input network matches the transistor input impedance to 50Ω while an AC-shorted resistor near the transistor's gate is added as an extra precaution to prevent instability.

The frequency response of the series filter together with the OMN must be broad enough to provide a large RF bandwidth, but also must sufficiently suppress the harmonic bands. Fig. 6.12 shows the simulated "filter response" of the complete output network, including the transistor output impedance (see Fig. 6.11). It can be observed that, between 1.75 and 2.60 GHz, the fundamental band is maintained flat (with a maximum deviation of 0.4 dB), while enough suppression is provided at the harmonic bands.

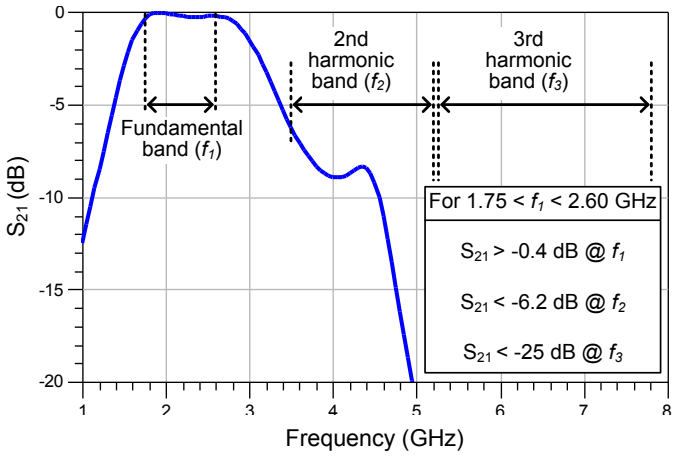


Figure 6.12: Filter response of the amplifier output network including the transistor output capacitance (see Fig. 6.11), where port-1 is the real part of the transistor output impedance and port-2 is the system 50Ω impedance.

6.4.2. COMPACT PA IMPLEMENTATION

This second PA is also implemented using technologies familiar to the implementation of a standard packaged high-power transistor. Both, 50Ω input and output matching networks are realized with bondwires and MIM/MOS capacitors, enabling a very compact design. A photograph of the implemented PA is shown in Fig. 6.13, while a cross-section of its output side is illustrated in Fig. 6.14. This PA employs the same 14.4 mm gate periphery GaN HEMT die used in the amplifier of the previous section. The GaN die was also mounted on top of a 1 mm-thick CuW flange and the shunt capacitors were placed on top of a 1 mm-thick copper plate, as illustrated in Fig. 6.14. Standard MOS pre-match silicon capacitor dies were used for most capacitors, while other non-available small values were implemented using MIM capacitors realized in a 2-layer PCB with 4 mil-thick Rogers 4350B substrate. The same PCB substrate was used for placement of the SMD components in the biasing arrangements.

Also similar to the previous design, the RF-path inductors were realized by placing several equal-shape 50μm diameter aluminum bondwires in parallel employing an automatic wire bonding machine. The specific shape of each bondwire set (e.g., bondwire height and length) was carefully designed for the desired inductance values by using extensive 3D EM simulations in HFSS. The transformer at the output of the PA is a parallel-bondwire transformer whose design was previously detailed in Section 5.4. This PBWT was implemented by two coupled parallel bondwire sets, providing a magnetic coupling above 0.6 and very low losses in the order of 0.2 dB ($G_{MAX} \approx 0.95$) [118]. Due to this implementation approach, the PA effective area was only 2.9-by-1.7 cm^2, including all 50Ω input and output matching networks and bias arrangements, as shown in the photograph in Fig. 6.13. Fig. 6.15 shows the entire 3D EM model used for the final design

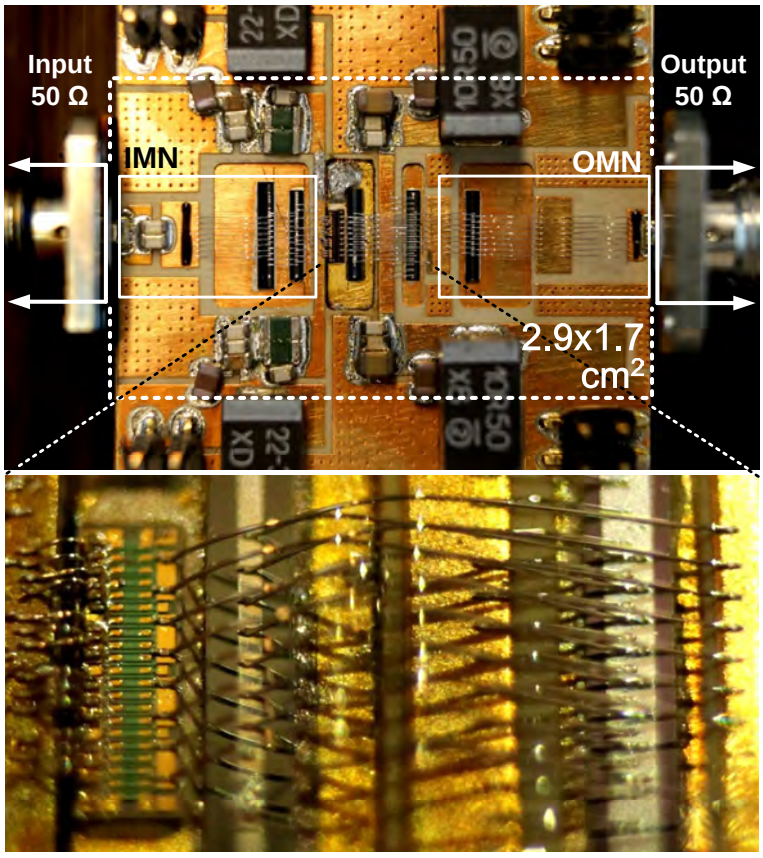


Figure 6.13: Photograph of the second implemented class-E power amplifier prototype.

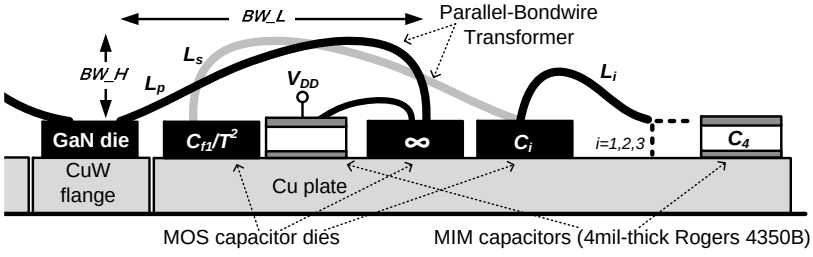


Figure 6.14: Cross-section of the second amplifier's output network (see schematic in Fig. 6.11).

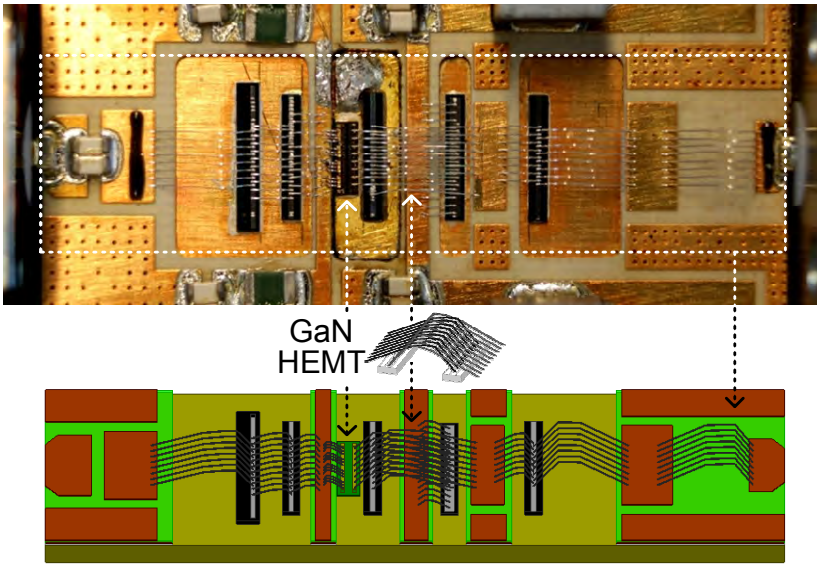


Figure 6.15: Close-up photograph and corresponding 3D EM model in HFSS of the second amplifier's RF section used for final design verification in Agilent ADS. A detail of the parallel-bondwire transformer is added for clarity.

verification of this amplifier along with a photograph of the corresponding RF section from the actual prototype.

6.4.3. POWER-SCALABLE PA IMPLEMENTATION

Due to the physical properties of the multi-wire parallel-bondwire transformer, the PA implementation is truly power-scalable. This can be explained as follows. To maintain class-E operation at different maximum output power levels (different sizes of the active die) the condition $q = 1/\omega\sqrt{L_E \cdot C_{out}}$ should remain constant [82] (refer to Subsection 3.3.2 for further details). Consequently, for a larger output power, the transistor die size will increase yielding increased C_{out} and having more drain contacts. When utilizing these additional drain contacts for more paralleled wires in the PBWT, the magnetizing inductance $L_p = L_E$ will be reduced. In order to keep q constant, the increase of C_{out} must be compensated for by a proportional reduction of L_E which can be fine-tuned by the PBWT's bondwires specific height and length. This is illustrated in Fig. 6.16 that shows that the product "$L_E \times C_{out}$" is roughly preserved for different transistor die sizes, maintaining the same class-E operation for different maximum output power levels. This assumes that distributed effects can be neglected, imposing certain practical limits on the maximum size of the transistor dies as well as maximum operating frequencies.

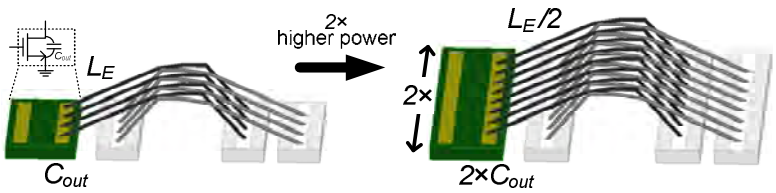


Figure 6.16: Illustration of the power-scalability feature of the second compact PA design. Observe that the product "$L_E \times C_{out}$" is preserved for different transistor die sizes, maintaining the same class-E operation for diferent maximum output power levels.

6.4.4. RF MEASUREMENT RESULTS

The measured results of the second implemented compact PA are shown in Fig. 6.17 for a supply voltage of 35 V. Also here, RF-pulsed measurements (10% duty-cycle, 100μsec) were performed for the characterization of this amplifier on the same in-house active load-pull system. At a power drive of 34.5 dBm, the transistor is about 3.5 dB in compression enforcing the transistor's switch-like behavior. From 1.75 to 2.60 GHz (39% bandwidth), the PA reaches an output power of 44 to 72 W (47.5±1.1 dBm), with a drain-efficiency and a *PAE* between 64 to 71% and 60 to 69%, respectively. In that band, the transducer power gain G_T remained at 12.9±1.1 dB. These results are summarized in Table 6.1 along with the previous PA design and other published GaN class-E PA designs operating above 1 GHz and with more than 5 W output power (listed in descending order with respect to the fractional bandwidth). It can be observed that this second PA has also a very favorable combination of output power, efficiency and form factor, along with a very large RF bandwidth.

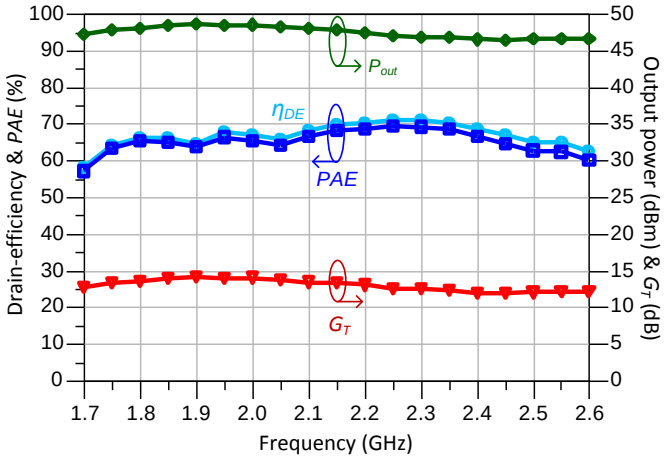


Figure 6.17: Measured RF performance of the wideband class-E PA prototype.

Table 6.1: COMPARISON BETWEEN GAN CLASS-E PAS ($f > 1$ GHZ AND $P_{out} > 5$ W).

Work	Bandwidth (GHz)	P_{out} (W)	η_{DE} (%)	PAE (%)
Design 1 (Section 6.3)	**1.70 - 2.30 (30%)**	**42 - 65**	**68 - 75**	**63 - 72**
Design 2 (Section 6.4)	**1.75 - 2.60 (39%)**	**44 - 72**	**64 - 71**	**60 - 69**
[124]	1.80 - 2.30 (24%)	3.2 - 5.2	57 - 63	52 - 57
[125]	2.00 - 2.50 (22%)	7 - 13	74 - 78	71 - 74
[121]	2.02 - 2.26 (11%)	74 - 112	69 - 76	65 - 71
[126]	2.06 - 2.24 (8%)	15 - 20	63 - 74	59 - 71

6.5. ANALYSIS OF BONDWIRE TOLERANCES

Manufacturing specific bondwire shapes using automatic bonding machines normally requires some practical experimentation because of the limited predictive simulation tools currently available for the wire bonding process [92]. However, once the proper settings of a given shape are determined, those shapes can be accurately reproduced by those automatic machines. Nevertheless, physical bondwire shape deviations lead to electrical inductance variations. Bondwire shape can slightly vary, for example, due to tolerances in die placement ($\triangle L$), in bondwire height ($\triangle H$) and in tip offset ($\triangle T$). These tolerances are illustrated in Fig. 6.18. Variations of up to 50μm in each of those tolerances are normal specifications and these can lead to inductance variations within about ± 10% on a regular sized bondwire. Therefore, the closer the realized shape is to the aimed one, the more accurate will be its electrical prediction through simulation. The actual impact of this electrical tolerance on the overall amplifier performance is strongly dependent on the Q of its matching networks. For this reason, low-Q matching networks in wideband designs relaxes to a great extend the impact of these variations.

The sensitivity of the two compact PA examples in this chapter with respect to bondwire inductance variations was reviewed by means of Monte Carlo simulations. For this, all the bondwire inductances in the nominal designs for those amplifiers were varied randomly within ±10% using a normal distribution. Each of the Monte Carlo simulated

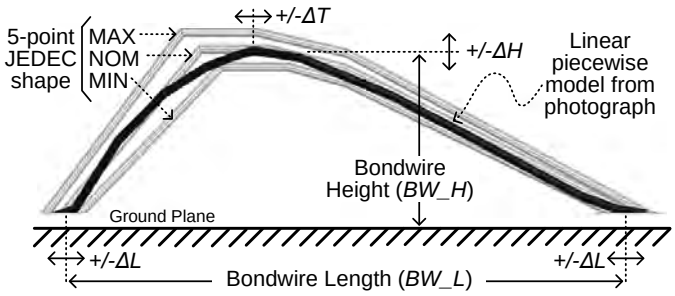
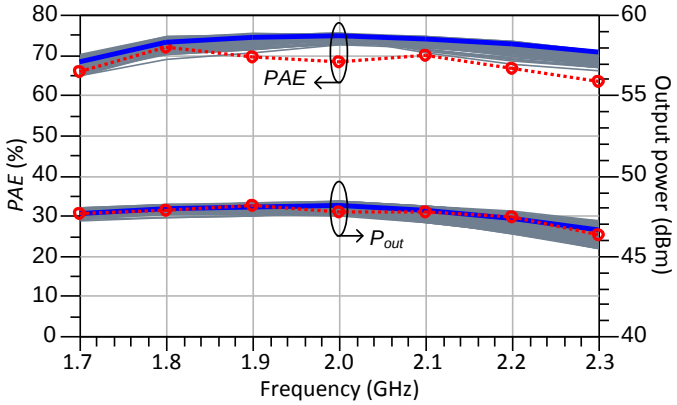
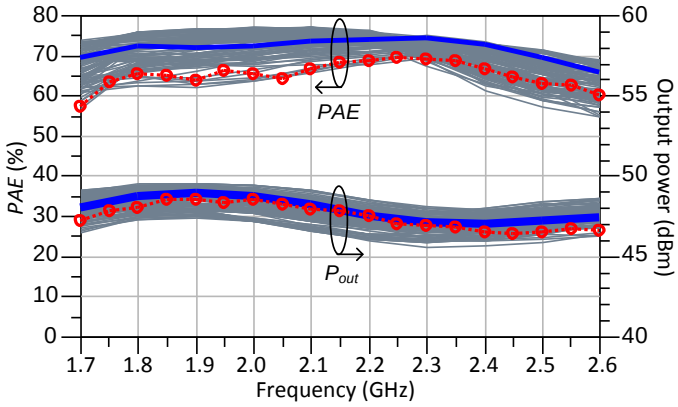


Figure 6.18: Impact in bondwire loop shape due to tolerances in die placement ($\triangle L$), bondwire height ($\triangle H$) and tip offset ($\triangle T$).

results are depicted with gray lines in Fig. 6.19 for efficiency and output power. The nominal results (i.e., without inductance variations) are given with a thick trace. Also, in the same figures, the actual measure performance is given with a dotted line. Good agreement can be observed between the expected (i.e. Monte Carlo simulations) and the measured performance, demonstrating the feasibility of design and the low expected spread of the wideband PA designs. Compared to the first PA design, the higher sensitivity for the second PA design, observed in Fig. 6.19b, is because the leakage inductance resulting from the limited transformer's coupling factor needs to be resonated out and this becomes less effective with spreading values for the rest of the circuit.



(a) Output power and *PAE* for the first RF PA described in **Section 6.3**.



(b) Output power and *PAE* the second RF PA described in **Section 6.4**.

Figure 6.19: Comparison between measured performance (dotted red), expected/nominal simulation (solid blue) and anticipated spread based on ±10% bondwire inductance tolerance (gray) for the two compact PA designs: a) the results for the first PA design in **Section 6.3**, and b) the results for the second PA design in **Section 6.4.**

6.6. CONCLUSIONS

The design approach for low-cost PAs using bondwire-based matching networks aimed for package integration has been discussed and demonstrated through the implementation of two compact >60 W GaN class-E PAs. These PAs used low-cost technologies normally found in packaged high-power transistors, such as bare transistor dies, bondwire-based structures and MIM/MOS pre-match capacitors. The resulting compact amplifier implementations were also targeted for broadband and efficient performance and each employed a different output network topology. The first design demonstrated that the frequency behavior of the optimum class-E load impedance can be controlled by tuning the DC feed inductance value. This yields flexibility to approximate the required behavior of the PA optimum load versus frequency with the one that can be provided by a practical matching network, such an *LC* ladder, providing accurate matching conditions for the fundamental and the harmonics over a wide frequency range. The second PA prototype was based on class-E with parallel-circuit loading and incorporated a very low-loss bondwire-based transformer along with a low Q_L filter. The use of the bondwire transformer in this second design was a needed exercise for the later introduced packaged-integrated outphasing PA of next chapter. In addition, the impact in PA performance due to practical bondwire loop shape tolerances (i.e. inductance spread) was evaluated. The encouraging results in terms of efficiency, bandwidth and size of the practical amplifier implementations on this chapter demonstrate the feasibility of low-cost fully package-integrated high-power amplifiers for wireless infrastructure applications.

7

PACKAGE-INTEGRATED CHIREIX OUTPHASING RF AMPLIFIER

7.1. INTRODUCTION

In the initial chapters of this thesis, the outphasing amplifier was described and it was shown that it can provide both high average efficiency and good linearity for large PAPR signals when designed appropriately. Also, in the former chapters practical design techniques were described that can lead to very compact amplifiers with improved performance compared to PCB-based implementations. In this chapter, these two aspects are brought together and the design of a state-of-the-art outphasing amplifier is thoroughly described. This amplifier, shown in Fig. 7.1, is in fact the first package-integrated implementation of a high-power Chireix outphasing RF amplifier that fairly competes with other state-of-the-art PAs, including Doherty and envelope tracking amplifiers, while having a very compact size. The basic Chireix outphasing concept was reviewed previously in Section 2.5 and in Section 2.3 it was described that higher efficiency at deep back-off can be obtained than previously expected when considering only the power factor of the combiner. This extra efficiency improvement can be obtained when using class-E for the branch amplifiers, as described previously in Section 3.5.2 and also in this chapter.

This chapter provides detailed design considerations and measurement results for the amplifier shown in Fig. 7.1. It starts by describing the broadband outphasing combiner and the specific class-E operation for the branch amplifiers. Then the design and implementation of the prototype demonstrator is discussed. Finally, static and dynamic RF measurement results are provided to validate the proposed amplifier.

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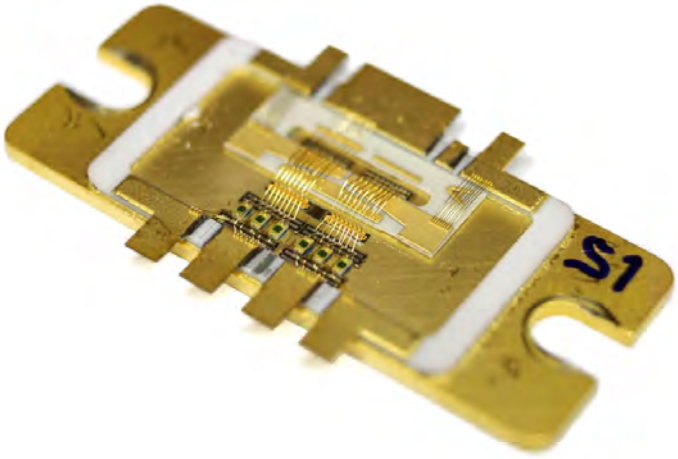


Figure 7.1: Photograph of the package-integrated Chireix outphasing RF high-power amplifier prototype.

7.2. BROADBAND OUTPHASING SWITCH-MODE AMPLIFIER

The efficiency of the outphasing amplifier depends on both its power-combining network and its branch amplifiers (including their specific driving profiles). Regarding the power combiner, most of the previous work has mainly focused on implementing such combiner with transmission lines [40, 51–53], where the usual Chireix compensation elements were either lumped or incorporated in the combiner [40, 52]. However, this approach is restricted in bandwidth due to the transmission line-based combiner itself [54], although such implementation is not fundamental to the original concept. More recent work has focused on transformer-based combiners [28, 30, 54–56, 65] and has reported in fact larger RF bandwidths, especially at deep back-off power levels [28, 65]. When considering the operating class of the branch amplifiers, switch-mode amplifiers (SMPA) have become more broadly used in outphasing amplifiers; such as voltage-mode class-D [30, 55] and class-E [28, 40, 49, 54, 56, 65]. For high-power, class-E has been identified as a good candidate for the branch PAs, demonstrating high efficiency over a wide dynamic range [40] and even broadband digital CMOS circuitry has been introduced for driving GaN HEMTs for the SMPAs directly [28, 75].

7.2.1. BROADBAND OUTPHASING COMBINER

Due to the bandwidth restriction imposed by (quarter-wavelength) transmission line-based power combiners [54], a wideband outphasing transmitter preferably delivers its power into a broadband floating load or, equivalently, to a transformer-based combiner, as shown in Fig. 7.2. In this case, as described earlier in Section 2.5, the branch amplifiers are considered as ideal voltage sources $\mathbf{V_{1,2}}$ and the *dynamic* (time-dependent)

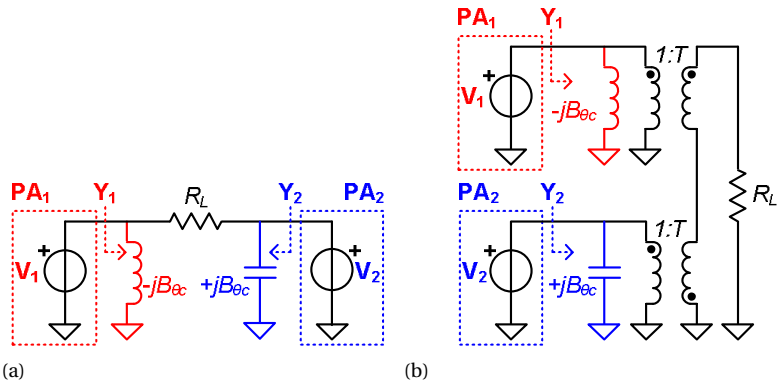


Figure 7.2: Principle of wideband Chireix combiner: a) with a floating load, b) with a transformer-based combiner.

admittance seen by each of those sources is given by

$$\mathbf{Y_{1,2}}(\theta(t)) = G(\theta(t)) \pm j\left[B(\theta(t)) - B_{\theta c1,2}\right] \tag{7.1}$$

in which

$$G(\theta(t)) = \left(\frac{1}{R_{PA}}\right)\sin^2(\theta(t)) \tag{7.2}$$

$$B(\theta(t)) = \left(\frac{1}{R_{PA}}\right)\frac{\sin(2\cdot\theta(t))}{2} \tag{7.3}$$

$$B_{\theta c1,2} = B\left(\theta_{c1,2}\right) \tag{7.4}$$

where $\theta(t)$ is the *dynamic* outphasing angle, R_{PA} is the load seen by each amplifier at full power (i.e., when $\theta(t) = \frac{\pi}{2}$), $\theta_{c1,2}$ and $B_{\theta c1,2}$ are the Chireix compensating angles and susceptances for branch 1 and 2, respectively. For the combiners in Fig. 7.2a and Fig. 7.2b, $R_{PA} = \frac{R_L}{2}$ and $R_{PA} = \left(\frac{1}{T^2}\right)\frac{R_L}{2}$, respectively, where T is the transformer's turns ratio.

The Chireix compensation elements $B_{\theta c}$ minimize the effects of the unwanted dynamic reactive load-modulation in (7.3) seen by each branch amplifier due to the outphasing mechanism. At certain back-off power levels, or equivalently "outphasing angles", $B_{\theta c}$ nulls $B(\theta(t))$ in (7.1) and thus the power factor (PF) increases. This is illustrated in Fig. 7.3 by showing the PF versus back-off power of the combiners in Fig. 7.2 for three cases: a) without Chireix compensation, and with compensation at 10 dB back-off power (i.e., at an angle of about 18.4°) at b) 1× and c) 1.2× the design frequency ω_0. In the figure, it can be observed that this Chireix combiner is indeed broadband because of the high PF over a large fractional bandwidth. Furthermore, Fig. 7.4 depicts the ideal load-$\Gamma\left(1/\mathbf{Y_{1,2}}\right)$ loci seen by each of the outphasing branch amplifiers for the same conditions used in Fig. 7.3. Note that each $\Gamma\left(1/\mathbf{Y_{1,2}}\right)$-locus rotates clock-wise with increasing frequency but only a little, indicating a small affectation on the efficiency over that bandwidth.

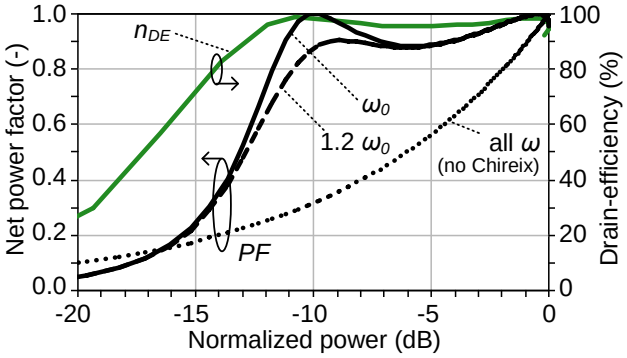


Figure 7.3: Net power factor of the broadband outphasing combiner (without Chireix compensation, and with compensation at 10 dB back-off power at 1× and 1.2× the design frequency) (left axis) and drain-efficiency of an outphasing amplifier using the ideal "load-insensitive" class-E SMPAs described in this chapter (right axis).

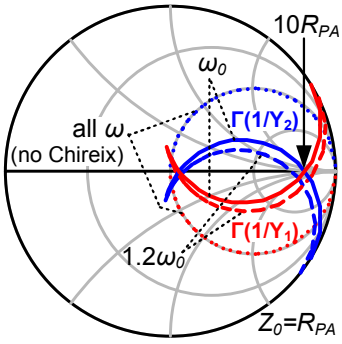


Figure 7.4: Load-$\Gamma\left(1/\mathbf{Y_{1,2}}\right)$ loci seen by each branch PA with the broadband outphasing combiner (without Chireix compensation, and with compensation at 10 dB back-off power at 1× and 1.2× the design frequency ω_0).

In addition, Fig. 7.3 depicts on the right axis the ideal η_{DE} for the class-E outphasing SMPA described in this chapter. Observe that such η_{DE} is higher than the PF of the power combiner itself, especially after 10 dB back-off where the efficiency has a softer roll-off. This higher efficiency at deep back-off will result in a significantly higher *average* efficiency for signals with high PAPR. As explained earlier in Section 2.3, the η_{DE} in this case is higher than the PF because the "apparent efficiency" $\eta_{S,\text{class E}}$ of the class-E branch amplifiers enhances it. This is, $\eta_{S,\text{class E}}$ varies during the outphasing load excursion and $\eta_{S,\text{class E}} \approx 1$ at 0 dB while $\eta_{S,\text{class E}} > 1$ at deeper back-off levels (e.g., after 10 dB).

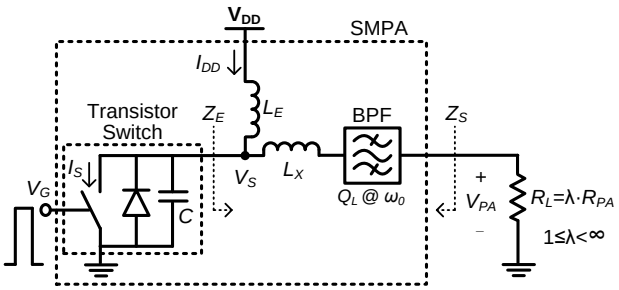


Figure 7.5: Generic class-E PA schematic with load modulation. R_{PA} is the nominal load (i.e., it is fixed) and λ is the outphasing load-modulation factor.

7.2.2. LOAD-INSENSITIVE SMPAS FOR OUTPHASING

The optimum branch amplifiers for outphasing must be able to handle the high dynamic load modulation depicted in Fig. 7.4 without compromising its performance, i.e. they should be "load-insensitive". In other words, the $\Gamma\left(1/\mathbf{Y_{1,2}}\right)$-locus in Fig. 7.4 should be located inside the high efficiency operating regions of the branch amplifiers. Class-E SMPAs are excellent candidates for this task [28, 40, 56] and can be even made wideband [87, 119, 127]. Although it is theoretically possible to achieve good performance over very large back-off power levels by adding tunable elements to the SMPA [56], it is not trivial to handle the increased complexity in high-power applications. Therefore, it is more appealing to make the SMPAs load-insensitive by design without the need for those extra tunable elements, as in [28, 65] and described here.

The "load-insensitive" class-E suitable for outphasing can be described using the generic schematic in Fig. 7.5, which assumes that the active device is an ideal switch. For the sake of simplicity, the load of this SMPA in an outphasing amplifier will be assumed to be ohmic and to change according to $R_L = \lambda \cdot R_{PA}$ for $1 \leq \lambda < \infty$. λ is the outphasing load-modulation factor and can be defined in terms of the normalized resistance seen by the branch amplifiers as $\lambda = \mathbf{Re}\left\{\frac{1}{Y_{1,2}}\right\}/R_{PA}$. As required for class-E, the bandpass filter (BPF) opens the higher harmonics and here is modeled as a series LC-filter whose Q_L is defined for the nominal R_{PA}. As explained earlier in Subsection 3.3.2, the fundamental load in the output load network in Fig. 7.5 can be designed arbitrarily for different class-E types according to the design parameter "$q = \frac{1}{\omega\sqrt{L_E \cdot C_E}}$" [82].

A well-known example is the classical "RF-choke" class-E PA [79, 81], which corresponds to the case when $q = 0$ that is characterized for having an RF choke and therefore $Z_{E_{choke}} = R_{PA} + j\omega L_X$ (since $L_E = \infty$ for $q = 0$). Another example is the "parallel-circuit" class-E PA [86], which results when $q \approx 1.4$ and uses a finite inductor in shunt with the output capacitance and hence $Z_{E_{parallel}} = R_{PA} || j\omega L_E$ (since $L_X = 0$ for $q \approx 1.4$). The specific case of the "load-insensitive" class-E PA happens when $q \approx 1.3$ [28]. Although L_X is non-zero in this specific case, in practical situations it can be neglected with minimum detriment on performance and therefore the load network $Z_{E_{insensitive}} \approx R_{PA} || j\omega L_E$ resembles the one of the "parallel-circuit" and shares similar broadband characteristics.

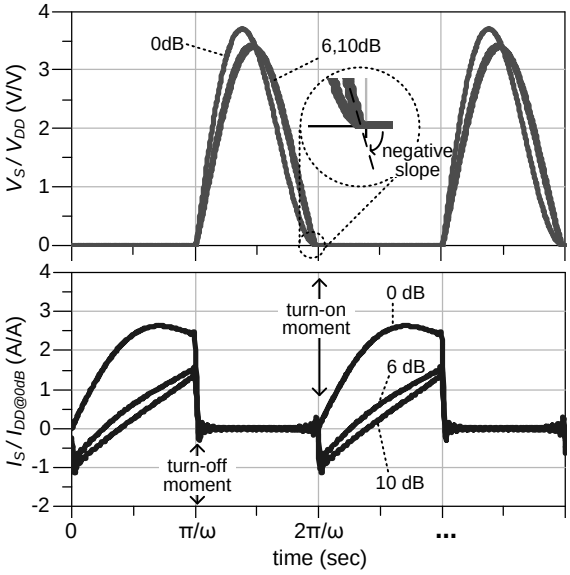
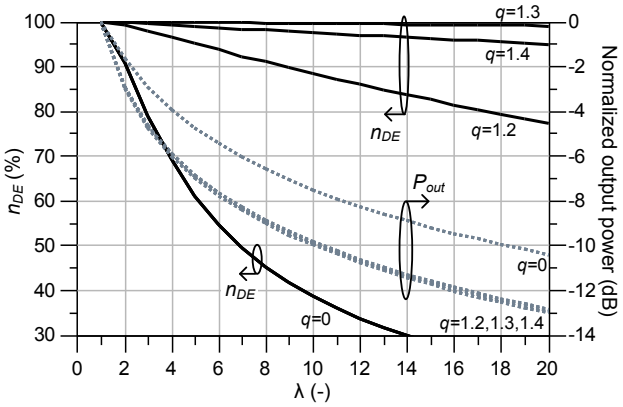
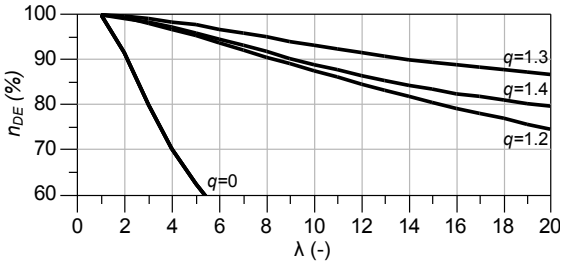


Figure 7.6: Simulated (and normalized) voltage and current waveforms at the intrinsic switch of the load-insensitive class-E SMPA (Q_L = 10) at 0, 6, and 10 dB back-off power (i.e., λ=1, 4, and 10, respectively).

The unique property of this "load-insensitive" SMPA is that even when its load resistance changes from its nominal (λ = 1) to a much higher value ($\lambda \gg 1$), it responds by changing its turn-on voltage-slope from zero to a negative value while still keeping its turn-on voltage close to zero (i.e., it enters into variable-slope operation [84]). This variable-slope operation can be seen in Fig. 7.6, which depicts the simulated and normalized voltage and current waveforms at the intrinsic switch for 0, 6, and 10 dB back-off power levels (or, equivalently from Fig. 7.5, for λ = 1, 4, and 10, respectively). Observe that at the turn-on moment, the voltage waveform indeed has more negative slope for increased back-off levels while maintaining its value close to zero and because of this, it causes no switching losses. Meanwhile, the peak current through the switch reduces with back-off at the same turn-on moment. Therefore, due to the resulting non-overlapping voltage and current waveforms, the efficiency will be preserved even for the varying load conditions that occur in an outphasing amplifier. This can also be concluded by analyzing the simulated drain-efficiency of these different SMPAs as a function of λ, as illustrated in Fig. 7.7. Observe from Fig. 7.7a that the load-insensitive SMPA ($q \approx 1.3$) indeed maintains its high efficiency for higher values of λ (i.e., deeper back-off power levels) compared to the other class-E amplifier implementations using different q values. Notice, however, that a side effect of an increasing λ is the reduction of the nominal Q_L of the filter, which will affect the PA performance at back-off due to lower harmonics-rejection. This can be seen when comparing Figs. 7.7a and 7.7b, which correspond to a very large (and unrealistic) value of nominal Q_L = 1000 and nominal Q_L = 10, respectively. Therefore, the BPF must be simultaneously optimized for bandwidth and high harmonics-rejection in order to maintain high efficiency and broadband



(a) with $Q_L = 1000$



(b) with $Q_L = 10$

Figure 7.7: Simulated drain-efficiency and normalized output power versus load-modulation factor λ for several class-E SMPAs with a) very large (unrealistic), and b) large values of nominal Q_L for the BPF.

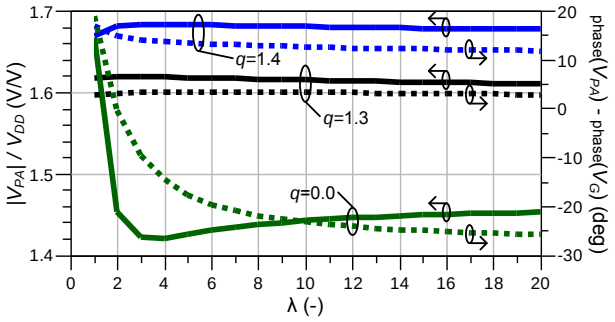


Figure 7.8: Simulated SMPA's output voltage waveform (V_{PA}) versus load-modulation factor λ for several class-E SMPAs ($Q_L = 10$).

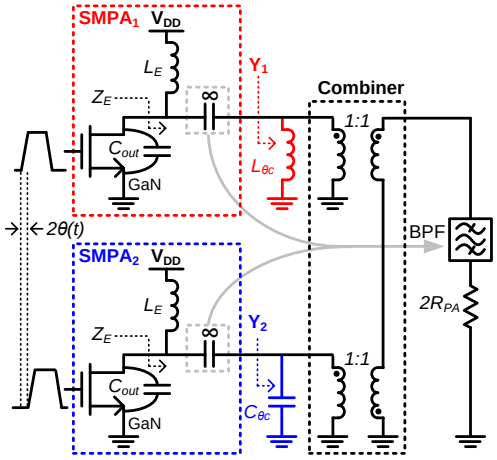


Figure 7.9: Simplified circuit schematic of the proposed outphasing SMPA used for system simulation.

performance.

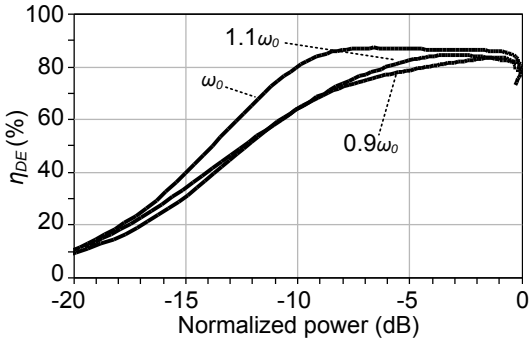
In addition, the load-insensitive SMPA can be effectively regarded as a voltage source, as required by the outphasing concept in Fig. 7.2. This can be appreciated in Fig. 7.8, which shows both magnitude and phase of the output voltage waveform V_{PA} (refer to Fig. 7.5) as a function of λ for the previous SMPAs. Notice that V_{PA} (in both magnitude and phase) hardly changes with λ when $q = 1.3$, and thus the load-insensitive SMPA's behavior approximates an "ideal" voltage source (i.e., its $Z_S \ll \frac{1}{\mathbf{Y_{1,2}}}$ in Fig. 7.5, where Z_S is the SMPA's output impedance).

7

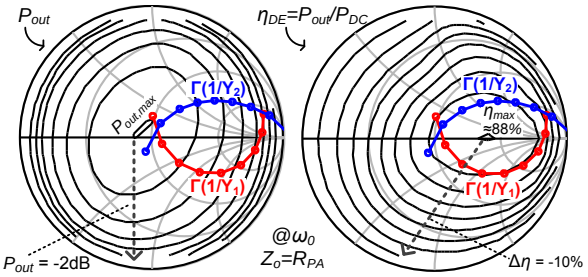
7.2.3. OUTPHASING SMPA SYSTEM PERFORMANCE

Fig. 7.9 depicts the simplified circuit schematic of the proposed outphasing amplifier using the broadband power combiner and the branch SMPAs described previously. Notice that a single BPF prior to the final load provides the high harmonics open termination required by each of the two branch SMPAs. The system simulation results are shown in Fig. 7.10. They include the large-signal model for the transistors used in the final demonstrator of this work and assume lossless passive components. Including the active device model helps to optimize simultaneously the specific branch amplifier class (i.e. L_E and R_{PA}, as discussed in Subsection 7.2.2), the Chireix compensating components ($L_{\theta c}$ and $C_{\theta c}$) and the BPF in order to maximize efficiency and bandwidth at both peak and back-off power levels.

The transistors employed are GaN HEMT with 0.25 μm gate length and 9.6 mm gate width from NXP Semiconductors. These devices have an f_T of 28 GHz and an off-state breakdown voltage higher than 150 V. For the simulation, the driving was considered quasi-ideal (i.e. square wave with sufficient swing and finite rising/falling times, e.g. 5 V and 20%, respectively). Fig. 7.10a shows the simulated drain-efficiency at 1.8-2.2 GHz.



(a)



(b)

Figure 7.10: Simulation results for the proposed outphasing SMPA using a large-signal transistor model and ideal passive components: a) η_{DE} versus normalized output power over 20% relative bandwidth, and b) the load-$\Gamma\left(1/\mathbf{Y_{1,2}}\right)$ of the branch amplifiers super-imposed with simulated single-transistor load-pull curves for normalized output power and η_{DE} at the central frequency ω_0.

Observe that under these idealized conditions, the PA can maintain $\eta_{DE} > 80\%$ for 10 dB back-off at 2 GHz with a relative bandwidth up to 20% (maintaining $\eta_{DE} > 60\%$). For further visualization purposes, Fig. 7.10b illustrates the dynamic load-$\Gamma\left(1/\mathbf{Y_{1,2}}\right)$ loci seen by the branch amplifiers super-imposed on the same Smith Chart of simulated load-pull contour curves for the (normalized) output power and the η_{DE} of a single transistor amplifier. Observe that the load-insensitive SMPA effectively matches these $\Gamma\left(1/\mathbf{Y_{1,2}}\right)$ loci with the high performance regions of the individual transistor amplifiers.

7.3. OUTPHASING SMPA DEMONSTRATOR

A very compact and high-power prototype was designed to demonstrate the proposed outphasing SMPA concept [65]. The core of this demonstrator was implemented inside a standard CuW-flanged ceramic transistor package with customized leads, refer to Fig. 7.1 for a photograph. Only the bandpass filter was placed externally on a PCB. As discussed earlier, package-integration is an appealing approach to achieve improved

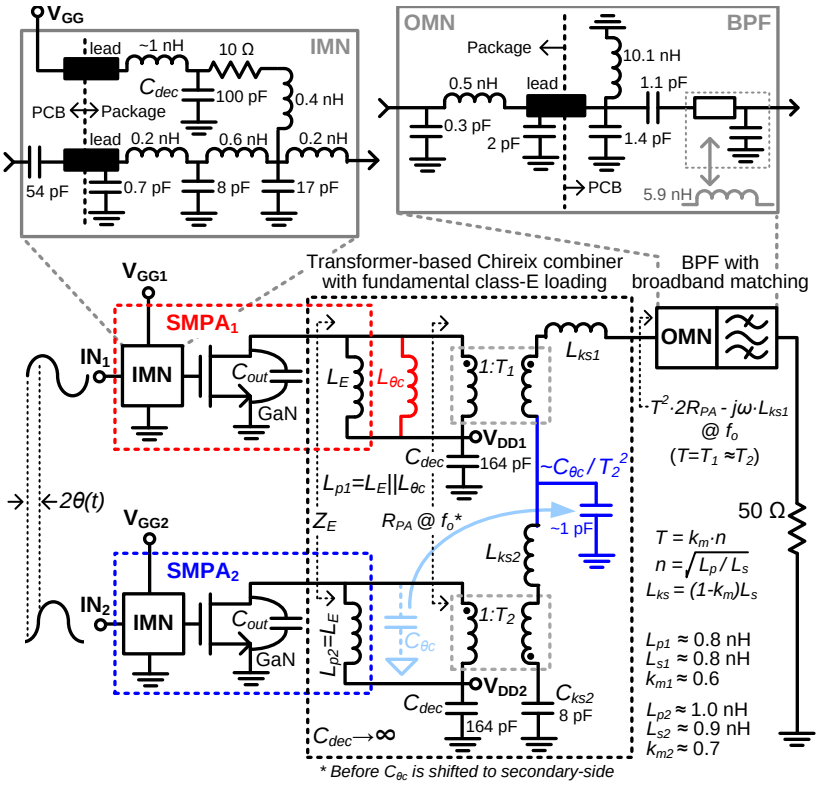


Figure 7.11: Detailed schematic of the proposed outphasing SMPA. The Chireix combiner comprises two lumped transformers (whose model is depicted for clarity).

RF performance in terms of bandwidth and efficiency, as well as lower memory effects, form-factor and cost [128]. The complete circuit schematic of this demonstrator is depicted in Fig. 7.11. The core of the amplifier comprises two SMPAs (as described in Subsection 7.2.2), a transformer-based power combiner with Chireix compensation and an output matching-network (OMN). For good heat dissipation, the PA was placed on a gold-plated 8 mm-thick copper block mounted on an aluminum heat sink, see Fig. 7.13.

7.3.1. TRANSFORMER-BASED CHIREIX COMBINER

The key component in this package-integrated outphasing SMPA is the wideband power combiner, whose detailed schematic is depicted in the center of Fig. 7.11. This combiner is constructed with two lumped transformers interconnected at their secondary side. Each of these RF transformers is a bondwire transformer [118], as described in Section 5.4 and Section 5.5, made up of parallel bondwires that directly connect to the transistor dies of the two SMPA branch amplifiers. The transformers can offer high mag-

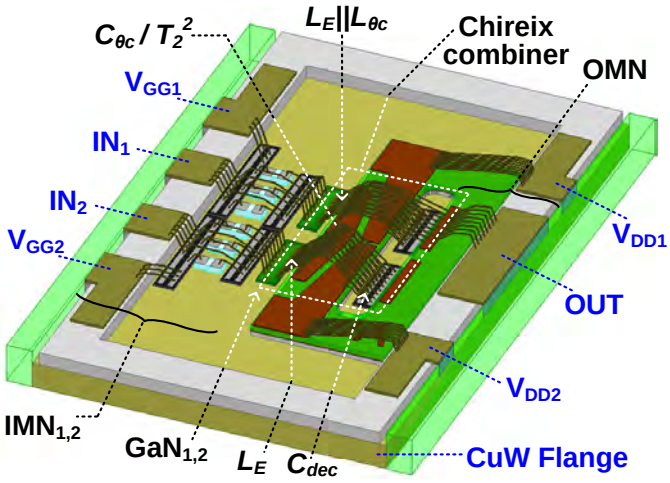


Figure 7.12: 3D EM model of the outphasing SMPA core (in-package section) used for design verification.

netic coupling (e.g. 0.7) and thus have a relatively low leakage inductance L_{ks}. In Fig. 7.11, any remaining leakage inductance is either absorbed by the broadband OMN or broadband-tuned by a capacitor C_{ks2}. In the combiner, the transformers' own magnetizing inductances L_p are used to implement the finite DC-feed inductance L_E required by the specific design of the branch SMPAs.

The Chireix compensating elements $L_{\theta c}$ and $C_{\theta c}$ are also incorporated in the combiner since they can be placed, after proper impedance scaling, at either side of each transformer. The Chireix element $L_{\theta c}$ is placed in parallel with L_E, and hence both elements are implemented together by the L_p of the transformer in the SMPA_1 branch. The Chireix element $C_{\theta c}$ is conveniently located at the secondary side of the transformer in the SMPA_2 branch, truly enabling a direct connection between the transistor's drain and that transformer.

Additionally, the combiner allows to integrate the drain-bias decoupling capacitance, C_{dec} in Fig. 7.11, inside the transistor package. This large capacitance creates an AC-short at the primary side of the transformers where the drain supply is connected to, right next to the active devices. This helps in minimizing memory effects associated with the biasing and thus improving the linearizability of the entire amplifier.

7.3.2. PA DESIGN AND IMPLEMENTATION

The components employed inside the package are: NXP Semiconductors' GaN HEMT bare dies with 0.25 μm gate length and 9.6 mm gate width, 50 μm-thick low- and high-density metal-insulator-metal silicon capacitor dies, 50μm-diameter gold bondwires, bondable 0402 chip resistors and a miniature double-sided PCB with 200 μm-thick Rogers 4003C substrate. The two bondwire transformers of the Chireix combiner are intercon-

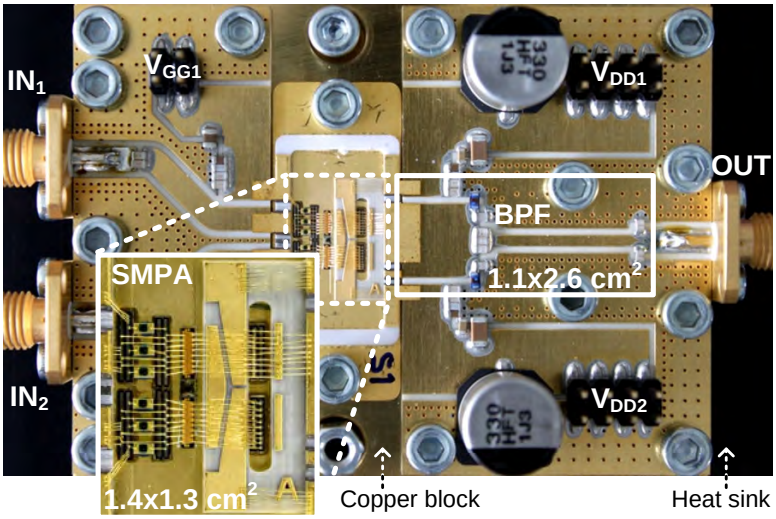


Figure 7.13: Photograph of the test board with the package-integrated Chireix outphasing SMPA (see inset). The total effective size is 4.7 cm^2.

nected on their secondary side by a track on this miniature PCB, whose capacitance to ground implements the impedance-scaled $C_{\theta c}$ (see Figs. 7.11 and 7.12). All the RF inductors and transformers were made using bondwires whose shape was carefully designed with the aid of a full wave 3D electromagnetic solver (Ansoft HFSS) and implemented by an automated bonding machine, as described in Subsection 7.2.2. The 50Ω output and input matching networks (IMN) were implemented as *LC*-ladder networks. The two identical 3-stage *LC*-ladder IMNs connect to the input package leads and contain stabilizing resistors for extra precaution, see Fig. 7.11. The OMN is a single-stage *LC*-ladder that connects to the output package lead, see also Fig. 7.11.

Due to space constraints, the BPF was implemented outside the package. This filter was simultaneously optimized for maximum bandwidth and high harmonics-rejection with minimum complexity. This resulted in a 2^{nd} order Butterworth BPF, implemented as a shunt *LC*-tank followed by a series *LC*-tank. To absorb all undesired parasitic elements, this filter was implemented with high-quality SMD components and a transmission line, as shown in Fig. 7.11.

The entire PA design was verified by comprehensible co-simulations using circuit and EM simulators, that included both the in-package and the PCB sections, and incorporated all relevant component models: a 3D EM model for the in-package section, large signal model for the transistors, and models for the rest of the passive components (including measurement-based and substrate-dependent models for the SMDs [129]). Fig. 7.12 depicts the final 3D EM model of the amplifier's core, while Fig. 7.13 shows the photograph of the complete demonstrator. The total effective size of the prototype is only 4.7 cm^2: 1.3×1.4 cm^2 for the in-package section (the core of the SMPA) plus 1.1×2.6 cm^2 of the BPF in the PCB.

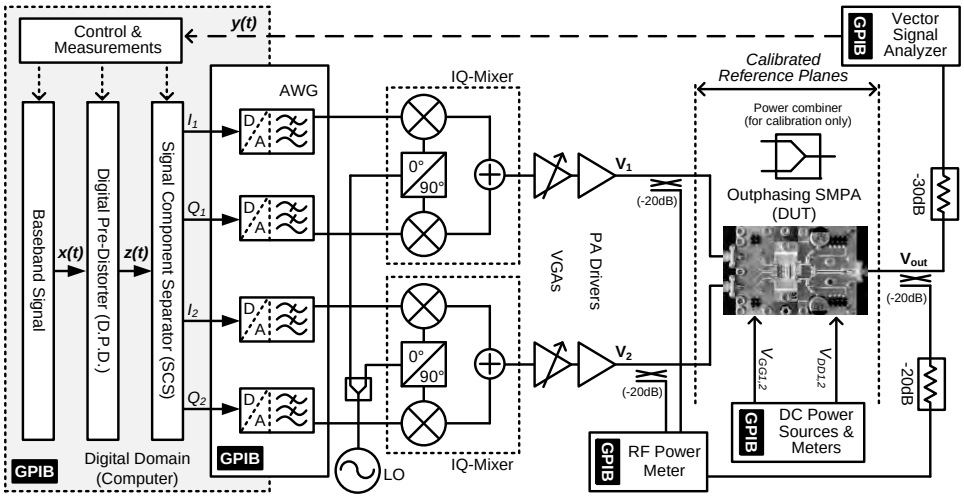


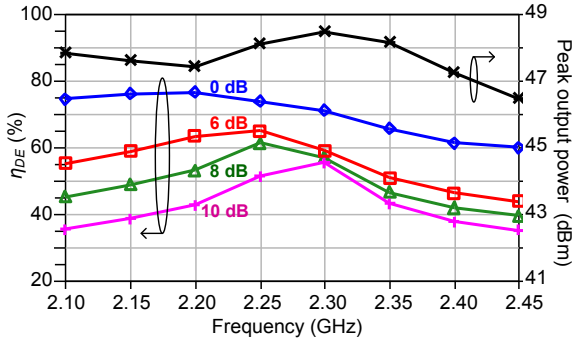
Figure 7.14: Dedicated measurement setup for the outphasing SMPA demonstrator.

7.4. EXPERIMENTAL RESULTS

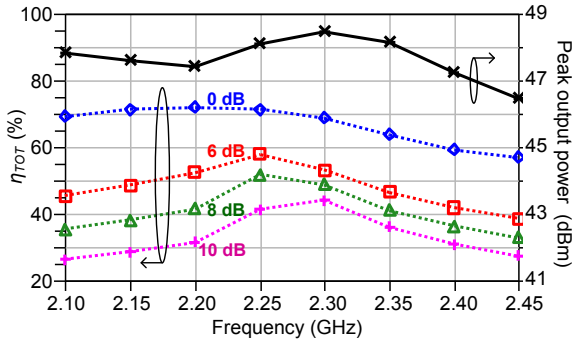
7.4.1. MEASUREMENT SETUP AND CALIBRATION

The prototype outphasing SMPA was characterized using a dedicated measurement setup developed by NXP Semiconductors, whose block diagram is illustrated in Fig. 7.14. The baseband processing is implemented in a PC where all the instruments are controlled and the measured data is captured and processed. The baseband (and also calibration) test signals are generated using a Tektronix's AWG5014 arbitrary waveform generator and fed to two IQ modulators, followed by additional variable-gain (VGA) and driver amplifiers. The output of the outphasing SMPA, or device under test (DUT), is fed to an R&S FSQ-26 signal analyzer (with high speed baseband option B72) that down-converts and samples the RF signal for digital predistortion and performs the linearity measurements. All RF inputs and output of the DUT are coupled to RF power meters in order to compute absolute power, efficiency and gain.

The entire setup is calibrated in two steps, for which a power combiner (see Fig. 7.14) is connected instead of the actual DUT. First, each IQ mixer is independently calibrated digitally to compensate for LO leakage and IQ phase and gain imbalance. In the second step, the two signal branches (i.e., the cascade of IQ-mixer, VGA and pre-amplifier in each branch) are calibrated with respect to each other in amplitude (AM) and phase (PM). Here, the two IQ mixers deliver equal-amplitude but out-of-phase signals such that, after combination, will null each other (-60 dBc or better) in the absence of any imbalance. Digital compensation is used for fine AM and PM adjustments. Once the measurement setup is AM- and PM-calibrated, the outphasing SMPA is connected and



(a)



(b)

Figure 7.15: Measured peak P_{out} and a) η_{DE}, b) η_{TOT} at different power back-off levels (0 to 10 dB) as a function of frequency with V_{DD} = 28 V.

a finer calibration is performed to compensate for the DUT's own AM/PM imbalances.

7.4.2. STATIC CHARACTERIZATION: SINGLE-TONE

The outphasing SMPA demonstrator was first evaluated by sweeping a single-tone CW from 2.10 to 2.45 GHz. The GaN switches were biased close to threshold (-2.3 V), and their input powers ($P_{in1,2}$) were fixed to 32 dBm. At each frequency, the outphasing angle was swept in order to modulate the output power. The drain-efficiency ($\eta_{DE} = \frac{P_{out}}{P_{DC}}$) was calculated as the output power at the module's 50Ω connector interface (P_{out}) divided by the total DC power supplied to the drains of the GaN transistors (P_{DC}). The total-efficiency ($\eta_{TOT} = \frac{P_{out}}{P_{DC}+P_{dr}}$) also included the total RF input power delivered to the two inputs of the DUT ($P_{dr} = P_{in1} + P_{in2}$). Fig. 7.15 shows the measured peak-output power, η_{DE} and η_{TOT} versus frequency and output power back-off with a nominal 28 V drain-supply. Excellent wideband performance is observed from 2.1-2.4 GHz, with P_{out}= 47.9±0.6 dBm (peak at 48.5 dBm) and η_{DE} > 50% across >260 MHz, >160 MHz and >80

MHz at 6, 8 and 10 dB back-off, respectively.

Measurements were also performed at 20 V drain-supply, and Fig. 7.16 shows and compares them with the nominal 28 V supply. Note that at 20 V the efficiency performance is excellent, but suffers a little at the desired 28 V due to practical implementation challenges encountered for this first prototype (e.g. higher deviations than expected in some bondwire shapes). Table 7.1 highlights some of these results which demonstrate the high potential of the proposed amplifier. The highest peak power and best deep back-off efficiency was achieved at 2.3 GHz and the nominal 28 V. For these conditions, Fig. 7.17 shows η_{DE}, η_{TOT} and the total operating power gain ($G_{TOT} = \frac{P_{out}}{P_{dr}}$) as a function of back-off power. G_{TOT} peaks at 13.2 dB and reduces linearly with back-off power since the driving power is constant.

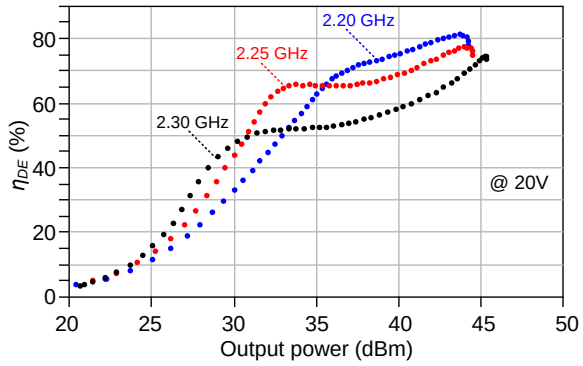
Table 7.1: HIGHLIGHTS OF MEASURED EFFICIENCY AT 20 AND 28 V SUPPLY.

DC supply	**Peak η_{DE}**	**Back-off range with $\eta_{DE} > 60\%$**
20 V	81% @ 2.20 GHz	12.5 dB @ 2.25 GHz
28 V	79% @ 2.20 GHz	8.1 dB @ 2.25 GHz

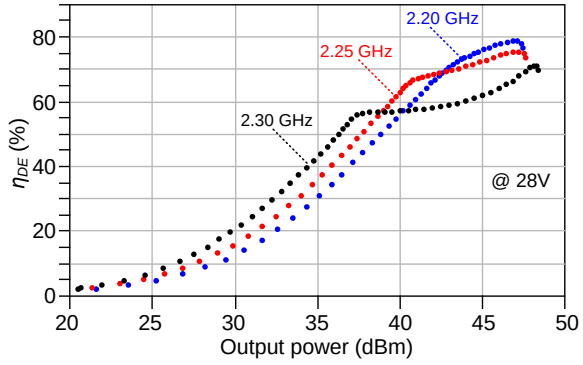
7.4.3. DYNAMIC CHARACTERIZATION: W-CDMA SIGNAL

The outphasing SMPA was characterized dynamically using a single-carrier 9.6 dB PAPR W-CDMA signal, whose PDF is shown in Fig. 7.17. It was linearized using an NXP's custom memoryless digital predistortion (DPD). Fig. 7.18 illustrates a simplified block diagram representing the DPD process, where $z(t)$ and $y(t)$ are the transmitter's baseband input and output signals, respectively (i.e., before up-conversion by the mixers and after down-conversion by the signal analyzer), and $x(t)$ is the original W-CDMA test signal. At first, $y(t)$ is captured without any DPD (i.e., $z(t) = x(t)$) over several signal periods and is averaged to reduce the system's noise contribution. Next, $y(t)$ and $x(t)$ are time-aligned using a circular correlation (for coarse alignment) followed by a linear sub-sample sweep (for fine alignment). A multiple-segment low-order polynomial AM-AM and AM-PM fitting process is used to model the inverse PA characteristics. It usually requires 5-7 segments of 3^{rd} or 4^{th} order polynomials. This approach can accurately model the PA's inverse characteristics without over-fitting which would occur with a single-segment high-order curve fit. Then, the DPD predistorts $x(t)$ and generates $z(t)$, which finally leads to an improved and more linear $y(t)$. This memoryless DPD was developed and optimized for outphasing amplifiers and provides optimum linearization even when bench-marked against Volterra DPD-based solutions.

Since this DPD is single-input/single-output, it is in fact linearizing the entire transmitter, i.e. including the (baseband) signal component separator. In principle, the signal component separator generates the signals of the two branches with a differential phase that is ideally an arc-sine function of the amplitude of the original signal (i.e. $\theta(t) = \sin^{-1}|E(t)|$ in Fig. 2.1). However, in practice this phase modulation function will



(a)



(b)

Figure 7.16: Measured η_{DE} versus P_{out} across frequency at a) V_{DD} = 20 V and b) V_{DD} = 28 V, between 2.2 and 2.3 GHz.

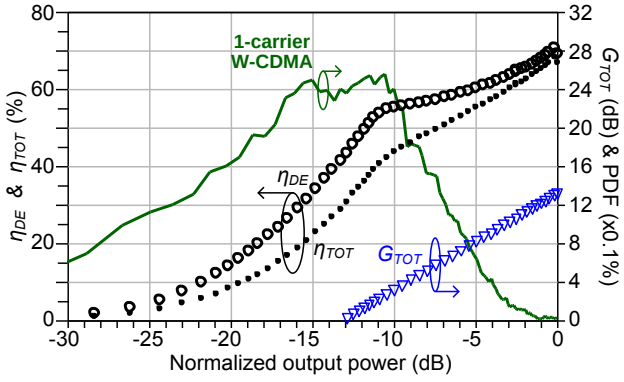


Figure 7.17: Measured G_{TOT} (blue triangles), η_{DE} (black circles) and η_{TOT} (black dots) as a function of back-off power at 2.30 GHz and V_{DD} = 28 V. Also, the PDF of a single-carrier W-CDMA is shown.

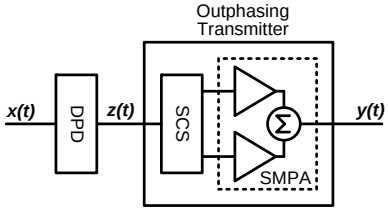


Figure 7.18: Simplified block diagram for the single-input/single-output memoryless DPD.

Table 7.2: COMPARISON STATE-OF-THE-ART GAN RF PAS.

W-CDMA PAPR (dB)	$P_{out,max}$ **(W)**	$\eta_{DE,av}$ **(%)**	$\eta_{TOT,av}$ **(%)**	**ACLR 1,2 (dBc)**	f_o **(GHz)**	$BW_{6dB,60\%}$ ** **(MHz)**	**Reference**
9.6	**70.6**	**53.5**	**43.8**	**-49, -56**	**2.30**	**> 100**	**This Work**
9.6	19	54.5	41.9	-47, -52	1.95	> 250	[12]
7.7	>150	73.1#1	51.7#2	<-45, <-50	2.14	N.R.	[10]
9.6	90	50.5	~47*	-47, -51	2.14	N.R.	[17]
11.5	100	55.0	53.0*	-51, -53	2.14	N.R.	[6]

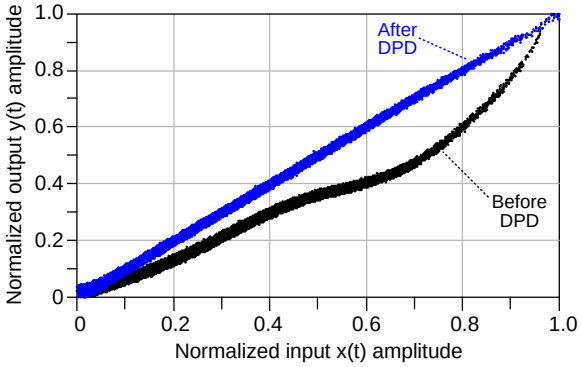
* PAE_{av} is given. #1Without and #2with (i.e. $\eta_{ET,av}$) DC-DC modulator.

** $BW_{6dB,60\%}$ is the bandwidth at 6dB output back-off power with drain-efficiency larger than 60% (N.R. = not reported).

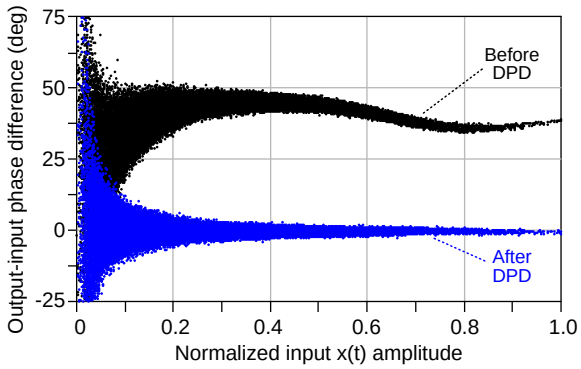
not match perfectly the real behavior of the amplifier, as discussed in Section 3.5.2, and will introduce distortion [16]. Therefore, applying the DPD before the SCS will compensate for this mismatch as well. Fig. 7.19 shows the measured AM-AM and AM-PM responses of the SMPA before and after DPD, while Fig. 7.20 shows the spectrum in both cases where the linearity improvement can be observed.

The adjacent and alternate channel leakage ratios (ACLR 1,2) were measured by the signal analyzer, as shown in Fig. 7.21, resulting in -49 and -56 dBc, respectively, meeting the stringent 3GPP linearity specifications [15] despite the use of a memoryless DPD. The measured average drain- and total-efficiency of the outphasing SMPA was 53.5% and 43.8%, respectively, with the 9.6 dB W-CDMA signal. Table 7.2 summarizes the main measured parameters for this outphasing SMPA and compares them with other published state-of-the-art GaN RF power amplifiers, including Doherty and envelope tracking PAs. Overall, the results of the proposed PA compare very favorably with the state-of-the-art but now with a much higher level of integration.

To the authors' best knowledge, this amplifier has the smallest form-factor ever reported of its kind and is the first package-integrated outphasing RF high-power amplifier. For a highly repeatable construction, it requires good control in both die placement and bondwire shapes, making automated die and wire bonders indispensable. Also, experimental tuning of the critical bondwires can improve performance. Although the small PCB insert in the prototype was a challenge for a fully automated die placement process, it enabled an excellent high-power and package-integrated demonstrator of the outphasing amplifier principle.



(a) AM-AM responses.



(b) AM-PM responses.

Figure 7.19: Measured AM-AM and AM-PM responses before and after memoryless DPD.

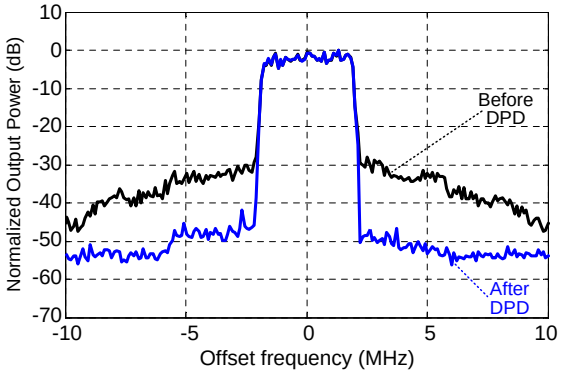


Figure 7.20: Captured spectrum with a 9.6 dB PAPR W-CDMA signal before and after memoryless DPD.

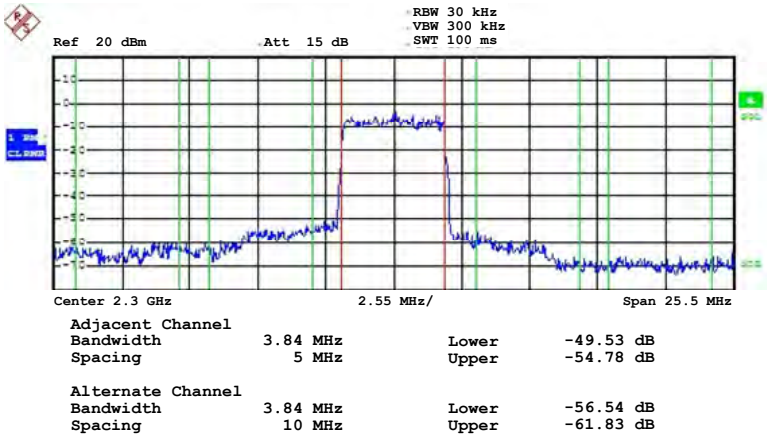


Figure 7.21: Measured ACLR levels with a 9.6 dB PAPR W-CDMA signal after memoryless DPD.

7.5. CONCLUSION

This chapter presents and describes the first package-integrated outphasing RF high-power amplifier, providing a high-performance, low-cost and compact solution for next generation wireless infrastructure systems. The classical quarter-wave transmission line outphasing combiner was replaced by a very compact and wideband bondwire-based transformer structure that included the Chireix compensation. The branch amplifiers were class-E GaN SMPAs optimized for high efficiency over a (time-varying) large load and frequency range, i.e. they were made load-insensitive by design. The demonstrator was measured with a single-carrier 9.6 dB PAPR W-CDMA signal and met the stringent 3GPP linearity requirements with a memoryless digital predistortion. It achieved state-of-the-art efficiency performance within the smallest form-factor ever reported. At 2.3 GHz and 28 V, it reached 70.6 W peak power and provided average drain and total efficiencies of 53.5% and 43.8%, respectively, with the 9.6 dB W-CDMA test signal.

In addition, this chapter provided deeper insight on the specific design of the branch amplifiers for outphasing transmitters and showed that class-E outphasing can indeed reach higher drain-efficiency at back-off than previously assumed when considering solely the net power factor of the combiner, as was addressed in Section 2.3. The high-performance prototype in this chapter demonstrated the feasibility of implementing very compact and efficient power amplifiers inside a "conventional" transistor package. Compared to conventional PA implementations, this allows up to a factor 100X in size reduction, as such opening up a new direction and opportunities for the next generation of wireless infrastructure systems.

8

HIGH-VOLTAGE CMOS DRIVERS FOR SWITCH-MODE PAS

8.1. INTRODUCTION

For handheld devices, state-of-the-art wireless communication transceivers are implemented in CMOS technology due to cost and integration advantages. For these applications, the RF power amplifiers are mostly realized in GaAs technology for linearity and efficiency considerations. Recently, watt-level silicon CMOS PAs have also been demonstrated [130] for low-cost handsets in the 2G handset market, starting to create competition on the cost/performance trade-off of the PA stage. In wireless infrastructure systems, the RF higher-power amplifier is often realized using silicon LDMOS with also recent inroads from III-V compound technologies, such as GaN, in order to enhance either the efficiency or the operating frequency. For next-generation reconfigurable infrastructure systems, switch-mode PAs seem to offer the required flexibility for multiband multimode transmitters, while at the same time they offer high-efficiency performance. In addition, device linearity in switch-mode operation is typically less of a concern, since this is mostly handled at the system level for example by the use of digital predistortion. To enable these next-generation switch-mode PA solutions, the high-power devices of the SMPAs need to be interfaced with the digital CMOS blocks of a transmitter. Consequently, wideband RF CMOS drivers capable of generating high-voltage (HV) swings are required. In this way, CMOS digital signal processing can be directly applied to control the required input pulsed shapes of the SMPA, enabling higher levels of integration and functionality.

Most of this chapter was published by: **D.A. Calvillo-Cortes**, M. Acar, M.P. van der Heijden, M. Apostolidou, L.C.N. de Vreede, D. Leenaerts, J. Sonsky, "A 65nm CMOS pulse-width-controlled driver with 8Vpp output voltage for switch-mode RF PAs up to 3.6GHz," in IEEE International Solid-State Circuits Conference (ISSCC) Digest of Technical Papers, pp. 58-60, Feb. 2011.

This chapter describes the design and implementation of HV drivers in standard 65nm CMOS technology capable of driving wide-bandgap transistors such as GaN HEMTs in high-power amplifiers. These drivers employ novel extended-drain MOS (EDMOS) devices which have been pioneered by NXP Semiconductors [131–133]. The work presented here has been initiated in the context of the NXP switch-mode PA project and was carried out under the direct guidance of M. Acar from NXP Semiconductors. The EDMOS technology will be briefly described first in this chapter. Then, the specific design and implementation of two HV CMOS drivers will be provided, along with their basic functionality and main features. After this, the actual RF measured performance will be given for the most complex driver. Finally, a brief description of practical SMPA prototypes done by others will be given that exemplify the drivers' actual capabilities.

8.2. HV CMOS TECHNOLOGY DESCRIPTION

A few-watt LDMOS or GaN transistor typically has an input capacitance of several picofarads and needs to be driven by pulsed signals with signal amplitudes exceeding 5 V peak-to-peak for optimum switch-mode operation. Therefore, the envisioned SMPA CMOS driver must provide both HV and Watt-level powers at RF. Unfortunately, standard devices in deep sub-micron CMOS technologies are severely limited in terms of maximum supply voltage due to oxide breakdown limits. Although device stacking is the most common HV-enabling technique [134, 135], it has complexity and performance limitations at RF [135]. Therefore, the design of HV CMOS drivers with EDMOS transistors [131] is preferable in order to avoid device stacking and hence increase performance.

The RF drivers described in this chapter are fabricated in a baseline low-standby-power 65 nm CMOS process that offers dual gate oxide (1.2 V thin-oxide core and 2.5 V thick-oxide I/O devices), triple well option, and up to seven metal layers (five thin and two thick metal layers) in the back-end. Additionally to the standard devices, high-voltage extended-drain MOSFETs can be built with both thin and thick gate oxides in the same technology without extra masks or process steps [131, 132]. These NXP Semiconductor's pioneered extended-drain devices offer an increased off-state breakdown voltage capability at the expense of little degradation of RF performance when compared to the 2.5 V I/O devices [132]. These EDMOS devices can be constructed using smart layout modifications, available implants and un-silicided drain extensions, profiting from fine dimensions in silicon, oxide and polysilicon regions in sub-100 nm CMOS processes [131].

Using only thin gate-oxide transistors for the complete driver provides several advantages in terms of speed and power consumption compared with thick-oxide devices. For this reason, the HV output stage of the proposed drivers uses only the "thin-oxide" EDMOS devices. The measured f_T of these devices exceed 30 GHz and 50 GHz for PMOS and NMOS, respectively, and their off-state breakdown voltage limit is about 12 V. Due to these devices, as it will be shown later, the proposed high-speed drivers can withstand 8 V peak-to-peak output swing up to 3.6 GHz. This allows driving directly wide-bandgap-based SMPAs, such as GaN, using baseline sub-micron CMOS technology.

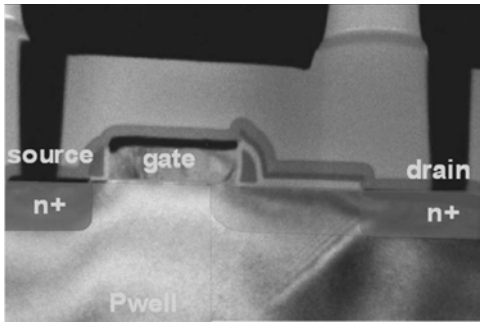


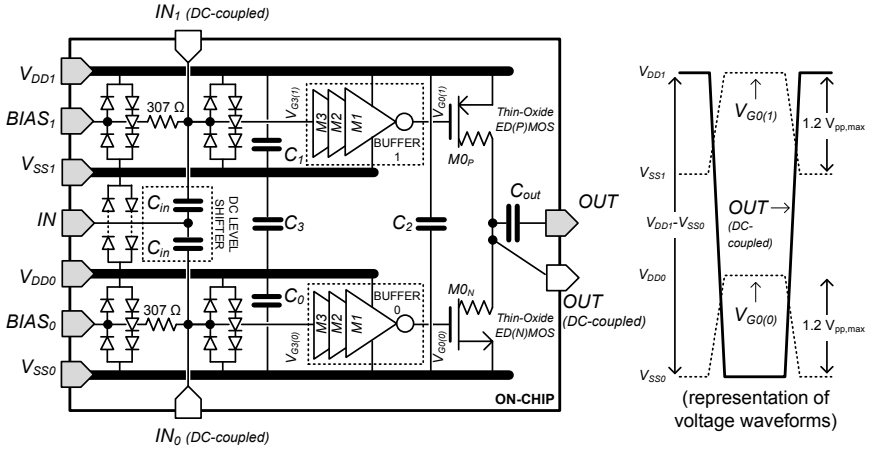
Figure 8.1: SEM cross-section photograph of an extended-drain NMOS in baseline 65nm CMOS (from [131] © 2008, IEEE.).

8.3. HV CMOS DRIVERS DESIGN

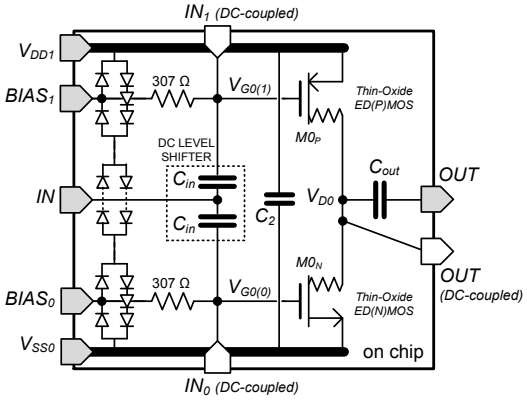
Two drivers using the thin gate-oxide EDMOS devices were designed and fabricated, and their basic schematic is depicted in Fig. 8.2. The output stage (M0) in both drivers consists of an EDMOS based inverter (i.e., ED-PMOS and ED-NMOS) which can be driven directly by the core low-voltage and high-speed standard transistors. This simplifies the integration of the output stage with other digital and analogue CMOS circuits on a single die. The most complex driver (Fig. 8.2a) has in addition two tapered buffers (buffers 0 and 1) that drive each EDMOS transistor. The other driver (Fig. 8.2b) is a simplified version without those buffers. Since the buffers are the main difference between these two drivers, the remaining description will refer to the first driver specifically while differences on the second driver will be indicated when required.

Fig. 8.3 illustrates two functional schematics of the driver in Fig. 8.2a that aids to its description. The tapered buffers in Fig. 8.2a are implemented with three CMOS inverter stages (M3-M1) made with high-speed standard devices. The two buffers have different DC levels to ensure that each CMOS inverter operates reliably within 1.2 V, i.e. $V_{DD1} - V_{SS1} = V_{DD0} - V_{SS0}$ =1.2 V. A DC-level shifter splits the input signal for each of the buffers and is implemented with two capacitors C_{in} = 16 pF (C_{in} = 37 pF for the driver in Fig. 8.2b) and two DC input biasing lines ($BIAS_{0,1}$). The output can be taken DC-coupled or AC-coupled using an on-chip capacitor C_{out} =49 pF. AC-coupling allows driving power transistors that require a negative gate biasing such as the intended GaN HEMTs. Four thick and wide power supply lines are routed inside the chip occupying most of the top metal layers: two on metal 6 (V_{SS0} and V_{SS1}) and two on metal 7 (V_{DD0} and V_{DD1}). The internal supply lines are decoupled with capacitors C_0 = 97 pF, C_1 = 96 pF, C_2 = 437 pF (C_2 = 560 pF for the driver in Fig. 8.2b) and C_3 = 104 pF. These large on-chip AC-coupling and –decoupling capacitors are implemented with dedicated parallel-plate interdigitated metal fringe capacitors. In addition, dedicated ESD protection circuitry was added to protect every single pin of the CMOS chips.

The resulting high-voltage capability of the driver is depicted in Fig. 8.3a. Each thin-oxide EDMOS device can withstand a large breakdown at their output, compared to the



a) HV CMOS driver I including pre-driver stages.



b) HV CMOS driver II with only output stage.

Figure 8.2: Schematic of the HV CMOS drivers: a) driver I including predriver stages (with relevant internal voltage waveforms), and b) driver II including only the output stage.

standard devices, and only needs an input swing of 1.2 V. This signal is given independently for ED-PMOS and ED-NMOS by each of the two buffers. Therefore, the overall output swing is determined by the "$V_{DD1} - V_{SS0}$" voltage which can be chosen freely up to the breakdown limit of the EDMOS devices, while the internal driver operation remains unchanged. This, however, requires a careful use of the deep N-well (DNW) option of the CMOS process as will be explained shortly. In addition to this, Fig. 8.3b shows a pulse-width-modulation (PWM) control feature of the driver. PWM control provides a means to perform fine adjustment/tuning functionality to enhance the performance in advanced SMPAs. This PWM is accomplished by using the "variable gate bias" technique [136]. The bias level at the first inverter (M3) of buffer 0 and 1 shifts up/down an RF sinusoidal input signal with respect to the inverter's own switching threshold. A change on this bias voltage will vary the pulse-width at the output of such first inverter

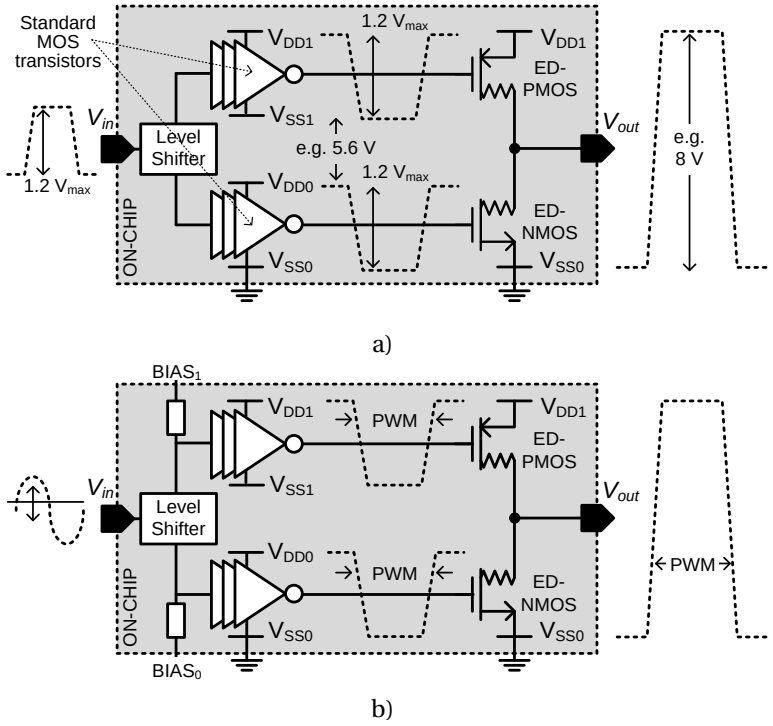
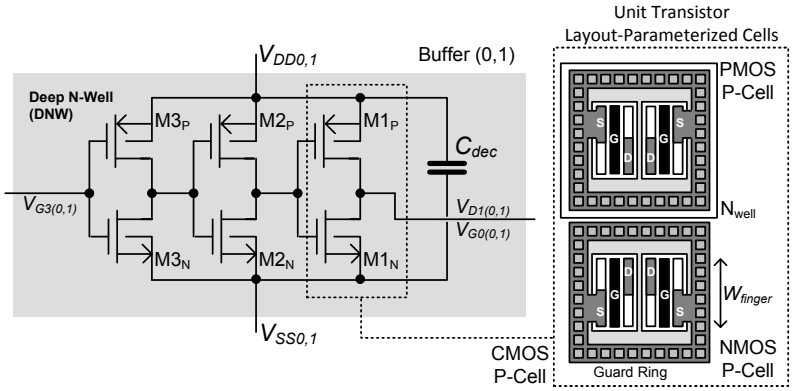


Figure 8.3: Functional schematics of the HV CMOS driver: a) high-voltage output swing capability, and b) pulse-width control feature.

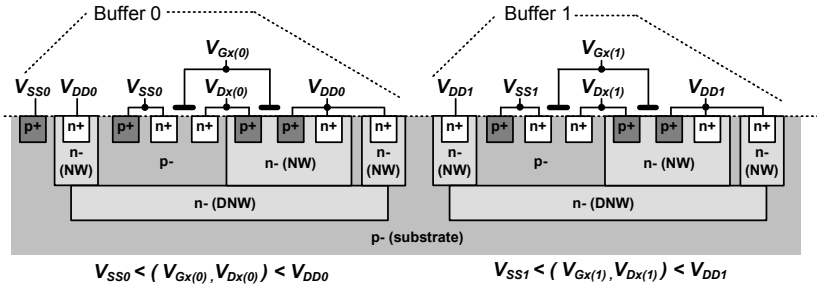
M3. Then, this PWM signal will propagate through the remaining inverters in the buffer, M2 and M1, and will be combined at the output EDMOS stage of the driver. This will effectively control the PWM of the output square wave.

In order to use different sets of supply voltages and to allow identical AC operation, the two buffers are identical and placed inside individual deep N-wells. Fig. 8.4a shows the schematic of the buffers, while Fig. 8.4b depicts a cross-section diagram illustrating the two DNWs. In order to ensure a proper operation of the inverter-chain and the DNW, the DC-biasing scheme showed in Fig. 8.4b must be followed. Observe that each DNW is biased at the highest DC-level of the buffer (i.e., V_{DD0} or V_{DD1}, depending on the specific buffer) by using N-well (NW) strips in the outer edges of the complete structure. Wide metal-contact stacks provide a low ohmic connection between those NW strips and the $V_{DD(0,1)}$ supply lines which are in the top and thicker metal layers of the chip. The bottom substrate must be biased at the lowest DC-level in the CMOS driver, i.e. V_{SS0} which is grounded. This will ensure that the each DNW is kept reverse-biased with respect to the bottom substrate during the driver operation, providing isolation to the inverter chains regardless of their specific biasing levels.

All the inverters in the chip (M0 to M3) employ a unitary PMOS-to-NMOS transistor size ratio in order to ease layout and ensure symmetry between the two RF paths



a) Buffer schematic with unit CMOS P-cell layout illustration.



b) Cross-section illustration of the active areas of the two buffers.

Figure 8.4: Details of the tapered buffers.

8

prior to the output stage. The transistors in the M0, M1, M2 and M3 stages have total widths of 4032μm, 1440μm, 480μm and 240μm, respectively, and have minimum gate length. The layout of each transistor was split up into many unit transistor layout-parameterized cells (P-cell) and was optimized to obtain maximum frequency performance according to the available bandwidth f_A figure-of-merit [137]. Maximizing f_A provides a good indication of optimum transistor layout (both, unit transistor P-cell layout and the arrangement of such unit cells in the total transistor) and hence of RF circuit performance[1]. Each P-cell is layout-scalable [133] and contains an asymmetric-layout multi-finger transistor with finger width of 3μm, with its own guard ring and all its interconnections up to metal 7. A top view of a CMOS P-cell in the buffers is illustrated at the right of Fig. 8.4a while Fig. 8.5 shows the actual layout view of those buffers. Notice that there is also some inter-stage AC-decoupling capacitance in the buffer, right next to the inverters, totaling about $C_{dec} \approx 2.4$ pF. Similarly, Fig. 8.6 depicts the actual layout view of one of the large EDMOS transistors, including the constitutive unit transistor P-cell.

[1] Unlike f_T or f_{MAX}, f_A can be measured (or simulated) without any extrapolation and is determined by both input and output parasitic capacitance which is strongly dependent on the layout, especially for large transistors. Therefore, f_A is a much better representation of the actual delays involved in accessing the intrinsic device by the external voltages at high frequencies compared to f_T and f_{MAX} [137].

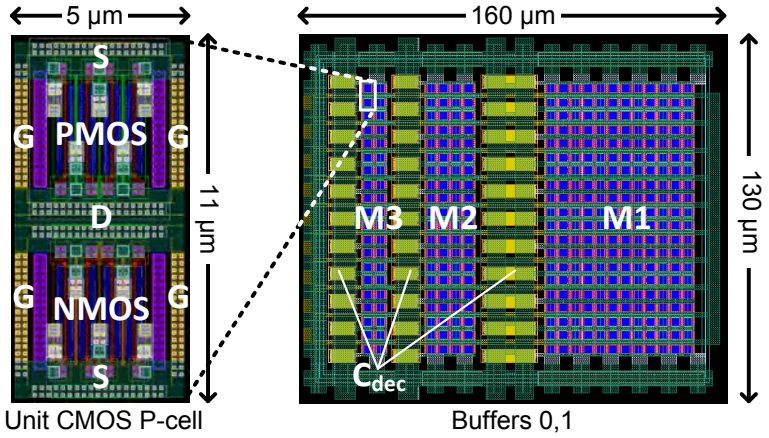


Figure 8.5: Layout view of the tapered buffers, showing the detail of a single CMOS unit P-cell.

Figures 8.7 and 8.8 show the micro photographs of the fabricated CMOS drivers. The first driver with buffers has an active area (EDMOS and buffers) of only is 0.16mm^{2}and a total chip area is 1.99mm^2. In turn, the driver without buffers has an active area of 0.08mm^{2}and a total chip area of 1.63mm^2. As can be appreciated from the pictures, most of the chip area is comprised by bondpads (for which the majority is for ground and DC supply). Besides the input and output capacitors, such large area (including underneath the bondpads) is actually exploited by the AC-decoupling capacitors C_0-C_3 as they are distributed along any available space in the chip in the form of segmented parallel-plate interdigitated fringe capacitors on the lower first five metal layers. This large decoupling reduces the sensitivity of the chip to the supply bondwires for large currents.

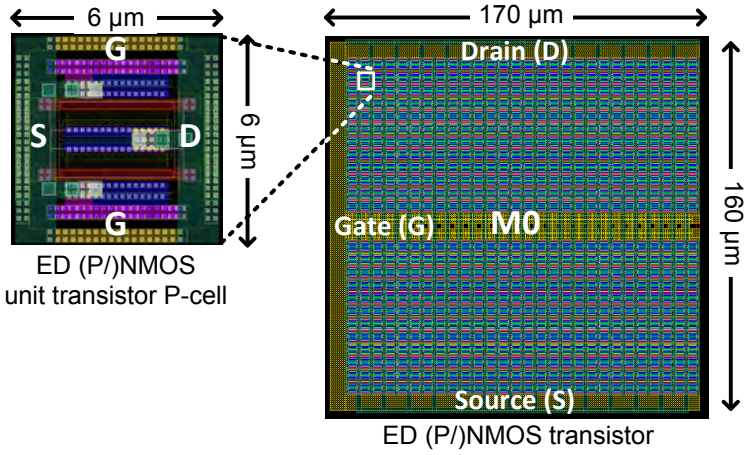


Figure 8.6: Layout view of a large EDMOS transistor, showing the detail of a single transistor unit P-cell.

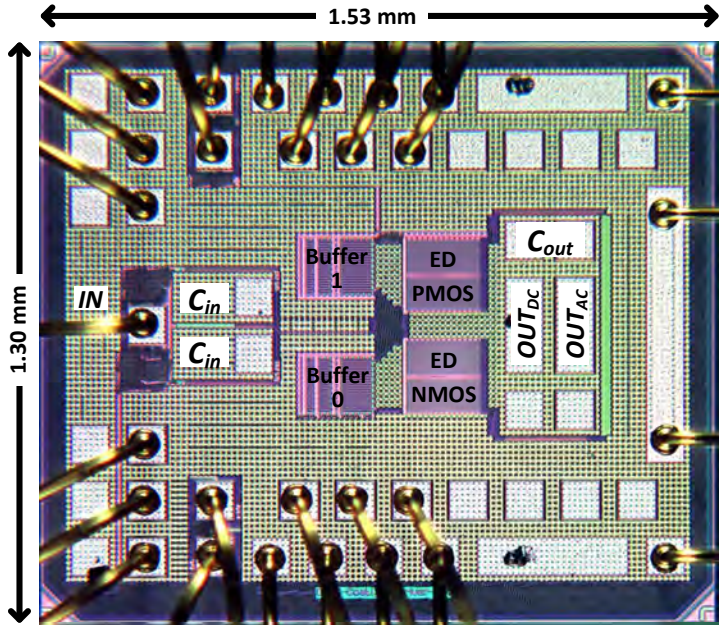


Figure 8.7: Micro photograph of the HV CMOS driver I with buffers (total chip area of 1.99mm^2 with an active area of 0.16mm^2).

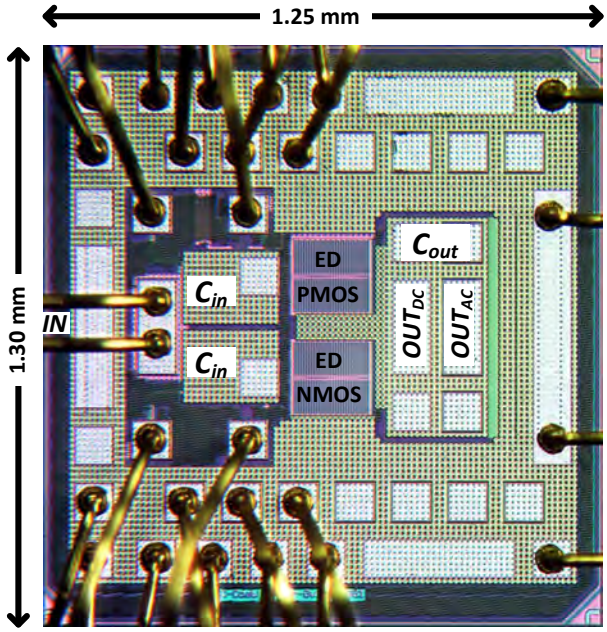


Figure 8.8: Micro photograph of the HV CMOS driver II without buffers (total chip area of 0.08mm^2 with an active area of 1.63mm^2).

8.4. HV CMOS DRIVERS MEASUREMENT RESULTS

The fabricated prototype dies were mounted on a dedicated PCB for test purposes with the bench setup depicted in Fig. 8.9. Since the two drivers share exactly the same output stage, only the results of the CMOS driver with buffers are described next. The measures were performed in a 50Ω load environment with the bias arrangement depicted in Fig. 8.9. The input of the driver was connected to the test PCB through a bondwire and the output was accessed using a 500 μm-pitch ground-signal-ground probe directly on top of the chip. The driver was excited by an RF signal generator while time-domain signals were captured using a high-speed digital sampling oscilloscope. The clock of the oscilloscope was triggered from another signal generator locked to the first one, as shown in the figure.

Fig. 8.10 shows the measured time-domain waveforms of the DC-coupled output of the RF driver at 3 V, 5 V, 7 V and 9 V supply voltage (i.e. "$V_{DD1} - V_{SS0}$") with an input sine wave at 2.1 GHz. The maximum swing measured was 8.04 V_{pp} for a 50Ω load and 9 V supply. The equivalent on-resistance of the driver was measured as 4.6Ω. Fig. 8.11 gives the measured pulse-width (expressed as duty-cycle) control range as a function of the normalized DC bias levels, i.e. $BIAS_{0,1} - V_{SS0,1}$. In the same figure, two time-domain waveforms are shown for different duty-cycle conditions. At 2.4 GHz and 5 V supply, a duty-cycle control range of 30.7 to 71.5% was observed. The measured 10-to-90% and 20-to-80% rise and fall times are given at different operating frequencies in Fig. 8.12 where it can be noticed that the CMOS driver maintains its pulsed shape behavior with 8V_{pp} up to 3.6 GHz (which corresponds to a period of about 278 nsec). In addition, further

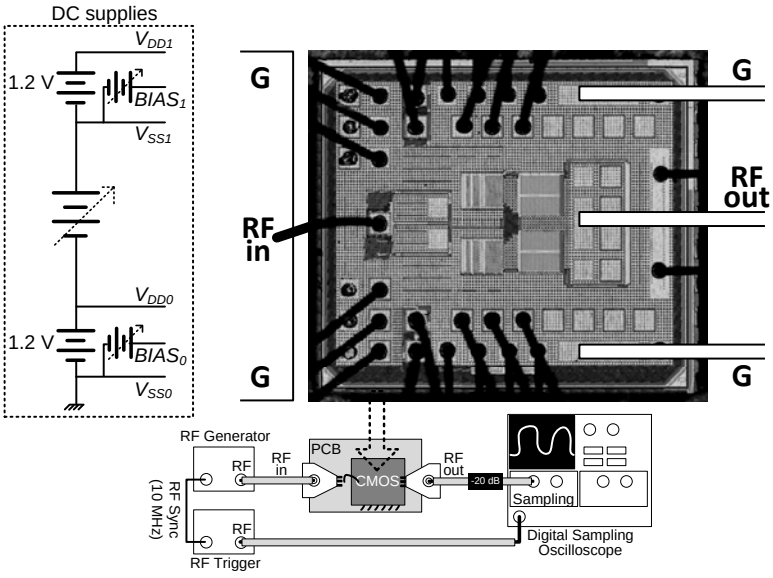


Figure 8.9: Test bench setup for measuring the HV CMOS drivers.

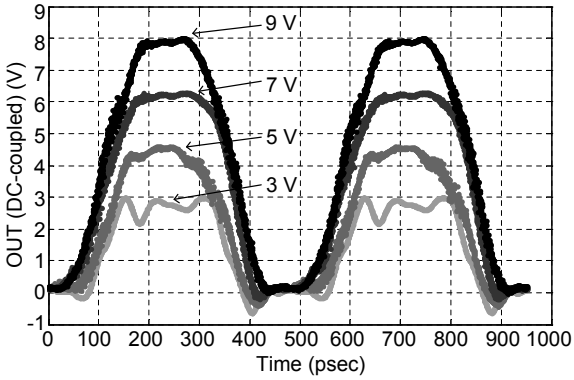


Figure 8.10: Measured time-domain waveforms with $V_{DD1} - V_{SS0}$ = 3 V, 5 V, 7 V and 9 V at 2.1 GHz.

measurements were performed at 2.4 GHz that monitored the continuous wave output swing and showed no performance degradation with 5 V and 9 V supply after 24 hours of continuous operation, as shown at Fig. 8.13.

Table 8.1 summarizes the measured performance of this CMOS driver and compares it with other published works. It can be observed from the table that the proposed driver reached a much larger output voltage swing and higher operating frequency as compared to the previous state-of-the-art in CMOS. Also, in addition to the pulse-width control functionality, this driver has larger output swings for similar frequencies when compared to a SiGe-BiCMOS equivalent circuit [138].

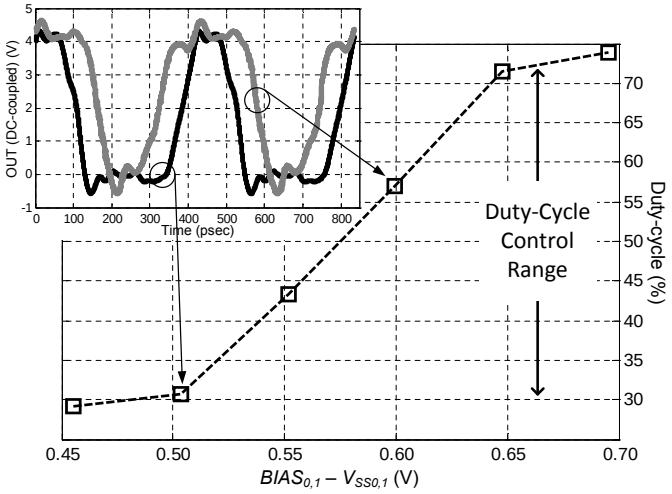


Figure 8.11: Measured duty-cycle performance versus normalized biasing levels at 2.4 GHz and $V_{DD1} - V_{SS0}$ = 5 V.

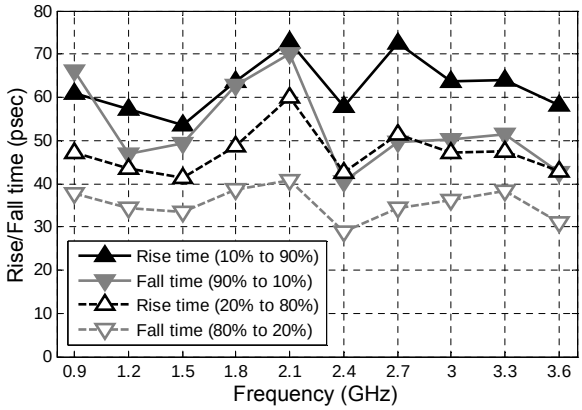


Figure 8.12: Measured rise and fall times versus frequency for a continuous wave signal with 50% duty-cycle at $V_{DD1} - V_{SS0} = 6$ V.

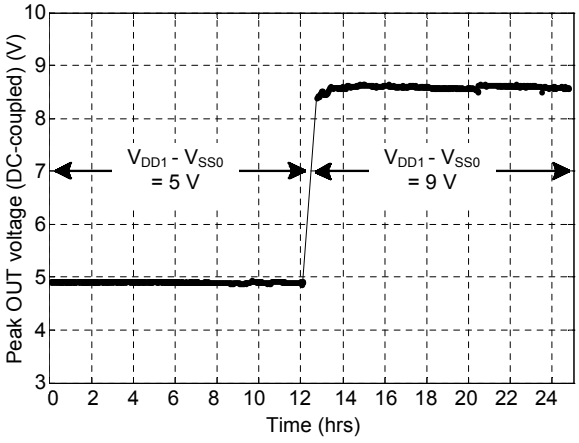


Figure 8.13: Measured long-term continuous wave operation showing no performance degradation for 5 V and 9 V supply after 24 hours.

Table 8.1: MEASURED PERFORMANCE AND PROCESS SPECIFICATIONS OF THE DRIVER IN THIS WORK AND THE PREVIOUS STATE-OF-THE-ART.

Parameter	[134]	[138]	**This work**
Technology	CMOS	SiGe-BiCMOS	CMOS
Node	0.25μm	0.25μm	65 nm
Nominal supply voltage	2.5 V	4.3 V	1.2 V
Operating supply voltage	7.5 V	4.3 V	up to 9 V
Load	50Ω	50Ω	50Ω
Maximum output swing	6.46V$_{pp}$	4V$_{pp}$	8.04V$_{pp}$
ON-resistance	5.9Ω	Not specified	4.6Ω
Operating frequency	10 MHz	0.5 to 3.5 GHz	0.9 to 3.6 GHz
Duty-cycle range	50% (fixed)	50% (fixed)	30.7 to 71.5%
			@ 2.4 GHz, 5 V
Square wave performance			
P_{out} @ Frequency, Supply	208 mW @ 10 MHz, 7.5 V	145 mW @ 0.9 GHz, 4.3 V	216 mW @ 0.9 GHz, 9 V
		230 mW @ 2.1 GHz, 4.3 V	221 mW @ 2.1 GHz, 9 V
		116 mW @ 3.5 GHz, 4.3 V	179 mW @ 3.5 GHz, 9 V

8.5. EXAMPLES OF HV CMOS DRIVERS IN GAN SMPAS

The CMOS drivers described previously have in fact been used in actual SMPA prototypes in other works by others [28, 139], demonstrating the control of GaN HEMTs in efficient RF power amplifiers. Next is a brief reference to those works with the sole aim of highlighting the presence of the HV CMOS driver described in this chapter.

The work of M.P. van der Heijden *et al.* in [28] uses two CMOS drivers to interface directly with a couple of GaN HEMTs in a very efficient and broadband class-E outphasing power amplifier. Fig. 8.14 provides a picture of the prototype in [28] highlighting the CMOS drivers and their interface with the GaN HEMTs. The CMOS and GaN dies, together with dedicated silicon AC-decoupling capacitors, were placed on top of a CuW-flange at the middle of a multilayer PCB. The rest of the circuit, including a Marchand balun, is fabricated in a dual-layer Rogers laminate to which the dies are connected to by short bondwires [28]. This 19 W CMOS-GaN prototype demonstrates state-of-the-art average efficiency and bandwidth performance, reaching 65.1% and 51.6% average drain- and total-efficiency, respectively, for a 7.5 dB PAR W-CDMA signal at 1.95 GHz and over 60% drain-efficiency across 6 dB power back-off and 250 MHz bandwidth.

The work of M. Ozen *et al.* in [139] employs one of the HV CMOS drivers described in this chapter to control a GaN HEMT class-E RF power amplifier in a dual mode: PWM at the high-power levels and linear operation at the back-off power levels. Fig. 8.15 shows

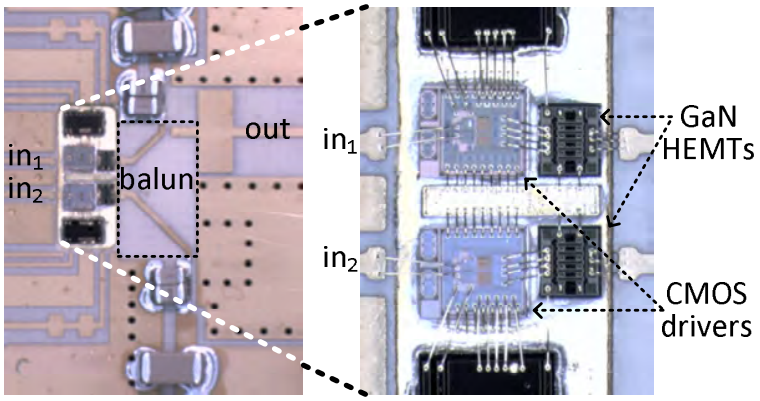


Figure 8.14: Example of use of the developed HV CMOS drivers (seen at the middle of the left inset), as implemented by M.P. van der Heijden, M. Acar *et al.* [28] in a 19 W outphasing amplifier using GaN HEMTs at 1.9-2.1 GHz. (Courtesy of M.P. van der Heijden from NXP Semiconductors, The Netherlands. © 2011, IEEE.)

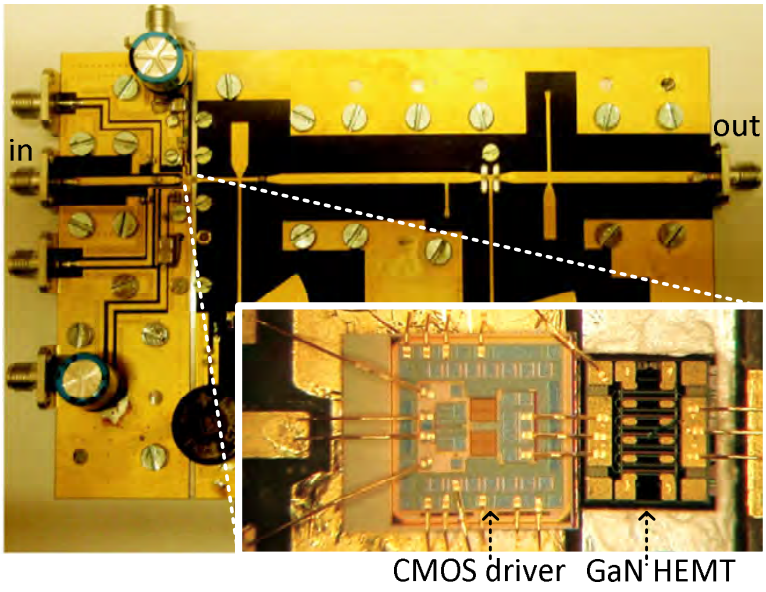


Figure 8.15: Example of use of the developed HV CMOS drivers (seen at the bottom-right inset), as implemented by M. Ozen *et al.* [139] in a 10 W class-E amplifier using one of this HV CMOS drivers as a pulse-width modulator to control a GaN HEMTs at 2.0 GHz. (Courtesy of M. Ozen from Chalmers University of Technology, Sweden. © 2011, IEEE.)

the picture of the prototype in [139] in which the HV CMOS driver is highlighted. The CMOS driver is mounted on top of a PCB while the GaN die is placed directly on an aluminum block underneath that PCB with short bondwires used for interconnection. Since the CMOS driver used in this prototype does not have buffers (see Fig. 8.2b), it is used as a saturated RF pulse-width modulator at the highest output power range of the class-E amplifier and as a linear driver for the lowest power range. In addition to the PWM-control provided by the driver, the fabricated 10 W CMOS-GaN prototype in [139] uses a SiC varactor for tuning the imaginary part of the fundamental load impedance to achieve over 70% drain-efficiency for 6.5 dB power dynamic range at 2 GHz.

8.6. CONCLUSIONS

This chapter described the design and implementation of high-voltage CMOS drivers capable of controlling directly high-power transistors such as GaN HEMT. These drivers generate very large output swings, up to $8V_{pp}$, while having a wideband operation up to 3.6 GHz. They were implemented in a 1.2 V baseline 65nm CMOS technology. At the output stage, they used complementary extended-drain MOS devices with off-state breakdown voltages of about 12 V in order to avoid device stacking and therefore save power. Since the EDMOS devices use thin-oxide at their gate, further circuitry using the standard and high-speed thin-oxide core devices can be added for increased functionality. In addition, a pulse-width modulation feature was demonstrated, reaching a duty-cycle control range from 30.7 to 71.5% at 5 V supply and 2.4 GHz, on a 50Ω environment. The practical operation of these drivers has also been demonstrated in practical switch-mode power amplifier implementations using GaN HEMT in the works by others: [28] and [139]. This kind of HV CMOS drivers can serve as a key building block for next generation reconfigurable multi-band multi-mode transmitters for wireless infrastructure systems, interfacing digital CMOS circuitry with high power transistors.

9

CONCLUSIONS AND RECOMMENDATIONS

The main objectives of this thesis are to improve the energy efficiency and physical form-factor of high-power amplifiers for base station applications. In view of this, the focus of this dissertation is placed on outphasing amplifier concepts, which can offer high-efficiency, good linearity and excellent opportunities for (system) integration. With this mind set, various outphasing concepts with their specific aspects has been studied at different levels of abstraction, starting from their fundamental operation in Chapter 2, to very detailed implementation considerations in Chapters 3 to 4. To enable package integration of complete RF power amplifiers, Chapter 5 introduced dedicated design techniques for constructing very compact high-power magnetic components that utilize standard low-cost wire bonding techniques. In particular, a low-loss and high-current-handling RF transformer concept was introduced that allows easy power scaling. In Chapter 6, the techniques of Chapter 5 were applied in the design and realization of very compact high-power class-E branch amplifiers. Chapter 7 provided one of the key demonstrators of this thesis work, namely; the design and implementation of a "70W fully packaged integrated GaN outphasing amplifier". To facilitate the advanced system integration of future LDMOS / GaN based switch-mode power amplifiers, Chapter 8 elaborated on the design of high-voltage CMOS drivers that can provide the essential physical link between the PA stages with the forgoing TX chain implemented in standard low-voltage CMOS technologies. In this Chapter we summarize the overall conclusions and recommendations achieved in this thesis work.

9.1. CONCLUSIONS

9.1.1. OUTPHASING AMPLIFIER TECHNIQUES

For several decades, the outphasing amplifier concept has been a very appealing concept for the implementation of highly-efficient and linear power amplifiers in communication systems. However, in spite of its potential, at the start of this thesis work there were no outphasing implementations that were convincing enough in terms of efficiency, bandwidth, output power, integration and cost level to serve macro-cell base station applications. It was one of the prime research goals of this work to change this situation. In literature, there are many different flavors of the outphasing concept reported, which include; variations in the power combiner used, the number of branch amplifiers, the operating class employed, the specific input drive profiles, etc. Clearly, from an efficiency point of view, use of non-isolating combiners and switch-mode branch amplifiers is more attractive due to their inherent higher efficiency potential; however SMPAs are significantly more challenging in their design and implementation.

Typically, the impact of the power combining network on the achievable efficiency is addressed using the so-called net power factor. Detailed analysis in this work showed there are specific conditions in which the overall efficiency of an outphasing amplifier can be significantly higher than what is typically estimated by this traditionally used figure-of-merit. A clear example of such occurrence is found when combing switch-mode class-E branch amplifiers with a non-isolating Chireix power combiner (as described in Section 2.3 and demonstrated in practice in Subsection 7.4.2). Closer inspection and comparison with alternative outphasing implementations show that it is this specific efficiency "enhancement" that makes this particular implementation the most appealing in terms of efficiency.

For outphasing amplifiers using class-E operation in their branches, the transistor's gain is a very important consideration. Smart drive profiles can improve the effective gain of the amplifiers by introducing some amplitude modulation and as such, saving power at deep back-off regions using mixed-mode control (see Chapter 3). Regarding the number of branches, four-way outphasing concepts can lower the unwanted dynamic reactance, which in principle can translate to higher efficiencies in power back-off operation. However, in practice clever two-way designs can offer very competitive performances with at a much lower complexity. In addition, some of the techniques discussed in this thesis for the two-way amplifiers, such as mixed-mode operation as well as class-E operation for the branch amplifiers, can also be employed in N-way outphasing amplifiers.

9.1.2. SYSTEM-LEVEL STUDIES OF LOAD-MODULATED AMPLIFIERS

A detailed system-level study of power amplifiers is presented in this thesis, which is very helpful to compare several amplifier topologies for their performance assuming a

common transistor device. In this work, the idealized transistor model allows to consider several important constrains and non-idealities of practical devices, such as finite power gain as well as voltage and current handling limitations. The objectives of this system study are twofold. First, to analyze the ideally achievable efficiency performance of the several Doherty and outphasing amplifier configurations, including the use of class-B and class-E branch amplifiers as well as the different input drive profiles for the branch amplifiers. The second objective is to analyze the bandwidth expansion of the branch signals of those amplifiers, with a particular focus on outphasing amplifiers. As such, in Chapter 3 it was demonstrated that the efficiency of outphasing amplifiers is typically higher than of two-way Doherty amplifiers when dealing with signals with a high PAPR (e.g. 10-12 dB). In addition, it was also shown that the required input power and drive profile for a particular amplifier concept has high impact on the achievable total-average efficiency. In view of this, use of mixed-mode control or other means to reduce the input drive proves to be very important. This is most visible by considering the rather spectacular drain-efficiency of a class-E (pure-mode) outphasing amplifier, which after including the required input power, yields in the end a comparable overall system efficiency as a mixed-mode class-B outphasing amplifier with optimum input signals for its branch amplifiers. Besides their efficiencies, class-B and class-E outphasing amplifiers have also other important differences. Contrary to the class-E case, the ideal input drive signal for a class-B outphasing amplifier, when using a voltage-source-like combiner, is no longer a pure phase-modulated signal as traditionally considered. In fact, although purely phase-modulated signals can be employed and the related efficiency performance is better than a stand-alone class-B amplifier, such performance is still far from its optimum. Consequently, the optimum drive for class-B outphasing PAs requires a specific amplitude control that depends on the applied power combining network. This makes the optimum drive profile for class-B outphasing amplifiers sensitive to the actual hardware configuration and therefore more complicated in practical cases.

The bandwidth expansion of the branch input signals in various Doherty and outphasing amplifiers is discussed in Chapter 4. In the Doherty amplifier, bandwidth expansion happens in the "peaking" branch, while in the outphasing amplifier it occurs for both branches. It was shown in this work that also the nature of the modulated signal itself has a significant impact on the bandwidth expansion. This can be related to the different trajectories near the origin, which due to the required non-linear transformations, leads to different degrees of bandwidth expansion. This effect is more profound in pure-mode outphasing amplifiers than in amplifiers that use some amplitude modulation for their drive signals, such as the Doherty and the mixed-mode outphasing amplifier. In the particular case of a pure-mode outphasing amplifier, the effect of limited branch amplifier bandwidths and original signal's over-sampling ratios on the distortion of the overall output was analyzed. This analysis considered the use of switch-mode PAs represented by ideal limiters. The simulation results indicated that band-limiting the branch signals, does not distort per se the output signal but rather introduces some amplitude variation in the branches. If SMPAs are used in the PA branches, then the phase-modulation of these signals is implicitly restored while the signal bandwidth is automatically expanded again. The net effect of this limiting by the SMPA is that some distortion in the overall outphasing amplifier appears. However, reasonably low branch

bandwidths and the use of sufficiently high over-sampling ratios can suffice to comply with in-band and out-of-band linearity specifications. This is a more objective way to quantify the impact of bandwidth expansion in outphasing amplifiers than traditionally done using an arbitrary power level definition as measure.

9.1.3. DESIGN OF COMPACT BONDWIRE MAGNETIC COMPONENTS

In Chapter 5, it was demonstrated that compact RF magnetic components can be designed and implemented using standard and low-cost wire bonding techniques. When several individual bondwires are employed in parallel arrangements, RF inductors and transformers can have very low losses and large current-handling capabilities. Full 3D electromagnetic tools are required for the design of such components. The agreement between the designed and the actual electric behavior depends to great extent on the accuracy to which the designed element can be implemented in practice. Currently, there are implementation limitations as most wire bonding machines still lack the ability to reproduce accurately a bondwire shape directly from geometrical specifications. Instead, some ad hoc practical experimentation is still needed to find practical recipes for the targeted shapes. Fortunately, once such shapes can be realized, automated machines can reproduce them easily and very consistently. In this regard, this thesis contributed a novel RF transformer component targeted for high-power applications. A prototype was built and measured, providing very low losses and large magnetic coupling factors for up to a few gigahertz. This component was subsequently used in the designs presented in other chapters and enabled very compact and highly-efficient amplifier demonstrators.

9.1.4. PACKAGE-INTEGRATED HIGH-POWER RF STAGES

This thesis described and demonstrated design techniques that enable the integration of high-power amplifiers inside otherwise standard transistor packages. In Chapter 6, it was shown that it is possible to design high performance amplifiers inside transistor packages by using low-cost and standard technologies. In particular, specific design aspects as well as verification strategies were discussed in the context of two highly efficient, broadband and high-power class-E amplifiers using GaN HEMT in an environment mimicking a transistor package. In addition to standard PCB-based amplifier design techniques, the design of package-integrated amplifiers requires the design of many of its individual passive components with bondwires. For this, and also for the entire design, extra simulation tools and strategies to the regular circuit simulators are required, including 3D EM tools that can simulate the non-planar bondwire-based components. The fabricated amplifier prototypes demonstrated in Chapter 6 provided very encouraging results in terms of efficiency, bandwidth, power and size. This demonstrated the feasibility of low-cost fully package-integrated high-power amplifiers for wireless infrastructure applications.

9.1.5. PACKAGE-INTEGRATED CHIREIX OUTPHASING AMPLIFIER

Many of the techniques and conclusions of the previous chapters were applied in the design and implementation of the first outphasing RF high-power amplifier integrated inside a customized transistor package, as described in Chapter 7. At the moment of this writing, this two-way amplifier design is state-of-the-art when accounting for its high efficiency performance and very compact size. In addition, its performance is on pair of other amplifier configurations and even better that more complex 4-way outphasing systems published recently [39]. In this novel outphasing PA implementation, the classical quarter-wave transmission line outphasing combiner was replaced by a very compact and wideband bondwire-based transformer structure that included the Chireix compensation. The branch amplifiers were class-E GaN SMPAs optimized for high efficiency over a (time-varying) large load and frequency range, i.e. they were made load-insensitive by design. The demonstrator was measured with a single-carrier 9.6 dB PAPR W-CDMA signal and met the stringent 3GPP linearity requirements using a memoryless digital pre-distortion algorithm. At 2.3 GHz and 28 V, it reached 70.6 W peak power and provided average drain and total efficiencies of 53.5% and 43.8%, respectively. This high-performance prototype demonstrates the feasibility of implementing very compact and efficient power amplifiers inside transistor packages, opening up a new direction and opportunities for the next generation of wireless infrastructure systems.

9.1.6. HIGH-VOLTAGE CMOS DRIVERS FOR SWITCH-MODE PAS

While most transceivers are implemented using deep-submicron silicon CMOS, high performance power amplifiers for base stations (such as switch-mode PAs) are currently being implemented using III-V semiconductors, such as GaN HEMTs. These transistors require large output voltage swings for their proper operation. In Chapter 8, high-voltage CMOS drivers capable of controlling directly such high-power and large-input-swing transistors were demonstrated. These CMOS drivers, based on a special extended-drain transistor technology from NXP semiconductors, were able to generate very large output swings up to 8 V_{pp}, while operating wideband up to 3.6 GHz. They were implemented in a 1.2 V baseline 65nm CMOS technology. At the output stage, they used complementary thin-oxide extended-drain MOS devices with off-state breakdown voltages of about 12 V. In addition, a pulse-width modulation feature was demonstrated, reaching a duty-cycle control range from 30.7% to 71.5% at 5 V supply and 2.4 GHz, on a 50 Ω environment. The practical operation of these drivers was demonstrated in practical switch-mode power amplifier implementations using GaN HEMT in other works [28, 139]. This kind of HV CMOS drivers can serve as a key building block for next generation reconfigurable multi-band multi-mode transmitters for wireless infrastructure systems, interfacing digital CMOS circuitry with high power transistors.

9.2. RECOMMENDATIONS FOR FURTHER RESEARCH

From the work and outcomes of this thesis, several suggestions can be given for further research:

- The system-level study of power amplifiers developed here proved to be very useful to analyze the ideal efficiency performance of several amplifier configurations using a simplified common transistor model. Although already some important practical constrains and non-idealities were considered in the device model, others can still be added. For example, the linearity and predistortability of amplifiers can be better evaluated when incorporating some of the main sources of distortion into the active device's model. For example, weak amplitude distortion can be incorporated by modeling the drain-source current source by a polynomial (for example the third order polynomial proposed in [16, Ch. 4]). Similarly, phase distortion can be accounted for by modeling the output capacitance with a non-linear function of the drain-source voltage. It is the author's belief that these two additions can provide a good starting point to compare the linearity performance and predistortability for the different amplifier configurations.

- The topic of the branch signals' bandwidth expansion on the different load-modulated amplifiers can be further researched. In particular, practical verification of simulation experiments are very appealing. For this, the individual and collective influence of more practical system parameters such as signal content, quantization noise, digital and analog filter details, bandwidth equalization, etc., are required in order to arrive to application specific conclusions.

- Regarding the outphasing amplifier configurations, many suggestions can be given in different and non-exclusive directions. On one side, techniques aimed to reduce the required drive power in outphasing amplifiers are very interesting, as this remains one of the true bottle necks of switch-mode operated amplifiers when considering their achievable total efficiency. Other examples of research opportunities relates to the further exploration of "mixed-mode" outphasing. On the other side, the use of multiple branches beyond two is a relatively new development that still requires more research, especially in the tradeoff between the attainable performance improvements (for both efficiency and linearity) and the related complexity.

- Furthermore, it is recommended to continue research on bondwire structures that facilitate the implementation of low cost, compact power combining and matching networks as they act like the key to a new generation of package integrated PA systems. Special attention should be given to reduce manufacturing complexity and yield problems.

- Also, it is recommended to continue research on alternative practical implementations of compact power amplifiers such as the ones described in this thesis. For example, more research activities can be targeted on reducing manufacturing complexity of the prototypes proposed in this work as well as targeted on compact implementation of other amplifier configurations.

- Finally, it is strongly recommended to continue on the path of integration of complete TX line-ups as they can offer higher data capacity and functionality, while allowing major energy, size and cost reductions. These are essential properties to fuel the devel-

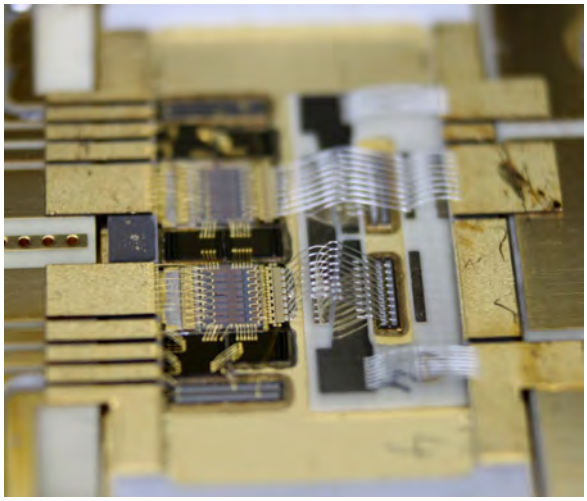


Figure 9.1: Photograph of a designed package-integrated outphasing system with HV-CMOS drivers realized by NXP Semiconductors in Nijmegen.

opment and implementation of the wireless infrastructure of the future which, according to various predictions, needs to handle a factor 1000x increase in data transport in the coming decades.

In view of this, and although unfortunately not completely finished within the time frame of this thesis work, an appealing demonstrator of such a highly integrated transmitter was developed in close support and cooperation with NXP Semiconductors, whose picture is given below in Fig. 9.1. This fully package integrated outphasing system with HV-CMOS drivers allows direct compatibility with the preceding TX chain. In future work also the TX chain itself can, in a relatively straight manner, be included on the CMOS driver IC, as such enabling “a high-power base station transmitter in a package”.

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SUMMARY

In the last few decades, information and communication technologies have experienced a tremendous development in order to satisfy the intrinsic need of humans to communicate. Today, these technologies are at the core of every modern knowledge-based society and serve billions of users, with more mobile than fixed subscriptions. This increase in users combined with the annual doubling of data traffic, drives the energy consumption of ICT devices and wireless infrastructure worldwide, resulting in significant economic and environmental footprints. As such, current telecommunication networks consume more than 1% of the total electricity worldwide and are responsible for a similar share of greenhouse gas emissions. These energy costs represent an important part of the total operating expenses of wireless networks. This fact, combined with the society demand for reduced environmental footprints, forces network operators to reduce, or at the minimum keep flat, their network energy consumption while handling more users and data traffic. Dedicated case studies estimate that more than 75% of all wireless network energy expenditure is due to the radio access equipment in the base station. In particular, the RF power amplifiers in these systems are considered the most power-hungry elements and, therefore, are a logic target for improvement and detailed research.

In view of this, the main objectives of this thesis are to improve the energy efficiency and physical form-factor of high-power amplifiers in base station applications. As such, the focus of this dissertation is placed on the outphasing amplifier concept, which can offer high-efficiency, good linearity and excellent opportunities for system integration. With this mind set, various outphasing concepts have been studied at different levels of abstraction, starting from their fundamental operation, to very detailed efficiency and bandwidth considerations. In order to enable the future package integration of complete RF high-power amplifiers and transmitter lineups, dedicated design techniques for very compact and high-power magnetic components have been developed utilizing low-cost wire bonding techniques. Using these techniques, a very low-loss, high-current RF transformer concept was introduced that allows straight forward power scaling in RF amplifiers. Next, to demonstrate the practical use of these low-loss magnetic components with their related design flow, two very compact high-power class-E branch amplifiers were realized and tested. Expanding on these initial works, one of the key demonstrators of this thesis was a "70W fully packaged-integrated GaN outphasing amplifier", which represents a remarkable combination of high-efficiency, high-output power with a very small form factor. Finally, to facilitate the future integration of advanced switch-mode outphasing systems in a single package, the design of high-voltage CMOS drivers was discussed and demonstrated. These devices can provide the essential physical link between the final PA stages with the intelligence of the forgoing TX chain, which is typically implemented in standard low-voltage CMOS technologies.

SAMENVATTING

In de afgelopen decennia hebben informatie en communicatie gerelateerde technologieën een enorme ontwikkeling ondergaan om aan de intrinsieke communicatiebehoefte van de samenleving te voldoen. Vandaag de dag vormen deze technologieën het kloppend hart van elke moderne kennismaatschappij en bedienen zij wereldwijd enkele miljarden gebruikers, met meer mobiele dan vaste verbindingen. Deze toename van gebruikers, gecombineerd met de jaarlijkse verdubbeling van draadloos dataverkeer, verhoogt het energieverbruik van ICT en draadloze infrastructuur wereldwijd, wat resulteert in aanzienlijke economische en ecologische voetafdrukken. Als zodanig, verbruiken de huidige telecommunicatienetwerken meer dan 1% van het totale elektriciteitsverbruik wereldwijd en zijn verantwoordelijk voor een evenredig aandeel in de uitstoot van broeikasgassen. Deze energiekosten vormen een belangrijk onderdeel van de operationele kosten van draadloze netwerken. Dit feit, gecombineerd met de maatschappelijke drang naar een kleinere ecologische voetafdruk, dwingt exploitanten het energieverbruik van hun netwerken te verminderen of op zijn minst gelijk te houden bij het verwerken van meer gebruikers en dataverkeer. Specifieke casestudies schatten dat meer dan 75% van al het energieverbruik in een draadloos netwerk toe te schrijven is aan de zendapparatuur in het basisstation. Het zijn de RF vermogensversterkers in deze systemen die als de meest energieverslindende elementen worden beschouwd en hierdoor een logisch onderwerp voor verbetering en wetenschappelijk onderzoek vormen.

Met deze achtergrond in gedachten zijn de belangrijkste doelstellingen van dit proefschrift gekozen, namelijk het verbeteren van de energie-efficiëntie en het verkleinen van de fysische afmeting van hoogvermogensversterkers in basisstations. Als focus voor dit proefschrift is het “outphasing” versterker concept gekozen, welke een hoog rendement, goede lineariteit en uitstekende mogelijkheden voor systeemintegratie biedt. Als dusdanig zijn diverse “outphasing” concepten bestudeerd op verschillende niveaus van abstractie, uitgaande van hun fundamentele werking, en zeer gedetailleerde efficiëntie / bandbreedte overwegingen. Om de toekomstige “overall” integratie van volledig RF zendversterkers / systemen mogelijk te maken zijn speciale ontwerptechnieken voor zeer compacte, magnetische componenten ontwikkeld die gebruik maken van goedkope draadbondtechnieken. Op basis hiervan is een RF transformator-concept geïntroduceerd voor toepassing in RF-versterkers, met zeer lage verliezen en goede hoge stroomeigenschappen, die zich eenvoudig laat schalen. Om de toepassing van deze magnetische componenten met lage verliezen in de praktijk te demonstreren, zijn twee zeer compacte hoogvermogen klasse-E versterkers geïmplementeerd en getest. Voortbouwend op deze resultaten is een van de belangrijkste demonstratie versterkers van dit proefschrift gerealiseerd, namelijk een "70W volledig behuizing geïntegreerde GaN outphasing versterker", die een opmerkelijke combinatie van hoge-efficiency, hoog-uitgangsvermogen en compactheid vertegenwoordigt. Tot slot, om de toekomstige integratie van geavanceerde “switch-mode outphasing” systemen in een enkele behuizing

te vereenvoudigen, is het ontwerp van HVCMOS aansturingsschakelingen besproken en gedemonstreerd. Deze op HVCMOS gebaseerde aansturingen kunnen de essentiële fysieke verbinding maken tussen de uiteindelijke vermogensversterker en de intelligentie van de voorafgaande TX-keten, die meestal wordt uitgevoerd in standaard CMOS-technologieën.

LIST OF PUBLICATIONS

Journal Papers

10. **D.A. Calvillo-Cortes**, M.P. van der Heijden, M. Acar, M. de Langen, R. Wesson, F. van Rijs, L.C.N. de Vreede, 'A Package-Integrated Chireix Outphasing RF Switch-Mode High-Power Amplifier," in *IEEE Transactions on Microwave Theory and Techniques,* vol. 61, no. 10, pp. 3721-3732, Oct. 2013.

Conference Papers

9. **D.A. Calvillo-Cortes** and L.C.N. de Vreede, "Analysis of Pure- and Mixed-Mode Class-B Outphasing Amplifiers," in *IEEE Latin American Symposium on Circuits and Systems (LASCAS) proceedings,* Feb. 2014.

8. **D.A. Calvillo-Cortes**, M.P. van der Heijden, L.C.N. de Vreede, "A 70W package-integrated class-E Chireix outphasing RF power amplifier," in *IEEE MTT-S International Microwave Symposium (IMS) Digest,* June 2013.

7. **D.A. Calvillo-Cortes**, K. Shi, M. de Langen, F. van Rijs, L.C.N. de Vreede, "On the design of package-integrated RF high-power amplifiers," in *IEEE MTT-S International Microwave Symposium (IMS) Digest,* June 2012.

6. **D.A. Calvillo-Cortes**, L.C.N. de Vreede, M. de Langen, "A compact and power-scalable 70W GaN class-E power amplifier operating from 1.7 to 2.6 GHz," in *Asia-Pacific Microwave Conference (APMC) proceedings,* pp. 1546-1549, Dec. 2011.

5. K. Shi, **D.A. Calvillo-Cortes**, L.C.N. de Vreede, F. van Rijs, "A compact 65W 1.7-2.3GHz class-E GaN power amplifier for base stations," in *European Microwave Conference (EuMC) proceedings* , pp. 1103-1106, Oct. 2011.

4. **D.A. Calvillo-Cortes**, L.C.N. de Vreede, M.P. van der Heijden, "A transformer for high-power RF applications using bondwires in parallel," in *European Microwave Conference (EuMC) proceedings,* pp. 103-106, Oct. 2011.

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2. **D.A. Calvillo-Cortes**, M. Acar, M.P. van der Heijden, M. Apostolidou, L.C.N. de Vreede, D. Leenaerts, J. Sonsky, "A 65nm CMOS pulse-width-controlled driver with 8Vpp output voltage for switch-mode RF PAs up to 3.6GHz," in *IEEE International Solid-State Circuits Conference (ISSCC) Digest of Technical Papers*, pp. 58-60, Feb. 2011.

Others

1. **D.A. Calvillo-Cortes**, M.P. van der Heijden, L.C.N. de Vreede, "Bond wire transformer," U.S. Patent Application 2012-0139640, filed December 2, 2011, and published June 7, 2012.

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