A Sub-1V, Micropower Bandgap Reference

by

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Abstract

Bandgap references are used in many ICs to produce 'stable' and 'temperature-independent' voltage. This thesis describes a sub-1V bandgap reference in 40 nm and 0.16μm CMOS technologies that is functional from $-40\,^{\circ}$C to $125\,^{\circ}$C. Traditionally, BJT based references are commonly used, but produce an output voltage of 1.2 V and are not suitable for supply voltages below 1 V. Previously area-intensive solutions that were based on resistive sub-divisions were used to realize sub-1V references. In this work, a compact and low power 'bandgap' reference was implemented in standard CMOS technology using a device known as a Dynamic Threshold MOSFET (DTMOST). 20 chips have been taped out in NXP 0.16μm CMOS technology (C14) and packaged in Ceramic DIL packages. A 3σ spread of 1.25% is observed. The chips work down to a supply of 0.9 V and occupy 0.05mm^2. Also, a prototype has been designed in a 40 nm CMOS process and post-layout simulations have been performed. The chip works down to a supply of 0.8 V and occupies 0.05mm^2. Simulated 3σ spread is 3.7%. The total current consumption for the chips in both technologies is less than 4μA in the worst case corners.

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Last but not the least; I owe everything to my parents. They have been the greatest gifts by God to me. To them, I dedicate this thesis!

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Chapter 1

Introduction

1.1 Motivation and Objectives

Bandgap references are ubiquitous in many electronic systems due to their (nearly) constant output voltages regardless of PVT (Process-Voltage-Temperature) variations. From a novel concept in the 60s and 70s ([7], [8], [9], [10]), the topic has evolved greatly leading to some outstanding designs in terms of very low spread between realized samples [11], low-supply voltage architectures [12] etc... Innovations are still rife in the field even after over four decades of research as evident by some excellent recent publications on compact sub-1V references [2] or references with extremely low temperature-coefficients [13].

An option for a circuit, that produces a stable voltage output, could be a non-linear voltage divider (see Fig. 1-1).

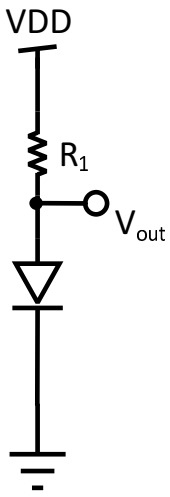


Figure 1-1: Basic Voltage Reference

In this case, the diode voltage is the output voltage. However, the diode voltage, V_{out} has a strong temperature dependence of about -2mV/°C and varies by hundreds of millivolts in the desired temperature range (−40 °C to 125 °C) [14].

A temperature-independent and stable voltage reference can be realized using a zener diode, biased in breakdown region, i.e at a reverse bias voltage greater than V_{br} when the voltage across the junction is constant over a large range of currents (see the current-voltage characteristic of a zener diode in Fig. 1-2).

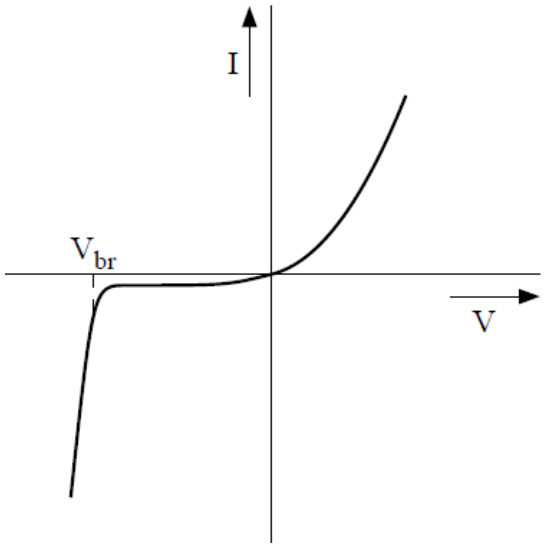


Figure 1-2: Current-voltage (I-V) characteristic of a zener diode [1]

The breakdown of a zener diode can occur via two kinds of mechanisms [1]:

- Avalanche breakdown: This type of breakdown occurs due to high electric fields. The charge carriers are accelerated in the presence of high electric field and ionize atoms. A larger number of charge carriers result, leading to a large current. The voltage due to avalanche breakdown has a positive temperature co-efficient. This is because with increased temperature, mobility of the charge carriers decreases and a higher electric field (and therefore, a higher voltage) is needed to effect the breakdown [1].
- Zener breakdown: Zener breakdown occurs at relatively lower voltages than avalanche breakdown. In [1], it is shown that at a lower breakdown voltage (than in the case of avalanche breakdown), separation W between conduction and valence bands reduces to a very small value (see Fig. 1-3). When W goes below a 'critical' value, charge carriers can tunnel through the bands, leading to zener breakdown. The voltage due to zener breakdown has a negative temperature co-efficient because the barrier width, W decreases with temperature [1].

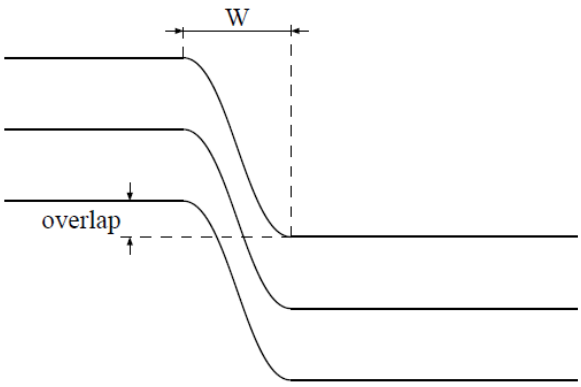


Figure 1-3: Band diagram with overlapping conduction and valence bands-zener breakdown [1]

If the zener diode is biased in such a way that zener and avalanche breakdown effects are equally significant, then a temperature -independent voltage can be realized. However, zener and avalanche breakdowns occur at 5-7 V [1]. Furthermore, deep buried zener diodes are not easily available in standard CMOS processes. Hence, references based on zener diodes have become quite obsolete and are also, not suitable for this work.

For lower supply voltages, a separate class of circuits called “bandgap references"[8] are used. In this class of circuits, the endeavour is to find two voltages having opposite temperature dependencies. In other words, if a voltage, V_{ptat}, with positive temperature dependence, and a voltage, V_{ctat}, with a negative temperature dependence, can be found; then a temperature-independent output voltage, V_{bg} could be obtained by appropriate signal processing (see Fig. 1-4).

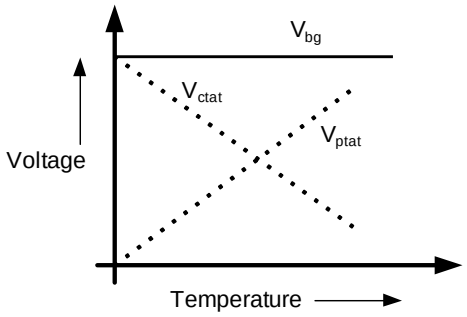


Figure 1-4: Obtaining a temperature-independent voltage source

For an ideal diode, the current I_{diode} is given by:

$$I_{diode} = I_s exp(\frac{V_{diode}}{kT/q}) \tag{1.1}$$

where, I_s is a process-dependent constant, called the saturation current, V_{diode} is the junction voltage across the diode, k is the Boltzmann constant ($1.38 * 10^{-23}$ J/K), T is the absolute temperature in Kelvin(K) and q is the electronic charge ($1.6 * 10^{-}19$ C). The voltage across a single diode V_{diode} is a CTAT quantity [14], [1]. Furthermore, if two diodes are biased with a current ratio of 1:N (for example-the ratio between I_1 and I_2 in Fig. 1-5) then (1.1) leads to :

$$V_{diode1} - V_{diode2} = \Delta V_{diode} = \frac{kT}{q} \ln N \tag{1.2}$$

Therefore, from (1.2), it is seen that an exponential current-voltage relationship helps to easily generate V_{ptat}. This, along with CTAT nature of the diode voltage V_{diode} [14], [1], indicates that devices with exponential current-voltage relationships can be used to realize a temperature-independent bandgap voltage by summing a V_{ctat} with an appropriately scaled V_{ptat} (see Fig. 1-5)

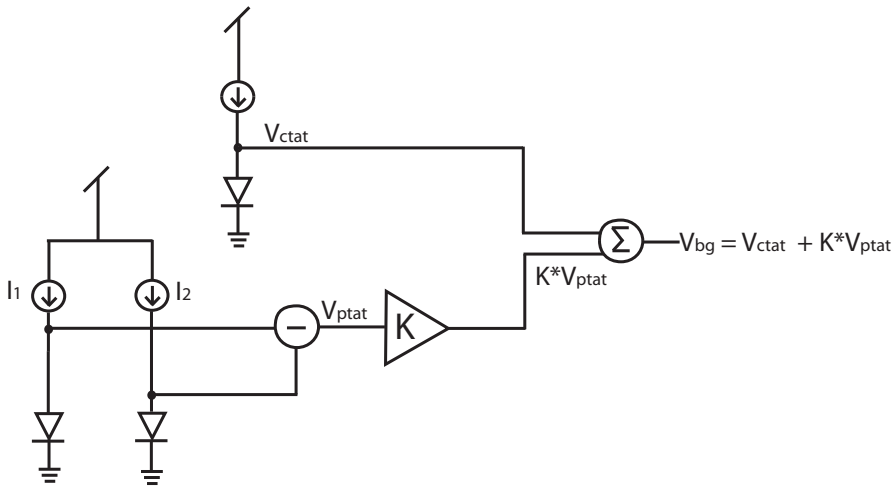


Figure 1-5: Principle of Bandgap Reference

Traditionally, designs have featured the use of BJTs because of their well-defined exponential current-voltage relationship [14]. Even for designs in CMOS processes, parasitic BJTs have been found to yield the best results [11]. However, with shrinking feature sizes, the use of traditional topologies becomes more and more difficult. The models for parasitic BJTs are not very well-defined in CMOS processes and the problem becomes more severe for lower feature sizes [15]. This leads to significant differences between the simulated results and actual silicon. But, perhaps the greatest issue with traditional BJT based references is that they produce an output voltage around the bandgap voltage of Silicon i.e, 1.2 V. However, with supply voltages going down to 1V and below in Deep Sub-Micron (DSM) technologies, these designs have become obsolete. Although current-mode references such as [12] produce lower output voltages, they tend to occupy a lot of area as they are mainly dependent on resistive divisions and therefore, need large resistors for implementation.

When operated in the sub-threshold region, standard MOSFETs also exhibit an exponential voltage-to-current behavior. As a result, they can also be used to realize "bandgap" voltage references. However, the resulting reference voltages are much less than the bandgap voltage of silicon. Hence, it is desirable to replace the BJTs by standard MOS transistors. Several attempts have been made in this regard to use MOSFETs in the sub-threshold region, but the results have been quite poor, compared to BJT based designs [16], [17], [18]. However, connecting the gate to the back-gate of a PMOS, leads to a new device called DTMOST (Dynamic Threshold MOSFET) [4]. The details of this device are discussed in Chapter 3. This device, when operated in weak inversion, has a near-ideal exponential current-voltage relationship, very similar to that of an ideal diode and produces a “bandgap" voltage of about 0.6V (half that of BJTs) [4].
Furthermore, results for bandgap reference [4] and temperature sensors have been published using DTMOSTs [15] that are comparable to state-of-the art bandgap references and temperature sensors using BJTs. This presents an excellent motivation to study the use of DTMOST for sub-1V Bandgap References. Other important goals are negligible power consumption and low silicon real estate.

Since the accuracy of a voltage reference depends on process spread, silicon validation is essential. In this work, the NXP 0.16 µm CMOS technology was chosen, since a DTMOST-based temperature sensor [15] was published with excellent temperature resolution. This was followed by demonstration of the feasibility of the approach in an advanced process like TSMC 40 nm CMOS. The key design goals are summarized in Table 1.1. It is pertinent to note that the reference is to be designed to drive a high-impedance load and hence, load regulation is not an important specification for this design.

Table 1.1: Main specifications for the Bandgap Reference

Parameter	Value
Output Voltage	~0.6-0.7V
Technology	Standard CMOS(0.16 µm, 40 nm)
Minimum Supply Voltage	< 1V
Temperature Range	$-40\,^{\circ}$C to $125\,^{\circ}$C
3σ spread	$< 5\%$
Temperature Drift	< 100 ppm/$\,^{\circ}$C
Current Consumption	< 5 µA at all corners
Active Area	$\leqslant 0.05\mathrm{mm}^2$

This thesis describes how a DTMOST based bandgap reference was implemented in CMOS technology. This has been demonstrated by a prototype, which will be described in Chapter 4. 20 chips have been taped out

in NXP 0.16μm CMOS technology (C14) and packaged in Ceramic DIL packages. A 3σ spread of 1.25% is observed. The chips work down to a supply of 0.9 V and occupy 0.05mm^2. Also, a prototype has been designed in a 40 nm CMOS process and post-layout simulations have been performed. The chips work down to a supply of 0.8 V and occupies 0.05mm^2. Simulated 3σ spread is 3.7%.

1.2 CMOS Bandgap References

Drawing on the basic principle of the bandgap references explained in the previous section, some of the following circuit topologies could be implemented in CMOS technology.

1.2.1 Classical Bandgap Reference

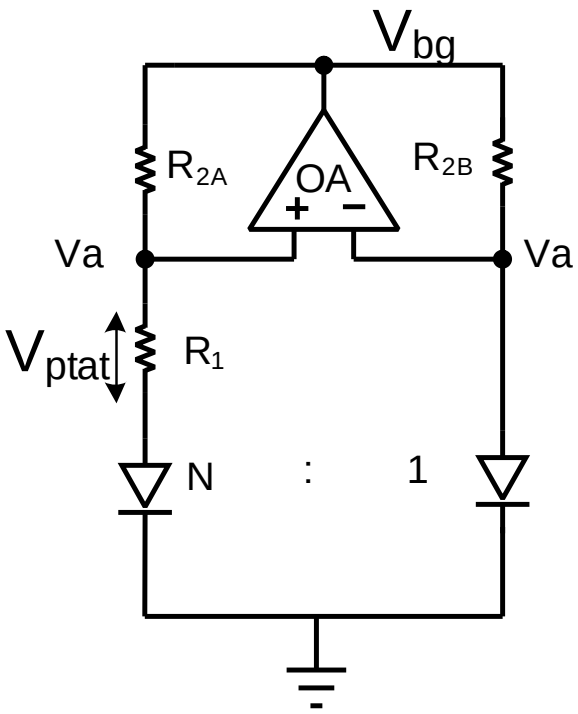


Figure 1-6: Classical Bandgap Reference. Note that the “diodes" are actually diode-connected PNPs.

Fig. 1-6 shows the most commonly used topology. The circuit's operation is based on the compensation of the base-emitter voltage of a BJT by a PTAT voltage. The base emitter voltage of a BJT is given by:

$$V_{be} = V_T \ln \frac{I_c}{I_s} \tag{1.3}$$

where V_T is the thermal voltage ($\approx$ 26 mV at room temperature), I_c is the collector current and I_s is the specific

current. The thermal voltage, V_T is given by:

$$V_T = \frac{kT}{q} \tag{1.4}$$

where k is the Boltzmann constant ($1.38 * 10^{-23}$ J/K), T is the absolute temperature in Kelvin(K) and q is the electronic charge ($1.6 * 10^{-}19$ C). The diode-connected BJTs are drawn as diodes in Fig. 1-6 and the subsequent figures in this dissertation. Matched resistors R_{2A} and R_{2B} force the same current through the diodes. The two diodes have different emitter areas, therefore they have different current densities and saturation currents. The difference between the two base-emitter voltages yields a PTAT voltage given by:

$$\Delta V_{be} = \frac{kT}{q} \ln N \tag{1.5}$$

$\frac{kT}{q}$ is the thermal voltage V_T and N is the ratio of the emitter areas of the two diodes. In Fig. 1-6, assuming a virtual ground at the op-amp input V_a :

$$V_{bg} = V_{be} + R_2 \times \frac{\Delta V_{be}}{R_1} = V_{be} + R_2 \times \frac{\frac{KT}{q} \ln N}{R_1} \tag{1.6}$$

Thus, by choosing appropriate values of R_1 and R_2, V_{bg} is the desired temperature-independent bandgap voltage. In CMOS technology, this value comes out to be close to 1.2 V, when using BJT diodes. Hence, the topology of Fig. 1-6 is not suitable for sub-1V supplies when using BJT diodes.

1.2.2 Sub-1V references

In 1999, a current-mode bandgap reference was reported in [12] that could function at sub-1V supplies. Consider the topology, reproduced in Fig. 1-7.

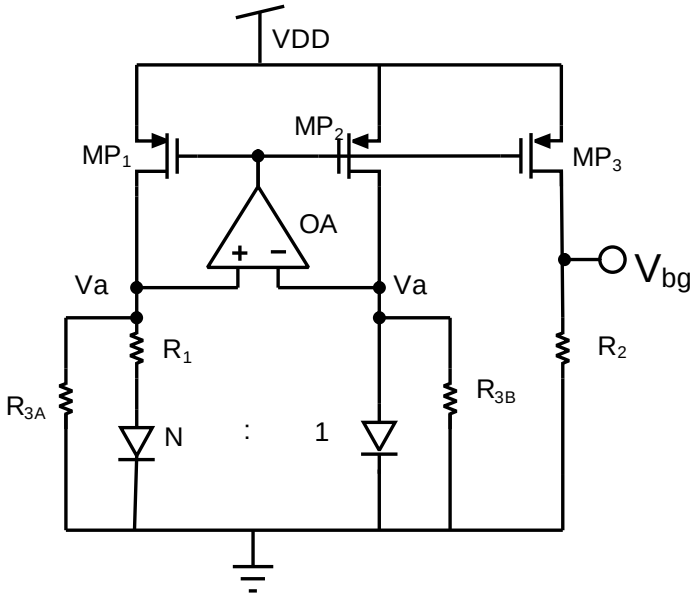


Figure 1-7: Current-Mode sub-1V reference

In Fig. 1-7, the PMOS current mirrors, MP_1, MP_2 and MP_3 have the same dimensions and therefore, carry the same current. The op-amp (OA) produces virtual ground at V_a. Thus, current across R_1 is PTAT given by $\frac{\Delta V_{be}}{R_1}$. Current through R_{3A} is CTAT given by $\frac{V_{be}}{R_3}$. Hence, the current through MP_1 and hence, MP_3 is a combination of a PTAT and a CTAT current. The Bandgap Voltage, V_{bg} is given by:

$$V_{bg} = R_2 \left(\frac{\Delta V_{be}}{R_1} + \frac{V_{be}}{R_3} \right) \tag{1.7}$$

Proper selection of R_1, R_2 and R_3 leads to a temperature-independent voltage that is much lower than 1.2 V and can be used with sub-1V supplies. However, large values of resistors (total resistance of about 5MΩ) were needed for this approach [12]. Hence, the above approach is not feasible for a small area reference, as targeted by this work.

Sub-1 V references could also be implemented using the so-called 'Reverse-Bandgap Approach' [19]. The topology is presented in Fig. 1-8

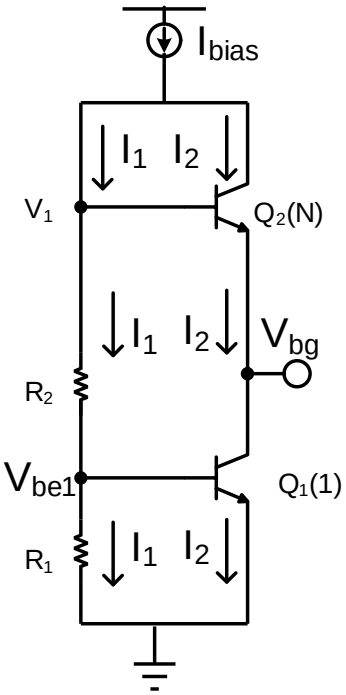


Figure 1-8: Reverse Bandgap Approach

Assuming, no base current in the npn transistors Q_1 and Q_2, it can be shown that:

$$V_{bg} = \Delta V_{be} + V_{be1}\frac{R_2}{R_1} \tag{1.8}$$

Thus, V_{bg} is a sub-1V reference. However, the error due to base-current becomes extremely large with the scaling down of technology [3]. Hence, the architecture of Fig. 1-8 is not very suitable, especially for implementation in an advanced technology node such as TSMC 40 nm, as desired in this dissertation. Furthermore, the required NPNs are not commonly available in CMOS processes.

MOSFETs biased in weak inversion can also be used to generate sub-1V references. One possible architecture was presented in [17].

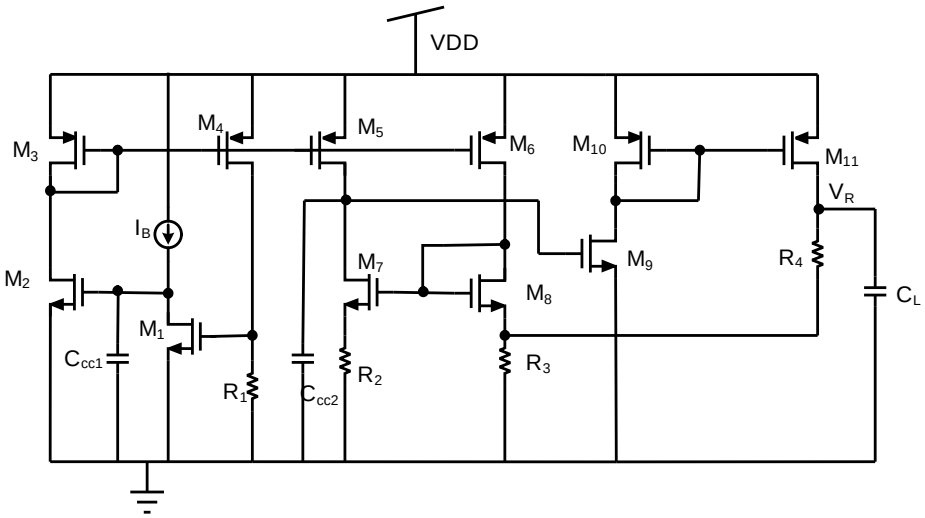


Figure 1-9: Sub-1V Bandgap Reference based on MOSFETs biased in weak inversion

The transistors, M_1-M_4, bias I_B, resistor R_1 and compensation capacitor C_{C1} set the current across R_1 ,I_{R1} to be dependent on V_{GS1} , which is a CTAT quantity. This CTAT current is mirrored on to the rest of the circuitry through M_5 and M_6. The reference V_R can be given as [17]:

$$V_R = \alpha V_{GS1} + \beta \frac{kT}{q} \tag{1.9}$$

where $\alpha = \left(\frac{R_4}{R_3} + 1\right) \frac{R_2}{R_1} \frac{S_5}{S_4} - \frac{R_4}{R_1}$ and $\beta = \left(\frac{R_4}{R_3} + 1\right) \ln \frac{S_8}{S_7} \frac{S_5}{S_4}$ In the above definitions, S refers to the aspect ratio $\frac{W}{L}$ where W and L are the gate width and length, respectively of the MOSFET. Proper selection of the resistors and transistor sizes can make V_R temperature-independent by making the temperature dependence of α and β to cancel out. The architecture of [17] was designed for a supply of 1.2 V but with lower threshold voltages can lead to sub-1V operation. However, the need of large compensation capacitors C_{C1} and C_{C2} (total of about 35pF) do not make this a suitable architecture for a compact reference targeted in this work.

In 2012, a novel approach for a sub-1V Bandgap reference was published in [2]. The topology is presented in Fig. 1-10.

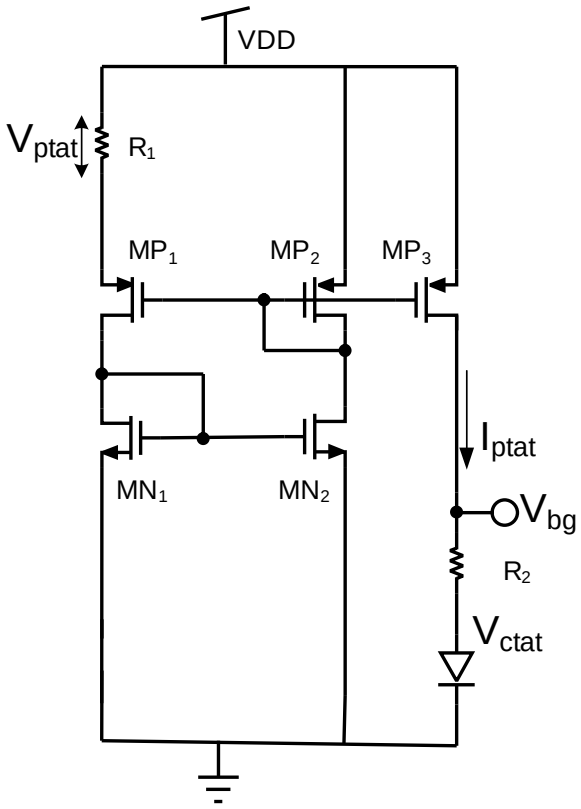


Figure 1-10: Sub-1V Bandgap Reference based on fixed threshold voltage difference between MOSFETs having different gate lengths and biased in weak inversion.

The key idea is to reduce the bandgap voltage by adding a scaled down version of V_{ptat} to V_{ctat}. It was shown in [2] that biasing, MP_1 and MP_2 in weak inversion,leads to a PTAT voltage over R_1. In addition, the gate lengths of MP_1 and MP_2 can be chosen such that MP_1 and MP_2 have a fixed threshold voltage difference over temperature(see Fig. 1-11).

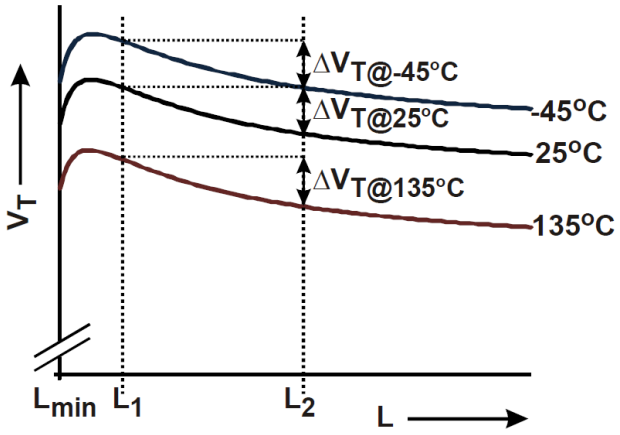


Figure 1-11: Threshold voltage (V_T) dependence of a PMOS at three different temperatures: Using a current mirror with lengths L_1 and L_2 leads to an almost temperature-independent offset in difference between the threshold voltages (ΔV_T) [2]

Consequently, V_{ptat} has a fixed temperature-independent offset from V_{ptat} that would be generated with same gate lengths for MP_1 and MP_2. Hence, this scaled-down version of V_{ptat} can be used to cancel out the negative temperature dependence of a BJT diode but with a smaller bandgap reference voltage V_{bg}. This is because V_{bg} is the sum of same V_{ctat} as a traditional reference and a lower V_{ptat} than a traditional reference(see Fig. 1-11). In the target 0.16 µm process, and without trimming, this reference achieved a 3 σ spread of 2.52 %.

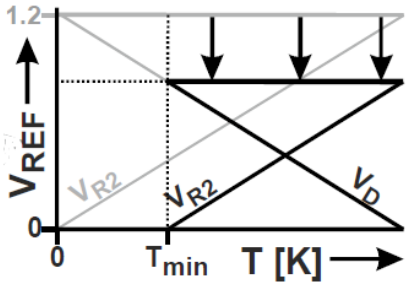


Figure 1-12: Principle of the sub-1V reference. A scaled down version of V_{ptat} (shown in the figure as V_{R2}) is added to a V_{ctat} (shown in the figure as V_D) to generate a “bandgap" voltage, V_{bg} (shown in the figure as V_{REF}) [2]

In Fig. 1-10, the mirrored PTAT current (through MP_3) is used to bias a BJT diode and generate the temperature-independent V_{bg} with proper choice of R_1 and R_2. However, this yields a V_{bg} of about 900mV in order to work down to −40 °C and hence, is not suitable for operation below a supply voltage of about 950mV. Hence, the solution would lie in developing a different topology or moving away from BJT diodes for this

implementation. The choice of the diodes is discussed in Chapter 2 and the used topology explained in Chapter 3.

1.3 Organization of the Thesis

This thesis discusses the implementation of a sub-1V bandgap reference. The motivation behind the work, desired performance specifications and some of the fundamental theory behind Bandgap References were discussed in this Chapter.

Chapter 2 focusses on the rationale behind the choice of the DTMOST diodes. The current-voltage characteristics of different suitable diodes are analyzed.

Chapter 3 presents the topology for the Bandgap Reference that was implemented. The rationale behind some of the architecture choices are discussed, along with an analysis of the various error sources present in the architecture.

Chapter 4 focusses on the implementation details of the design. The various design choices are discussed. The results of the taped out chip in C14 and the post-layout simulation results of the 40 nm chip are presented, along with a comparison with some of the existing literature.

Finally, the conclusions and recommendations for future work are presented in Chapter 5.

Chapter 2

Choice of diode-connected transistors

2.1 Overview

In the previous chapter, some state-of-the art bandgap references were discussed. It was shown that for a bandgap reference, diode-connected transistors (hereafter, referred to as diodes) are needed to have a CTAT characteristic. Moreover, the difference between the diode voltages should have a PTAT characteristic. These considerations lead to the circuit of Fig. 2-1, which will be used as the standard bandgap reference for the discussions in this chapter.

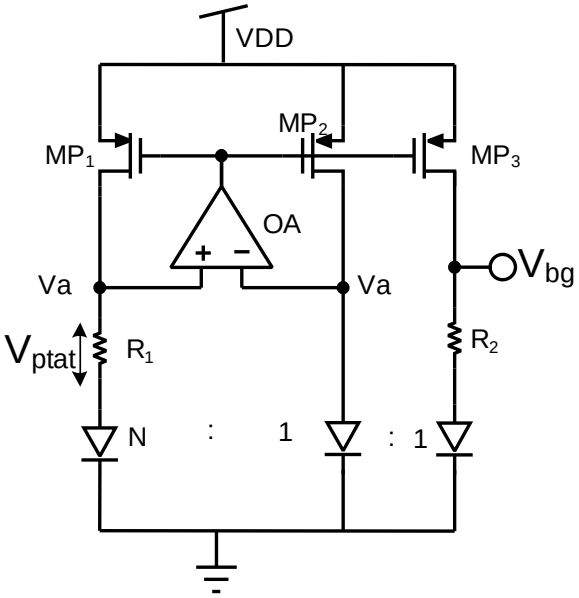


Figure 2-1: Representative Bandgap Reference

In Fig. 2-1, the PMOS current mirrors, MP_1, MP_2 and MP_3 have the same dimensions and therefore,

carry the same current. The op-amp (OA) produces virtual ground at V_a. Thus, current across R_1 is PTAT given by $\frac{\Delta V_{be}}{R_1}$. Current through MP_2 is therefore, PTAT. Hence, the voltage V_{bg} is given by:

$$V_{bg} = V_{diode} + \frac{R_2}{R_1}\frac{kT}{q}\ln N \tag{2.1}$$

With V_{diode} being a CTAT voltage and $\frac{kT}{q}\ln N$ being a PTAT voltage, proper selection of R_2 and R_1 makes V_{bg} a temperature-independent bandgap voltage. It is pertinent to note that the circuit of Fig. 2-1 has an high output impedance and cannot be used to drive low impedance loads. However as stated in Chapter 1, driving a low impedance load is not the focus of this work. The selection of the diodes (with the area ratio N:1:1) in Fig. 2-1 is the topic of discussion in this Chapter. The following choices exist in standard CMOS technology for the implementation of diodes:

- Lateral and Substrate Bipolar Junction Transistors (BJTs).
- MOSFET biased in weak inversion.
- Dynamic Threshold MOSFET Transistors (DTMOSTs) biased in weak inversion.

2.2 Lateral and Substrate BJTs

In single n-well technologies, only PNP BJTs are available. These come in two varieties -substrate and lateral. Fig. 2-2 shows the two types of BJTs. The substrate BJT is shown in grey and the lateral BJT is shown in black. In [3], it was shown that the substrate BJTs are preferred due to their insensitivity to packaging stress

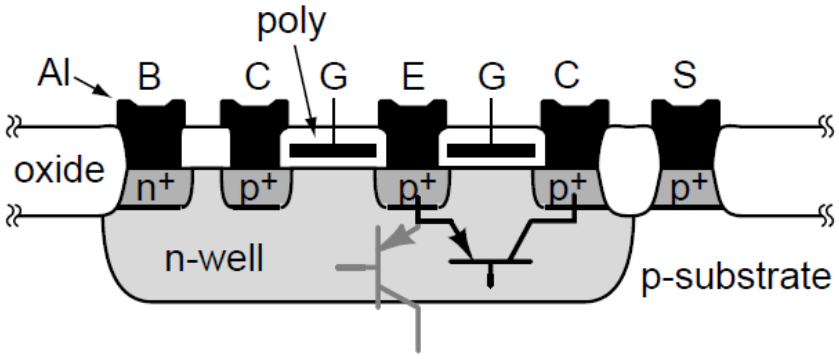


Figure 2-2: Parasitic BJTs [3]

and lower spread compared to lateral BJTs. The collector of the BJT is actually the substrate and is connected to ground. It is known [14] that :

$$V_{be} = V_T \ln \frac{I_c}{I_s} \tag{2.2}$$

where I_c is the collector current and I_s is the saturation current, given as :

$$I_s = bT^{4+m} exp\left(\frac{-E_g}{kT}\right) \tag{2.3}$$

where b and m are proportionality constants and E_g is the bandgap energy of silicon (1.2 eV). Differentiating V_{be} with respect to temperature yields (assuming constant I_c):

$$\frac{\partial V_{be}}{\partial T} = \frac{\partial V_T}{\partial T} \ln \frac{I_c}{I_s} - \frac{V_T}{I_s} \frac{\partial I_s}{\partial T} \tag{2.4}$$

Now,

$$\frac{\partial I_s}{\partial T} = b\,(4+m)\,T^{3+m} exp\left(\frac{-E_g}{kT}\right) + bT^{4+m} exp\left(\frac{-E_g}{kT}\right) \frac{E_g}{kT^2} \tag{2.5}$$

Therefore,

$$\frac{\partial V_{be}}{\partial T} = \frac{V_{be} - (4+m)\,V_T - E_g/q}{T} \tag{2.6}$$

Thus, V_{be} has a negative slope with temperature and is hence, CTAT. In the first order approximation, this dependence can be considered to be linear with a slope of about -2 mV/K. Assuming the same collector current, I_c, same saturation current, I_s (technology constant) and ratio 1:N between diodes (e.g in Fig. 2-2), the difference between the diode voltages is given by :

$$V_{be2} - V_{be1} = \Delta V_{be} = V_T \ln N \tag{2.7}$$

Since V_T is equal to $\frac{kT}{q}$, the voltage ΔV_{be} is PTAT in nature. Thus, both PTAT and CTAT voltages can be obtained by the BJT diodes. Therefore, it can be seen that for the circuit of Fig. 2-1 to work, the diodes must have an exponential current-voltage relationship:

$$I \propto exp\left(\frac{V_{diode}}{V_T}\right) \tag{2.8}$$

After matching the slopes of the PTAT and CTAT voltages in the first order, the bandgap voltage is approximately equal to E_g , which is equal to about 1.2 V [14]. Thus, BJT diodes cannot be used in the bandgap reference of Fig. 2-2 for a sub-1V supply voltage, which was the primary goal of this work. Hence, parasitic BJTs are ruled out as the diodes.

2.3 Subthreshold MOSFET

The "ideal" model of a MOSFET [14] is that it starts conducting only when the magnitude of the gate-source voltage is greater than or equal to the magnitude of the threshold voltage:

$$|V_{gs}| \geqslant |V_{th}| \tag{2.9}$$

This is based on the assumption that the inversion charge, Q_I goes to zero for gate voltages below the threshold voltage. However, Q_I does not go to zero , but becomes a small quantity varying exponentially with gate voltage. Thus, a small drain current flows for $|V_{gs}| < |V_{th}|$. This region of operation of a MOS transistor is known as the weak-inversion or sub-threshold region. In weak inversion, the drain-current is an exponential function of V_{gs}, given by:

$$I_{ds} = \mu C_{ox} \frac{W}{L} (m-1) V_T^2 exp\left(\frac{V_{gs} - V_{th}}{mV_T}\right)\left(1 - exp\left(\frac{-V_{ds}}{V_T}\right)\right) \tag{2.10}$$

where I_{ds} is the drain current, μ is the carrier mobility, C_{ox} is the gate-oxide capacitance, V_{gs} is the gate-source voltage,V_{ds} is the drain-source voltage, V_{th} is the threshold voltage and V_T is the thermal voltage ($\frac{kT}{q}$). The parameter $m = 1 + \frac{C_D}{C_{ox}}$ is the body-effect coefficient an C_D is the depletion capacitance[15]. The factor $\mu C_{ox} \frac{W}{L}$ is also known as the transconductance coefficient(β) and μC_{ox} is known as the unit transconductance coefficient($\beta_\square$).

Thus, for $V_{ds} > 4V_T$, the drain current reduces to :

$$I_{ds} \propto exp\left(\frac{V_{gs}}{mV_T}\right) \tag{2.11}$$

Therefore, a MOSFET biased in weak inversion has an exponential current-voltage relationship. Thus, the difference between two PMOS diodes (in weak inversion), which are biased at the same drain current and have size ratio N is PTAT :

$$\Delta V_{gs} = m\frac{kT}{q} lnN \tag{2.12}$$

The CTAT nature of V_{gs} is shown in [17]. For $V_{ds} > 4V_T$,

$$I_{ds} \simeq Xexp\left(\frac{\phi_s - 2\phi_B}{V_T}\right) \tag{2.13}$$

where X is a constant, ϕ_s and ϕ_B are the surface and bulk potentials, respectively. Also,

$$I_{ds} \simeq Xexp\left(\frac{V_{gs} - V_{th} - V_{OFF}}{mV_T}\right) \tag{2.14}$$

where V_{OFF} is a correction constant in the BSIM model. Therefore,

$$\left(\frac{V_{gs} - V_{th} - V_{OFF}}{mV_T}\right) = \left(\frac{\phi_s - 2\phi_B}{V_T}\right) \tag{2.15}$$

Also,

$$\phi_s(T) - 2\phi_B(T) = [\phi_s(Tr) - 2\phi_B(Tr)]\frac{T}{Tr} \tag{2.16}$$

where Tr is a reference temperature. Therefore,

$$V_{gs}(T) = V_{th}(T) + V_{OFF} + \frac{m(T)}{m(Tr)}\left[V_{gs}(Tr) - V_{th}(Tr) + V_{OFF} + \frac{m(T)}{m(Tr)}\right]\frac{T}{Tr} \tag{2.17}$$

Assuming m does not vary significantly with temperature and temperature dependence of the threshold voltage, V_{th} can be modeled by

$$V_{th}(T) = V_{th}(Tr) + K_T\left(\frac{T}{Tr} - 1\right) \tag{2.18}$$

where $K_T < 0$. Hence, V_{gs} is given by

$$V_{gs}(T) \simeq V_{gs}(Tr) + K_G\left(\frac{T}{Tr} - 1\right) \tag{2.19}$$

K_G is given by

$$K_G = K_T + V_{gs}(Tr) - V_{th}(Tr) - V_{OFF} \tag{2.20}$$

For typical values of these quantities, K_G is negative [17] and hence, V_{gs} decreases with temperature (CTAT quantity). Also, the obtained “bandgap" voltage is about half than in the case of BJT (0.6V) [4]. Hence, MOSFETs biased in weak inversion are a suitable choice for diodes with sub-1V supply. An important figure-of-merit for a sub-threshold MOSFET is its sub-threshold swing, S (mV/decade) [20]. It can be defined as

$$S = \frac{\partial V_{gs}}{\partial \log I_{ds}} = mV_T \ln(10) \tag{2.21}$$

The sub-threshold slope is different from the ideal value of 60 mV/decade which corresponds to the pure exponential relationship with half slope for BJT [20]. More significantly, m is a function of the depletion capacitance; thus, it varies greatly with process. So in general, MOSFET based references have much greater spread than corresponding BJT based references. Hence, using PMOS diodes would lead to large spread in the bandgap reference and is hence, not desirable.

2.4 Sub-Threshold DTMOST

Annema [4] used MOSFETs connected in a different fashion to obtain the diodes for a bandgap reference. This device is a traditional PMOS transistor with its gate and back-gate (bulk) tied together. Such a device

is called a Dynamic Threshold MOSFET (DTMOST). The inter-connection of gate and back-gate causes the threshold voltage to vary dynamically, and hence, the name DTMOST[15]. Fig. 2-3 shows the cross-section of a normal DTMOST transistor.

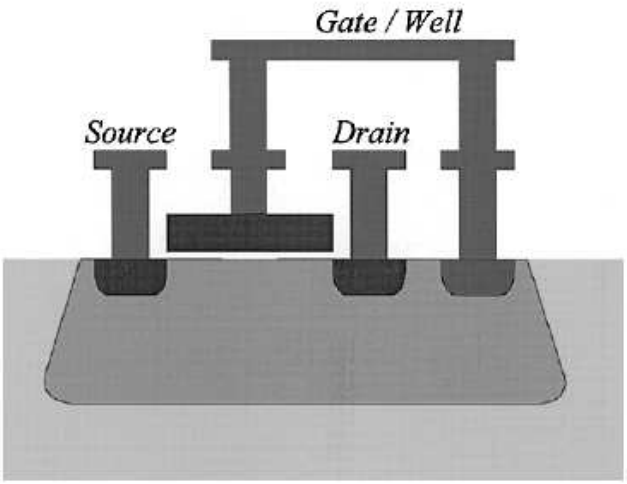


Figure 2-3: Cross Section of a DTMOST[4]

The schematics of DTMOST and DTMOST diodes are shown in Fig. 2-4.

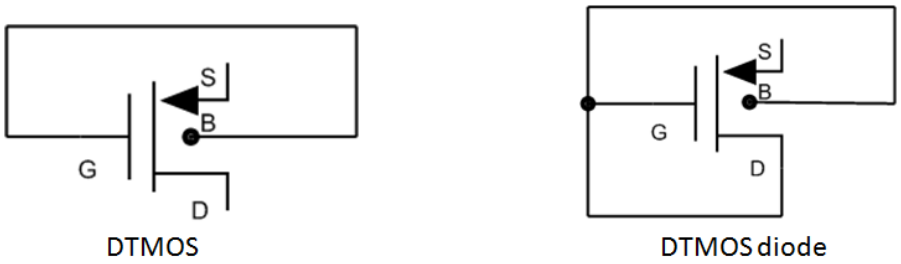


Figure 2-4: Schematic of DTMOST and DTMOST diode

The depletion layer is fixed in case of a DTMOST. It was shown in [5] that a DTMOST has ideal sub-threshold swing of 60 mV/decade. Consider the band bending illustrated in Fig. 2-5 [5]. It is seen that the band-bending ψ_s^0 (also sometimes called ϕ_s) and depletion layer width w_0 are fixed in DTMOST.

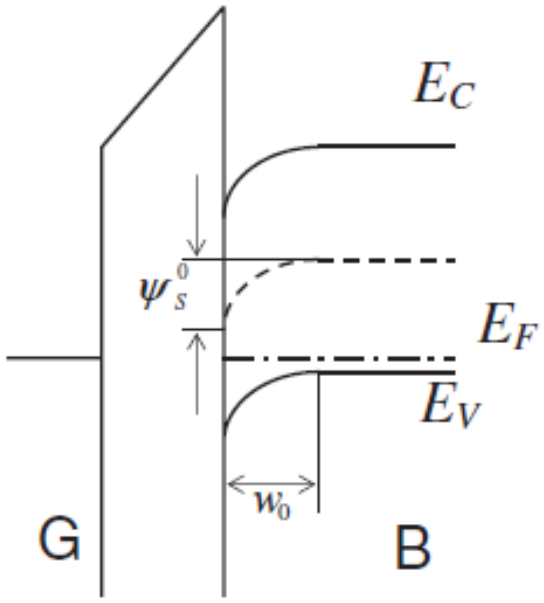


Figure 2-5: Band Bending in DTMOST device. ψ_s^0 is the surface potential and w_0 is the width of depletion region [5]

Therefore, the surface potential change $\Delta\psi_s$ is equal to V_{gs}. Furthermore, the depletion layer is fixed and the sub-threshold swing is given by [5]

$$S = V_T \ln(10) \tag{2.22}$$

There is no dependence on the depletion capacitance C_D. Hence, the spread due to process and mismatch is expected to be much less for DTMOST diodes than PMOS diodes. Indeed, it was observed in [4] that spread in DTMOST diodes is less than that of PMOS diodes by a factor of about two. Furthermore, it was shown in [4] that a DTMOST can be viewed as a lateral PNP BJT with an extra gate over its base. The applied "V_{be}" is increased due to this 'gate-base' built-in voltage. This derivation is repeated here. If the built-in potential between the P-type gate and N-well is expressed as ϕ_{GW}, the drain current in a DTMOST, I_D is given by:

$$I_D = I_o T^{\eta} \exp\left(\frac{q(V_{gs} + \phi_{bl} - E_{g,0})}{kT}\right) \tag{2.23}$$

where I_o and η are process-dependent constants, T is the temperature, q is the electronic charge, V_{gs} is the applied gate-source voltage and $V_{bg,0}$ is the material bandgap voltage of silicon (1.2V). The barrier lowering voltage, ϕ_{bl} is given by the capacitive division of the built in voltage between the gate oxide and silicon as:

$$\phi_{bl} = \frac{\phi_{GW} C_{ox}}{C_{ox} + C_D} \tag{2.24}$$

Where C_{ox} is the oxide capacitance and C_D is the depletion capacitance. The observed “bandgap" voltage is given by:

$$V_{bg} = V_{bg,0} - \phi_{bl} \tag{2.25}$$

Hence, the obtained “bandgap" voltage is less than the material bandgap of silicon. This “bandgap" voltage is found [4] to be about 0.6 V and the slope of V_{gs} with temperature is about -1mV/K (half that in the case of BJT diodes).

2.5 Summary

The key conclusions of this Chapter are summarized below:

- Diodes with exponential current-voltage relationships are needed for bandgap references.
- Substrate PNP BJTs fit the description and have been widely used in literature. However, they lead to a bandgap voltage of about 1.2 V and cannot be used for sub-1V supplies, using traditional architectures such as Fig. 2-1.
- PMOS transistors biased in weak inversion show an exponential I-V characteristic with a “bandgap" voltage of 0.6 V. However, they spread significantly compared to BJTs.
- PMOS diodes, with gate connected to back gate, lead to a new device called the DTMOST. A DTMOST has a more ideal sub-threshold characteristic than its PMOS counterpart. Its spread is much reduced and the “bandgap" voltage obtained is about 0.6 V. This makes DTMOST diodes most suitable for development of sub-1V “bandgap" references. Such DTMOST diodes were used for the implementation in this work.

Chapter 3

A Sub-1V, Micro power Bandgap Reference

3.1 Overview

Some common bandgap references were discussed in Chapters 1 and 2. One key similarity between most of these architectures was the presence of an op-amp to create a virtual ground. However, this type of implementation leads to extra branch (es) for current consumption (in the op-amp) along with the branch(es) for the diodes. An op-amp less topology is described in this chapter that eliminates the extra branch, thereby reducing the power consumption. This is followed by a discussion of the required current mirrors and the different error sources associated with them as well as the error sources in the “bandgap" topology.

3.2 PTAT generator

As discussed in Chapter 1, a bandgap reference consists of a PTAT voltage and a CTAT voltage. This section focuses on the development of the circuit to generate the PTAT voltage (and current).

3.2.1 Op-Amp based PTAT generator

Fig. 3-1 shows the traditional op-amp based PTAT generator.

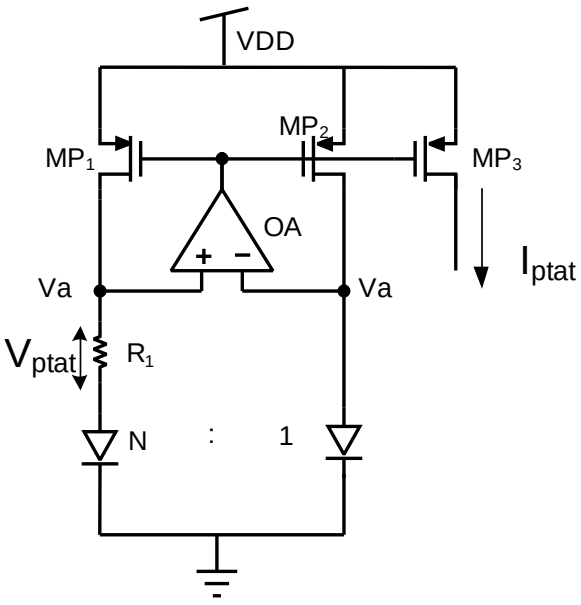


Figure 3-1: Op-Amp Based PTAT generator

The op-amp (OA) establishes a virtual ground at its inputs (V_a). The current mirrors MP_1 and MP_2 (1:1 ratio) ensure that the two diodes are biased at the same current. Given that the diodes have a size ratio N:1 as shown in Fig. 3-1, a voltage (ΔV_{gs}) is observed across the resistor R_1. It has been shown in Chapter 2 that ΔV_{gs} is a PTAT voltage. Thus, the voltage across the resistor R_1 is PTAT in nature. The PTAT current flows through both diodes and the current mirror (MP_1-MP_2) and can be mirrored out as shown in Fig. 3-1.

It is pertinent to note here that in Fig. 3-1, the feedback signal produced by the op-amp returns to both its inputs. The negative feedback factor is given by:

$$\beta_N = g_{mp}(R_1 + R_x) \tag{3.1}$$

The positive feedback factor is given by:

$$\beta_P = g_{mp}R_x \tag{3.2}$$

In (3.1) and (3.2), g_{mp} is the transconductance of MP_1 and MP_2 and R_x is the dynamic resistance of both diodes (biased by current, I) given by:

$$R_x = \frac{1}{g_m} = \frac{mV_T}{I} \tag{3.3}$$

where g_m is the transconductance of the DTMOST diode. Clearly, β_N is greater than β_P. However, there are some issues with this op-amp based topology. At low supply voltages, a two-stage opamp topology maybe required, leading to extra bias current. Furthermore, the op-amp will typically require its own biasing network

and the current through the op-amp stages cannot be used to bias the DTMOST 'diodes'. This leads to extra power consumption and hence, it is desirable to eliminate the op-amp from the PTAT generator.

3.2.2 Opamp-less PTAT generator

To mitigate the problems of op-amp based generators, the topology of Fig. 3-2 can be used.

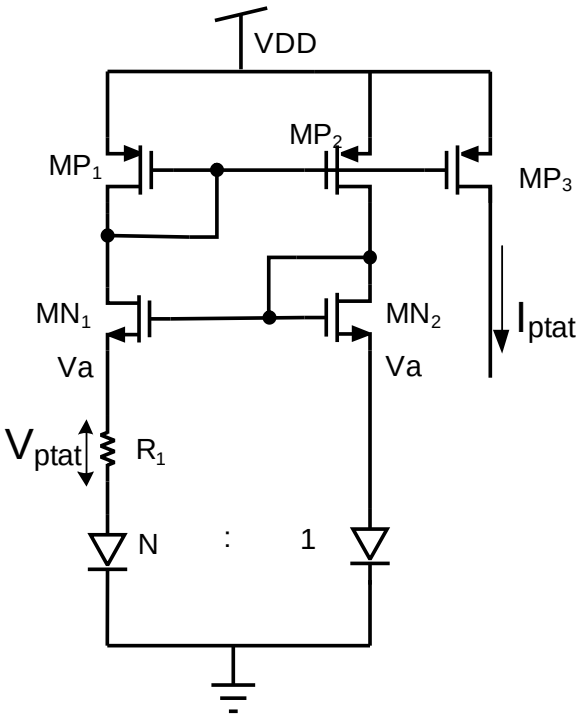


Figure 3-2: Opamp-less PTAT generator

In Fig. 3-2, MP_1-MP_2-MN_1-MN_2 form a self-biased differential common gate amplifier [6]. The amplifier formed by MP_1-MP_2-MN_1-MN_2 creates a virtual short between the nodes V_a. The source of MN_1 acts as non-inverting input node and the source of MN_2 acts as the inverting input node. The drain of MP_1 is the non-inverting output node and that of MP_2, the inverting output node. It does not require a separate biasing block or second stage and also shares the biasing current with the diodes; therefore, it consumes less power than the topology in Fig. 3-1. However, due to channel-length modulation in the PMOS current mirrors, the currents in the two branches are not equal. Furthermore, there is a significant voltage offset at the virtual ground, V_a due to mismatch between MN_1-MN_2 and MP_1 and MP_2. It is shown in [6] that the current mismatch between the current mirrors and voltage offset at the virtual ground, V_a are strong functions of the supply, VDD and thus, the PSRR of Fig. 3-2 is quite poor. A possible solution is to reduce these mismatches by helping the current mirrors with negative feedback as shown in Fig. 3-3 to keep the current mirroring transistors at the same (similar) V_{ds}. The working of the feedback loop can be explained as follows. Suppose

the voltage at the drain of MP_1 (positive output node) increases a little, the amplifier formed by MP_5 and R_{load} works on this increased small signal voltage and this is applied to the gate of MN_2. Consequently, the drain of MN_2 (and MP_2) has an increase in small-signal voltage. This leads to an increase in the small-signal gate voltage of MP_2 and hence that of MP_1. This pulls back the drain voltage of MP_1. Hence, the negative feedback ensures the same drain voltage for MP_1 and MP_2. This ensures the same current between MP_1 and MP_2. The gain for the negative feedback between the drain nodes of MP_1 and MP_2 can be given by:

$$\beta \simeq (-g_{mp5}R_{load})\left(\frac{g_{mn2}}{1+g_{mn2}R_x}\left[r_{dsn2} \parallel \frac{1}{g_{mp2}}\right]\right) \tag{3.4}$$

g_{mp} are the transconductances and r_{ds} are the drain resistances of the MOSFETs (with subscript p and n for PMOS and NMOS).

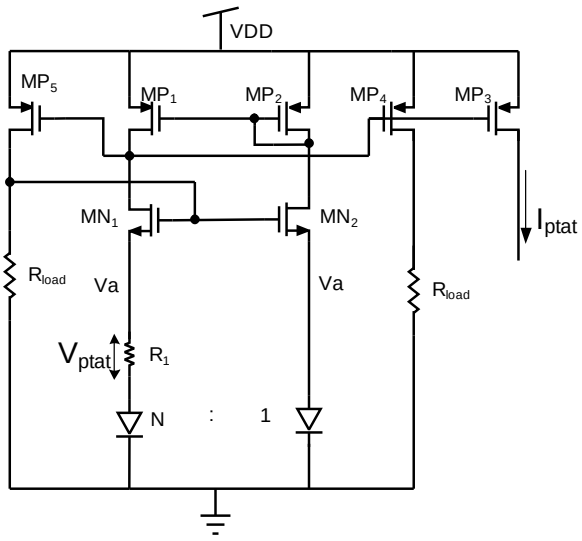


Figure 3-3: Helping the current mirrors with negative feedback

In Fig. 3-3, there are both positive and negative feedback paths to the input of the overall amplifier (at the source of MN_1 and MN_2). The overall negative feedback should be greater than the overall positive feedback for proper functioning of the amplifier. .It can be shown that :

$$\beta_N \simeq g_{mp5}R_{load}\frac{g_{mn}(R_1+R_x)}{1+g_{mn}(R_1+R_x)}. \tag{3.5}$$

$$\beta_P \simeq g_{mp5}R_{load}\frac{g_{mn}R_x}{1+g_{mn}R_x}. \tag{3.6}$$

Thus, negative feedback factor (β_N) is greater than the positive feedback factor (β_P). However, there is an extra branch for the negative feedback and this leads to extra current consumption. The current can be reused to bias the diodes as in Fig. 3-4. However, since V_a is at a larger voltage than ground, a smaller value of R_{load} is required than in Fig. 3-3 for the same current consumption in the amplifier branch (same g_{mp5}). This leads

to reduced loop gain (due to reduced β) and hence, reduced PSRR.

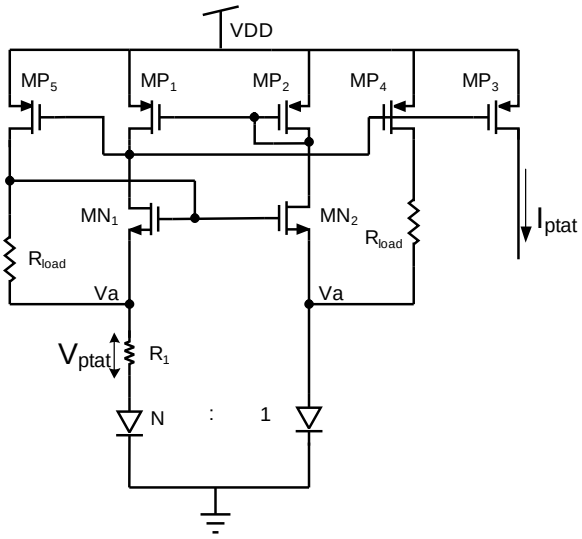


Figure 3-4: Reusing the current to bias the diodes [6]

To solve this problem, the loop gain can be increased by introducing cross-coupling (Fig. 3-5) [6].

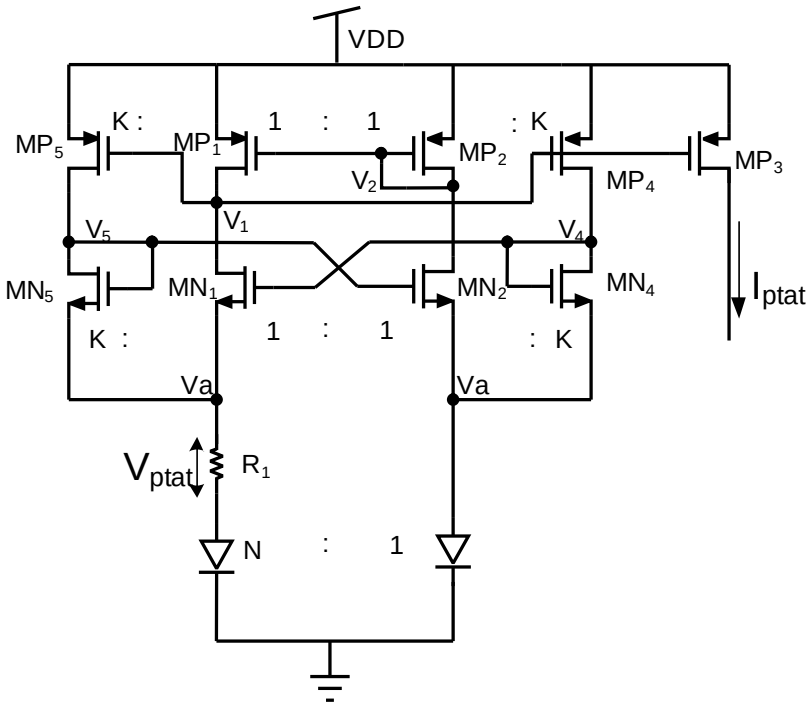


Figure 3-5: Cross-Coupling to increase the loop gain [6]

The resistive load, R_{load} is replaced by a diode load in Fig. 3-5. Furthermore, as stated, cross-coupling (or positive feedback) improves the loop gain. Symmetry and feedback ensures that $V_1 = V_2$ and $V_5 = V_4$

to ensure proper gate drive for MP_4. Moreover, the transistor pairs MP_4-MP_5, MP_1-MP_2, MN_4-MN_5 and MN_1-MN_2 are well-matched. The overall negative feedback is given by:

$$\beta_N \simeq g_{mp4}(\frac{1}{g_{mn4}} + R_1 + R_x)\frac{g_{mn1}(R_1 + R_x)}{1 + g_{mn1}(R_1 + R_x)} \tag{3.7}$$

And the overall positive feedback is given by:

$$\beta_P \simeq g_{mp5}(\frac{1}{g_{mn5}} + R_x)\frac{g_{mn2}R_x}{1 + g_{mn1}R_x} \tag{3.8}$$

Since g_{mn5} =g_{mn4}, g_{mp1} =g_{mp2} and g_{mn1} =g_{mn2}, β_N is much greater than β_P. Another important thing to note is the ratio K between the current mirrors in the primary amplifier and the feedback branches. If the generator consumes the same total current with K=1 and K $>$ 1 , it is shown in [6] that the PSRR is better for increased value of K as the output resistance of the PMOS MP_1 and MP_2, r_{dsp} increases by a factor of K+1 (due to decrease in drain current by the same factor) and PSRR increases with increased value of r_{dsp}.

3.3 Bandgap Reference

A bandgap reference consists of a PTAT voltage compensating a CTAT voltage to generate a temperature-invariant voltage. The generation of the PTAT voltage was discussed in detail in the previous section. From there, it is simple to obtain the bandgap voltage. Consider Fig. 3-6 generated from Fig. 3-5. The PTAT current generated is mirrored by the PMOS MP_3. This PTAT current is used to bias another DTMOST diode. It was shown in Chapter 3 that the V_{gs} of a DTMOST diode is CTAT in nature. This is shown as V_{ctat} in Fig. 3-6. The voltage V_{bg} is given by:

$$V_{bg} = V_{ctat} + \frac{R_2}{R_1}V_{ptat} \tag{3.9}$$

. Thus, with proper selection of R_2, V_{bg} is the desired bandgap voltage.

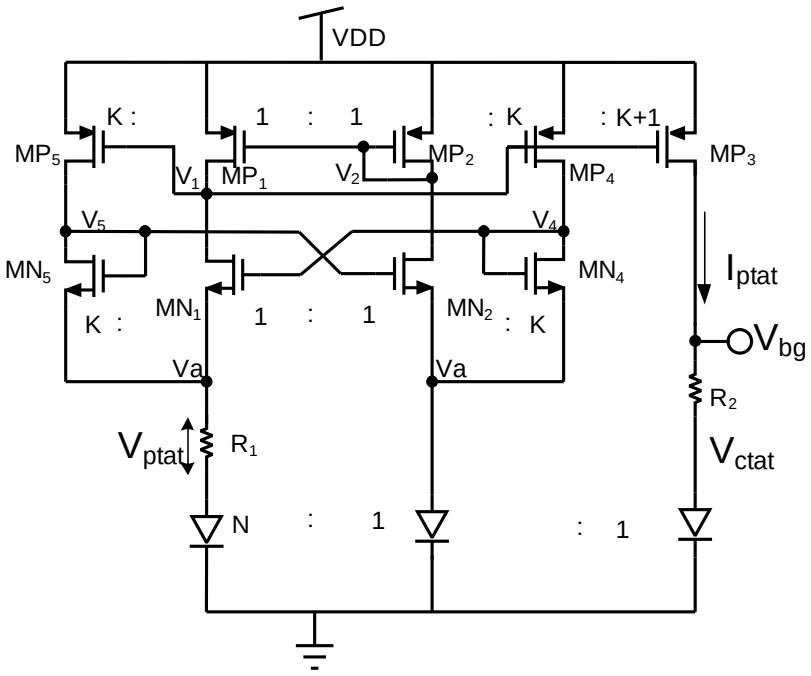


Figure 3-6: Op-Amp less Bandgap Reference

The accuracy of the bandgap reference is greatly dependent on the matching of the transistor pairs MP_4-MP_5, MP_1-MP_2, MN_4-MN_5 and MN_1-MN_2. It can be argued that to reduce the mismatch the PMOS and NMOS should be biased in strong inversion. However, considering Fig. 3-6, for a bandgap voltage (V_{bg}) of 600 mV (specification), V_{ctat} should be about 400 mV at $-40\,^{\circ}$C (considering a ratio of N=8 and a resistor ratio of 5 for first order temperature-independence of V_{bg}). Consequently, the source of MN_4 is at about 350 mV. The threshold voltages of both PMOS and NMOS can be as high as 450-500 mV at $-40\,^{\circ}$C (for both technologies). This implies that the node V_4 has to be as high as 950 mV. This severely limits the minimum possible supply voltage, VDD. As one of the primary goals of this work is operation at sub-1V supply, it is preferred to bias the MOSFETs in weak inversion.

3.4 StartUp Circuit

Every self-biased bandgap circuit requires a start up circuit to ensure that the critical nodes (such as the bandgap voltage or the virtual ground at the amplifier input) do not remain at 0V. The complete implemented topology, with the start-up is shown in Fig. 3-7. The working of the start-up circuit is as follows. If the node V_{bg} is at low voltage, the two inverters Inv_1 and Inv_2 force the PMOS MP_S to conduct current. This, in turn, lifts the node V_4 to the appropriate voltage. Consequently, MN_1 forces V_1 to appropriate voltage and the circuit starts up. Note that if the output of MP_S was fed to V_5, then it would not work to generate appropriate gate bias for MP_4 and MP_3 as they are connected to the node V_1 and not V_2. The sizing of the start-up circuit

is discussed in Chapter 4.

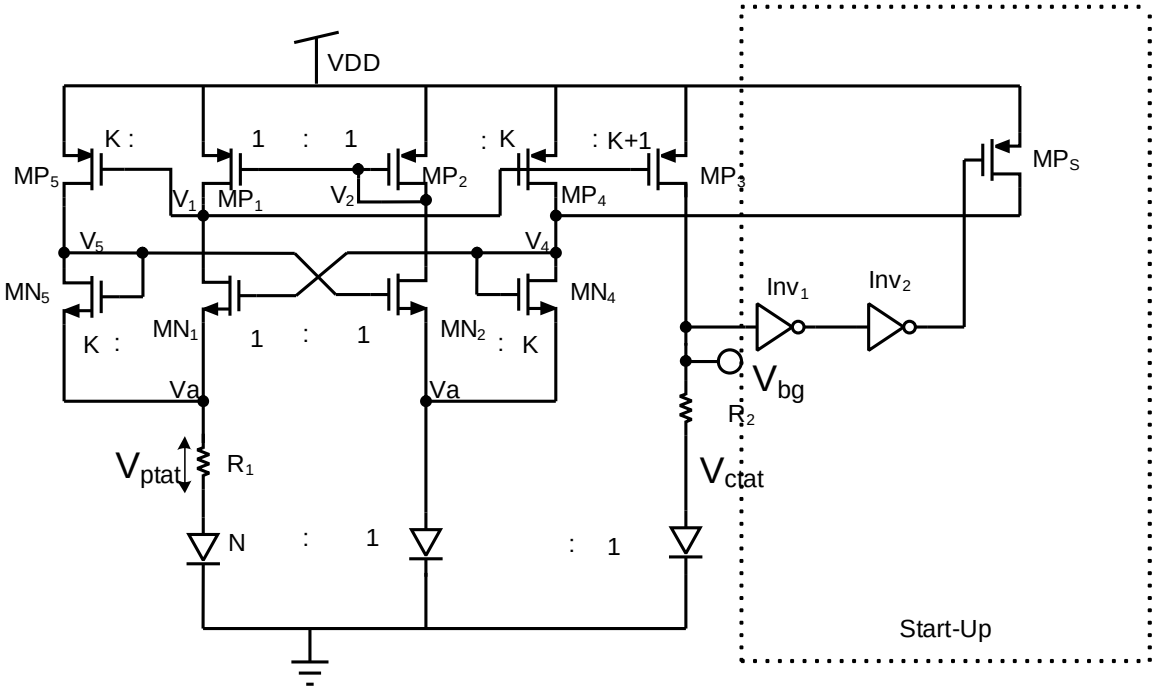


Figure 3-7: Bandgap Reference with startup

3.5 CMOS current mirrors in weak inversion

The topology for the implemented bandgap reference (see Fig. 3-6) makes use of a large number of CMOS current mirrors, biased in weak inversion. The properties of such current mirrors are discussed in this section with a focus on the different error/mismatch sources. Fig. 3-8 shows a CMOS current mirror, one of the most common blocks in analog circuits. Diode connected M_1 is the input device and M_2 is the output device.

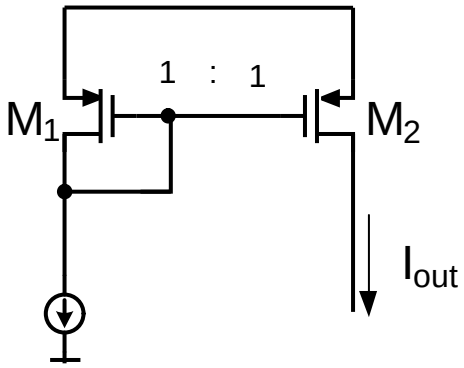


Figure 3-8: CMOS Current Mirror

The current in a MOS transistor, biased in weak inversion, is given by:

$$I_{ds} = \mu C_{ox} \frac{W}{L} (m-1) V_T^2 exp\left(\frac{V_{gs} - V_{th}}{mV_T}\right)\left(1 - exp\left(\frac{-V_{ds}}{V_T}\right)\right) \tag{3.10}$$

where I_{ds} is the drain current, μ is the carrier mobility, C_{ox} is the gate-oxide capacitance, V_{gs} is the gate-source voltage,V_{ds} is the drain-source voltage, V_{th} is the threshold voltage and V_T is the thermal voltage ($\frac{KT}{q}$). The parameter $m = 1 + \frac{C_D}{C_{ox}}$ is the body-effect coefficient ; C_D is the depletion capacitance[15]. The factor $\mu C_{ox} \frac{W}{L}$ is also known as the transconductance coefficient(β) and μC_{ox} is known as the unit transconductance coefficient($\beta_\square$).

In the first order approximation, assuming that the technology parameters are invariant for the two devices and they have the same drain voltage, the ratio of drain currents is determined by the ratio of the $\frac{W}{L}$ ratios.

$$\frac{I_{ds1}}{I_{ds2}} = \frac{W1/L1}{W2/L2} \tag{3.11}$$

For the ratio 1:1, as shown in Fig. 3-8, both the CMOS have the same drain current.

The accuracy of (3.11) is determined by the mismatch between the devices. These mismatch sources can be grouped into two categories:

- Random: Mismatches due to the unit transconductance coefficient ($\beta_\square$), the threshold voltage (V_{th}) and the body-effect coefficient (m) are the random sources of error.
- Deterministic: This consists of error due to difference in the drain-source voltage (V_{ds}).

3.5.1 Mismatch in β

Transconductance coefficient is defined as :

$$\beta = \mu C_{ox} \frac{W}{L} \tag{3.12}$$

where μ is the carrier mobility , C_{ox} is the oxide capacitance, W is the length of the MOSFET and L its length. Assuming W and L are constant (although they may have variations as well [21]), both μ and C_{ox} vary from device-to-device on the same die and lead to random mismatches in β. It has been shown in [22] that in silicon, μ can be expressed as:

$$\mu = \alpha T_n^{-0.57} + \frac{\Delta T^{-2.33}}{1 + \left(\frac{N}{\gamma T_n^{2.4}}\right) \delta T_n^{-0.146}} \tag{3.13}$$

In the above equation, T is the absolute temperature (in Kelvin), T_n is the normalized temperature ($\frac{T}{300K}$), $\alpha, \Delta, \gamma, \delta$ are empirical constants and N is the total carrier concentration (cm^{-3}). Thus, from (3.13), μ is dependent on temperature and impurity concentration. The doping concentration is not uniform over a die and can vary upto 30-40 % [20]. Therefore, devices on the same die might have different μ and hence, it is a random source of mismatch between them.

The oxide capacitance, C_{ox} is expressed as [20] :

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} \tag{3.14}$$

ϵ_{ox} is the dielectric constant of the oxide and t_{ox} is its thickness. The oxide thicknes, t_{ox} varies up to 5-10 % due to process variations ([23] , [24]). Thus, $\beta_\square$ is a random source of mismatch for the current mirror.

3.5.2 Mismatch in m and V_{th}

The parameter $m = 1 + \frac{C_D}{C_{ox}}$ is the body effect coefficient. As discussed in the previous section, C_{ox} varies randomly with process. Also C_D depends on the width of the depletion layer , which in turn depends on the doping concentration N and the surface potential ϕ_s [20]:

$$C_D = \frac{\epsilon_{Si}}{x_d} \tag{3.15}$$

where ϵ_{Si} is the the dielectric constant of Silicon and x_d is the depletion width given by [20] (q is the electronic charge):

$$x_d = \left(\frac{2\epsilon_{Si}\phi_s}{qN}\right)^{1/2} \tag{3.16}$$

Since N and ϕ_s are process dependent, m varies randomly.

For a PMOS, the threshold voltage is given by [20]:

$$V_{th} = \left(-\sqrt{4\epsilon_{Si}qN_dV_T\ln\frac{N_d}{n_i}} - Q_{SS}\right)\left(\frac{t_{ox}}{\epsilon_{ox}}\right) + \phi_{ms} - 2\phi_{fn} \tag{3.17}$$

Similarly for an NMOS, threshold voltage can be expressed as [20] :

$$V_{th} = \left(\sqrt{4\epsilon_{Si}qN_aV_T\ln\frac{N_a}{n_i}} - Q_{SS}\right)\left(\frac{t_{ox}}{\epsilon_{ox}}\right) + \phi_{ms} + 2\phi_{fp} \tag{3.18}$$

where Q_{SS} is the trapped charge density per unit area , ϕ_{ms} is the metal-semiconductor work function , ϕ_{fn} is the potential difference between intrinsic fermi-level and the fermi-level in an n-type substrate, ϕ_{fp} is the potential difference between intrinsic fermi-level and the fermi-level in a p-type substrate N_d / N_a is the doping concentration of the substrate and n_i the intrinsic charge concentration. Other symbols are as expressed earlier in this Chapter. Therefore, the threshold voltage is dependent on the doping concentration (N_d or N_a) and hence , is process dependent. Moreover, the threshold voltage is inversely proportional to temperature as n_i is given by [20] :

$$n_i = \sqrt{N_cN_v exp\left(\frac{-E_g}{KT}\right)} \tag{3.19}$$

where N_c and N_v are density of states at given temperature and E_g is the intrinsic bandgap voltage (difference between conduction and valence bands). For the 40nm process node, V_{th} varies from 500mV to 200 mV from $-40\,^{\circ}C$ to $125\,^{\circ}C$. Furthermore, the batch-to-batch spread of V_{th} was found to be about $3.5-4\%$ (tested by Monte-Carlo simulations with both process and mismatch variations turned on).

3.5.3 Mismatch in V_{ds}

V_{ds} plays a role in mismatch of the current mirror by changing the output impedance of the output MOSFET and thus, leading to mismatch in current. Channel length modulation is specially significant in deep-submicron technologies [14]. To reduce the impact of V_{ds} mismatch, the following steps can be taken :

- V_{ds} should be greater than 5-6 V_T i.e, about 150 mV at room temperature.This comes from (3.10) as $1 - exp\left(\frac{-V_{ds}}{V_T}\right)$ equals 0.982 , 0.993 and 0.997 when $\frac{-V_{ds}}{V_T}$ is 4 , 5 and 6 , respectively at room

temperature.

- Traditional circuit techniques like cascoding and gain boosting [14] help to reduce the mismatch by improving the output impedance, but at the cost of voltage headroom.
- At low supply voltages and ultra Deep-Sub Micron Technologies, sometimes the most effective solution is to increase the length the of the MOSFET (as output impedance is indirectly proportional to the channel length [14]). However, tradeoff is in terms of area and increased parasitics.

3.5.4 Effect of mismatch sources

For a current mirror (1:1 ratio), it can be shown [21] that the error in the output current due to the mismatch sources can be given as (also including the impact of m) :

$$\frac{\Delta I_{out}}{I_{out}} = \sqrt{\left(\frac{\sigma_\beta}{\beta}\right)^2 + \left(\frac{\sigma_{V_{th}}}{mV_{th}}\right)^2 + \left(\frac{\sigma_m}{m-1}\right)^2} + \left| \frac{exp\left(\frac{-V_{ds}}{V_T}\right)}{1 - exp\left(\frac{-V_{ds}}{V_T}\right)} \frac{\Delta V_{ds}}{V_T} \right| \tag{3.20}$$

In [25] , it is shown that :

$$\frac{\sigma_\beta^2}{\beta^2} = \frac{A_\beta^2}{WL} \tag{3.21}$$

$$\sigma_{V_{th}}^2 = \frac{A_{V_{th}}^2}{WL} \tag{3.22}$$

A_β and $A_{V_{th}}$ are constants and these equations hold in both strong and weak inversion. By a similar argument:

$$\sigma_m^2 = \frac{A_m^2}{WL} \tag{3.23}$$

where A_m is a constant. Thus, in order to reduce mismatch, larger area of MOSFET is useful. It is pertinent to note here that the constants (A's) are smaller in strong inversion than weak inversion [21]; thereby, leading to lesser spread. However, the MOSFETs are biased in weak inversion in the used topology due to headroom issues (explained in Section 3.3).

3.6 Error Sources

There are several error sources in the implemented bandgap reference (repeated for convenience in Fig. 3-9).

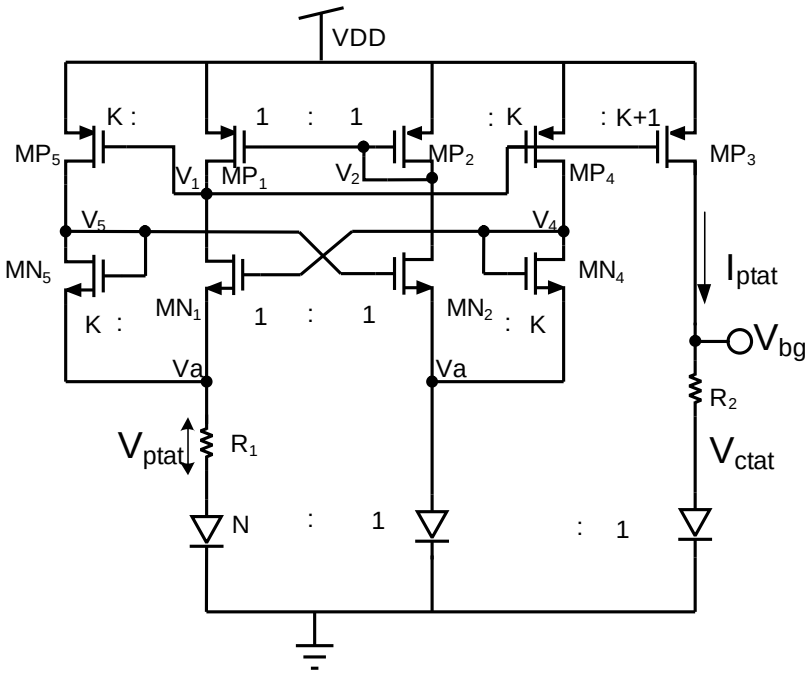


Figure 3-9: Op-Amp less Bandgap Reference

This section discusses the main error sources and their impact on the bandgap performance. The main error sources can be summarized as below:

- Mismatch in the drain currents of the DTMOST diodes generating V_{ptat}.
- Mismatch in the drain currents of MP_1 and MP_3.
- Process variations of DTMOST, leading to errors in V_{ctat}.
- Voltage offset at the virtual ground, V_a (source nodes of MN_1 and MN_2).
- Resistor spread and mismatches.

This analysis is done on similar lines as in [11] and [26].

3.6.1 Mismatch in drain currents of DTMOST generating V_{ptat}

If the drain currents are given by I_{d1} and I_{d2}, the bandgap voltage can be given as:

$$V_{bg} = V_{ctat} + \frac{R_2}{R_1} V_T \ln\left(\frac{I_{d1}}{I_{d2}} N\right) \tag{3.24}$$

Consider a δ_I mismatch between the currents, defined as $I_{d1} = I_{d1}|_{\delta_I=0}(1+\delta_I)$. Then,

$$V_{bg} = V_{ctat} + \frac{R_2}{R_1} V_T \ln\left(\frac{I_{d1}|_{\delta_I=0}(1+\delta_I)}{I_{d2}} N\right) \tag{3.25}$$

Therefore,

$$V_{bg} \approx V_{ctat} + \frac{R_2}{R_1} V_T \ln\left(\frac{I_{d1}|_{\delta_I=0}}{I_{d2}} N\right) + \frac{R_2}{R_1} V_T \delta_I \tag{3.26}$$

And hence,

$$V_{bg} \approx V_{bg}|_{\delta_I=0} + \frac{R_2}{R_1} V_T \delta_I \tag{3.27}$$

Assuming a nominal V_{bg} of 600mV , $\frac{R_2}{R_1}$ of 5 and a current mismatch δ_I of 5%, the obtained bandgap voltage is 606.5 mV which is already an error of 1%. Moreover, the current mismatch is not a linear function of temperature [6]. Hence, this error cannot be removed by a single temperature trim.

3.6.2 Mismatch in Drain Currents of MP_1 and MP_3

The bandgap voltage can also be written as:

$$V_{bg} = V_{ctat} + R_2 (I_{ptat}) \tag{3.28}$$

where I_{ptat} is the current through R_1 given by $\frac{V_{ptat}}{R_1}$. A mismatch of δ_I, in the drain currents, yields :

$$V_{bg} = V_{ctat} + R_2 (I_{ptat} + \delta_I I_{ptat}) \tag{3.29}$$

Hence, the obtained voltage is:

$$V_{bg} = V_{bg}|_{\delta_I=0} + R_2 (\delta_I I_{ptat}) \tag{3.30}$$

Assuming a nominal V_{bg} of 600mV , R_2 of 325kΩ ,a current mismatch δ_I of 5%, and the nominal current I_{ptat} as 700nA, the obtained bandgap voltage is 611.375 mV which is already an error of 1.9%. Moreover, the current mismatch is not a linear function of temperature [6]. Hence, this error cannot be removed by a single temperature trim.

3.6.3 Process variations of DTMOST, leading to errors in V_{ctat}

Process variations play an important role in the variation of V_{ctat}. It can be stated that :

$$V_{ctat} = V_{gs} = V_T \ln \frac{I_d}{I_o} \tag{3.31}$$

I_o is a process dependent constant that is a function of μ , m and C_{ox} . As explained in Section 3.5, these parameters vary greatly with process and temperature. Assuming an error of ΔI_o, :

$$V_{ctat} = V_T \ln \frac{I_d}{I_o + \Delta I_o} \tag{3.32}$$

This reduces to:

$$V_{ctat} = V_{ctat}|_{\Delta I_o = 0} - V_T \frac{\Delta I_o}{I_o} \tag{3.33}$$

Assuming a nominal V_{ctat} of 350mV at room temperature, an I_o of 700nA and a mismatch of 20%, there is an error of about 3mV at room temperature. It was shown in [11] that this error is PTAT in case of a BJT based diode. However, this does not hold true for a DTMOST diode.

3.6.4 Voltage offset at the virtual ground, V_a (source nodes of MN_1 and MN_2)

Assume an offset of V_{os} at V_a. Then $\Delta V_{gs} = \Delta V_{gs}|_{V_{os}=0} + V_{os}$. Noting that V_{bg} is :

$$V_{bg} = V_{ctat} + \frac{R_2}{R_1} \Delta V_{gs} \tag{3.34}$$

Thus, V_{bg} changes to:

$$V_{bg} = V_{ctat} + \frac{R_2}{R_1} \left(\Delta V_{gs}|_{V_{os}=0} + V_{os} \right) \tag{3.35}$$

Hence, V_{bg} becomes:

$$V_{bg} = V_{bg}|_{V_{os}=0} + \frac{R_2}{R_1} V_{os} \tag{3.36}$$

Therefore, the offset is amplified by the resistor ratio. Hence, an offset of 1 mV would lead to an error of 5 mV in V_{bg}. The error due to this offset is another non-PTAT source of error [11].

3.6.5 Resistor Spread and Mismatches

Consider a δ_R mismatch in the resistors, then this leads to an error in V_{bg}.

$$V_{bg} = V_{ctat} + \frac{R_2|_{\delta_R=0} + R_2 \delta_R}{R_1} V_{ptat} \tag{3.37}$$

Hence,

$$V_{bg} = V_{bg}|_{\delta_R=0} + \frac{R_2 \delta_R}{R_1} V_{ptat} \tag{3.38}$$

A mismatch of 0.2% leads to an error of 0.5mV in V_{bg}. But a bigger problem is the spread in actual value of resistors due to spread in sheet resistance. Assuming a fractional change δ_{RA} in each of the resistors, :

$$V_{bg} = V_{bg}|_{\delta_{RA}=0} + V_T \delta_{RA} \tag{3.39}$$

A 16% variation in sheet resistance would lead to an error of roughly 4mV. Proper analog layout techniques like common-centroid method and use of dummy devices [27] help to reduce mismatch δ_R.

3.6.6 Summary of error sources

The error sources are summarized in Table 3.1. Most of the errors are non-PTAT and this indicates the

Table 3.1: Different error sources

Error Source	Typical value	Error Contribution	Type of error
Current mismatch between DTMOST	5 %	6.5 mV	Non-PTAT
Current mismatch between MP_1 and MP_3	5 %	11.375 mV	Non-PTAT
Variations in V_{ctat}	20 %	3 mV	Non-PTAT
Voltage offset	1 mV	5 mV	Non-PTAT
Resistor Mismatch	0.20 %	0.5 mV	PTAT
Resistor Spread	16 %	4 mV	PTAT
Total		14.896 mV	

possibility of a two (or more) temperature trim for reducing the spread. The errors add in mean square fashion, resulting in an error of about 15 mV which corresponds to a 3σ variation of 2.5% for a V_{bg} of 600 mV in the untrimmed case. The current mismatches have been reduced greatly to 5% range by increasing the loop gain (by circuit techniques described in this section) as well as using larger channel lengths (5 μm for the 40 nm design and 2μm for the 0.16 μm design).

3.7 Summary

The topology of the implemented bandgap reference was discussed in this Chapter. Op-amps consume additional power; hence, eliminating them saves power. An op-amp less bandgap reference (biased entirely in weak inversion) was discussed. It was found that the architecture had significant current mismatch and voltage offset at the virtual ground. Therefore, active feedback branches were introduced to improve the performance. It was always ensured that the overall negative feedback exceeded the overall positive feedback. A start-up circuit was suggested for the bandgap reference. It was shown that there are significant variations in current mirrors, biased in weak inversion, due to process as well as temperature variations. Finally, the various error

sources, associated with the reference, were analyzed to get an idea of the relative impact of the different error sources.

Chapter 4

Implementation and Results

4.1 Overview

This chapter describes the implementation of a DTMOST-based “bandgap" reference in standard CMOS technology. As stated in Chapter 1, the design was taped out in NXP 0.16 µm CMOS technology (C14) and also simulated in TSMC 40 nm CMOS technology. The available devices and features of each process are described in Section 4.2, followed by a discussion of the various design choices made. Measurement results are presented for the taped out prototypes in C14 along with a comparison with the post-layout simulations of the implementation in TSMC 40 nm node. Finally, a comparison with the state-of-the-art is presented. The key specifications for the design were stated in Chapter 1 and are repeated in Table 4.1.

Table 4.1: Main specifications for the Bandgap Reference

Parameter	Value
Output Voltage	~0.6-0.7V
Technology	Standard CMOS(0.16 µm, 40 nm)
Minimum Supply Voltage	< 1V
Temperature Range	$-40\,^{\circ}$C to $125\,^{\circ}$C
3σ spread	$< 5\%$
Temperature Drift	< 100 ppm/$\,^{\circ}$C
Current Consumption	< 5 µA at all corners
Active Area	$\leqslant 0.05\mathrm{mm}^2$

4.2 Design Choices

The NXP C14 process is a five metal-one poly process (5M-1P)[23] whereas the TSMC 40 nm is a 7M-1P process [24]. The layout was limited to three metals and the poly layer for both technology nodes. The following section describes the reasons behind the various design choices. Since similar trends are observed in both technologies, only the results of some proof of concept simulations are presented. Any differences between the technologies will be highlighted when necessary. As explained in Chapter 3, the key devices for this topology are the resistors and the DTMOST.

4.2.1 Choice of resistors

Both technology nodes have n-well as well as polysilicon resistors. The 40 nm node also has silicided polysilicon resistors. The n-well resistors have high temperature coefficient ([23], [24]) and are hence, least suitable for operation as using them would increase the temperature co-efficient of the bandgap reference. Silicided resistors have the best performance with temperature, but their sheet resistance is very low ([23], [24]). This would lead to large area for the implementation. Thus, unsilicided poly resistors are a good tradeoff and hence, they have been used in both implementations.

4.2.2 Choice of MOSFETs

Both technologies provide access to standard, high-voltage, low and high threshold voltage MOSFETs. In addition, the 40 nm node also provides access to native devices. In order to ensure good matching, similar types of devices (two devices with an area ratio of 1: N) are used to provide the difference in the diode voltage, ΔV_{gs}. Native devices are rejected as they generally have high-leakage current and thus larger variation of threshold voltage. Low and high threshold devices are ignored as:

- They are not available across all technologies and one of the major goals of this thesis is to develop a design that can be easily ported across different technology nodes.
- For generation of the low/high threshold devices, additional masking steps are involved. This leads to a greater uncertainty during the fabrication process and hence, more spread.

Therefore, the choice remains between the standard and high-voltage MOSFETs as well as between PMOS and NMOS types for the realization of the DTMOSTs. Since the p-well of N type DTMOST has a low impedance path to the p-substrate in twin-well processes, N-type DTMOSTs cannot be well-controlled [4]. Another important factor in this decision is the behavior of the PTAT voltage. Fig. 4-2 shows the deviation of the observed PTAT voltage from the ideal PTAT voltage ($\frac{KT}{q}\ln(N)$) when N-type and P-type DTMOSTs (with an area ratio 1:N) are biased by same current (Fig. 4-1).

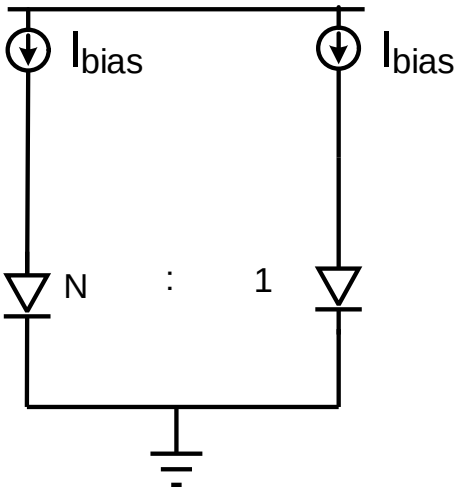


Figure 4-1: Setup with PTAT generating diodes biased by same current

Note that the following trend, with single values of bias current and sizes, is also viewed across different sizes and bias currents across both processes.

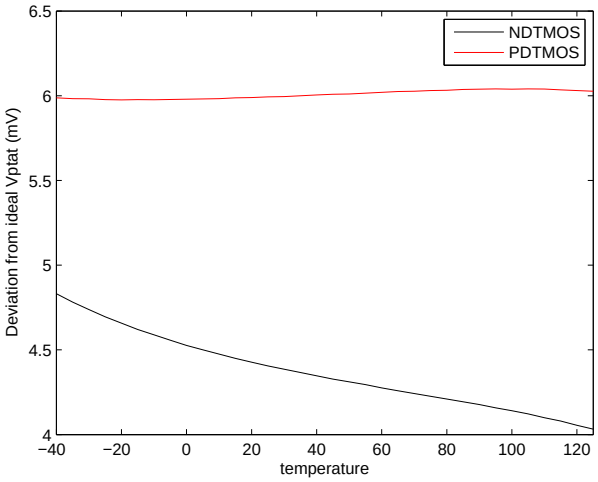


Figure 4-2: Deviation from ideal PTAT voltage

Thus, the deviation is not constant with temperature for N-type DTMOSTs and hence, they are overlooked. Only P-type DTMOSTs are used for the purposes of this design. Note that there is a small variation with temperature for the P-type DTMOSTs as well. But, as shown in Fig. 4-2, this variation is relatively constant when compared to the case of N-type DTMOSTs. It was observed that for the C14 process, P-type DTMOSTs with thick oxides (IO DTMOSTs) have less 3σ spread than standard DTMOST and are hence, used for the fabrication in the C14 tapeout. However, it was observed that the obtained bandgap voltage is lower for implementations with thin oxide (standard) DTMOSTs than with thick oxide DTMOSTs. This leads to

operation at lower supply voltages for designs with standard DTMOSTs. It was observed from the simulations in 40 nm technology node that the spread was the same for both thick and thin-oxide DTMOSTs. Thus, thin oxides (standard) DTMOSTs were used to ensure operation at a lower supply voltage. Consequently, the C14 chip works down to 0.9V and the 40 nm chip works down to 0.8V (from post-layout simulations). In summary, IO devices were used as DTMOST diodes in the C14 chip to reduce spread and the standard DTMOST devices were used in the 40 nm node to ensure operation at lower supply voltage.

4.2.3 Ratio N for the DTMOST

For this implementation, the PTAT generating diodes are biased at the same current (Fig. 4-1). Thus, to ensure different current densities, they must have different effective area. This is done by using the two diodes in the ratio 1:N. For low value of N (N=2), large value of resistors are needed to compensate the slope of V_{ctat}.This leads to large area consumption. Also, for too high value of N, the DTMOSTs might operate in different bias points. N=8 is chosen for this design.

4.2.4 Sizing of resistors

As explained in Chapter 3, $V_{bg} = V_{ctat} + \frac{R_2}{R_1}\frac{KT}{q}\ln(N)$. So, there is only one degree of freedom in choosing the value of resistor. Choosing R_1 fixes the value of R_2 to ensure temperature independence (first order) of V_{bg}. There are two considerations for choosing the value of R_1:

- R_1 defines the current in the PTAT diodes. The current should be within the current budget($< 5\mu A$) at all corners. Assuming worst case current of $5\mu A$ at 125 °C, current through each diode will be $\frac{5\mu A}{3} = 1.67\mu A$(since three equal branches contribute to the net current; see Fig. 4-12). Thus, $R_1 > 21k\Omega$.
- From simulations of the slope of V_{ctat}, $R_2 \simeq 4.5 - 4.7R1$. Thus, the size of R_1 should be chosen carefully to be within the area specifications.

Fig. 4-3 shows the deviation of the PTAT voltage from the ideal PTAT over temperature as the bias current is changed (at room temperature).

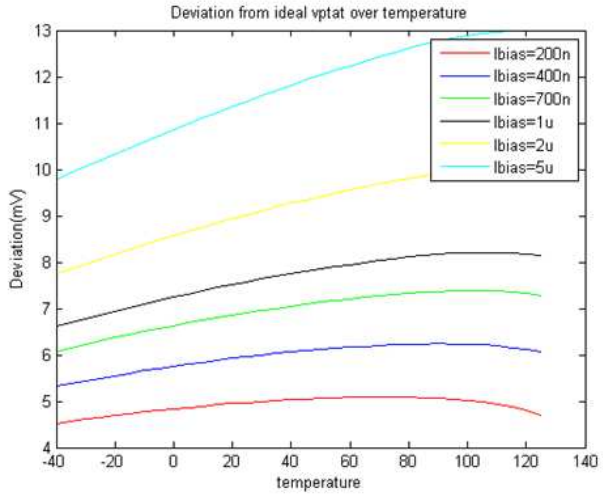


Figure 4-3: Choosing the bias current

Clearly, on decreasing the bias current, the device goes deeper into weak inversion. This leads to a more ideal-exponential current-voltage relationship and hence, less deviation from the ideal V_{ptat}. To keep the area in check, too small values for bias current (and thus, too large values for resistor) cannot be chosen. A bias current of 700nA serves as a good tradeoff. This corresponds to R_1 of 77KΩ. An R_1 of 75kΩ is chosen, leading to $R_2 \simeq 350$kΩ.

4.2.5 Sizing of DTMOSTs

The key goal is to ensure that the 3σ spread is as low as possible (the deviation from ideal V_{ptat} is ensured by choosing proper value of N and bias current). For this, Monte-Carlo simulations were performed with the set-up of Fig. 4-4. The DTMOST diodes were subjected to process and mismatch variations in the Monte-Carlo simulations. The ideal operational amplifier is implemented using an ideal voltage-controlled voltage source.

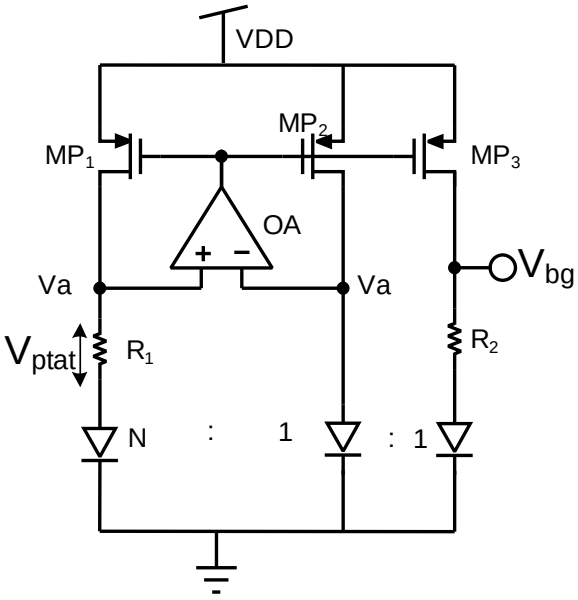
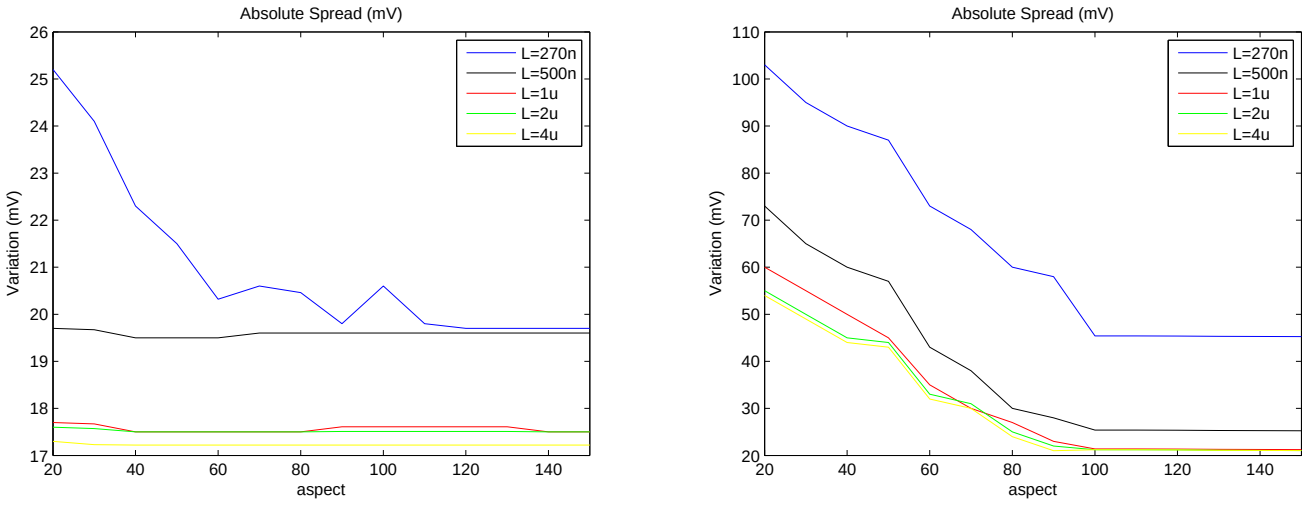


Figure 4-4: Setup for sizing the DTMOST

The spread is shown in Fig. 4-5(a) and Fig. 4-5(b). It can clearly be observed that at very low values of length, L and/or aspect ratio(defined as $\frac{W}{L}$, where W is the width), the spread is pretty large. But after a certain value of aspect ratio and length, the spread remains nearly constant.



(a) 40 nm

(b) C14

Figure 4-5: Sizing of the DTMOST: Deviation of the resulting PTAT voltage from its ideal value as a function of aspect ratio and for different lengths in C14 and 40nm processes

Size chosen is $\frac{30\mu m}{1\mu m}$ in the 40 nm node and $\frac{100\mu m}{1\mu m}$ in C14. For the subsequent sections,the sizing is done for the implemented topology described in Chapter 3 and reproduced in Fig. 4-6.

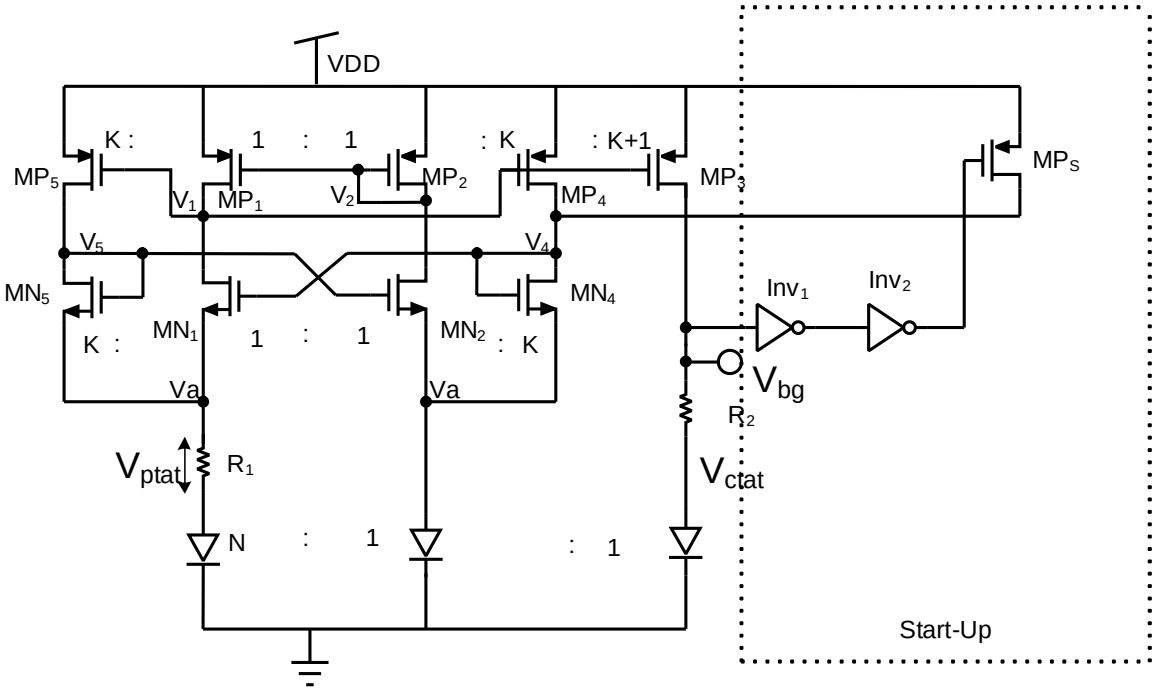


Figure 4-6: Implemented topology

4.2.6 Sizing of the PMOS and NMOS

Taking into account the following considerations, different PMOS and NMOS transistors were sized.

- Due to channel length modulation, there is an error in the current copying by the current mirrors. Since this error is temperature-dependent, this leads to large deviation in the temperature-coefficient of the bandgap voltage. The spread increases significantly due to current mirror mismatch. To overcome these problems, large lengths of the MOSFET (2-5 µm) are used for the implementations.
- To ensure sub-threshold operation, a pretty large aspect ratio is needed. To reduce the 1/f noise due to the current mirrors, large area is needed. These two requirements determine the widths of the MOSFET. An aspect ratio of 10 is used for the 40 nm version and that of 30 is used for the 0.16 µm version.

The chosen sizes are shown in Fig. 4-9(a) and Fig. 4-9(b).

4.2.7 Value of K

As explained in [6], higher value of K (Fig. 4-6)leads to a higher loop gain. This leads to better value of PSRR at DC as well as better noise performance. However, due to the constant value of gain-bandwidth product, bandwidth (3 dB bandwidth value of PSRR) decreases with K. This trade-off is visible in Fig. 4-7. Note that

the magnitude of PSRR is plotted in this figure. Optimum value of K=10 and K=15 were chosen for C14 and 40 nm implementations, respectively.

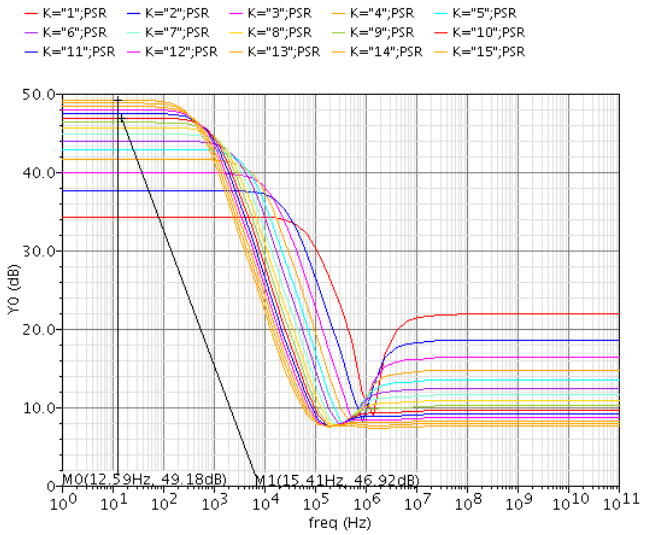
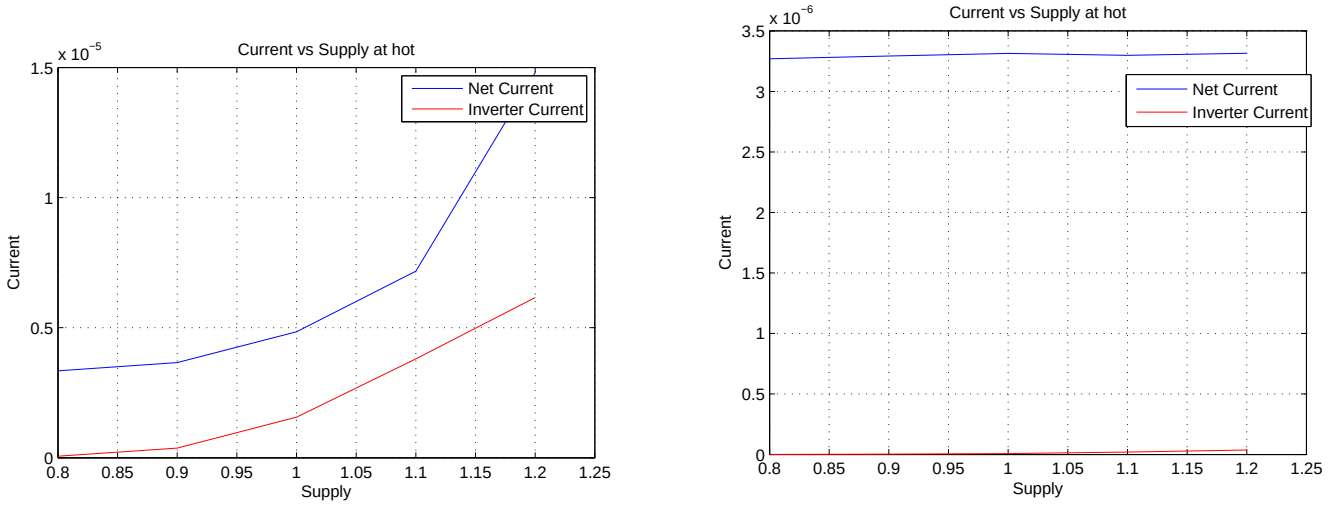


Figure 4-7: Impact of varying K:PSRR is shown versus frequency for different values of K

4.2.8 Sizing of the startup circuit

As explained in Chapter 3, the start-up circuit pulls up the bandgap voltage (V_{bg}). But the key issue is in the sizing of the first inverter. As the voltage is pulled up, the NMOS of the first inverter is switched on. If the supply voltage is sufficiently high, then the PMOS is switched on as well, leading to large leakage current. This is of particular concern at the highest supply voltage and highest temperature (125°C). This problem can be mitigated by making the $\frac{W}{L}$ ratio of the transistors in the first inverter small. This ensures flow of very small current as the on-resistance is proportional to $\frac{L}{W}$. This is demonstrated in Fig. 4-8(a) and Fig. 4-8(b). In Fig. 4-8(a), both inverters have the nominal size($\frac{120nm}{40nm}$ in 40 nm process and $\frac{0.768\mu m}{0.16\mu m}$. Clearly, large leakage currents are visible at higher supply voltage. In Fig. 4-8(b), the length of the first inverter is increased to $20\mu m$, while keeping the same width. This greatly increases the on-resistance and hence, the current is very low.



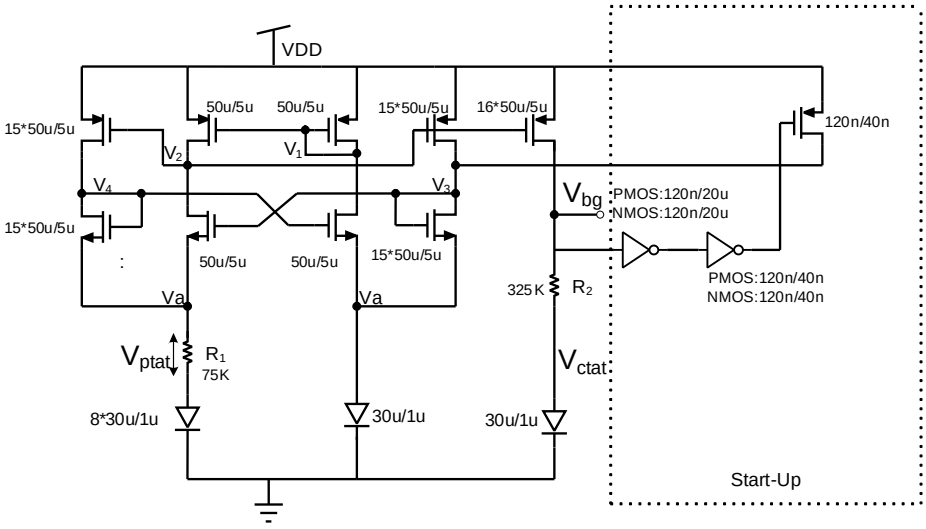
(a) With normal sized inverter

(b) With inverter having small $\frac{W}{L}$

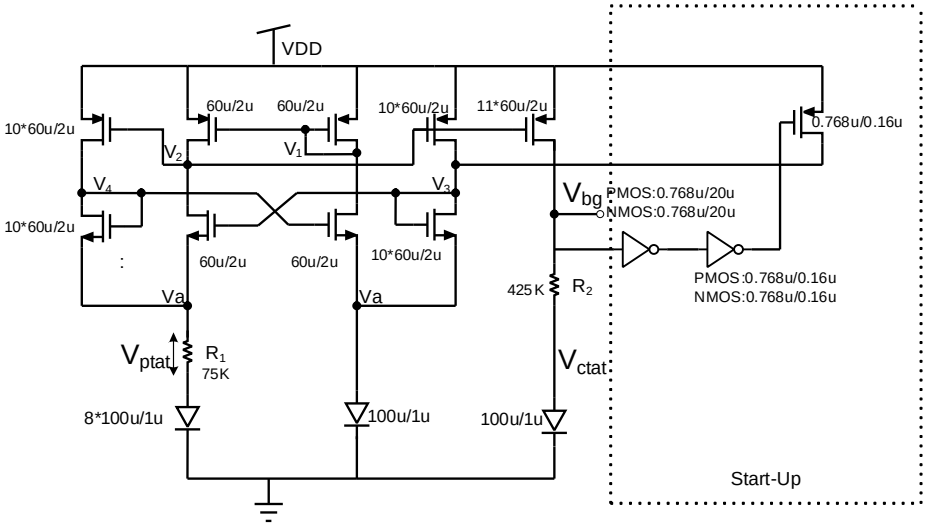
Figure 4-8: Currents after adding start-up block

4.2.9 Complete circuit

Fig. 4-9(a) and Fig. 4-9(b) show the complete circuit with the chosen sizes for each technology. Sizes are chosen as described in Section 4.2.



(a) 40nm



(b) C14

Figure 4-9: Full circuit with chosen sizes

4.3 Error Contributions

The 3σ spread is one of the key criteria for characterizing the bandgap reference. The key error sources are listed below:

- Mismatch in the DTMOST diodes.
- Mismatch in the resistors.
- Mismatch in the current mirrors.

Monte-Carlo simulations were carried out to find the individual contributions of each of the error sources. Unfortunately, the C14 PDK/simulation setup does not have the option of turning on the Monte-Carlo (mismatch) models for selective devices in a topology. Hence, results are reported only for the 40 nm node in Table 4.2. It is pertinent to note here that the errors add in root mean square fashion. Clearly, most of the spread

Table 4.2: Error Contributions for the Bandgap Reference

Total Spread	Spread in DTMOST only	Spread in Resistors only	Spread in amplifier only
21 mV (3.7%)	17.67 mV (3.26%)	2.56 mV(0.44%)	11.05mV (1.95%)

comes from the DTMOST core. Thus, precision techniques like chopping on the amplifier might not lead to significant reduction of spread. However, trimming might be helpful. Note that for the C14 node, approximate simulations could be performed -using ideal resistors and ideal op-amps, but even then, the DTMOST diodes dominate the spread.

4.4 Layout

The circuit was implemented in 40nm and C14 CMOS Technologies. The layouts are displayed in Fig. 4-10 and Fig. 4-11. Analog layout techniques[27] like common-centroid layout, using dummy cells were used. Extra guard rings were built around the matching-sensitive DTMOST and resistor parts. Both layouts occupied an active area of $0.05\mathrm{mm}^2$.

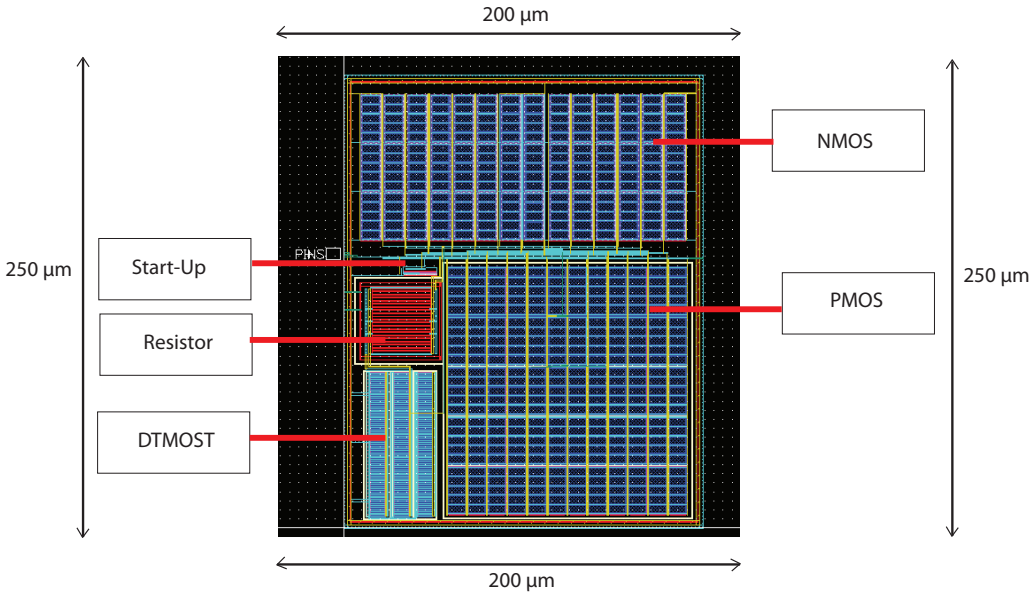


Figure 4-10: Layout in 40 nm

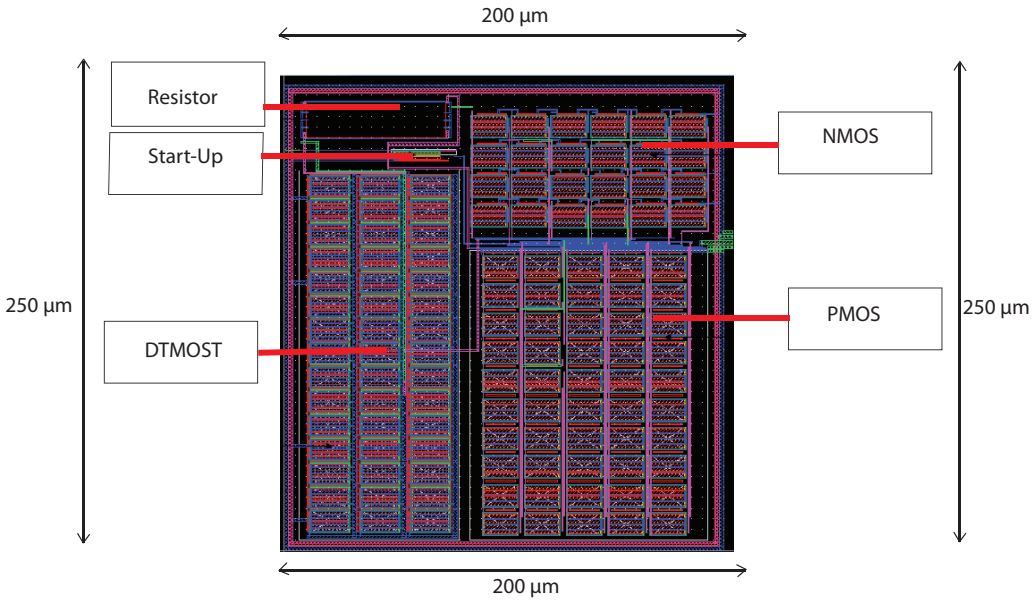


Figure 4-11: Layout in C14

For the 40 nm layout, pins for supply, ground and the output voltage were provided. For the taped out C14 version, another extra current mirror branch was designed (Fig. 4-12) to measure the net current consumption. Thus, an additional pin for current was introduced. Note that the net current in the Bandgap core is approximately three times the measured output current.

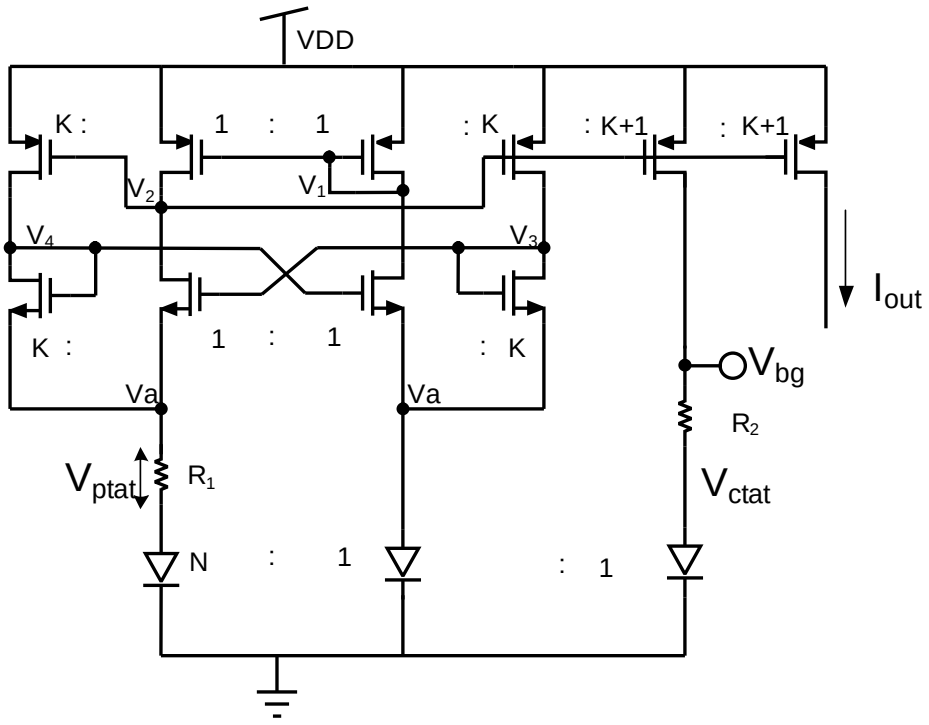


Figure 4-12: Full circuit taped out in C14

4.5 Measurement Results in C14

20 samples of the C14 chip were packaged in ceramic DIL package. The measurement results are presented in this section.

4.5.1 Inaccuracy over temperature

The 20 samples were measured from −40°C to 125°C over different supply voltages. The bandgap voltage versus temperature is plotted in Fig. 4-13 in blue for the 20 samples at supply of 1V. The 3σ boundary is plotted in red.

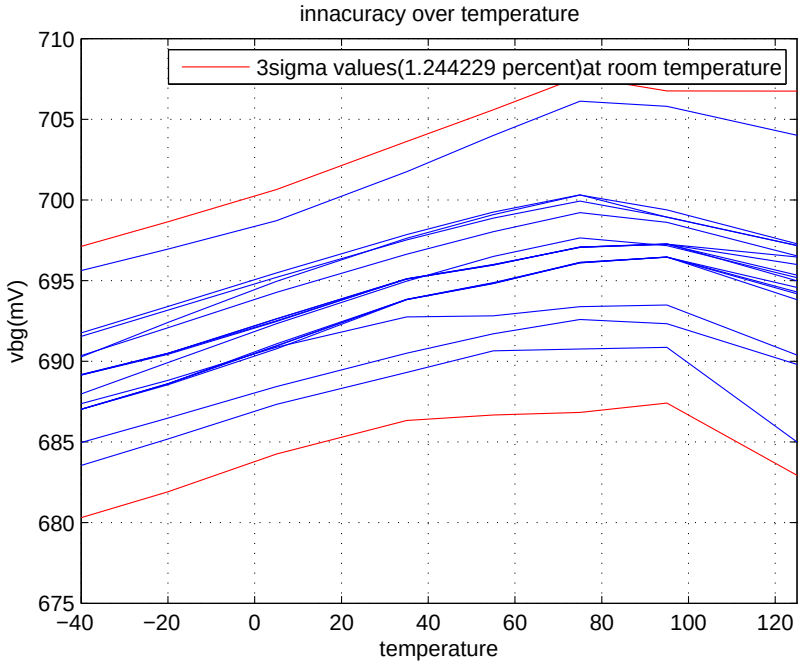


Figure 4-13: Band gap voltage vs temperature at 1V supply in C14

The variation of the bandgap voltage with supply is also studied as shown in Fig. 4-14. From the plot, it is clear that the chip is functional from 0.9 V.

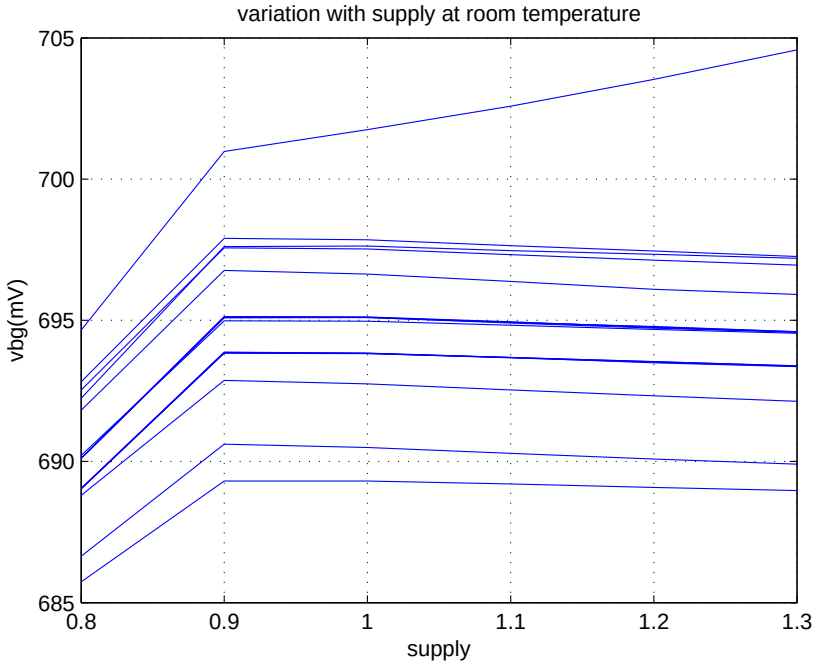


Figure 4-14: Bandgap voltage vs supply at room temperature in C14

The performance of the C14 samples at different supply voltages is shown in Table 4.3.

Table 4.3: Measured Bandgap References at C14

Supply	3σ at room temperature	Tempco	Remarks
0.8		700ppm/°C	Insufficient supply
0.9	1.04%	43-84ppm/°C	Chip starts working at this supply
1	1.25%	50-90ppm/°C	
1.1	1.18%	71-110ppm/°C	Needs to be trimmed
1.2	1.30%	75-125ppm/°C	Needs to be trimmed
1.3	1.38%	77-140ppm/°C	Needs to be trimmed

The temperature coefficients were calculated as shown below.

$$\mathrm{Tempco} = \frac{V_{bg}\,(max) - V_{bg}\,(min)}{125 - (-40) \times V_{bg}\,(roomtemperature)} \times 10^6.$$

From the Table 4.3, the temperature coefficients are a little high (especially at higher supply voltages). Therefore, trimming is necessary to reduce the temperature coefficient. The results from a Monte Carlo simulation on the layout in C14 is shown in Fig. 4-15.

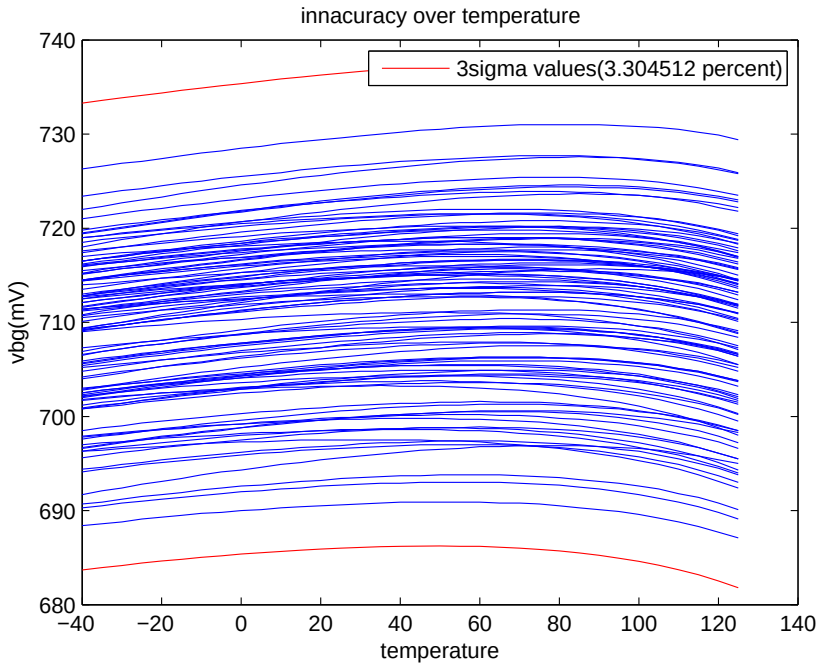


Figure 4-15: Post layout Monte Carlo simulation result for C14 chips. The bandgap voltage is plotted vs temperature at a supply of 1V.

It is pertinent to note that from post-layout Monte Carlo simulations (with both process and mismatch variations turned on), the spread was expected to be 3.3%. But, measurements show the spread to be 1.25%. However, since the samples came from a single run, spread might increase on testing samples from different fabrication runs. Furthermore, the post-layout simulations had predicted a temperature coefficient $< 60\mathrm{ppm}/^{\circ}\mathrm{C}$ in the discussed supply range (0.9-1.3V). But from Table 4.3, the measured temperature coefficients were found to be higher. Fig. 4-16 shows the current consumed at the highest supply voltage. The reported value is three times the measured current ($\mathrm{I_{out}}$)(see Fig. 4-12), which is (approximately) equal to the net current consumed by the bandgap core. From Fig. 4-16, the current is PTAT as expected. Changes in the slope around $100^{\circ}\mathrm{C}$ is consistent with larger leakage (source to bulk), for the DTMOST diodes, taken into account by shifting the maxima of the Vbg around $75^{\circ}\mathrm{C}$ (Fig. 4-13)and not $45^{\circ}\mathrm{C}$ (mid-point of $-40^{\circ}\mathrm{C}$ and $125^{\circ}\mathrm{C}$).

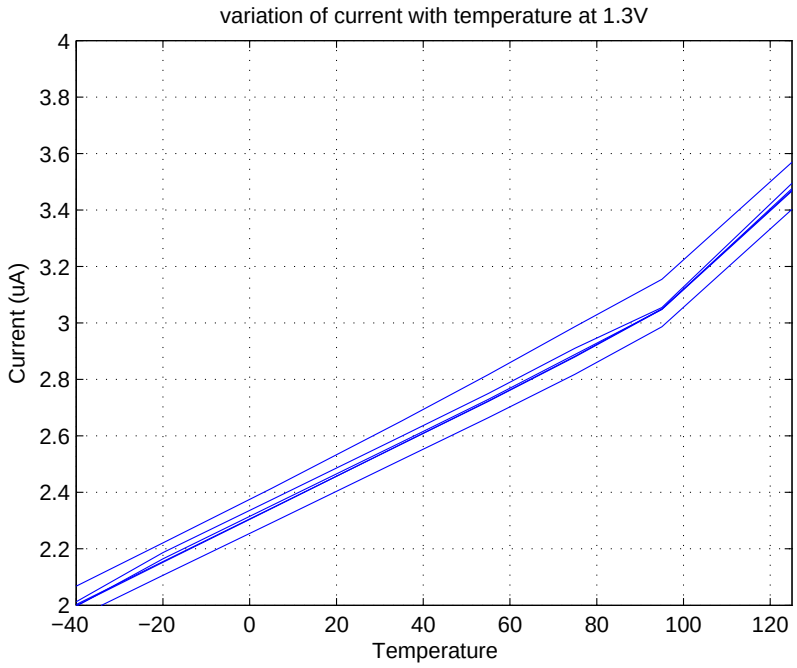
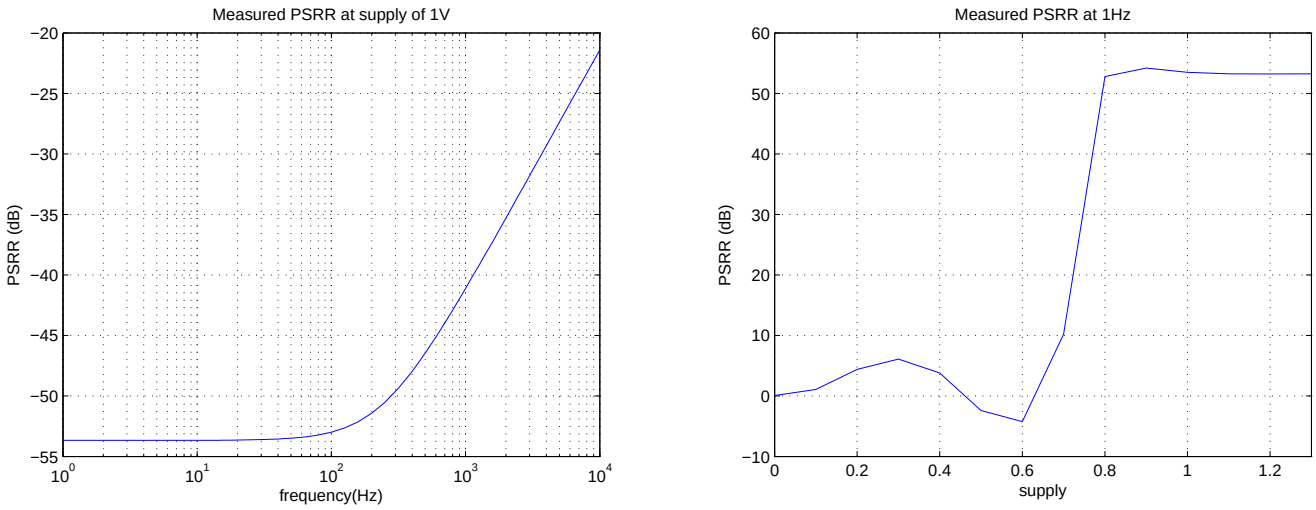


Figure 4-16: Net Current at highest supply voltage in C14.

4.5.2 PSRR and Noise Measurements

The PSRR and noise measurements were done using dynamic signal analyzer HP3562A at room temperature. The signal was fed to the signal analyzer after passing it through an AC-coupled pre-amplifier (with a gain of 1), which served as a buffer. The worst case behavior (among the 20 samples) is plotted in this section. For the PSRR measurements, DC (offset) shifted sine-waves (with AC amplitude of one) were generated from the signal analyzer and fed as supply to the circuit for measurements. The PSRR measurements are shown in Fig. 4-17(a) and Fig. 4-17(b).



(a) Measured PSRR in C14 at 1V supply

(b) Magnitude of PSRR vs supply in C14

Figure 4-17: PSRR measurements in C14

From Fig. 4-17(a), it is seen that the PSRR is -53dB at room temperature for 1Vsupply. Also, the variation over supply reaffirms that the chip starts working at 0.9V supply.

For noise measurements, a battery pack was used as supply .This is to counteract the strong influence of the 50 Hz tone and its harmonics that was visible while using the power supply. Fig. 4-18 shows the noise spectrum at 1V supply. The 1/f cut-off frequency is at 100 Hz. The total integrated noise from 1 to 100 Hz was found to be $23\mu Vrms$. The noise floor (after 100 Hz) is about $856nV/\sqrt{Hz}$.

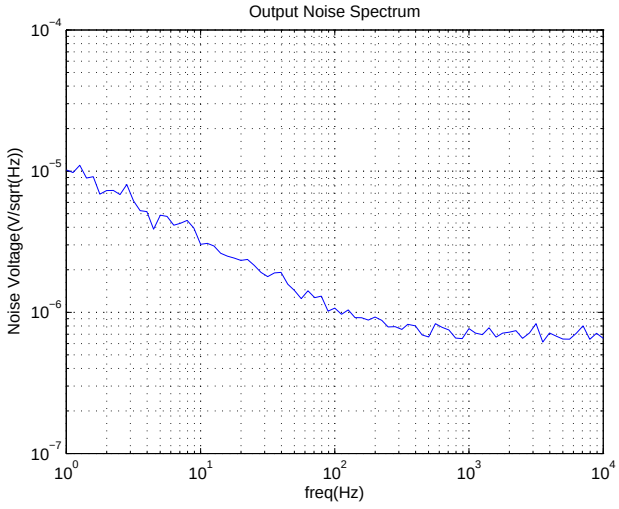


Figure 4-18: Noise spectrum at 1V supply in C14

The post-layout simulation results for PSRR and noise at room temperature and 1 V supply are shown in

Fig. 4-19 and Fig. 4-20, respectively. The simulations and measurements match quite nicely for PSRR. The measured noise is slightly higher (by about 2 $\mu V/\sqrt{(}Hz)$ for the measurements.

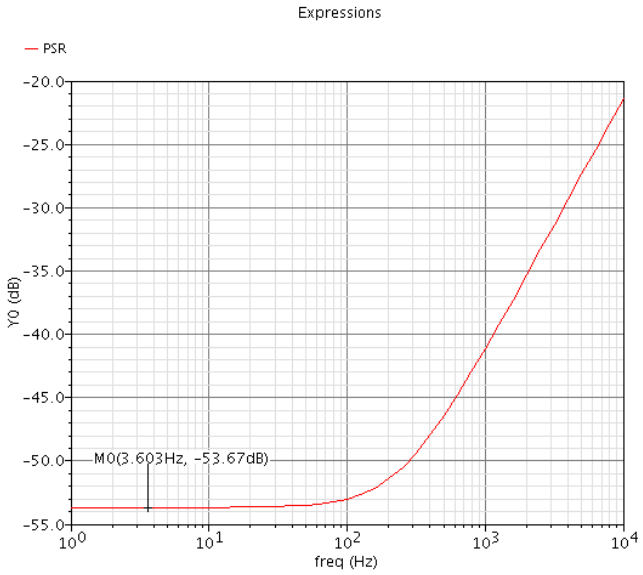


Figure 4-19: Post layout simulation result for PSRR at 1V supply and room temperature in C14

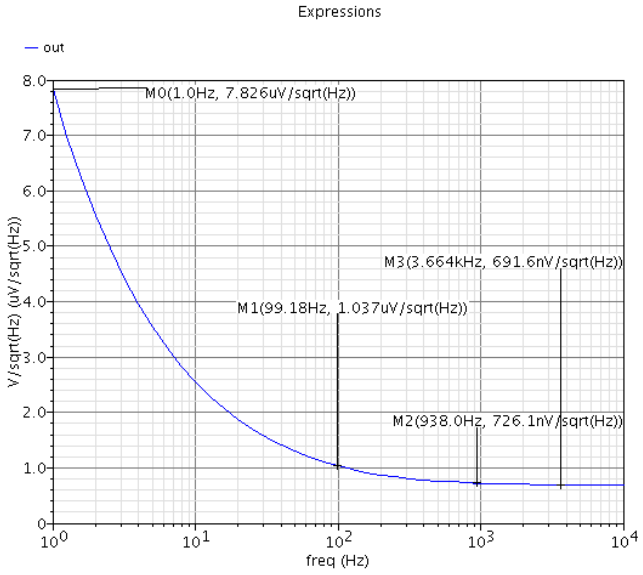


Figure 4-20: Post layout simulation result for noise spectrum at 1V supply and room temperature in C14

4.6 Comparison between the measurement and post-layout simulation results in C14

The comparison between the measurement and simulation results is given below:

- Simulations predict a 3σ spread of 3.3 %. But the measured chips show a spread of 1.25%. This is because both process and mismatch variations were turned on for the post-layout Monte Carlo simulations but the measured chips were fabricated in a single batch. In an industrial production (several batches), higher 3σ spread than 1.25% can be expected.
- The measured chips have a larger temperature coefficient (worst case $> 100\mathrm{ppm}/^{\circ}\mathrm{C}$ compared to $< 60\mathrm{ppm}/^{\circ}\mathrm{C}$ for the simulated case). This could be compensated by trimming or changing the mid-point of the V_{bg} curve (zero slope with respect to temperature) in a future implementation in this technology.
- The measured PSRR values match quite well with the simulations (-53 dB). However, the measured noise is slightly higher.

4.7 Post-Layout Simulation Results in 40 nm CMOS

Some of the post-layout simulation results for the 40 nm design are presented in this section. Fig. 4-21 shows the inaccuracy over temperature at supply of 1V. A 3σ spread of 3.7% is observed for Monte-Carlo simulations (both process and mismatch) for 100 samples. Temperature coefficient of 34-60ppm/°C is observed.

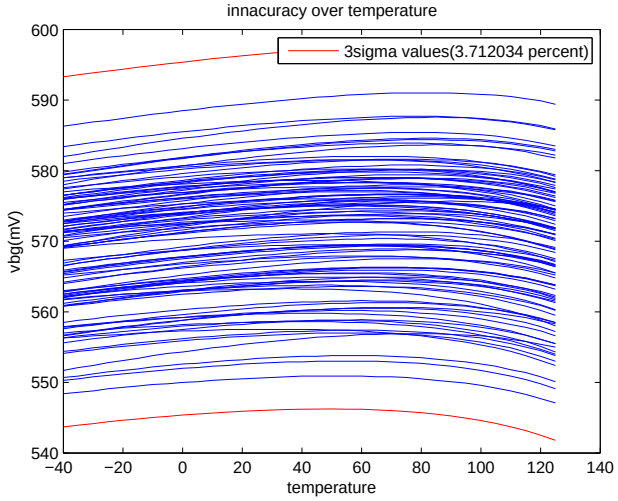


Figure 4-21: Band gap voltage vs temperature at 1V supply in 40 nm

The chips start functioning at a supply voltage of 0.8V. At DC, PSRR of 45.3 dB is observed at room temperature and supply of 1V. The noise spectrum is shown in Fig. 4-22. The $\frac{1}{f}$ cut-off frequency is at 100 Hz. The total integrated noise from 1 to 100 Hz was found to be $23.17\mu Vrms$. The noise floor (after 100 Hz) is about $541.1nV/\sqrt{Hz}$.

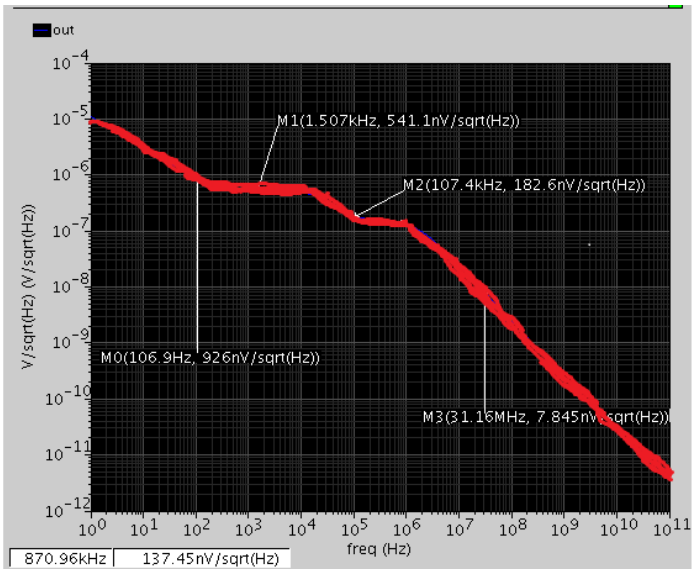


Figure 4-22: Noise spectrum at 1V supply in 40nm

4.8 Summary and Benchmark

Table 4.4 summarizes the performance of the bandgap references (measurement results in C14 and post-layout simulation results in 40 nm) and compares the performance with previous publications.

Previous CMOS based references ([4], [18], [17], [16]) showed much greater spread or temperature coefficient (TC) than the present work. When compared to BJT-based precision references like [11], the present work occupies much lower area and consumes lower current. [6] has comparable performance (lower TC) but much larger power consumption for sub-1V operation. [2] does not work for supply voltages lower than 950mV.[28] has much lower power consumption, much lower area and comparable spread. However, the untrimmed TC in [28] is worse than the presented work and the behavior is studied for a smaller temperature range. The presented work, therefore, performs quite admirably when compared to the state-of-the-art.

Table 4.4: Performance Comparison

	Tech.	Type of Diode	Min Supply	Vbg	Current at Room Temperature (RT)	Temp Range	TC	Spread (3σ)	PSRR at RT	Noise (rms)	Active Area
This work (C14)	0.16 μm	DTMOST	0.9V	670mV	2.4μA (1V supply)	$-40^\circ C$ to $125^\circ C$	50-90 $ppm/^\circ C$ (1V supply)	1.25%	-53dB (1V supply)	23μV (1-100 Hz;1V supply)	0.05mm^2
This work (40 nm) (post-layout sims)	40 nm	DTMOST	0.8V	571.6 mV	2.58μA (1V supply)	$-40^\circ C$ to $125^\circ C$	34-47 $ppm/^\circ C$ (1V supply)	3.70%	-45.3dB (1V supply)	23.17μV (1-100 Hz;1V supply)	0.05mm^2
Ge [11]	0.16 μm	BJT	1.7V	1.0875V	55 μA	$-40^\circ C$ to $125^\circ C$	5-12 $ppm/^\circ C$ (post-trim and curvature-correction)	0.75% (untrimmed)	-74dB	6.1μV (1-10 Hz)	0.12mm^2
Lam [6]	0.35 μm	BJT	0.9V	635 mV	16.6 μA	$5^\circ C$ to $95^\circ C$	24 $ppm/^\circ C$	n/a	-47.6dB	n/a	0.059mm^2
Annema [4]	0.35 μm	DTMOST	0.85V	650 mV	1.2 μA	$-20^\circ C$ to $100^\circ C$	60 $ppm/^\circ C$	6%	n/a	n/a	0.063mm^2
Annema [2]	0.16 μm	MOSFET	1.1V	944 mV	1.5 μA	$-11^\circ C$ to $135^\circ C$	30 $ppm/^\circ C$	2.52%	n/a	n/a	0.0025mm^2
Seok [28]	0.13 μm	MOSFET-different class of circuit	0.5V	175 mV	4.4 pA	$-20^\circ C$ to $80^\circ C$	16.9-231$ppm/^\circ C$ (untrimmed);5.3-47.4$ppm/^\circ C$ (post-trim)	$1.7-2.55\%$	-53dB	n/a	0.00135mm^2 (untrimmed); 0.0093mm^2 (post-trim)
Annema [29]	32 nm	FINFET	0.9V	$\sim$600mV	14 μA	$0^\circ C$ to $150^\circ C$	962$ppm/^\circ C$	n/a	n/a	n/a	0.016mm^2
Vita [16]	0.35 μm	MOSFET	0.9V	670 mV	40 nA	$0^\circ C$ to $80^\circ C$	10$ppm/^\circ C$	9.3%	-53dB	n/a	0.045mm^2
Giustolisi [17]	1.2 μm	MOSFET	1.2V	295.3 mV	3.58 μA	$-25^\circ C$ to $120^\circ C$	83.3-154.7$ppm/^\circ C$	$\sim 3.66\%$	n/a	n/a	0.23mm^2
Kinget [18]	90 nm	MOSFET	0.55V	247mV;241mV	23.63μA; 876.36μA	$-25^\circ C$ to $120^\circ C$	270$ppm/^\circ C$; 150$ppm/^\circ C$	4.45%; 7.45%	n/a	n/a	0.019mm^2; 0.07mm^2

Chapter 5

Conclusions

5.1 Main findings

The main findings of this dissertation are summarized below.

- Bandgap references with BJT-based diodes are unsuitable for sub-1V supply operation.
- Architectures, that reuse the current in the amplifier to bias the diodes, lead to low-power consumption.
- The use of DTMOSTs in an op-amp less architecture is demonstrated via working prototypes and post-layout simulations.
- The implemented topology can be easily ported across technologies. This is demonstrated by realizations in two different technology nodes -0.16μm and 40 nm.

5.2 Recommendations for Future Work

The following topics would be interesting to study in a future reference.

- Investigation into trimming schemes. It would be interesting to investigate improvement of the performance by single or multi-temperature trimming. Different options could be trimming either or both of R_1 and R_2, trimming the number of DTMOSTs in parallel and trimming the current through the output branch by a current DAC.
- Investigation of the effect of applying Dynamic Element Matching (DEM) to the diodes. It was observed that the major source of error was due to mismatch between the DTMOSTs. Applying a scheme such as DEM could help reduce the mismatch and thereby, spread of the output voltage.

- Investigation of improving the temperature-coefficient by some type of curvature-correction. Curvature-correction can be studied to improve performance. Solution could be inserting or removing some current from the output branch, as in [11].
- Investigation of circuit techniques for functioning at elevated temperatures. It was observed that the bulk-to gate leakage of DTMOSTs increases with temperature. It would be useful to devise a way for compensating this effect.
- Investigation into the possibility of adding a buffer at the output node. Currently, the developed topology is designed for a high impedance load (such as the gate of an NMOS transistor). Addition of a buffer at the output could improve the load regulation.
- Investigation of ways to improve the noise performance. Techniques such as chopping could be studied to improve the noise performance.

Appendix A

Trimming

Precision bandgap references employ trimming [11] to reduce their temperature coefficients and/or 3σ spread. Trimming schemes were not implemented in the current work. However, a preliminary investigation was carried out in MATLAB and is described in this appendix to study the impact of trimming.

For the implemented reference, the bandgap voltage is given by:

$$V_{bg} = V_{ctat} + R_2 I_{ptat} \tag{A.1}$$

From the measured prototypes in C14 (chapter 4), two results are available:

- The measured bandgap voltage, V_{bg}.
- The mirrored PTAT current, I_{ptat}.

The investigation is performed at the supply of 1.3 V (the worst case results for 3σ spread and temperature coefficient) as described in chapter 4 and repeated in Table A.1.
The strategy for trimming is as follows. It is assumed that resistive trimming is performed by trimming the resistor R_2, with nominal value of 425 kΩ. From the measured results of V_{bg} and I_{ptat}, V_{ctat} is estimated as:

$$V_{ctat} = V_{bg} - 425\text{k}\Omega \times I_{ptat} \tag{A.2}$$

For ease of implementation, it is assumed that a single temperature trim is performed. Generally, this is done at room temperature. However, for this exercise it is assumed that a single temperature trim could be performed at one of the following temperatures : −40 °C, −20 °C, 5 °C, 35 °C, 55 °C, 75 °C, 95 °C and 125 °C. These represent a fairly even distribution of temperatures over the desired range (−40 °C to 125 °C).

Table A.1: Measured Bandgap References at C14

Supply	3σ at room temperature	Tempco	Remarks
0.8		700ppm/°C	Insufficient supply
0.9	1.04%	43-84ppm/°C	Chip starts working at this supply
1	1.25%	50-90ppm/°C	
1.1	1.18%	71-110ppm/°C	Needs to be trimmed
1.2	1.30%	75-125ppm/°C	Needs to be trimmed
1.3	1.38%	77-140ppm/°C	Needs to be trimmed

At the desired trim-temperature, the mean of I_{ptat} is calculated for the measured samples. A suitable value of trim resistance, ΔR_2 is calculated for each sample such that each sample would have the obtained mean V_{ptat} at the trim temperature, when the measured I_{ptat} is multiplied by $R_2 + \Delta R_2$. Then the obtained value of I_{ptat} is multiplied by $R_2 + \Delta R_2$ and added to V_{ctat} to obtain the 'trimmed' V_{bg} for each sample.

$$V_{bg,trimmed} = V_{ctat} + (R_2 + \Delta R_2)\, I_{ptat} \tag{A.3}$$

The underlying assumption is that V_{ctat} and I_{ptat} do not change due to the resistive trimming. In reality, there will be some change specially in V_{ctat} due to change in bias current by changing R_2. However, it can be expected that this change should not alter the findings significantly. The obtained temperature coefficients and spread for each trim temperature is given in Table A.2 along with the change in the trim resistance ΔR_2.

Table A.2: MATLAB simulation results after trimming at different temperatures

Trim Temperature	3 sigma spread	Tempco	Delta R2
Untrimmed	1.80%	77-141 ppm/°C	0
-40 °C	1.01%	71-119 ppm/°C	-12 to 11 kΩ
-20 °C	1.70%	84-112 ppm/°C	-9.86 to 13.52 kΩ
5 °C	1.26%	79-118 ppm/°C	-9.62 to 12.53 kΩ
35 °C	1.39%	77-117 ppm/°C	-10.1 to 12.42 kΩ
55 °C	1.06%	81-112 ppm/°C	-11.68 to 12.08 kΩ
75 °C	1.36%	79-112 ppm/°C	-12.1 to 12.6 kΩ
95 °C	0.86%	87-108 ppm/°C	-13.33 to 9.84 kΩ
125 °C	0.50%	81-115 ppm/°C	-10.77 to 9.55 kΩ

From Table A.2, it can be seen that trimming should be performed at 125 °C. This entails a range of trim resistance of about 20 kΩ. In practice, it would be probably better to use a two temperature trimming scheme - first trimming at room temperature, followed by a trim at 125 °C. This is expected to yield the desired accuracy of about 100ppm/°C in the worst case with a 3 σ spread less than 1%.

Appendix B

Alternate sub-1V reference

A sub-1V bandgap reference has been presented in this thesis using only DTMOST as the diode-connected devices. An alternative solution is described in this appendix. The idea is basically adapted from the implementation in [12](Fig. B-1).

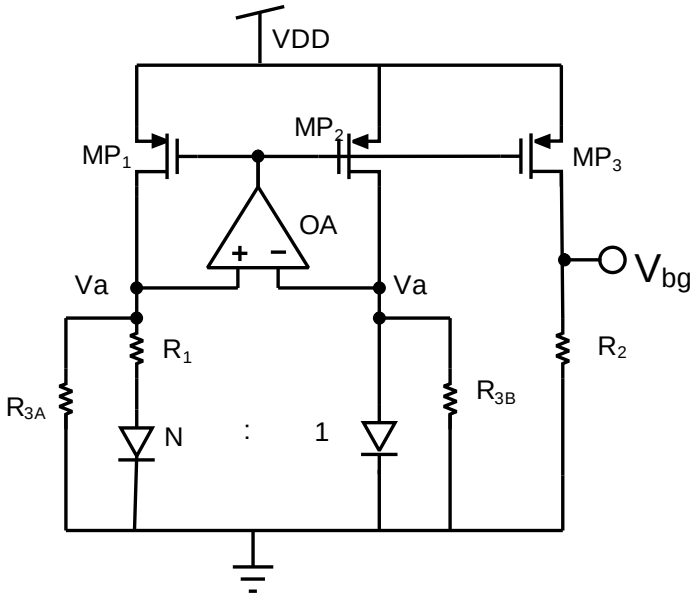


Figure B-1: Sub-1V reference from Banba. Note that the diodes represent diode-connected PNPs.

The problem in the architecture of Fig. B-1 was that the resistor R_{3B} had to be large (about 2 MΩ) as its value had to be comparable to the dynamic resistance ($\frac{1}{g_m}$) of the BJT diode so as to ensure sufficient bias current for the BJT diode. This problem can be solved using the architecture of Fig. B-2.

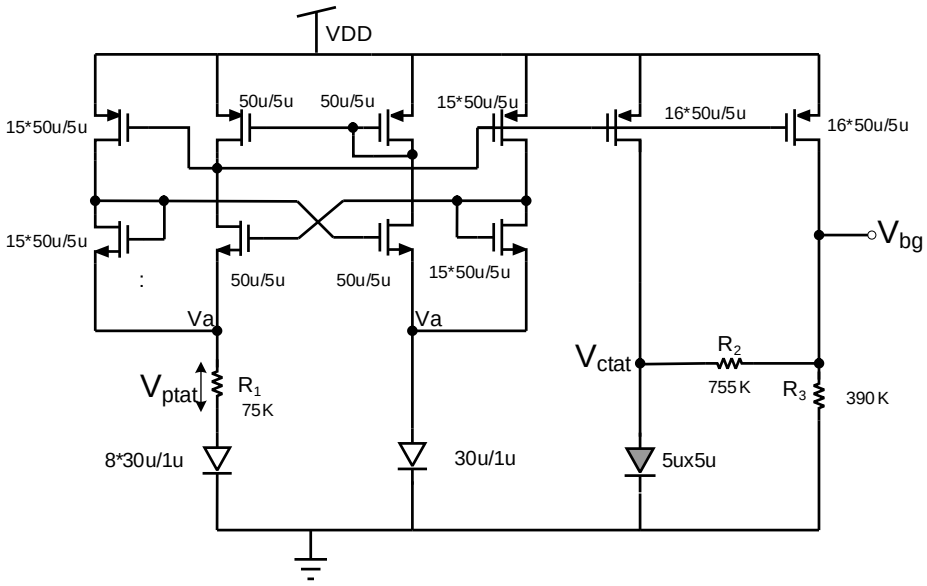


Figure B-2: Alternate sub-1V reference. Note that the grey diode represents a diode-connected PNP and the other two diodes represent diode-connected DTMOSTs.

In Fig. B-2, the grey diode represents a BJT diode (used to generate V_{ctat}) and the other two diodes are DTMOST diodes (used to generate V_{ptat}). When compared to the architecture in Fig. B-1, R_2 +R_3 have to be comparable to the dynamic resistance of the BJT diode. Therefore, the requirement on the resistor size is much smaller (the total resistor is 5 times less than in [12]). The bandgap voltage is given by:

$$V_{bg} = R_3 \parallel R_2 \left(\frac{V_{ctat}}{R_2} + \frac{V_{ptat}}{R_1} \right) \tag{B.1}$$

This topology has the following salient features:

- Scaling by the parallel combination of R_3 and R_2 makes this reference suitable for sub-1V operation. Furthermore, R_3 can be changed to make the output voltage scalable compared to the implemented topology.
- The error contribution due to V_{ctat} is reduced by the square of R_1 (as errors add up in root mean square fashion). Furthermore, a BJT diode is expected to spread less than a DTMOST diode. Therefore, this reference should spread less and have less temperature coeffficient than the implemented reference.
- The noise due to the current mirrors is reduced by $R_3 \parallel R_2$, compared to reduction by R_2 for the implemented reference and hence, this reference would have better noise performance.
- On the flip side, the area consumption is much larger for this reference, compared to the implemented reference. Hence, with a hard limit of 0.05 mm^2 for the reference, this topology was not implemented.

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