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## 18.3 An Auto-Zero Stabilized Voltage Buffer with a Quiet Chopping Scheme and Constant Input Current

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The readout of high impedance sensors and sampled voltage references [1] requires amplifiers that can achieve both low offset and low input current. Recently, it has been shown that this unique combination can be achieved by an auto-zero (AZ) stabilized buffer [2]. However, its low-frequency (LF) noise density is  $\sqrt{5}$  times higher than the buffer's own white noise density  $e_n$ . Furthermore, its input current is not constant, but varies significantly with the input voltage. To overcome the first issue, a chopped AZ stabilization loop with an optimized duty-cycle is proposed to bring the LF noise density close to  $\sqrt{2} \cdot e_n$ , the fundamental limit of an AZ stabilized amplifier. The second issue is solved by replacing the transmission-gate input switches used in [2] with NMOS switches and a constant  $V_{gs}$  drive. This keeps their charge injection constant over a wide input voltage range, and results in a constant input current.

As shown in Fig. 1, the AZ stabilized buffer consists of a buffer (BUF), whose offset ( $V_{os1}$ ) and  $1/f$  noise are periodically cancelled by a first AZ stabilization loop, which consists of an OTA (AZ1), an integrator (INT and  $C_{int11-int12}$ , 10pF each) and an OTA (AZ3) [2]. AZ1 is itself auto-zeroed by a second AZ loop that consists of another integrator (INT and  $C_{int21-int22}$ , 10pF each) and another OTA (AZ2). To prevent noise folding, the correction range of both AZ loops is quite small ( $\sim 500\mu V$ ). So a digitally-assisted AZ loop [2] is used to trim the mV offsets of AZ1 and BUF at startup (Fig. 2).

The minimum LF noise density of the AZ stabilized buffer is  $\sqrt{5} \cdot e_n$  [2], where  $e_n$  is the white noise density of AZ1 and BUF (Fig. 1). This can be intuitively understood as follows. During phase  $\Phi_1$  the first AZ loop cancels the LF noise of BUF, while AZ1 contributes noise both directly and via the previously stored noise at nodes EF, leading to a total contribution of  $\sqrt{2} \cdot e_n$ . During phase  $\Phi_2$  the noise of BUF, AZ1 and the noise of AZ1 held on nodes EF is stored on nodes GH, leading to a total contribution of  $2 \cdot e_n$ . Assuming a 50% AZ duty cycle, the noise over the two phases would be  $\sqrt{3} \cdot e_n$ . However, the correlation of the sampled AZ1 noise at nodes EF in both phases leads to a LF noise of  $\sqrt{5} \cdot e_n$ .

In order to remove this correlation, the AZ stabilization loop is chopped (Fig. 1). Choppers around AZ1 periodically invert the polarity of the noise held at nodes EF on its way to nodes GH. Over one chopping period, this should cancel its noise contribution, reducing the LF noise floor to  $\sqrt{3} \cdot e_n$ . Since the second AZ loop is still active, however, the noise held at nodes EF will slowly change during chopping and so will not be perfectly cancelled. The amount of change depends on the duration of the chopping period, and hence on the AZ frequency  $f_{AZ}$ . Setting  $f_{AZ} = 15\text{kHz}$ , which is enough to cancel the buffer's  $1/f$  noise, only reduces the LF noise floor slightly (Fig. 1). To approach the  $\sqrt{3} \cdot e_n$  limit, simulations show that  $f_{AZ}$  would have to be some  $3 \times$  higher, resulting in significantly more input switching, and hence, more input current.

To preserve the noise on nodes EF during a chopping period, extra integration capacitors  $C_{int31-int32}$  (1pF each) are used to implement a modified  $\Phi_2$  phase, denoted by  $\Phi_3$  (Fig. 1). During  $\Phi_3$ , nodes EF are not connected to the output of INT. Also, resistors  $R_{1,2}$  (2M $\Omega$ ) limit the gain of INT, preventing it from clipping due to the residual output current of AZ1 (Fig. 1). The noise at nodes EF can then be perfectly chopped without changing  $f_{AZ}$ . The chopping transitions are arranged to occur in phase  $\Phi_2$ , when the input chopper is disconnected from the input by the AZ switches. With these two measures, the AZ stabilization loop can be chopped without introducing extra spikes or input current.

Another challenge is the offset of the integrator, which, via the chopper at its input, appears as a square-wave ripple voltage at the output of AZ1. This will be translated into a ripple voltage at the input of the buffer via the transconductance and finite output impedance of AZ1. With an expected integrator offset of about 2mV, the output impedance of AZ1 should be quite high ( $>150\text{M}\Omega$ ) to ensure that the resulting ripple is negligible ( $<100\text{nV}$ ). This requirement is met by implementing AZ1 as a folded cascode OTA.

The buffer's noise level can be further reduced by adjusting the  $\Phi_1$ :  $\Phi_2$  duty-cycle, noting that the noise in phase  $\Phi_1$  ( $\sqrt{2} \cdot e_n$ ) is less than the noise in phase  $\Phi_2$  ( $2 \cdot e_n$ ). So the more time the buffer spends in phase  $\Phi_1$ , the closer its noise gets to  $\sqrt{2} \cdot e_n$ . Since some settling time is required for  $\Phi_2$ , the resulting noise level will then be somewhere between  $\sqrt{3} \cdot e_n$  and  $\sqrt{2} \cdot e_n$ .

In [2], the input switches are implemented as transmission gates. Depending on the input voltage, this means that either the NMOS, PMOS or both devices will be turned "off" by clock transitions. Their charge injection, and thus, the input current will then be dependent on the input voltage (Fig. 3), typically changing by about 0.9 pA over the buffer's input voltage range (0 to 1.3V). In this design, the input switches are implemented as NMOS switches. Half-sized dummy transistors are used to partially cancel their charge injection. The NMOS switches are driven at constant  $V_{gs}$  by a circuit consisting of two latching transistors (MN1,2) and two boosting capacitors (CB1,2), which ensure that the clock waveform is superimposed on the input voltage. A simple buffer drives the capacitors, ensuring that their charging current does not load the buffer's input. Measurements show that the resulting input current is quite constant, varying by less than 0.2pA with input voltage (Fig. 3). As in [2], the input current is measured by observing the discharge of the hold capacitor  $C_H$  ( $= 36\text{pF}$ ) of an on-chip low-leakage S&H circuit.

The buffer was realized in a 0.18  $\mu\text{m}$  CMOS process (Fig. 7). It draws 210  $\mu\text{A}$  from a 1.8V supply, and has an active area of 0.55  $\text{mm}^2$ , 0.12  $\text{mm}^2$  of which is occupied by the S&H circuit. With a 1V input and  $f_{AZ} = 15\text{kHz}$ , measurements show that its input current is below 0.8 pA (15 samples), and that its offset does not exceed 0.4  $\mu\text{V}$  (Fig. 4). In Fig. 5, the buffer's voltage noise density is shown. With auto-zeroing alone, a LF noise density of 31  $\text{nV}/\sqrt{\text{Hz}}$  is achieved, which equals the  $\sqrt{5} \times$  noise limit. When chopped with the extra  $\Phi_3$  phase enabled, the LF noise drops to 25  $\text{nV}/\sqrt{\text{Hz}}$ , which equals the  $\sqrt{3} \times$  noise limit. Finally when a 75% duty-cycle is used, a LF noise of 20  $\text{nV}/\sqrt{\text{Hz}}$  is achieved, which is very close to the  $\sqrt{2} \times$  noise limit. This reduction from  $\sqrt{5} \times$  to  $\sqrt{2} \times$  noise corresponds to a 2.5 $\times$  power saving in the input stages. No tones at  $f_{AZ}$  or  $f_{CH}$  can be seen, demonstrating that the use of chopping does not add spikes. While the 75% duty-cycle does not change the offset or input current.

In Fig. 5, the input current vs input voltage of a typical sample is shown. With and without chopping, no significant difference in input current can be seen. The voltage drift across  $C_H$  is also shown (typical sample, 1V input). With AZ off, no drift can be seen, illustrating that the leakage of the S&H is indeed negligible. Furthermore, a measurement of the input current vs  $f_{AZ}$  shows a linear relationship, which indicates that charge injection is the dominant source of input current. In Fig. 6 the performance of the auto-zeroed voltage buffer is summarized and compared with the state-of-the-art. A special chopping scheme allows it to achieve a LF voltage noise of 20 $\text{nV}/\sqrt{\text{Hz}}$ , while also achieving a constant and low input current (0.8 pA), as well as state-of-the-art offset (0.4  $\mu\text{V}$ ).

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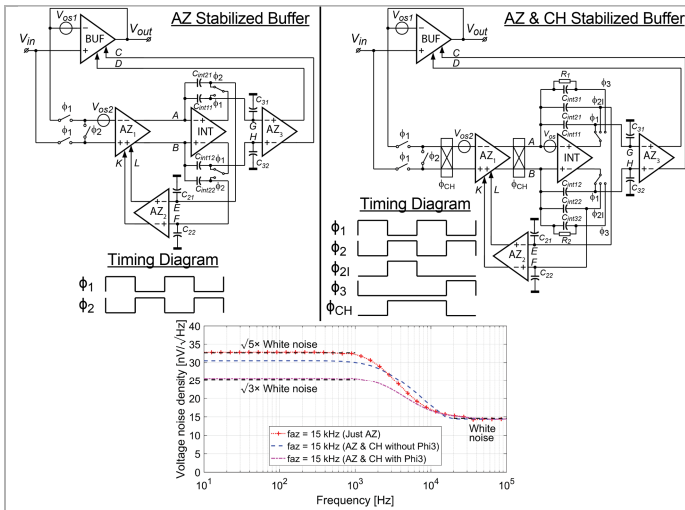


Figure 18.3.1: An auto-zero stabilized buffer without and with a chopped stabilization loop and additional  $\Phi_3$  phase. Voltage noise density simulation for different configurations (AZ, AZ&CH without and with  $\Phi_3$ ).

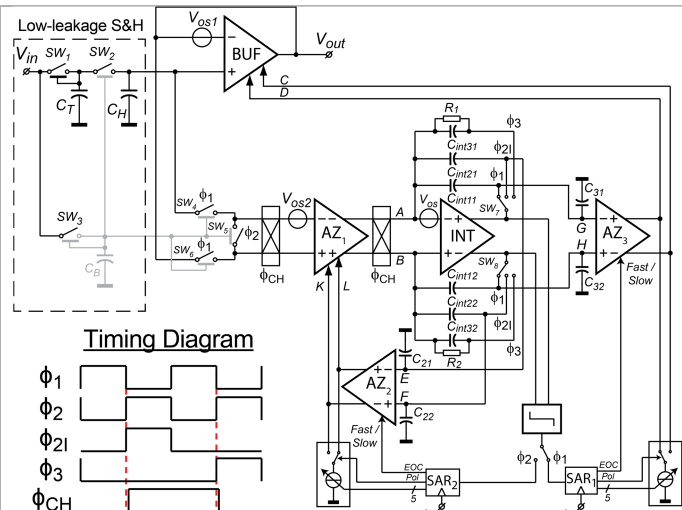


Figure 18.3.2: Block diagram of the auto-zero stabilized voltage buffer with chopped stabilization loop and digital assistance.

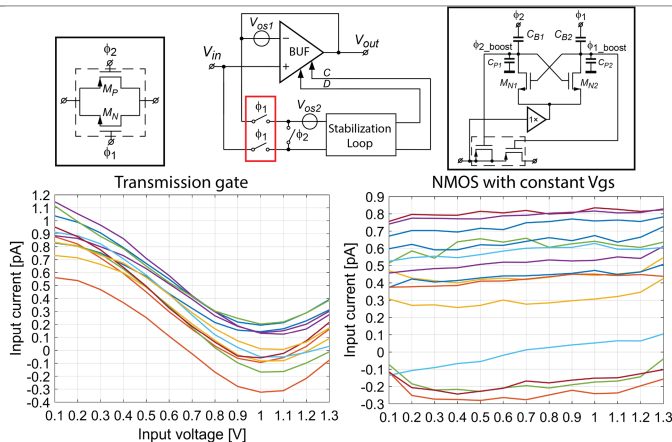


Figure 18.3.3: Measured input current vs input voltage for different type of input switches: transmission gates (Left) and NMOS with constant  $V_{gs}$  drive (Right).

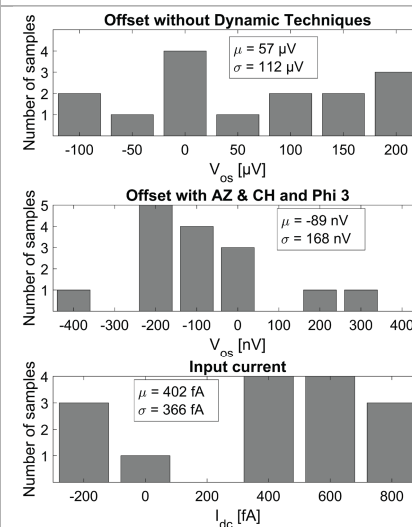


Figure 18.3.4: Histograms (15 samples) of the measured offset (without and with AZ) and input current with AZ&CH and  $\Phi_3$  ( $f_{AZ} = 15$  kHz,  $V_{in} = 1$  V).

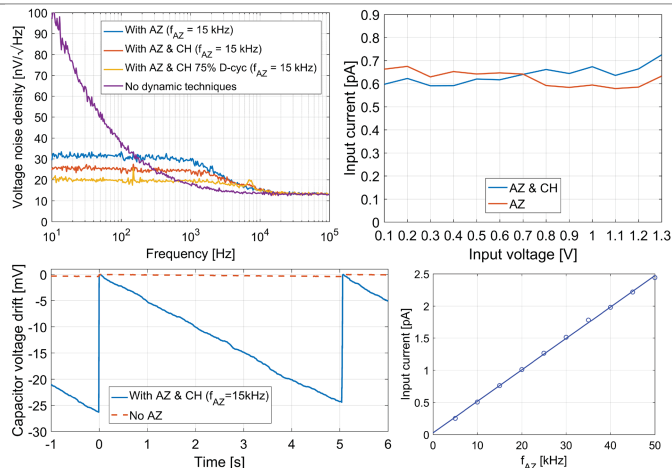


Figure 18.3.5: Measured voltage noise PSD: No AZ, with AZ and with AZ & CH (Top left). The input current vs the input voltage for a typical sample for AZ and AZ&CH (Top right). The capacitor voltage drift of a typical sample with and without AZ & CH (Bottom Left). The input current vs AZ frequency with chopped stabilization loop (Bottom Right).

	This work	[2]	[3]	[4]	[5]	[6]	[7]
Dynamic technique(s)	<b>Auto-zeroing and Chopped Stabilization</b>	Auto-zeroing	Chopping	Chopping and Auto-zeroing	Chopping and Auto-zeroing	Auto-zeroing	Chopping and Auto-zeroing
Input current (Max)	<b>0.8 pA</b>	0.6 pA	72 pA	40 pA	-	50 pA	-
Offset (Max)	<b>0.4 <math>\mu</math>V</b>	0.6 $\mu$ V	0.78 $\mu$ V	3 $\mu$ V	2.8 $\mu$ V	5 $\mu$ V	4 $\mu$ V
Voltage noise (nV/ $\sqrt$ Hz)	<b>31 (AZ) 25 (AZ&amp;CH) 20 (75% AZ&amp;CH)</b>	29	5.9	20	38 (AZ) 27 (CH&AZ)	75	140 (AZ) 28 (CH&AZ)
NEF	<b>7.3</b>	7.4	8.7 <sup>a</sup>	21.8 <sup>a</sup>	43.5 <sup>a</sup>	-	-
GBW (MHz)	<b>1.45</b>	1.45	4	2.5	0.8	1	-
PSRR (dB)	<b>125</b>	125	142	-	138	130	128
Frequency (kHz)	<b>15 (<math>f_{AZ}</math>) / 7.5 (<math>f_{CH}</math>)</b>	15	200	15 ( $f_{CH}$ ) / 7.5 ( $f_{AZ}$ )	28 ( $f_{AZ}$ ) / 14 ( $f_{CH}$ )	4	11 ( $f_{CH}$ ) / 7.33 ( $f_{AZ}$ )
Supply current	<b>210 <math>\mu</math>A</b>	210 $\mu$ A	1.47 mA	800 $\mu$ A	1.7 mA	750 $\mu$ A	480 $\mu$ A
Supply voltage	<b>1.8 V</b>	1.8V	2.5 - 5.5 V	5 V	2.7 - 5.5 V	2.7 V	3.3 - 5.5 V
Technology	<b>0.18 <math>\mu</math>m</b>	0.18 $\mu$ m	0.35 $\mu$ m	0.6 $\mu$ m	0.5 $\mu$ m	-	0.5 $\mu$ m
Die area (mm <sup>2</sup> )	<b>1.4<sup>b</sup></b>	1.4 <sup>b</sup>	1.26	0.67	2.5	-	1.48

Figure 18.3.6: Performance summary and comparison with previous works.  
<sup>a</sup> Estimated value [3] <sup>b</sup> 0.12 mm<sup>2</sup> of which is occupied by the S&H circuit

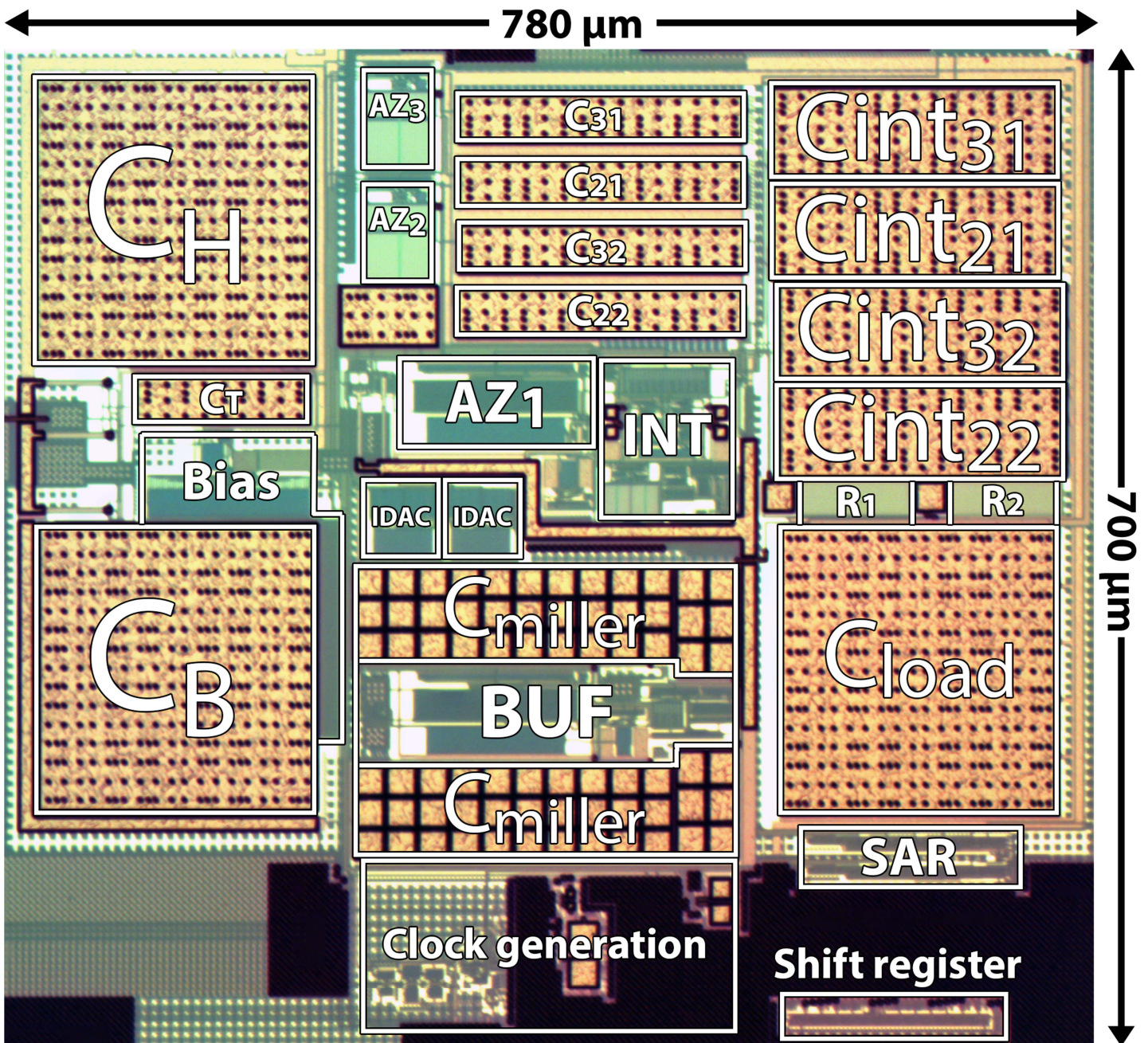


Figure 18.3.7: Chip micrograph of the active area.