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The Efficiency and Power Utilization of Current-Scaling Digital Transmitters

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***Abstract*— The RF performance of current-scaling digital transmitters (DTX) with polar, unsigned Cartesian, signed Cartesian, and multiphase architectures have been compared regarding power utilization of their output-stage switch banks and drain efficiency. The analysis includes various switch bank operation modes, such as switch bank sharing, segment activation interleaving, and their activation times (RF duty cycle of the segments). Current-scaling DTXs can be made compatible with high-power operations while offering high system efficiency and RF bandwidth. The average efficiency using Doherty power back-off efficiency enhancement is analyzed, and a comparison of the different proposed DTX implementations is presented.**

***Index Terms*— Current mode, current scaling, digital transmitter (DTX), Doherty, efficiency, multiphase, peak-to-average-power ratio (PAPR), polar, power utilization, RF-DAC, signed Cartesian (SC), upconversion.**

I. Introduction

DIGITAL transmitters (DTXs) can offer higher integration and system efficiency than their analog counterparts. However, DTXs come in different flavors, each with benefits and shortcomings. This work provides the theoretical background of current-scaling DTXs, which show remarkable properties in terms of drain efficiency, linearity, RF bandwidth, and scaling of their output power. Furthermore, these transmitters have relaxed demands on their output-matching network and breakdown voltage, which are comparable to those used in analog class-B transmitters. However, different from analog designs, input matching is omitted, allowing a close to perfect frequency-agile operation of transmitter output stages without any stability issues [1].

Current-scaling DTXs use segmented output stages preferably operating in saturated, or current-limited, mode (Fig. 1). The total RF output signal results from the current summation in the segmented output stages, referred to as switch banks. The output stage segments act to a great extent like current sources, which are digitally controlled by an amplitude codeword (ACW). Doing so, the effective gate width (w_g) of the output device is scaled, rather than the drain current (i_d) as a function of the gate voltage (v_{gs}), as is the case in analog implementations. Since the output current scales (in first-order approximation) linearly with the ACW, current-scaling DTXs behave linearly up to the point, where g_m drops due to compression [2].

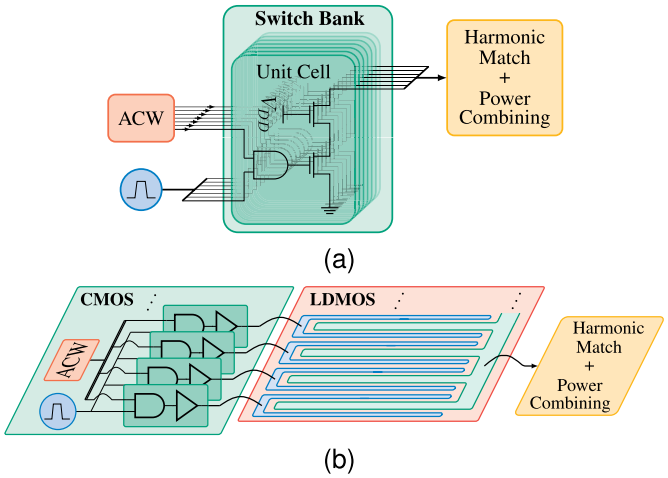

Fig. 1. Simplified concept illustrations of current-scaling DTX approaches (a) low-power CMOS DTX switch bank using unit cells and (b) high-power LDMOS DTX switch bank with CMOS driver DTX using gate segmentation in its output stage.

All segments of the switch bank are directly connected to the drain terminal; therefore, the combined output capacitance of the segments is $C_{\text{out}} = C_{\text{ds,bank}}$. At the input of the switch bank(s), the effective loading of the individual drivers for the equal-sized gate segments is $C_{\text{gs,bank}}/N$, where $C_{\text{gs,bank}}$ is the gate capacitance of the total bank, and N is the number of gate segments [1]. In the case of a high-power, dual-chip implementation, the bond wires introduce a parasitic inductance. The resonance frequency of this inductance combined with the segment gate capacitance $C_{\text{gs,bank}}/N$ should be well above the operating frequency. Additionally, the mutual inductance between the bond wires should be minimized [1]. C_{out} will have a significant value when aiming for higher output powers. Consequently, C_{out} needs to be compensated by the output matching network when operating at RF. To handle C_{out},

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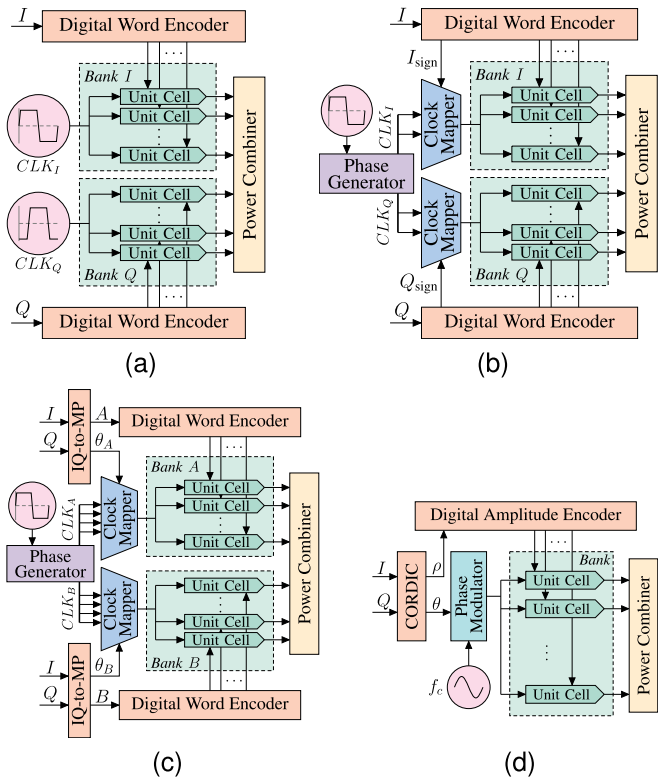

Fig. 2. Top-level block diagrams of four g_m-scaling DTX architectures. (a) Unsigned Cartesian configuration using fixed clocks, (b) SC configuration using a clock mapper to switch the I and Q clocks by 180°, (c) multiphase configuration, using more clock phases, and (d) polar configuration using a continuously varying phase-modulated clock to drive the (single) switch bank.

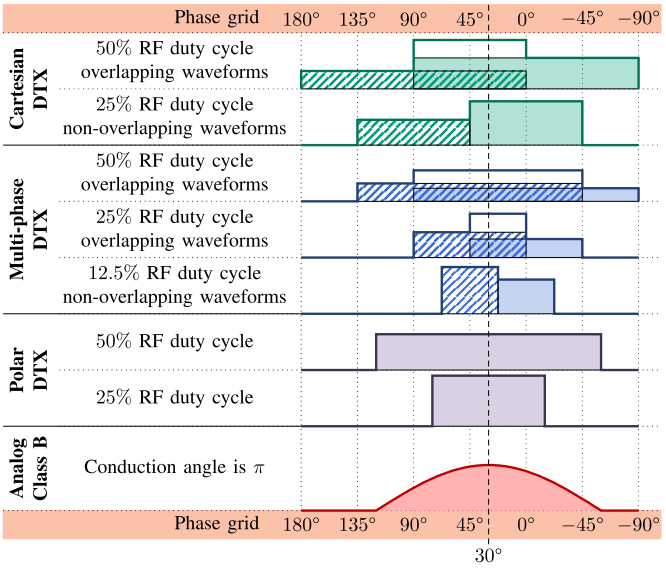

Fig. 3. Exemplary waveforms for the different DTX architectures using different RF duty cycles, addressing the IQ-point $(3)^{1/2}/2+1/2j$, or $\rho_{\mathrm{BB}} = 1$ and $\theta_{\mathrm{BB}} = 30°$. The multiphase waveform has a smaller effective duty cycle than Cartesian concepts, yielding a better approximation of the polar architecture.

conventional analog transmitters mostly employ class-B-like matching to reach the best compromise between linearity, efficiency, and RF bandwidth, even though other operating classes (e.g., class-F) promise higher theoretical efficiency. However, these operating classes typically rely on open conditions for some of their harmonics (e.g., the third for class-F), which is difficult to achieve over a large bandwidth when C_{out} is high. Continuous operating classes [3] can offer higher bandwidth, but this comes at the expense of higher drain voltage swings and varying complex loading conditions across the frequency band of interest, of which the latter is challenging to combine with N-way wideband Doherty operation.

Furthermore, in contrast to analog implementations, where the current waveform is a half-sine wave, DTX typically operates with square-wave-shaped drain currents due to the digital (voltage) control of its gate segments. A square wave drain current will have a higher fundamental content (boosting the output power) than a rectified half-sine wave drain current having the same amplitude and (RF) duty cycle. However, the 50% duty cycle of a square wave also yields a more extensive overlap with the typical sinusoidal drain voltage resulting from class-B operation, increasing the power dissipation of the output stage switch bank. Likewise, as in analog, there is a direct relationship between the duty cycle (thus, conduction angle) of the DTX-generated drain current pulses, the output power, and efficiency. However, unlike in analog class-C operation, which suffers from gain expansion, in a current-scaling DTX transmitter, the linearity of the transfer (e.g., ACW−RF output current) is inherently preserved when changing the amplitude [2]. In DTX, the duty cycle is an important design parameter and will, therefore, be included in our discussions.

This article first provides an overview of different (current scaling) DTX upconversion and switch bank architectures and, second, compares them for output power and efficiency. Third, the theoretical analysis is verified by measurements, and finally, a comprehensive literature review is performed in which alternative DTX architectures are compared for their output power and peak-to-average-power ratio (PAPR).

II. Types of Upconversion Architectures

Four different current-scaling DTX architectures are considered in this work (Fig. 2). They range from Cartesian, which is suited for handling wide modulation bandwidths, to efficient "narrow-band" polar TX lineups. Next, we will discuss their operation principles.

A. Unsigned Cartesian DTX

The unsigned Cartesian DTX architecture uses two nonmodulated clocks to perform the baseband-IQ to RF upconversion [Fig. 2(a)] [4], [5], [6]. Because of this, the clocks used in the switch banks cannot be adjusted for their activation phase, so the activation itself must always be positive. Consequently, only class-A-like operation is possible, and the input IQ data are shifted to the top-right quadrant, as shown in Table I. As a result, this architecture suffers from a high constant dc current in the output stage, which cannot be tolerated in a high-efficiency transmitter concept. However, this constant current tends to reduce the impact of bias network-induced memory effects, making this configuration highly linear and, therefore, an attractive option for direct digital RF modulators (DDRMs) [4], [5]. Since the emphasis of this work is on

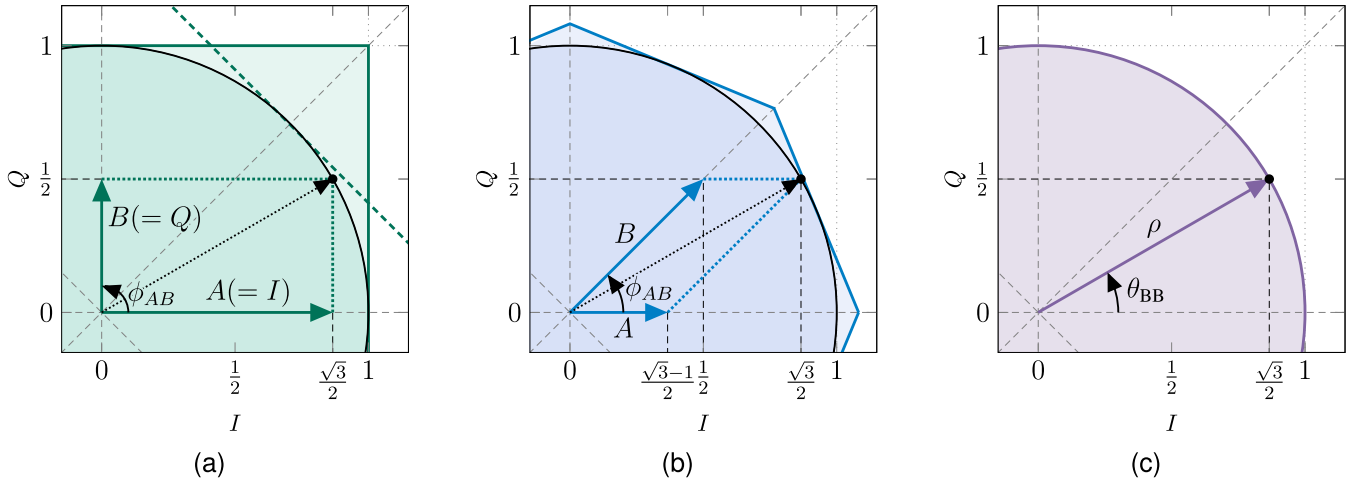

Fig. 4. Plots showing the top-right quadrant of the IQ plane with vector representations of the IQ point $(3)^{1/2}/2 + 1/2j$, using a DTX architecture based on (a) SC (green), (b) (eight-phase) multiphase (blue), and (c) polar (purple) architectures.

high-efficiency TX output stages, we will, in the following paragraphs, focus on the DTX architectures capable of achieving higher efficiencies.

B. Signed Cartesian DTX

In an SC architecture [Fig. 2(b)], both the in-phase (I) and quadrature (Q) clocks can be switched by 180° [6], [7], allowing for negative I and Q values to be transmitted by shifting the RF phase of a positive activation by 180°. For consistency in this work, we define the two (current) summing vectors as A and B, with a phase angle ϕ_{AB} between them. For SC, $A = I$, $B = Q$, and $\phi_{AB} = 90°$ (Table I). In this case, the phase mapper selects the required clocks from four input clocks based on the sign bits of the original I and Q data [8]. Fig. 3 provides an example of the time domain current waveform that addresses the IQ point $(3)^{1/2}/2+1/2j$, or $\rho_{\mathrm{BB}} = 1$ and $\theta_{\mathrm{BB}} = 30°$. It should be mentioned that the positive phase shifts lag in time, in correspondence to the trigonometry: $\rho_{\mathrm{BB}} \cos(\omega_0 t + \theta_{\mathrm{BB}}) = I \cos(\omega_0 t) - Q \sin(\omega_0 t)$. Fig. 4(a) illustrates the corresponding vector summation of the current pulses. Digital word decoders send the in-phase and quadrature amplitudes to the unit cells in the corresponding banks.

SC DTX supports class-B-like operation since quiescent currents are no longer required, and the switch bank can cover all quadrants. Furthermore, the I and Q paths are very similar in terms of their hardware, and the amplitude decoder and the phase mapper can operate synchronously in a clocked domain. It should be noted that, due to the splitting of the sign and amplitude information, the SC operation is, in its essence, not fully linear. Namely, the phase mapper is effectively a high-speed, 1-bit phase modulator, creating a phase-modulated clock. Moreover, taking the absolute value of a signal is also a nonlinear operation. Only after combining the amplitude data and phase-modulated clock in the switch banks, the desired (linear) output signal is retrieved. Due to its digital nature, the amplitude and phase paths operate in a fully synchronous, clocked domain, allowing the handling of wideband modulated signals.

However, the 90° phase angle between the vectors [as shown in Fig. 4(a)] unfortunately results in complex loading conditions arise for the I and Q switch banks when both are active. As a consequence, the efficiency of a Cartesian DTX is compromised for the off-axis constellation points, which is discussed in detail in Section V-C.

C. Multiphase DTX

The SC architecture can be extended to operate with more than four possible phases (e.g., with eight phases) to drive its cells: yielding the multiphase architecture [Fig. 2(c)] [6], [9], [10], [11], [12], [13]. Doing so, the phase angle (ϕ_{AB}) between the clocks driving the unit cells (or gate segments) in the switch bank is reduced, alleviating the reactive loading of the switch bank segments for off-axis constellation points. As such, increasing the efficiency for these points compared with the SC operation [Figs. 4(b) and 5]. Further increasing the number of driving phases for the unit cells in the switch banks, e.g., from 8 to 16 or more, yields an even closer approximation of the behavior of the polar architecture. The phase angle between the vectors equals 360° divided by the number of phases (assuming uniform distribution), yielding 45° for eight-phase and 22.5° for 16-phase operations.

For multiphase operation, the input IQ data needs to be mapped to the A and B vectors, with their corresponding activation phases (see Tables I and II) [9]. This phase selection again can be performed by the phase mapper [6], which controls the moment of activation by selecting the proper clocks provided by the phase generator, using the eight-phase grid (Fig. 3). Just like in the SC architecture, the high-speed phase selection is performed in the clocked domain, and thus, the amplitude and phase of the switch bank can be updated synchronously. Mapping the IQ data to A and B vector representations over more than four phases compromises the orthogonal nature of the TX unit, compared with working with the IQ data directly. This feature can affect the spectral purity when dealing with very high modulation bandwidths (e.g., beyond 200 MHz). However, the synchronous operation

TABLE I

IQ (BASEBAND) DATA MAPPING TO POLAR, CARTESIAN, SC, AND EIGHT-PHASE DTX SIGNAL REPRESENTATIONS

Unsigned Cartesian	Signed Cartesian	8-phase operation	Polar
$A = \frac{I+1}{2}$ $B = \frac{Q+1}{2}$	Vector amplitude: $A = \lvert I\rvert$ and $B = \lvert Q\rvert$ Phase selection: $\mathrm{sgn}(I)$ or $\mathrm{sgn}(Q)$	$A = \lvert\lvert I\rvert - \lvert Q\rvert\rvert$ $B = \sqrt{2}\min(\lvert I\rvert, \lvert Q\rvert)$	$\rho = \sqrt{I^2+Q^2}$ $\theta = \mathrm{atan2}(Q, I)$

TABLE II

SELECTION OF THE DRIVING BANK PHASES FOR THE EIGHT-PHASE OPERATION

Octant	Logic Expression	θ_A	θ_B
I	$(I \geq 0) \wedge (Q \geq 0) \wedge (\lvert I\rvert \geq \lvert Q\rvert)$	0	$\frac{\pi}{4}$
II	$(I \geq 0) \wedge (Q \geq 0) \wedge (\lvert I\rvert < \lvert Q\rvert)$	$\frac{\pi}{2}$	$\frac{\pi}{4}$
III	$(I < 0) \wedge (Q \geq 0) \wedge (\lvert I\rvert < \lvert Q\rvert)$	$\frac{\pi}{2}$	$\frac{3\pi}{4}$
IV	$(I < 0) \wedge (Q \geq 0) \wedge (\lvert I\rvert \geq \lvert Q\rvert)$	π	$\frac{3\pi}{4}$
V	$(I < 0) \wedge (Q < 0) \wedge (\lvert I\rvert \geq \lvert Q\rvert)$	π	$\frac{3\pi}{4}$
VI	$(I < 0) \wedge (Q < 0) \wedge (\lvert I\rvert < \lvert Q\rvert)$	$-\frac{\pi}{2}$	$-\frac{3\pi}{4}$
VII	$(I \geq 0) \wedge (Q < 0) \wedge (\lvert I\rvert < \lvert Q\rvert)$	$-\frac{\pi}{2}$	$-\frac{\pi}{4}$
VIII	$(I \geq 0) \wedge (Q < 0) \wedge (\lvert I\rvert \geq \lvert Q\rvert)$	0	$-\frac{\pi}{4}$

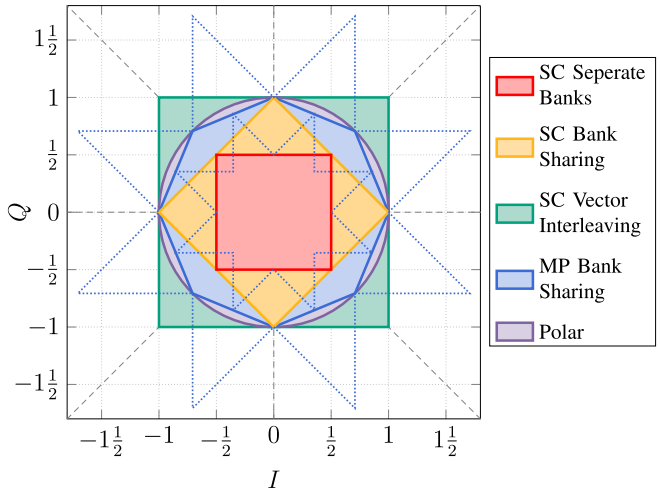

Fig. 5. Effective DTX signal constellation-area coverage for a given fixed total (normalized) gate width of the switch bank. For the SC operation using: separate banks (red), bank sharing (yellow), and segment activation interleaving (green); multiphase (MP) operation using bank sharing (blue); and polar operation (purple). The dashed blue lines refer to the possibility of multiphase operation with two dedicated switch banks (small area) and segment activation interleaving (larger area).

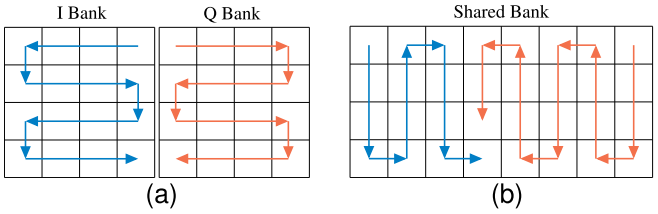

Fig. 6. Switch bank activation (a) without IQ sharing, using separate banks, and (b) with IQ sharing, using one combined bank for I and Q data.

of a multiphase transmitter makes this modulation bandwidth limitation much less severe than in polar architectures.

D. Polar DTX

In a polar architecture, there is only one activation phase for the switch bank, which is typically created by a high-resolution phase modulator, using a CORDIC to determine its digital phase word [Fig. 2(d)] [14], [15], [16], [17], [18]. The number of activated unit cells/gate segments directly sets the RF output amplitude without any vector summation. For this reason, maximum efficiency and output power can be achieved at any phase (Fig. 5). However, a CORDIC implements a nonlinear IQ-to-amplitude and phase transformation (see Table I), yielding severe bandwidth expansion [19], [20], [21]. Furthermore, the amplitude and phase paths are not synchronized (Fig. 3), requiring exact time alignment of these paths when they combine in the output stage to reconstruct the desired output signal. Any minuscule delay mismatch between the amplitude and phase path will result in severe adjacent channel power ratio (ACPR) and error vector magnitude (EVM) degradation, especially for wideband signals. In practice, excellent time alignment is not easy to achieve due to the different hardware nature of the two paths. As a result, practical polar transmitter implementations are generally considered unsuited for high-modulation bandwidths (e.g., beyond 100 MHz) when high linearity is required.

III. SWITCH BANK UTILIZATION IMPROVEMENTS

When using vector summation in Cartesian and multiphase architectures, a straightforward DTX implementation uses a separate switch bank for each vector, as indicated in Fig. 6(a) [22]. Assuming an output stage with a total of N unit cells/gate segments, with each single bank having $N/2$ unit cells, the maximum (current) output contour for this architecture is limited by $A_{\max} = N/2$ and $B_{\max} = N/2$. This arrangement limits the maximum output power along the A- and B-axes by a factor $1/2$ compared with a polar architecture that can activate all its N unit cells at any phase (see Fig. 5).

Next, two techniques to improve the switch bank utilization and, thereby, the output current/power utilization is discussed, namely, switch bank sharing and segment activation interleaving.

A. Switch Bank Segment Sharing

When using switch bank segment sharing, a single output-stage switch bank with N segments generates both the A and B (current) vectors. Each of its segments can be activated (within an RF cycle) at either the A or the B phase [see Fig. 6(b)]

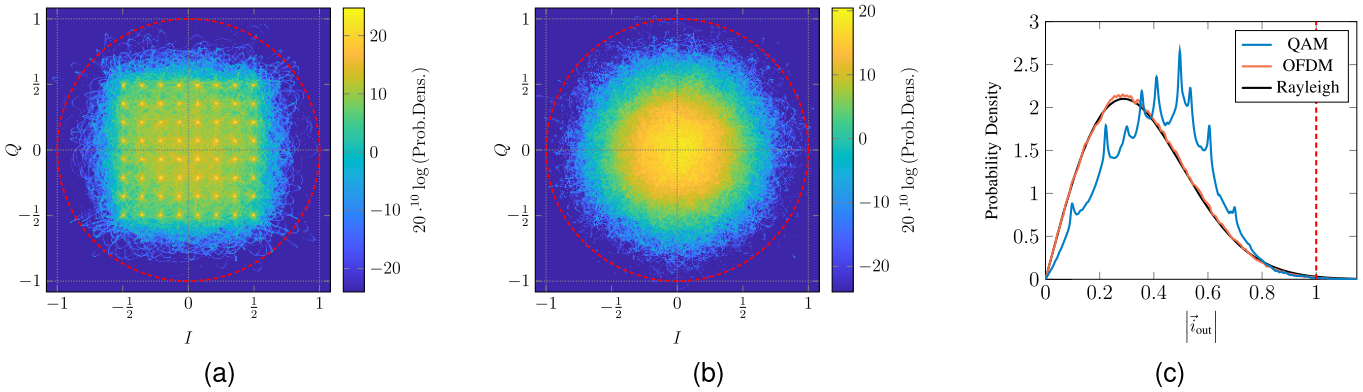

Fig. 7. (a) Heatmap of the probability density of a resampled QAM signal centered around its carrier frequency, resulting in a square-like coverage of the IQ output plane. (b) Probability density of a 16-channel OFDM upconversion, resulting in a circular coverage of the IQ plane and is, thus, independent of the phase. (c) Probability density plot of the amplitude of the QAM and OFDM signals, the latter follows the Rayleigh distribution.

[23], [24], [25]. Assuming a shared bank with N segments in total, the maximum output contour is given by the relation $A_{\max} + B_{\max} = N$. The lowest maximum output power occurs when $A = B$, i.e., $\theta_{\mathrm{BB}} = \phi_{AB}$. Especially, for a multiphase architecture, this technique greatly improves the output power utilization, allowing its output power contour to approximate that of a polar architecture (Fig. 5).

To avoid one segment being activated for both the A and B data, the activation order typically starts from opposite sides of the switch bank, as shown in Fig. 6(b) [26]. Using segment sharing, the switch bank can be activated completely along the in-phase and quadrature axes. As a result, the maximum output is also achieved at these axes. The effective constellation area coverage of such a DTX is a 45° rotated square (Fig. 5). A snake-like activation pattern can be used to improve the differential nonlinearity (DNL) (Fig. 6) [24].

When using quadrature amplitude modulated (QAM) signals, which cover a (more or less) square area [Fig. 7(a)], in the SC operation, IQ-data mapping can be applied to maximize the usage of this output current/power capability. The related mapped values of I' and Q' are simply calculated as follows [25]:

$$I' = I + Q \quad Q' = I - Q. \tag{1}$$

B. Switch Bank Segment Activation Interleaving

The output power utilization of the switch bank can be further improved by applying switch bank segment activation interleaving. In this activation technique, each unit cell/gate segment can be activated at both the A and the B vector phases within one RF cycle [4]. Therefore, the entire output switch bank is fully available for both vectors, yielding a maximum output contour given by the relation $A_{\max} = N$ and $B_{\max} = N$, for a switch bank with a total of N segments. The lowest achievable peak output power occurs along the vector axes and is equal to the polar architecture. At off-axis constellation points, even higher output powers can be obtained, yielding a square-shaped output current contour in the SC operation. In multiphase operation, the constellation area becomes star-like, adding only a minimal increase of its effectively usable area coverage compared with bank sharing, as we will discuss further in Section IV-B.

Moreover, when using the activation interleaving technique, the waveforms created by the A and B vectors should be nonoverlapping (Fig. 3). Therefore, in this case, the maximum RF duty cycle $d \leq \phi_{AB}/360°$ for the switch bank segments activation (Fig. 3).

Finally, the rise and fall times, in combination with the nonlinear v_{gs}–i_{ds} relation of practical devices, will reduce the effective RF duty cycle of the activated switch bank segments. Using segment activation interleaving, a single segment can be activated twice within one RF cycle. In between the two consecutive activations, the active device possibly does not switch (completely) off due to nonzero rise and fall times. The resulting effective activation is not equal to the sum of two separate activations. In other words, the two vectors interact, which will compromise the spectral purity.

IV. DTX Output Power Comparison

The previously described DTX architectures, with their various switch bank activations, provide different coverages of the IQ constellation plane with their TX signals. Therefore, meaningful normalization is required to compare their output power capability. Based on the normalized output powers, we compare the different architectures for their (maximum) output power, after which we discuss the effect of the RF duty cycle on the output power. Finally, some other performance considerations regarding w_g and the output matching strategy are discussed.

A. Normalization

The coverage of the IQ constellation plane is in this article considered in the current domain to stay close to the nature of the DTX current-scaling concept [2]. Furthermore, we assume class-B/C-like output matching, fundamental ohmic loading for the (combined) output of the switch bank(s), and short-circuit conditions for their higher harmonics. Like their analog counterparts, the drain voltage in these conditions is purely sinusoidal, with its maximum constrained by the breakdown voltage of the output stage technology. For a predefined TX peak output power level, a certain fundamental switch bank output current is needed, which we normalize as $|\vec{i}_{\mathrm{out,peak}}| = 1$.

Modulated signals like QAM have square-like constellation diagrams; however, resampling and low-pass filtering yield a somewhat circular IQ plane coverage, as shown in Fig. 7(a). When the center frequency is shifted away from the carrier frequency, the frequency offset translates to a constantly increasing or decreasing phase, yielding a continuous rotation of the output constellation and, thus, a circular IQ plane coverage over time. Furthermore, in the widely used orthogonal frequency division multiplexing (OFDM) technique, the inverse FFT is applied in the modulation algorithm, which gives rise to a circular coverage of the IQ plane as well [Fig. 7(b)]. Consequently, to make a fair comparison between the various DTX concepts, we require $|\vec{i}_{\text{out,max}}| \geq 1$ for all phases, thus covering a unit circle in the IQ plane (Fig. 5). Hereby, $|\vec{i}_{\text{out,max}}|$ is the maximum current that can be provided for a certain phase and follows from the previously described output current contours.

B. Power Utilization of the Switch Bank(s)

Using the condition $|\vec{i}_{\text{out,max}}| \geq 1$ for all phases, we can compare the current/power utilization of the different architectures by looking at their minima in $|\vec{i}_{\text{out,max}}|$. Since in a polar architecture, the maximum output current is available at any phase, we compare each architecture to this case. For now, we concentrate on the consequence of the vector summation of the RF fundamental at the output of the segmented output stage, which consists of the vectors $\vec{A}$ and $\vec{B}$.

In architectures using a dedicated switch bank for $\vec{A}$ and $\vec{B}$, the maximum achievable output current along the activation axes is limited to only half of the total current capability, yielding a required total w_g twice as large as the for a polar architecture, assuming equal duty cycles. Using switch bank segment activation interleaving, the achievable output current along the activation axes is equal to the total current capability of the power device, yielding the same required total w_g as the polar architecture (Fig. 4).

When the switch bank segment sharing utilization technique is used, the effective output current depends on the applied upconversion method (SC or multiphase, see Fig. 5). In all these cases, the magnitude of the fundamental RF output current results from the (complex) vector summation $|\vec{A}+\vec{B}|$, whereas the total number of activated segments is given by the summation of the vector magnitudes, $|\vec{A}|+|\vec{B}|$ (Fig. 4). Consequently, we introduce the upconversion current utilization factor, F_{up}, which describes the ratio between this vector summation and summation of their absolute values as

$$F_{\text{up}}(\theta_{\text{BB}}, \phi_{AB}) = \frac{\left|\vec{A}+\vec{B}\right|}{\left|\vec{A}\right|+\left|\vec{B}\right|} = \frac{\sin(\phi_{AB})}{\sin(\phi_{AB}-\theta_{\text{BB}})+\sin(\theta_{\text{BB}})} \tag{2}$$

where ϕ_{AB} is the phase angle between the two vectors, and θ_{BB} is the phase of the baseband input data. The upconversion current utilization factor describes the maximum achievable output current (illustrated in Fig. 5) as a function of the input phase. The current utilization is limited to the value for which F_{up} is minimum, which occurs at $\theta_{\text{BB}} = \phi_{AB}/2$

$$F_{\text{up,min}}(\phi_{AB}) = \cos\left(\frac{\phi_{AB}}{2}\right). \tag{3}$$

Using this upconversion current utilization factor, the required total gate-width for a vector summing architecture with (shared) vector banks with a phase angle ϕ_{AB} between the two vectors, relative to a polar architecture using the same RF duty cycle, is calculated to be

$$\frac{w_{g,\text{tot}}}{w_{g,\text{tot,polar}}} = \frac{1}{F_{\text{up,min}}(\phi_{AB})} = \frac{1}{\cos\left(\frac{\phi_{AB}}{2}\right)}. \tag{4}$$

TABLE III
CURRENT UTILIZATION OF DIFFERENT DTX ARCHITECTURES AND REQUIRED GATE WIDTH TO GENERATE THE SAME RF SIGNAL, RELATIVE TO THE POLAR ARCHITECTURE

Bank usage	Architecture	Output current utilization	Required relative $w_{\text{g,tot}}$
One bank	Polar	1	1
Dedicated banks	Signed Cartesian / multi-phase	$1/2$	2
Switch bank sharing	Signed Cartesian $\phi_{AB} = 90°$	≈ 0.71	≈ 1.41
Switch bank sharing	8-phases $\phi_{AB} = 45°$	≈ 0.92	≈ 1.08
Switch bank sharing	16-phases $\phi_{AB} = 22.5°$	≈ 0.98	≈ 1.02
Segment activation interleaving	Signed Cartesian / multi-phase	1	1

Table III gives an overview of the output current utilization of different DTX architectures. Using dedicated vector banks drastically limits the current utilization, demanding a $2\times$ higher total w_g to achieve the same output current at any phase compared with a polar architecture. Using switch bank sharing, this is reduced to $1.41\times$ for SC operation and even to $1.08\times$ and $1.02\times$ for multiphase operation with eight and 16 phases, respectively. Using multiphase operation with a vector sharing bank gives only a minimal penalty in output current utilization compared with the polar operation. Using vector interleaved operation, this penalty is completely avoided. However, in practical DTX implementations, this yields other disadvantages that might affect the resulting spectral purity and enforces restrictions in the duty cycle ($d \leq \phi_{AB}/360°$).

C. RF Duty Cycle Considerations

Section IV-B only considered the RF fundamental of the currents resulting from the ($\vec{A}$ and $\vec{B}$) activations. However, the current-scaling DTX concept uses a square/rectangular-shaped current waveform, of which the effective duty cycle is set by the time that the switch banks are conducting current. When using "class-B"/"class-C"-like output matching, the duty cycle can be reduced to improve its efficiency [2], [3]. However, when doing so, the fundamental content of the reduced duty

cycle rectangular wave also reduces, demanding a larger $w_{g,\mathrm{tot}}$ to maintain the same fundamental current drive capability.

The magnitude of the fundamental output current, $|\vec{i}_{\mathrm{out}}|$, resulting from the rectangular current waveform, is calculated using the first term of the Fourier series of the applied current waveform. In the vector summation architectures, the applied current waveform consists of two pulses. However, since summation is preserved when the Fourier transform is applied, we first derive the fundamental Fourier term of the single-rectangular waveforms, and then utilize the (vector) summation on resulting RF fundamentals, rather than applying the Fourier series on the composite waveform. We now only need to derive the first Fourier term of a single pulse. The fundamental output current of the rectangular wave relates to its current amplitude, I_{rect}, and the applied RF duty cycle (d) via

$$\left|\vec{i}_{\mathrm{out}}\right| = I_{\mathrm{rect}} \frac{2\sin(\pi d)}{\pi}. \tag{5}$$

For analog class-B, having a rectified half-sine wave current, the fundamental current follows from the maximum current via: $|\vec{i}_{\mathrm{out}}| = I_{\mathrm{half\text{-}sine,max}}/2$, where $I_{\mathrm{half\text{-}sine,max}}$ is the half-sine amplitude. Consequently, for a duty cycle of 50%, $w_{g,\mathrm{tot}}$ of a polar DTX can be $\pi/4$ smaller than that of an analog class-B TX for the same fundamental current. For a duty cycle of 29%, the same $w_{g,\mathrm{tot}}$ as in analog operation can be used in the DTX polar output stage. The required relative $w_{g,\mathrm{tot}}$ of all discussed DTX architectures using different RF duty cycles are summarized in Table IV.

In practical situations, the current waveform has a nonzero rise and fall time, which degrades to some extent the output power for short duty cycles at high operating frequencies (e.g., less than 25% above 5 GHz [6]). When the switch bank activation becomes very short, practical switching speed constraints of the active devices can negatively affect the achievable DTX output powers since the rise and fall times start to dominate at these shorter duty cycles [1].

D. Other (Practical) DTX Performance Considerations Concerning w_g

The total required w_g directly scales the input capacitance (C_{in}) and output capacitance (C_{out}) of the power switch bank. The required (maximum) driver power needed for the switch bank activation of the DTX is directly proportional to the input capacitance. Assuming a digital driver providing sufficient voltage swing to entirely switch the (power) FET devices in the output switch banks between "ON" and "OFF" at a given operating frequency. The required driver power to operate the DTX switch bank is

$$P_{\mathrm{in}} = (\mathrm{ACW}_A + \mathrm{ACW}_B)\left(C_{\mathrm{gs,bank}} + NC_{\mathrm{driver}}\right)V_{\mathrm{gg}}^2 f_0 \tag{6}$$

with V_{gg} representing the driver output voltage swing (being the gate voltage of the power switch bank), $C_{\mathrm{gs,bank}}$ is the gate capacitance of the total bank, C_{driver} is the total driver capacitance per segment [1], and ACW_A and ACW_B the normalized switch bank activation, of which its sum ($\mathrm{ACW}_A + \mathrm{ACW}_B$) is a value between 0 and 1. Following this equation, the required input power scales are inversely proportional to the upconversion current utilization factor. Furthermore, the shorter the required rise and fall times, the lower the required R_{on} of the driver, increasing the driver size and, thus, C_{driver}. Consequently, shorter duty cycles improve the drain efficiency but yield higher drive power, indicating an optimum when considering the overall line-up efficiency [1].

With a larger required $w_{g,\mathrm{tot}}$, the output capacitance C_{out} also scales accordingly. Its value will limit, combined with the provided ohmic load and chosen matching strategy, the achievable RF bandwidth and the maximum (drain) efficiency of the DTX [27].

E. Matching Strategies for the Switch Bank Output

Many DTX implementations in literature use an output match tailored to the maximum achievable fundamental peak output current. This choice provides linear operation for the entire constellation area coverage, e.g., a square-shaped area in an SC architecture, which is suited for single-channel QAM modulation. In these cases, a lower load is applied, yielding an increased output power (factor $(2)^{1/2}$ for SC operation). In this article, we aim to achieve optimal matching over a circle to reach the full voltage swing without clipping for the maximum of the modulated signal at any phase rotation. When a circular constellation coverage is required, the optimum load should be applied for any phase and $|\vec{i}_{\mathrm{out,peak}}| = 1$, yielding

$$R_L = \frac{v_{\mathrm{dd}}}{\left|\vec{i}_{\mathrm{out}}\right|} = \frac{v_{\mathrm{dd}}\pi}{2I_{\mathrm{rect}}\sin(\pi d)} \cdot \frac{1}{F_{\mathrm{up,min}}(\theta_{\mathrm{BB}}, \phi_{AB})} \tag{7}$$

where R_L is the load resistance.

V. Efficiency Considerations

In this section, we compare the efficiency of the various current-scaling DTX architectures. First, we will compute the DTX peak efficiencies by analyzing the impact of the RF duty cycle and the effects of vector summation on the efficiency. Second, we calculate the average efficiency when dealing with complex modulated signals and when applying a DTX in the Doherty efficiency enhancement configuration.

A. Impact of the RF Duty Cycle

The drain efficiency of the output stage(s)/switch bank(s) is defined as

$$\eta_d = \frac{P_{\mathrm{out,RF}}}{P_{\mathrm{DC}}} \tag{8}$$

where $P_{\mathrm{out,RF}}$ is the fundamental RF output power and P_{DC} the final stage(s) power consumption. We use the previous normalization: $|\vec{i}_{\mathrm{out,peak}}| = 1$. Under the condition of a perfect ohmic output load and short-circuited conditions for all harmonics, the output voltage is a perfect sine wave, with normalized peak voltage, $|\vec{v}_{\mathrm{out,peak}}| = 1$. Using (5), this yields

$$\begin{aligned} P_{\mathrm{out,RF}} &= \frac{R_L\left|\vec{i}_{\mathrm{out}}\right|^2}{2} \\ &= R_L I_{\mathrm{rect}}^2 \frac{2\sin^2(\pi d)}{\pi^2}. \end{aligned} \tag{9}$$

The dissipated dc power is given by

$$P_{\rm dc} = v_{\rm dd}\frac{1}{T}\int_{-\frac{d}{2}T}^{\frac{d}{2}T} I_A + I_B dt = v_{\rm dd}\cdot(I_A + I_B)\cdot d \tag{10}$$

where d is the RF duty cycle, T is the period, and I_A and I_B are the amplitudes of the rectangular current waveforms of the A and B vector, respectively. Logically, in a polar architecture, there is only one rectangular current phase instead of A and B.

B. Efficiency of the Polar DTX Architecture

In a polar architecture, following from (5) and (10), the dc power is derived as a function of the duty cycle as

$$P_{\rm dc} = v_{\rm dd}\frac{\pi d}{2\sin(\pi d)}\left|\vec{i}_{\rm out}\right|. \tag{11}$$

Using (9) and (10), the drain efficiency for a current-scaling polar DTX is given by

$$\eta_{d,\rm polar} = \frac{R_L}{v_{\rm dd}}\cdot\frac{\sin(\pi d)}{\pi d}\left|\vec{i}_{\rm out}\right|. \tag{12}$$

Fig. 8 gives the theoretically achievable drain efficiency versus RF output power for a polar DTX using a rectangular current wave for a varying duty cycle compared with analog polar from class-A to deep class-C conditions [2]. The polar DTX provides better output power and efficiency for the same w_g for duty cycle values below 50%. A 25% duty cycle for the switch bank activations is a favorable choice since it can offer higher efficiency (90% ideally) than analog class-B operation (78.5% ideally) while requiring only an 11% larger total w_g (Table IV). The 25% duty cycle can be synthesized digitally using simple divide-by-two circuits. Furthermore, the rising and falling edges of a 25% duty cycle clock coincide with the edges of the I and Q clocks of an SC DTX. By recombining the different phase clocks, 25% duty cycle clocks can easily be synthesized [8]. Similarly, by recombining the multiphase clocks, 12.5% or 37.5% duty cycle can be synthesized.

C. Efficiency of Vector Summation DTX Architectures

When the output waveform is synthesized using two rectangular current pulses, the dc power depends on the absolute sum of the current at the "A" and "B" activation. This sum can be expressed as a function of the fundamental RF output current $\vec{i}_{\rm fund}$, using (2), (5), and (10)

$$P_{\rm dc} = v_{\rm dd}\frac{\pi d}{2\sin(\pi d)}\left(\left|\vec{i}_A\right| + \left|\vec{i}_B\right|\right) = v_{\rm dd}\frac{\pi d}{2\sin(\pi d)}\cdot\frac{\left|\vec{i}_{\rm out}\right|}{F_{\rm up}(\theta_{\rm BB},\phi_{AB})}. \tag{13}$$

This yields a theoretical drain efficiency for multivector architectures of

$$\eta_{d,\rm vector\text{-}sum} = \frac{R_L}{v_{\rm dd}}\cdot\frac{\sin(\pi d)}{\pi d}F_{\rm up}(\theta_{\rm BB},\phi_{AB})\left|\vec{i}_{\rm out}\right|. \tag{14}$$

From (4), the upconversion current utilization yields the largest degradation in efficiency at $\theta_{\rm BB} = \phi_{AB}/2$, yielding $1/(2)^{1/2}$, and 0.92 for SC and eight-phase operation, respectively, compared with a polar system. Fig. 9 shows the efficiency per constellation point of the different architectures for a 25% RF duty cycle.

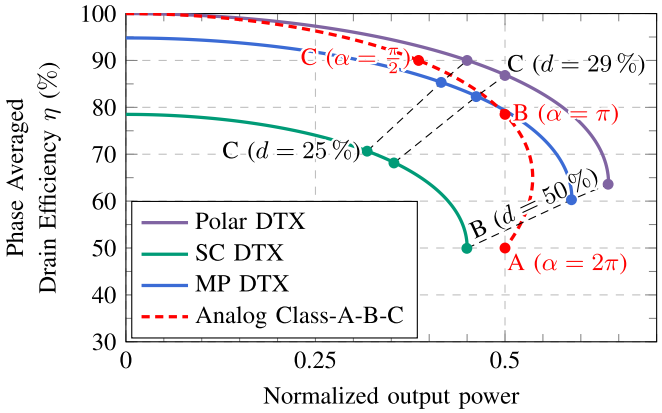

Fig. 8. Theoretical peak drain efficiency averaged over the phase of the modulation ($\theta_{\rm BB}$) versus normalized output power for a DTX switch bank. Efficiencies are shown for an analog polar architecture (red), polar DTX (purple), SC DTX (green), and multiphase (MP) DTX (blue) [2].

1) Average Efficiency Over Phase: Section IV-A concluded that the probability distribution of the modulated TX signal (e.g., OFDM) can be assumed independent over phase for multichannel signals. However, the dc power consumption of the vector summing DTX architectures will vary as a function of the phase angle of the modulated signal. It is, therefore, useful to calculate the average dc power consumption when changing the TX signal phase from vectors A to B by integrating $1/F_{\rm up}(\theta_{\rm BB},\phi_{AB})$ from 0 to ϕ_{AB}

$$\frac{1}{F_{\rm up,av}(\phi_{AB})} = \frac{1}{\phi_{AB}}\int_0^{\phi_{AB}}\frac{1}{F_{\rm up}(\theta_{\rm BB},\phi_{AB})}d\theta_{\rm BB} = \frac{1}{\phi_{AB}}\int_0^{\phi_{AB}}\frac{\sin(\phi_{AB}-\theta_{\rm BB})+\sin(\theta_{\rm BB})}{\sin(\phi_{AB})}d\theta_{\rm BB} = \frac{2}{\phi_{AB}}\tan\left(\frac{\phi_{AB}}{2}\right) \tag{15}$$

where $F_{\rm up}(\theta_{\rm BB},\phi_{AB})$ in (14) can be substituted by $F_{\rm up,av}(\phi_{AB})$ to calculate the average efficiency.

Using (15), we find the increase in average dc power consumption, relative to a polar system, of $(4/\pi) = 1.27$ for SC and $(8/\pi)((2)^{1/2}-1) = 1.055$ for eight-phase operation. The resulting efficiencies averaged over phase and power utilization of the SC and multiphase architecture are given in Fig. 8, which shows that the output power and efficiency are compromised for SC architectures, whereas the multiphase architecture exhibits an output power/efficiency tradeoff which is much closer to the polar architecture. Multiphase operation with a 25% duty cycle seems to be particularly attractive since it offers higher efficiency than analog class-B operation, with only a limited output power penalty. Furthermore, its phase-coherent operation avoids the need for a (wideband) CORDIC and continuous phase modulator.

In Table IV, an overview is given of the required $w_{g,\rm tot}$ relative to an analog polar system, the maximum efficiency, the peak efficiency at $\theta_{\rm BB} = \phi_{AB}/2$, and the peak efficiency

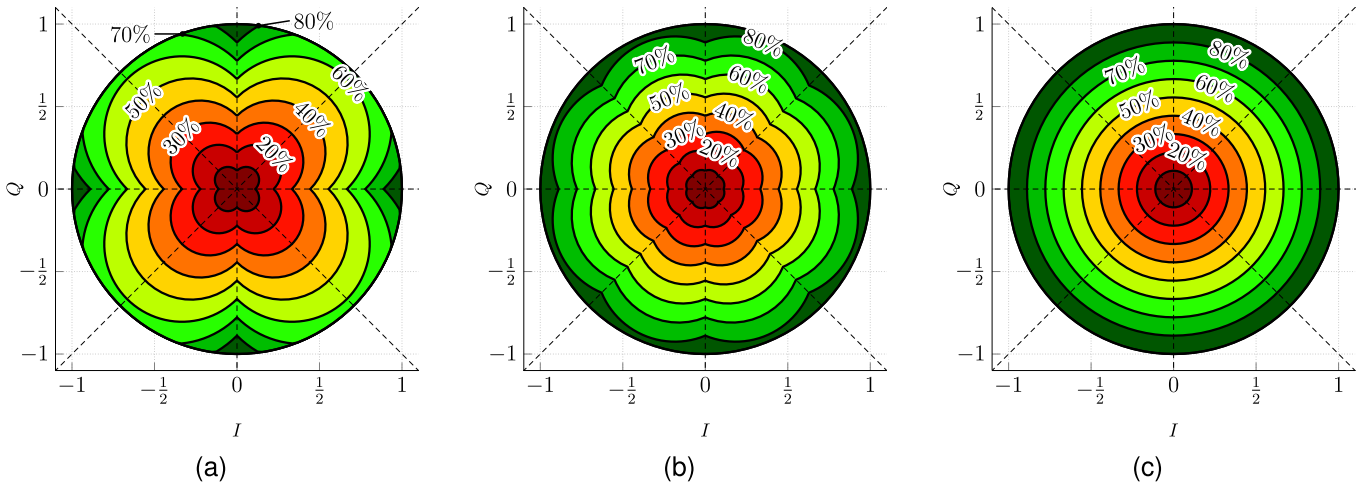

Fig. 9. Contour plots showing the theoretical drain efficiency for (a) SC, (b) multiphase, and (c) polar operation over the IQ plane, given a 25% RF duty cycle, illustrating the phase dependency of the efficiency for SC operation, and a more "polar-like" efficiency profile for eight-phase operation.

TABLE IV
CURRENT-SCALING DTX ARCHITECTURES WITH THEIR $w_{g,\mathrm{TOT}}$ AND EFFICIENCY PERFORMANCES RELATIVE TO AN ANALOG POLAR SYSTEM

	Duty Cycle	Required relative $w_{g,\mathrm{tot}}$	$\eta_{\mathrm{d,pk}}$ @θ_{BB} = 0	$\eta_{\mathrm{d,pk}}$ @θ_{BB} = $\phi_{\mathrm{AB}}/2$	$\eta_{\mathrm{d,pk,av}}$
Analog Polar Class-B		1	78.5%	–	–
Polar DTX	50%	0.79	63.7%	–	–
	28.8%	1	86.7%	–	–
	25%	1.11	90.0%	–	–
	12.5%	2.05	97.5%	–	–
Signed Cartesian dedicated I&Q banks	50%	1.57	63.7%	45.0%	50.0%
	28.8%	2	86.7%	61.3%	68.4%
	25%	2.22	90.0%	63.7%	70.7%
	12.5%	4.10	97.5%	68.9%	76.5%
Bank sharing Signed Cartesian	50%	1.11	63.7%	45.0%	50.0%
	28.8%	1.41	86.7%	61.3%	68.1%
	25%	1.57	90.0%	63.7%	70.7%
	12.5%	2.90	97.5%	68.9%	76.5%
Bank sharing 8-phase	50%	0.85	63.7%	58.8%	60.4%
	28.8%	1.08	86.7%	80.1%	82.2%
	25%	1.20	90.0%	83.2%	85.4%
	12.5%	2.22	97.4%	90.0%	92.4%

averaged over the phase for the discussed TX architectures at various duty cycles.

D. DTX Doherty Operation

Due to their (close to) linear operation, the efficiency of the current/g_m-scaling DTX architectures will roll-off linearly with RF output current (quadratic with output power). To enhance DTX (deep) power back-off (PBO) efficiency when dealing with complex modulated signals (like OFDM) having a large PAPR, Doherty efficiency enhancement techniques are a favored approach. Namely, current-scaling DTX units are perfect replacements for the analog branches conventionally used in these Doherty designs. They can use similar or even identical output power combiners and output-matching arrangements. More importantly, in contrast to the analog Doherty, the branch driving profiles for the main and peaking branches in a DTX can be obtained almost effortlessly in the digital domain, rather than manipulating their bias points in combination with a complicated analog input splitter design. Furthermore, their digital input drive is frequency-agile in nature. This improved branch control allows achieving close to perfect transfer functions and Doherty efficiency versus power back-off even for higher order N-way Doherty combiners over larger RF bandwidths [8], [28], [29].

Furthermore, all Doherty branches in the DTX, including the main branch, can be operated in their highest efficiency mode since the transfer function can be set independently of the duty cycle. Finally, all quiescent currents can be eliminated in DTX implementations, allowing significant power savings in low-traffic scenarios [30].

Next, we will evaluate the theoretically achievable average efficiencies of N-way DTX-based Doherty configurations. DTX-based Doherty configurations can be adapted for any kind of power combining networks with free-to-choose switch bank sizes and activation schemes. However, to limit the number of configurations considered in this work, we only focus on N-way Doherty combiners using a linear (nonsaturating) current profile [31] having equal switch bank sizes for the implementation of their branches. Using equal-sized switch banks relaxes the DTX design logistics and time. Consequently, the following DTX configurations are studied: single-line-up, symmetrical Doherty (1:1) [32], the three-way Doherty (1:1:1) [33], and the four-way Doherty (1:1:1:1) [34]. Moreover, the supply voltages used for all branches are considered to be identical.

1) Power Back-Off Efficiency Profiles: To find the power back-off efficiency profiles, we calculate the dc power as a function of the fundamental RF output current. When using vector summation operation, such as SC or multiphase, in a Doherty DTX, each branch needs to operate with the same vector ratio to ensure proper Doherty load modulation for the RF outputs of the switch banks at any phase. Having an equal RF duty cycle and the same v_{dd} for each branch, using (2), (11), we find

$$P_{\mathrm{dc}} = v_{\mathrm{dd}} \frac{\pi d}{2\sin(\pi d)} \cdot \frac{\left|\vec{i}_m\right| + \sum_{n=1}^{N-1} \left|\vec{i}_{p,n}\right|}{F_{\mathrm{up}}(\theta_{\mathrm{BB}}, \phi_{AB})} \tag{16}$$

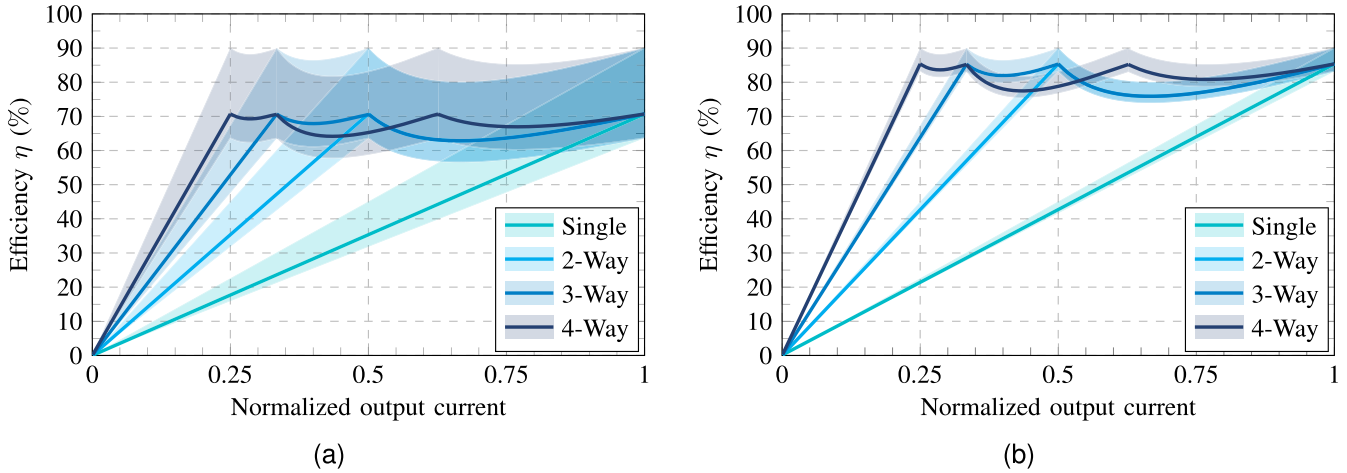

Fig. 10. Efficiency profile of symmetric one-way to four-way Doherty architectures for (a) SC and (b) multiphase operation. The plotted lines represent the phase averaged efficiency, and the shaded area shows the phase dependency of each operation.

where $|\vec{i}_m|$ and $|\vec{i}_{p,n}|$ are the fundamental currents in the main and the nth peaking branch, respectively. For an N-way Doherty, the high-efficiency power back-off points follow from (30) and (31), derived in Appendix B. The fundamental drain currents in each branch are given in (32).

Although the efficiency peaks of this type of Doherty with equal bank sizes appear at different PBO points compared with those of the classical symmetric Doherty configurations, it can be shown that for a given set of power back-off points, the related efficiency versus output current/power function, is independent of the actual Doherty implementation used, under the condition of a lossless power combination and ideal current source behavior of the active devices. This facilitates the results of this analysis to be used in a broader context.

Using (16), the Doherty efficiency is defined as

$$\eta_{d,\mathrm{Doh}}\left(|\vec{i}_{\mathrm{out}}|\right) = \frac{R_L|\vec{i}_{\mathrm{out}}|}{v_{\mathrm{dd}}} \cdot \frac{\sin(\pi d)}{\pi d} F_{\mathrm{up}}(\theta_{\mathrm{BB}}, \phi_{AB}) D_{\mathrm{eff}}\left(|\vec{i}_{\mathrm{out}}|\right) \tag{17}$$

where $D_{\mathrm{eff}}(|\vec{i}_{\mathrm{out}}|)$ is defined as the Doherty efficiency factor for a given fundamental output current level, which can be used to describe the efficiency versus power back-off, normalized to 100% for its peak efficiency

$$D_{\mathrm{eff}}\left(|\vec{i}_{\mathrm{out}}|\right) = \frac{|\vec{i}_{\mathrm{out}}|}{|\vec{i}_m| + \sum_{n=1}^{N-1} |\vec{i}_{p,n}|}. \tag{18}$$

The efficiency profile of the considered Doherty configurations versus the normalized RF output current for both SC and eight-phase operation are shown in Fig. 10. The solid line in the plot represents the efficiency averaged over phase, and the shaded area represents the range over which the instantaneous efficiency can vary as a function of its modulation phase (θ_{BB}).

2) Average Efficiency and Probability Density: Using the efficiency profiles derived in Section V-D.1, the overall average efficiency for a modulated signal with a given PAPR can be derived. For this purpose, the 2-D probability density must be considered. As shown in Fig. 7(b), the coverage of an OFDM signal is constant over phase, and thus, the amplitude can be considered independent of the phase in this calculation. Consequently, the average efficiency can be calculated by evaluating the average upconversion utilization factor and the average dc current in power back-off. Assuming that an OFDM signal has a bivariate Gaussian distribution over the constellation, with equal variance for the in-phase and quadrature-phase, the probability density of the vector amplitude of such a distribution is described by the Rayleigh distribution [32], [35], as shown in Fig. 7(c)

$$f_{\mathrm{Ray}}\left(|\vec{i}_{\mathrm{out}}|,\, \sigma^2\right) = \frac{|\vec{i}_{\mathrm{out}}|}{\sigma^2} e^{-\frac{|\vec{i}_{\mathrm{out}}|^2}{2\sigma^2}} \tag{19}$$

where $|\vec{i}_{\mathrm{out}}|$ is normalized to: $0 \leqslant |\vec{i}_{\mathrm{out}}| \leqslant 1$ and σ^2 represents the variance of I and Q. The average output power of such a distribution, based on the integral from 0 to ∞, is $2\sigma^2$. The switch bank output is only defined for the range $0 \leqslant |\vec{i}_{\mathrm{out}}| \leqslant 1$. Consequently, the average output power is calculated using this interval, yielding an average output power of

$$\begin{aligned} P_{\mathrm{out,RF,av}} &= R_L \int_0^1 f_{\mathrm{Ray}}\left(|\vec{i}_{\mathrm{out}}|, \sigma^2\right) |\vec{i}_{\mathrm{out}}|^2 d|\vec{i}_{\mathrm{out}}| \\ &= R_L \left(2\sigma^2 \left(1 - e^{-\frac{1}{2\sigma^2}}\right) - e^{-\frac{1}{2\sigma^2}}\right). \end{aligned} \tag{20}$$

For a given PAPR, we can make the approximation: PAPR $\approx (1/2\sigma^2)$ (for PAPR = 7 dB, the deviation is 0.25 dB).

The same integral and (16) are used to calculate the average dc power

$$\begin{aligned} P_{\mathrm{dc,av}} = v_{\mathrm{dd}} \frac{d\pi}{2\sin(\pi d)} \cdot \frac{1}{F_{\mathrm{up,av}}(\phi_{AB})} \\ \cdots \int_0^1 f_{\mathrm{Ray}}\left(|\vec{i}_{\mathrm{out}}|, \sigma^2\right) \left(|\vec{i}_m| + \sum_{n=1}^{N-1} |\vec{i}_{p,n}|\right) d|\vec{i}_{\mathrm{out}}|. \end{aligned} \tag{21}$$

The average efficiency, $\eta_{\mathrm{d,av}}(\sigma^2)$ is defined as

$$\begin{aligned} \eta_{d,\mathrm{av}}\left(\sigma^2\right) = \frac{R_L}{v_{\mathrm{dd}}} \cdot \frac{\sin(\pi d)}{d\pi} \cdot F_{\mathrm{up,av}}(\phi_{AB}) \\ \cdots \frac{\int_0^1 f_{\mathrm{Ray}}\left(|\vec{i}_{\mathrm{out}}|\right) |\vec{i}_{\mathrm{out}}|^2 d|\vec{i}_{\mathrm{out}}|}{\int_0^1 f_{\mathrm{Ray}}\left(|\vec{i}_{\mathrm{out}}|\right) \left(|\vec{i}_m| + \sum_{n=1}^{N-1} |\vec{i}_{p,n}|\right) d|\vec{i}_{\mathrm{out}}|} \end{aligned} \tag{22}$$

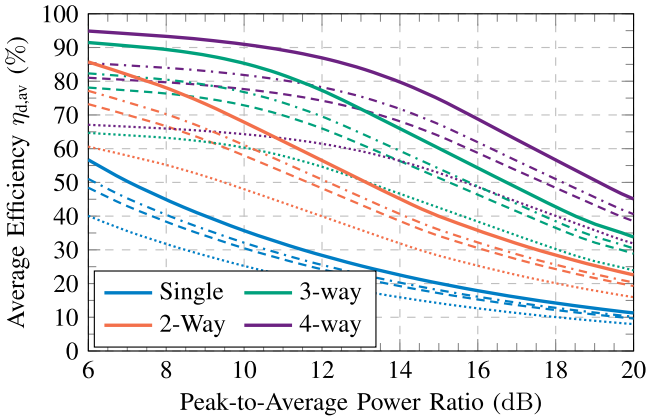

Fig. 11. Plot showing the average drain efficiency as a function of the PAPR of a single line-up and a symmetric two-way, three-way, and four-way Doherty. The solid line shows the Doherty efficiency factor, $D_{\text{eff,av}}$ (efficiency normalized to $\eta_{d,\text{peak}} = 100\%$). Additionally, the dashed-dotted lines, dashed lines, and dotted lines represent the theoretical average efficiency for a polar DTX, multiphase DTX, and SC DTX, respectively, using a 25% duty cycle.

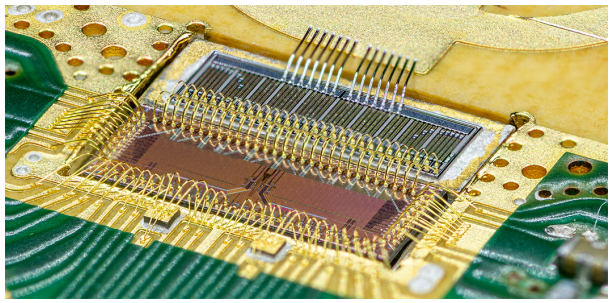

Fig. 12. Picture of the CMOS-LDMOS power DTX [2].

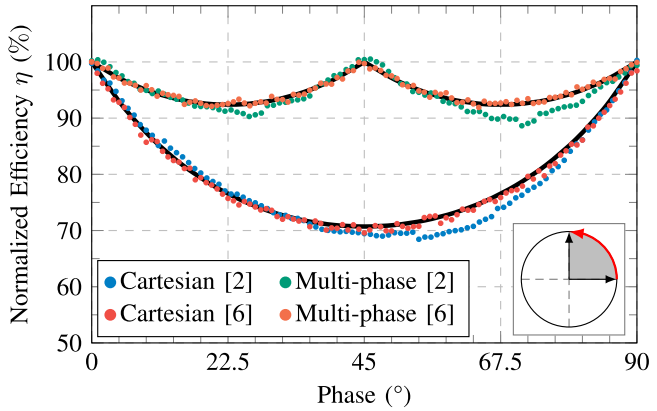

Fig. 13. Plot showing the normalized efficiency as a function of phase for SC and multiphase operation, verifying the upconversion current utilization factor (F_{up}). The theoretical value is plotted, as well as (normalized) measured data from the DTX implementations presented in [2] and [6].

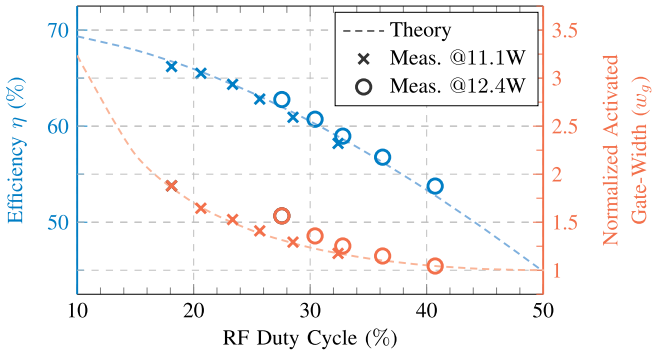

Fig. 14. Normalized efficiency and required activated w_g for a constant RF output power as a function of the duty cycle. With the applied duty cycle calibration, the measurements verify the predicted trends.

which is plotted in Fig. 11, using a duty cycle of 25% for different variants of DTX architectures.

VI. Verifications in Measurement

To verify some of the theoretical findings and values derived in this article, additional measurements are performed on two already available DTX configurations, presented in [2] and [6], that excel in terms of output power, configurability, or Doherty order. Since all previously derived theory assumes lossless operation, some normalization is needed to allow a meaningful comparison and confirmation of the predicted trends.

A. Vector Summation Efficiency

The modulation-phase–efficiency relation for SC and multiphase operation is verified by performing additional measurements on the CMOS-LDMOS power DTX presented in [2] and [29] (Fig. 12) and the CMOS only DTX presented in [6]. The LDMOS output stage has two segmented banks that can be independently controlled and, thus, used as designated *A* and *B* banks in SC or multiphase operation. Fig. 13 shows the drain efficiency, measured for different phase inputs while ensuring the output power was equal for all different phases. The measured peak efficiency (54% at ∼50% duty cycle with only one phase activated) has been normalized to allow comparison with the theory.

B. Duty Cycle Reduction

Also, the anticipated relation between the duty cycle and drain efficiency has been verified by measurements. While the effective LDMOS duty cycle could not be measured directly, the duty cycle can be derived using the duty-cycle-dependent dc value of the additional trigger pin at the output of the CMOS driver. The duty cycle of the CMOS driver is higher than that of the LDMOS drain current, which is caused by its nonzero threshold voltage (v_t) and nonlinear $v_{\text{gs}} - i_{\text{ds}}$ relation. In the measurement, the duty cycle of the DTX CMOS driver is varied, while its ACW is continuously adjusted to keep the RF output power constant. Using the ACW increase at lower duty cycles, needed to keep the RF output power constant, the effective duty cycle of the LDMOS drain current can be estimated using similar dependencies, as shown in Fig. 8. Fig. 14 shows the expected theoretical and experimental results for two RF output power levels versus duty cycle, confirming the predicted trends.

VII. Comparison With Literature

To verify our key conclusions for a current-scaling DTX with other experimental data, a comprehensive literature review has been performed. Alternative DTX architectures are included to put the current-scaling DTX concept in a better perspective. These include the following.

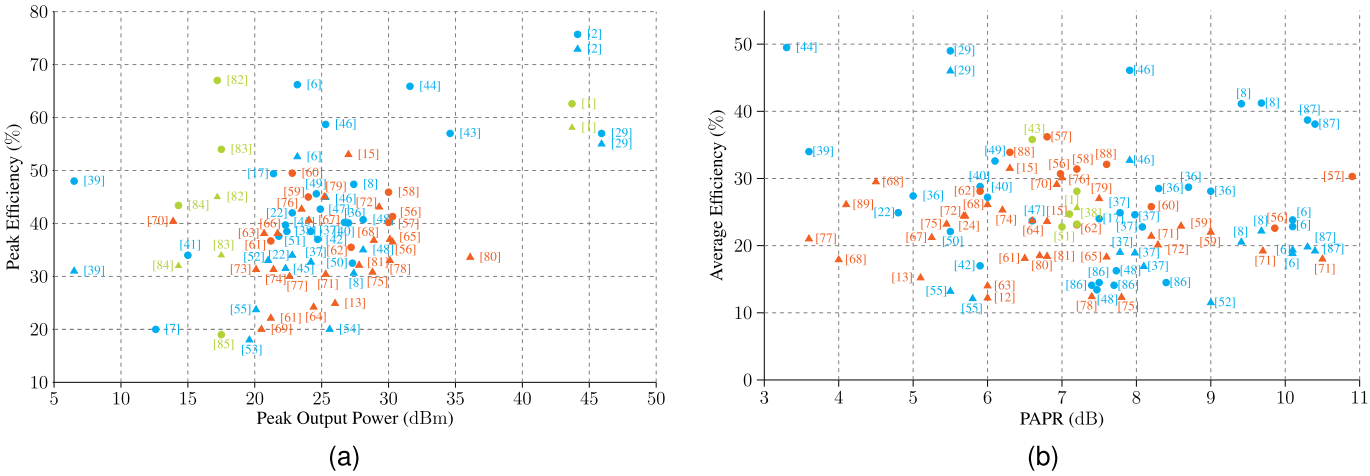

Fig. 15. Literature comparison of proposed DTXs over the last decade (a) in terms of peak efficiency versus peak output power and (b) in terms of average efficiency versus PAPR. The circles represent the drain efficiency, and the triangles represent the DTX system efficiency. The blue-colored shapes represent current-scaling architectures, the red-colored shapes represent switched capacitor architectures, and the green-colored shapes represent architectures that use switching to scale their on-resistance.

1) Switched capacitor DTX approaches, that rely on digital switch banks with class-D output stages to control the amount of (series) output capacitance that is actively switched between ground and supply, and as such, provides a means to control its RF output power via a resonant output match [79].
2) Switched resistor-based DTXs, that use switch banks composed out of small output transistors to toggle at the transmit frequency between off-state and R_{on}, of which the later depends on the number of activated output stage devices in the switch bank. Using this approach, its RF output power can be controlled even when performing a class-E-like operation [90].
3) Hybrid DTX architectures, which typically rely on a combination of current/capacitor/resistor and/or voltage scaling. Nonscaling DTXs, like (classical) out-phasing configuration, are not included in this comparison [38].

First, the DTX architectures reported in the literature are compared for their peak RF output power and efficiency [Fig. 15(a)]. Both peak drain efficiency (dot) and system efficiency (triangle) are provided when available. Most reported single-chip CMOS DTX implementations are found in the $+20$ and $+30-$ dBm range. This is caused by the limited breakdown of the advanced CMOS technologies used in the output stages, and thus, restricted output voltage swing(s). Targeting higher RF output powers using these high-speed CMOS technologies demands (very) low load impedance(s), or extensive power combiner network(s), which both make the circuitry very sensitive to output losses. Here, the use of an external PCB matching network can help to lower these losses [6], [83]. Current-scaling (blue symbols) and resistor-scaling (green symbols) DTX implementations tend to be more forgiving for losses in their output stages/networks than switched capacitor solutions (red symbols). As such, current-scaling and resistor-scaling approaches can reach peak efficiencies over 60%. Since resistor scaling/class-E-like approaches (green symbols) typically use a higher voltage swing for a given output power level, they seem to be more power restricted when using the same process, or comparable technology, for their switch bank implementation [21], [91].

Dual-chip DTX solutions, e.g., a CMOS DTX driver combined with a (gate) segmented output stage in high-voltage technology, can provide much higher RF output powers, e.g., over 40 dBm. A v_t down-shifted segmented LDMOS technology with a breakdown voltage of 65 V was used for the implementation of [1], [2], and [29]. In principle, a similar approach can also be used with a GaN power device. However, up to date, this has not been reported since achieving a sufficiently low v_t and a fine segmentation is less straightforward in GaN technology. In view of this, note that [43] uses a current-scaling CMOS driver followed by a single-input common-gate GaN device that has no segmentation, so [43] is still relying on an analog PA output stage; however, it is capable of delivering $+34.6$ dBm.

The average DTX drain (circles) and system efficiency (triangles) versus PAPR are shown in Fig. 15(b). It indicates that current-scaling DTXs also report the highest average efficiencies [6], [8], [29], [44], [87].

Two-way Doherty efficiency enhancement yields the highest average efficiency for DTXs [6], [46] at moderate PAPRs ($4.5-8$ dB). For higher PAPRs, we find the best average efficiency performance with a four-way Doherty DTX configuration. When considering the switched-capacitor PA (SCPA) architectures, [57] stands out in average drain efficiency for a very high PAPR of 10.9 dB. This result is achieved using a combination of dual-supply class-G, Doherty load modulation, and time interleaving to create eight high-efficiency power back-off points.

VIII. Conclusion

This article benchmarks the Cartesian, multiphase, and polar current-scaling DTX architectures with their switch bank implementation (separate IQ banks, IQ bank sharing, and interleaving) against the performance of ideal classical analog class-B operation. To do so, the IQ baseband-to-RF-signal upconversion of the various DTX architectures is

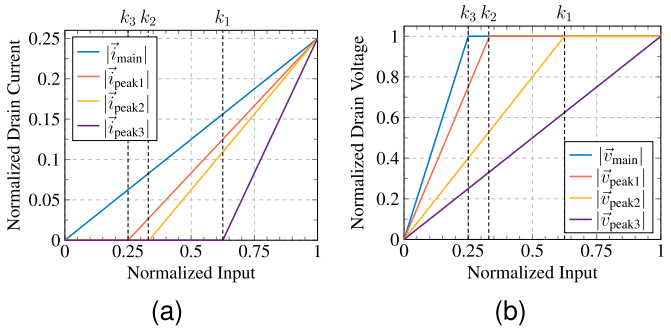

Fig. 16. (a) Drain current and (b) voltage profile for a four-way Doherty architecture using a linear current profile.

expressed through the upconversion current utilization factor F_{up}. Also, the coverage of the current constellation plane for the different DTX architectures is evaluated. Using a realistic OFDM multichannel modulation scenario, the modulation phase dependency of Cartesian and multiphase DTX architectures can be eliminated as a variable, allowing a straightforward normalization of their output current capability. Next, the impact of the duty cycle for the current pulses/vectors is taken into account, enabling a straightforward comparison with the ideal analog class-B operation in terms of the required total gate width ($w_{g,\text{tot}}$) and peak drain efficiency. Performing these steps, it is found that the use of low-duty-cycle current pulses provides a better power/efficiency tradeoff for DTX than its analog counterpart. Meanwhile, it does not show the gain expansion as is present in analog class-C. Although polar DTX operation provides by far the best efficiency and output power, Cartesian and multiphase DTX operation strongly benefit from their phase coherent upconversion, allowing straightforward retiming of their unit cells in the output stage and, as such, avoiding the bandwidth expansion of polar operation, while eliminating the need for a CORDIC or phase modulator. This makes Cartesian and multiphase operations better suited for handling wideband modulated signals.

Unfortunately, Cartesian DTX efficiency still suffers from the 90° phase difference between its (summing) current vectors. For this reason, the eight-phase operation with a 25% duty cycle seems to be an interesting candidate in terms of overall DTX performance. Namely, it approximates the efficiency of a polar DTX, ($\eta_{\text{pk,av,multiphase}} = 85\%$) and requires only a relative $w_{g,\text{tot}}$ of 1.2 in a bank sharing architecture, whereas being compatible with wideband modulation signals [6]. Meanwhile, the output match in all these considered architectures only requires shorts for higher harmonics, which are easy to implement and also compatible with wideband operation. Since current-scaling-based DTX operation provides superior control in terms of current amplitude and phase, it is perfectly suited to be used in N-way Doherty configurations that facilitate high average efficiency when handling modulation signals with high PAPR. Consequently, the theoretical achievable average efficiencies of a single DTX and two-way, three-way, and four-way Doherty DTX have been computed for polar, multiphase, and Cartesian operations assuming a 25% duty cycle for their current pulses. The theoretical trends found in terms of efficiency/output power versus duty cycle have been verified in measurements for the polar, Cartesian, and multiphase operations. Also, an extensive comparison with DTX results in the literature has been given, showing the recent DTX progress in peak efficiency versus output power and average efficiency versus PAPR.

Appendix A
Upconversion Current Utilization Factor

In this appendix, a closed-form equation is derived for the upconversion current utilization as a function of the phase angle between the two applied vectors and the phase of the input signal. The upconversion current utilization factor is defined as

$$F_{\text{up}}(\theta_{\text{BB}}, \phi_{AB}) = \frac{|I + \text{jQ}|}{A + B}. \tag{23}$$

In which $|I + \text{jQ}|$ represents the magnitude of the wanted fundamental current in the constellation plane, and A and B are the two current vectors used for its construction. To derive the closed-form equation for $F_{\text{up}}(\theta_{\text{BB}}, \phi_{AB})$, we first calculate the values of A and B as a function of the input amplitude (ρ_{BB}) and phase (θ_{BB}). For this purpose, the input IQ value is rewritten to polar notation

$$\begin{aligned} I &= \Re\left(\rho_{\text{BB}} e^{j\theta_{\text{BB}}}\right) = \rho_{\text{BB}} \cos(\theta_{\text{BB}}) \\ Q &= \Im\left(\rho_{\text{BB}} e^{j\theta_{\text{BB}}}\right) = \rho_{\text{BB}} \sin(\theta_{\text{BB}}). \end{aligned} \tag{24}$$

In this analysis, we only consider the first segment ($0 \leq \theta_{\text{BB}} \leq \phi_{AB}$), utilizing the symmetries present in Figs. 5 and 9. In this segment, only the B vector contributes to the quadrature (imaginary) part of the input IQ value, yielding

$$Q = \Im\left(B e^{j\phi_{AB}}\right) = B \sin(\phi_{AB}) \tag{25}$$

and thus,

$$B = \rho_{\text{BB}} \frac{\sin(\theta_{\text{BB}})}{\sin(\phi_{AB})}. \tag{26}$$

Furthermore, in this first segment, the A vector is in-phase and only contains a real value. The amplitude of the A vector is calculated by subtracting the real part of the B vector from the real (in-phase) part of the baseband input

$$A = \Re\left(\rho_{\text{BB}} e^{j\theta_{\text{BB}}}\right) - \Re\left(B e^{j\phi_{AB}}\right) \tag{27}$$

and thus,

$$A = \rho_{\text{BB}} \left(\cos(\theta_{\text{BB}}) - \frac{\sin(\theta_{\text{BB}})}{\sin(\phi_{AB})} \cos(\phi_{AB}) \right). \tag{28}$$

Using the equations earlier, the upconversion factor can now be written as

$$\begin{aligned} F_{\text{up}}(\theta_{\text{BB}}, \phi_{AB}) &= \frac{\rho_{\text{BB}}}{A + B} \\ &= \frac{\sin(\phi_{AB})}{\sin(\phi_{AB} - \theta_{\text{BB}}) + \sin(\theta_{\text{BB}})}. \end{aligned} \tag{29}$$

APPENDIX B
DOHERTY DC POWER

The analysis provided is based on the current and voltage profiles, of which a four-way example is shown in Fig. 16 [31]. This configuration uses linear current relations for its branches, in contrast to the classical N-way Doherty. The linear relations avoid discontinuities, yielding higher linearity in practical designs [8], [92].

The maximum branch currents ($|\vec{i}_{m,\max}|$, $|\vec{i}_{p1,\max}|$, ...,) are directly proportional their relative size, in our case equal to $|\vec{i}_{\text{out,max}}|/4$ for each branch. As shown in Fig. 16, the main branch's current increases linear from 0 to $|\vec{i}_{m,\max}|$ over the full input range (ρ_{BB}), whereas the other branch currents are activated successively at higher drive levels, indicated by k_3, k_2, and k_1. The already activated branches reach their maximum swing and, thus, efficiency at these points. Consequently, k_1, k_2, and k_3 are the high-efficiency PBO points.

To calculate the values of k_{1-3}, the output power is expressed as the sum of the powers provided by each branch, assuming a lossless Doherty power combiner is given as

$$|\vec{i}_{\text{out}}||\vec{v}_{\text{out}}| = |\vec{i}_m||\vec{v}_m| + \sum_{m=1}^{N-1} |\vec{i}_{p,m}||\vec{v}_{p,m}|. \tag{30}$$

Using the linear current profiles given in Fig. 16, the following branch current relations are derived

$$\begin{aligned} |\vec{i}_m| &= \rho_{\text{BB}}|\vec{i}_{m,\max}| \\ |\vec{i}_{p,m}| &= \begin{cases} \dfrac{\rho_{\text{BB}} - k_{N-m}}{1-k_{N-m}}|\vec{i}_{\text{p,m,,max,}}|, & \text{for } k_{N-m} < \rho_{\text{BB}} \leqslant 1 \\ 0, & \text{elsewhere} \end{cases} \end{aligned} \tag{31}$$

for an N-way Doherty configuration with $m = \{1, 2, \ldots, N-1\}$. The input values k_3, k_2, and k_1 are found at the points, where the drain voltage at each active branch reaches its maximum value, $|\vec{v}_{\text{out,max}}| = 1$ and the currents in the nonactivated (peaking) branches are zero. Furthermore, we assume that $|\vec{i}_{\text{out}}|$ relates linearly to ρ_{BB} and use $|\vec{i}_{\text{out}}||\vec{v}_{\text{out}}| = |\vec{i}_{\text{out}}|^2 R_l$, whereas $R_l = 1$ and $v_{\text{dd}} = 1$. As an example, using these conditions and substituting (31) into (30) yield the following high-efficiency power back-off points for the four-way symmetric Doherty:

$$k_3 = \frac{1}{4}, \quad k_2 = \frac{1}{3}, \quad k_1 = \frac{3}{8}.$$

The drain currents as a function of the input amplitude ρ_{BB} and the high-efficiency PBO points are hereby

$$\begin{aligned} |\vec{i}_m| &= k_3\rho_{\text{BB}} \\ |\vec{i}_{\text{p,1}}| &= \begin{cases} k_2(\rho_{\text{BB}} - k_3), & \text{for } k_3 < |\vec{i}_{\text{out}}| \leqslant 1 \\ 0, & \text{elsewhere} \end{cases} \\ |\vec{i}_{p,2}| &= \begin{cases} (k_1 - k_3)(\rho_{\text{BB}} - k_2), & \text{for } k_2 < |\vec{i}_{\text{out}}| \leqslant 1 \\ 0, & \text{elsewhere} \end{cases} \\ |\vec{i}_{\text{p,3}}| &= \begin{cases} (1 - k_2)(\rho_{\text{BB}} - k_1), & \text{for } k_1 < |\vec{i}_{\text{out}}| \leqslant 1 \\ 0, & \text{elsewhere.} \end{cases} \end{aligned} \tag{32}$$

Similarly, this method can be used to analyze other N-way (e.g., two-way, three-way, and/or asymmetric) Doherty configurations.

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