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A Digital PLL-Based Phase Modulator With Non-Uniform Clock Compensation and Non-linearity Predistortion

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***Abstract*— In this article, we present a low-power digital phase-locked loop (PLL)-based phase modulator targeting low error vector magnitude (EVM). We introduce a new non-uniform clock compensation (NUCC) scheme to tackle an EVM degradation resulting from the beneficial use of a time-varying sampling clock that is re-timed to the phase-modulated carrier. We also employ a phase-domain digital predistortion (DPD) to combat the intrinsic non-linearity of an LC-type digitally controlled oscillator (DCO), thus avoiding the complications of frequency-dependent calibrations. The prototype, implemented in 40-nm CMOS, modulates the carrier in the range of 2.7–3.9 GHz from a 40-MHz reference. The measured EVM is −47 dB for a 60-Mb/s 64-PSK modulation under the case that the phase-modulated output is frequency-divided by $K = 8$, i.e., when the DCO exhibits the most significant non-linearity due to the large fractional FM bandwidth. When $K = 8$ or 4, the measured EVM remains below −43 dB across the carrier-frequency tuning range and without re-calibrating the DCO non-linearity.**

***Index Terms*— Digital polar transmitter (TX), fractional-*N* phase-locked loop (PLL), *LC*-tank non-linearity, non-uniform clock compensation (NUCC), phase modulator, phase-domain digital predistortion (DPD), PLL-based modulator, polar modulation, two-point modulation.**

I. Introduction

LIFETIME of a battery-operated radio for the Internet-of-Things (IoT) applications is severely limited by the power consumption of its wireless transmitter (TX). Therefore, its energy-efficient realizations are a subject of great interest, and this favors a digital polar TX architecture [1], [2], [3], [4]. The polar TX utilizes a phase modulation (PM) path in parallel with an amplitude modulation (AM) path to compose a complex-valued RF signal, as shown in Fig. 1. Low-power implementations of the PM path typically perform a direct or a two-point frequency/phase-modulation of an RF oscillator, e.g., a digitally controlled oscillator (DCO) in a phase-locked loop (PLL) [4], [5], [6], [7]. This solution renders unnecessary such power-hungry PM blocks as delaylines [3], [8], [9] and IQ interpolators [2], [10], thus maximizing the system energy efficiency, especially at lower output power.

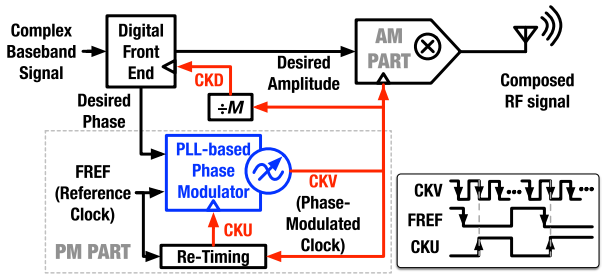


Fig. 1. Block diagram of a digital polar TX. The DCO-update clock, CKU, is obtained by re-sampling and inverting the reference clock, FREF, by the falling edges of the DCO variable clock, CKV.

On the other hand, IoT standards such as Wi-Fi HaLow are currently evolving toward high-order modulation schemes, such as 256-QAM, which requires an error vector magnitude (EVM) below −32 dB for the entire TX. From a system perspective, the AM path is usually allowed to corrupt a greater EVM portion since it handles a large signal amplitude and is more prone to nonlinearity and EVM degradation. As a result, the PM path is allocated a much lower portion of the EVM budget (e.g., ≤−40 dB).

Although the recently published PLL-based phase modulators have reported EVM below −40 dB [11], [12], maintaining such performance is challenging under some practical system-level constraints. One is that the ever widening signal bandwidth (BW_{sig}) in advanced communication standards tends to become a large fraction of the RF channel frequency (f_{RF}), i.e., BW_{sig}/f_{RF}, ultimately aggravating the $1/\sqrt{LC}$-induced nonlinearity of the DCO. For example, WiFi HaLow may use a signal bandwidth up to 16 MHz around 800 MHz, resulting in $BW_{sig}/f_{RF} \approx 2\%$. If this signal is transmitted by a polar TX, the DCO on the PM path needs to update at a frequency much higher than BW_{sig} to suppress the replicas and spectral regrowth due to the FM expansion [5]; e.g., the update frequencies in [7], [13], and [14] are over 16× of BW_{sig}. The DCO's FM bandwidth (BW_{FM}) is usually a large fraction of

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the update frequency, even equal to it to guarantee the PM range of $[-\pi, \pi]$ [11], [15]. Consequently, BW_{FM} can be many times wider than BW_{sig}, covering a portion of f_{RF} much higher than 2%. Across such a wide FM range, an LC-tank DCO will exhibit significant nonlinearity due to its $1/\sqrt{LC}$ law conversion [16].

So far, the DCO nonlinearity has been tackled by predistorting the oscillator tuning word (OTW). Noting that the predistortion setting is highly frequency-sensitive, [17], [18] calibrate the settings in the foreground at multiple frequency points. This not only costs extra power but may also fail to maintain the optimum EVM since a foreground calibration cannot track the relevant parameters under temperature and supply drift. Although the background calibration in [7] and [12] addresses the drawbacks of the foreground calibration, the convergence times are long, e.g., up to 100 ms in [7]. Considering that the background calibration there involves not only the nonlinearity but also the DCO gain (K_{DCO}) [12], which is cubically related to the channel frequency [16], the calibration results can easily turn invalid after hopping to some reasonably faraway channel. Therefore, re-calibration may be frequently needed during channel hopping, wasting considerable time and energy.

Another challenging system-level constraint is that the phase modulator should operate at a non-uniform clock aligned with the channel-dependent and phase-modulated RF clock [14], [19], [20], [21], [22], such as the variable clock (CKV) in Fig. 1. As shown, the digital polar TX uses multiple clock domains (i.e., CKU, CKV, CKD) to allow sufficiently high clock sampling rates of each block while being aware of their effects on power consumption. Aligning all the clocks with a common reference, i.e., CKV, helps to avoid data misalignment and glitches during cross-clock-domain data synchronization. This prevents the EVM and output spectrum from getting degraded by glitches of AM data [21] and misalignment between AM and PM signals [22].

Two strategies are widely utilized to generate the phase modulator's updating clock (CKU) that is synchronous with CKV. One is to frequency-divide the CKV [14], [17], [19], [22], [23]; the other is to re-time the significant edge of the PLL's reference clock (FREF) by that of CKV [1], [21], [24], as exemplified by the CKU generation timing diagram in Fig. 1 (in this design, the significant edges of FREF and CKV are both falling, while those of CKU are rising). Since CKV is phase modulated, any clock synchronous with CKV will exhibit some non-uniformity—the clock periods are time-varying; the offsets between its significant edges and those corresponding to an ideal uniform clock (e.g., those between CKU and FREF in Fig. 1) vary across cycles. Considering that PLL-based phase modulators have overwhelmingly adopted the two-point modulation scheme [25], [26], which directly modulates the DCO phase through one feed point and eliminates the excess phase prior to the phase detector through the other feed point, the non-uniform period and time-varying offset of the generated clock will, respectively, affect the DCO PM and excess phase elimination (details will come in Section II-B). These two mechanisms will disturb the PLL and finally degrade the EVM. Currently, the prior arts [14], [23] merely tackle the effects of period variation, but ignore the impairment related to offset variation. Even for the period variation compensation, the existing methods are only valid for the CKU generated by dividing CKV, whose period is determined by the instantaneous CKV frequency, but cannot be extended to the case of using the reference clock re-timed to CKV, whose period is affected by the accumulative CKV phase.

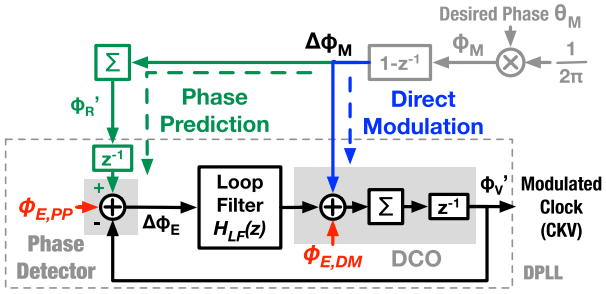


Fig. 2. Discrete-time domain model of an ideal PLL-based phase modulator with a two-point modulation. The gains of DCO and phase detector, respectively, K_{DCO} and K_{PD}, are implied as normalized, as in [27], hence hidden.

In this article, being an extended version of [28], we propose a phase modulator for a polar TX that utilizes a two-point PLL modulation scheme and updates data at a non-uniform digital clock, which is generated by re-timing the reference clock to CKV, thus inevitably disturbing the PLL and degrading the EVM of the output signal. To analyze the variations and effects of the re-timed clock, we extend the conventional discrete-time phase modulator model to a hybrid-time domain (Section II). Based on this new model, we propose a non-uniform clock compensation (NUCC) scheme to suppress the disturbance on the PLL and improve the PM accuracy (Section III). Furthermore, a phase-domain digital predistortion (DPD) is also proposed to combat the $1/\sqrt{LC}$-induced DCO nonlinearity (Section IV). Parameters of the proposed DPD are established analytically, thereby avoiding the hardship of a frequency-dependent calibration. The implemented phase modulator (Section V) was experimentally verified with a 60 Mb/s 64-PSK signal to prove the efficacy of the proposed NUCC and phase-domain DPD (Section VI).

II. Modeling a PLL-Based Phase Modulator

A. Ideal Phase Modulator Model in Discrete-Time Domain

Fig. 2 shows a discrete-time domain model of an ideal PLL-based phase modulator. To produce the CKV clock with the excess phase ϕ'_V (i.e., excluding the carrier component), the desired modulation commanding phase θ_M is first normalized by $1/(2\pi)$ to ϕ_M.[1] Then, ϕ_M is differentiated to $\Delta\phi_M$, which is the target phase shift to be developed by ϕ'_V during a single reference cycle. $\Delta\phi_M$ modulates the PLL through two feeding points [29], defined as direct modulation (DM) and phase prediction (PP). Through the DM point, $\Delta\phi_M$ directly

[1]In this article, the phase symbol θ is in the conventional unit of radian, but, for practical reasons, ϕ is normalized by $1/(2\pi)$, i.e., in unit intervals (UI).

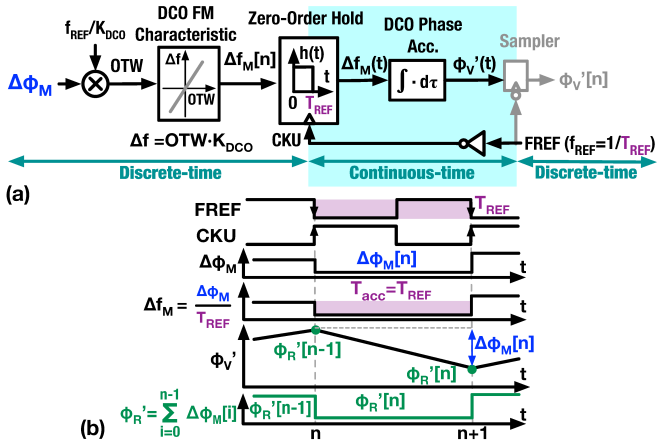


Fig. 3. Hybrid-time model of the DCO: (a) schematic and (b) waveforms.

modulates the DCO. Due to its phase integration nature [30], the DCO accumulates $\Delta\phi_M$ cycle by cycle such that the output phase ϕ'_V equals the delayed modulation target ϕ_M, i.e., $\phi'_V[n] = \phi_M[n-1]$. Meanwhile, the PP-related path also emulates the DCO behavior for its elimination purpose, i.e., by accumulating $\Delta\phi_M$ and then delaying it to predict the DCO phase with $\phi'_R[n-1]$. Any deviation of ϕ'_V from ϕ'_R, i.e., $\Delta\phi_E$, will be detected and gradually corrected by the loop.

Ideally, $\phi'_V[n] = \phi'_R[n-1]$, so $\Delta\phi_E = 0$ signifies that the loop is oblivious to the modulation "perturbations." In practice, however, errors will occur in relation to these two feed points. The DM-induced error is denoted as $\phi_{E,\mathrm{DM}}$ and stems from various impairments of the DCO, such as its phase noise and frequency quantization, as well as the nonlinearity of its FM characteristics. Without the feedback loop, even a tiny but persistent $\phi_{E,\mathrm{DM}}$ can accumulate without bound in the DCO as a PM error. Fortunately, a closed-loop PLL will gradually correct it, thus preventing the accumulation in the long run. A wider PLL bandwidth helps to suppress the effects of $\phi_{E,\mathrm{DM}}$, but it makes the PM accuracy more vulnerable to the PP-induced error, i.e., $\phi_{E,\mathrm{PP}}$, which stems from the phase detector's noise and nonlinearity, as well as the prediction error of ϕ'_R. This implies an optimum PLL bandwidth to balance the PM error due to $\phi_{E,\mathrm{DM}}$ and $\phi_{E,\mathrm{PP}}$. However, the optimum bandwidth is merely a trade-off. To achieve a lower EVM, this work focuses on minimizing both $\phi_{E,\mathrm{DM}}$ and $\phi_{E,\mathrm{PP}}$.

B. DCO Model in Hybrid-Time Domain

The DCO model in Fig. 2 is merely a discrete-time domain approximation assuming that both the modulating input $\Delta\phi_M$ and developed output phase ϕ'_V update simultaneously on the same uniform clock-spacing grid, thus incapable of properly handling the effects of clock impairments, i.e., the FM-induced skew and period variations. To include these non-idealities, the DCO model is expanded to a hybrid (i.e., discrete/continuous)-time domain, with the diagram and waveforms shown in Fig. 3. The DCO is basically an FM device whose offset frequency Δf_M from the f_0 carrier changes instantaneously in response to the OTW that is updated by the CKU clock. This FM characteristic is modeled in the discrete-time domain. To be consistent with the discrete-time DCO in Fig. 2, we expediently use an ideal CKU aligned with the PLL's reference (FREF), but we will add the timing non-idealities to the CKU later. Considering that OTW is denormalized from $\Delta\phi_M$ by $f_{\mathrm{REF}}/K_{\mathrm{DCO}}$, where f_{REF} is the frequency of FREF and K_{DCO} is the DCO FM transfer gain, then Δf_M during the nth clock cycle is related to $\Delta\phi_M$ by the following equation:

$$\Delta f_M[n] = \Delta\phi_M[n] \cdot f_{\mathrm{REF}} = \frac{\Delta\phi_M[n]}{T_{\mathrm{REF}}} \tag{1}$$

where T_{REF} is the period of FREF. On the other hand, the DCO also exhibits phase-accumulation characteristic with which it acquires the excess phase ϕ'_V by integrating Δf_M over time [31], i.e., $\phi'_V(t) = \int_0^t \Delta f_M(\tau)\mathrm{d}\tau$. This characteristic is modeled in a continuous-time domain, and a zero-order hold is added to convert the discrete-time $\Delta f_M[n]$ to continuous-time $\Delta f_M(t)$ [32]. Thus, the continuous-time $\phi'_V(t)$ can be described as follows:

$$\phi'_V(t) = \sum_{i=0}^{n-1} \Delta\phi_M[i] + \Delta f_M[n] \cdot (t - n \cdot T_{\mathrm{REF}}) \tag{2}$$

where $n = \lfloor t/T_{\mathrm{REF}} \rfloor$. Interestingly, $\phi'_V(t)$ sampled by FREF (for phase detection), i.e., $\phi'_V[n]$, equals the $\sum_{i=0}^{n-1} \Delta\phi_M[i]$ term, which is exactly the $\phi'_V[n]$ prediction term $\phi'_R[n-1]$ in Fig. 2. Consequently, no error will be detected and so the PLL remains unperturbed. Note that two conditions should be satisfied to perfectly cancel the sampled and predicted phases. First, from the phase accumulation aspect, the excess phase shift in the nth clock cycle should exactly equal the input of $\Delta\Phi_M$, i.e.,

$$\Delta\phi'_V[n] = \Delta f_M[n] \cdot T_{\mathrm{REF}} = \Delta\phi_M[n]. \tag{3}$$

Aside from an Δf_M error caused by the DCO FM nonlinearity, this condition can also be impaired by the DCO-phase-accumulation time (T_{acc}) deviating from T_{REF} [33]. This occurs if CKU is time-varying, as in Fig. 1. Then, the CKU period variation will degrade the PM accuracy through $\phi_{E,\mathrm{DM}}$. Second, from the phase-detection perspective, the DCO update clock CKU should ideally align with the sampling clock FREF. If any offset exists (this will be discussed in Section II-C), ϕ'_R will not precisely predict ϕ'_V. The associated error adds to $\phi_{E,\mathrm{PP}}$, thereby disturbing the PLL and affecting the EVM.

C. Hybrid-Time Model of Phase Modulator

A realistic CKU might not be perfectly aligned with FREF due to various circuit delays on the FM path, e.g., CKU's propagation delay and DCO's settling time. For simplicity, all these delays are included in the nominally constant offset between FREF and CKU, i.e., Δt_{cnst} (exaggerated) in Fig. 4(a). Then, ϕ'_R predicts $\phi'_V(t)$ sampled at the CKU grid, instead of that at FREF. Therefore, using ϕ'_R for the phase detection leaks some ϕ'_V information to $\phi_{E,\mathrm{PP}}$, resulting in an error of

$$\phi_{\mathrm{R2S}}[n] = \Delta t_{\mathrm{cnst}} \cdot \Delta f_M[n] = \frac{\Delta t_{\mathrm{cnst}}}{T_{\mathrm{REF}}} \cdot \Delta\phi_M[n]. \tag{4}$$

Fig. 4(b) sketches a hybrid-time phase-modulator model, which merges the hybrid-time DCO in Fig. 3(a) with the discrete-time phase modulator of Fig. 2. To reflect the ϕ'_V

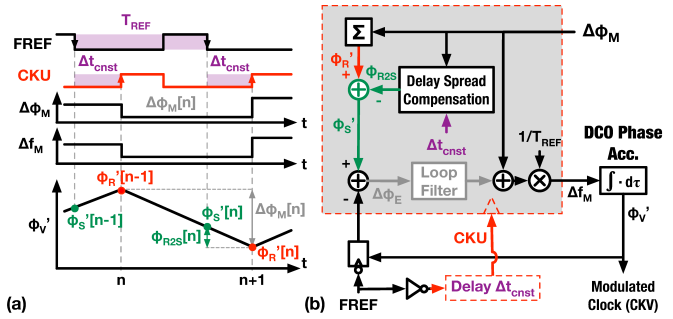


Fig. 4. Phase modulator with delay spread compensation: (a) waveforms and (b) block diagram.

leakage mechanism due to the Δt_{cnst} skew, the hybrid model emphasizes the clock-domains—FREF is used in the ϕ'_V sampling and CKU drives all the remaining discrete-time blocks and updates the DCO's Δf_M. Furthermore, this model also converts $\phi'_R[n]$ to the $\phi'_V(t)$ prediction at the FREF grid, i.e., $\phi'_S[n] = \phi'_R[n] - \phi_{\text{R2S}}[n]$. Utilizing ϕ'_S for phase detection can completely avoid the ϕ'_V leakage.

It should be noted that [15] has also found this ϕ'_V leakage mechanism, defined as "delay spread," and compensated for it by recursively predicting ϕ'_S. However, [15] considers only the case of constant Δt_{cnst}. In the non-uniform CKU case (to be discussed in Section III), CKU's offset relative to FREF becomes time-varying. Under such a condition, using ϕ_{R2S} to predict ϕ'_S can be more convenient, since it only involves the phase accumulation within one CKU cycle and the prediction error would not propagate to or accumulate on subsequent cycles due to the non-recursive form.

III. Non-Uniform Clock Compensation

A. Foundation for NUCC—Δt_S Estimation

Due to the system-level constraints discussed in Section I, the proposed phase modulator adopts the *update* clock CKU that is generated by re-timing the FREF falling edge to the 5th subsequent CKV falling edge (for timing reasons), as shown in Fig. 5(a). Consequently, CKU shows the time-varying offset (relative to FREF) and period, thus, respectively, contributing errors to $\phi_{E,\text{PP}}$ and $\phi_{E,\text{DM}}$. To tackle these errors, the first step is to estimate the variations of CKU offset and period. This entails knowing Δt_S, i.e., the instantaneous time offset between FREF and its first subsequent CKV edge, due to two reasons: Regarding the CKU's offset from FREF, Δt_S dominates the variation component because this offset breaks down to two parts—Δt_S and four CKV periods (i.e., $4T_{\text{CKV}}[n]$, where $T_{\text{CKV}}[n]$ is the CKV period during the nth CKU cycle). The former one varies across CKU cycles; the latter one is roughly constant, approximately 4 average $T_{\text{CKV}}[n]$, i.e., $\Delta t_{\text{cnst}} \approx 4\overline{T_{\text{CKV}}}$, given that BW_{FM} is sufficiently smaller than the DCO carrier frequency (f_0). Regarding the CKU period, its variation can be simply derived by differentiating the relevant offsets, more specifically Δt_S's.

Actually, the Δt_S prediction is widely used in the recent PLLs to narrow down the phase detectors' input range [34], [35], [36], [37], [38]. Predicting Δt_S requires the absolute phase of CKV, i.e., ϕ_V, which counts not only the excess phase ϕ'_V due to modulation, but also the carrier phase ϕ_{C} [see Fig. 5(b)].[2] Using the predicted ϕ_V at the FREF grid, i.e., ϕ_S, Δt_S in the nth CKU cycle can be predicted as follows:

$$\Delta t_S[n] \approx (1 - \phi_{S,\text{frac}}[n]) \cdot \overline{T_{\text{CKV}}} \tag{5}$$

where $\phi_{S,\text{frac}}$ is the fractional part of ϕ_S.

To facilitate the Δt_S prediction, the phase modulator model in Fig. 5(c) includes the DCO's carrier phase ϕ_{C}: On the direct-modulation side, ϕ_{C} is modeled by integrating the DCO carrier frequency f_0 over time. Then ϕ_{C} adds to ϕ'_V to represent the absolute CKV phase ϕ_V. On the phase-prediction side, the frequency control word (FCW), i.e.,

$$\text{FCW} = \frac{f_0}{f_{\text{REF}}} = \frac{T_{\text{REF}}}{\overline{T_{\text{CKV}}}} \tag{6}$$

is accumulated to reflect the behavior of ϕ_{C} at the FREF grid

$$\phi_C[n] = \int_0^{n \cdot T_{\text{REF}}} f_0 \text{d}\tau = \sum^{n} \text{FCW}. \tag{7}$$

The accumulated FCW adds to ϕ'_S (the prediction of ϕ'_V at the FREF grid), yielding ϕ_S. With its fractional part $\phi_{S,\text{frac}}$, the NUCC block can predict Δt_S as well as estimate the CKU's period and offset deviation relative to FREF, and then compensate the associated effects on $\phi_{E,\text{DM}}$ and $\phi_{E,\text{PP}}$ with ϕ_{DMC} and ϕ_{R2S}, respectively.

B. Tackling $\phi_{E,\text{DM}}$ Due to CKU Period Variation

Fig. 6 illustrates $\phi_{E,\text{DM}}$ due to the non-uniform period of CKU. The excess phase ϕ'_V will accumulate the desired phase shift of $\Delta\phi_M$ if the modulating frequency Δf_M precisely lasts the duration of T_{REF} [see (3)]. However, the realistic phase accumulation time T_{acc} deviates from T_{REF} due to the time-varying CKU. Therefore, an error of $\Delta\phi'_{V,E}$ is added onto ϕ'_V in each cycle. The error in the nth CKU cycle is

$$\Delta\phi'_{V,E}[n] = \frac{T_{\text{acc}}[n] - T_{\text{REF}}}{T_{\text{REF}}} \cdot \Delta\phi_M. \tag{8}$$

The $T_{\text{acc}}[n]$ variation relative to T_{REF} can be estimated by the following equation:

$$T_{\text{acc}}[n] - T_{\text{REF}} = \Delta t_S[n] - \Delta t_S[n-1]. \tag{9}$$

Substituting (5), (6), and (9) into (8) yields the estimation of $\Delta\phi'_{V,E}$ based on $\phi_{S,\text{frac}}$. To address $\Delta\phi'_{V,E}[n]$, the NUCC core adds to the direct-modulation-related path a compensation phase equal to $-\Delta\phi'_{V,E}[n]$ in the next CKU cycle, i.e.,

$$\phi_{\text{DMC}}[n+1] \approx (\phi_{S,\text{frac}}[n] - \phi_{S,\text{frac}}[n-1]) \cdot \frac{\Delta\phi_M[n]}{\text{FCW}}. \tag{10}$$

Consequently, the DCO frequency slightly changes by $\phi_{\text{DMC}}[n+1]/T_{\text{REF}}$. If this extra frequency shift could sustain for exactly T_{REF}, the DCO would acquire a compensation phase of $\phi_{\text{DMC}}[n+1]$ to perfectly correct the excess phase error $\Delta\phi'_{V,E}[n]$ from the previous cycle. However, this condition is violated due to the time-varying CKU period. Therefore, there is a secondary residue error with the magnitude around $\Delta\phi_M[n]/\text{FCW}^2$. Fortunately, this error is negligible, especially at large FCW's (e.g., FCW $>$ 60 in the implemented chip).

[2]In this article, a generic excess phase ϕ'_x represents the absolute phase ϕ_x excluding the ideal carrier phase ϕ_{C}.

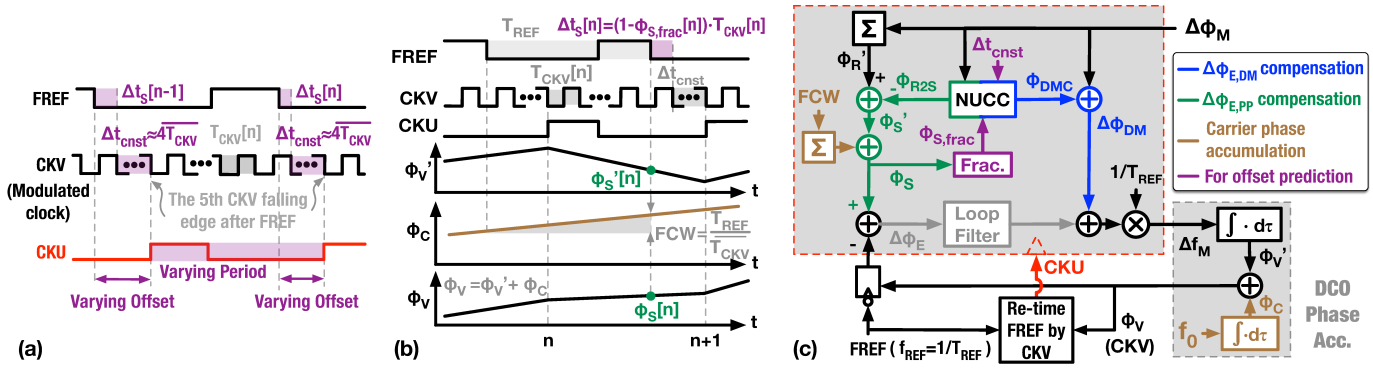


Fig. 5. Phase modulator with the proposed non-uniform clock compensation (NUCC): (a) Waveforms showing CKU generation by re-timing FREF by CKV, (b) waveforms illustrating the phases related to Δt_S prediction, and (c) system diagram.

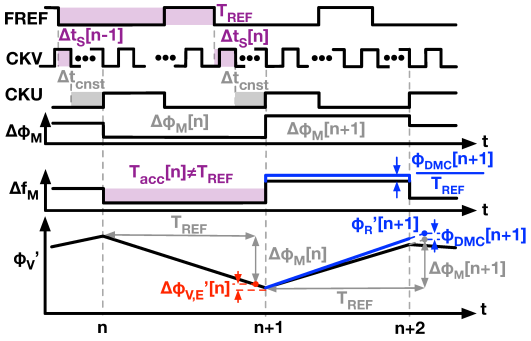


Fig. 6. Waveforms of the phase modulator, showing ϕ'_V error due to the non-uniform CKU period, i.e., $\Delta\phi'_{V,E}$, and the correction through ϕ_{DMC}.

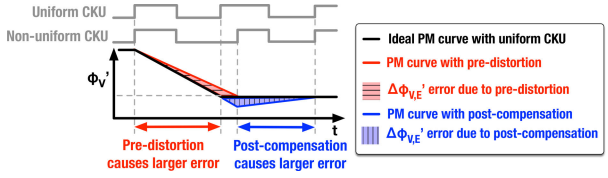


Fig. 7. Comparison of the $\Delta\phi'_{V,E}$ correction strategies in predistortion and post-compensation styles that correct the error with a latency of 0 or 1 CKU cycle, respectively.

One may also notice $\Delta\phi'_{V,E}$ is post-compensated, i.e., corrected with one CKU cycle latency, and wonder if it would be better to predistort $\Delta\phi'_{V,E}$ to prevent this error from occurring. In fact, these two methods would result in the same simulated EVM. The reason is clarified in Fig. 7. Due to the phase integration feature of DCO, compensating $\Delta\phi'_{V,E}$ takes one CKU cycle, instead of being completed immediately. Therefore, the $\Delta\phi'_{V,E}$-compensation error would stay on the $\phi'_V(t)$ trajectory for *one* clock cycle, whichever strategy is adopted.

C. Addressing $\phi_{E,\mathrm{PP}}$ Due to CKU Offset Variation

Compared to the delay spread compensation in Fig. 4, the $\phi_{E,\mathrm{PP}}$-compensation in NUCC specifically addresses the ϕ_{R2S} prediction error raised by the time-varying component of the offset between FREF and CKU. Similar to the scenario in (4), calculating $\phi_{\mathrm{R2S}}[n]$ requires the instantaneous modulation

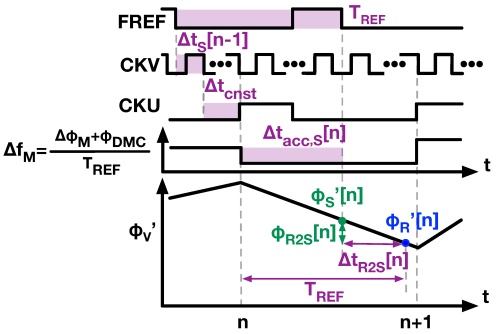


Fig. 8. Predicting ϕ'_S by subtracting ϕ_{R2S} from ϕ'_R, in face of the non-uniform CKU.

frequency $\Delta f_M[n]$ and time offset $\Delta t_{\mathrm{R2S}}[n]$, which replaces the constant Δt_{cnst} to characterize the time-varying delay between the two critical moments when the excess-phase trajectory $\phi'_V(t)$ crosses $\phi'_R[n]$ and $\phi'_S[n]$ (see Fig. 8). Since the aforementioned compensation phase ϕ_{DMC} from NUCC has shifted the modulation frequency to $\Delta f_M[n] = (\Delta\phi_M[n] + \phi_{\mathrm{DMC}}[n])/T_{\mathrm{REF}}$, ϕ_{R2S} can be determined by the following equation:

$$\phi_{\mathrm{R2S}}[n] = \frac{\Delta t_{\mathrm{R2S}}[n]}{T_{\mathrm{REF}}} \cdot (\Delta\phi_M[n] + \phi_{\mathrm{DMC}}[n]). \tag{11}$$

So far, $\Delta t_{\mathrm{R2S}}[n]$ is obscure because the $\phi'_R[n]$-crossing moment of $\phi'_V(t)$ deviates from the CKU grid. However, given that NUCC has compensated the $\Delta\phi'_{V,E}$ errors (due to the CKU period variation) from all the previous CKU cycles, ϕ'_V can ideally hit ϕ'_R if the relevant CKU cycle virtually lasts for the duration of T_{REF} (see $\phi'_R[n+1]$ and the related T_{REF} in Fig. 6). This observation helps to locate $\phi'_R[n]$ on the $\phi'_V(t)$ trajectory in Fig. 8, and finally leads to the conclusion that $\Delta t_{\mathrm{R2S}}[n]$ equals the time offset between FREF and CKU in the preceding CKU cycle, i.e.,

$$\Delta t_{\mathrm{R2S}}[n] = \Delta t_S[n-1] + \Delta t_{\mathrm{cnst}} \tag{12}$$

considering either side of the formula equals $T_{\mathrm{REF}} - \Delta t_{\mathrm{acc},S}[n]$, where $\Delta t_{\mathrm{acc},S}[n]$ denotes the duration between the nth CKU and the subsequent FREF edges. Substituting (5), (6), (12) into

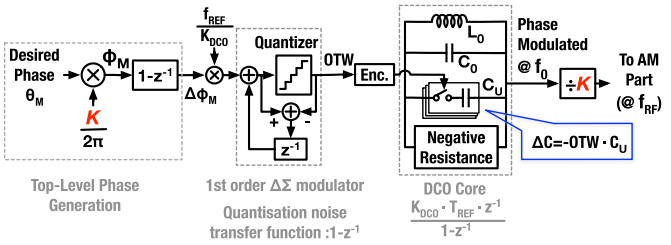


Fig. 9. Extracted open-loop representation in the direct-modulation path of the phase modulator, highlighting the influences of the forward frequency division ($\div K$), $\Sigma\Delta$ dithering and LC-tuning of the DCO.

(11) yields a $\phi_{S,\text{frac}}$-based ϕ_{R2S} prediction, i.e.,

$$\phi_{\text{R2S}}[n] \approx \left(\frac{\Delta t_{\text{cnst}}}{T_{\text{REF}}} + \frac{1-\phi_{S,\text{frac}}[n-1]}{\text{FCW}}\right) \cdot \Delta\phi_M[n] \quad (13)$$

where the ϕ_{DMC} term is ignored due to its negligible influences (in the order of $\Delta\phi_M/\text{FCW}^2$). Δt_{cnst} in this expression characterizes the constant component of the offset between FREF and CKU, thus can be estimated with the least mean squares (LMS) algorithm in [15]. Consequently, ϕ_{R2S}, ϕ'_S, and ϕ_S can be accurately predicted [see Fig. 5(c)]. This will not only compensate the $\phi_{E,\text{PP}}$ error due to the non-uniform CKU, but will also provide an accurate $\phi_{S,\text{frac}}$ for $\phi_{E,\text{DM}}$-compensation in the next cycle [see (10)].

IV. DCO Frequency Error Compensation

A. Characterizing the Error Induced by $1/\sqrt{LC}$

Fig. 9 sketches an open-loop representation of the direct-modulation path in a PLL-based phase modulator. The instantaneous resonant frequency of the LC tank is controlled by a switched-capacitor (SC) bank, thereby suffering from errors related to the $1/\sqrt{LC}$-induced nonlinearity. As mentioned in Section I, these errors increase dramatically at higher values of the fractional FM bandwidth $\text{BW}_{\text{FM}}/f_0$. The quantitative analysis starts with the DCO carrier frequency $f_0 = 1/(2\pi(L_0C_0)^{1/2})$, where L_0 and C_0 are the tank's inductance and capacitance, respectively. With the capacitance change of ΔC, the resonant frequency shifts by the following equation:

$$\Delta f(\Delta C) = \left(\frac{1}{\sqrt{1+\Delta C/C_0}} - 1\right) \cdot f_0. \quad (14)$$

However, nearly all published frequency modulators utilize just the linear (or first-order) approximation of (14) to estimate the frequency shift due to ΔC, i.e.,

$$\Delta f_{\text{lin}}(\Delta C) \approx -\frac{1}{2}\frac{\Delta C}{C_0} \cdot f_0. \quad (15)$$

Consequently, a realistic DCO frequency shift deviates from the expected Δf_{lin} with a relative error of

$$\text{Err}(\Delta f_{\text{lin}}) = \frac{\Delta f - \Delta f_{\text{lin}}}{\Delta f_{\text{lin}}} \approx \frac{3}{2}\frac{\Delta f_{\text{lin}}}{f_0}. \quad (16)$$

Considering that the maximum Δf_{lin} during modulation equals half of the FM bandwidth (i.e., $\text{BW}_{\text{FM}}/2$), $\text{BW}_{\text{FM}}/f_0$ thus reflects the level of the $1/\sqrt{LC}$-induced FM error.

According to the discussion above, a polar TX under the assumption of invariant signal characteristics (e.g., BW_{sig} and BW_{FM}) suffers from a higher $1/\sqrt{LC}$-induced PM error when it generates a lower RF channel frequency f_{RF} simply due to the increased $\text{BW}_{\text{FM}}/f_0$, if the DCO directly oscillates at f_{RF}, i.e., $f_0 = f_{\text{RF}}$. However, in a practical polar TX, the DCO output may be first scaled down by a programmable frequency divider $\div K$ before input to the AM part (see Fig. 9) so as to extend the lower operational range of f_{RF} [17]. Since $\div K$ allows the DCO to maintain the resonance at high frequency, i.e., $f_0 = K \cdot f_{\text{RF}}$, one may wonder how this would affect the nonlinearity characterized by $\text{BW}_{\text{FM}}/f_0$. Actually, $\div K$ also attenuates the DCO phase by K. To ensure the divided output maintains the desired phase θ_M, it should be amplified by K before modulating the DCO (see Fig. 9). This forces BW_{FM} to also expand by K. In the end, $\text{BW}_{\text{FM}}/f_0$ and the $1/\sqrt{LC}$-induced nonlinearity remains the same as in the basic case of $f_0 = f_{\text{RF}}$.

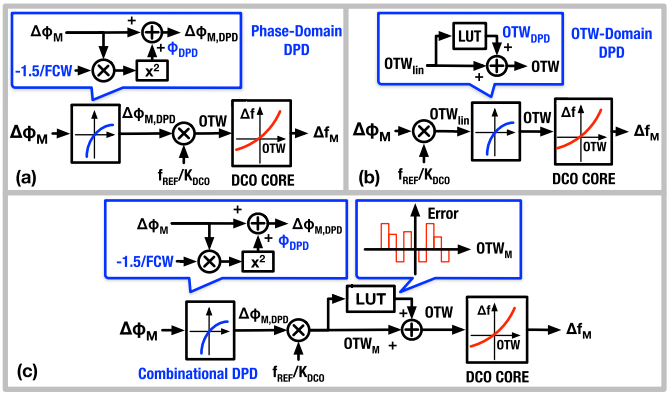


Fig. 10. Predistorting of DCO nonlinearity in (a) phase domain, (b) OTW domain, and (c) both domains, i.e., the combinational DPD.

B. Phase-Domain DPD

Considering the DCO nonlinearity due to the $1/\sqrt{LC}$ law being well captured in the presented math formulas, it can be compensated by polynomials whose coefficients are determined by pure math. As shown in Fig. 10(a), we predistort the nonlinearity in the phase domain with a second-order polynomial term, i.e., adding it to $\Delta\phi_M$. Derivation of this coefficient relies on the LC-DCO model in Fig. 9. Considering (14) and the capacitance change due to OTW, i.e., $\Delta C = -\text{OTW} \cdot C_U$, where C_U is the capacitance of the SC units, the DCO frequency shift of Δf would require an OTW of

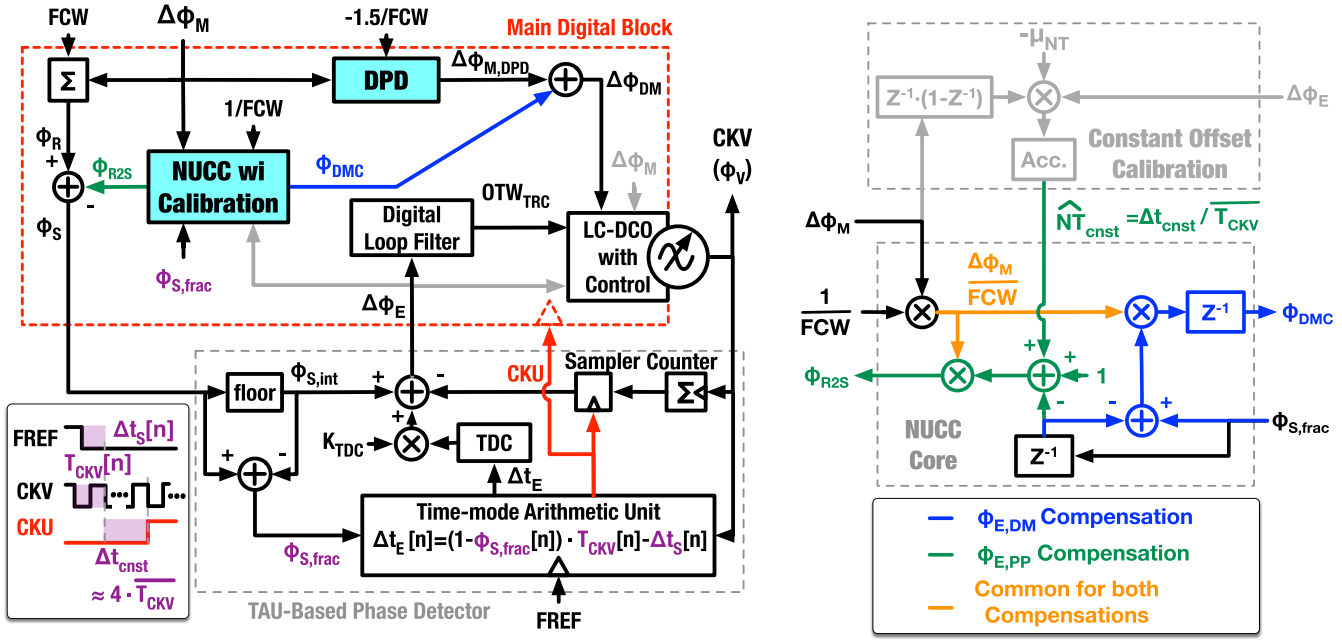
$$\text{OTW} = \frac{C_0}{C_U} \cdot \left[1 - \frac{1}{(1+\Delta f/f_0)^2}\right]. \quad (17)$$

By applying a Taylor series to (17) and exploiting (1) and (6), OTW can be written as a function of $\Delta\phi_M$

$$\text{OTW} = \frac{C_0}{C_U} \cdot \left[\frac{2\Delta\phi_M}{\text{FCW}} - \sum_{i=2}^{\infty}(i+1) \cdot \left(-\frac{\Delta\phi_M}{\text{FCW}}\right)^i\right]. \quad (18)$$

The coefficient of the linear $\Delta\phi_M$ term also equals $f_{\text{REF}}/K_{\text{DCO}}$, which is the denormalization factor from $\Delta\phi_M$ to OTW in the linearized DCO models, e.g., Fig. 3(a). Therefore, (18) can be rewritten as follows:

$$\text{OTW} = \frac{f_{\text{REF}}}{K_{\text{DCO}}} \cdot [\Delta\phi_M + \phi_{\text{DPD}}] \quad (19)$$



(a) (b)

Fig. 11. (a) Simplified block diagram of the implemented phase modulator, where the gray signals are used in the LMS calibration and (b) implementation of NUCC with the calibration for the constant time offset, Δt_{cnst}.

where

$$\phi_{\text{DPD}} = \sum_{i=2}^{\infty} \frac{i+1}{2 \cdot (-\text{FCW})^{i-1}} \cdot \Delta\phi_M^i. \tag{20}$$

ϕ_{DPD} can be used for the phase-domain DPD. In the implemented system, the terms with $i > 2$ are discarded as negligible.

Interestingly, prior arts tend to predistort the DCO nonlinearity exclusively in the OTW domain [12], [17], [18], i.e., by adding a compensation signal OTW_{DPD} into OTW [Fig. 10(b)], rather than into $\Delta\phi_M$. According to (19) and (20), OTW_{DPD} significantly correlates with K_{DCO}, i.e.,

$$\text{OTW}_{\text{DPD}} = \sum_{i=2}^{\infty} \frac{i+1}{2} \left(-\frac{K_{\text{DCO}}}{\text{FCW} \cdot f_{\text{REF}}} \right)^{i-1} \cdot \text{OTW}_{\text{lin}}^i \tag{21}$$

where OTW_{lin} is the OTW linearly denormalized without DPD, i.e., $\text{OTW}_{\text{lin}} = \Delta\phi_M \cdot f_{\text{REF}}/K_{\text{DCO}}$. Considering K_{DCO} varies dramatically across frequency [16], this might come as no surprise as to why the prior arts suffer from the frequency-dependent OTW_{DPD}, thus requiring extensive calibration. In contrast, the phase-domain DPD can be calibration-free because the coefficients in (20) rely only on the foreknown FCW.

Note that the phase-domain DPD mainly tackles the nonlinearity caused by the $1/\sqrt{LC}$ law. As for that caused by device mismatches, the OTW-domain DPD can address it with relatively fixed settings since the mismatch is expected to be stable after the fabrication [16]. Therefore, combining the OTW- and phase-domain DPD ultimately leads to a frequency-insensitive solution to address the DCO nonlinearity, i.e., the combinational DPD in Fig. 10(c).

V. System Implementation

A. System Overview

Fig. 11(a) presents an overview of the implemented phase modulator. The main body is a time-mode-arithmetic-unit (TAU)-based PLL reported in [39], which natively operates in a fractional-N regime and where the phase error (i.e., normalized timing of CKV relative to FREF), $\Delta\phi_E$, is extracted by the TAU-based phase detector, then passed through the digital loop filter to be iteratively corrected by tuning the DCO through OTW_{TRC} (the OTW for carrier *tracking*). The phase detector extracts $\Delta\phi_E$ according to ϕ_S, i.e., the predicted CKV phase ϕ_V at the FREF grid, in a coarse-fine style: The coarse path counts the number of CKV edges, representing the integer part of ϕ_V, then cancels it with the integer portion of ϕ_S, i.e., $\phi_{S,\text{int}}$. On the fine path, the TAU samples Δt_S, reflecting the fractional ϕ_V, cancel it with T_{CKV} scaled by $(1 - \phi_{S,\text{frac}})$ to extract the time error Δt_E. After Δt_E is quantized by a time-to-digital converter (TDC) and normalized by the TDC gain (K_{TDC}), the resulting phase adds to that of the coarse path, constituting $\Delta\phi_E$. The TAU also launches the CKU, which aligns with the fifth CKV falling edge after FREF and clocks the main digital block.

The PM function is realized through the two-point modulation scheme: On the DM side, the phase shift target $\Delta\phi_M$ is added to ϕ_V by tuning the DCO's offset frequency through $\Delta\phi_{\text{DM}}$; on the PP side, $\Delta\phi_M$ accumulates with FCW so that ϕ_S reflects the excess phase and ideally cancels with the sampled ϕ_V prior to the digital loop filter. As discussed in Sections III and IV, the PM accuracy suffers from two significant error sources. One is the DCO's FM nonlinearity raised by $1/\sqrt{LC}$, which is compensated by the proposed second-order phase-domain DPD. The other is the non-uniform

characteristics of CKU. It is tackled by the NUCC introduced in Fig. 5(c), whose separate accumulators for FCW and $\Delta\phi_M$ are combined here without affecting the functionality.

B. Implementation of NUCC

Fig. 11(b) shows the implemented NUCC. The $\phi_{E,\mathrm{DM}}$ and $\phi_{E,\mathrm{PP}}$ compensation paths share the common term $\Delta\phi_M/\mathrm{FCW}$, which characterizes the expected phase accumulation on DCO during the average CKV period, i.e.,

$$\Delta f_M[n]\cdot\overline{T_{\mathrm{CKV}}}=\Delta\phi_M[n]\cdot\frac{\overline{T_{\mathrm{CKV}}}}{T_{\mathrm{REF}}}=\frac{\Delta\phi_M[n]}{\mathrm{FCW}}. \tag{22}$$

Scaling $\Delta\phi_M/\mathrm{FCW}$ with $(\phi_{S,\mathrm{frac}}[n]-\phi_{S,\mathrm{frac}}[n-1])$ yields ϕ_{DMC}, which compensates $\phi_{E,\mathrm{DM}}$ due to the CKU period variation. This matches (10). To compensate $\phi_{E,\mathrm{PP}}$ due to the CKU offset variation, $\Delta\phi_M/\mathrm{FCW}$ is scaled to generate ϕ_{R2S}, i.e.,

$$\phi_{\mathrm{R2S}}[n]=(\widehat{NT}_{\mathrm{cnst}}+1-\phi_{S,\mathrm{frac}}[n-1])\cdot\frac{\Delta\phi_M[n]}{\mathrm{FCW}}. \tag{23}$$

This equation is a re-arranged version of (13). $\widehat{NT}_{\mathrm{cnst}}$ represents the constant component of CKU offset (relative to FREF) normalized by the average CKV period, i.e.,

$$\widehat{NT}_{\mathrm{cnst}}=\frac{\Delta t_{\mathrm{cnst}}}{\overline{T_{\mathrm{CKV}}}}. \tag{24}$$

$\widehat{NT}_{\mathrm{cnst}}$ is estimated by an LMS algorithm that correlates the differentiated $\Delta\phi_M$ with the detected phase error $\Delta\phi_E$, emulating [15]. The diagram is also shown in Fig. 11(b), where the factor μ_{NT} adjusts the calibration convergence speed.

Obviously, larger amplitudes in ϕ_{R2S} and ϕ_{DMC} indicate that more PM error is compensated by NUCC. Since $\Delta\phi_M/\mathrm{FCW}$ is the base scaling term in both (10) and (23), NUCC can improve the PM accuracy more conspicuously when a wideband signal (with a higher distribution probability at large $\Delta\phi_M$ amplitudes) modulates the PLL with a small FCW. Besides, the impact of ϕ_{DMC} outweighs that of ϕ_{R2S}: The former scales $\Delta\phi_M/\mathrm{FCW}$ with a factor (i.e., $\phi_{S,\mathrm{frac}}[n]-\phi_{S,\mathrm{frac}}[n-1]$) ranging from -1 to 1, and reduces $\phi_{E,\mathrm{DM}}$, which could directly accumulate on the DCO and interfere with the PM signal across multiple CKU cycles until corrected by the PLL. The latter scales $\Delta\phi_M/\mathrm{FCW}$ with a factor (i.e., $\phi_{S,\mathrm{frac}}[n-1]$) distributed within [0, 1), and reduces $\phi_{E,\mathrm{PP}}$, which can be attenuated by the loop filter before disturbing the DCO.

Since NUCC tackles the $\phi_{E,\mathrm{DM}}$ and $\phi_{E,\mathrm{PP}}$ errors whose impacts depend on the PLL bandwidth (see Section II-A), the EVM improvement due to NUCC is also bandwidth-dependent. To demonstrate that, time-domain simulations of a 3188-MHz PLL-based phase modulator shown in Fig. 11 have been carried out. The simulation conditions (e.g., using a 64-PSK signal, f_{REF} of 40 MHz, feedforward frequency division $K=8$, and so on) and the way to evaluate EVM are identical as in the measurements later presented in Fig. 20(b). The DCO in this simulation has perfect linearity and ultra-fine resolution, thereby contributing negligible distortion and quantization error to EVM. This benefits in observing the impacts of non-uniform CKU and NUCC. The simulated EVM versus the PLL bandwidth is shown in Fig. 12. Enabling NUCC (see the "NUCC on" curve) improves EVM by at least 10 dB compared with the case when NUCC is disabled (see the "NUCC off" curve). Hence, the "NUCC off" behavior is dominated by the impact of non-uniform CKU, thereby roughly reflecting the EVM degradation due to the non-uniform CKU. According to the "NUCC off" curve, the non-uniform CKU degrades EVM more forcefully at narrower PLL bandwidths because the degradation is dominated by the $\phi_{E,\mathrm{DM}}$ error being less suppressed by the PLL loop. Therefore, especially at low PLL bandwidths, the bulk of EVM improvement from NUCC is obtained by merely enabling ϕ_{DMC} (see the curve of "only ϕ_{DMC} of NUCC on"). The EVM associated with the ϕ_{DMC}-only option increases at wider PLL bandwidths because the non-uniform CKU contributes more PM error through $\phi_{E,\mathrm{PP}}$ when the PLL bandwidth is wider. This necessitates activating the ϕ_{R2S} component of NUCC at wide PLL bandwidths. Finally, simultaneously utilizing both options in NUCC nearly entirely removes the effects of non-uniform CKU and lowers the EVM to the level limited by phase noise across a wide range of PLL bandwidths.

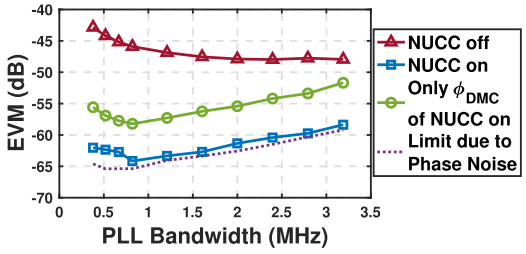


Fig. 12. Simulated EVM versus PLL bandwidth under different NUCC settings. The simulation conditions (i.e., PM signal, reference frequency f_{REF}, carrier frequency f_0, feedforward division ratio K, and so on) are the same as those in Fig. 20(b).

C. DCO With Calibration

Fig. 13(a) depicts a schematic of the DCO core, consisting of the LC-tank and complementary cross-coupled transistor pairs. The resonant frequency is tuned by the switched-capacitor (SC) banks. While performing PM, the active banks can be functionally categorized into two types. The first tracks the carrier, i.e., the 32-b unary tracking bank (TB). The second is used for FM and configured in a segmented style, i.e., consisting of an 8-b unary coarse modulation bank (MCB) and a 16-b unary fine modulation bank (MFB). All the encoded OTWs are resampled by CKU before toggling the DCO SC units in order to avoid the data-dependent propagation delay, which may vary the effective phase accumulation time in each CKU cycle and finally degrade the PM accuracy.

All the banks adopt the SC-unit structure sketched in Fig. 13(a), whose unit capacitor C_U is inspired by the layout of a SAR ADC [40]. Here, the ground and output (VP/VN) nets can shield the internal switching node from the surroundings to minimize the systematic capacitance mismatch. This layout style also allows the SC units to abut each other, thereby shortening critical connection lines (i.e., VP and VN) to minimize the FM error related to the parasitic routing inductance.

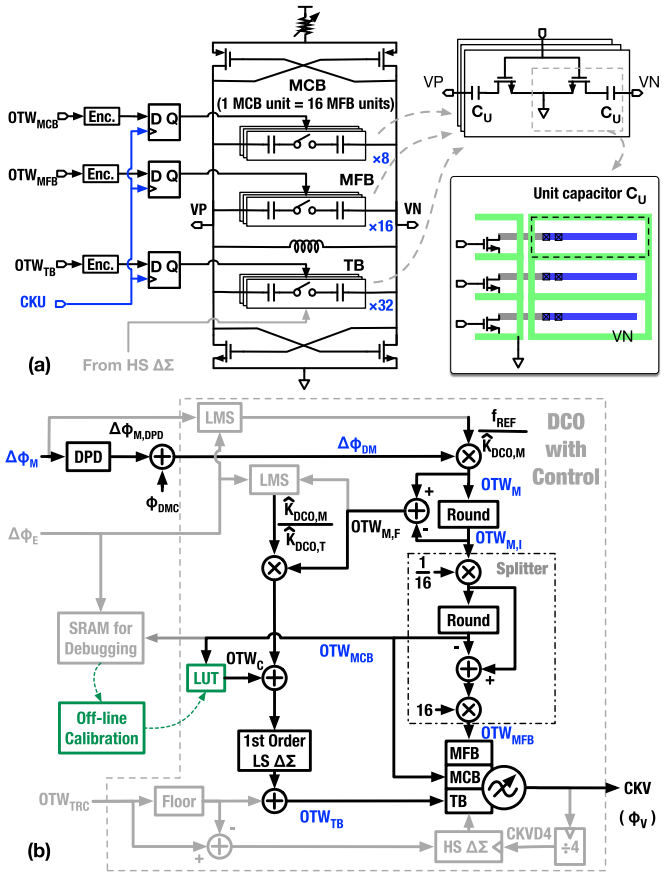


Fig. 13. (a) Schematic of the DCO core and (b) control logic surrounding the DCO core, where the digital blocks are implicitly clocked by CKU, except for the CKV clock divider (÷4) and the high speed (HS) ΔΣ.

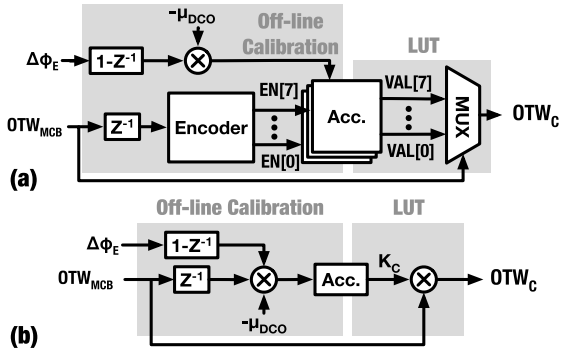


Fig. 14. Behavioral description of the LUT with off-line calibration in Fig. 13: (a) calibrating the LUT content with the piecewise LMS algorithm in [12] and (b) updating the LUT with an LMS algorithm emulating K_{DCO} calibration.

Fig. 13(b) illustrates the control logic surrounding the DCO core. Regarding the carrier phase tracking, the integer portion of OTW_{TRC}, i.e., OTW_{TB}, directly tunes the number of active TB units, and the fractional OTW_{TRC} dithers one TB unit through a high-speed (HS) ΔΣ modulator clocked by CKVD4 at 1/4 CKV frequency to improve resolution [27].

For PM, $\Delta\phi_{\text{DM}}$, i.e., the compensated $\Delta\phi_M$, is first denormalized to OTW_M by $f_{\text{REF}}/\widehat{K}_{\text{DCO},M}$, where $\widehat{K}_{\text{DCO},M}$ estimates the MFB's frequency resolution. To control MCB and MFB separately, the integer part of OTW_M after rounding, i.e., $\text{OTW}_{M,I}$, splits into OTW_{MCB} and OTW_{MFB} without extra re-scaling. This is because each MCB unit contains 16 MFB units, resulting in a nominal resolution ratio of 16. To employ TB's fine resolution (around 1/9 of the MFB), the rounding residue OTW_M, i.e., $\text{OTW}_{M,F}$, modulates TB after it is scaled by the resolution ratio between MFB and TB, i.e., $\widehat{K}_{\text{DCO},M}/\widehat{K}_{\text{DCO},T}$, where $\widehat{K}_{\text{DCO},T}$ estimates the frequency resolution of TB.

Among the three SC-banks, MCB has the coarsest resolution and affects the DCO FM linearity the most significantly. To address the frequency error associated with each OTW_{MCB} codeword (9 in total), a lookup table (LUT) adds an OTW_{MCB}-dependent compensation code, OTW_C, to the TB-tuning path. However, the control words from the scaled $\text{OTW}_{M,F}$ and LUT contain fractional bits, incompatible with the integer OTW_{TB}. Therefore, their sum is noise-shaped by a first-order low-speed (LS) ΔΣ modulator (at the CKU rate) before being added to OTW_{TB} to prevent the quantization error from accumulating on the DCO. To further suppress the quantization error, one can also add the fractional bits to the high-speed ΔΣ modulator, as in [11].

Two categories of parameters need to be estimated in Fig. 13(b). The first category is related to K_{DCO}, i.e., $f_{\text{REF}}/\widehat{K}_{\text{DCO},M}$ and $\widehat{K}_{\text{DCO},M}/\widehat{K}_{\text{DCO},T}$. They are calibrated by an LMS-based algorithm, which correlates the detected phase error $\Delta\phi_E$ [input of the digital loop filter, see Fig. 11(a)] and the relevant phase tuning target (i.e., $\Delta\phi_{\text{DM}}$ or $\text{OTW}_{M,F}$), as in [15]. The second category is the LUT content, which is updated by correlating $\Delta\phi_E$ with OTW_{MCB}. The detailed algorithm depends on the dominant mechanism of non-idealities in MCB. For example, if the mismatch between the MCB units dominates, the piecewise LMS algorithm shown in [12] is preferred. Fig. 14(a) sketches the calibration principle. The LUT function is represented by the mux which conditionally passes the OTW_{MCB}-associated compensation codes, $\text{VAL}[0,\ldots,7]$, to OTW_C. After the chosen $\text{VAL}[n]$ is used, the corresponding $\Delta\phi_E$ difference is scaled by μ_{DCO} and added to that $\text{VAL}[n]$ (enabled by EN[n]). VAL[n] finally converges at the value that exactly compensates for the error of the associated OTW_{MCB} codeword. One may notice only 8 VAL units (VAL[0] to VAL [7]) are adopted to compensate the 9 OTW_{MCB} codewords, i.e., integers ranging from -4 to 4 (considering MCB is 8-b unary). In fact, the frequency error associated with the codeword $\text{OTW}_{\text{MCB}} = 0$ gets implicitly counted in the carrier frequency f_0 and automatically corrected by the PLL since $\text{OTW}_{\text{MCB}} = 0$ is used when PLL locks the DCO to f_0.

On the other side, if the dominant DCO non-ideality mechanism arises from the gain mismatch between MCB and MFB, i.e., the resolution ratio between MCB and MFB deviates from the nominal 16, all the desired VAL's linearly correlate with OTW_{MCB} through the same factor, say K_C. Consequently, the piecewise calibration in Fig. 14(a) simplifies to a K_{DCO}-calibration-like algorithm shown in Fig. 14(b), where all the OTW_{MCB} codewords and their corresponding $\Delta\phi_E$ difference data are correlated with estimate the same gain factor K_C. Then, $K_C \cdot \text{OTW}_{\text{MCB}}$ replaces

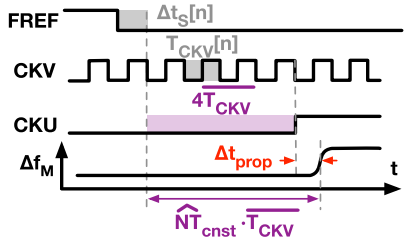


Fig. 15. Breaking down $\widehat{NT}_{\rm cnst}$ components.

the function of LUT. One may doubt whether K_C calibration interferes with that for $f_{\rm REF}/\widehat{K}_{{\rm DCO},M}$, considering both ultimately correlate $\Delta\phi_E$ with $\Delta\phi_M$ ($\rm OTW_{MCB}$ is proportional to $\Delta\phi_M$ if the phase-domain DPD is ignored). Actually, the mutual interference can be suppressed by activating these two calibrations at different moments: $f_{\rm REF}/\widehat{K}_{{\rm DCO},M}$ is calibrated only when $\rm OTW_{MCB} = 0$; during this time, K_C naturally does not update.

To maintain flexibility in modifying the algorithm, the LUT is updated in an off-line style [see Fig. 13(b)]: $\Delta\phi_E$ and $\rm OTW_{MCB}$ sequences are collected and stored in an SRAM for debugging. The software reads the data, processes it, and updates the LUT. With the new content in the LUT, $\Delta\phi_E$ and $\rm OTW_{MCB}$ samples are collected again to update the LUT, whose content settles after several iterations.

D. Calibrated Parameters in Face of Channel Hopping

The implemented system utilizes, in total, four calibration loops related to PM, i.e., those for $\widehat{NT}_{\rm cnst}$, $f_{\rm REF}/\widehat{K}_{{\rm DCO},M}$, $\widehat{K}_{{\rm DCO},M}/\widehat{K}_{{\rm DCO},T}$, and the LUT tackling the $\rm OTW_{MCB}$-associated error. Blindly re-calibrating all these parameters after channel hopping may take a long time before the EVM reaches back its optimum. To accelerate this re-calibration process, we first examine the frequency dependence of these parameters and then roughly compensate them according to the change in FCW.

Considering (24), $\widehat{NT}_{\rm cnst}$ is designed to be a constant 4 because $\Delta t_{\rm cnst}$ ideally represents an offset between CKU and the first CKV edge after FREF, and roughly equals $4\overline{T_{\rm CKV}}$. However, the DCO modulation frequency Δf_M does not change immediately after the rising edge of CKU. An additional delay, i.e., $\Delta t_{\rm prop}$ in Fig. 15, is always present mainly due to the propagation latency of control signals (e.g., OTW's). This delay is substantially constant in the time domain but turns frequency-dependent after being normalized by $\overline{T_{\rm CKV}}$. Since the estimated $\widehat{NT}_{\rm cnst}$ also counts $\Delta t_{\rm prop}$, the $\Delta t_{\rm prop}$-related part of $\widehat{NT}_{\rm cnst}$ should be re-normalized according to the FCW (inversely proportional to $\overline{T_{\rm CKV}}$) after each channel hopping, i.e.,

$$\widehat{NT}_{\rm cnst}\big|_{\rm new} = 4 + \left(\widehat{NT}_{\rm cnst}\big|_{\rm old} - 4\right)\cdot\frac{\rm FCW|_{new}}{\rm FCW|_{old}} \tag{25}$$

where the subscripts "old" and "new" distinguish the corresponding parameters in the previous and newly hopped channels. After the channel hopping, if $\Delta t_{\rm prop}$ does not significantly change (for example, caused by environmental variations, such as supply voltage or temperature), (25) can directly set $\widehat{NT}_{\rm cnst}$ to the value accurate enough to achieve optimum EVM in a new frequency channel. Consequently, re-calibration will be unnecessary.

Per mathematical derivation in [16], $K_{\rm DCO}$ exhibits a cubic relationship with the resonant frequency. Hence, after hopping to a new channel, $f_{\rm REF}/\widehat{K}_{{\rm DCO},M}$ should be re-calculated by the following equation:

$$\left.\frac{f_{\rm REF}}{\widehat{K}_{{\rm DCO},M}}\right|_{\rm new} = \left.\frac{f_{\rm REF}}{\widehat{K}_{{\rm DCO},M}}\right|_{\rm old}\cdot\left(\frac{\rm FCW|_{old}}{\rm FCW|_{new}}\right)^3. \tag{26}$$

This equation is derived under the assumption of an ideal inductor. Considering a real inductor behaves a bit differently due to its parasitic capacitance, the estimated value might not be accurate enough for low EVM. Hence, some further calibration might still be needed. In contrast, $\widehat{K}_{{\rm DCO},T}/\widehat{K}_{{\rm DCO},M}$ is determined by the capacitance ratio of the SC units in MFB and TB, thus independent of frequency and in no need of any further adjustment.

Regarding the LUT for MCB, it is utilized in combination with the phase-domain DPD which tackles the $1/\sqrt{LC}$-induced parabolic nonlinearity. Hence, the LUT mainly compensates for the non-idealities raised by device mismatches, e.g., the capacitance mismatch between MCB units or the gain mismatch between MCB and MFB. Considering these mismatch ratios are roughly constant after the fabrication, the LUT content does not need a frequency-dependent adjustment unless extremely low EVM is targeted.

In summary, after channel hopping, the values of $\widehat{NT}_{\rm cnst}$ and $f_{\rm REF}/K_{{\rm DCO},M}$ need to be modified using (25) and (26) to compensate their frequency dependence. Only $f_{\rm REF}/K_{{\rm DCO},M}$ needs re-calibration. These observations can help to shorten the calibration time.

E. Simplified Implementation Details of TAU

TAU is utilized here for phase detection because it exhibits high linearity (i.e., showing low fractional spurs in [39]), which helps to minimize the PM error due to $\phi_{E,\rm PP}$. The TAU in Fig. 11(a) is a universal timestamp-signal processor which outputs a weighted sum of an arbitrary number of timestamp inputs. In the implemented system, to extract the time error Δt_E induced by the phase noise and PM error, the TAU calculates the weighted sum of $T_{\rm CKV}$ and Δt_S as follows:

$$\Delta t_E[n] = (1-\phi_{S,\rm frac}[n])\cdot T_{\rm CKV}[n] - \Delta t_S[n]. \tag{27}$$

A simplified diagram of the TAU is shown at the bottom of Fig. 16. The controller programs the differential weighted time registers (WTR) to calculate (27).

Fig. 16 (top) shows the details of a WTR [39]. It outputs a constant time offset minus the weighted sum of all the time inputs, Δt_i's. The WTR consists of a variable resistor R_V, a variable capacitor C_V and a level-crossing slicer. The variable resistor and capacitor are, respectively, realized by switched-resistor and -capacitor banks, whose values are controlled by RT and CT codewords. Before processing the time inputs, the capacitor's voltage V_C is initially preset to $V_{\rm init}$ by a charging switch SWC. Then, LOW levels of the SWD signal discharge C_V through R_V. The widths of these active-low SWD pulses

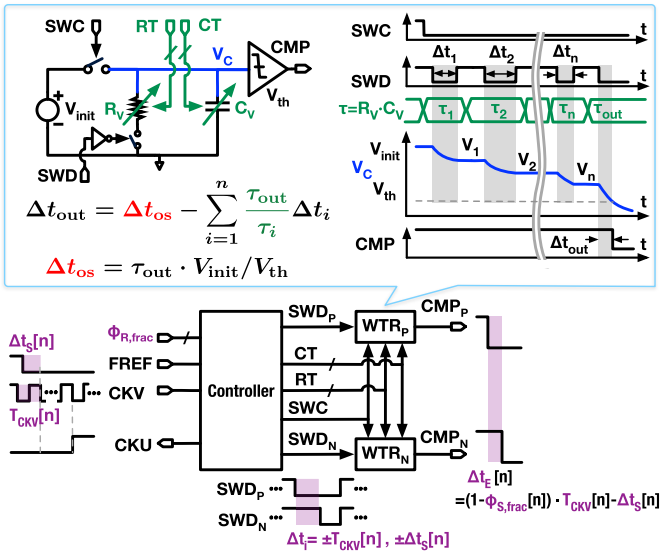


Fig. 16. Simplified diagram and waveforms of the TAU, which utilizes differential WTRs to calculate the weighted sum of input times (i.e., T_{CKV} and Δt_S) and outputs the result as Δt_E.

define the time inputs of the WTR, i.e., Δt_i's. These Δt_i's are stored and summed as voltage drops on V_C during the discharging events. The weights of Δt_i's in the summation are controlled by the RC product of R_V and C_V, i.e., $\tau = R_V \cdot C_V$. To properly read the weighted sum stored in the WTR, SWD should stay LOW till the slicer launches a CMP falling edge, indicating the moment V_C crosses V_{th}, threshold voltage of the slicer. The time offset between the last SWD falling edge and CMP asserting (i.e., falling edge) is defined as the WTR's time output Δt_{out}, which equals a constant time offset Δt_{os} minus the desired weighted sum of Δt_i's.

The implemented TAU ultimately uses two WTRs in a pseudo-differential manner to cancel Δt_{os} and add $\pm$ sign onto the Δt_is' weighting factors. Accordingly, the differential WTRs' inputs and output are, respectively, redefined as the width differences of the SWD pulse pairs and the time offsets between CMPs. The controller in TAU programs the differential WTRs to calculate (27)—The controller samples T_{CKV} and Δt_S from CKV and FREF clocks, and converts them to differential WTRs' inputs; the controller also encodes CT and RT sequences according to $(1 - \phi_{R,\mathrm{frac}})$. In addition, the controller also generates the master clock for the main digital blocks, i.e., CKU. More details are discussed in [39].

VI. Measurement Results

The proposed phase modulator is fabricated in TSMC 40-nm CMOS and occupies an active area of 0.31 mm^2 [excluding the pad drivers and SRAMs, see Fig. 17(a)]. With a reference clock of 40 MHz, it generates a phase-modulated clock whose carrier frequency f_0 ranges from 2.7 to 3.9 GHz. Fig. 17(b) shows the power consumption breakdown. The overall power drain is 4.6 mW, which is dominated by the DCO and its buffer, costing 2.35 mW at a 1.1 V supply. All other blocks are supplied with 1.0 V. The power consumption for the TAU-based phase detector sub-system (including TAU, TDC, counter, and so on) and digital logic are,

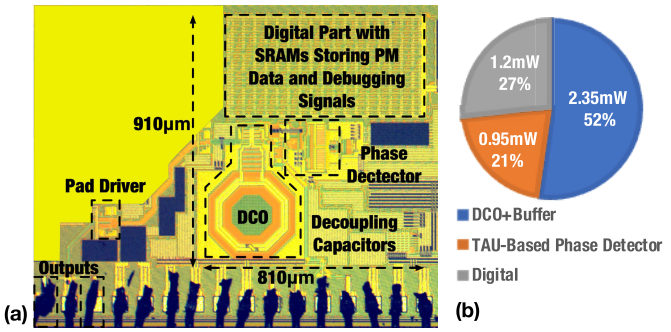


Fig. 17. (a) Chip micrograph and (b) power consumption breakdown.

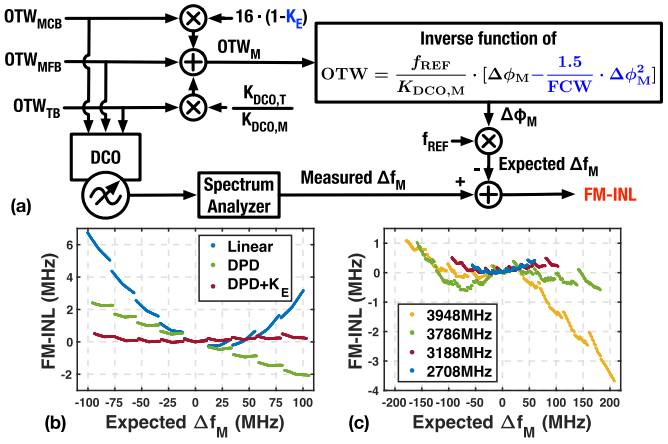


Fig. 18. DCO FM-INL: (a) Measurement setup, (b) measured results with different DCO linearization settings when $f_0 = 3188$ MHz, and (c) measured results with the proposed phase-domain DPD and the same $K_E = 0.023$ at multiple f_0's.

respectively, 0.95 and 1.2 mW. The digital power is measured with the feedforward frequency division $K = 8$ after engaging all the proposed options (i.e., phase domain DPD, LUT, NUCC), and the calibrations for $\widehat{NT}_{\mathrm{cnst}}$ and K_{DCO}'s. Considering the obvious circuit simplicity and low clock rate of the off-line calibration for the LUT, if the calibration shown in Fig. 14(a) were to be implemented on-chip, it would add a negligible power penalty to the overall 4.6-mW figure.

A. Measurement of the DCO's FM-INL

To measure the integral nonlinearity (INL) of the DCO's FM characteristic ("FM-INL"), we adopt the flow in Fig. 18(a). All possible combinations of the FM-related OTW's are input to a free-running DCO to measure the frequency differences relative to the corresponding f_0, as in [41]. Such measured frequency difference reflects Δf_M in a realistic FM operation. Meanwhile, the three OTW's are combined into $\mathrm{OTW_M}$, then "restored" to $\Delta\phi_M$ through a reversed data flow relative to Fig. 13(b). Afterward, $\Delta\phi_M$ is converted to the expected Δf_M according to (1). The difference between the measured and expected Δf_M's reflects the FM-INL of the DCO.

Fig. 18(b) shows the measured FM-INL at $f_0 = 3188$ MHz. The "linear" (blue) case restores $\Delta\phi_M$ by assuming that the $\Delta\phi_M$-to-OTW function [in Fig. 18(a)] contains only the first-order term, thereby reflecting the FM-INL of the DCO under the conventional *linear* assumption, as in Fig. 3(a). In reality,

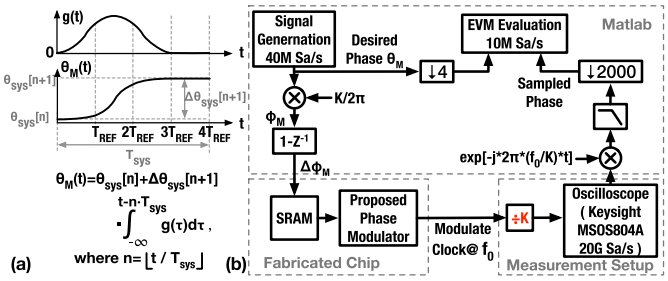


Fig. 19. (a) M-PSK signal generation by interpolating the symbol phases (θ_{sys}) with a frequency pulse-shaping filter [$g(t)$] and (b) setup for measuring the phase modulator's EVM.

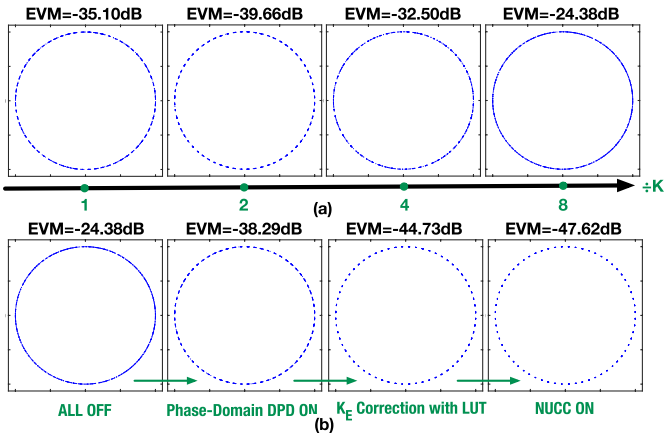


Fig. 20. Constellation diagram of a 60 Mb/s 64-PSK signal measured at $f_0 = 3188$ MHz: (a) Feedforward frequency division K increases from 1 to 8, with all compensation options off (i.e., phase-domain DPD, LUT for OTW_{MCB}, and NUCC) and (b) $K = 8$ and all the compensation options are incrementally turned on.

the INL curve is parabolic, and the maximum frequency deviation can exceed 7 MHz. After including the second-order term in the $\Delta\phi_M$-to-OTW function, which emulates the case of applying the proposed phase-domain DPD, the INL curve (green) becomes a linear staircase. This residue error after the DPD can be attributed to the fact that the resolution ratio between MCB and MFB deviates from the nominal value of 16; it is because this curve contains nine stairs, coincident with the number of MCB codewords. To compensate for this error, we introduce a small correction factor K_E when combining the OTW's [see Fig. 18(a)]. With $K_E = 0.023$, the maximum INL reduces to 0.5 MHz, below 0.26% of the full FM range (i.e., 197 MHz). K_E merely describes the nonlinear behavior, and the associated effect will be addressed by the LUT for OTW_{MCB} when characterizing the PM accuracy.

Fig. 18(c) shows the FM-INL curves at multiple f_0's under the *same* DCO linearization settings, i.e., using the second-order phase-domain DPD and $K_E = 0.023$. From 2708 to 3786 MHz, the frequency error is always below 0.45% of the full range, validating the efficacy of the phase-domain DPD in a wide range of carrier frequencies. The declining trend of the 3948-MHz curve can be attributed to the behavior of the physically realized inductor, whose effective value (defined as the reactance X_L over angular operating frequency $\omega = 2\pi f_0$, i.e., $L_{\text{eff}} = X_L/\omega$) was assumed to be constant in the derivation of the phase-domain DPD, but it actually changes with frequency due to the distributed parasitic capacitance [42].

B. PM Signal Generation and Measurement Setup

Although a GMSK signal is commonly used to evaluate the accuracy of phase modulators, it may fail to reflect the performance across the full PM range because it employs only two possible phase shifts between symbols (i.e., $\pm 0.5\pi$), exercising limited OTW codewords. Therefore, using M-PSK signals is deemed more reasonable. To avoid AM in conventional M-PSK signals [43], we generate the test signal by interpolating the symbols using a frequency pulse-shaping filter from the continuous phase modulation (CPM) [44].

Fig. 19(a) illustrates how the symbol is interpolated in this work. The frequency pulse-shaping filter $g(t)$ lasts four sampling clock (FREF) cycles, equal to one symbol period T_{sys}. The integral of $g(t)$ defines the transition between symbol phases, i.e., θ_{sys}. During the first three T_{REF}'s, $g(t)$ traverses the shape of a raised-cosine filter to smoothen the phase trajectory $\theta_M(t)$. In the last T_{REF}, $g(t) = 0$, thus freezing $\theta_M(t)$ at the associated θ_{sys}. Consequently, the symbols can be simply restored by sampling the transmitted signal during this period.

The measurement setup is shown in Fig. 19(b). The desired phase, i.e., the discrete-time θ_M, is processed to $\Delta\phi_M$, loaded into an on-chip SRAM, and then input to the proposed phase modulator. The modulated output centers at f_0 and is further frequency-divided off-chip by K (programmable from 1 to 8). The division extends the carrier to a lower RF channel frequency emulating a realistic multiband polar TX, and helps to evaluate the effects DCO nonlinearity at large $\text{BW}_{\text{FM}}/f_0$. The divided clock is sampled by a high-speed oscilloscope, then processed in MATLAB to evaluate the EVM.

C. Modulation Performance at 64-PSK

A 64-PSK signal with a data rate of 60 Mb/s is finally adopted to evaluate the PM accuracy. Fig. 20 shows the measured constellation diagram at $f_0 = 3188$ MHz. According to Fig. 20(a), when the feedforward division ratio K increases from 1 to 8 with all compensation options turned off (i.e., phase-domain DPD, LUT for OTW_{MCB}, and NUCC), EVM degrades from -35.1 to -24.4 dB. This is because the large K requires wider BW_{FM} (expanding from 24 to 192 MHz),[3] which boosts $\text{BW}_{\text{FM}}/f_0$ (increasing from 0.75% to 6.02%), and finally intensifies the $1/\sqrt{LC}$-induced DCO nonlinearity.

Fig. 20(b) begins with the worst case ($K = 8$) in Fig. 20(a). After enabling the phase-domain DPD, EVM is improved to -38.3 dB. However, as indicated by the DCO FM-INL curve in Fig. 18(b), the DPD performance is masked by the error in the resolution ratio between MCB and MFB, i.e., K_E in Fig. 18(a). To combat this K_E error, the LUT for OTW_{MCB} [see Fig. 13(b)] is updated by the K_{DCO}-calibration-like algorithm shown in Fig. 14(b), where the compensation gain K_C is equivalent to $16K_E \cdot \widehat{K}_{\text{DCO},M}/\widehat{K}_{\text{DCO},T}$. Then, EVM

[3]Because the frequency pulse-shaping filter smooths out the phase transitions between any two subsequent symbols, $\Delta\phi_M$ of the 64-PSK signal ranges from -0.3 to 0.3. This results in $\text{BW}_{\text{FM}} = 0.6 f_{\text{REF}} = 24$ MHz when $K = 1$. For arbitrary K, $\text{BW}_{\text{FM}} = K \times 24$ MHz.

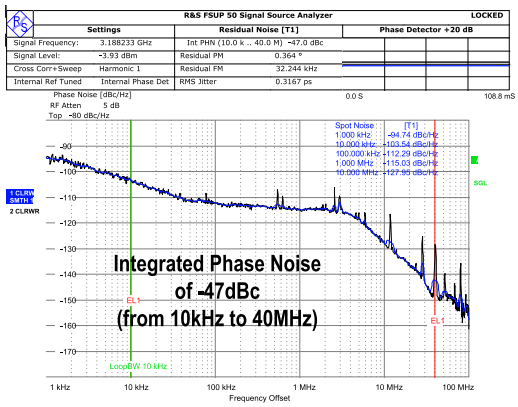


Fig. 21. Measured phase noise at 3188 MHz under the same loop bandwidth setting as the EVM measurements in Fig. 20.

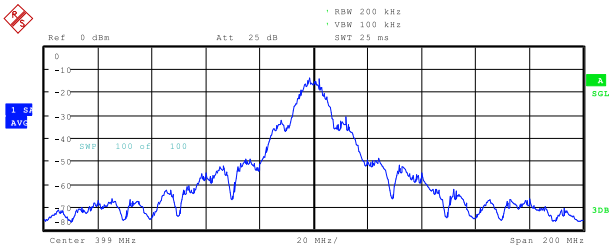


Fig. 22. Measured spectrum of the RF output clock modulated with a 60 Mb/s (10 MSymbol/s) 64-PSK signal at the RF channel frequency of 3188 ÷ 8 MHz.

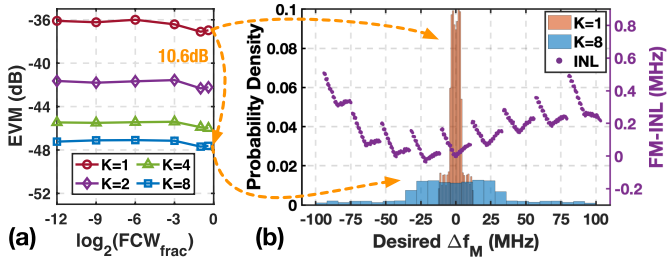


Fig. 23. (a) Measured EVM versus fractional FCW (FCW_{frac}) for different feedforward frequency-division ratios (K) when the integer FCW is fixed at 79 (i.e., f_0 around 3160 MHz) and (b) Δf_M distribution correlated with the DCO's FM-INL.

is improved to −44.7 dB. This suggests that the LC-DCO can be sufficiently linearized by the proposed phase-domain DPD with a proper K_{DCO} estimation. On top of that, enabling the NUCC further improves EVM by 2.9 to −47.6 dB. The final EVM is limited by the unexpected DCO nonlinearity [see the FM-INL in Fig. 18(c)]. The difference in EVM before and after applying NUCC suggests that NUCC removes a PM error around −47.9 dB, agreeing with the simulation result (see the "NUCC off" curve in Fig. 12) at a large PLL bandwidth (around 3 MHz according to the phase noise profile in Fig. 21). In addition, the output spectrum of this case is shown in Fig. 22.

Fig. 23(a) shows the measured EVM versus the fractional FCW (FCW_{frac}) at different forward frequency division ratios (K) when the integer FCW and all compensation options remain the same as in the final state of Fig. 20(b). Under the constant K, EVM varies within 1 dB across FCW_{frac}.[4] With K increasing from 1 to 8, EVM shows a 10.6 dB improvement, similar to the trend of quantization noise that decreases with $-20\log_{10} K$. However, the EVM is actually dominated by the DCO nonlinearity according to the EVM breakdown for the rightmost case on the $K = 1$ curve: The contribution due to the DCO's finite resolution is −43 dB. This is because the TB's frequency resolution $\Delta f_{\text{res}} = 156$ kHz and update interval $T_{\text{REF}} = 25$ ns result in phase resolution of $\theta_{\text{res}} = 2\pi \cdot \Delta f_{\text{res}} \cdot T_{\text{REF}}$, which adds to the modulated phase as a quantization noise with the power of $\theta_{\text{res}}^2/12$, given that the noise transfer function of the low-speed first-order $\Delta\Sigma$ modulator in Fig. 13(b), i.e., $N(z) = 1 - z^{-1}$ [45], cancels out the accumulation characteristic of DCO, i.e., $1/(1 - z^{-1})$ in the transfer function (see Fig. 9). Additionally, the integrated phase noise (IPN) of the unmodulated carrier degrades the EVM by −44 dB, which is 3 dB higher than the double-sided IPN of −47 dBc shown in Fig. 21, since the modulated signal spreads over both positive and negative offset frequencies. The combined EVM contribution from these two sources is −40.5 dB, which is 3.5 dB lower than the measured EVM of −37 dB. The DCO nonlinearity appears the only candidate to explain this gap.

To further explore why the DCO nonlinearity affects EVM in a similar trend as does the quantization noise, Fig. 23(b) provides the Δf_M distribution together with the DCO's FM-INL curve, on which the 9 discrete segments correlate with the 9 MCB codewords, and the V-shape of each segment arises from the mismatch between the MFB units. When $K = 1$, the exercised Δf_M range almost overlaps with the central V-shape segment, so only the FM-INL related to MFB degrades the EVM. However, when K increases to 8, the INL grows 2.5×, i.e., from 0.2 to 0.5 MHz. Considering that the operational Δf_M range is also multiplied by 8, the INL relative to the exercised range shrinks by 0.31, agreeing with the 10 dB improvement in EVM. Therefore, the high EVM at small K is mainly attributed to the MFB exhibiting unexpectedly strong nonlinearity, which is even higher than that due to MCB considering the frequency-tuning range. To further improve the EVM, additional measures are needed to combat the MFB-related INL, e.g., an additional LUT for OTW_{MFB} or the dynamic element matching (DEM) in [46].

Fig. 24 shows the measured EVM versus the DCO carrier frequency f_0 at different forward frequency division ratios K. EVM basically decreases at low f_0 and large K cases because they exercise a wider portion of the DCO's frequency-tuning range to dilute the effect of MFB's nonlinearity. To demonstrate that the combinational DPD addressing the

[4]In the realized phase modulator, the FREF signal couples to and periodically disturbs the DCO. The disturbance strength depends on the instantaneous phase difference between the FREF and DCO clocks, thus fluctuating at the frequency of $\text{FCW}_{\text{frac}} \cdot f_{\text{REF}}$. At lower FCW_{frac}, the disturbance experiences less filtering by the DCO (described by the DCO's phase-domain transfer function, i.e., $1/s$). The unfiltered disturbance not only directly degrades EVM by increasing the PM error, but also results in a larger detected phase error $\Delta\phi_E$. A large $\Delta\phi_E$ can saturate the TDC (detecting time errors ranging from −3.5 to 3.5 ps), and slow down the PLL's transient response. Therefore, PM errors stay uncorrected for a longer time, thereby further degrading the EVM. This is a possible explanation as to why the EVM increases at very small FCW_{frac}.

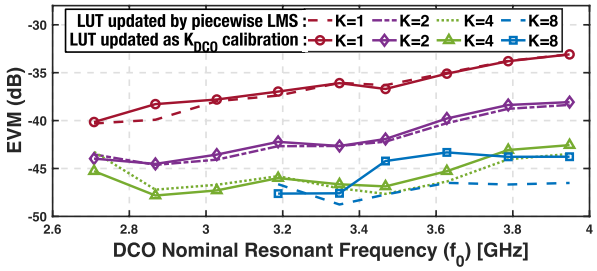


Fig. 24. Measured EVM versus the DCO carrier frequency (f_0) at different forward frequency division ratios (K). The corresponding $\mathrm{BW_{FM}}$ scales with K, i.e., $\mathrm{BW_{FM}} = K \times 24$ MHz.

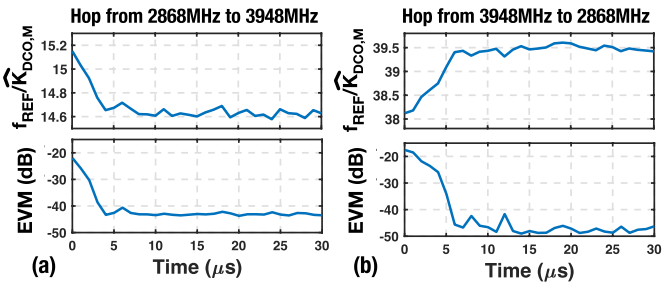


Fig. 25. Measured transient trajectories of the calibration coefficients and EVM. Modulation and calibration are turned on at $t = 0$ after PLL gets locked to the target frequency f_0. Results are measured at $K = 4$, when f_0 hops (a) from 2868 to 3948 MHz and (b) vice versa.

TABLE I
COMPARISON WITH STATE-OF-THE-ART PLL-BASED PHASE MODULATORS

	This Work	JSSC' 12 [15]	JSSC'16 [12]	SSCL' 20 [11]	RFIC'20 [47]	TMTT'18 [17]	JSSC'19 [7]
Modulation Type	**64-PSK**	QPSK	GMSK	32-PSK	GFSK	64QAM	1024QAM
DCO Carrier Freq. (f_0) Range (GHz)	**2.7-3.9**	2.9-4.0	10.1-12.4	13.0-14.5	1.6-1.94	2.8-7.6	9.9-12.1
Measured f_0 (GHz) / Freq. Division K	**3.188 / 8**	3.6 / 1	10.24 / 1	13.75 / 1	1.81 / 2	5.14 / 2	11 / 2
Integrated RMS Jitter (fs)	**317**	503	180	95.2	NA	1091	168
Data Rate (Mbit/s)	**60**	20	10	250	1	201.6	25
Ref. Freq. (MHz)	**40**	40	40	200	60	26	40
$\mathrm{BW_{FM}}$ (MHz)	**192**	40	2.5	200	0.5	416	≤80
$\mathrm{BW_{FM}}$ / f_0 (%)*	**6.02**	1.11	0.024	1.45	0.028	8.09	≤0.73
EVM @ f_0 / K (dB)	**-47.6**	-36	-37.4	-42.2	-30.9	-28.7	-41.3
IPN** @ f_0 /K (dBc)	**-65**	-42	-41.7	-44.7	N/A	-38.1	-47.6
$\mathrm{EVM_{rescale}}$*** (dB)	**-47.6**	-55.1	-65.6	-73	-38	-44.9	-64.1
EVM excl. IPN @ f_0 / K (dB)	**-47.8**	-39	-43.3	N/A	N/A	-29.8	-44
Power (mW)	**4.6**	5	8.1	31.5	5.3	40.7****	17.7****
Energy/Bit (nJ/bit)	**0.08**	0.25	0.81	0.13	5.3	0.2****	0.71****
Active Area (mm^2)	**0.31**	0.5	0.25	0.7	0.3831	2.12****	1.31
CMOS Process (nm)	**40**	65	28	28	65	28	28

* Unchanged if the DCO directly operates at f_0/K
**Only integrated over postive or negative frequencies
*** Rescaled to 398.5MHz
**** Including only the phase modulator part

DCO-nonlinearity, i.e., the DPD simultaneously applied in both phase and OTW domains, can achieve the frequency-insensitive performance, the EVM is measured in two scenarios. In the first case (solid lines in Fig. 24), the compensation settings (i.e., phase-domain DPD, the $\mathrm{OTW_{MCB}}$ LUT, and NUCC) are kept the same as in the final state in Fig. 20(b) irrespective of f_0. In the second scenario (the dashed lines), the $\mathrm{OTW_{MCB}}$ LUT is updated at each frequency point with the piecewise calibration shown in Fig. 14(a) to represent the optimum EVM of this design. At most points, the solid lines coincide with the dashed ones. In the case of $K = 4$ and $K = 8$, EVM on the solid lines remains below -43 dB across the full tuning range of f_0. This validates the frequency-insensitive performance of a combinational DPD solution.

One may notice a greater deviation between the solid and dashed lines at relatively high frequencies ($f_0 > 3.4$ GHz) and $K = 8$. This is because the DCO exhibits a larger FM-INL [after compensated by a *fixed* gain factor, K_C, shown in Fig. 14(b)] at higher resonant frequencies and across wider exercised Δf_M ranges (i.e., $\mathrm{BW_{FM}}$ which scales with K) according to Fig. 18(c).

Due to its relatively frequency-insensitive performance, the combinational DPD can reduce the efforts required in the DCO nonlinearity calibration and shorten the time to reach optimum EVM after each channel-frequency hop. To prove this, we hopped the PLL's center frequency f_0 between 2868 and 3948 MHz, then measured [recorded by the debugging SRAM in Fig. 13(b)] the settling curves of $f_{\mathrm{REF}}/\widehat{K}_{\mathrm{DCO},M}$ (the only parameter that will likely require a re-calibration according to Section V-D), as shown in Fig. 25.

At each new frequency, $f_{\mathrm{REF}}/\widehat{K}_{\mathrm{DCO},M}$ starts with an initial value that is calculated from the final value of the previous frequency using (26), and then settles within 15 us. Regarding the remaining PM-related parameters, $\widehat{NT}_{\mathrm{cnst}}$ values were calculated as per (25); $\widehat{K}_{\mathrm{DCO},M}/\widehat{K}_{\mathrm{DCO},T}$ and the LUT content are frequency-independent, thus staying unchanged. These parameters are not shown in Fig. 25 because they are temporally frozen during the $f_{\mathrm{REF}}/\widehat{K}_{\mathrm{DCO},M}$ settling to avoid any mutual influence with the unsettled $f_{\mathrm{REF}}/\widehat{K}_{\mathrm{DCO},M}$, thereby accelerating the calibration. The measured transient $f_{\mathrm{REF}}/\widehat{K}_{\mathrm{DCO},M}$ was also written back to the phase modulator to measure the corresponding EVM in the $K = 4$ case (where the calibration process also used the same PM sequence in accordance with $K = 4$). As shown in Fig. 25, EVM settles to the optimum value within 15 us. This time is much shorter than the 100 ms needed by the phase modulator to calibrate the DCO's nonlinearity with the piecewise LMS algorithm [7]. One might argue that this comparison is unfair since the aforementioned 100 ms is the calibration time during an initialization, which can be shorter if optimized for channel hopping. However, the assumed shorter calibration time after channel hopping is not true for the piecewise LMS since the calibration results of the piecewise LMS are not only related to the DCO nonlinearity but also to the estimated K_{DCO}'s [12]. After the DCO hops to the frequency associated with a faraway channel, K_{DCO}'s will change significantly. Consequently, the piecewise LMS will need to correct rather huge errors, and so the corresponding calibration time will not considerably differ from that in the original initialization.

D. Performance Comparison

Table I compares this work with state-of-the-art PLL-based phase modulators. While running the DCO at 3188 MHz, this design produces a transmitted RF carrier at 398.5 MHz after

the division by $K = 8$. When generating the 64-PSK signal, the DCO exercises an FM bandwidth (BW_{FM}) of 192 MHz, corresponding to 6.02% fractional BW_{FM} ($\text{BW}_{\text{FM}}/f_0$); hence it results in a large FM error due to the $1/\sqrt{LC}$-induced DCO nonlinearity. Despite this, the proposed phase modulator achieves the lowest EVM and energy per bit, i.e., −47.6 dB and 0.08 nJ/bit, respectively.

It should be noted that the issue of comparing EVMs across designs is still an open question in the literature. Cherniak et al. [11] have chosen to normalize the EVMs to the same output frequency. This is equivalent to measuring the EVM after virtually dividing[5] the PM clock by $K_{\text{rescale}} = f_{\text{reported}}/f_{\text{chosen}}$, where f_{reported} is the original output frequency reported in a given reference paper, and f_{chosen} is our chosen target output frequency for re-scaling (here equal to 398.5 MHz). Under an expedient assumption that the PM error is dominated by random jitter (i.e., thermal phase noise), the rescaled EVM in dB, i.e., $\text{EVM}_{\text{rescale}}$, equals the original EVM minus $20\log_{10}(K_{\text{rescale}})$ because the divided carrier period becomes K_{rescale} times larger, but the random jitter remains the same. Table I also lists the calculated $\text{EVM}_{\text{rescale}}$ values of each work.

However, the above $-20\log_{10}(K_{\text{rescale}})$ scaling assumption does not hold under a realistic scenario of a wideband TX when distortion dominates the PM error because the distortion increases with K_{rescale}. This can be understood by inspecting the distortion induced by the error in the modulation frequency (Δf_M): According to Section IV-A, the *relative* Δf_M error due to the $1/\sqrt{LC}$ nonlinearity is roughly reflected by $\text{BW}_{\text{FM}}/f_0$. If the original PM clock at f_0 was to be (virtually) frequency-divided by K_{rescale} (for the EVM rescaling), BW_{FM} should multiply by K_{rescale} to keep the PM characteristics (e.g., data rate and constellation) unchanged after the division. Hence, a larger K_{rescale} increases $\text{BW}_{\text{FM}}/f_0$, indicating stronger *relative* Δf_M error and higher EVM contribution. This is verified by Fig. 20(a), contradicting with the EVM-rescaling trend indicated by the jitter-dominant assumption. Although linearizing the DCO can suppress the Δf_M error, the residue increases dramatically with $\text{BW}_{\text{FM}}/f_0$ due to the high-order nonlinearities indicated in (18).[6] This will ultimately dominate the EVM.

Considering that the EVM contributions due to jitter and distortion change differently in the frequency rescaling, we prefer to separately compare these two contributors, rather than merely considering the overall EVM. In Table I, the former one is already covered by the integrated rms jitter, and the latter is reflected by the EVM *excluding* IPN (integrated phase noise) at their original output frequencies. The "EVM excl. IPN" is calculated by the following equation:

$$\text{EVM excl. IPN} = 10\log_{10}\left(10^{\frac{\text{EVM(dB)}}{10}} - 10^{\frac{\text{IPN(dB)}+3}{10}}\right) \quad (28)$$

where 3 dB is added to IPN because it integrates phase noise over positive or negative offset frequencies and counts merely half of the EVM contribution. The proposed phase modulator exhibits the lowest distortion level compared with other works.

[5]In general, a multiplication is also possible but, for the sake of simplicity, here we only describe a division.

[6]$\text{BW}_{\text{FM}}/f_0$ correlates with $\Delta\phi_M$/FCW in (18) because the former represents the maximum $\Delta f_M/f_0$, and the latter equals $\Delta f_M/f_0$ according to (1) and (6).

VII. Conclusion

This article has demonstrated a digital PLL-based phase modulator of high accuracy yet low power consumption. Although the DCO updates at a non-uniform clock and suffers from strong nonlinearity due to the wide FM bandwidth, the phase modulator can still achieve EVM below −47 dB at a 60-Mbit/s 64-PSK signal. This benefits from the two proposed innovations: 1) the NUCC that addresses PLL disturbances arising from the time-varying period and offset of the updating clock and 2) the phase-domain DPD that compensates the $1/\sqrt{LC}$-induced DCO nonlinearity. From the methodology perspective, the NUCC analysis entails the improved PM model in the hybrid-time domain. The new model is effective in analyzing the time-related distortions in general PLL-based phase modulators. Moreover, combining the proposed phase-domain predistortion with the conventional OTW-domain counterpart could constitute a frequency-insensitive solution compensating for DCO nonlinearity. These two powerful tools would benefit low-power PLL-based phase modulators in improving accuracy, thereby paving the way for future polar TXs supporting high-data-rate applications.

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