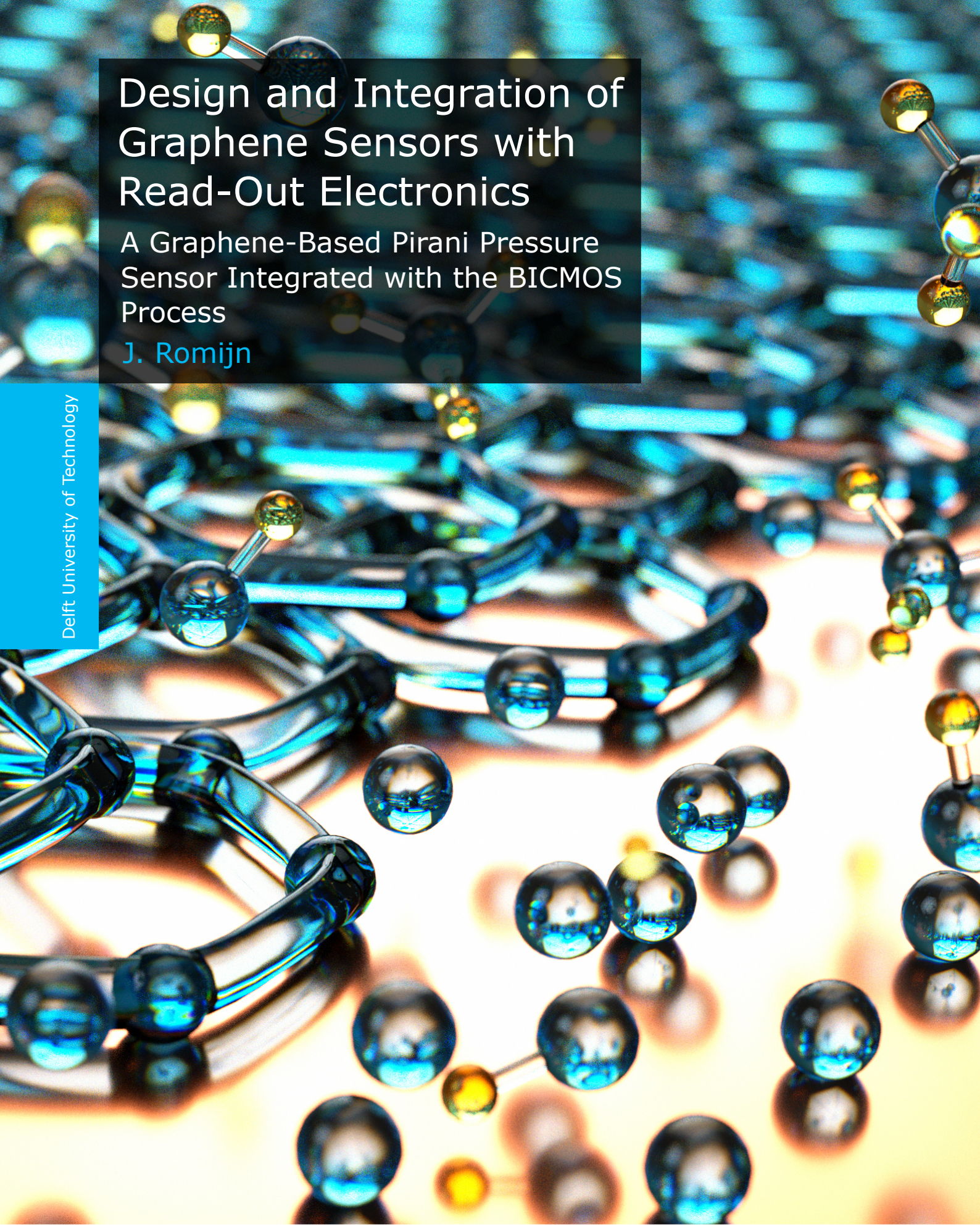

Design and Integration of Graphene Sensors with Read-Out Electronics

A Graphene-Based Pirani Pressure Sensor Integrated with the BICMOS Process

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TU Delft Delft University of Technology

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Design and Integration of Graphene Sensors with Read-Out Electronics

A Graphene-Based Pirani Pressure Sensor Integrated with the BICMOS Process

by

Joost Romijn

in partial fulfillment of the requirements for the degree of

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Abstract

In this research work, efforts have been made to successfully integrate graphene in a standard CMOS fabrication process without the need for wafer-to-wafer transferring. For this purpose, a graphene-based Pirani sensor is integrated in the BICMOS process. Two batches of graphene-based Pirani sensors are characterized, resulting in world's first operating graphene-based Pirani pressures sensors. The maximum measured resistance change is $2.8\ \%$ which is comparable to current state-of-the-art implementations using other materials. The graphene-based implementation allowed for miniaturization of the devices with low power consumption design possibilities.

The BICMOS technology used at EKL at the Delft University of Technology is characterized and effects of graphene growth are investigated. This led to an electrical read-out design in CMOS technology of which the digital circuits performed as designed. Operational digital logic gates were measured alongside grafeen, but with a reduced yield. The analog circuits proved to be challenging in the BICMOS technology and did therefore not operate as intended. From this it is concluded that it is indeed possible to integrate grafeen with a CMOS process.

Future research work that focuses on the details of the fabrication process flow should result in higher fabrication yields and better reproducibility. Additional measurements on the grafeen structures will help to characterize the graphene-based Pirani better and allow for attempts to fit an analytical model to the measurement data.

Preface

This thesis is part of the Master graduation project that is conducted in partial fulfillment of the requirements for the degree of Master of Science in Electrical Engineering. The project is conducted over a period of fifteen months. During this project, a graphene-based Pirani pressure sensor is integrated in the BICMOS process of the TU Delft to demonstrate that graphene is compatible with standard CMOS processing.

In the first stage of this project, the focus lay on characterization of the Pirani pressure sensor. Earlier attempts of fabricating such a device were already contucted by Sten and Robin. I observed how the most recent batch was fabricated by Sten at Kavli, which I could then start to characterize in a controlled pressure measurement setup. This setup was build by Robin, who then showed me how to use it. The results were good and the first working devices were a fact. A second batch was made and characterized after that to acquire more data. Not all parameters of the existing analytical model for Pirani pressure sensors in literature could be determined beforehand. Therefore, the electrical read-out design was based purely on the measurement results.

The second stage involved clean room training and characterization of the CMOS devices before and after a graphene growth process. The training was given mainly by Sten and discussions on the characterization were often with Henk van Zeijl. The graphene growth step effects on the CMOS devices are clear, but the causes are left open to discussion as this would involve too much time to fully investigate.

During the third stage of the project, the electrical design of the read-out electronics was performed. This involved both analog and digital design in Cadence Virtuoso. Instructions on the software and discussions on the design with Ronaldo Martins da Ponte were very valuable. After extensive simulations, the layout was made also in Cadence. This layout was exported to L-Edit, were the final layers involving the graphene-based Pirani pressure sensor were created. In total three masks with each four images were ordered and used in the fabrication process.

In the fourth stage the fabrication process was performed, which involved many trial and error steps in the process to achieve the desired result. The preservation of the graphene and molybdenum until the final process steps, proved to be the largest challenge in fabrication. Many discussions with Sten on the results eventually led to the working process that is presented.

The final stage of this project was the characterization and verification of the fabricated devices. Simple circuit measurements could be performed in a probe station. The larger circuits were measured in a wire bonded package on a bread board. The measurement equipment in the Tellegen Hall at EEMCS was used for these electrical measurements. Finally, the pressure controlled measurement setup build by Robin was used to perform pressure dependency measurements. The result is a successful integration of a graphene-based Pirani pressure sensor with CMOS electronics, even though not all designed read-out electronics are operational.

The thesis committee consists of professor Lina Sarro, the head of the ECTM laboratory, my daily supervisor Sten Vollebregt, highly involved PhD candidate Robin Dolleman at Quantum Nanoscience at Applied Sciences and professor Peter Steeneken at PME at Mechanical Engineering.

Joost Romijn
Delft, February 2018

Acknowledgments

There were many people involved in this project and together we achieved the successes presented in this thesis work. First of all, I thank my daily supervisor Sten. His enthusiasm, creativity and commitment inspired me to strive for the best results in each stage. He is always prepared to discuss problems or provide help. Secondly, I thank Robin for his work and help regarding the pressure dependency measurements and Pirani pressure sensor characterization. I thank Henk for discussions and help on fabrication in the clean room, Ronaldo for discussions on measurements results and help in designing, Manju for help on MEDICI and TSUPREM simulations, Zahra for providing a starting point in my design and Laurens for his work on a visualization program for wafermaps. Furthermore, I thank all people involved at the clean room for their help and hard work and my office mates Levar, Thijs, Ziqiao and the other master students for their support and cheerful company. I thank all people who took the time to read the draft versions of this thesis and provided critical feedback to improve it. Finally, I thank my parents for their support, patience and understanding throughout my entire studies.

Contents

1

Introduction

Nowadays, many regular kinds of electronics are upgraded to a smart variant of that particular electronic device, which results in smart homes, smart phones, smart sensors, smart cars, etc. This 'More than Moore' trend requires an increased functionality of the existing electronic designs. For this purpose, integrated sensors with improved sensitivity, lower power consumption and smaller footprint are required. This is achieved by introducing new materials with favorable properties for sensing applications. The integration of these new materials in standard CMOS processes, allows for sensor signal read-out and conditioning on chip in favor of the smart sensors.

For successful integration of new materials in the CMOS process it is important that the yield is high and that they can be patterned by lithography. So far the integration of graphene with CMOS electronics is only achieved by wafer-to-wafer transferring. Such transfer steps induce wrinkles and defects in the transferred material, which impacts the yield and reproducibility. Furthermore, the alignment is not guaranteed and therefore no small structures are transferred, which poses difficulties during the patterning after transfer. Successful integration therefore demands that the new material and the CMOS devices are fabricated without a wafer-to-wafer transfer step.

A novel material with promising properties for sensor applications is graphene. Graphene is a two dimensional sheet of carbon atoms that has a thickness of a single atom and is ordered in a hexagonal structure, as illustrated in Figure 1.1. Several layers of graphene on top of each other is called multi-layer graphene, while the single layer is often called mono-layer graphene. It was first created using scotch-tape exfoliation from a graphite crystal for which the discoverers received the Nobel prize in 2010 in Physics [1]. Graphene has several remarkable properties such as high area to thickness ratio, high elasticity, high mechanical strength, high carrier mobility and high thermal conductivity [2–4]. There are no other known materials that possess these properties, which is why graphene is called the first super material.

These properties make graphene a promising material for applications involving flexible, transparent and conductive thin films [5] and high frequency transistors exceeding state-of-the art silicon transistors performance [6]. Recent developments in synthesis of large area mono-layer graphene films has enabled studies of various potential sensor types based on graphene [7, 8]. This includes chemical, electrochemical, photoelectric, electric field, magnetic field and mechanical sensors [9, 10].

However, so far this material has not yet been integrated without wafer-to-wafer transfer with CMOS electronics, which renders its full potential unused in the trend towards a world with smarter devices. To open possibilities for integrated graphene sensors in smart devices in the future, the challenge of integration without wafer-to-wafer transfer in a standard electronics fabrication process has to be overcome. This is the main driving force behind this thesis research work. This work aims on introducing world's first integration of graphene with CMOS electronics, without a wafer-to-wafer transfer step. This opens the door to graphene-based sensors integration with read-out electronics with a high yield and satisfies the 'More than Moore' trend in pursuit of a world with smarter devices.

This research work is considered successful when working CMOS circuits as well as an operating graphene-based structure are implemented alongside each other without a transfer step. The success is arguably already achieved if single CMOS devices are found to be operating, but working circuits demonstrate that the process allows for designing circuits as well. The best expected result is an integration in which the graphene-based structure is connected to CMOS electronics successfully.

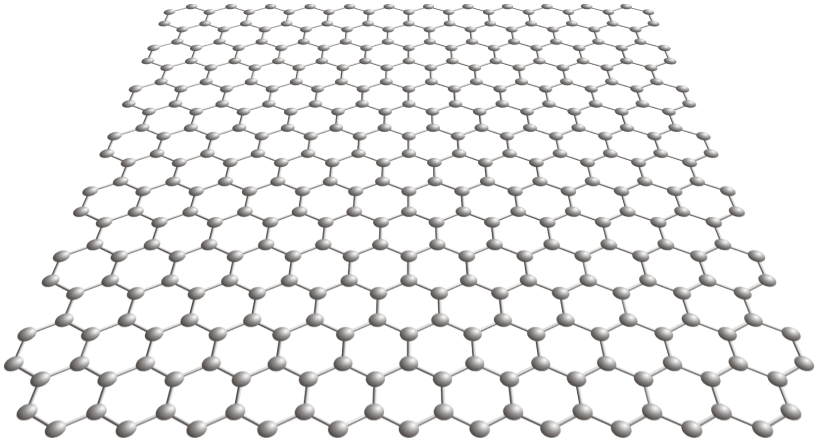


Figure 1.1: Illustration of a mono-layer graphene film [11].

1.1. Problem Formulation

The potential of graphene as a material for various applications is not incorporated in electronics, as no fabrication process without wafer-to-wafer transfer currently exists. It is therefore of great value to investigate the feasibility of such a process with the current technology to allow for further advances in the trend of smart devices that require improved integrated sensors. In this research it is important to asses the implications on the already existing fabrication process of single graphene devices and standard electronics. As a result, the central research question that drives this research work is:

"Can graphene synthesis be integrated in a standard CMOS process, without wafer-to-wafer transfer?"

Additionally, the research project is given a more concrete goal by defining the application in which graphene is to be incorporated. This is done by choosing a graphene-based sensor on which promising efforts were already made by Sten Vollebregt and Robin Dolleman, which is the Pirani pressure sensor. The architecture, properties and advantages of a graphene-based variant of this sensor are discussed in the background theory in Section 2.1.1. However, a graphene-based Pirani pressure sensor has not been reported yet. It is therefore required to first investigate the feasibility and advantages of such a device. The additional research question is:

"Can a Pirani pressure sensor be based on graphene and what are the advantages?"

Although the main research question can also be answered by implementing a graphene device and some generic electronics on the same die without wafer-to-wafer transfer that are not connected, the ultimate application is a fully interconnected design. To integrate the graphene-based Pirani pressure sensor with standard electronics, read-out electronics are to be designed that interface with the sensor. These read-out electronics consist of a graphene-based sensor topology, signal amplifier and analog-to-digital converter. No specific requirements for the read-out electronics such as amplifier gain or analog-to-digital converter resolution are given, as it is pure proof of principle.

1.2. Proposed Solution

The additional research question is to be answered first. For the implementation of the graphene-based Pirani pressure sensor, the fabrication method that results from the efforts made by Sten Vollebregt and Robin Dolleman is used as a starting point. This fabrication method is described in detail in the background theory in Section 2.1. This method does not require wafer-to-wafer transfer, which is a requirement for the main research question. If a graphene-based Pirani pressure sensor is fabricated successfully, it is to be characterized to provide a starting point for the design. Therefore, it is investigated which sensor dimensions produce good results and the device is characterized electrically.

After successful results in the implementation of the graphene-based sensor, attempts can be made to integrate it in the standard electronics fabrication process developed at the Else Kooi Laboratory to answer the main research question. Since the implementation of graphene used in the graphene-based Pirani sensor is at high temperature, most metals used conventionally for the device interconnect material will melt during that process step. The

graphene implementation is therefore performed before the metal interconnect implementation. Furthermore, the graphene implementation is performed in a potentially copper contaminated environment, which poses restrictions on allowed processes after that step. It is therefore desired to postpone the graphene implementation towards the end of the fabrication process. The graphene implementation process is therefore integrated with the standard electronics fabrication process by placing the required steps between the front-end and back-end of line (BEOL) of the fabrication process.

1.3. Research Goals

To achieve the proposed solutions, several research goals are formulated and listed below. Each individual research goal is equally important in answering the research question. Therefore, each research goal is defined as a research stage and has its own chapter in this thesis. Prior to the chapters that each house a research goal, the required background theory is given in Chapter 2. The thesis is concluded and recommendations for future work are given in Chapter 8. The Appendix lists additional figures and measurement results as well as a list of used acronyms. The listed probe station measurement results could be visualized in colorful wafermaps due to the results of a case study by Laurens van Dam.

1. **Implementation and characterization of the graphene-based Pirani sensor**
   In this stage the implementation of the graphene-based Pirani sensor is investigated and characterized. The results are given in Chapter 3.
2. **Characterization of the standard electronics and the effect of the graphene implementation at high temperature**
   During this stage clean room training is followed during which the standard electronics are fabricated and characterized. This is followed by a run that incorporates the graphene growth step to investigate the effects on the devices. The results are discussed in Chapter 4.
3. **Electrical design of the read-out electronics and mask design of the complete design**
   The read-out electronics are designed and simulated during this stage accordingly to measurement results obtained in the previous stages. The layout is then designed and completed by adding the graphene-based sensor layers. The results are elaborated in Chapter 5.
4. **Defining the details of a suitable integrated fabrication process**
   In this stage the fabrication of the design is performed. To find a suitable fabrication process, different approaches are investigated to find the most suitable solution. The results are given in Chapter 6.
5. **Characterization and verification of the fabricated devices**
   In this final stage measurements are performed to test the success of integrating the graphene-based sensor in the standard electronics fabrication process. The results are discussed in Chapter 7.

2

Background Theory

This chapter addresses the research topics with corresponding studies that are relevant to this research. The theory, architecture, fabrication and analytical model of the Pirani pressure sensor is discussed in Section 2.1. The graphene synthesis and characterization are then discussed in Section 2.2. This is followed by the description of the BICMOS process and a model for the device threshold voltage. Finally, the chapter is concluded by a short summary of the findings.

2.1. Pirani Pressure Sensor

Pirani pressure sensors are an attractive and often used sensor due to their simplicity and robustness as no hermetic cavity, moving parts or accurate deflection measurement methods are required. However, current Pirani implementations are bulky and not suitable for low power applications. Typical dimensions are $100\ \mu$m x $200\ \mu$m or larger, with power consumption of 1 mW or more and operating range of 10^{-3} mbar to 10^{3} mbar [12–15]. An implementation with much smaller footprint, lower power consumption and higher operating range has been achieved by using CNTs, but the reported fabrication process gives unpredictable results and low yield [16].

2.1.1. Theory and Architecture of the Pirani Pressure Sensor

The Pirani pressure sensor is based on the principles of resistive heating and heat conduction. The standard Pirani sensor architecture is illustrated in Figure 2.1 where an electrically conductive bridge is implemented over a cavity in the wafer substrate. Alternative Pirani architectures exist such as a buried architecture [15]. The device is placed in a gas mixture and an electrical current is forced through the bridge. The forced current generates heat in the bridge, which is partially absorbed by colliding particles in the gas mixture. The final increase of the bridge temperature is therefore dependent on the composition and pressure of the gas mixture. The electrical resistance of the bridge material changes as a result of the temperature increase. This resistance is therefore also dependent on the gas mixture composition and pressure. The boundary conditions for this principle to work, are discussed next.

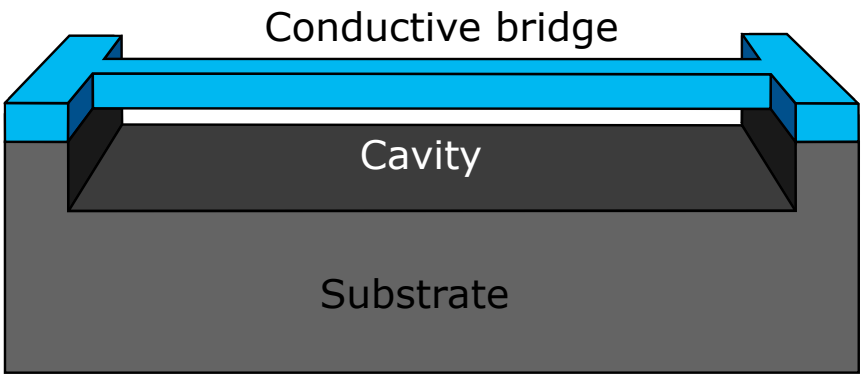


Figure 2.1: Pirani pressure sensor architecture [15] with the conductive bridge marked in blue over a cavity in the substrate.

The first boundary condition affects the used substrate material. For the Pirani sensor to operate effectively, the substrate should not conduct a significant amount of electrical current compared to the bridge. Secondly, the gas mixture composition and pressure need to be in a specific range for the principle of heat conduction to be dominant. This specific range is related to Knudsen's number. The relation between Knudsen's number and the heat transfer is depicted in Figure 2.2. There are three different types of heat transfer, each of which is dominant in a specific range of Knudsen's number. These heat transfer types are radiation, conduction and convection and are marked in the graph. The boundary condition for the Pirani sensor requires that the heat transfer is dominated by conduction as in that case the gas composition and pressure influence the cooling. This desired range is marked with blue in the graph. The corresponding range of Knudsen's number is roughly 0.01 to 1. These limits are later used in combination with the value of the cavity depth to find the pressure range.

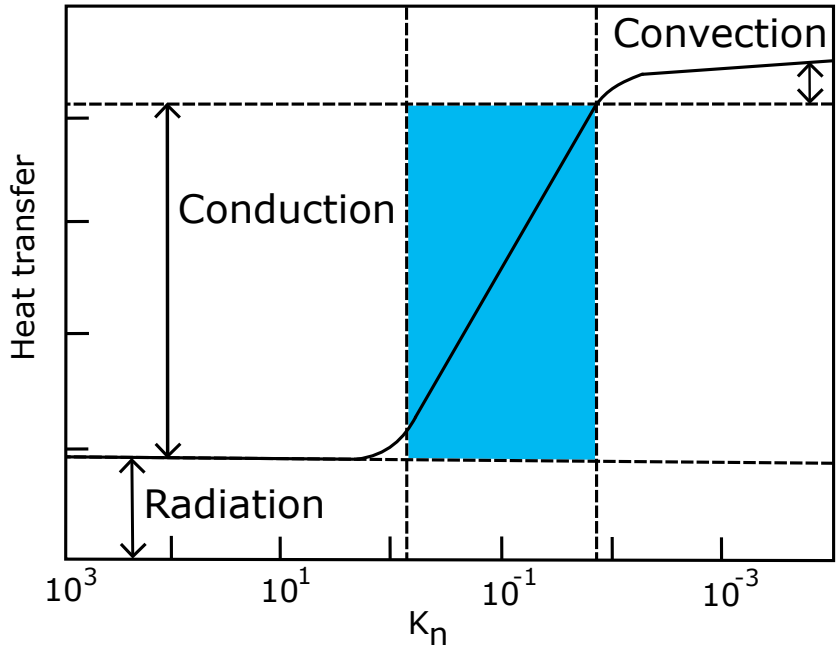


Figure 2.2: Relation between the heat transfer and Knudsen's number. The three heat transfer types are indicated and the desired heat transfer range for the Pirani sensor is marked in blue [17].

Knudsen's number K_n is calculated by Equation 2.1 where λ is the average free molecular path of the gas surrounding the bridge and g the characteristic length of the device, which is equal to the cavity depth of the Pirani sensor. Note that Knudsen's number is dimensionless.

$$K_n = \frac{\lambda}{g} \tag{2.1}$$

The average free path is calculated by Equation 2.2 where d_0 is the average molecular diameter and n the density in atoms per volume of the gas mixture surrounding the conductive bridge [17]. In this research, the gas mixture is regular air, which has an average molecular diameter of $9.7 \cdot 10^{-10}$ m [18].

$$\lambda = \frac{1}{\sqrt{2}\pi d_0^2 n} \tag{2.2}$$

The pressure is calculated by Equation 2.3, which gives the ideal gas law. Here, T is the gas temperature, ρ the density in mass per volume and R_d the gas constant for dry air which is 287 J·kg^{-1}·K^{-1} [19].

$$P = \rho R_d T \tag{2.3}$$

Finally, the two densities n and ρ are related by Equation 2.4 where M_d is the molar mass of dry air and N_A the Avogadro constant, which equal $2.896 \cdot 10^{-2}$ kg·mole^{-1} [20] and $6.022 \cdot 10^{23}$ mole^{-1} respectively.

$$\rho = n\frac{M_d}{N_A} \tag{2.4}$$

Equations 2.1-2.4 are combined and solved in Equation 2.5 for the pressure in terms of the cavity depth, as this is the only undetermined parameter left. The operational pressure range is found by filling in the limits of Knudsen's number. The result dictates that the operational pressure range scales inversely proportional with respect to the cavity depth and no other geometry parameters have any influence on the pressure range.

$$P = \frac{R_d M_d T}{\sqrt{2}\pi d_0^2 N_A K_n} \frac{1}{g} \tag{2.5}$$

Equation 2.5 is now used to obtain the pressure range corresponding to the found Knudsen's number range for different values for the cavity depth. The investigated cavity depth values are $100\ \mu$m, $10\ \mu$m, $1\ \mu$m and $0.1\ \mu$m, which are considered typical values. The result is depicted in Figure 2.3. The pressure range clearly scales inversely proportional with respect to the cavity depth. Atmospheric pressure is at approximately 10^3 mbar, which implies that the pressure range results are generally for low pressures. The exception is a cavity depth of $0.1\ \mu$m, which results in a pressure range of 10^2 mbar to 10^4 mbar.

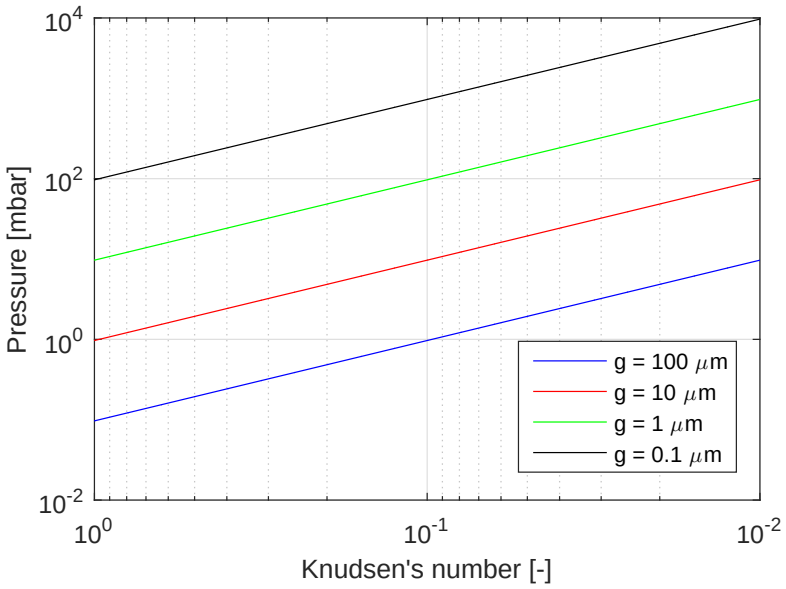


Figure 2.3: Pressure ranges of Pirani sensors with four different values for the cavity depth in the found Knudsen' number range.

2.1.2. Analytical Model of a Pirani Pressure Sensor

A widely used and confirmed analytical model of the Pirani pressure sensor is presented below [15, 21]. The Pirani sensor geometry parameters bridge length L, thickness t and width w and the cavity depth g are depicted in Figure 2.4, which depicts the top and side view of the Pirani sensor architecture of Figure 2.1.

The conductive bridge pressure dependent resistance $R(p)$ is calculated by Equation 2.6 where $R_\square$ is the sheet resistance of the bridge material measured at room temperature and ambient pressure, ξ the temperature coefficient of resistance (TCR) of the bridge material and $\bar{u}(p)$ the pressure dependent average temperature rise of the conductive bridge as a result of resistive heating caused by an electric current.

$$R(p) = R_\square \frac{L}{w}(1 + \xi \bar{u}(p)) \tag{2.6}$$

The pressure dependent average temperature rise of the conductive bridge $\bar{u}(p)$ is calculated by Equation 2.7 where δ represents the ohmic heat generation and $\epsilon(p)$ the pressure dependent heat conduction to the gas surrounding the conductive bridge.

$$\bar{u}(p) = \frac{\delta}{\epsilon(p)}\left(1 - \frac{\tanh(\sqrt{\epsilon(p)}L/2)}{\sqrt{\epsilon(p)}L/2}\right) \tag{2.7}$$

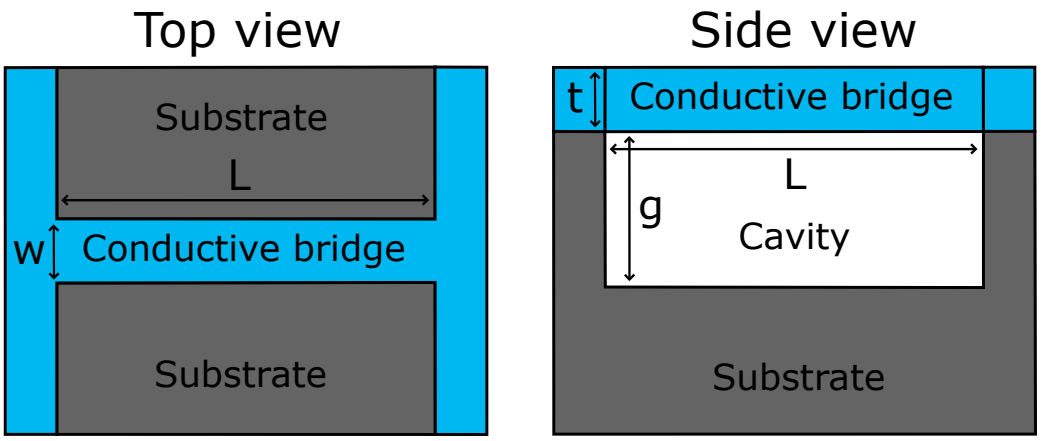


Figure 2.4: The Pirani pressure sensor top and side view with the conductive bridge marked in blue. The bridge length L, thickness t and width w and the cavity depth g are indicated.

The pressure dependent heat loss through the gas $\epsilon(p)$ is calculated by Equation 2.8 where η is the correction factor for the fringing of the heat flux through the cavity that is typically equal to 1, $\kappa_g(p)$ the pressure dependent thermal conductivity of the surrounding gas mixture and κ_b the thermal conductivity of the bridge.

$$\epsilon(p) = \frac{\eta \kappa_g(p)}{\kappa_b g t} - \delta\xi \tag{2.8}$$

The ohmic heat generation δ is calculated by Equation 2.9 where I is the electric current forced through the conductive bridge.

$$\delta = \frac{I^2 R_\square}{\kappa_b w^2 t} \tag{2.9}$$

The pressure dependent thermal conductivity of the surrounding gas mixture $\kappa_g(p)$ is now approximated by Equation 2.10 where p_0 is the transition pressure and κ_c the continuum limit of thermal conductivity, which equals $2.2 \cdot 10^{-2}$ W·m^{-1}·K^{-1} [15].

$$\kappa_g(p) \approx \kappa_c \left(\frac{p}{p + p_0} \right) \tag{2.10}$$

The transition pressure p_0 is approximated by Equation 2.11 where T_s is the substrate temperature and $\bar{v}$ the average molecular velocity. In this approximation, it is assumed that the substrate temperature is equal to the surrounding gas temperature and that the width of the conductive bridge is several orders of magnitude higher than the thickness ($w \gg t$).

$$p_0 \approx \frac{\eta \kappa_c T_s}{g \bar{v}} \tag{2.11}$$

The average molecular velocity is calculated by Equation 2.12 where m_d is the average mass of a dry air molecule and k_B the Boltzmann constant, which equals $1.381 \cdot 10^{-23}$ m^2·kg·s^{-2}·K^{-1}.

$$\bar{v} = \sqrt{\frac{8 k_B T_s}{\pi m_d}} \tag{2.12}$$

Finally, the average mass of a dry air molecule is calculated by Equation 2.13 where M_d and N_A represent the previously given molar mass of dry air and the Avogadro constant respectively.

$$m_d = \frac{M_d}{N_A} \tag{2.13}$$

Note that the given analyical model in Equations 2.6-2.13 is to be solved for the pressure dependent resistance $R(p)$ with the pressure p as the single free variable to simulate the electrical graphene-based Pirani pressure sensor behavior. This implies that all other variables need to be determined by literature research, measurements or estimation. These variables can be grouped as physical constants, gas mixture parameters, geometry parameters, bridge material parameters and measurement parameters. For convenience, these groups with corresponding variables are listed in Table 2.1.

Table 2.1: List of grouped variables used in the analytical model for the Pirani pressure sensor.

Group	**Variables**
Physical constants	N_A, k_B and κ_c
Gas mixture parameters	M_d and T_s
Geometry parameters	L, w, g, t and η
Bridge material parameters	ξ, κ_b and $R_\square$
Measurement parameters	I

The physical constant values are previously given and the gas mixture parameters are determined by assuming dry air at room temperature. Therefore the previously given molar mass of dry air M_d and substrate temperature T_s of 293 K are used. The geometry parameters depend on the device implementation and are determined in Section 3.3. The bridge material parameters for graphene are not taken from literature as they depend strongly on the fabrication process and the quality of the graphene. Instead, they are measured on an implemented device in Section 3.4. Finally, the measurement parameter I is given for each measurement, unless it is a voltage controlled measurement. In that case, the analytical model can not be rewritten for a forced voltage due to the hyperbolic function in Equation 2.7, which implies that the current has to be measured or determined quantitatively from the measurement results.

2.1.3. Graphene-Based Pirani Pressure Sensor Fabrication

An overview of the fabrication method that resulted from the efforts made by Sten Vollebregt and Robin Dolleman is schematically illustrated in Figure 2.5. The first step in Figure 2.5a consists of the deposition and patterning of a 50 nm thick molybdenum (Mo) layer on a 600 nm thick silicon dioxide (SiO_2) layer on a silicon (Si) substrate. This is followed by the selective chemical vapor deposition (CVD) of graphene on Mo in Figure 2.5b. The details of the graphene growth step are discussed in Section 2.2.1. The metal contacts to the graphene are then implemented by the deposition and patterning of gold (Au) in a lift-off process, followed by the etching of a cavity defined by photoresist under the Mo in the SiO_2 using buffered hydrofluoric acid (BHF) in Figure 2.5c. Finally, the photoresist is removed and the Mo is etched in hydrogen peroxide (H_2O_2) in Figure 2.5d followed by critical point drying (CPD) which results in a suspended graphene bridge.

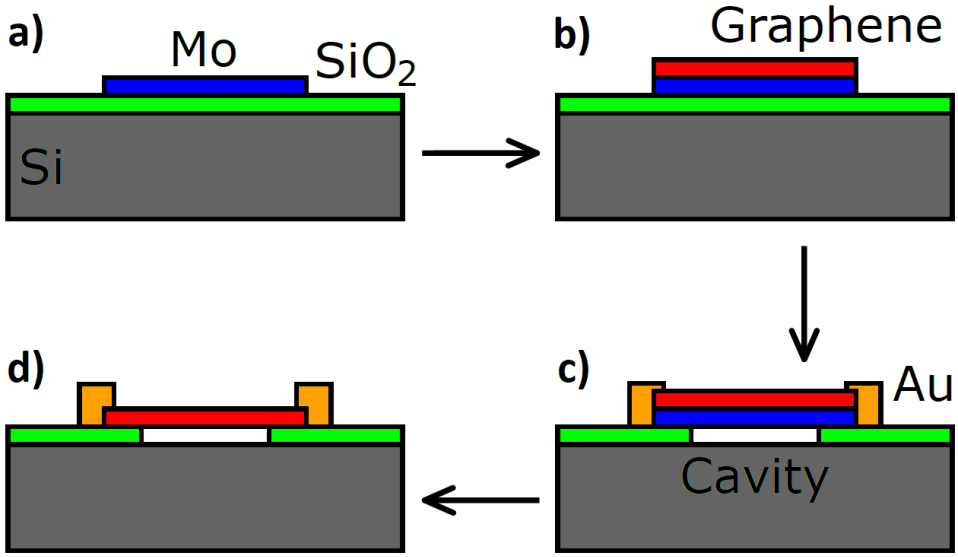


Figure 2.5: Overview of the Pirani sensor fabrication process. In a) the patterning and deposition of Mo on a SiO_2 layer is performed, in b) the selective CVD of graphene on Mo, in c) the metal contact cavity implementation and in d) the Mo etching which result in a suspended graphene bridge.

The proposed Pirani sensor fabrication method as well as the incorporation of graphene as the Pirani bridge material have significant advantages. Firstly, the proposed Pirani fabrication method does not require a wafer-to-wafer transfer step. Secondly, due to the high area-to-thickness ratio, graphene-based Pirani devices can be much smaller than implementations with other materials as these materials would break for such area-to-thickness ratios. This reduces the device footprint which reduces the average fabrication cost and opens possibilities for in

situ pressure monitoring inside sealed MEMS. Thirdly, the fabrication process with tuned cavity depth benefits the design of pressure sensors for specific ranges. Finally, a Pirani sensor can also be used as a gas sensor, as it is dependent on the composition of the gas mixture surrounding the conductive bridge. A graphene-based Pirani sensor therefore offers miniaturization to the field of thermal conductivity detectors (TCD).

A graphene-based Pirani pressure sensor has the advantage that it can be made smaller than current implementations. A smaller value for the bridge width w results in an inversely quadratic increase of the ohmic heat generation δ, according to Equation 2.9. The increase of δ in turn decreases the pressure dependent heat loss through the gas $\epsilon(p)$, according to Equation 2.8. The combination of increasing δ and decreasing $\epsilon(p)$ and L results in a strong increase of the pressure dependent average temperature rise of the conductive bridge $\bar{u}(p)$, according to Equation 2.7. This results in an increase of the pressure dependent resistance $R(p)$, according to Equation 2.6. Therefore, decreased w and l result in a stronger pressure dependency of $R(p)$, which implies that graphene-based Pirani pressure sensors allow a higher sensitivity compared to existing implementations. Furthermore, the low thickness of graphene increases δ inversely proportional as well.

2.2. Graphene Growth and Characterization

In recent years the production of high quality graphene films has been achieved. This includes the synthesis of both mono- and multi-layer graphene. There are various methods to synthesize graphene [2, 3], which include mechanical exfoliation of graphite [1], annealing of silicon carbide (SiC) [22], unzipping of carbon nanotubes (CNT) [23] and CVD growth on transition metals [24, 25]. Mechanical exfoliation, annealing of SiC and the unzipping of CNT can not be integrated with a standard electronics fabrication process without a wafer-to-wafer transfer step. This renders these methods insufficient with regard to the main research question. However, the CVD growth on transition metals does not require a (wafer-to-wafer) transfer step and is furthermore an efficient and inexpensive method for graphene synthesis [26]. Commonly used transition metals are copper (Cu) foils [24] and nickel (Ni) foils [25]. This method of graphene synthesis is also used in the proposed graphene-based Pirani sensor fabrication in Section 2.1.3, but with the use of Mo as catalyst.

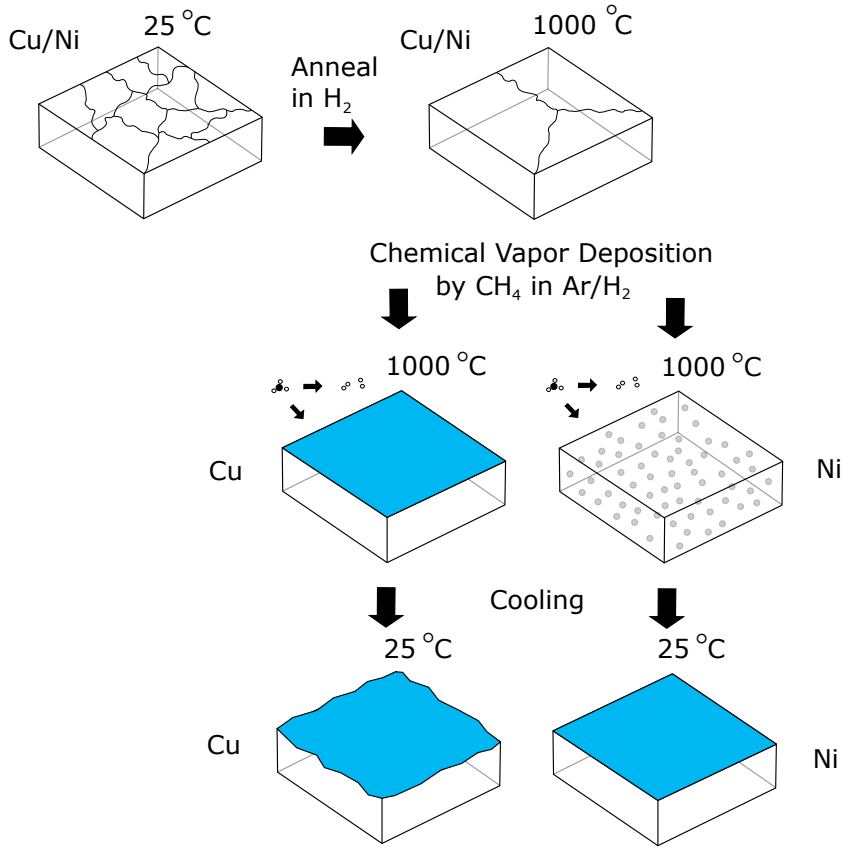


Figure 2.6: CVD growth process of graphene on transition metals Cu and Ni. The thin films are first annealed followed by the CVD step with methane. The wafers are cooled down to room temperature. The graphene layer is depicted in blue.

2.2.1. Selective CVD of Graphene on Molybdenum

The CVD growth process consists of several steps, for which the details differ between the different transition metals. Figure 2.6 shows the CVD growth process steps and differences between the commonly used transition metals Cu and Ni. The process starts with a thin film of poly crystalline Cu or Ni on top of the Si bulk at room temperature. Generally there is a SiO_2 layer between the metal thin-film and Si bulk to prevent diffusion of the metal atoms into the Si bulk. The poly crystalline Cu or Ni thin films are first annealed at at 900 °C to 1000 °C to increase the thin film grain size and reduce the metal oxide to metallic state, which allows for higher quality graphene films as the grain boundaries result in defects in the graphene formation. Secondly, the CVD growth step is performed at high temperature with methane, that acts as the carbon source. Finally, the wafers are cooled down to room temperature. Note that the actual growth process is different for Cu and Ni due to different carbon solubilities.

The thin film transition metals are exposed to methane during the CVD growth step. The methane molecules decompose in carbon and hydrogen at the surface of the transition metals, which function as a catalyst that lowers the energy barrier for this decomposition. The carbon atoms then dissolve in the Ni thin film while they adsorb to the Cu surface, due to the difference in carbon solubility. This solubility is low for Cu, while it is high enough for carbon atoms to diffuse in Ni. The difference in physical process is illustrated in Figure 2.7. Before cooling, graphene has already formed on the Cu thin film while this is not the case for Ni. The different thermal expansion coefficients of graphene and Cu result in wrinkles in the formed graphene film when the wafer is cooled. These wrinkles can form across grain boundaries which indicates that the graphene film is continuous. In the case of Ni, the carbon atoms diffuse in the thin film during the CVD growth and then segregate to the Ni thin film surface during cooling, which is due to the carbon solubility decreasing as temperature decreases. Depending on the amount of carbon atoms in the Ni thin film, the amount of layers of graphene formed on the surface is different. The lattice of Ni(111) is similar to that of the hexagonal lattice of graphene, which allows for excellent graphene growth without wrinkles on Ni(111). The graphene film uniformity is limited by the Ni thin film grain size as the diffusion rates are different at the grain edges [27]. Multi-layers on Ni therefore tend to be non-uniform.

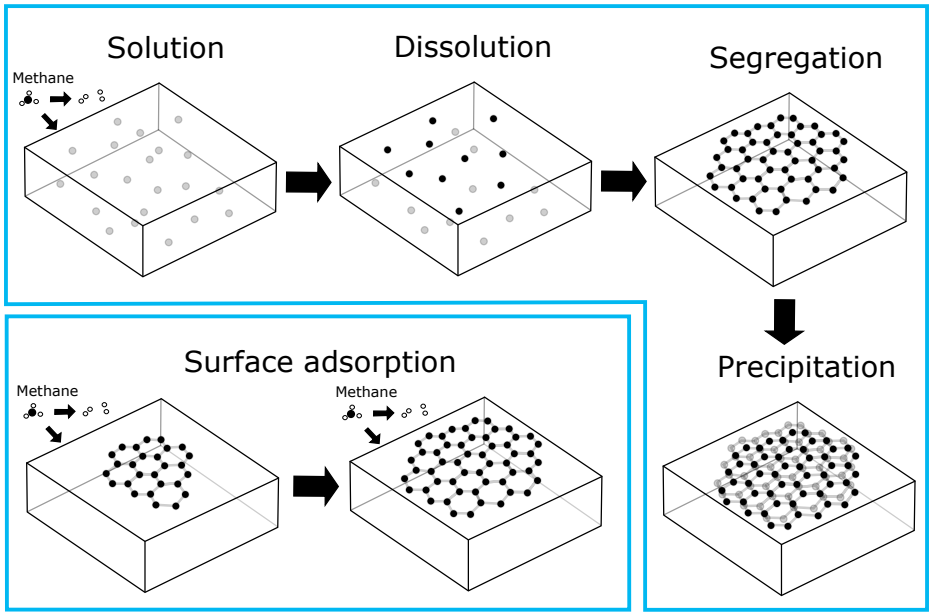


Figure 2.7: Graphene formation by either the surface adsorption or dissolution and segregation process [3].

The transition metals Ni and Cu are difficult to work with in terms of patterning, as the growth temperature is close to the melting temperature of these metals. Furthermore, these Cu poses contamination issues in the front-end fabrication. To use the grown graphene on Ni or Cu films in applications using standard CMOS processing, a wafer-to-wafer transfer step is required [28]. This implies that these transition metals can not be used in this research. Fortunately, a transfer free CVD process developed by our group that uses Mo as transition metal exists [29] after the feasibility for CNT growth on Mo was already reported [30]. The CVD process for Mo is similar to that of Ni, but the carbon solubility of Mo is lower and it has a larger range of optimal cooling rates which additionally allows for a more controllable and uniform multi-layer graphene growth [28, 31–33]. Furthermore, the methane flow rate and

growth time do not affect the graphene formation on Mo, with exception of the amount of multi-layers, while this may affect graphene growth on Ni. The advantages of Mo over Cu and Ni is that it is front-end compatible with the fabrication process, it has a much higher melting temperature than the graphene growth step and it forms uniform multi-layer graphene.

2.2.2. Graphene Characterization Technique

There are various different tools that can be used to characterize aspects of the fabricated graphene [2]. Some effective methods are optical contrast [34], scanning electron microscopy (SEM) [35], electron diffraction [36] and Raman spectroscopy [37]. Even individual atoms in the graphene film can be observed by using High-Angle Annular Dark-Field Scanning Transmission Electron Microscopy, which visualizes single defects in the graphene lattice [38]. The method used in this research project is Raman spectroscopy, as these the most widely used method and equipment is available at the university faculty. Additionally, SEM is used for visualization and evaluation of various samples at different stages of the fabrication process.

Raman spectroscopy is a measurement technique that measures the frequency shift of reflective light by exposing the sample to a laser with a known wavelength. This technique is primarily used to characterize the amount of layers and defects in the graphene film, but more properties can be probed. It is a powerful tool when comparing slightly different graphene synthesis processes [2, 37, 39]. The graphene Raman spectrum consists of various peaks which are depicted in Figure 2.8. The intensity is in is arbitrary units (a.u.) as this is related to the counts of a detector that will vary for different setups and over time. To compare Raman spectra, the ratio between peaks is therefore used. Note that the location of the peaks depends on the laser wavelength used to probe the graphene film.

The three most important bands are the G-, D- and 2D-peaks. The G-peak is located at approximately 1580 cm^{-1} and it is induced by in-plane vibrations of the sp^2 hybridized carbon atoms. The intensity increases linearly for an increasing amount of layers when compared to the other bands [40]. The D-peak is located at approximately 1350 cm^{-1} and it is induced by all kinds of defects in the graphene film. This includes the amount of layers [2] and wrinkles [28]. Its shape, width and position change for increasing amount of layers in the graphene film [41]. The D'-peak is induced by similar processes as the D-peak and becomes observable when the D-peak is of significant intensity which can cause an apparent shift in the G-peak. The 2D-peak is located at approximately 2700 cm^{-1} and is the overtone of the D-peak as result of the double resonance Raman scattering process and appears even without defects in the graphene film [37]. Note that this peak will therefore be present even if the D-peak is absent. This peak is directly dependent on the amount of layers in the graphene film and is hence the most reliable peak when determining the amount of layers [41]. However, this dependency is only strong for few-layer graphene. For a mono-layer graphene film, the full width at half maximum (FWHM) is approximately 25 cm^{-1} [2].

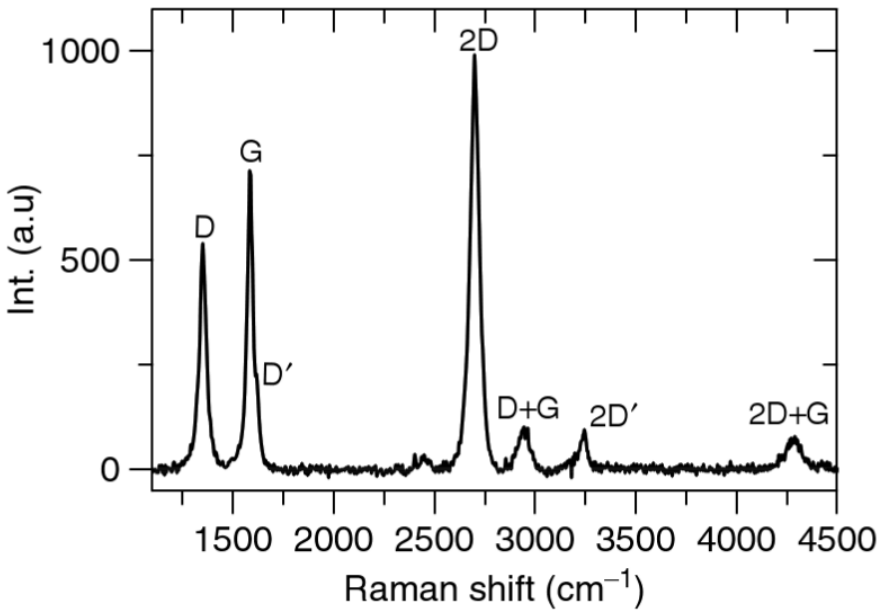


Figure 2.8: Example of a Raman spectrum of a mono-layer graphene film probed with a 514.5 nm laser [2].

The G-peak is shifted due to induced strain [42], orientation [43] or other environmental effects. The strain and orientation affect the phonon behavior in the graphene film, which causes the shift of the peak. Moreover, significant amount of induced strain splits the G-peak in two peaks [2]. This phenomenon is depicted in appendix Figure B.1. The 2D-peak is similarly dependent on induced strain.

2.3. BICMOS Process

The BICMOS process of the Else Kooi Laboratory (EKL) at the Delft University of Technology is used primarily for educational purposes [44]. It can be used to fabricate both bipolar and CMOS devices, while it only requires five masks. This research work only focuses on CMOS electronics as these are most popular nowadays. The simplicity of the BICMOS process makes it a suitable process to experiment with and is therefore adopted in this work. Unfortunately, no full design kit is available for this process nor has it been properly characterized in circuit design. The work in the process of Zahra Kolahdouz Esfahani [45] is used as a starting point in this research work.

2.3.1. BICMOS Core Fabrication Steps

The five core fabrication steps of the BICMOS process are schematically illustrated in Figure 2.9, which are the N-well (NW), shallow p-type (SP), shallow n-type (SN), contact openings (CO) and metal interconnect (IC). The process starts with bare p-type silicon with a highly uniform background dopant concentration epi-layer. The NW step then implements the n-type doped N-well that is required for a PMOS device. Phosphorus ions (P^+) are implanted and diffused deep in the silicon bulk to form a well. This is followed by the SP step that implements the highly doped shallow p-type regions. These consist of source and drain of the PMOS and the guard ring of the NMOS and are implemented by boron ions (B^+) implantation. The third step is the SN step that complements the doped regions by arsenic (As^+) implantation to form the source and drain of the NMOS and the guard ring of the PMOS. In the fourth step the gate material is formed by wet thermal oxidation and contacts to the doped regions in the silicon bulk are etched through the SiO_2. The final step implements the metal interconnect which is often 99% aluminum and 1% silicon (AlSi) as this material does not diffuse in the Si bulk and has a low contact resistance. Each core processing step requires a mask to define the respective regions.

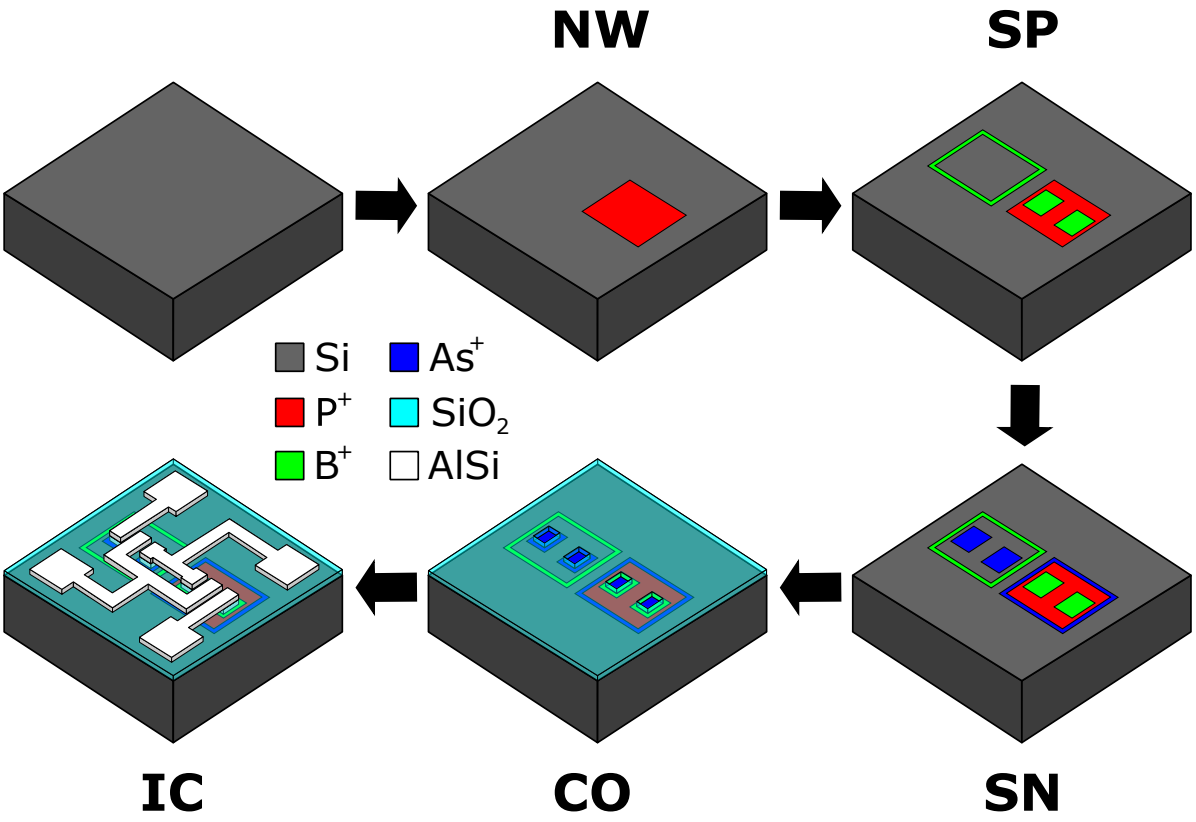
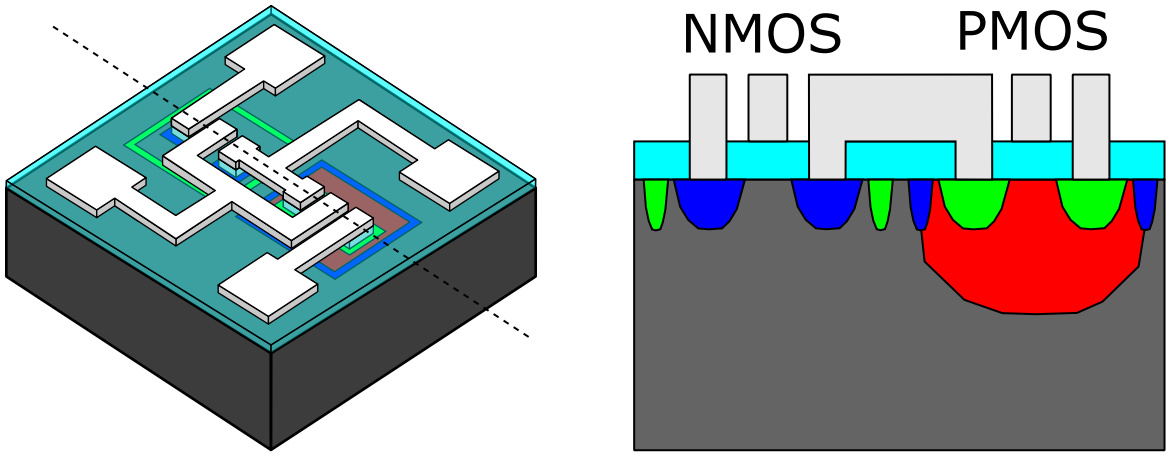


Figure 2.9: The five core fabrication steps of the BICMOS process, depicting the implementation of a single inverter. The legend shows the corresponding materials of each color used in the schematic illustration.

The implanted dopant atoms are activated by annealing the wafer at high temperature. This activation is the process of placing the dopant atoms in the damaged silicon lattice. A long anneal is performed after the NW step to activate and diffuse the dopant atoms in the lattice. Another anneal is performed during the wet thermal oxidation of the gate material, which activates the SN and SP regions. Contrary to the illustration in Figure 2.9, the doped regions have no color difference compared to the silicon bulk. Prior to the ion implantation a dirt barrier on the wafer is created by thermal oxidation. This layer captures dirt particles that may hit the wafer during the ion implantation and act as a scatter layer for the implantation ions to prevent channeling effects.

A cross section of the single inverter is schematically illustrated in Figure 2.10. Note that the N-well is much deeper than the SN and SP regions. Furthermore, in the source and drain of the PMOS are both P^+ and B^+ present although the concentration of the latter is several order of magnitude higher. The guard rings are left unconnected in this illustration in favor of simplicity. In reality, these need to be connected and correctly biased to be effective. It is common practice to connect the NMOS and PMOS guard ring to ground and supply voltage respectively.



(a) 3D representation of the inverter. (b) Cross section of the inverter.

Figure 2.10: Schematic illustration of the inverter with in a) the 3D representation and in b) the cross section at the dotted line. The used colors match those used in Figure 2.9.

There are oxide formation or depostion methods available at EKL of which two are used in this work. The first is the mentioned wet thermal oxidation used for the gate material implementation. This method grows highly uniform SiO_2 on the silicon bulk at a high temperature of approximately 1100 °C by providing a water vapor flow in the furnace. At this temperature the water molecules diffuse through the SiO_2 and react with the silicon, resulting in SiO_2 growth on both sides of the wafer by consuming silicon. The growth rate is predicted with the Deal-Grove model [46]. The growth rate is different for the doped regions by approximately 2x and 1.5x for the SN and SP regions respectively. Since the SiO_2 color is highly dependent on the layer thickness, there is a distinct color difference between the SN, SP and field oxide. This dependency is depicted in Figure 2.11, resulting in metallic blue, light blue and yellow for the field, SP and SN oxide respectively in this process. The second method is tetraethylorthosilicate (TEOS) plasma-enhanced chemical vapor deposition (PECVD) at approximately 350 °C. The TEOS plasma reacts at the exposed wafer surface and forms SiO_2 directly, without consuming silicon. It can therefore be deposited on other materials than silicon and is a faster process although the SiO_2 is less uniform compared to wet thermal oxidation.

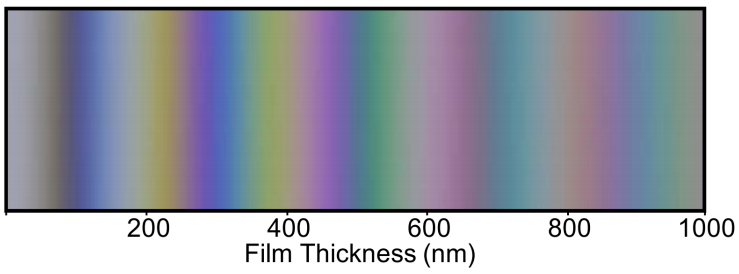


Figure 2.11: Color dependency on thickness of a thermal SiO_2 layer [47].

2.3.2. Threshold Voltage Adjustment

The threshold voltage of the NMOS and PMOS devices is influenced by adding a blanked of B^+ after the SN step and before the gate oxidation step. In this educational process, it is common practice to vary the blanket dose in each wafer quadrant to pursuit symmetry in threshold voltage of the NMOS and PMOS. This concept with corresponding adjustment doses is illustrated in Figure 2.12. A higher voltage adjustment dose increases the threshold voltage of all devices as it increases the p-type concentration in the channels. The threshold voltage is an important characteristic of CMOS devices and information on it is required during the design stage. The mathematical model for the threshold voltage of CMOS devices is given below [48].

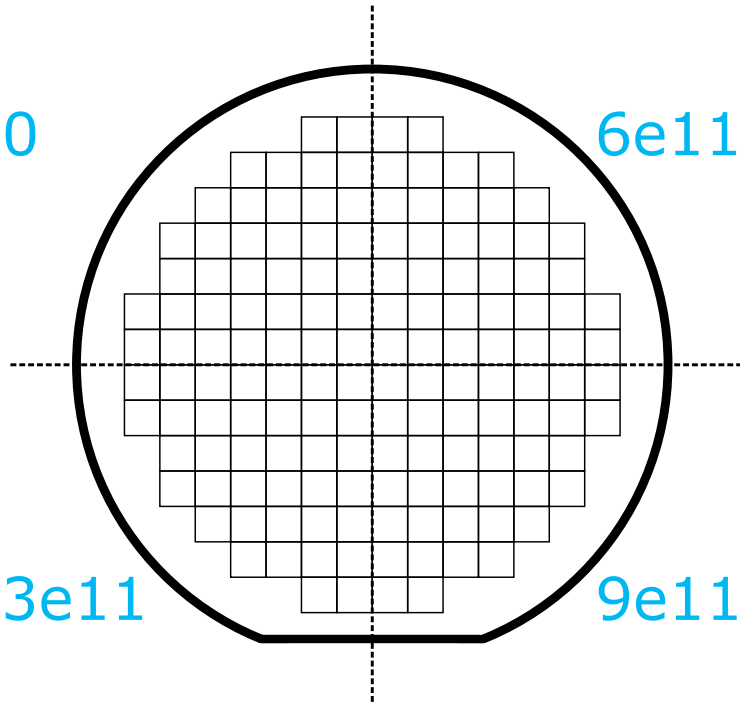


Figure 2.12: Threshold voltage adjustment doses of B^+ implantation for each wafer quadrant. Note that the unit of the doses is atoms·cm^{-2}.

The threshold voltage of an NMOS device is calculated by Equation 2.14 where ϕ_{ms} is the metal-semiconductor work function difference, ϕ_{fp} the fixed work function of a p-type channel, $|Q'_{SD}(max)|$ the magnitude of the maximum space charge density per unit area of the depletion region, Q'_{SS} the oxide charge, t_{ox} the oxide thickness and ϵ_{ox} the permittivity of SiO_2, which equals $3.45 \cdot 10^{-13}$. The the metal-semiconductor work function difference ϕ_{ms} is estimated using the channel doping and gate material in literature [48].

$$V_{Tn} = (|Q'_{SD}(max)| - Q'_{SS})\left(\frac{t_{ox}}{\epsilon_{ox}}\right) + \phi_{ms} + 2\phi_{fp} \tag{2.14}$$

The fixed work function of a p-type channel ϕ_{fp} is calculated by Equation 2.15 where N_a is the acceptor doping concentration, n_i the intrinsic carrier concentration and V_t the thermal voltage. Constants n_i and V_t equal $1.45 \cdot 10^{10}$ cm^{-3} and $2.26 \cdot 10^{-2}$ at 300 K respectively.

$$\phi_{fp} = V_t \, ln\left(\frac{N_a}{n_i}\right) \tag{2.15}$$

The magnitude of the maximum space charge density per unit area of the depletion region $|Q'_{SD}(max)|$ is calculated by Equation 2.16 where x_{dT} is the maximum space charge width for a given doping concentration and q the electron charge, which equals $1.60 \cdot 10^{-19}$ C.

$$|Q'_{SD}(max)| = qN_a x_{dT} \tag{2.16}$$

The maximum space charge width for a given doping concentration x_{dT} is calculated by Equation 2.17 where ϵ_s is the permittivity of Si, which equals $1.04 \cdot 10^{-12}$.

$$x_{dT} = \sqrt{\frac{4\epsilon_s \phi_{fp}}{qN_a}} \tag{2.17}$$

Similarly, the threshold voltage of a PMOS device calculated by Equation 2.18, where ϕ_{fn} is the fixed work function of an n-type channel that is calculated using Equation 2.15 by substituting N_a by N_d that represents the donor doping concentration. Furthermore, x_{dT} is calculated by Equation 2.16 using the same substitution.

$$V_{Tp} = (-|Q'_{SD}(max)| - Q'_{SS})\left(\frac{t_{ox}}{\epsilon_{ox}}\right) + \phi_{ms} - 2\phi_{fn} \tag{2.18}$$

Note that there are still three undetermined parameters in the model that are determined by the process, when considering a fixed gate material. These are the density of doped carriers N_a or N_d in [cm^{-3}], the gate material thickness t_{ox} in [cm] and the fixed charge for surface states Q'_{SS} in [C·cm^{-2}].

2.4. Conclusions

The proposed Pirani sensor fabrication method does not require a wafer-to-wafer transfer step and will be used to experimentally integrate in the BICMOS process. Furthermore, it offers the ability of tuning the gap depth which determines the operating range. Graphene-based Pirani devices can be smaller than current implementations due the high area-to-mass ratio. An analytical model for the Pirani pressure sensor is defined and its parameters are grouped of which most are to be determined later. The graphene is implemented through CVD on Mo as this is compatible with the front-end fabrication and can be patterned before graphene growth. The educational BICMOS process is a simple five step process and is therefore used in this work. An analytical model for the device threshold voltages is defined and three parameters are pointed out as to be determined by the fabrication process.

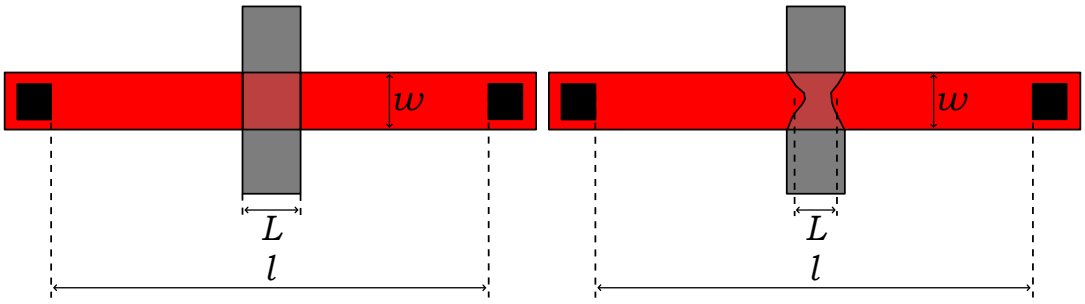
3

Graphene-Based Pirani Pressure Sensor Characterization

This chapter investigates the properties of a Pirani pressure sensor. Two batches of devices are fabricated and released. The pressure dependency of the resistance is measured in a pressure controlled experimental setup. All fabricated devices have an etched cavity depth of 0.6 μm and multi-layer graphene bridge thickness of ~ 7 nm, which are two of the geometry parameters. Equation 2.5 results in an operational pressure range of approximately $1.5 \cdot 10^1$ mbar to $1.5 \cdot 10^3$ mbar. Furthermore, the other geometry parameters and design aspects are chosen based on the measurement results. This is followed by the determination of the bridge material parameters from measurements. Finally, the chapter is concluded by listing the important findings.

3.1. First Batch Graphene-Based Pirani Sensor Results

The Pirani sensors of the first batch are fabricated according to the mask layout design that is schematically illustrated in Figure 3.1a. The red rectangle marks the graphene film, the grey rectangle the window used to etch the cavity and the black squares the metal contacts to the metal IC layer. Note that no IC is illustrated apart from the contacting points in favor of simplicity. Furthermore, the figure depicts the total graphene film length l, conductive bridge length L and width w. Figure 3.1b illustrates the layout that will result from the mask design, where rounded edges below the conductive bridge are caused by inevitable incomplete under etching of the cavity. This is due to the fact that the etchant etches under the bridge from the sides and can therefore not create a straight cavity sidewall below the graphene bridge. Note that this affects the effective bridge length L.



(a) Mask layout design. (b) Fabrication result.

Figure 3.1: Top view of the Pirani sensor layout of the first batch with in (a) the used mask layout design and in (b) the fabrication result according to this mask layout design. Red marks the graphene, grey the cavity and black the metal.

The SEM image in Figure 3.2 depicts the typical fabrication result of the first batch. Two dies were released in the first batch, of which a complete set of suspended Pirani sensor SEM images is listed in appendix Figure C.1 and Figure C.2. Four and six suspended Pirani sensors were observed on the first and second die respectively. The typical aspect ratio is ~ 1.4 and the graphene bridge typically sags towards the substrate, causing the effective gap depth to decrease.

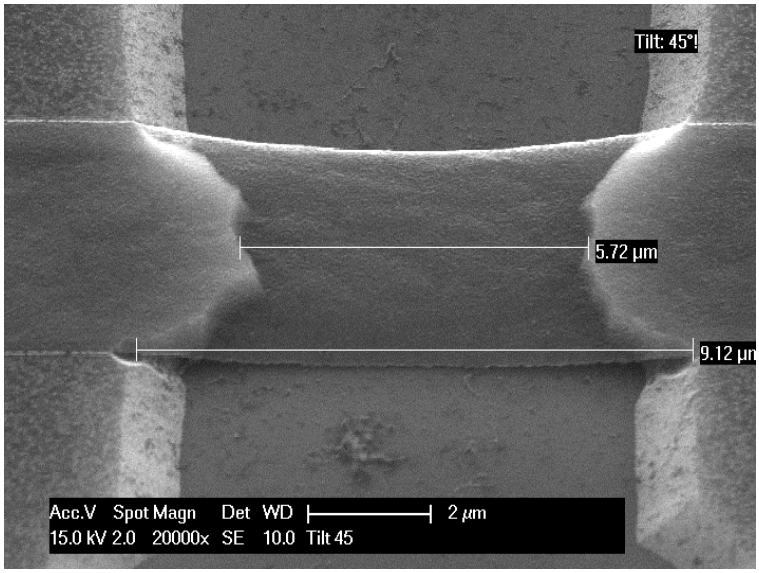


Figure 3.2: SEM image of the typical fabrication result of a Pirani pressure sensor in the first batch at a tilt of $45°$. It has a width of 5 μm and effective length of ~ 7 μm.

The pressure dependency measurement setup is schematically illustrated in Figure 3.3 and is capable of automated measurements. A *Matlab* script running on a laptop communicates through USB with the source-and-measurement unit (SMU) and pump controller. The SMU is capable of performing both 2- and 4-wire measurements. Note that in the first batch, only 2-wire measurements are possible due to its layout design. The pump controller is a controlled voltage source that controls the pressure controller with an analog signal. The pressure controller regulates the pressure in the vacuum chamber using a gas source and is read out by a multimeter. The gas source used is nitrogen (N_2), whose properties are similar to dry air. An upward and downward pressure sweep is performed to monitor drift and hysteresis of the resistance. Neither is observed in the reported measurement results.

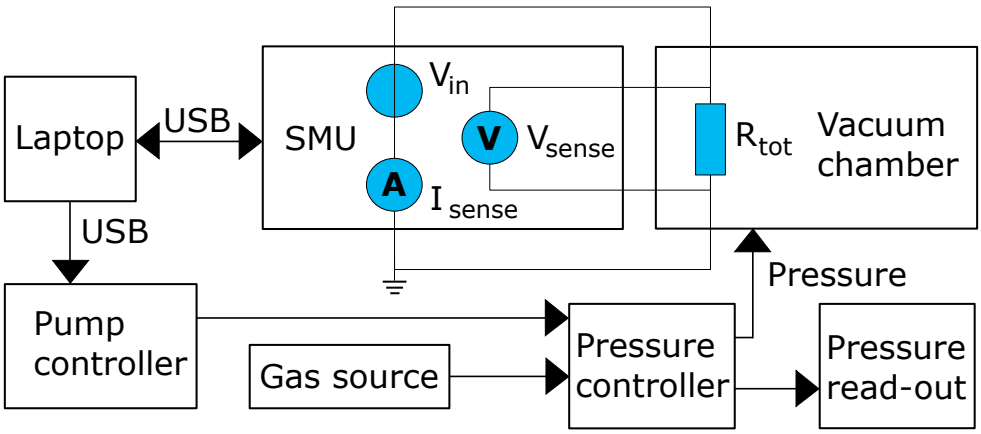


Figure 3.3: Schematic illustration of the automated pressure dependency measurement setup. A Keysight B2901A SMU, Rigol DP832A voltage source pump controller, Proportionair PA2254 dual-valve pressure controller and Keithey 199 pump read-out are used in the setup.

The results of the pressure dependency of the conductive bridge resistance of the first batch are depicted in Figure 3.4a. The measured pressure range corresponds well with the predicted operating range of $1.5 \cdot 10^1$ mbar to $1.5 \cdot 10^3$ mbar. Unfortunately, just two devices are found to operate, which are both on the second die and is likely due to wire bonding issues. The resistance change is defined as the ratio in Equation 3.1 where R is the measured resistance dataset and R_{max} the maximum value in that dataset. There is a definite pressure dependency where magnitude is dependent on the bias voltage, which makes this batch world's first graphene-based Pirani pressure sensors. A larger bias voltage implies a larger current I, which results in more ohmic heat generation. The largest maximum resistance change is 2.8 % observed on device 2F for a bias voltage of 15 V. The power consumption is calculated by V^2/R and the lowest power consumption is at a bias voltage of 9 V with maximum resistance change of 0.8 % at 0.9 mW observed on device 2D. The sheet resistance is determined in Section 3.4.

$$\text{Resistance change} = \frac{R}{R_{max}} * 100 \tag{3.1}$$

The sensitivity to pressure is depicted in Figure 3.4b, which is derived by fitting a third order polynomial to the measurement data and calculating the derivative with respect to the pressure. The sensitivity maximum is not included in the measured pressure range and appears to be at lower pressure. The sagging of the conductive bridges gives a smaller cavity depth, which results in a higher pressure range according to Equation 2.5. The shift towards a lower pressure range suggests that a dominant factor other than cavity depth is left out. The gentle increase of sensitivity for the highest pressures is due to a fitting artifact.

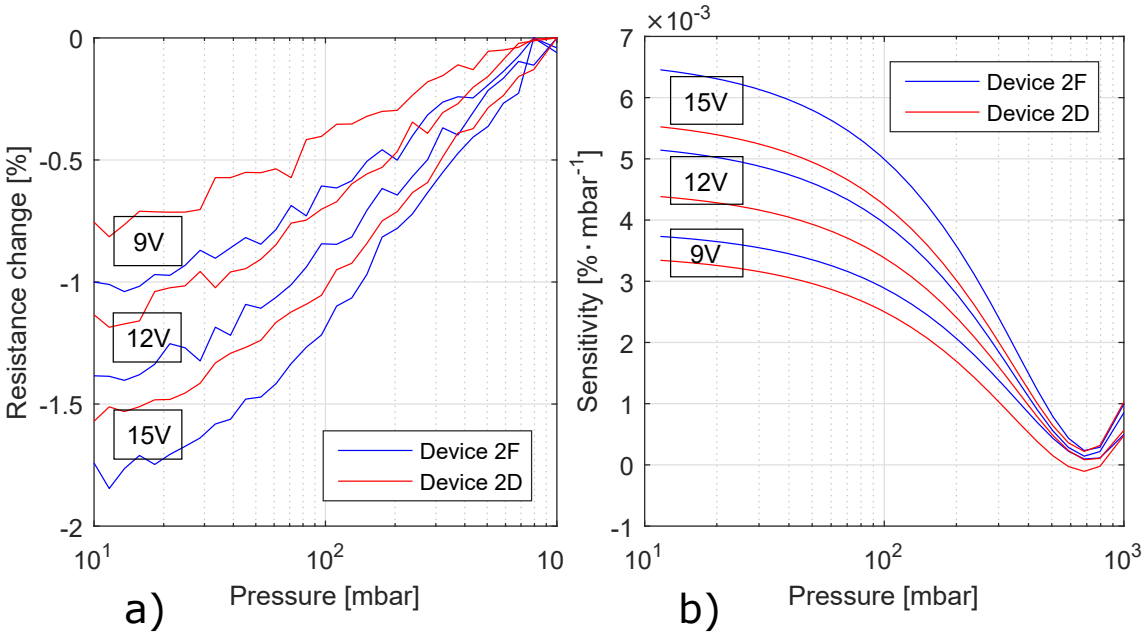


Figure 3.4: Measurement results of the pressure dependency of the Pirani sensor conductive bridge resistance in a) and the found device sensitivity in b). Three different bias voltages are applied and two devices are found to operate. The sensitivity is derived by the derivative of a third order polynomial fit to the data. The device labels correspond with the listing in appendix Figure C.2.

3.2. Second Batch Graphene-Based Pirani Sensor Results

The second batch of Pirani sensors is fabricated according to the mask layout design that is schematically illustrated in Figure 3.5. The incomplete under etching is still inevitable and the used colors match the layout design given before. This design opens the possibility of 4-wire measurements as it has two extra contacts. The force pair is V_{in} and GND and the sense pair is marked by V_{sense}. Note that the total length l is reduced significantly, which reduces the impact of the non-suspended graphene film caused by ohmic heating.

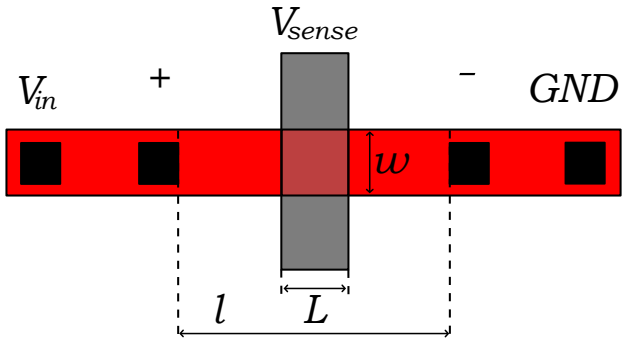


Figure 3.5: Top view of the Pirani sensor layout of the second batch. Red marks the graphene, grey the cavity and black the metal.

The SEM images in Figure 3.6 depicts the fabrication results of different aspect ratios in the second batch. One die was released in the first batch with device aspect ratios up to 8. On this die, the yield of suspended Pirani sensors is ~ 75 %. The SEM images reveal that devices with a longer bridge length tend to contact the Si substrate.

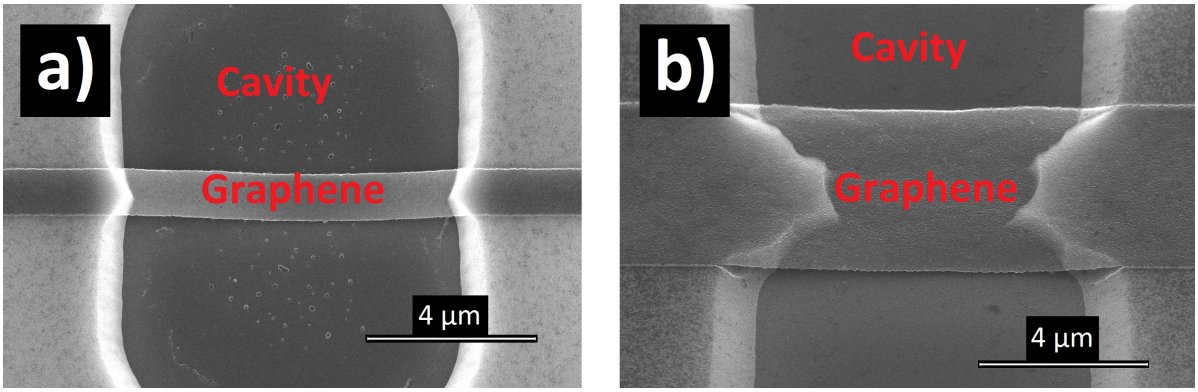


Figure 3.6: SEM images of suspended Pirani sensors in the second batch with a) high aspect ratio (width of 1 μm and length of ~ 8μm) and b) with low aspect ratio (width of 5 μm and length of ~ 6μm). Images taken under a 45° angle.

Additionally, Raman spectroscopy is performed on the devices in the second batch during different stages in the process. This includes on Mo before release and after release on SiO_2 and when suspended. The results are given in Figure 3.7. The D/G ratios are similar in all monitored process stages, from which is concluded that the process steps do not affect the graphene quality.

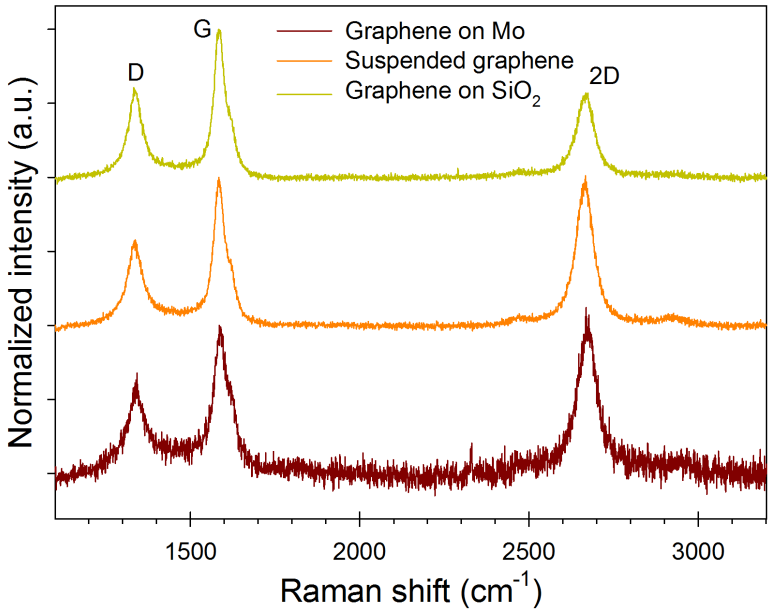


Figure 3.7: Raman spectroscopy of graphene strips in the second batch at different stages of the process. This includes before release on Mo, after release on SiO_2 and suspended. Identical D/G ratios indicate no change in defect density.

The results of the pressure dependency of the conductive bridge resistance of the second batch are depicted in Figure 3.8a. At least five devices with different geometries are found to be operating. The reason for leaving out the results of other devices is due to drift in the measurement results, which causes the devices to give irreproducible results. Additionally, the pressure dependency of non-suspended graphene strips is measured and depicted in Figure 3.8a. It is concluded that non-suspended strips show no pressure dependent resistance while the suspended strips do. All measurements were done at a 7.5 V bias.

The sensitivity to pressure is depicted in Figure 3.8b, which is derived by fitting a third order polynomial to the measurement data and calculating the derivative with respect to the pressure. The sensitivity maximum is again not included in the measured pressure range and appears to be at lower pressure. The gentle increase of sensitivity for the highest pressures is due to a fitting artifact. Equation 2.9 in the analytical model of the Pirani pressure sensor states that the ohmic heat generation increases inversely quadratic for decreasing bridge width, which in turn increases the maximum resistance change. Figure 3.8b complies with this statement as the narrower bridges generally have a larger sensitivity. Although the $2\ \mu$m narrow bridge has a larger sensitivity than the $1\ \mu$m narrow bridge, but this could be related to effects like the sagging. Equation 2.6 states that the pressure dependent temperature rise is dependent on the bridge length, but no quantitative relation of the bridge length is derived from Figure 3.8b. The shortest bridge has the highest sensitivity in the measurement results. For equal sensitivity a decreased geometry results in a decreased power consumption.

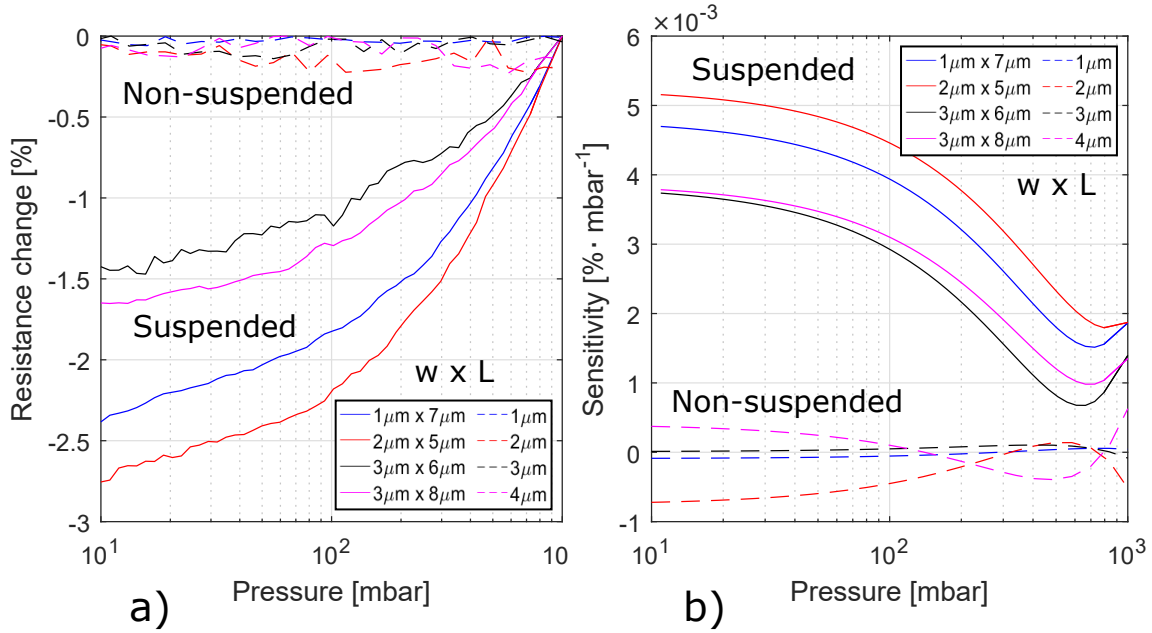


Figure 3.8: Measurement results of the pressure dependency of the Pirani sensor conductive bridge resistance in a) and the found device sensitivity in b). The devices were biased at 7.5 V and five devices were found to be operational. The pressure dependency of non-suspended graphene strips is included as reference. The sensitivity is derived by the derivative of a third order polynomial fit to the data.

3.3. Pirani Pressure Sensor Design Choices

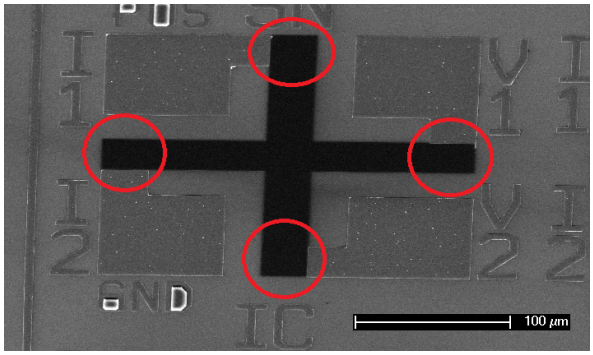
The gap depth and bridge thickness were already mentioned and are kept the same in favor of future comparisons. Multiple combinations of the bridge width and length are incorporated in the design to better characterize the relation between width, length and sensitivity in the future. The bridge width should be kept as low as possible to increase the sensitivity and is therefore chosen to be $1\ \mu$m, $2\ \mu$m and $3\ \mu$m. The bridge length is kept to a minimum to reduce the observed sagging effects. The cavity width is therefore chosen to be $1\ \mu$m, $2\ \mu$m and $3\ \mu$m. This geometry allows for the miniaturization with a factor of at least 100x compared to state-of-the-art implementations [12–15]. Note that different etch times are required to fully etch the cavities under the bridge, which in turn results in different bridge lengths. This is summed up in Table 3.1 where etch times A, B and C correspond with the time required to fully etch under the corresponding bridge width. These etch times are determined by dividing the oxide layer thickness by the etch rate. To characterize all devices, it is therefore required to release three different dies with each a different etch time.

Furthermore, the metal contacts to the graphene bridge can not be placed directly at the edge of the cavity due to the risk of under etching the metal contact when etching the cavity. The distance was $\sim 14\ \mu$m and $\sim 3\ \mu$m in the first batch and second batch respectively. It is chosen that a minimal distance of $3\ \mu$m is required between cavity edge and metal contact. The total graphene strip length l between metal contacts is also listed in Table 3.1. The non-suspended part of the graphene strip reduces the sensitivity of the device significantly as it is responsible for at least half of the total graphene strip resistance.

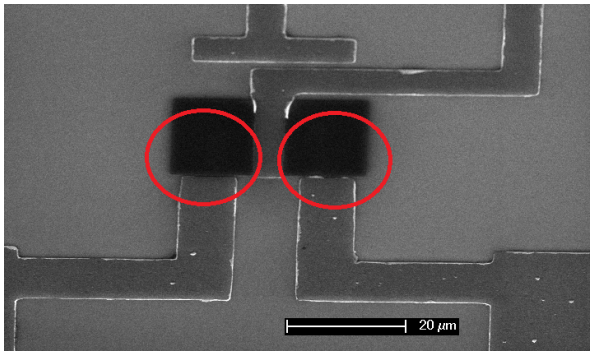
Table 3.1: Design geometry parameters with minimum widths and length. The edge time is dependent on the bridge width and is marked with A, B or C.

Width w	**Cavity width**	**Etch time**	**Length** L	**Total length** l
1 μm	1 μm	A	2 μm	8 μm
1 μm	2 μm	A	3 μm	9 μm
1 μm	3 μm	A	4 μm	10 μm
2 μm	1 μm	B	3 μm	9 μm
2 μm	2 μm	B	4 μm	10 μm
2 μm	3 μm	B	5 μm	11 μm
3 μm	1 μm	C	4 μm	10 μm
3 μm	2 μm	C	5 μm	11 μm
3 μm	3 μm	C	6 μm	12 μm

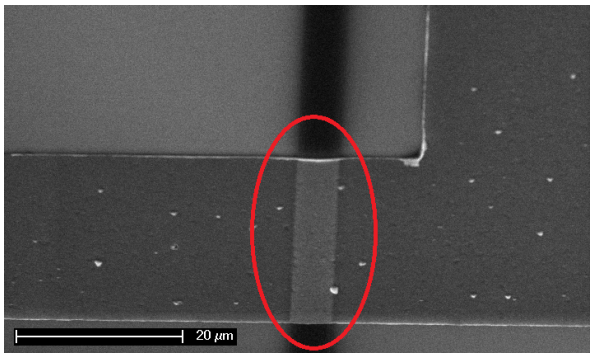
The contact between AlSi and graphene is investigated on a test wafer. The AlSi did not adhere well to the graphene, which results in missing AlSi at large contact areas with graphene. The SEM images in Figure 3.9a and Figure 3.9b show these areas and mark missing AlSi with red circles. Fortunately, the AlSi does adhere to the graphene at smaller contact areas with overlap on two sides of the graphene strip. These areas are depicted in Figure 3.9c and Figure 3.9d.



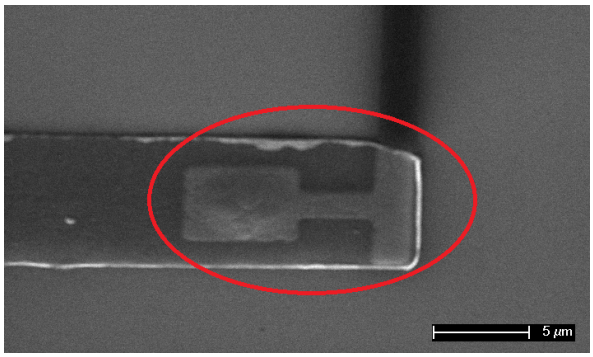
(a) Van der Pauw layout.



(b) NMOS device layout.



(c) Van der Pauw layout.



(d) NMOS device layout.

Figure 3.9: SEM images of large contact areas between graphene and AlSi with in (a) a Van der Pauw layout and in (b) a zoomed view of an NMOS layout and small contact areas between graphene and AlSi with overlap on two sides of the graphene strip with in (c) a guard ring crossing and in (d) a contact to an electric linewidth structure. All images are taken on a test wafer at an angle of 45° where graphene is implemented as the SN layer.

All the pressure dependency measurements were performed by forcing a voltage over the Pirani sensor in contrast to the forced current in the analytical model. This is done since a voltage supply is more common as well as to reduce the risk of damaging the devices. The analytical model can not be rewritten analytically for a forced voltage due to the hyperbolic function in Equation 2.7. Therefore, the forced current is to be quantitatively derived from the measured resistance to verify the analytical model.

3.4. Bridge Material Parameter Measurements

The average sheet resistance $R_{\square}$ is determined by measuring the resistance of graphene strips and dividing by the aspect ratio of the strip. This results in 10.6 kΩ and 0.8 kΩ for the first and second batch respectively. This large difference of $\sim$ 13x has not been further investigated. It is assumed that it is caused by differences or variations in the fabrication process. It should therefore be checked after fabrication. Although the resistance of the graphene strips in the first and second batch is different, the sensitivity is comparable. However, the power consumption is $\sim$ 0.9mW and $\sim$ 8.5mW in the first and second batch respectively. This is significantly different and implies that the higher sheet resistance strips of the first batch are desirable in applications where power consumption is a constraint, as the power relates to I^2R. Wafer-scale measurements on three different structures on the mentioned test wafer result in a sheet resistance of 6.2 ± 0.8 kΩ. The measurement results of each die are depicted in appendix Figure C.3.

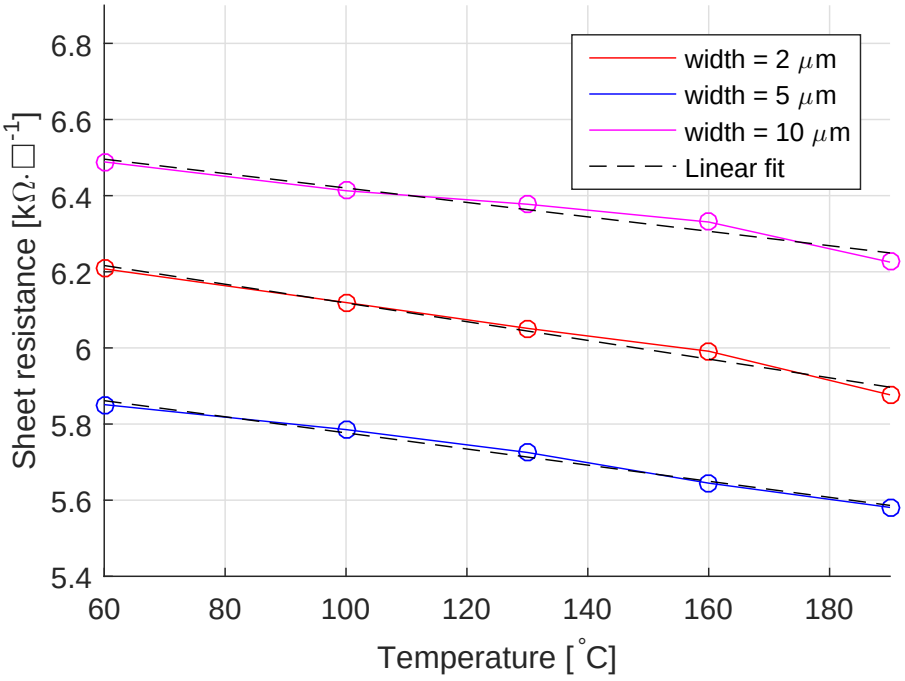


Figure 3.10: Graphene sheet resistance of non-suspended strips for five different temperatures. Three different strips are measured with variable width and length 206 μm. The difference between strips is $\sim$ 5 % and is considered due to process variations. A linear fit is included to determine the TCR.

The TCR ξ of graphene is determined on the aforementioned test wafer devices. The average sheet resistance is measured for five different temperatures and the results are depicted in Figure 3.10. The measurement results of each die and temperature are depicted in appendix Figure C.4-C.8. The devices are measured at low bias to minimize the effect of ohmic heating. The figure includes linear fits of which the largest fit error is 0.5 %. The TCR is therefore concluded to be constant for this temperature range. An average TCR value of $(-3.6 \cdot 0.5) \cdot 10^{-4}$ K^{-1} is found for the graphene strip, which matches values from literature [49].

The direct measurement of the thermal conductivity κ_b is considered out of the scope of this project. Unfortunately, no fit of the analytical model to the data is achieved. A larger data set with different geometries could provide a solution. The value of κ_b is therefore left undetermined for now, but literature suggests a κ_b of 1000 W·m^{-1}·K^{-1} for multi-layer graphene [49]. The analytical model can not be used to make predictions, due to the many uncertainties.

3.5. Conclusions

Two batches of graphene-based Pirani pressure sensors were released and characterized, leading to world's first graphene-based Pirani pressure sensors. The largest maximum resistance change observed was 2.8 % at a bias voltage of 15 V and a low power of 0.9 mW was achieved at a bias voltage of 9 V with maximum resistance change of 0.8 %. The second batch provided several different aspect ratio devices, with similar performance as the first

batch but with lower bias voltage and higher power consumption. The sheet resistance of graphene was found to differ significantly between processes. Raman spectroscopy revealed that the fabrication process itself does not damage the graphene. The geometry parameters are determined, as well as the TCR and sheet resistances. The thermal conductivity is left undetermined and no fit of the analytical model to the datasheet is achieved. With these results the additional research question is answered. It is indeed possible to fabricate an operational graphene-based Pirani sensor and it has comparable performance as current state-of-the art implementations. It has the advantage of miniaturization and the low power consumption that follows from this. Furthermore, the gap depth can be tuned to experiment with different operating ranges.

4

BICMOS Characterization

This chapter investigates the BICMOS proces and characterizes the graphene growth impact on the CMOS devices. For this purpose, a reference wafer without any graphene processes is fabricated, followed by an investigation on different IC materials in favor of a simpler process that includes graphene growth. Finally, the observations on the effect of a graphene growth step are given and these effects are then discussed in attempt to give the cause of the observed effects.

Before one is authorized to work with the equipment at EKL, a training has to be completed for each piece of equipment that will be used during the final processing run. It is decided to incorporate a training processing run in this project that covers the complete process flow and graphene test devices that will be used in the final processing run, while achieving new insights along the way. Eight wafers are used to investigate the graphene growth impact on the behavior of the CMOS devices as well as exploring difficulties in preserving the graphene during BEOL processing. The two main investigations are the effect of different graphene growth times on the CMOS devices and the effect of different IC materials and methods. The differences between the eight wafers are listed in Table 4.1. To characterize the BICMOS devices a test structure mask set that is available in EKL is used, including different sized NMOS and PMOS devices and Van der Pauw structures to determine the sheet resistance of the different layers. The wafer is split in two sets of dies in a checkerboard pattern, where one half is used for BICMOS and the other half for graphene test structures.

Table 4.1: Process differences of the eight BICMOS wafers used in the training run. The two main investigations are the effect of different graphene growth times on the CMOS devices and the effect of different IC materials and methods after graphene has been grown.

Wafer number	**Graphene growth**	**Interconnect**
1	10 minutes	AlSi
2	20 minutes	AlSi
3	40 minutes	AlSi
4	20 minutes	AlSi (lift-off)
5	20 minutes	AlSi (lift-off)
6	-	Mo
7	-	Ti
8	-	Al

It should be noted that the preservation of the Mo and graphene stack through the BEOL processing brings important limitations. The regular cleaning line to remove possible organic residues in nitric acid is no longer possible, as this rapidly etches Mo. The use of dry etching severely damages the graphene and should be avoided. Furthermore, the use of plasma to remove photoresist also etches the graphene. The removal of photoresist is therefore done in NMP near boiling temperature and general cleaning can be performed by acetone and isopropanol.

4.1. Training Run Reference Wafer

A reference wafer is processed completely according to the standard BICMOS fabrication process without a graphene growth step and AlSi is used as IC material. This reference wafer is wafer 8, of which the threshold voltages and sheet resistances are measured on wafer-scale. The wafer-scale measurements are performed in a *Cascade* probe station that supports automated measurements.

The threshold voltage measurement results are depicted in the wafermaps in Figure 4.1. This concerns test devices with channels that are 20 μm in width and 5 μm in length, which are used as a benchmark as the final design consists of devices with channel length 4 μm. The first observation is a clear distinction between the different wafer quadrants. This is caused by the difference in threshold voltage adjustment implantation described in Section 2.3.2. The lower right quadrant, that corresponds to the highest adjustment dose, is concluded to provide the most symmetric threshold voltages between NMOS and PMOS.

The second observation is the difference in threshold voltage between the quadrants. This difference is ~ 0.3 V and ~ 0.2 V for the NMOS and PMOS respectively, although the two lowest doped quadrants of the PMOS show a negligible shift. According to this trend a better symmetry is achieved for even higher adjustment doses. That investigation is considered out of scope for this project. Note that just a single device is broken. Measurements on devices with channels that are 20 μm in width and 2 μm and 10 μm in length are listed in appendix Figure D.2, with similar results. A channel length of 1 μm results in significant channel length modulation of the NMOS and the PMOS is a short circuit and are therefore not listed.

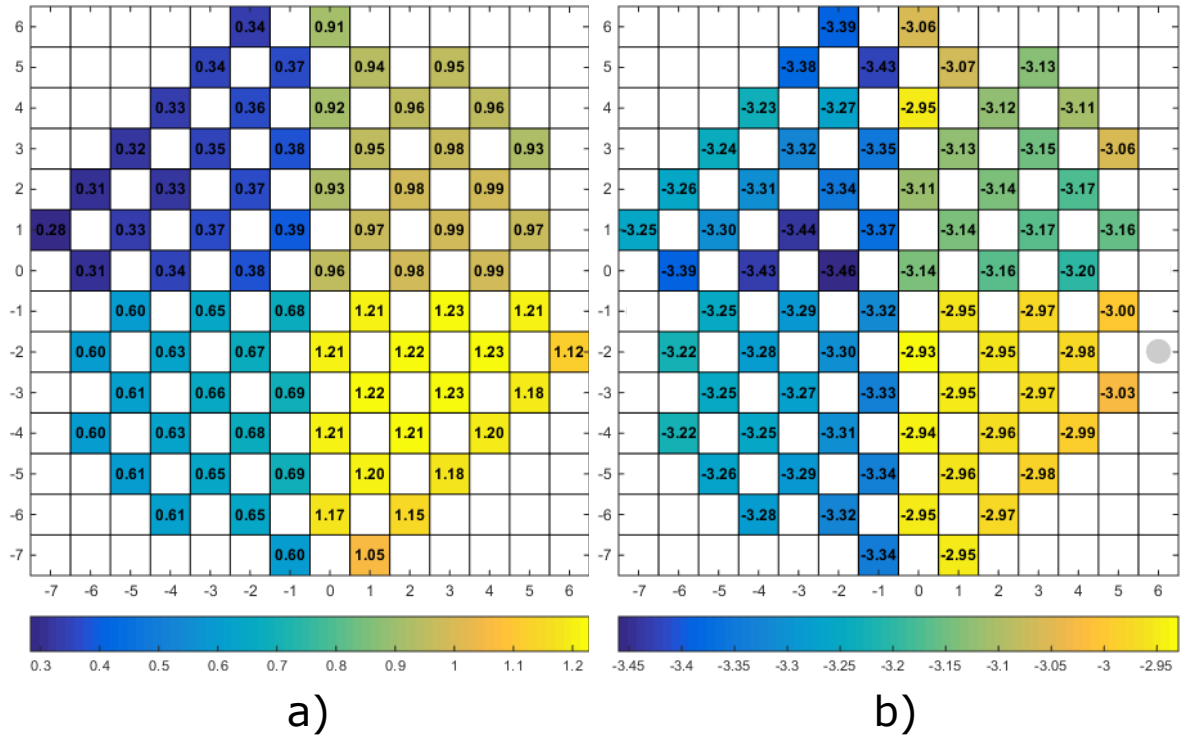


Figure 4.1: Wafermaps depicting threshold voltage [V] of 20x5 devices on wafer 8 with the V_{Tn} of NMOS devices in a) and the the V_{Tp} of PMOS devices in b). Broken devices are marked with a grey circle.

The sheet resistances of the IC, NW, SN and SP are measured using Van der Pauw structures present on the test design. The wafer-scale measurement results are listed in the wafermaps in appendix Figure D.3. Values of 0.1 Ω, 56 Ω and 92 Ω are found for the IC, SN and SP respectively with high uniformity over the wafer. The NW sheet resistance is dependent on the adjustment dose, as it is a lower implantation dose. The found threshold voltages and NW sheet resistances of each wafer quadrant are listed in Table 4.2.

Table 4.2: Threshold voltages and NW sheet resistances of all quadrants on the reference wafer in the training run. The wafer-scale measurement results are depicted in wafermaps in Figure 4.1 and appendix Figure D.3.

Adjustement dose	V_{Tn}	V_{Tp}	**NW**
0e11	0.35 V	−3.30 V	1.65 kΩ
3e11	0.65 V	−3.30 V	1.70 kΩ
6e11	0.95 V	−3.15 V	1.75 kΩ
9e11	1.20 V	−2.95 V	1.80 kΩ

4.2. Different Interconnect Materials and Processes

Different interconnect materials and processes are now investigated to determine the possibilities in the final fabrication run. The problem is that the graphene and Mo need to be preserved until the end of the fabrication process. This severely limits the possibilities of etch methods. However, if the metal layer can be implemented before the graphene growth, the wafer can be etched and cleaned regularly.

Wafer 7 is processed identically to the reference wafer, but with titanium (Ti) as the IC material. Some test results in the research group suggest that Ti has better a contact resistance to graphene [50]. Furthermore, the melting point of Ti is sufficiently high that it can withstand the graphene growth step, allowing it to be deposited before the graphene growth and can therefore be etched with regular methods. This can potentially simplify the integration of graphene. The threshold voltage measurement results are depicted in the wafermaps in Figure 4.2. Similarly to the reference wafer, a clear distinction between the different wafer quadrants is observed. The other device sizes with similar results are listed in appendix Figure D.4. The threshold voltage value of devices on wafer 7 is shifted significantly compared to the reference wafer by ~ -1.3 V and ~ -1.8 V for the NMOS and PMOS respectively.

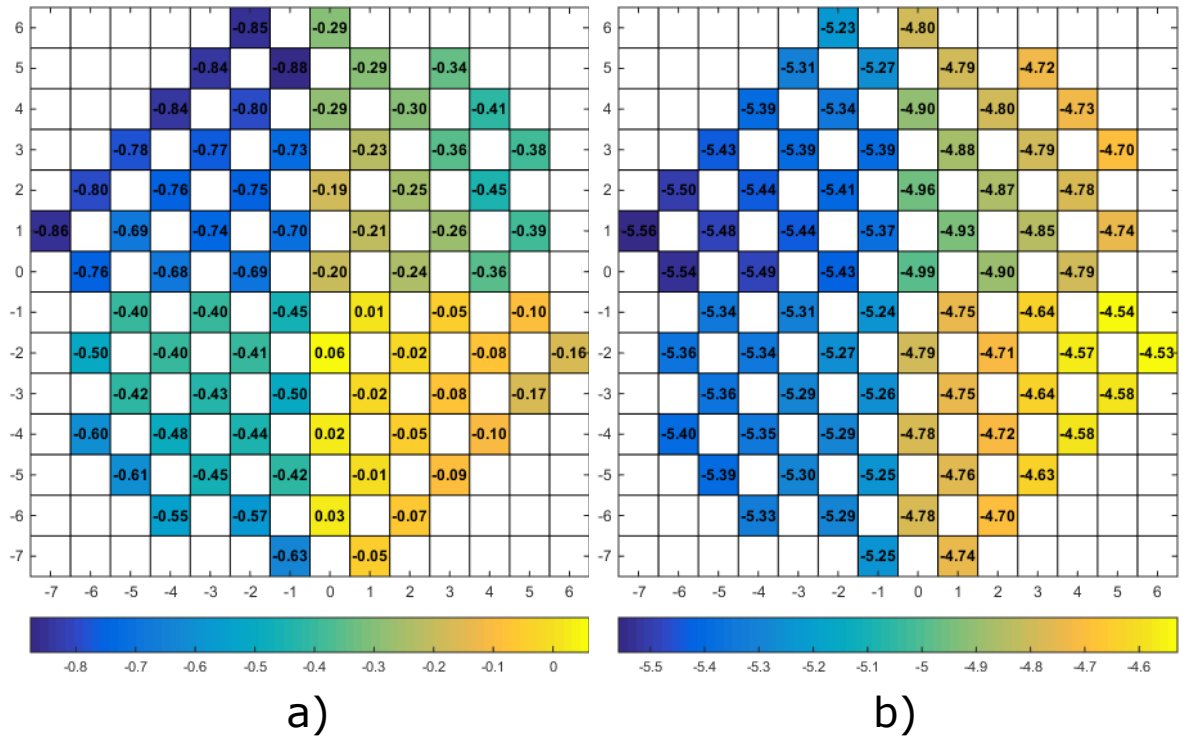


Figure 4.2: Wafermaps depicting threshold voltage [V] of 20x5 devices on wafer 7 with the V_{Tn} of NMOS devices in a) and the the V_{Tp} of PMOS devices in b).

Furthermore, the sheet resistance of the IC, NW, SN and SP is measured. The wafer-scale measurement results are listed int the wafermaps in appendix Figure D.5. The values found for the NW, SN and SP are similar to that of the reference wafer. The IC sheet resistance is higher, which is to be expected, and less uniform. From these results it is concluded that Ti IC severely shifts the threshold voltages while doped region sheet resistances remain equal and can therefore not be used as IC material. The exact cause is considered out of scope for this work.

However, the difference in Al and Ti work function is small and can therefore not be the reason. It is suspected that the Ti layer induces a lot of stress, which damages the gate oxide.

Wafer 6 is processed identically to the reference wafer, but with Mo as the IC material as it has a higher melting point than the graphene growth temperature. The threshold voltage measurement results are depicted in the wafermaps in Figure 4.3. Note that there are several broken devices at the wafer edge. This is due to non-uniform etching of Mo that results in Mo residue at the edge. Similarly to the reference wafer, a clear distinction between the different wafer quadrants is observed. The threshold voltage value of devices on wafer 7 is shifted significantly compared to the reference wafer with ~ 0.4 V and ~ -0.7 V for the NMOS and PMOS respectively. However, the threshold voltage differs significantly between devices sizes, of which the wafermaps are listed in appendix Figure D.6.

The sheet resistance of the IC, NW, SN and SP is again measured. The wafer-scale measurement results are listed in the wafermaps in appendix Figure D.7. The values found for the SN and SP are similar to that of the reference wafer. The IC and NW sheet resistance is higher. Considering the threshold voltage shift and dependency on device size as well as the increase of NW sheet resistance, it is concluded that Mo is not a suited IC material. However, a graphene growth test is performed nonetheless. During this test, just the temperature step of the graphene growth step without the actual carbon source gas is performed. After the growth step, no operating devices were measured. The concept of IC implementation before graphene growth step is therefore discarded.

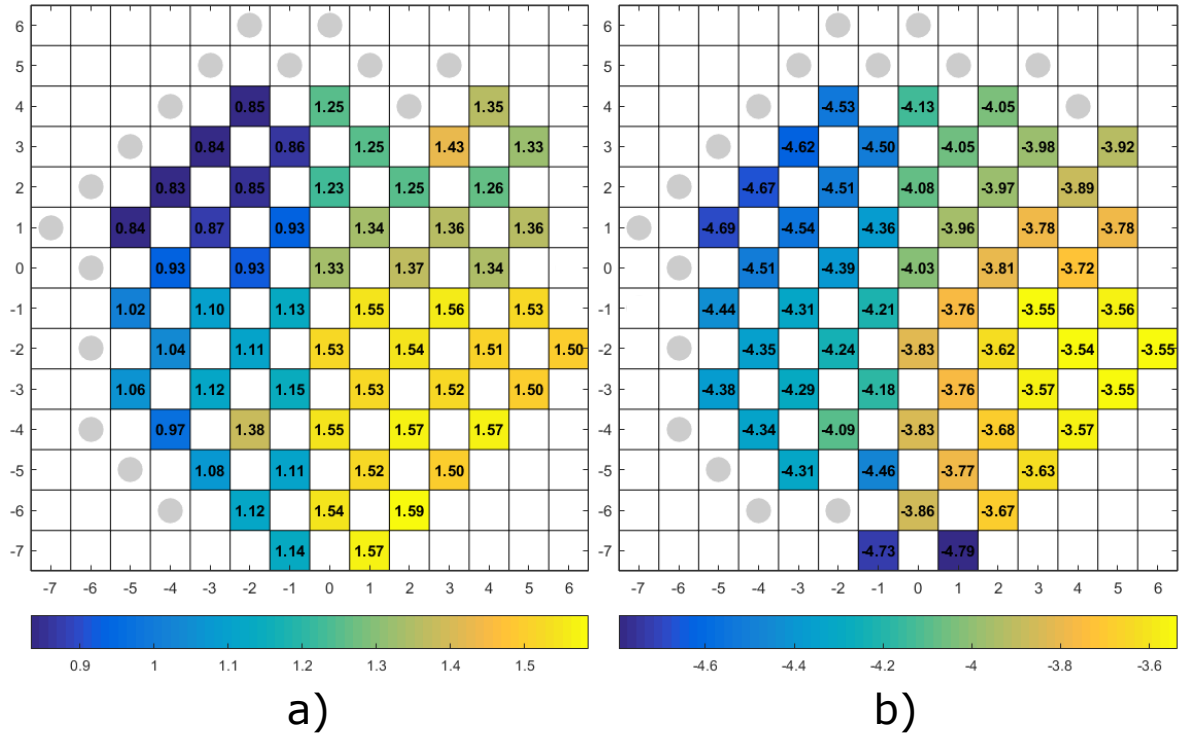


Figure 4.3: Wafermaps depicting threshold voltage [V] of 20x5 devices on wafer 6 with the V_{Tn} of NMOS devices in a) and the the V_{Tp} of PMOS devices in b). Broken devices are marked with a grey circle.

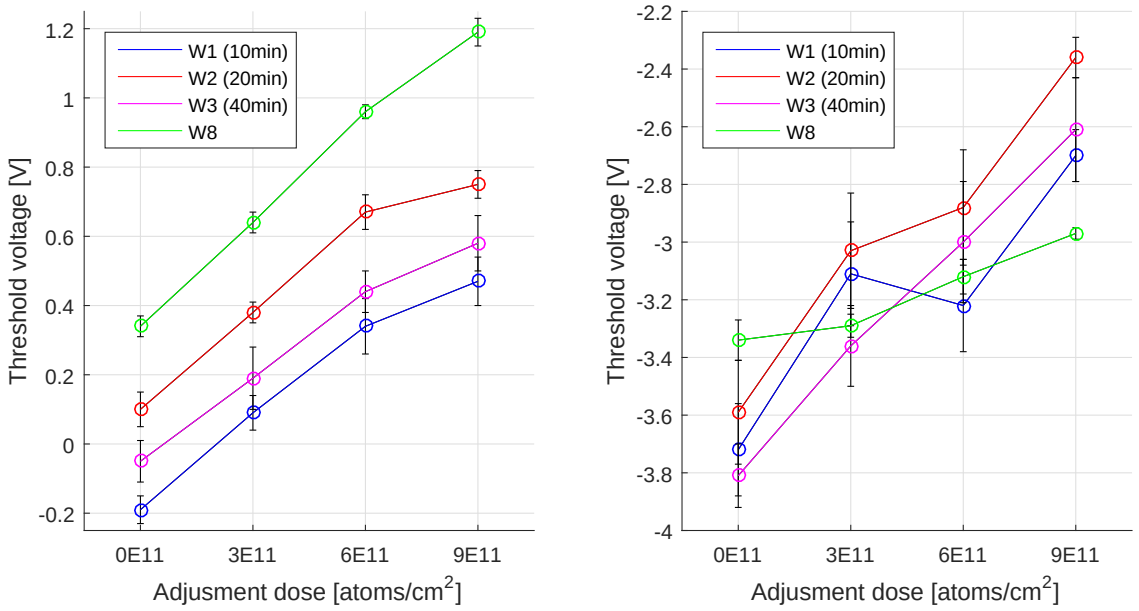
Since it is concluded to implement the IC after the graphene growth step, the possibilities for the implementation are limited. Both wet and dry etching are inconvenient as most methods also etch either the Mo or graphene. Possible solutions are covering the Mo and graphene stack before metal deposition or using a lift-off process. The test mask set allows for the investigation of the feasibility of a lift-off process with AlSi. A first try on performing lift-off with AlSi after graphene growth is done on wafer 4. Unfortunately, this wafer had no contact between the metal and silicon bulk which implies that no electrical measurements are listed. It is found that contact is made after applying a voltage of 20 V or higher. This suggest that there is native oxide in the contact openings. Moreover, the SEM images of the contacts listed in appendix Figure D.1 show no other possible causes for the broken contacts. Fortunately, AlSi contact to graphene was good and therefore this wafer was used in the TCR measurement in Section 3.4.

Wafer 5 is processed identically as wafer 4 with the exception of performing a twice as long native oxide removal prior to the metal sputter deposition. Unfortunately, the results are similar to that of wafer 4 which suggests that native oxide before metal deposition is not the cause. Lift-off with AlSi is concluded to not be feasible and therefore the Mo and graphene stack is covered before metal deposition to protect it. The layout design requires a mask that can be used to cover and protect the Mo and graphene stack during the first metal deposition stage.

4.3. Effect of Graphene Growth on BICMOS Characteristics

The effect of graphene growth on the BICMOS process is investigated on wafers 1, 2 and 3 by performing different graphene growth times that are listed in Table 4.1. Due to a copper contaminated reactor in which the graphene growth takes place, many processing steps after the graphene growth are manual. The first step after graphene growth is the CO implementation. This was performed by wet etching with BHF which etches SiO_2 and not Mo or graphene. Unfortunately, wet etching resulted in a residue that could only be removed by long dry etching. The long exposure to plasma hardens the photoresist, which could then only be removed by an oxide plasma from which is concluded that dry etching the CO is a necessity in the final integration run. The test mask set exposes the graphene during the CO etch step, as a result the graphene is stripped of the wafers to be able to measure the CMOS devices. The final design will not expose the graphene during the CO implementation.

The wafer-scale measurements of the threshold voltage of the 20x5 devices on wafers 1, 2 and 3 are listed in appendix Figure D.8 and Figure D.9. The other device sizes with similar results are listed in appendix Figure D.10-D.12. On behalf of readability, the mean value of each quadrant of each wafer including the reference is taken and plotted in Figure 4.4 where the bars correspond to the standard deviation. Several observations are made from these results. Firstly, the threshold voltage shifts as result of the graphene growth step, but the longest time does not correspond with the largest shift. Secondly, the slope in Figure 4.4 caused by the voltage adjustment doses remains equal for NMOS devices, but increases for PMOS devices. Furthermore, the highest adjustment dose has a reduced effect on the wafers that underwent the graphene growth step. These observations hold for the other device sizes. The effect of the adjustment doses for the PMOS devices on wafer 1 show a deviating step between 3E11 and 6E11. It is concluded that a growth time of 20 minutes results in the most symmetrical threshold voltages in the 9E11 quadrant and will therefore be used in the final fabrication run.



(a) NMOS. (b) PMOS.

Figure 4.4: Mean threshold voltages in each quadrant of wafers 1, 2, 3 and 8 where the bars correspond with the standard deviation. Results of NMOS 20x5 devices in (a) and PMOS 20x5 devices in (b).

The wafer-scale measurements of the sheet resistances on wafers 1, 2 and 3 are listed in appendix Figure D.13-D.15. The mean value of each sheet resistance on each wafer including the reference is taken and plotted in Figure 4.5 where the mean in the 0E11 quadrant is taken for the NW and the bars correspond with the standard

deviation. The IC and NW sheet resistances are constant, while the SN and SP sheet resistances have reduced after graphene growth. The difference in sheet resistance between wafers 1, 2 and 3 is negligible.

All measured wafers use the same IC material and thickness, which naturally results in equal sheet resistance. The NW doped region is activated at ~ 1150 °C for 4 $l$hours and the graphene growth occurs at ~ 915 °C. This significantly lower temperature has no noticeable effect on the NW doped region activation. However, the SN and SP doped regions are activated during the gate oxidation which takes place at ~ 1000 °C for 10 min. It is therefore concluded that the SN and SP regions are activated further during the graphene growth step, as this explains the decrease in $R_{\square}$. The thermal oxidation can be too short to activate all carriers. The growth time does not make a large difference, which suggests that the doped regions are maximally activated during the graphene growth step.

The additional dopant activation accounts for the equal change in sheet resistance, but it does not explain the different threshold voltage shifts nor the change in adjustment dose effect. The threshold voltage is therefore investigate further in the next section.

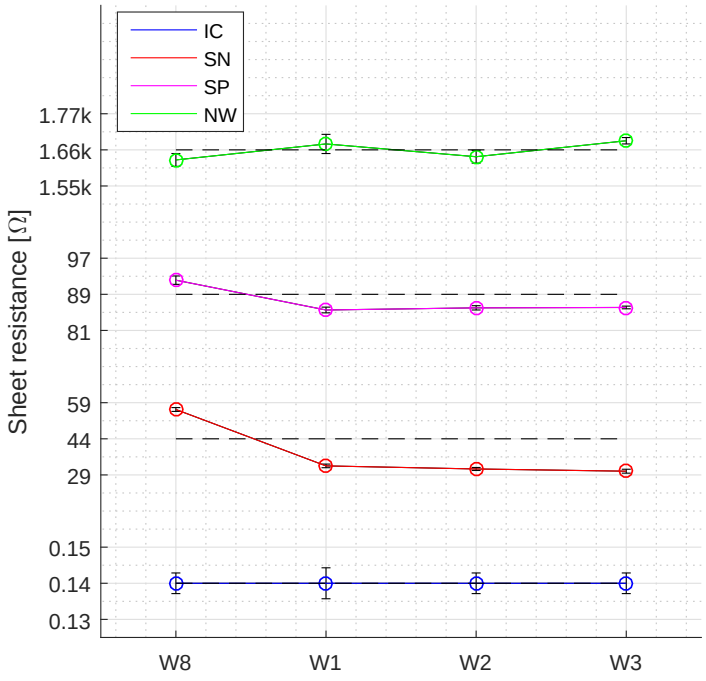


Figure 4.5: Mean sheet resistance of the IC, NW, SN and SP on wafers 1, 2, 3 and 8 where the bars correspond with the standard deviation.

4.4. Analysis of the Effects of Graphene Growth on the Threshold Voltage

The equations for the threshold voltage described in Section 2.3.2 are used to investigate which parameter is responsible for the observed shift in threshold voltage. The equations have three undetermined parameters that are determined by the fabrication process, which are the density of doped carriers in the channel N_a or N_d in [cm^{-3}], the gate material thickness t_{ox} in [cm] and the fixed charge for surface states Q_{fc} in [C·cm^{-2}]. The gate oxide is ~ 15 nm less for the graphene processed wafers due to a non-selective Mo etch step, but the effect on the threshold voltage is negligible. This means that there are just two candidates left.

The density of doped carriers N_a and N_d is determined by simulations in *TSUPREM* and *MEDICI*. Unfortunately, the device simulations in this software did not comply with the performed measurements with regards of threshold voltage. However, these simulations are used here make estimations for N_a and N_d which are listed in Table 4.3.

The extra temperature step of the graphene growth step does not impact the value of N_a according to the simulation, but it does change N_d significantly.

Table 4.3: List of estimations for N_a and N_d extracted using *TSUPREM* and *MEDICI*.

Adjustment dose [cm^{-2}]	**N_a [cm^{-3}]**	**N_d [cm^{-3}]**	**N_d [cm^{-3}]** (after graphene growth)
0E11	1.00E16	1.45E16	1.45E16
3E11	1.29E16	1.28E16	1.12E16
6E11	1.95E16	1.00E16	0.95E16
9E11	2.40E16	0.79E16	0.21E16

The fixed charge for surface states Q_{fc} is difficult to measure, but theoretical estimates exist [48]. These estimates are depicted in Figure 4.6, which are given in cm^{-2} by dividing by the electron charge q. Estimations of the Q_{fc} are made by interpolating the curves in Figure 4.6 at the reported threshold voltage measurement results and corresponding simulated density of doped carriers. Note that Q_{fc} is named Q_{ss} in the figure. For the reference wafer the fixed charge for surface states is estimated to be lower then 10^{11} cm^{-2}. This value is $\sim 4 \cdot 10^{11}$ cm^{-2}, $\sim 10^{11}$ cm^{-2} and $\sim 2 \cdot 10^{11}$ cm^{-2} for wafers 1, 2 and 3 respectively.

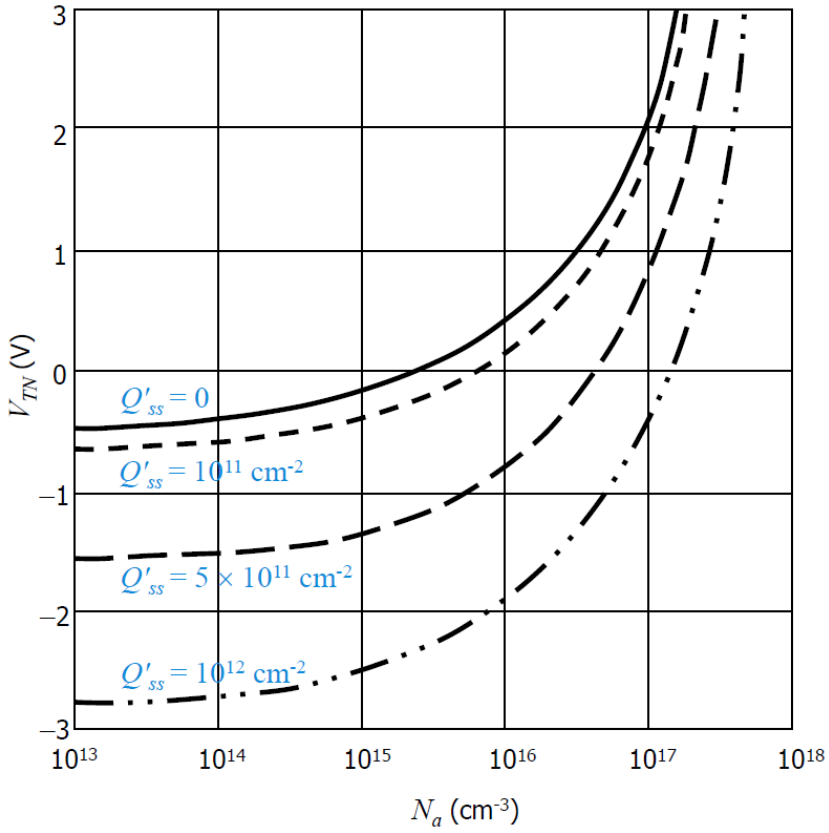


Figure 4.6: Theoretical relation between the threshold voltage V_T and the density of doped carriers N_a of an NMOS device for different values of the fixed charge for surface states Q_{fc} [48].

Furthermore, the Q_{fc} is calculated for both the NMOS and PMOS devices by using the measured threshold voltage and estimated density of doped carriers of wafers 1, 2, 3 and the reference which results in Figure 4.7. The reference results show a mean value for the Q_{fc} over the entire wafer for both NMOS and PMOS of $\sim 4.2 \cdot 10^{11}$ cm^{-2}. The NMOS results of the other wafers show values of $\sim 5.6 \cdot 10^{11}$ cm^{-2}, $\sim 4.8 \cdot 10^{11}$ cm^{-2} and $\sim 5.4 \cdot 10^{11}$ cm^{-2} for wafers 1, 2 and 3 respectively. The PMOS results are in the same range but show large deviations between quadrants.

The calculated values for the Q_{fc} are higher than the estimations made from the theoretical curve. Together with the observation of the non-constant value for the PMOS devices and the poor agreement of the model used to estimate the density of doped carriers, it is concluded that the density of doped carriers is different in reality. The

investigation on the exact cause is considered out of scope for this project, but two possibilities are given here. Firstly, the non-selective Mo etch step roughens up the gate oxide which increases the area responsible for the Q_{fc}. Secondly, the methane gas used in the graphene growth decomposes at the Mo surface in hydrogen and carbon. Charged hydrogen or carbon atoms could get trapped in the amorphous gate oxide.

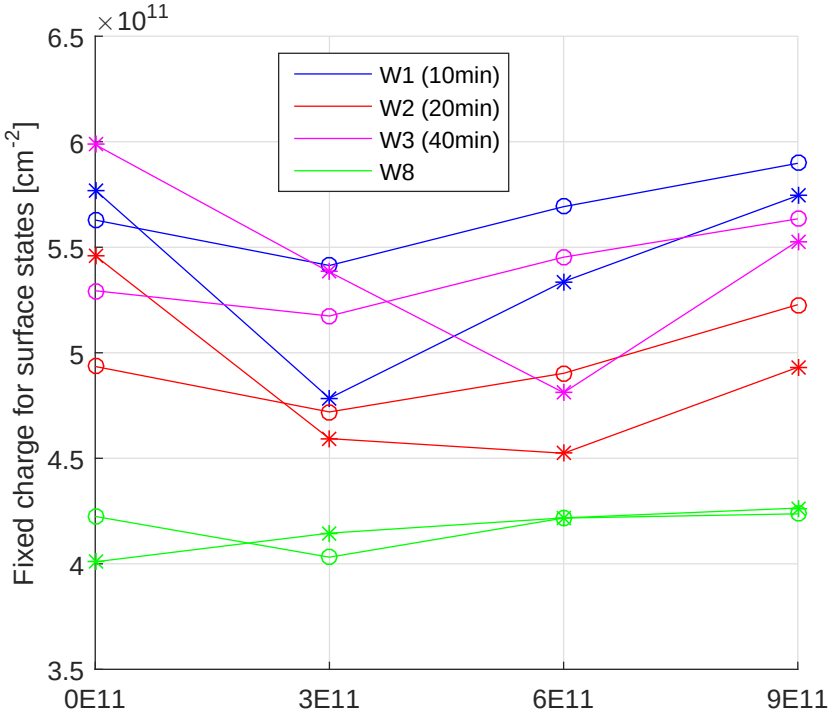


Figure 4.7: Calculated fixed charge for surface states of wafers 1, 2, 3 and the reference derived from both NMOS and PMOS devices. The NMOS results are marked with a "o" and the PMOS results with a "*". The calculation is based on rough estimates of N_a and N_d.

4.5. Conclusions

The threshold voltage adjustment doses result in distinct differences in threshold voltage in each wafer quadrant. On the reference wafer it is concluded that the most symmetric threshold voltages are found in the lower right quadrant, that has a adjustment dose of 9e11. The sheet resistance of the doped regions is highly uniform on the reference wafer. Different IC materials and methods are investigated and unfortunately all had negative results. As a consequence the IC is not implemented prior to the graphene growth by using Ti or Mo, nor is lift-off with AlSi performed after graphene growth. The remaining solution is to protect the Mo and graphene stack by covering it during the first metal layer implementation. Different graphene growth times are performed to investigate the effects on the BICMOS devices. Due to the inability of implementing the IC while keeping the Mo and graphene stack, it was decided to strip the graphene after the graphene growth. The processing steps required to implement graphene shifted the threshold voltage of the CMOS devices towards more negative values. The growth time does have a significant effect and 20 minutes is concluded to give the best results. The SN and SP sheet resistance drop as result of the graphene growth and it is concluded that this is caused by dopant activation. Estimations of the density of doped carriers were made to find the cause of the threshold voltage shift, but the results were different from the theoretical curve. Nonetheless it is concluded that the fixed charge of surface states changes as result of the graphene growth steps and shifts the threshold voltages.

5

Read-Out Electronics and Complete Layout Design

In this chapter the electrical circuit design is discussed. A schematic overview of the the block diagram of the design is illustrated in Figure 5.1. The four blocks depict the graphene-based sensor topology, differential amplifier, 4-bit analog-to-digital converter (ADC) and biasing block. The latter is placed off chip to allow changes to the bias when process differences with the simulations are encountered. The other three blocks are on chip and discussed in the sections below. The electric design, simulation and layout design of the amplifier and ADC is done in *Cadence Virtuoso*. The final layout layers are added in *L-Edit*. The models for the BICMOS devices derived by Zahra Kolahdouz Esfahani [45] are used in simulation with corresponding threshold voltages of $V_{tn} = 2.1$ V and $V_{tp} = -3.2$ V and analog CMOS devices with channel width of 400 μm and length of 4 μm.

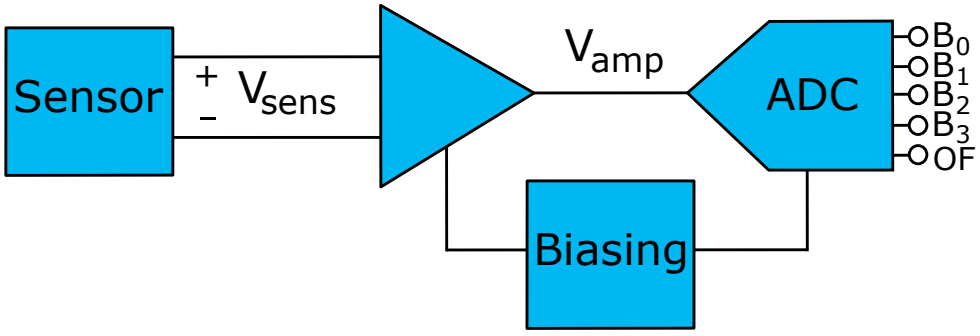


Figure 5.1: Block diagram of the sensor with read-out electronics circuit design.

5.1. Sensor Read-Out Topology

The sensing element in the design is a resistor. A common topology to measure the change in resistance is with a Wheatstone bridge, which output is a differential voltage. This topology has a quarter, half or full bridge version. However, only a quarter or half bridge can be used as a full bridge requires resistor pairs of which one increases and the other decreases in resistance. The half bridge has a higher sensitivity than the quarter bridge and is therefore used in this design, although the fabrication of two graphene-based Pirani pressure sensors in one sensor might decrease the fabrication yield or cause mismatch errors.

The half Wheatstone bridge topology is illustrated in Figure 5.2 with supply voltage V_{DD}, outputs V_+ and V_-, the additional non-suspended graphene resistance between Pirani and metal contact R_A, pressure dependent conductive bridge resistance $R(p)$ and non-suspended graphene with equal geometry as the suspended counterpart R_0. The contact resistance to the graphene R_C can typically be ignored with respect to $r_{\square}$. The Wheatstone bridge output V_{sens} is given in Equation 5.1. The supply voltage is set at 15 V to provide a ~ 7.5 V drop over the resistances, which is equal to the applied voltage during measurements on the second batch of graphene-based Pirani pressure sensors. A change Δ of $R(p)$ translates to $\sim (\Delta/2)V_{DD}$ when neglecting R_A. The maximum measured change in resistance of 2.8 % in the second batch therefore results in a maximum value of ~ 0.2 V for V_{sens}.

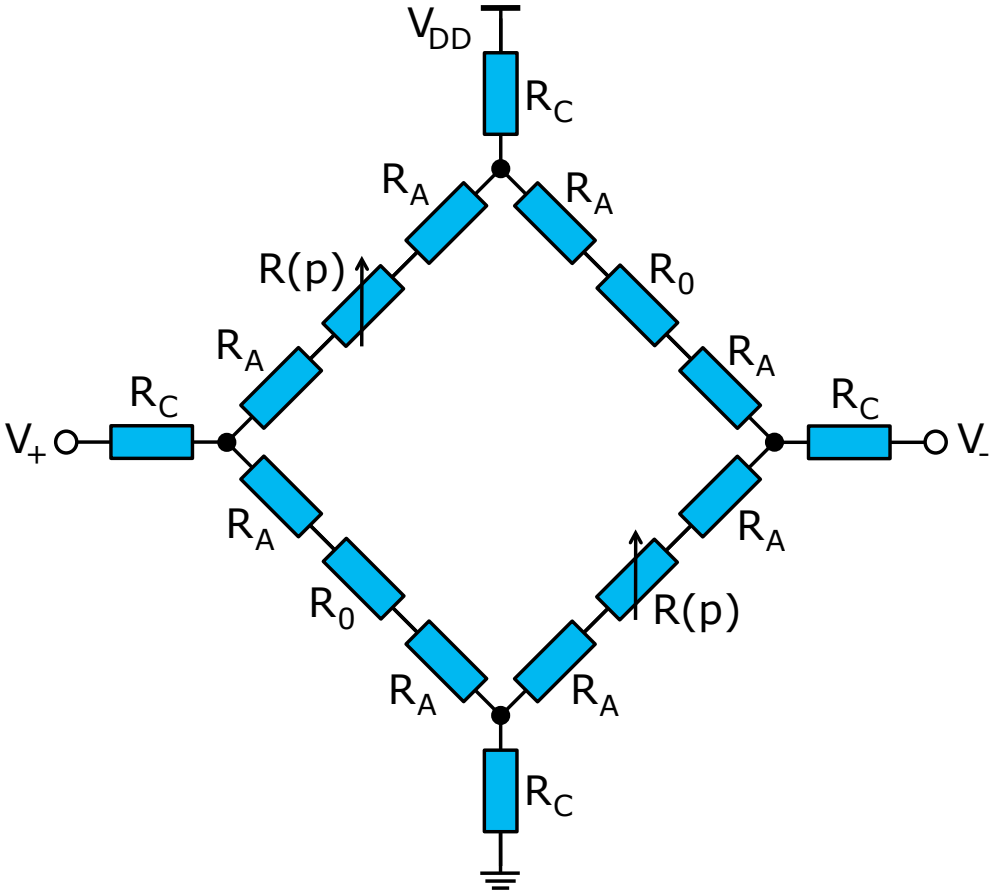


Figure 5.2: Wheatstone half bridge topology with supply voltage V_{DD}, outputs V_+ and V_-, contact resistance to the graphene R_C, additional non-suspended graphene resistance between Pirani and metal contact R_A, pressure dependent conductive bridge resistance $R(p)$ and non-suspended graphene with equal geometry as the suspended counterpart R_0.

$$V_{sens} = V_+ - V_- = \frac{R_0 - R(p)}{4R_A + R_0 + R(p)} V_{DD} \tag{5.1}$$

The temperature increase of suspended and non-suspended graphene can be determined quantitatively to determine the quality of the Wheatstone bridge design. All resistances are subjected to temperature rise due to ohmic heating, which are defined by Equation 5.2 similarly to the definition given in the analytical model in Equation 2.6. Note that $\bar{u}_1$ and $\bar{u}_2(p)$ are the average temperature increase of the non-suspended and suspended graphene strip respectively and that geometry parameters l, L and w as defined in Figure 3.5 are used.

$$\begin{aligned} R_A &= R_\square \frac{l-L}{w}\left(1 + \xi \bar{u}_1\right) \\ R_0 &= R_\square \frac{L}{w}\left(1 + \xi \bar{u}_1\right) \\ R(p) &= R_\square \frac{L}{w}\left(1 + \xi \bar{u}_2(p)\right) \end{aligned} \tag{5.2}$$

The nodal equations are derived for the output nodes V_+ and V_- and solved for $\bar{u}_1$. The result is given in Equation 5.3. This gives two equations with two undetermined parameters, which are $\bar{u}_1$ and $\bar{u}_2(p)$. However, due to symmetry they can not be equated to find those parameters. A third equation is required.

$$\begin{aligned} V_+ : \quad \bar{u}_1 &= \frac{1}{\xi} \frac{LV_+}{lV_{DD} - (2l - L)V_+}\left(1 + \xi \bar{u}_2(p)\right) - \frac{1}{\xi} \\ V_- : \quad \bar{u}_1 &= \frac{1}{\xi} \frac{L(V_{DD} - V_-)}{(2l - L)V_- - (l - L)V_{DD}}\left(1 + \xi \bar{u}_2(p)\right) - \frac{1}{\xi} \end{aligned} \tag{5.3}$$

The equivalent resistance of the bridge is used in combination with Ohm's Law to find the third equation that is required. The result is given in Equation 5.4 which again gives an equation with the undetermined parameters $\bar{u}_1$ and $\bar{u}_2(p)$. These can be used to determine the ratio of temperature increase between suspended and non-suspended graphene in the design.

$$\bar{u}_1 = \frac{1}{\xi}\frac{1}{2l-L}\frac{2wV_{DD}}{R_{\square}I_{DD}} - \frac{1}{\xi}\frac{L}{2l-L}\left(1+\xi\bar{u}_2(p)\right) - \frac{1}{\xi} \tag{5.4}$$

5.2. Amplifier Circuit Design

The output voltage of the sensor circuit V_{sens} is amplified before it is read out. A voltage-to-voltage differential amplifier topology is used to achieve this. This topology is depicted in Figure 5.3, where resistors R_1, R_2, R_3 and R_4 determine the closed loop gain. Note that the voltage supply is V_{CC}, which is 10 V and not equal to V_{DD}. The amplifier input is redefined as $V_{sens} = V_{cm} \pm V_d$ where V_{cm} is the common-mode voltage of 7.5 V and V_d the differential signal. The estimated maximum value for V_{sens} is ~ 0.2 V which implies that the maximum V_d is ~ 0.1 V The output voltage V_{amp} is calculated by Equation 5.5.

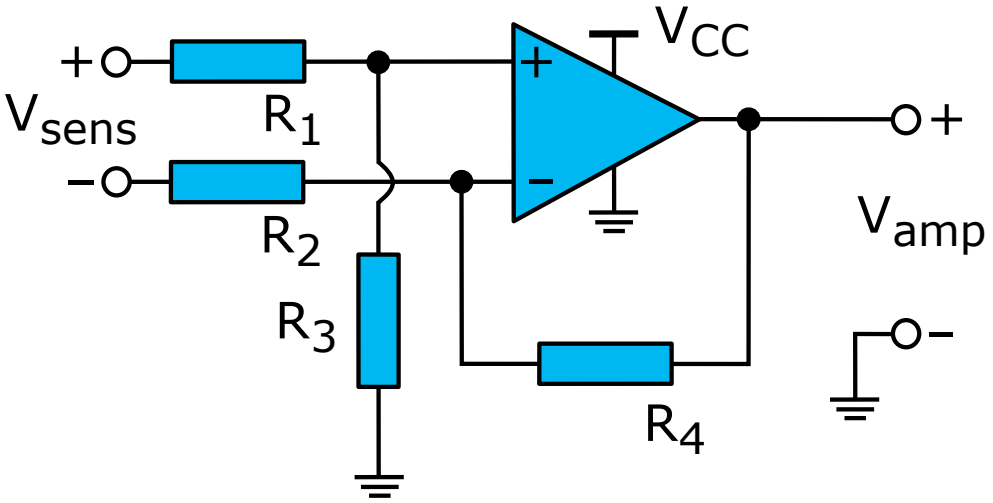


Figure 5.3: Differential voltage-to-voltage amplifier topology with the sensor output V_{sens} as input and V_{amp} as output. Resistors R_1, R_2, R_3 and R_4 determine the closed-loop gain.

$$V_{\text{amp}} = \left(\frac{R_3}{R_1+R_3}\cdot\frac{R_2+R_4}{R_2}\right)(V_{\text{cm}}+V_{\text{d}}) - \frac{R_4}{R_2}(V_{\text{cm}}-V_{\text{d}}) \tag{5.5}$$

It is not desired to have the common mode voltage V_{cm} in the transfer function. Equation 5.5 is rewritten by taking $R_1 = R_2$ and $R_3 = R_4$ which results in Equation 5.6 that only contains the differential signal V_d. Due to the definition of the input terminals the differential signal V_{sens} can be substituted for $2V_d$.

$$V_{\text{amp}} = 2\frac{R_3}{R_1}V_{\text{d}} = \frac{R_3}{R_1}V_{\text{sens}} \tag{5.6}$$

Resistors R_1, R_2, R_3 and R_4 are placed off chip to allow for flexibility in the gain, which implies that just the operational amplifier is to be designed on chip. In this research project the focus is not on creating an optimal design specifically tailored for the application. Instead, it is desired to use a robust and well known design to increase the chance on a working implementation. It is therefore chosen to use the a folded cascode opamp (FCO) as it is the most popular CMOS operational amplifier [51]. The FCO has a differential input and a common-mode rejection, which is required in the used topology. Furthermore, the FCO has a high voltage gain, large output voltage swing and only two poles in the Bode plot. However, it does not have a large current gain to drive the output. The circuit diagram of the FCO is illustrated in Figure 5.4 with supply voltage V_{CC}, ground V_{SS}, input terminals V_+ and V_-, output terminal V_{out} and bias terminals V_{b0}, V_{b1} and V_{b2}. Note that all CMOS device bulk connections are connected to V_{SS} and V_{CC} for NMOS and PMOS respectively.

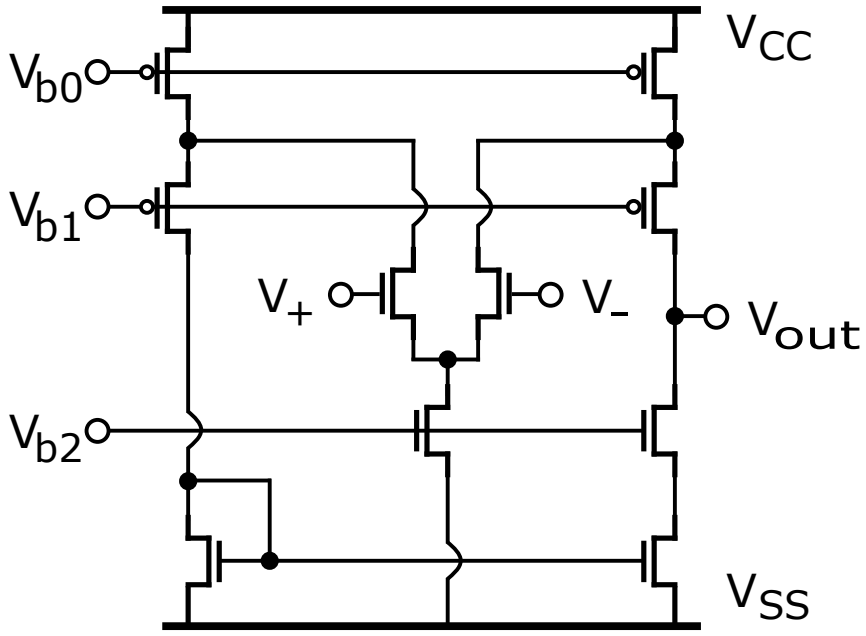


Figure 5.4: The FCO circuit diagram with supply voltage V_{CC}, ground V_{SS}, input terminals V_+ and V_-, output terminal V_{out} and bias terminals V_{b0}, V_{b1} and V_{b2}.

The FCO is simulated by connecting it to a load of 10 MΩ with 100 pF in parallel which represents the high impedance input of the ADC. The first design step is finding correct bias voltage values for V_{b0}, V_{b1} and V_{b2}. An initial guess is used as starting point where V_{b0} is $V_{CC} - V_{Tp}$, V_{b1} is $V_{CC} - 2V_{Tp}$ and V_{b2} is V_{Tn}. DC sweeps are performed for all three bias voltages independently, while the derivative of the output current is monitored. The maximum of the derivative of the output current curve indicates the desired value of the respective bias voltage of which an example is depicted in Figure 5.5. The found bias voltage values are 6.8 V, 5.5 V and 1.8 V for V_{b0}, V_{b1} and V_{b2} respectively.

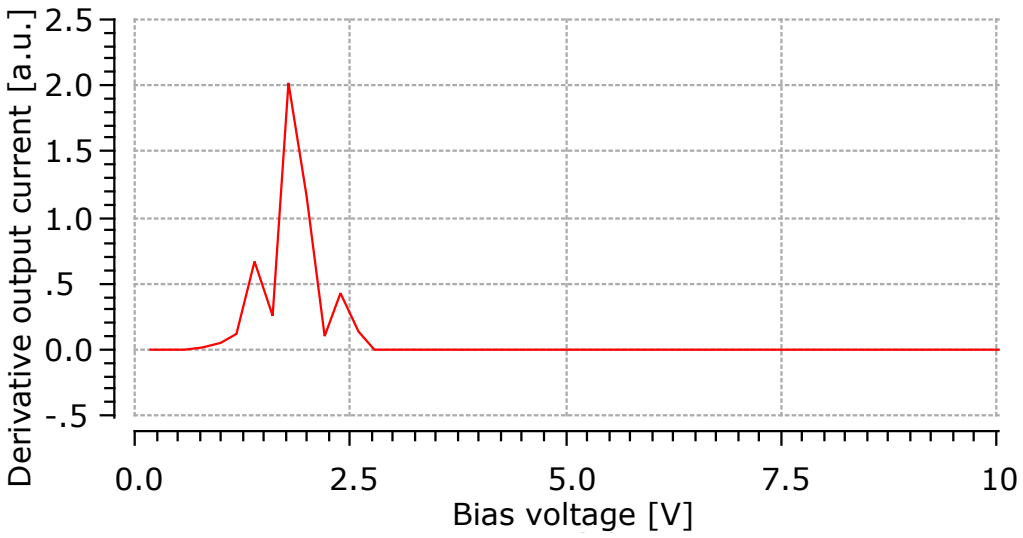


Figure 5.5: The derivative of the output current as function of the bias voltage V_{b2}. The maximum indicates the desired bias voltage value.

It is desirable to use the entire output range of the amplifier. Since the maximum input voltage is ~ 0.2 V and the maximum output voltage is 10 V the FCO should have a closed-loop gain of ~ 34 dB. The bandwidth is of less importance as the pressure dependency measurements are at constant pressure steps. AC analysis of the open-loop voltage gain is performed and the result is depicted in Figure 5.6. The open-loop voltage gain is ~ 28 dB with a bandwidth of ~ 0.5 kHz. The found gain is too low to be able to use the entire output range of the amplifier.

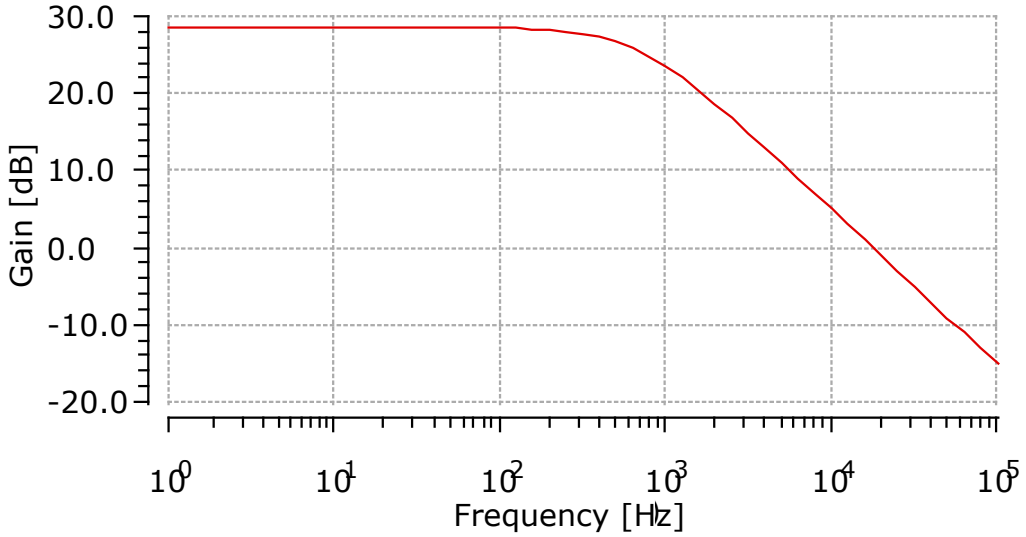


Figure 5.6: AC analysis of the open-loop voltage gain of the FCO with the gain results in dB.

DC analysis of the open-loop voltage gain is performed to investigate the offset and linearity. The result is depicted in Figure 5.7 and shows a linear open-loop gain upto an input voltage of ~ 0.25 V, which corresponds to an output voltage of ~ 7.8 V. Furthermore, the offset output voltage is ~ 1.15 V. A gain of 40 dB or an offset of 0.35 V is achieved by changing the bias voltage values, but this affects the gain linearity since the bias voltages are no longer at the optimum values.

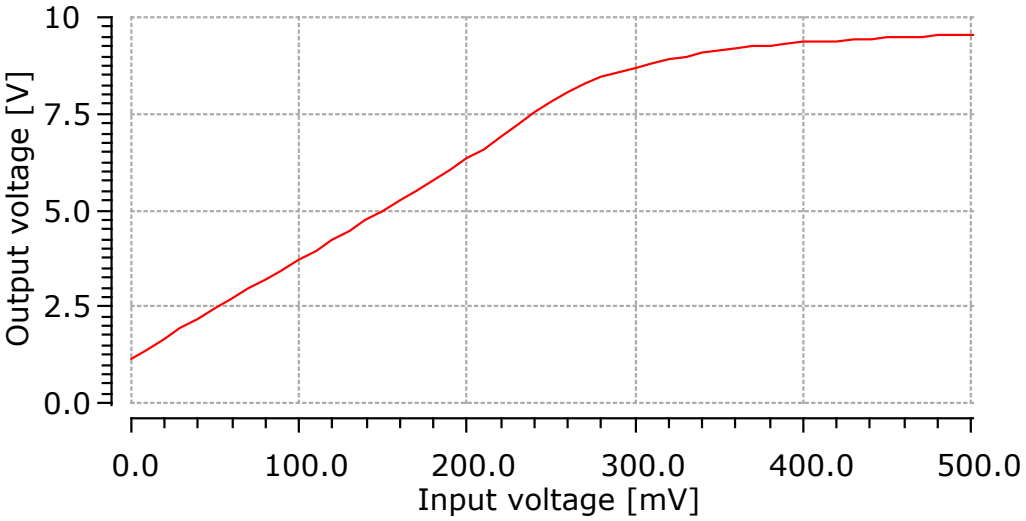


Figure 5.7: DC analysis of the open-loop voltage gain of the FCO from which the offset and linearity are derived.

Unfortunately, when the FCO is used as the operational amplifier in Figure 5.3 it is unable to supply the required current to drive the feedback network as it has a low current gain. A possible solution is to buffer the output with a source follower (SF), which does have a large current gain. The circuit diagram of the used SF is depicted in Figure 5.8 which is a two stage amplifier with unity voltage gain. The first stage is a differential pair and the second stage is a common drain stage and terminals V_{b0} and V_{b1} are used to bias the SF. The bias voltage range for which the SF operates is relatively large and the found optimum values are 4.6 V and 6.7 V for V_{b0} and V_{b1} respectively. AC analysis of the unity voltage gain of the SF is depicted in appendix Figure E.1 and is ~ 1.03 with a bandwidth of 1 kHz. The deviation of 3 % from unity gain is considered good enough. DC analysis of the open-loop voltage gain is depicted in appendix Figure E.2 which shows a linear open-loop gain over the entire output range and an offset of ~ 0.25 V.

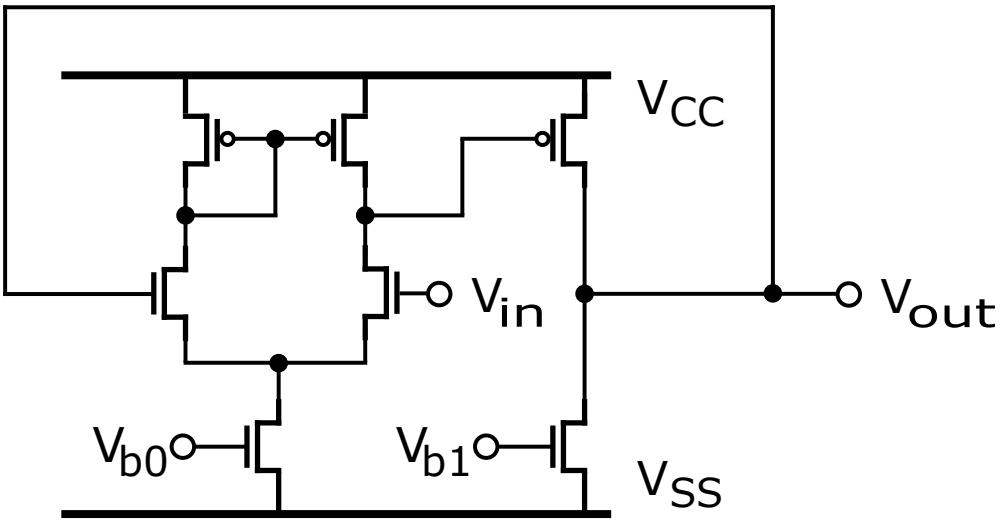


Figure 5.8: The SF circuit diagram.

The FCO and SF are now connected in series as illustrated in Figure 5.9 and simulated again. The bias voltages of the SF are changed to 8.0 V and 3.9 V for V_{b0} and V_{b1} respectively to obtain the output range that is reached by the FCO. AC analysis of the open-loop voltage gain is depicted in appendix Figure E.3 and shows a gain of ~ 32 dB with a bandwidth of ~ 80 kHz. Both the AC gain and the bandwidth have increased significantly compared to just the FCO. Unfortunately, the required closed-loop voltage gain of 34 dB is not reached. Settling for a slightly lower closed-loop gain is acceptable, but stills requires an open-loop gain of several order higher to achieve a stable closed-loop gain. DC analysis of the open-loop voltage gain is depicted in appendix Figure E.4 and shows a linear gain range upto an output of ~ 8.0 V and an offset of ~ 1.2 V.

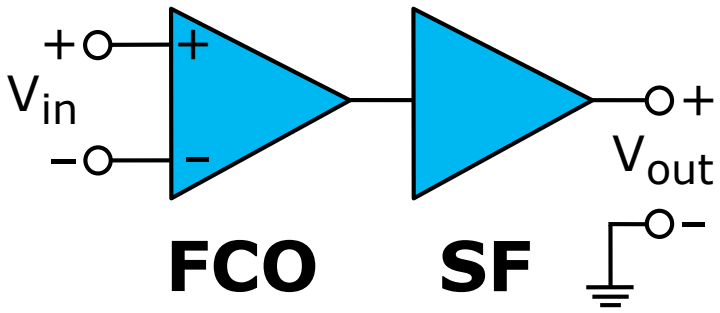


Figure 5.9: Connection diagram of the FCO and SF combination.

The FCO and SF combination is cascaded with another FCO and SF combination as illustrated in Figure 5.10. Note that the additional voltage terminal V_{tune} is added which compensates for the offset caused by the first FCO. AC analysis of the open-loop voltage gain is depicted in appendix Figure E.5 and shows a gain of ~ 69 dB with a bandwidth of ~ 60 kHz which fulfills the requirements. DC analysis is depicted in appendix Figure E.6 and shows an output range of ~ 8.0 V and offset of ~ 0.1 V although the gain linearity is not good.

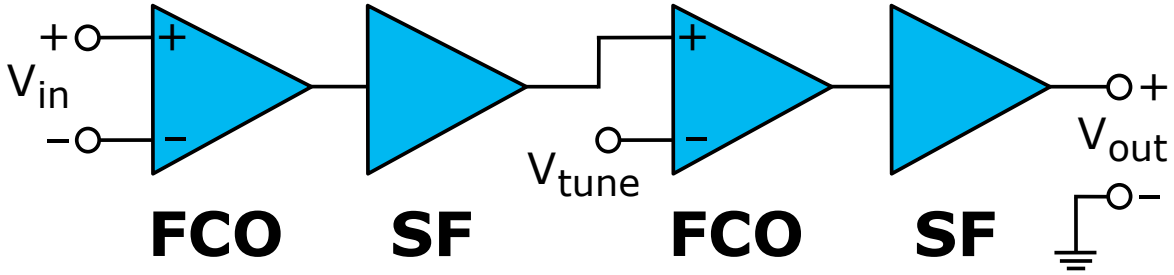


Figure 5.10: Connection diagram of the cascaded FCO and SF combination.

The opamp is now used with feedback resistor values $R_1 = R_2 = 5$ kΩ and $R_3 = R_4 = 200$ kΩ which sets a closed-loop gain of ~ 32 dB. AC analysis results are depicted in Figure 5.11 and shows a closed-loop gain of ~ 31.9 dB with a bandwidth of 200 kHz. The 0.4 % lower closed-loop gain is considered acceptable.

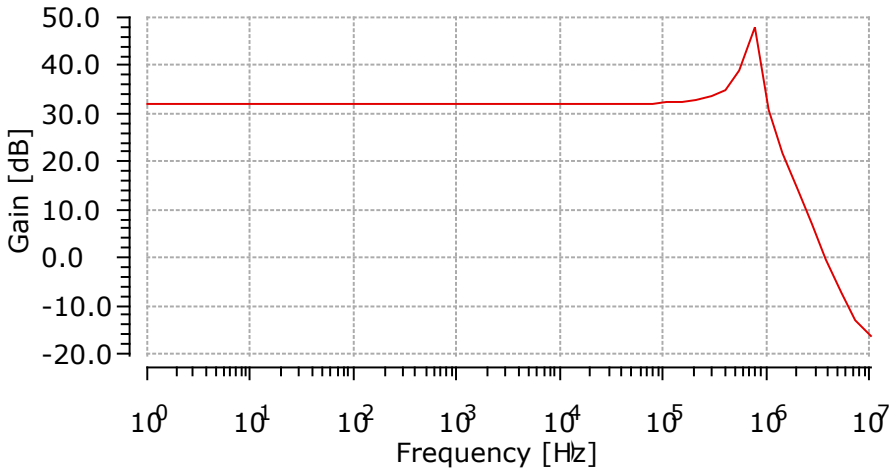


Figure 5.11: AC analysis of the closed-loop gain of the opamp with the gain results in dB.

DC analysis of the closed-loop gain is depicted in Figure 5.12 and shows a linear gain with an output range of ~ 8.4 V with an offset of ~ 17 mV which is is minimized by V_{tune}.

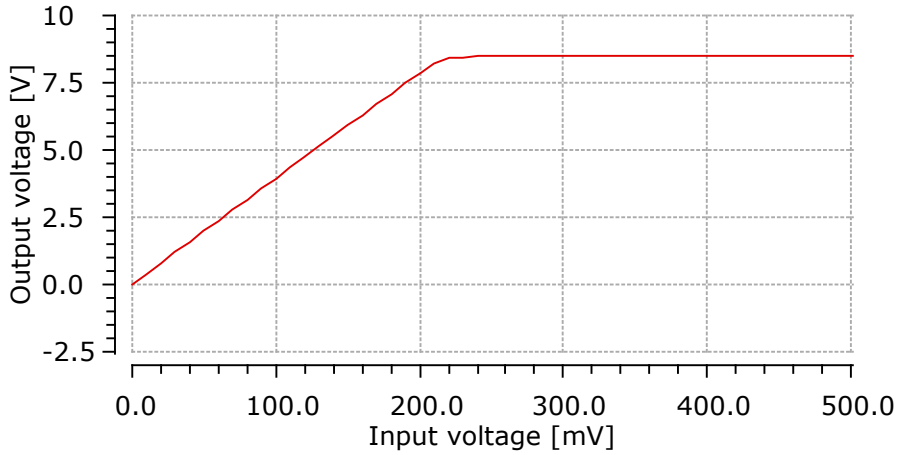


Figure 5.12: DC analysis of the closed-loop voltage gain of the opamp from which the offset and linearity are derived.

Until now the default model values for the threshold voltages are used in simulation, although the measured threshold voltages on the reference wafer differ significantly from these values. Fortunately, the design still operates as intended for the different threshold voltage values. However, different bias voltages are found to be optimal. Furthermore, it is impractical to supply all the different bias voltages with voltage supplies off chip. Therefore, current mirrors are used in combination with bias resistors off chip. According to the performed simulations the operational amplifier is suitable for the defined application. However, high frequency noise can affect the stability of the operational amplifier. If measurements reveal that this is indeed a problem, frequency compensation can be performed since the feedback network is kept off chip.

5.3. Analog-to-Digital Converter Design

The 4-bit flash ADC is composed of several blocks which are illustrated in Figure 5.13. The comparator array block transforms the analog output of the amplifier V_{amp} to 16 digital signals T. It toggles each digital output signal by comparing the analog input with 16 different reference voltages V_{ref} that are provided by the resistive string. The step size between each reference voltage is constant and the design allows for the range to be set off chip to match the ADC input range with the amplifier output range. The thermometer encoder transforms the 16 digital signal to a 4-bit signal with overflow (OF) signal that indicates that the maximum output value is reached.

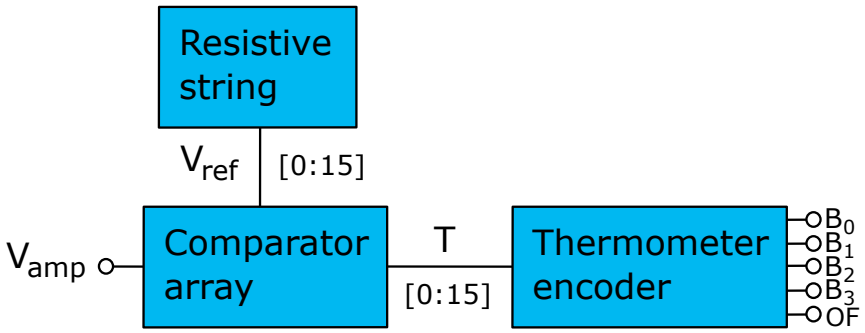


Figure 5.13: Block diagram of the ADC design.

The resistive string is a series of resistors in between V_{cc} and ground. Each node in the string corresponds with a reference voltage used for the comparator array. The first and last resistor in the string, connected to ground or supply voltage, are kept off chip which allows for adjustment of the range of reference voltages. It is defined that V_{ref0} and V_{ref15} are the lowest and highest reference voltage respectively. Resistor values of 10 kΩ are used in simulation.

The single comparator circuit design is illustrated in Figure 5.14 which has a differential input stage and inverter at the output to provide current gain. The biasing of the single comparator is done similarly to the FCO and SF. A current mirror is connected to terminal V_{b0}, which is connected to a biasing resistor. The comparator has a wide range of acceptable bias voltage values and a value of 100 kΩ for R_b is found to be fitting.

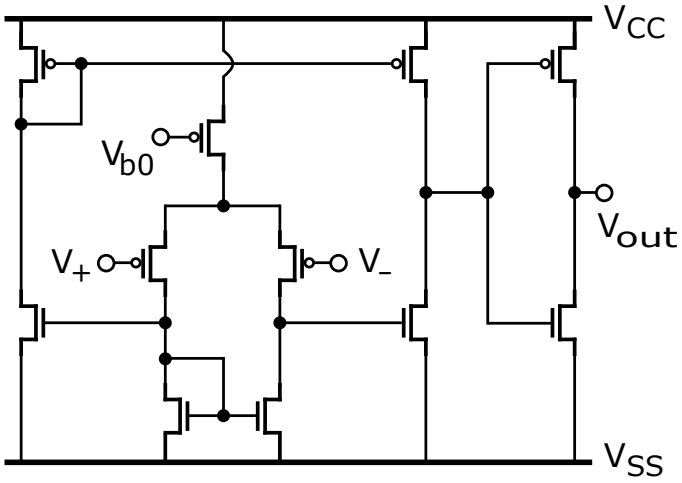


Figure 5.14: The single comparator circuit diagram.

A reference voltage is connected to the V_- terminal and A DC sweep is performed on the V_+ terminal of the comparator. Several different values of V_{ref} are simulated ranging between 0.5 V and 9.5 V to investigate the offset of the transition of high to low of the output. The transition point is defined as the input value for which the output voltage is half of V_{cc}. The resulting simulated offsets are listed in Table 5.1 and shows a constant value for the offset of ~ -55 mV with the exception of the lowest and highest reference voltage. This can be compensated for by using the off chip resistors of the resistive string to increase all reference voltage values with a constant value if desired. Note that the minus sign indicates that the output transition point occurs for too low input values.

Table 5.1: List of output transition point offsets found by simulating the comparator for different values for V_{ref}.

$\mathbf{V}_{ref}$	**Offset**
0.5 V	−74 mV
1.5 V	−57 mV
2.5 V	−56 mV
3.5 V	−55 mV
4.5 V	−55 mV
5.5 V	−54 mV
6.5 V	−53 mV
7.5 V	−53 mV
8.5 V	−53 mV
9.5 V	−470 mV

The comparator is used in a comparator array to create the 16 digital outputs which is illustrated in Figure 5.15. Note that this design requires 16 distinct comparators. The V_- terminals are connected to the different reference voltages and the V_+ terminals are all connected to each other and the V_{in} terminal. A single current mirror is used to provide the bias for all the comparators in the array.

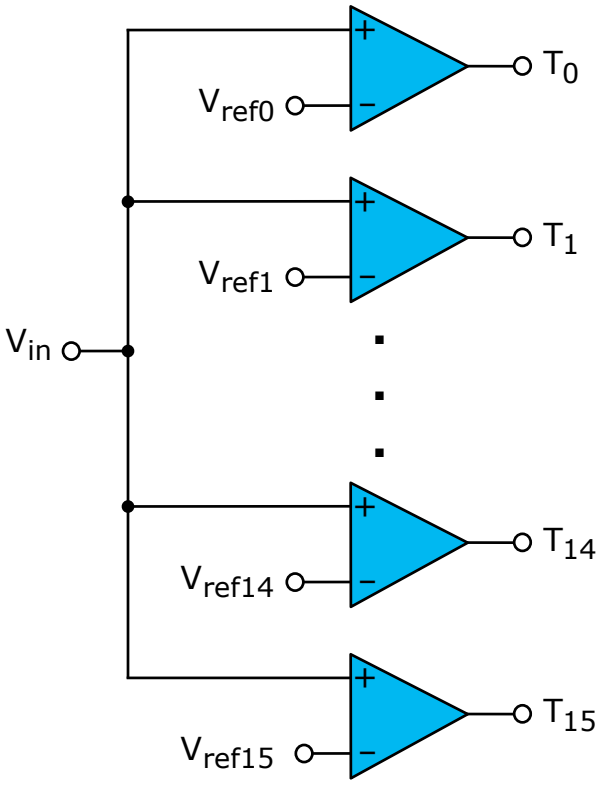


Figure 5.15: The comparator array circuit diagram. The dots represent repetition.

A transient analysis is performed to investigate the operation of the comparator array where the input voltage V_{in} is ramped from 0 V to 10 V and the result is depicted in Figure 5.16. The resistive string is used to supply the different reference levels with the differential amplifier output range of 0.0 V to ~ 8.4 V using the off chip resistors. The digital comparator outputs T switch from high to low when the respective reference V_{ref} is reached by the input V_{in}.

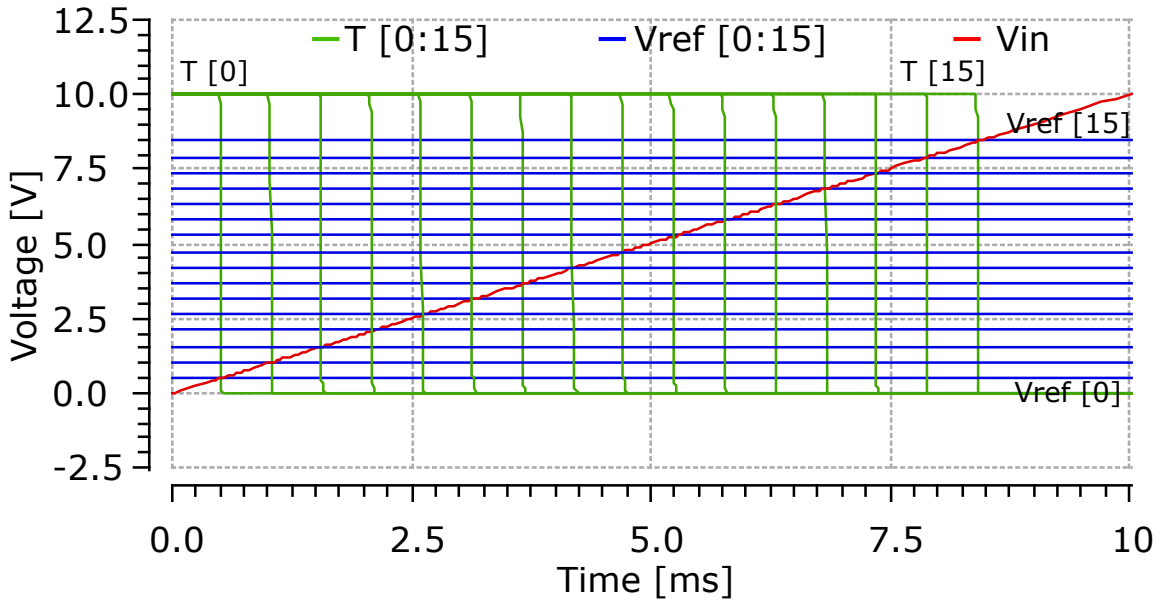


Figure 5.16: Transient simulation result of the comparator array where the input V_{in} is incremented and the outputs T are monitored. Note that signals T and V_{ref} consist of 16 signals each that are colored the same in favor of readability.

The thermometer encoder consists of many digital logic gates, which implies that a large amount of CMOS devices are required. Since digital circuits are less sensitive to device deviations, the used CMOS devices can be much smaller than those used in the analog design of the amplifier and comparator. The used device sizes are listed in Table 5.2. Note that the PMOS is two times as wide as the NMOS which results in a transition point at $\sim V_{cc}/2$.

Table 5.2: List of CMOS device sizes used in the logic gates of the thermometer encoder.

Logic gate	**NMOS (wxL)**	**PMOS (wxL)**
Inverter	20 μm x 4 μm	80 μm x 4 μm
NAND	40 μm x 4 μm	80 μm x 4 μm
NOR	20 μm x 4 μm	40 μm x 4 μm

The thermometer encoder transforms the 16 digital outputs of the comparator array to a 4-bit signal. To achieve this it first performs parity checks between outputs T of which the logic circuit is illustrated in Figure 5.17. The thermometer encoder then propagates the outcome of the parity checks to the respective output bit by means of OR gates. The complete thermometer encoder logic circuit is illustrated in appendix Figure E.7 in favor of readability. The implementation does not include a bubble correction mechanism which implies that for brief periods of time the output of the flash ADC may be wrong as the analog input changes. However, the ADC is used in a DC application and it is decided to not implement a bubble correction mechanism to save chip area.

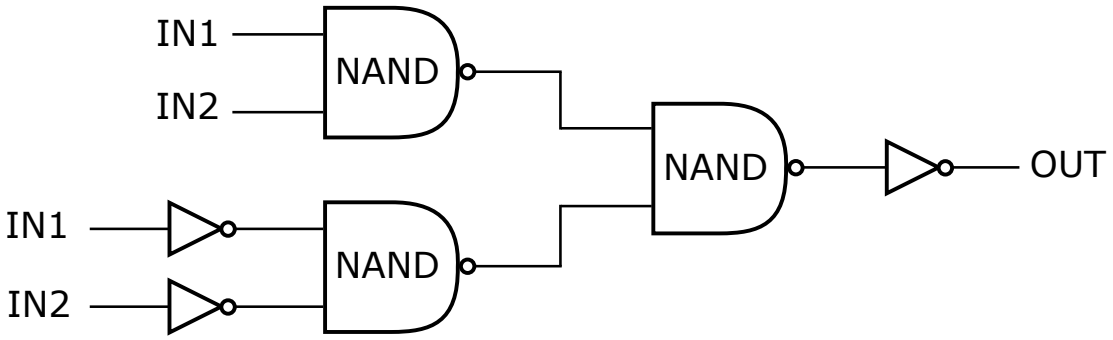


Figure 5.17: The parity check logic circuit.

Transient analysis of the complete flash ADC is performed and the results are depicted in Figure 5.18. The output bits switching delay is negligible on the given timescale. Note that the OF signal switches to high when the thermometer encoder counts 16, which implies that the input is out of the flash ADC range.

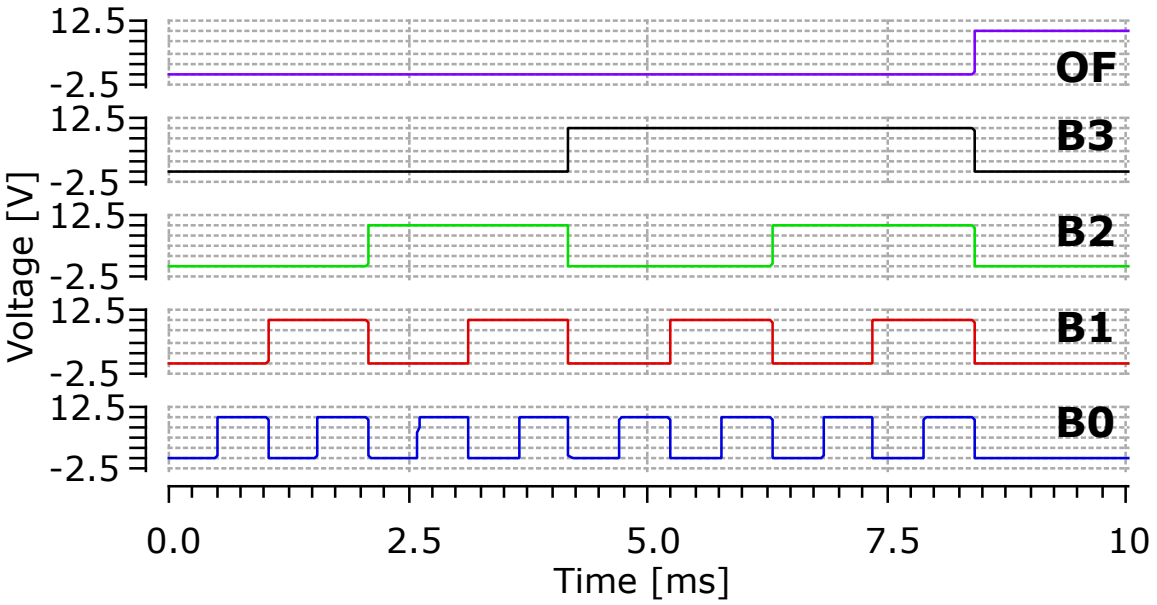


Figure 5.18: Transient simulation result of the complete flash ADC where the input V_{in} is incremented and the output bits are monitored.

Similarly to the amplifier simulations, the default threshold voltages are used until now. The use of the threshold voltage pairs corresponding to the reference wafer and graphene growth wafer resulted in negligible differences and are therefore not listed. For each pair, the offset of the transition point remains below 10 % of the step size between the reference voltage levels which is considered acceptable.

5.4. Complete Circuit Design Simulation

The designed blocks are now connected to form the complete read-out electronics design. The Wheatstone bridge is simulated by performing a DC sweep of the pressure dependent resistors corresponding with the measurement results. Unfortunately, the connection of the designed Wheatstone bridge to the amplifier significantly changes the intended value of V_{sens}. This is due to a resistive path between V_{sens+} and ground through the resistive feedback network in the differential amplifier which lowers the potential at that node. The problem is solved by choosing the resistive feedback resistors in the differential amplifier significantly larger than the resistor values in the Wheatstone bridge. From simulation follows that for Wheatstone bridge resistor values of ~ 10 kΩ a value of 200 kΩ for feedback resistors R_1 and R_2 is sufficient.

DC analysis of the complete design by incrementing the resistance change of the pressure dependent resistors is depicted in Figure 5.19. The amplifier output V_{amp} reaches its maximum around a resistance change of ~ 2.8 %, which corresponds with the maximum measured resistance change. This is also the point where OF switches to high. Using the other threshold voltage pairs causes negligible change in results. The complete design operates as intended with considered acceptable specifications and its layout design is done in the next section.

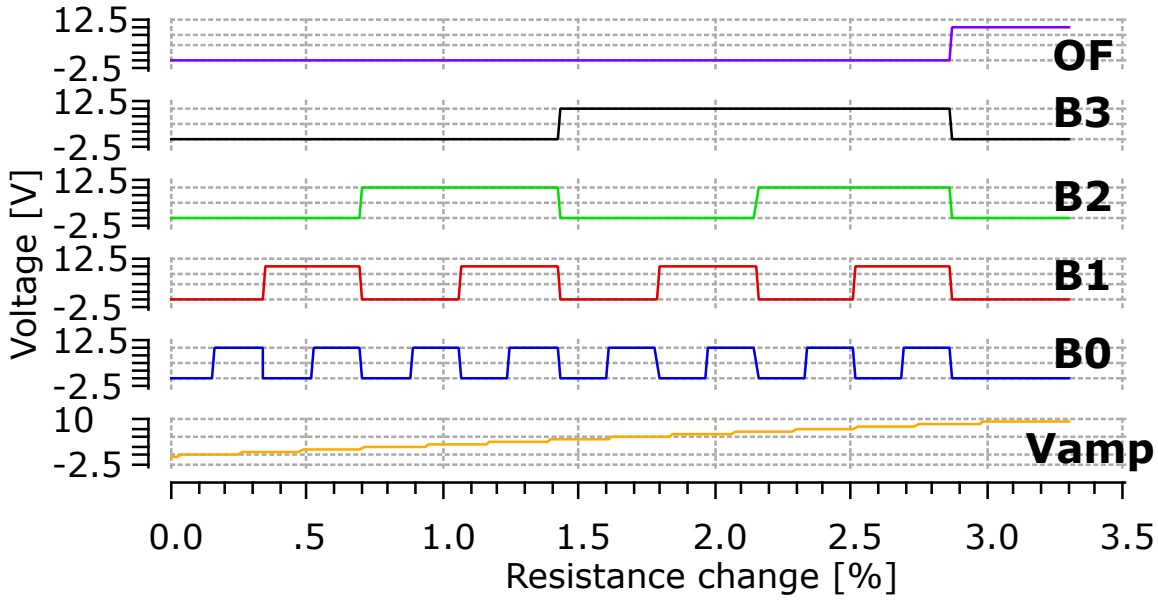


Figure 5.19: DC analysis simulation result of the complete design by incrementing the resistance change of the pressure dependent resistors.

5.5. Layout Design of the Complete Circuit

The 400x4 NMOS and PMOS layouts of the devices used in analog components are illustrated in Figure 5.20. Due to the high aspect ratio of the devices it is chosen to place four 100x4 in series, which results in devices close to an aspect ratio of 1 with layout dimensions of 122 μm x 113 μm. However, this design inevitably requires two metal layers to be connected in a circuit. This is considered acceptable, as the circuit complexity most likely requires two metal layers. The CO mask layer is now split in the contacts from the first metal to the silicon CT and the contacts from the second metal to the first metal V1. The IC mask layer is now split in the first metal layer M1 and the second metal layer M2. The device gates are connected in M1 and the source and drain are connected in M2. The layouts of the smaller CMOS devices used in logic gates are illustrated in appendix Figure E.8. The aspect ratios of these devices are much lower than the ones used for analog circuit and do therefore not incorporate multiple devices in series.

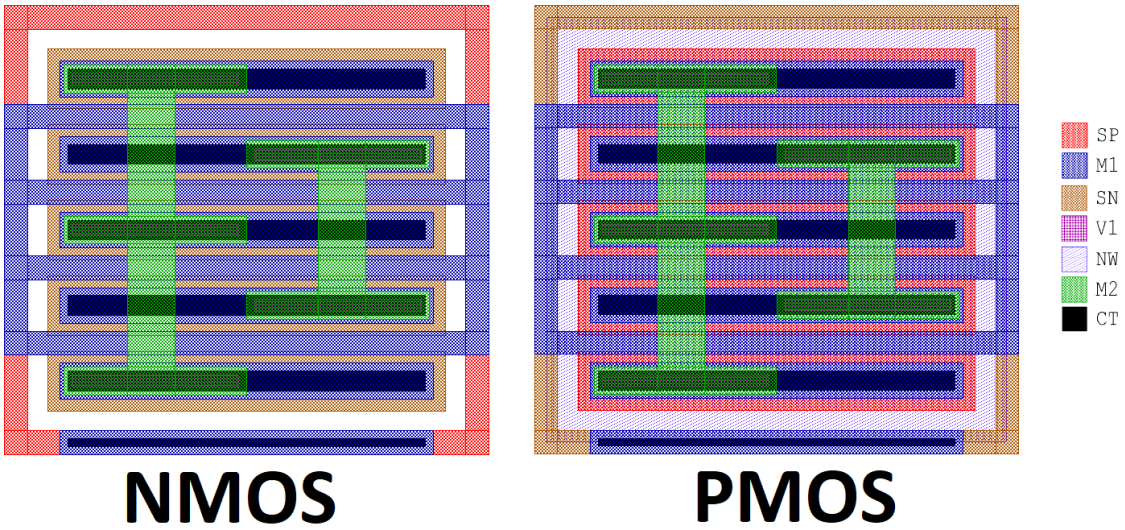


Figure 5.20: Layout design of the 400x4 NMOS and PMOS with the 7 stacked layers. The legend indicates the different layers.

The opamp layout with marked terminals is illustrated in Figure 5.21 and it consists of two identical blocks that contains the FCO and SF combination. The routing is mainly done in the M2 layer as this layer has a lower resistance and should thus add less noise to the analog signals. The M2 interconnect lines have a width of $12\ \mu$m and the power supply lines have a width of $25\ \mu$m. A distance of $12\ \mu$m is kept between devices and a distance of $8\ \mu$m is kept between routing lines. Note that all PMOS and NMOS devices are placed in the top and bottom half of the layout where they are connected to the V_{CC} and ground lines respectively and that the current mirrors responsible for the biasing are not included. The layout dimensions are 2.4 mm x 0.6 mm.

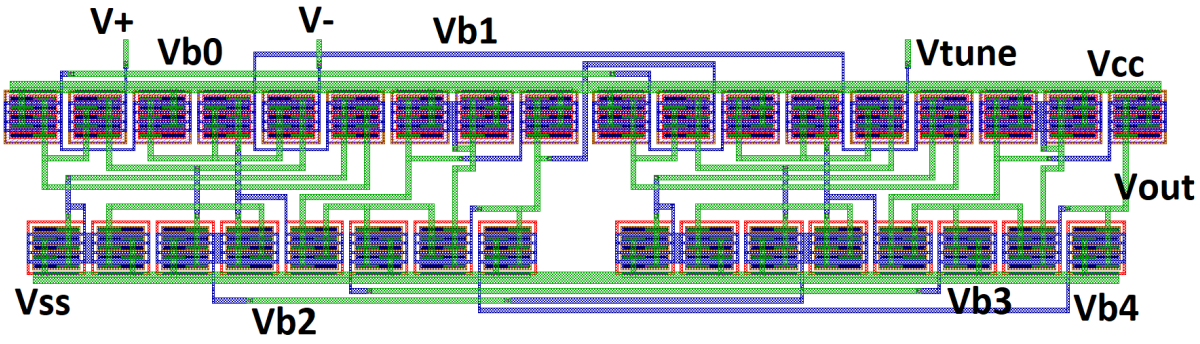


Figure 5.21: Layout design of the opamp with all the terminals marked.

The test structures for the FCO, SF and opamp are combined in a single block used for characterization of the opamp, which is illustrated in Figure 5.22. In this block, current mirrors are included for each test structure and bond pads are added to allow wire bonding the relevant signals to a chip package. The layout dimensions are 7.3 mm x 1.0 mm and the block has 35 terminals in total.

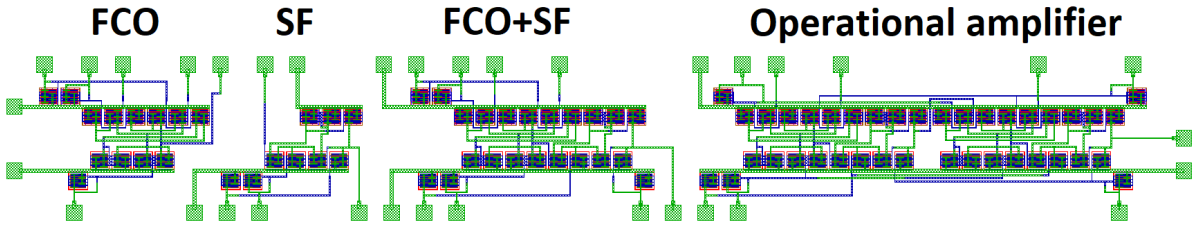


Figure 5.22: Layout design of the opamp test structures block, including the FCO, SF and FCO cascaded with SF combination.

The comparator layout is illustrated in Figure 5.23. Similar to the operational amplifier design, the PMOS devices are in the top half and the NMOS devices are in the bottom half. Note that the current mirror responsible for the biasing is not included. The layout dimensions are 0.8 mm x 0.3 mm.

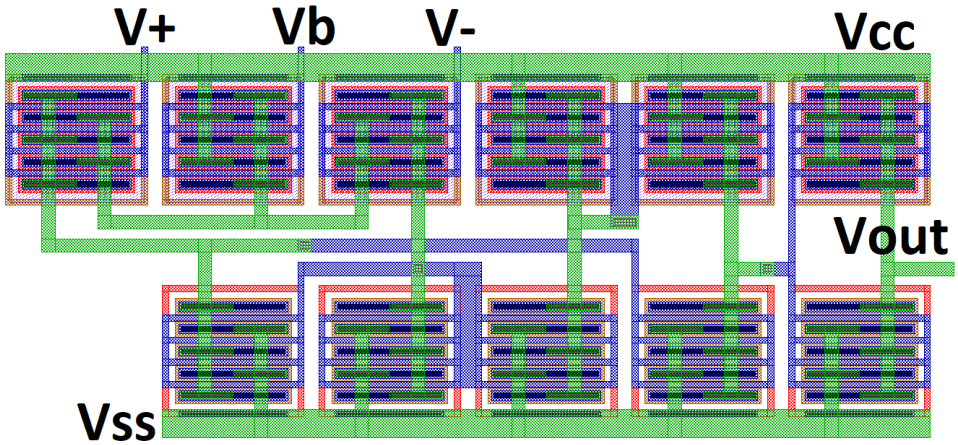


Figure 5.23: Layout design of the comparator with all the terminals marked.

Test structures for the single comparator and the entire comparator array are combined in a single block used for characterization of the comparator, which is illustrated in Figure 5.24. The current mirror and bond pads are added. The layout dimensions are 8.5 mm x 1.4 mm and the block has 42 terminals in total. Note that both the V_{CC} and ground lines run in a U-shape to allow for a folded comparator array layout with four rows of devices. Routing is done mostly in the M2 layer with 25 μm wide traces, as these traces are long.

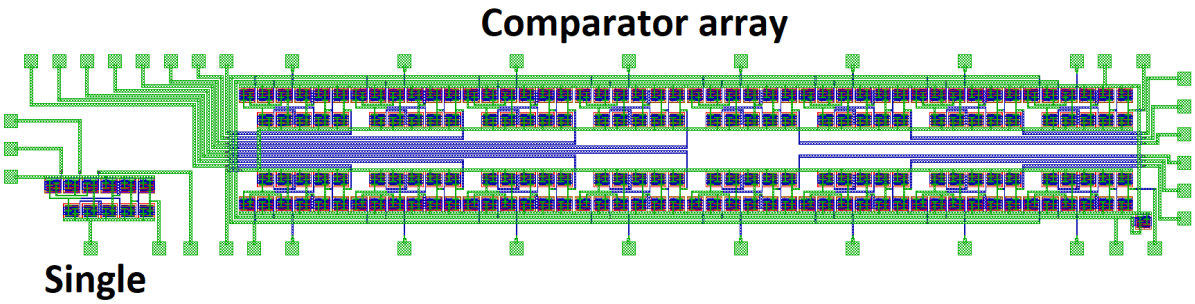


Figure 5.24: Layout design of the comparator test structure block, including the single comparator and comparator array.

The resistive string layout is illustrated in Figure 5.25 and is implemented in the NW layer as it does not change in sheet resistance after the graphene growth step and is in the same order of magnitude as the used resistor values in simulation. A guard ring in the SP layer is placed around the string. The layout dimensions are 1.0 mm x 0.2 mm. No test structure block is designed to measure the resistive string entirely, due to the large amount of pins that would be required for this. Instead, a single NW resistor is placed in a test structure.

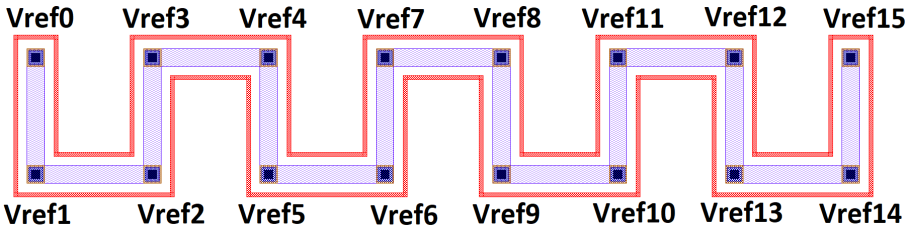


Figure 5.25: Layout design of the resistive string that is implemented in the NW layer with an SP guard ring.

The thermometer encoder layout design is illustrated in Figure 5.26 which consist of logic gates and no bias voltages are required. The V_{CC} and ground lines are folded such that eight rows of devices can be used. Routing is done mostly in the M2 layer with traces of a width of 25 μm since the traces can be several mm long. The layout dimensions are 5.8 mm x 1.7 mm.

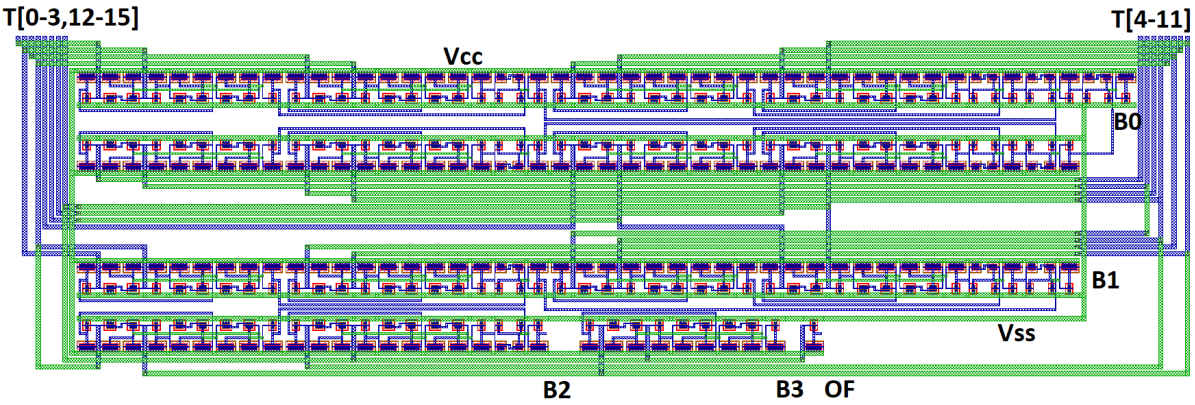


Figure 5.26: Layout design of the thermometer encoder with all the terminals marked.

The individual logic gates and thermometer encoder are tested using the digital test structures block illustrated in Figure 5.27. The layout dimensions are 7.1 mm x 2.2 mm and and the block has 42 terminals in total.

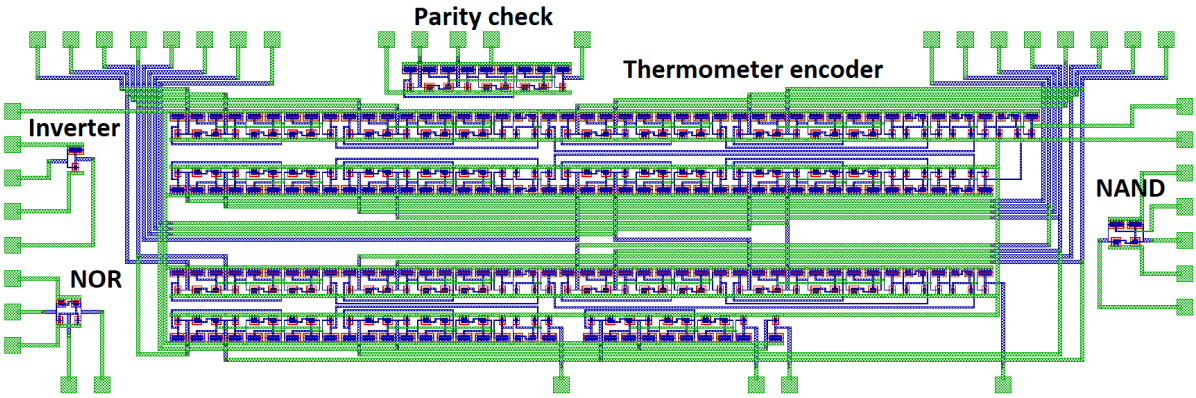


Figure 5.27: Layout design of the digital test structures block including logic gates and the thermometer encoder.

The Wheatstone half bridge layout incorporating graphene-based Pirani pressure sensors is illustrated in Figure 5.28. Note that these structures reside in chip area that has a thicker SiO_2 layer than the CMOS electronics, which requires a mask to create. Taking the results of Section 3.3 into account, the metal interconnect lies on the SiO_2 layer on both sides of the graphene strip to improve the contact. Furthermore, no large graphene planes are implemented with metal on top of it. The layout dimensions are $\sim 20\ \mu$m x $\sim 20\ \mu$m, depending on the bridge geometry. Note that this is significantly smaller than any MOS device that is used in the design. The layout of the graphene-based Wheatstone bridge including bond pads is illustrated in Figure 5.28. The layout dimensions are 0.7 mm x 0.2 mm.

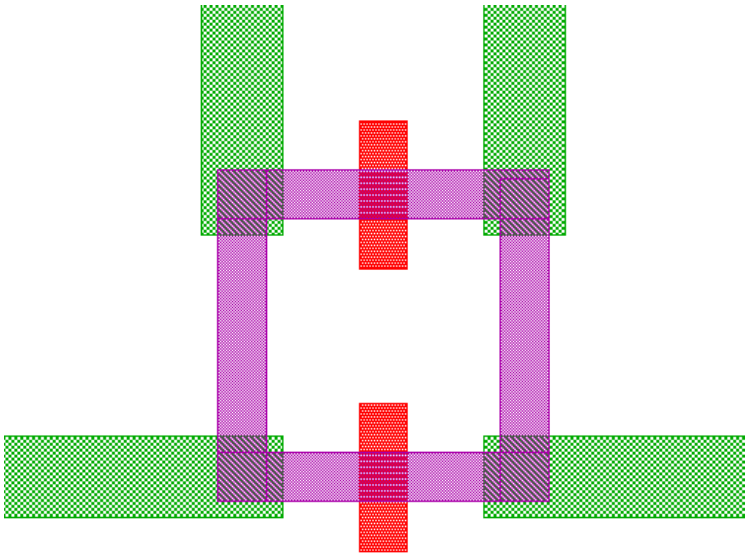


Figure 5.28: Layout design of graphene-based Pirani pressure sensors in a Wheatstone half bridge. Purple represents the graphene strip, red the patterned cavity and green the second metal layer.

The Wheatstone bridge could suffer from matching problems. Therefore, it is decided to add another structure in which the matching problem can be solved off chip. The two legs of the Wheatstone bridge are split in two, resulting in the structure illustrated in appendix Figure E.10. These structures have one regular graphene resistor and one Pirani pressure sensor. Problems in resistor matching are solved by adding a resistor off chip.

The complete layout is on a 10 mm x 10 mm die and its organization is schematically illustrated in Figure 5.29. The *Analog test structures* houses the operational amplifier test structures illustrated in Figure 5.22, the *Digital test structures* the test structures illustrated in Figure 5.27 and the *Comparator test structures* consists of the structures illustrated in Figure 5.24. In the *Graphene structures* all structures that contain graphene are placed, including Wheatstone bridges, single legs of the Wheatstone bridge, single Pirani pressure sensors and Van der Pauw sheet resistance structure. The *Probe* block consists of standard test structures to be measured in an automated probe station, including all used transistor sizes, Van der Pauw sheet resistance structures and an NW resistor. Several devices in the *Probe* block are implemented in both the M1 and M2 layer to allow for measurements at different stages in the process. Finally, all relevant blocks are placed in *Complete design*, but they are not connected. If measurements show that certain blocks do not operate as intended, they are left out.

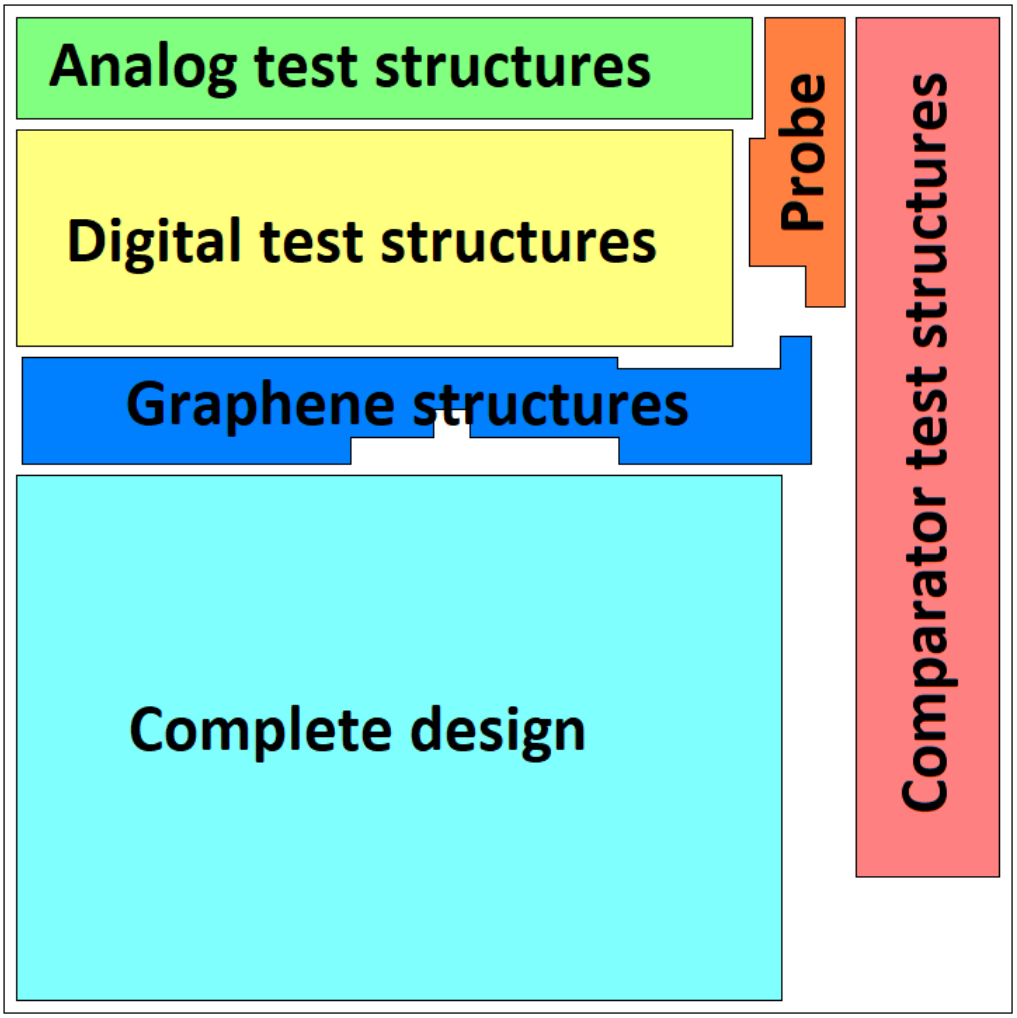


Figure 5.29: Organization of the complete 10 mm x 10 mm die layout.

The complete layout design is illustrated in Figure 5.30 matching the organization as in Figure 5.29. The dashed red boxes indicate the regions where thermally grown 100 nm SiO_2 is located for the CMOS device gates. These regions are also the only regions where the dielectric between M1 and M2 is deposited. As a result, M1 is only present inside these regions. Outside these regions, TEOS oxide deposition is performed to implement 600 nm thick SiO_2 for the Pirani pressure sensors. To allow for dicing of the dies, a saw lane of 125 μm is kept free in the design. The minimum bondpad to metal trace distance is 50 μm, the minimum distance between bondpads is 100 μm and the bondpads have a size of 100 μm x 100 μm.

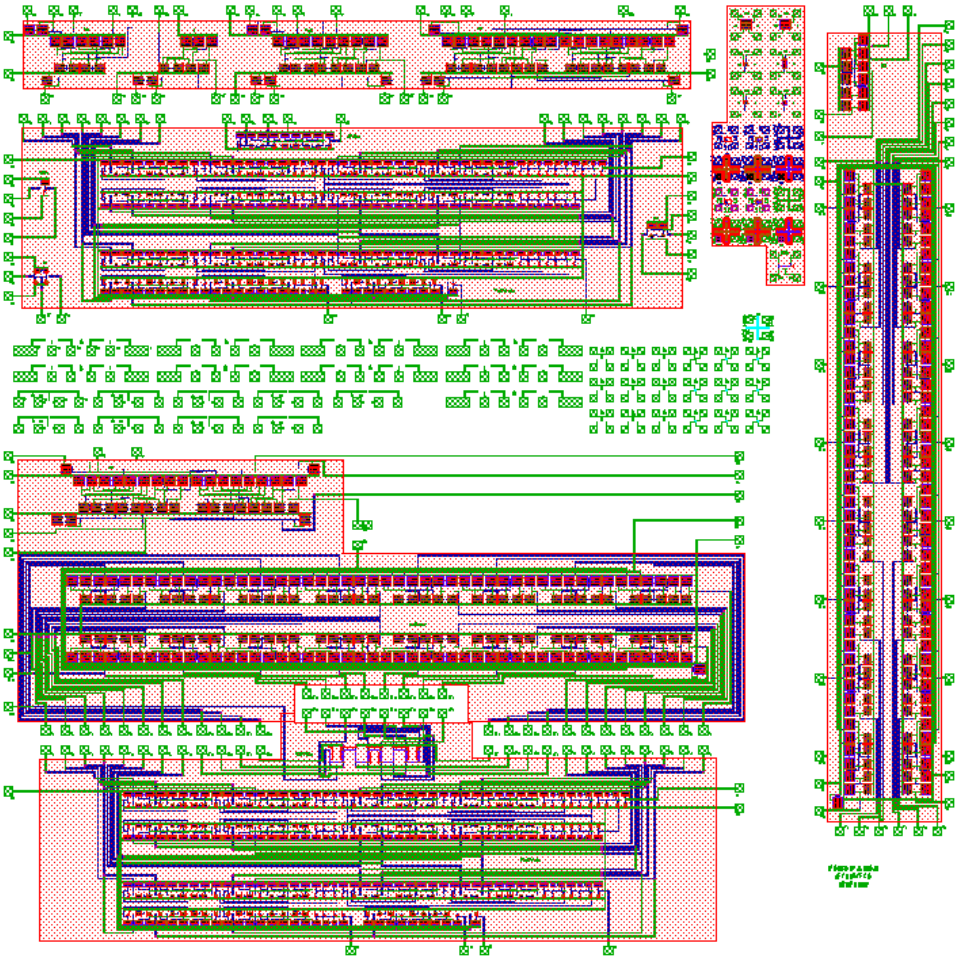


Figure 5.30: The complete 10 mm x 10 mm design with all ten layers, indicating thermal oxide regions with dashed red boxes.

Finally, the masks that are used in the fabrication process are extracted and ordered. There are ten layers used in the layout design which are the NW, SN, SP, CT, M1, M2, V1, GR, CA and RE, where GR is the graphene layer, CA the patterned cavity layer and RE the region layer that indicates where thermally grown oxide is located. Each mask consists of a 2x2 frame of individual layers and therefore three masks are required to house all ten layers. Two unused locations remain, that can be used for extra masks that allow more process freedom. It is decided to include opposite field types for the V1 and RE layers. The mask organization is illustrated in Figure 5.31

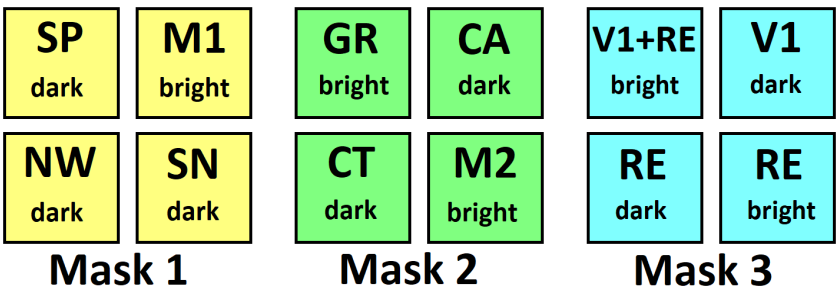


Figure 5.31: The mask organization including all ten layers with the addition of two extra V1 and RE field types.

5.6. Conclusions

A half Wheatstone bridge topology is used to read out the graphene-based Pirani pressure sensor. The Wheatstone bridge is implemented in graphene, which could be subject to mismatch errors. Therefore separate structures are included that consist of just a single Wheatstone bridge leg. This topology can also be used to quantativily determine the ratio between temperature increase of suspended and non-suspended graphene. A differential voltage-to-voltage amplifier is used to amplify the Wheatstone bridge output which consists of several stages to achieve enough voltage and current gain. The feedback network and bias resistors are kept off chip to allow for adjustments. The design operates as intended for different threshold voltage pairs according to simulations. No frequency compensation is included as no high frequencies are expected in the application.

A 4-bit flash ADC is used to transform the sensitive analog signal to a digital representation. The resistive string is implemented in the NW layer and two off chip resistors are used to set the range of reference voltages. The comparators in the comparator array have offsets below 10 % of the step size and are considered adequate for this design. The thermometer encoder design uses parity checks to identify the bit states and does not incorporate a bubble correction mechanism as the application is for DC measurements. The complete design operates as intended according to simulations.

The complete layout is designed on a 10 mm x 10 mm die and houses many test structures. The graphene structures are all placed together, as there is a difference in SiO_2 thickness required for the Pirani gauge and the CMOS devices. In the complete design, the individual blocks can be connected through wire bonding. This allows for the omission of blocks that are found to be faulty or not functioning correctly. For fabrication three masks each containing four design layers are ordered.

6

Fabrication Results and Discussion

The complete fabrication process is described in this chapter and the results of the fabrication are shown, as well as test device measurements that are compared to the results of the training run in Chapter 4. Measurements on the designed circuits are performed in the next chapter. A reference batch is fabricated to test the dielectric and second metal layer implementation and compare the results with the training run reference wafer. The various fabrication challenges are discussed, including the different oxide thicknesses in the design, protection of the Mo and graphene stack, dielectric and second metal and the etching of the sensor cavity. The batch used in the fabrication process run is defined in Table 6.1. The purpose of each wafer is either test device characterization measurements on wafer-scale or circuit measurements on single dies.

Table 6.1: Fabrication process run batch definition that consists of a reference and fabrication set. The wafers are used for device and/or circuit characterization. The investigated processes on each wafer are listed.

Wafer number	**Set**	**Purpose**	**Investigated processes**
1	Reference	Test devices	M1, M2 and dielectric material
2	Reference	Spare	-
3	Reference	Circuits	-
4	Reference	Spare	-
5	Fabrication	Test devices	M1, protection, dielectric
6	Fabrication	Test devices	M1, protection, M2
7	Fabrication	Test devices/circuits	Protection, M2
8	Fabrication	Spare	-
9	Fabrication	Spare	-
10	Fabrication	Spare	-

6.1. Fabrication Run Reference Batch

The batch of reference wafers consists of wafers 1-4 and are processed completely according to the standard BICMOS fabrication process without a graphene growth step and AlSi used as interconnect material. The addition of a dielectric between M1 and M2, contacts V1 and an AlSi M2 implementation are included. Wafers 1 and 2 are intended for wafer-scale measurements and will not be diced and wafers 3 and 4 are intended for wire bonding to perform circuit measurements. Furthermore, the dielectric used on wafers 1 and 3 is SiO_2 formed by TEOS deposition while wafers 2 and 4 are kept as spare for a possible different material. It is later concluded that the SiO_2 dielectric is feasible, which renders wafers 2 and 4 currently unused.

Reference wafer 1 is processed up to the M1 implementation by depositing 150 nm of AlSi with 50 nm of TiN on top in favor of good contact to M2 as TiN prevents oxidation. However, this implementation has stress issues that cause the metal interconnect to curl up at the edges after patterning. An example of this observation is depicted in appendix Figure F.1. This problem is solved by etching the TiN on wafer 1 away and deposit extra AlSi. The wafer-scale measurements are performed and are depicted in Figure 6.1 and the mean values of each wafer quadrant are listed in Table 6.2.

Comparing the results with the reference wafer in the training run in Section 4.1 it is observed that the NMOS threshold voltage is lower in this batch by ~ 0.3 V, while the PMOS threshold voltage is similar. This suggests that the density of doped carriers in the NMOS channel is lower and could be due to process variations. However, it is more likely that the formed epi-layers are not equally doped or the stress issues damaged the gate oxide. Furthermore, the yield is lower compared to the training run which was close to 100 %. Wafer 1 is completed by implementing the M2 and all devices used in the design are measured on wafer-scale and listed in appendices Figure F.2 and Figure F.3. The threshold voltage results are similar, although the smaller NMOS devices used for logic gates have a larger non-uniformity.

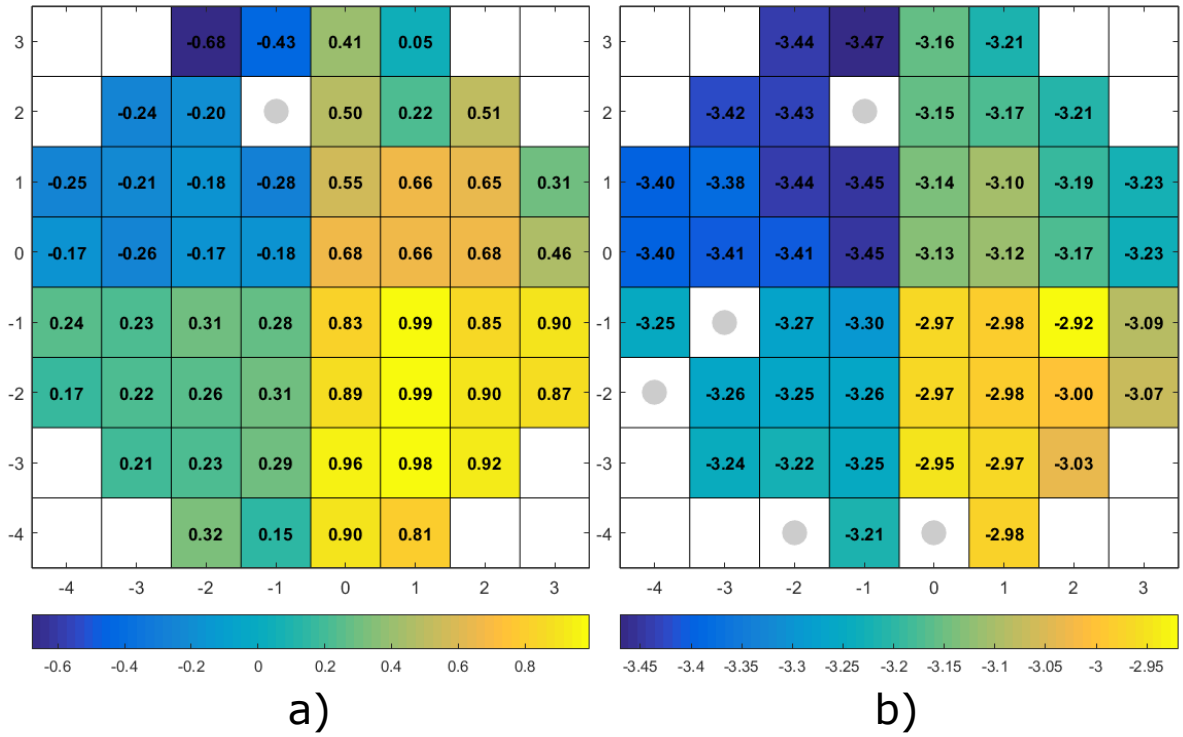


Figure 6.1: Wafermaps depicting threshold voltage [V] of NMOS 20x5 in a) and of PMOS 20x5 in b) after M1 implementation. Broken devices are marked with a grey circle. Measured on W1.

Similarly to the threshold voltage measurements, the sheet resistance is measured after the M1 implementation and after the M2 implementation. No differences are observed and therefore just the results of the measurements after the M2 implementation are reported, complemented by the M1 sheet resistance, in Figure F.4. Unfortunately, the NW sheet resistance can not be measured due to an error in the layout design where highly doped SN contacts are missing. Values of $0.2\ \Omega$, $0.02\ \Omega$, $66\ \Omega$ and $89\ \Omega$ are found for the M1, M2, SN and SP respectively. The SN results are less uniform compared to the training run results.

Table 6.2: Threshold voltages of all quadrants on the reference wafer in the fabrication run. The wafer-scale measurement results are depicted as wafermaps in Figure 6.1.

Adjustement dose	V_{Tn}	V_{Tp}
0e11	-0.20 V	-3.40 V
3e11	0.25 V	-3.25 V
6e11	0.60 V	-3.15 V
9e11	1.00 V	-3.00 V

From the results of wafer 1 it is concluded that the process works for the reference batch and therefore wafer 3 is processed accordingly, with the exception that TiN is omitted and a standard RF etch is used before the second metal deposition. The final process of the reference wafer batch is illustrated in Figure 6.2 where the contacts V1 are implemented by dry etching. The wafer-scale measurements of the threshold voltage on wafer 3 are listed in appendix Figure F.5 and Figure F.6 and show a higher yield and uniformity compared to wafer 1, although the NMOS threshold voltage shift compared to the training run reference remains. It is therefore concluded that the threshold voltage shift is due to a differently doped epi-layer. The wafer-scale sheet resistance measurements are listed in Figure F.7 and are similar to the results of wafer 1 with a higher uniformity for the SN results. Wafer 3 is used in Chapter 7 for circuit characterization.

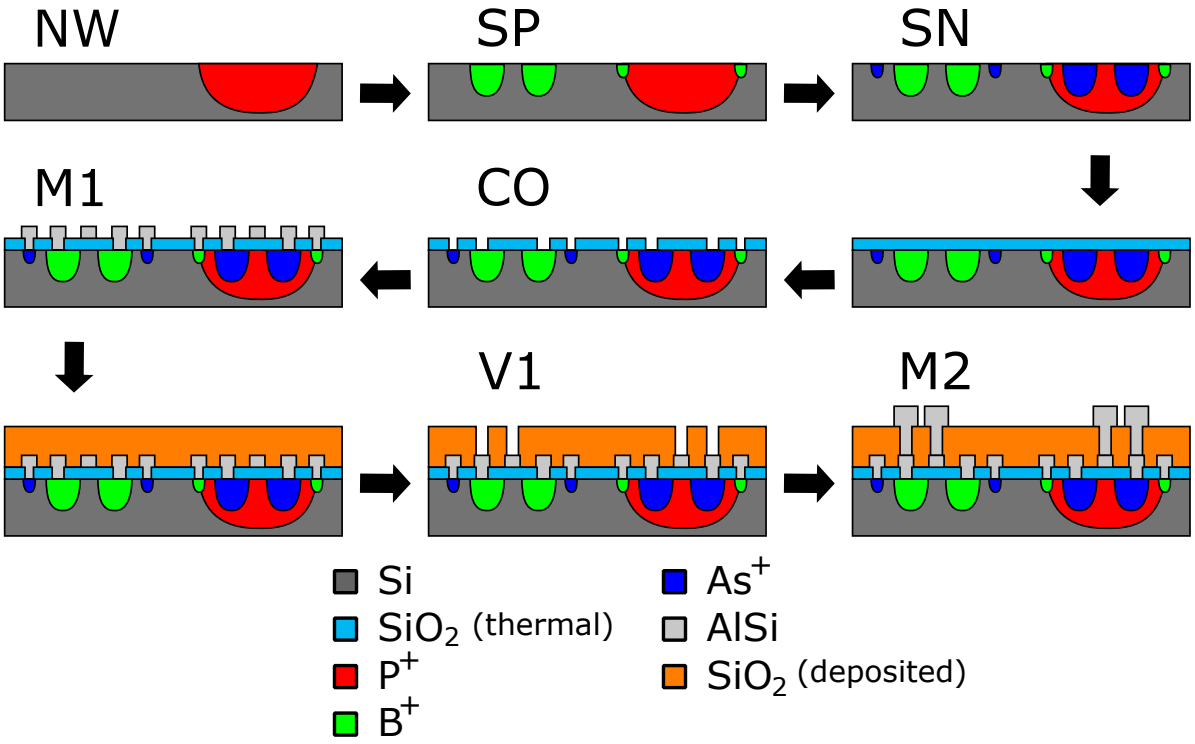


Figure 6.2: Final process of the reference wafers. The first five standard steps of the BICMOS process are illustrated and are followed by the dielectric implementation by SiO_2 TEOS deposition, dry etching of the contacts V1 and the M2 implementation in AlSi.

6.2. Graphene Implementation in the Fabrication Process

The fabrication batch that incorporates both CMOS and graphene is defined by wafers 5-10. For the graphene-based Pirani sensor it is required to define a separate chip area with different SiO_2 thickness, since the CMOS gate oxide is 100 nm thick and the Pirani gap depth is 600 nm. The solution is illustrated in Figure 6.3, which starts right after the final implantation step. The solution starts by performing TEOS deposition of 600 nm and etch it away in the CMOS regions by wet etching. This is followed by wet thermal oxidation to form the gate oxide, that mostly grows in the CMOS regions. The Mo catalyst is then deposited and patterned by lithography to define the graphene locations. Finally, graphene is grown by selective CVD in 20 minutes as described in Section 4.3.

The oxide thickness is measured on wafer 5 at several stages in the process. The PECVD TEOS deposited SiO_2 thickness before gate oxidation is $\sim$ 585 nm. After the gate oxidation the SiO_2 of the Pirani sensor is $\sim$ 620 nm and the gate oxide is $\sim$ 100 nm. It is concluded that there is also thermal oxide forming under the TEOS deposited SiO_2, causing this layer to be thicker. This could result in difficulties when etching the cavity of the Pirani sensor. After the dry etching of the Mo catalyst, the gate oxide is reduced to $\sim$ 80 nm.

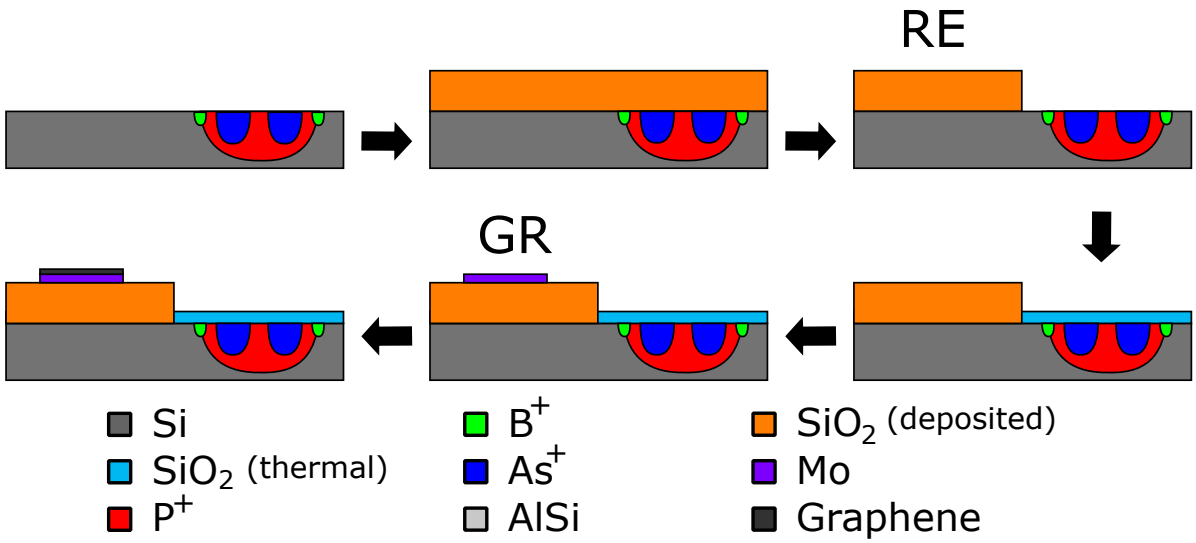


Figure 6.3: Flow of the different SiO_2 thickness solution required for the CMOS and Pirani pressure sensor. SiO_2 TEOS deposition is used for the Pirani sensor oxide, followed by wet thermal oxidation for the gate oxide. The Mo catalyst is patterned on the TEOS deposited SiO_2 and allows for the selective CVD growth of graphene.

6.3. Graphene Protection During First Metallization

The next stage entails the first metal layer implementation. It is concluded in Section 4.2 that AlSi should be used and that the Mo and graphene stack has to be protected. The solution is illustrated in Figure 6.4, which starts where the previous section ended. The first step is the CO implementation, which is done by dry etching as the graphene is protected by photoresist since it has no CO. Then the Mo and graphene stack is protected by a layer of photoresist. This is followed by the deposition and dry etching of the AlSi. Note that the dry etching process lands on both photoresist and SiO_2. Finally, the photoresist protection layer is removed.

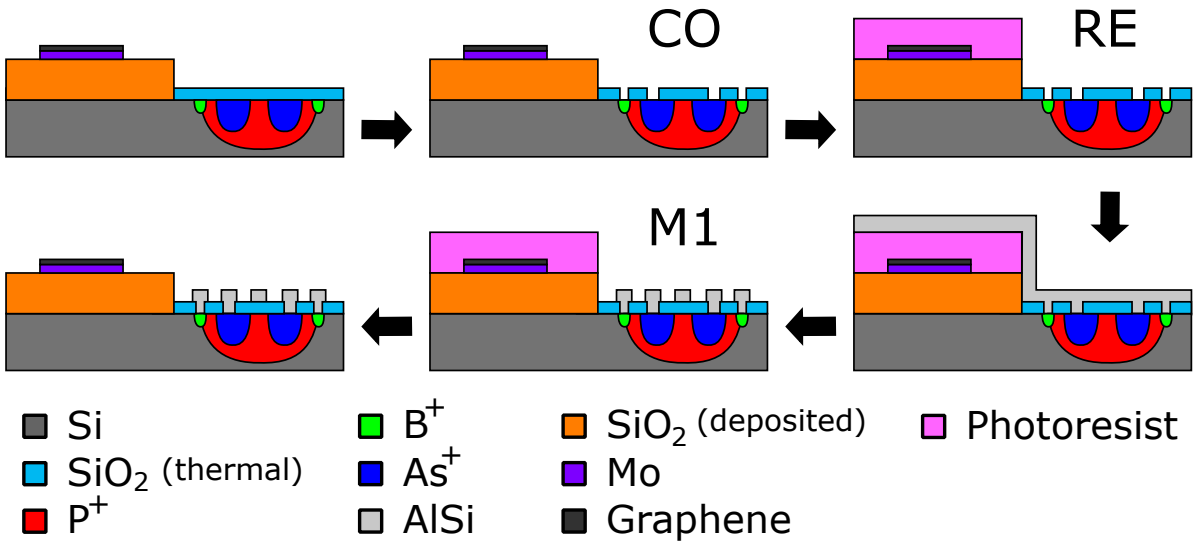


Figure 6.4: Flow of the Mo and graphene stack protection during the first metal implementation. The CO are dry etched, followed by a protective photoresist layer on the Mo and graphene stack. The AlSi is deposited and dry etched and the protective layer is then removed.

The proposed solution is first tested on wafer 5 and proved to have significant challenges. After the AlSi deposition the wafer is coated to perform lithography. This resulted in large bubbles in the AlSi in the TEOS deposited SiO_2 regions that got worse after the development step. From this it is concluded that the protective photoresist is outgassing during the bake steps performed in the coating and development.

Furthermore, the AlSi was corroding heavily after the dry etching over the course of one day. This is due to the fact that the dry etch process lands on large areas of photoresist. A chloride gas is used, which causes chloride ions to attach to the photoresist surface. Over time the ions react with hydrogen in the air and form chloride, which will continue to etch the AlSi. Due to the corrosion, no devices could be measured.

The bubbles in the AlSi are solved on wafer 6 by performing a deep ultra-violet (DUV) bake after the photoresist protection layer is implemented. As a result, there were no more bubbles observed. However, the final cleaning step proved to be difficult as the photoresist residue did not come of entirely even after a night of soaking in the NMP solvent. Furthermore, the residues were flipped of the TEOS deposition regions on to the CMOS regions which causes yield issues. The corrosion problem is solved by rinsing wafer 6 in water immediately after the AlSi dry etching. When measuring the single devices, it was observed that the metal did not form a proper contact to the Si. An alloy step resulted in better contacts in the SP regions, but not in the SN regions. Wafer 6 is not used any further.

Wafer 7 is processed similarly to wafer 6, but the DUV bake is substituted by a 10 minute bake at 115 °C and the HF dip before metal deposition is twice as long. Some small bubbles in the AlSi are observed after development, but are concluded to be negligible. After dry etching the AlSi, some metal clusters remain over the wafer that do not etch in the chloride gas. A 1 minute rinse in 0.5 % hydrofluoric acid (HF) is performed which removes the metal clusters. Unfortunately, the residue of the photoresist protection is similar to that on wafer 6 from which it is concluded that the baking step is not the dominant cause for the curing. This points to the dry etching being the problem. HF can be used to wet etch the AlSi to keep the protective photoresist layer from exposure to plasma, which should make it easier to remove. This is however not tested in this research work. The single devices could be measured, but the contact resistance remained high. An alloy step is performed, resulting in good contact resistance and measurable single devices.

The wafer-scale threshold voltage results after the first metal layer are listed in appendix F.8, which are similar to the reference wafer results. No threshold voltage shift as result of the graphene growth is observed. This wafer was alloyed, which could have reduced the gate oxide surface charge to regular values, reducing the threshold voltage shift.

6.4. Dielectric and Second Metallization Implementation

Wafer 5 is used to test the dielectric and second metal layer implementation. Raman spectroscopy is used to verify that there is graphene on the wafer. Then the TEOS deposition of SiO_2 is performed, followed by lithography that exposes the vias and elevated graphene regions. The deposited SiO_2 is etched in a (1:7) BHF solution, which revealed difficulties. The vias were etched highly non-uniform with some vias etched not at all while others were over etched to more than twice the intended area. Furthermore, it is difficult to inspect if the Mo and graphene stack is etched clear. Raman spectroscopy showed that there is still graphene on the wafer, from which is concluded that a TEOS deposition can be used as dielectric and no alternatives are investigated in the research work. The second metal layer is then implemented by a chromium/gold (Cr/Au) lift of process, which was also used in the two batches of graphene-based Pirani pressure sensors. Unfortunately, measurements revealed that there was no contact between the first and second metal layer.

On wafer 7 the etch step of the dielectric is split in two. After the TEOS deposition of SiO_2, the vias are exposed and dry etched which gave no difficulties. This is followed by the exposure of the large TEOS deposited SiO_2 region where the Mo and graphene stacks reside. These regions are etched clear by wet etching in a (1:7) BHF solution, while carefully monitoring the oxide thickness. A slight over etch is performed resulting in an oxide thickness of ~ 600 nm compared to the ~ 620 nm before dielectric deposition. After stripping the photoresist, a (1:7) BHF dip of 15 seconds is performed followed by the metal deposition of 100 nm of Ti with 1 μm of AlSi on top. The Ti layer is added in favor of good contact resistance to the graphene. After lithography, the AlSi is dry etched by landing on the Ti layer as Ti etches significantly slower in chloride. Finally, the Ti is wet etched in a 0.55 % HF solution for 80 seconds. Unfortunately, the AlSi is under etched as the Ti layer is over etched. Additionally, a silicon haze is observed over the wafer.

The fabrication process described for wafer 7 is illustrated in Figure 6.5, which starts where the previous section left off. First the TEOS deposited SiO_2 is formed, followed by the dry etching of the V1. The Mo and graphene stack is then etched free by wet etching. Note that the wet etch lands on TEOS deposited SiO_2. Then a 100 nm Ti layer with a 1 μm AlSi layer on top is deposited and patterned by dry etching the AlSi in a chloride gas followed by an HF dip to wet etch the Ti.

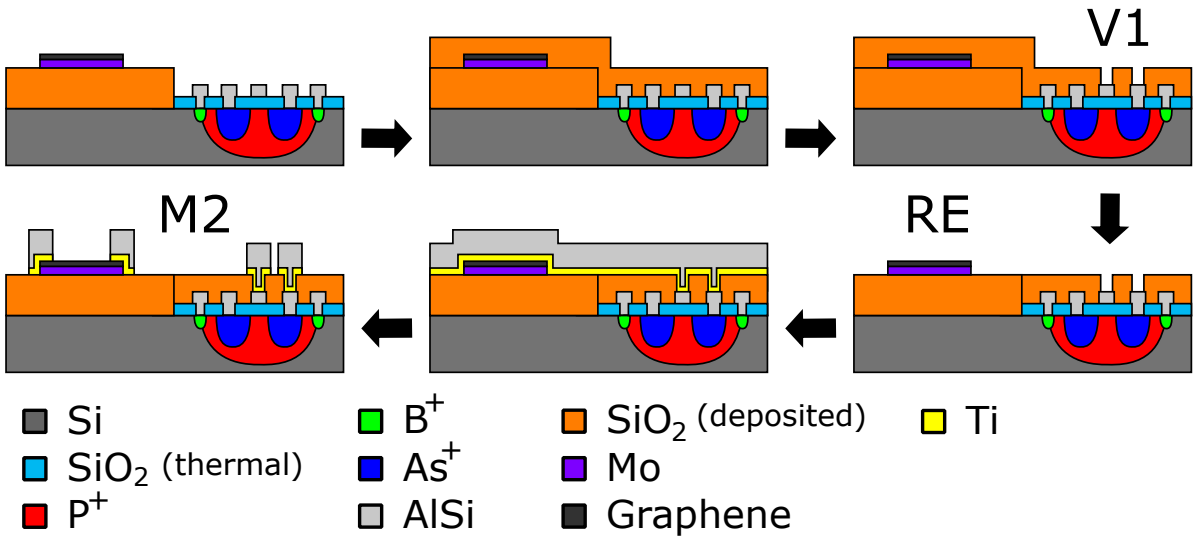


Figure 6.5: Implementation of the dielectric and second metal layer. The dielectric is formed by TEOS SiO_2 deposition. The vias are dry etched, followed by wet etching the Mo and graphene stack clear in a 40 % BHF solution. A 40 % BHF dip is performed prior to the metal deposition of 100 nm Ti layer with a 1 μm AlSi that is then etched by dry etching the AlSi and wet etching the Ti in a 0.55 % HF solution.

Wafer-scale measurements are now performed on wafer 7, which reveal operating devices. The threshold voltage results of the benchmark devices of size 20x5 are depicted in Figure 6.6. The NMOS and PMOS threshold voltages are $\sim$ 0.5 V and $\sim$ 0.2 V less compared to the results after first metal implementation respectively. Furthermore, the yield is reduced significantly. It is concluded that Ti potentially induces a high stress that damages the gate oxide and shifts the threshold voltage and should therefore not be used in future implementations.

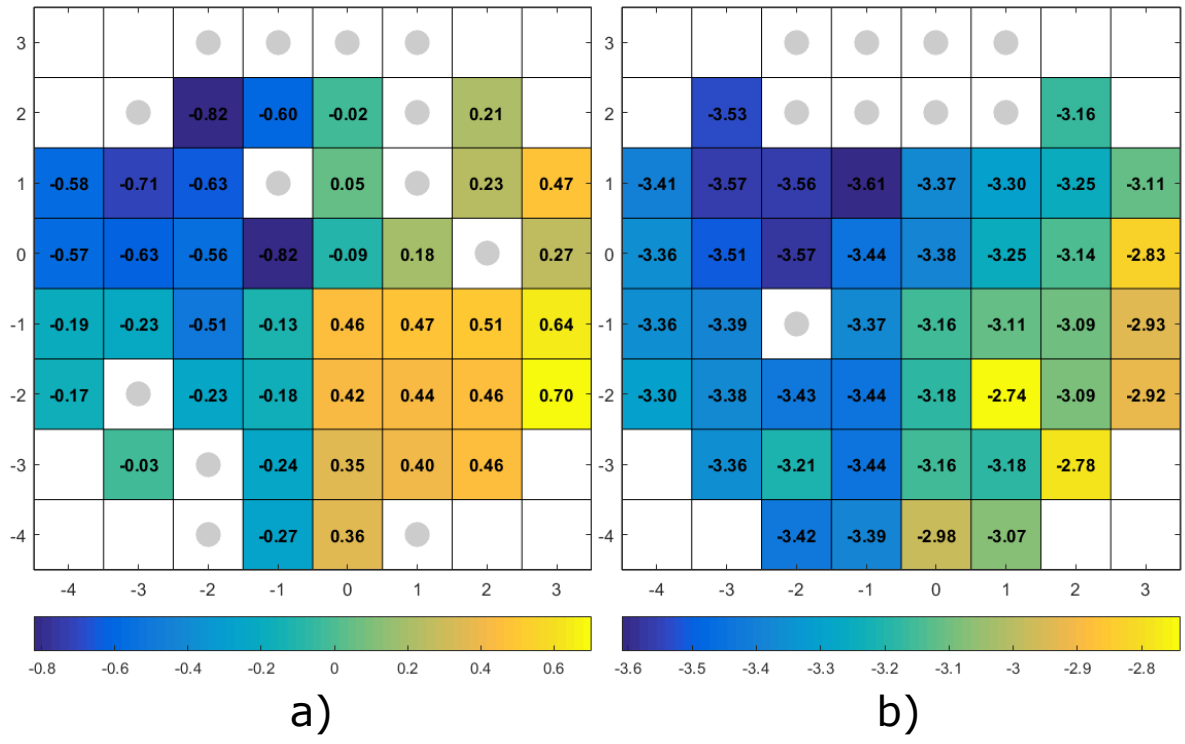


Figure 6.6: Wafermaps depicting threshold voltage [V] of NMOS 20x5 in a) and of PMOS 20x5 in b). Broken devices are marked with a grey circle. Measured on W7.

Wafer-scale measurements of the sheet resistances on wafer 7 are listed in appendix F.9. Values of 0.1 Ω, 0.03 Ω, 38 Ω and 89 Ω are found for the M1, M2, SN and SP respectively. Just the SN sheet resistance decreased compared to the reference wafer, while the SP decreased as well during the training run.

6.5. Pirani Pressure Sensor Cavity Etch and Release

The final processing steps that form the suspended graphene strip are illustrated in Figure 6.7. The cavity is etched under the Mo and graphene stack in the TEOS deposited SiO_2 by wet etching in a BHF solution with photoresist as mask. The photoresist is stripped in acetone, followed by wet etching the Mo in H_2O_2. Then CPD is performed resulting in suspended graphene strips alongside a PMOS device with two metal layers. The full illustration of all process steps is given in appendix Figure F.10. Note that the wafer has to be diced prior to the cavity etch as the CPD tool is only capable of processing single dies. The lithography prior to the cavity etch can be performed on wafer-scale. The full flowchart of wafer 7 is listed in appendix Table F.1 and gives details on recipes used at EKL.

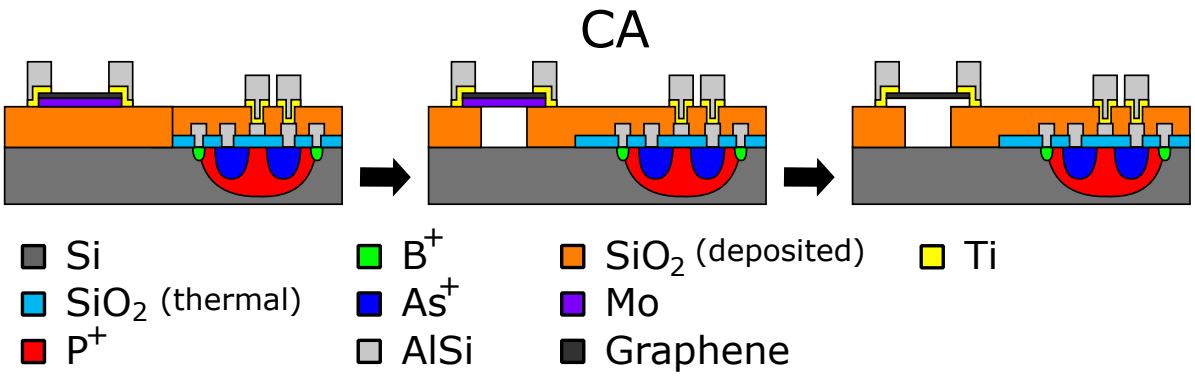


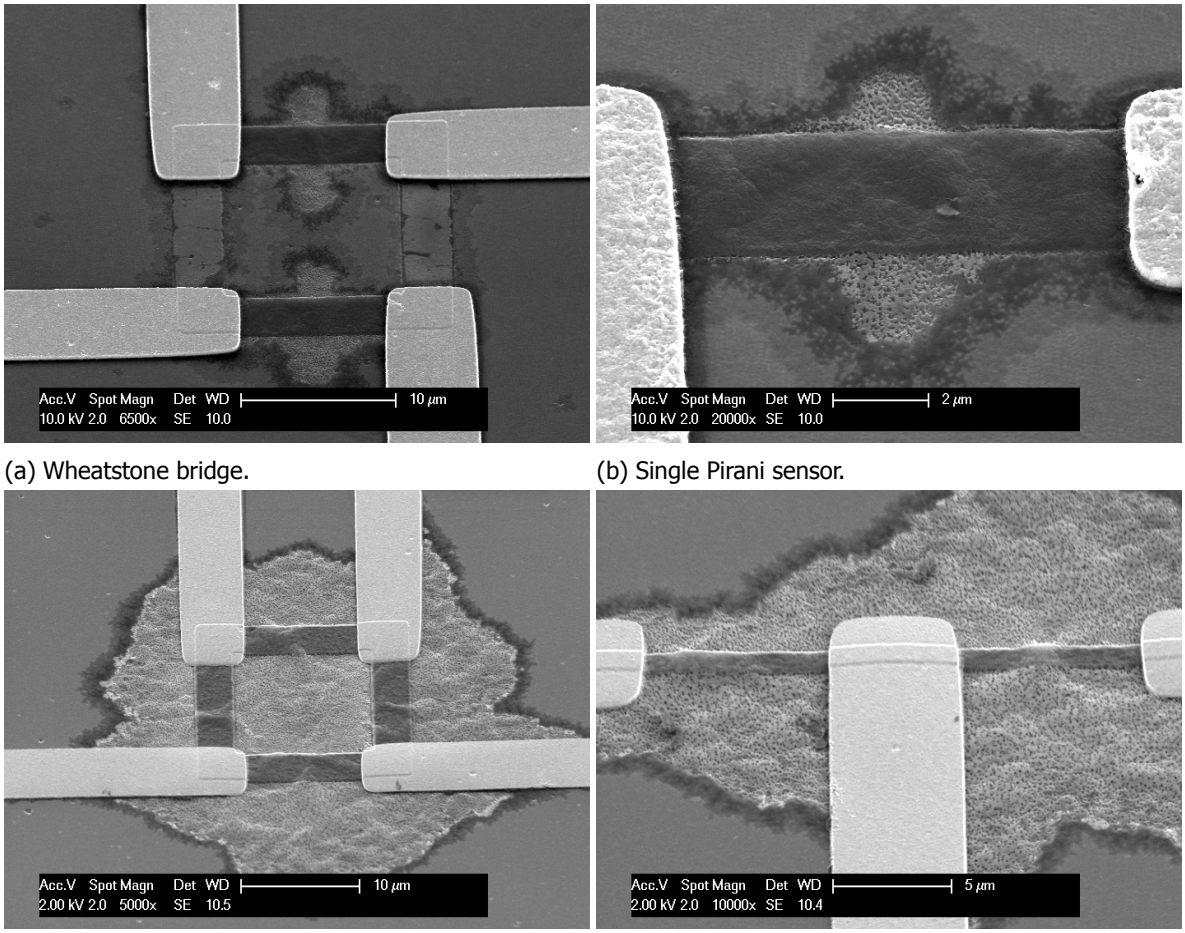
Figure 6.7: Release of the graphene strips by etching the cavity in the TEOS deposited SiO_2 under the gaphene strip. This is followed by the wet etching of Mo in H_2O_2 and CPD and results in a suspended graphene bridge alongside a PMOS device with two metal layers.

Even though wafer 5 has a corroded first metal layer and bad electrical contact between the first and second metal layer, an attempt is made to perform the release by etching the cavities under the graphene strips. Three different etch times are used for the three different bridge widths in the design, which are 1, 2 and 3 minutes. Unfortunately, the results on wafer 5 are not good. SEM images of the results on wafer 5 are depicted in Figure 6.8.

The images in Figure 6.8a and 6.8b depict devices on the die that was etched for 1 minute. The first image in Figure 6.8a depicts a Wheatstone bridge with a length of 4 μm and width of 3 μm. The image reveals some layer on top of the unexposed graphene as it is of the same color as the field oxide. Furthermore, the cavities are not etched all the way through the TEOS deposited SiO_2 layer. The etchant appears to have under etched the entire graphene strip which should only partially be suspended. The image in Figure 6.8b of a single Pirani sensor shows more clearly that the etchant has reached all the way up to the metal connections, while it should only have etched the cavity. Such behavior has not been observed in the first batches of Pirani sensors characterized in Chapter 3.

The images in Figure 6.8c and 6.8d depict devices on the die that was etched for 2 minutes. The images show a large crater that suggests that these devices are over etched. However, despite the large area the craters are not etched all the way through the TEOS deposited SiO_2 layer. From these observations it is concluded that the etchant hardly reaches the SiO_2 that is to be etched, but the amount of etchant that does reach it is not removed by the rinsing step which results in over etching at the surface. Therefore, it is assumed that a very thin and porous layer lies over the entire wafer. This could well be photoresist residue as the cleaning step after the graphene protection during the first metal layer implementation proved to be difficult.

Wafer 7 is cleaned more extensively to reduce the amount of photoresist residues after the second metal layer implementation, although residues still remain. This allowed for accurate oxide thickness measurements using reflectometry during the wet etching to clear the Mo and graphene stack. This was not the case for wafer 5, confirming the presence of a residue layer.



(a) Wheatstone bridge.

(b) Single Pirani sensor.

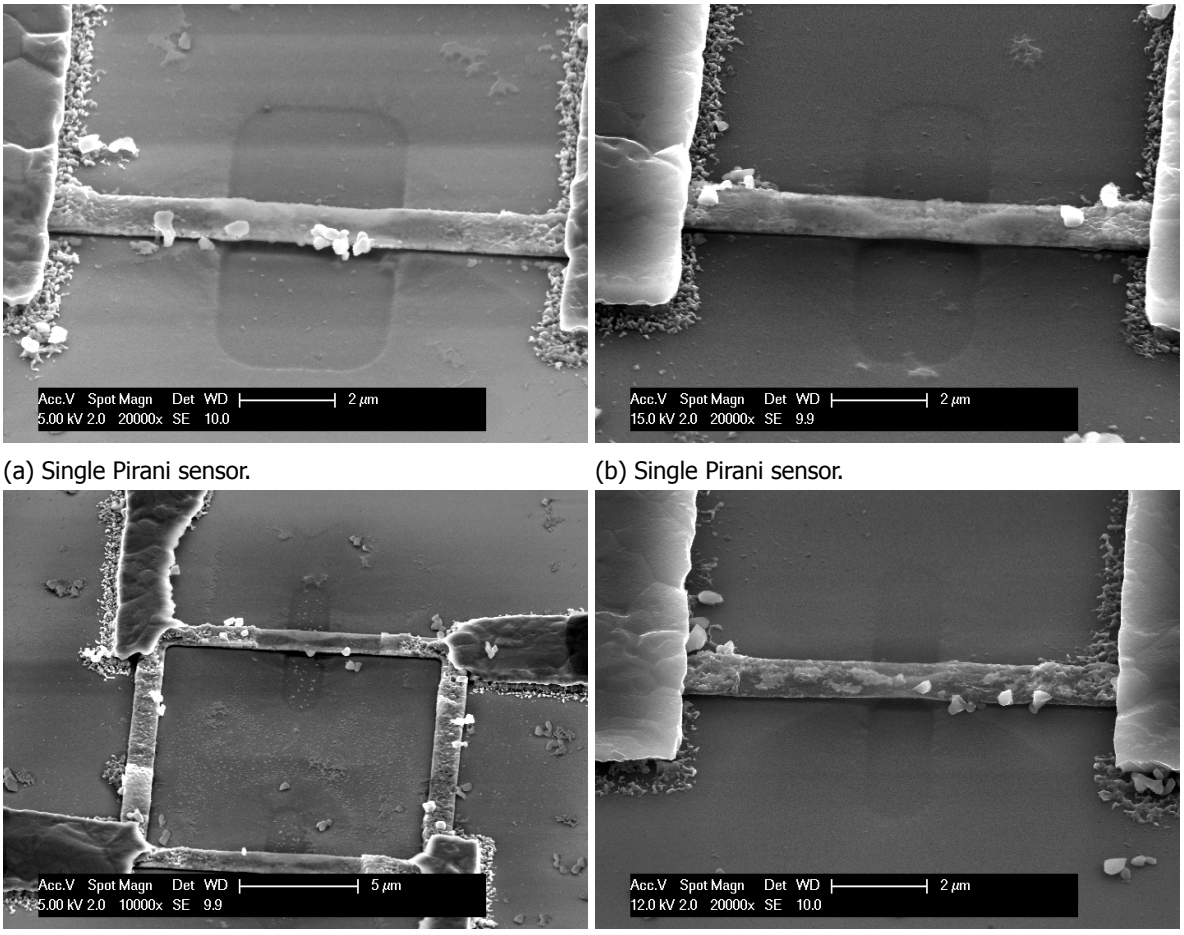
(c) Wheatstone bridge.

(d) Additional test structure.

Figure 6.8: SEM images of graphene structures on wafer 5 consisting of Wheatstone bridges and single Pirani sensors. The structures in a) and b) were etched for 1 minute and the structures in c) and d) were etched for 2 minutes.

The SEM images listed in Figure 6.9 depict Pirani pressure sensors on wafer 7. It is clear that wafer 7 does not suffer from the crater phenomena of wafer 5. Furthermore, the cavities are etched on the intended locations. The metal traces as well as the graphene are covered with debris that is likely to be metal residue or TEOS deposited SiO_2. Furthermore, the metal traces are damaged due to the over etched Ti. Fortunately, the graphene strips appear to be suspended although it is difficult to observe due to the debris. Additionally, the cavity bottom does not look like bare silicon, instead it looks like SiO_2. This could be thermal oxide that has formed under the TEOS deposited SiO_2 during the gate oxidation step.

The etch stop at thermal oxide could be solved by implementing both field oxides in thermal oxide. This ensures that all oxide under the graphene strip is of the same kind with equal etch rate. The wet etching of Ti is very aggressive and the over etch has severe damaging effects on the metal traces. Furthermore, the process would benefit from a method to cover the Mo and graphene stack to allow better cleaning during the process after graphene deposition.



(a) Single Pirani sensor.

(b) Single Pirani sensor.

(c) Wheatstone bridge.

(d) Single Pirani sensor.

Figure 6.9: SEM images of graphene structures on wafer 7 consisting of Wheatstone bridges and single Pirani sensors. The structures in a), b) and c) were etched for 3 minutes and the structure in d) was etched for 2 minutes.

6.6. Conclusions

The designed structures and circuits were fabricated on a reference batch without graphene growth processes and a batch containing all processes. Measurements revealed that TiN on top of AlSi in favor of contact resistance induces stress, which curls the metal traces up at the edges and is therefore discarded. The reference wafers in this fabrication run have NMOS threshold voltages that are slightly lower compared to the training run. It is concluded that this is due to differences in epi-layer growth. The PMOS threshold voltage and sheet resistances correspond with the training reference wafer. Furthermore it is concluded that TEOS deposited SiO_2 can be used as dielectric between the first and second metal layer.

The difference in required field oxide thickness for the Pirani pressure sensors and the CMOS devices is solved by TEOS deposited SiO_2 for the Pirani sensors followed by thermal oxidation for the CMOS devices. However, the final inspection after release revealed that it is likely that thermal oxide also forms under the TEOS deposited SiO_2, which causes difficulties in the cavity etch step. This could be solved by implementing both regions in thermal SiO_2. Furthermore, the graphene process steps reduce the gate oxide thickness by 20 nm, which is concluded to not cause difficulties.

The Mo and graphene stack is protected by a photoresist layer. It is found that a post bake is required as the layer will otherwise outgas during coating of the metal layer that is on top. However, it proved to be difficult to remove the photoresist protection layer afterwards, leaving residues on the CMOS areas. Operating devices were measured after the first metal layer implementation.

The dielectric is implemented in TEOS deposited SiO_2, which is found to not destroy the graphene layer. Furthermore, the second metal layer is implemented by a Ti and AlSi stack in favor of better contact resistance to the graphene. Unfortunately, the Ti induced stress that severely shifted the threshold voltages of the CMOS devices. Additionally, the Ti was over etched as this is aggressively etched, causing damage to the metal traces.

Finally, the cavities under the graphene strips is implemented. Inspection reveals metal traces and graphene strips that are covered in debris that is likely to be metal. Nonetheless the graphene strips seems to be suspended. The cavity depth is not as designed as the bottom is not on bare silicon, from which is concluded that thermal SiO_2 forms under the TEOS deposited SiO_2.

7

Implemented Design Characterization and Verification

In this chapter the measurements on the designed circuits are performed on the reference wafer and graphene pirani wafer. Some smaller circuits are performed on wafer-scale first to investigate deviations and yield. This is followed by the dicing and packaging of three dies that are measured on a breadboard. Unfortunately, no pressure dependency measurements on the designed graphene structures are performed, due to a lack of time.

7.1. Wafer-Scale Measurement Results

The inverter logic gate is investigated by determining its switching voltage. This switching voltage is defined to be the input voltage at which the derivative of the output voltage is at its maximum. The measurement results are given in Figure 7.1.

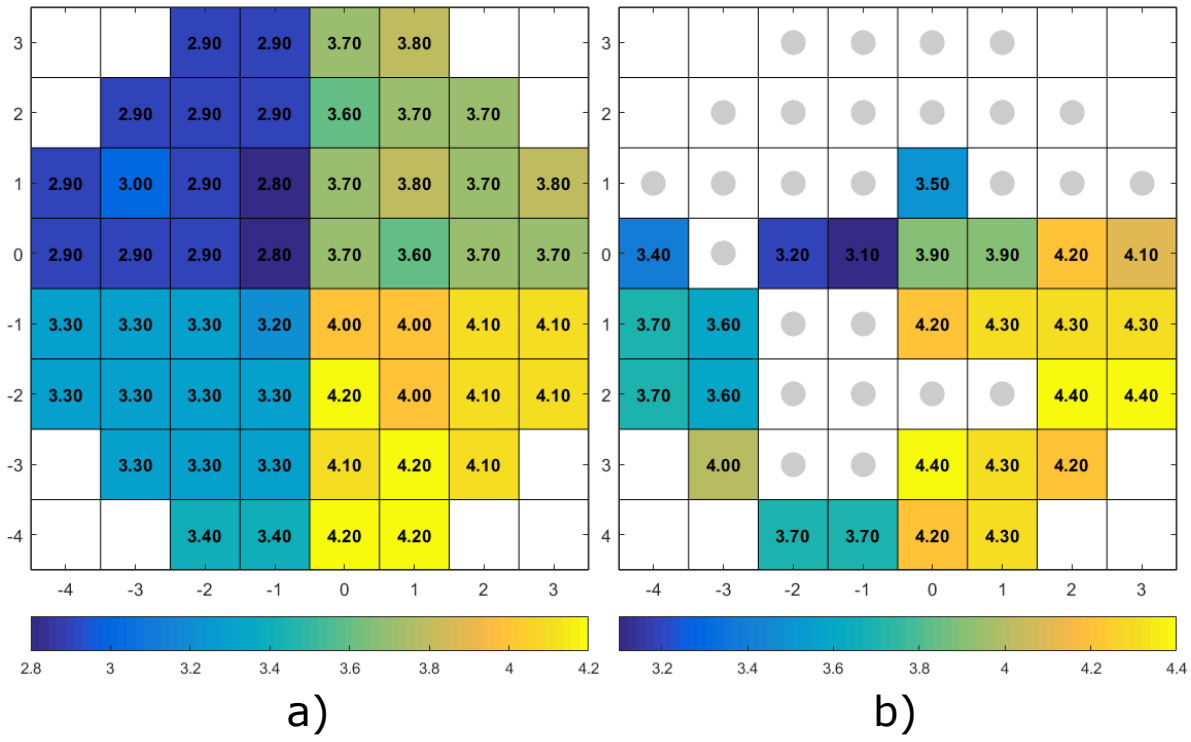


Figure 7.1: Wafermaps depicting inverter switching voltage value [V] of wafer 3 in a) and wafer 7 in b). Broken devices are marked with a grey circle.

The inverters are designed to have a switching voltage of $\sim V_{cc}/2$, which is 5 V. The reference wafermap has a value of 4.1 V in the quadrant with highest voltage adjustment dose, which comes closest to the designed value. The other quadrants have lower switching voltages. Note that all inverters operate on the reference wafer. The yield on wafer 7 is much lower. However, the switching voltage in the wafermap is similar to that of the reference wafer. Even though this wafer underwent more processing steps including graphene growth, the division of two different field oxide regions and difficult cleaning steps. The inverter is concluded to be robust in performance, although the yield has reduced significantly.

The NAND gate is measured and the results are depicted in Figure 7.2. The switching voltage on the reference wafer is lower compared to the inverter with the optimal values in the same quadrant at 3.7 V. Similarly to the inverter results, the results on wafer 7 give a reduced yield with a large correspondence of broken devices in the top half of the wafer. However, the switching voltage of the NAND on wafer 7 is $\sim$ 0.3 V higher compared to the reference wafer, which is closer to the designed value.

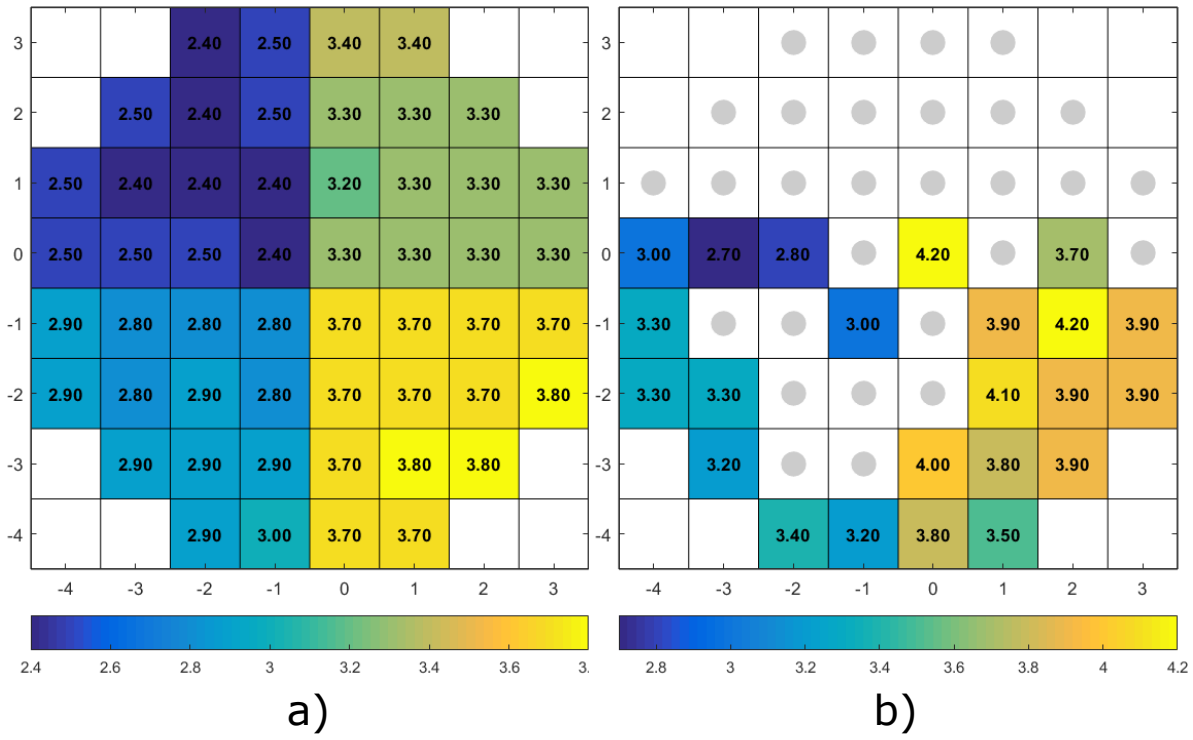


Figure 7.2: Wafermaps depicting NAND switching voltage value [V] of wafer 3 in a) and wafer 7 in b). Broken devices are marked with a grey circle.

The typical response of the NAND is depicted in Figure 7.3. The output should only give a digital zero when both inputs are digital ones. This is indeed the case, with the exception of a spike when both inputs are equal to half the digital one voltage. Since the transition voltage of the NAND is at 3.7 V input values of 5 V result in a zero at the NAND output. However, the input of the NAND is digital which means that this input combination should not occur and is therefore considered acceptable.

Wafer-scale measurements of the NOR gate are listed in appendix Figure G.1. The switching voltage is slightly lower compared to the NAND gate at 3.4 V in the same quadrant. Again the switching of the NOR on wafer 7 is $\sim$ 0.3 V higher compared to the reference wafer. Furthermore, the wafer-scale measurements of the parity check gate are listed in Figure G.2. The switching voltage of the reference wafer is similar to that of the inverter, with similar spikes in the response as the NAND. The yield on wafer 7 is even lower then that of the NAND and NOR gates, but has similar switching voltages as the reference wafer.

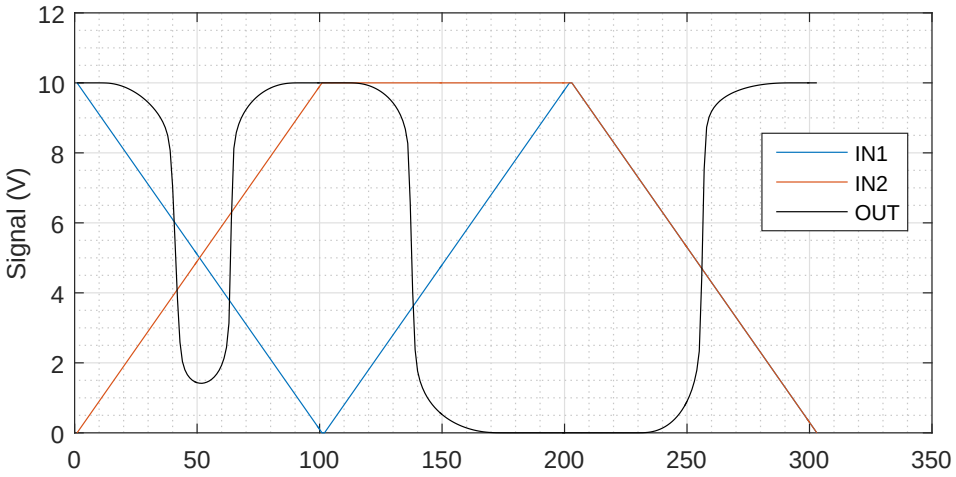


Figure 7.3: Typical transient response of the NAND on wafer 3. Note that the output should be 1101. The x-axis denotes the time in arbitrary units.

The following devices are only measured on the reference wafer due to time constraints to finish the research work. Nonetheless, these devices can be measured on wafer 7 or a new wafer in future work. The wafer-scale measurements of the NW resistor are depicted in Figure 7.4. It is designed to have a resistance of ~ 10 kΩ, derived by using the sheet resistance of 1.6-1.8 kΩ $\cdot \square^{-1}$ and a NW resistor layout of 6 □. The measurement results show a lower value for the NW resistor of approximately 7 kΩ. Unfortunately, the error in the mask design does not allow for measuring the NW sheet resistance to further investigate. However, for the resistive string, the exact value is not crucial. When biasing the resistor differently, the resistance changes. This change is observed to be less than 10 % of the total resistance and is considered to be acceptable for the resistive string.

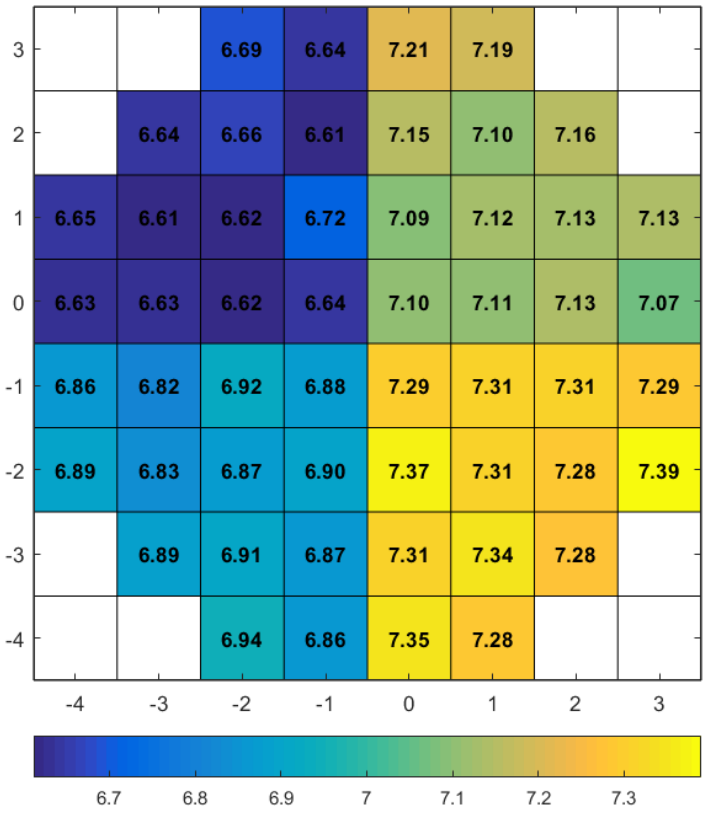


Figure 7.4: NW resistor measurement results in [kΩ]. The resistor was designed for ~ 10 kΩ.

The wafer-scale measurement results of the maximum offset voltage of the comparator is determined and depicted in the wafermap in appendix Figure G.3. The maximum found value is 0.11 V, although the majority of devices has a value lower than 0.05 V. The measured values are therefore considered good as the maximum offset is typically only for the largest reference voltage.

A typical response of the comparator is depicted in Figure 7.5. For higher reference voltage levels, the comparator does no longer operate. The maximum level lies at 6.0 V in the quadrant that has no voltage adjustment and at 8.0 V in the highest voltage adjustment quadrant. During simulation, the maximum was set at 8.4 V. The measured value in the quadrant that has the highest voltage adjustment is considered acceptable and devices from this quadrant are therefore desirable to obtain a large input range of the flash ADC.

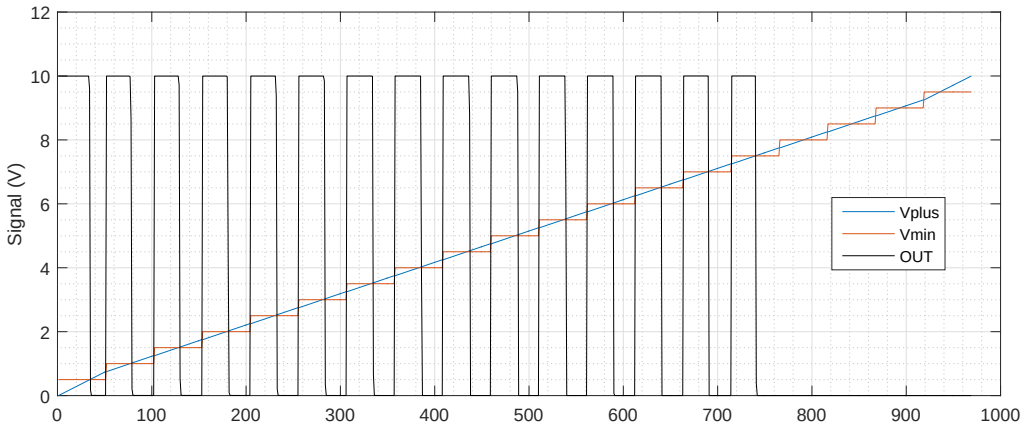


Figure 7.5: Typical response of the comparator on wafer 3 in the highest threshold voltage adjustment quadrant. The x-axis denotes the data number. The devices were biased at 3 V.

The analog test structures on the die allow for measurements on the SF and FCO. However, the measurement setup does only allow DC measurements which means that only measurements on the bias voltages and gain linearity can be performed in the probe station. The FCO analog circuit is measured on wafer 3 in the probe station by determining the correct bias voltages and gain linearity. The range is determined on wafer-scale and depicted in Figure 7.6.

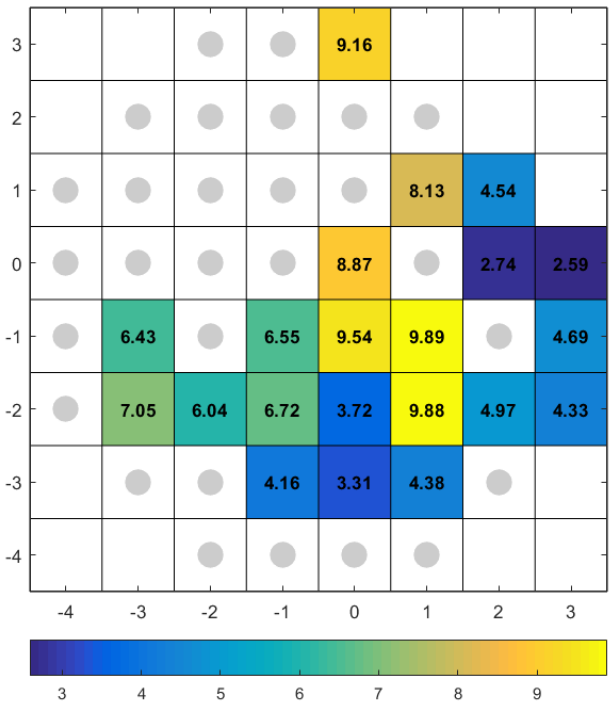


Figure 7.6: Output range of the FCO on wafer 3.

The yield is not high and the found output range is not uniform over the wafer. Furthermore, there are just six dies with a range over 8 V. The bias voltages used during the measurements are listed in Table 7.1. Bias voltage V_{b2} had to be tuned finely to obtain the best results.

Table 7.1: List of used bias voltages during wafer-scale measurements on the FCO for each quadrant on wafer 3.

Bias voltage	**0E11**	**3E11**	**6E11**	**9E11**
V_{b0}	7.4 V	7.2 V	6.8 V	6.3 V
V_{b1}	5.0 V	5.0 V	5.0 V	5.0 V
V_{b2}	0.80 V	0.70 V	0.58 V	0.30 V

An example of a typical output response of one of the six circuits with a range above 8 V is depicted in Figure 7.7. This example has a large range and offset comparable with simulation results and the gain linearity is considered good.

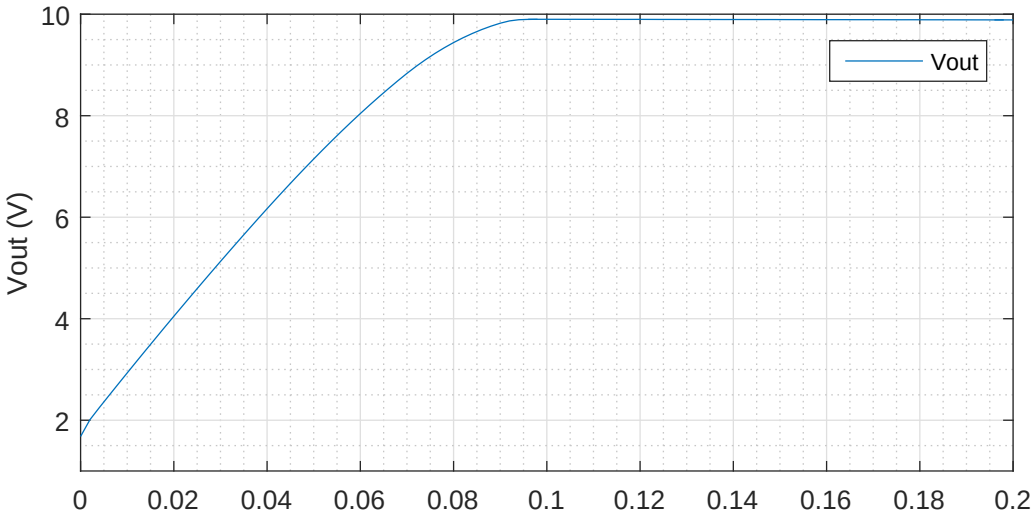


Figure 7.7: Output response of an FCO with a large range in one of the two highest voltage adjustment quadrants. The x-axis denotes the differential input voltage [V].

Finally, the SF analog circuit is investigated on wafer-scale by determining the correct bias voltages and gain linearity. The maximum offset is depicted in the wafermap in Figure 7.8. The yield is much higher than that of the FCO. However, the maximum offset is largest in the highest threshold voltage adjustment dose quadrant which contradicts the preferred 9E11 quadrant so far. However, the operating range is highest in the 9E11 quadrant.

Table 7.2: List used bias voltages during wafer-scale measurements on the SF for each quadrant on wafer 3.

Bias voltage	**0E11**	**3E11**	**6E11**	**9E11**
V_{b0}	0.0 V	1.0 V	1.2 V	1.4 V
V_{b1}	1.1 V	0.8 V	1.3 V	1.7 V

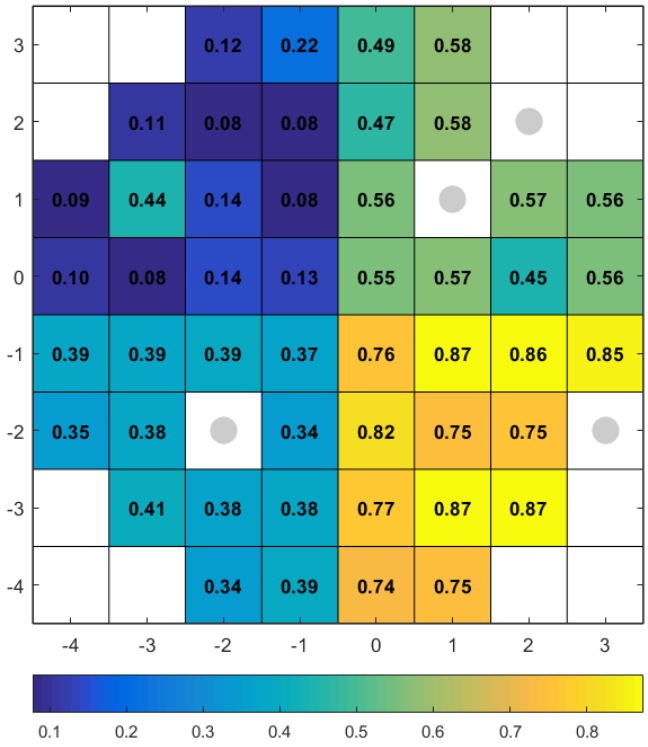


Figure 7.8: Maximum offset voltage of the SF on wafer 3.

An example of the typical output response of the SF in the highest threshold voltage adjustment dose quadrant is depicted in Figure 7.9. From the plot it is quickly observed what the cause of the large maximum offset is. This maximum occurs for small input voltages. Since the threshold voltages are not the same in each quadrant, the saturation regime of the devices is different. While all the NMOS in the design are directly biased, the PMOS are only indirectly biased. This has impact on the differential pair output, as it is self biased by a PMOS current mirror. The PMOS devices in this current mirror are likely not saturated in the mentioned quadrants, which results in the incorrect output of the SF.

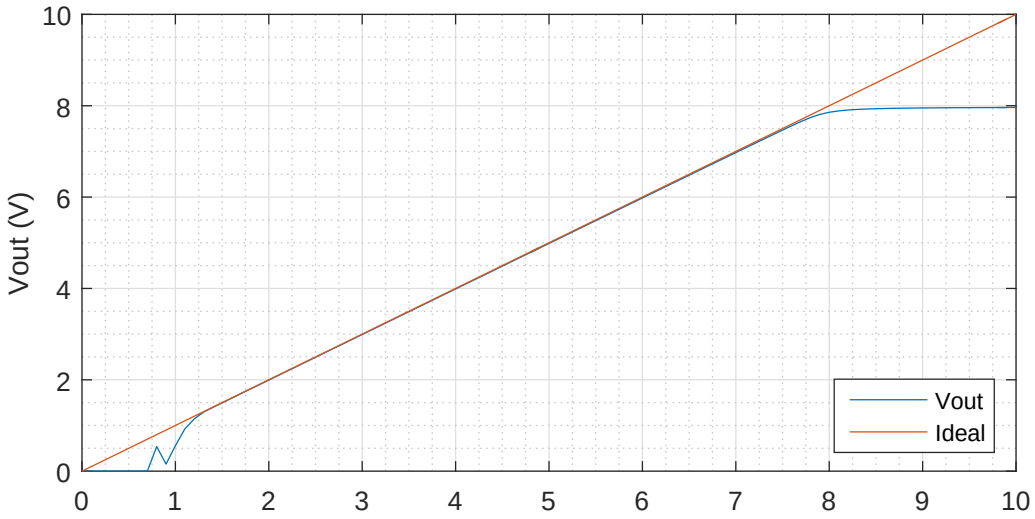


Figure 7.9: Output response of an SF with a large range in one of the two highest voltage adjustment quadrants. The x-axis denotes the input voltage [V].

7.2. Single Die Measurement Results

After the dicing of wafer 3, the larger circuits are wire bonded in order to investigate their operation. A disadvantage of this, is that no yield or wafer uniformity is monitored. The limitation of the wafer-scale measurements is that the probe station has six needles and can be modified to eight needles, which is not enough for most of these circuits. Furthermore, the probe station is not capable of AC analysis required for the analog blocks. Dies (0,-1), (1,-1) and (1,-2) are wire bonded for the different circuits as these have best results for the FCO in the wafer-scale measurements. The packaged dies are placed on a breadboard and connected to the power supplies and measurement equipment available at the Tellegen Hall in EEMCS.

The thermometer encoder is investigated first. The yield of the thermometer encoder is estimated at ~ 55 %, by using the wafer-scale results of the logic gates. All expected input combinations for the thermometer encoder are applied, while monitoring the output. The results of the three dies are listed in Table 7.3 which reveals that two out of three dies work perfectly, which corresponds with the estimated yield. The thermometer encoder on die (0,-1) does not work perfectly as B[1] is sometimes high when it should be low. This error is marked in red and is concluded to be related to T[6]. Furthermore, the circuit draws significantly more current on this die when T[6] is high. No visual damage on the circuit is observed.

Table 7.3: List of measurement results of the thermometer encoders on dies (0,-1), (1,-1) and (1,-2) on wafer 3. All expect input combinations T are applied while monitoring B[0:3] OF. Wrong output values are marked in red.

Input string T[0:15]	Die (0,-1)	Die (1,-1)	Die (1,-2)
1111111111111111	0100 0	0000 0	0000 0
1111111111111110	1100 0	1000 0	1000 0
1111111111111100	0100 0	0100 0	0100 0
1111111111111000	1100 0	1100 0	1100 0
1111111111110000	0110 0	0010 0	0010 0
1111111111100000	1110 0	1010 0	1010 0
1111111111000000	0110 0	0110 0	0110 0
1111111110000000	1110 0	1110 0	1110 0
1111111100000000	0101 0	0001 0	0001 0
1111111000000000	1101 0	1001 0	1001 0
1111110000000000	0101 0	0101 0	0101 0
1111100000000000	1101 0	1101 0	1101 0
1111000000000000	0011 0	0011 0	0011 0
1110000000000000	1011 0	1011 0	1011 0
1100000000000000	0111 0	0111 0	0111 0
1000000000000000	1111 0	1111 0	1111 0
0000000000000000	0000 1	0000 1	0000 1

The next investigated circuit is the comparator array. From the wafer-scale yield of a single comparator it is estimated that the array has a yield of ~ 1 %. Unfortunately, no measurement results can be given as the array was broken during measurements which corresponds with the expected yield. Some important observations that were made before the circuit broke are given. The array was connected to an off chip resistive string made out of 10 kΩ resistors and the range of reference voltages was set to 8 V. However, when connecting the resistive string to the comparator array, the reference voltages dropped significantly. This suggest that a significant amount of current is flowing into the gates of the differential input compared to the current through the resistive string. The current through the resistive string is ~ 50 μA, while the current flowing into the gate of single CMOS devices on wafer-scale was measured to be lower than 1 μA. The observation could be due to the faulty comparator array circuits, wire bonding problems or factors induced by the different measurement equipment.

When measuring the same FCO and SF circuits as done in the wafer-scale measurements, the results in the packaged setup do not match. Several observations are made. First of all, the measurement results of the wafer-scale measurements could not be replicated in this setup even when changing the bias voltages. When applying the biasing with bias resistors, the value for V_{b2} of the FCO and both bias voltages of the SF could not be reached as they are too low. Similarly to the results of the comparator array, it is observed that significant currents are flowing in the differential input gates. Since these circuits were not faulty during the wafer-scale measurements, it is concluded that the wire bonding or measurement setup is the cause.

In the single die measurements it was found that just the digital circuit operates. Furthermore the measurement results of analog blocks on wafer-scale could not be replicated in the single die setup. From this it is concluded that future work in the BICMOS process should give priority to wafer-scale measurements of all designed blocks. This implies that there is a constraint with regard to the amount of connections to be probed. On-chip resistors can provide a solution for a resistive string and bias voltages that are not crucial. Furthermore, multiplexers can be employed to switch between signals. Since the digital electronics are concluded to function and prove to be robust, they are recommended over analog circuits.

7.3. Conclusions

Operating logic gates are measured on both the reference wafer and wafer 7 which includes graphene. The switching voltage is lower compared to the designed value and differs between logic gates as it is closest for the inverter and parity check gate and lowest for the NAND and NOR. The wafer quadrant with the best results got the highest voltage adjustment dose. The yield is 100 % on the reference wafer with the exception of the parity check gate that has two broken devices. The yield on wafer 7 is less than half of that, but broken gates correlate to similar dies. In conclusion, digital circuits alongside graphene have been realized. The other devices and circuits are not measured on wafer 7 due to time constraints, but can be measured in future work. The spare wafers could be processed according to the flowchart of wafer 7 in attempt of improving the yield.

The NW resistor functions, but has a lower value than designed. For the resistive string this is no problem as the exact value of the used resistors is not important as long as they match. Biasing the resistor at different biases changes the resistance, but this is concluded to be of acceptable magnitude. Wafer-scale measurements of the comparator reveal a lower yield compared to the digital circuits, but the offset voltage is deemed acceptable. The FCO results show a low yield with just six devices that have an output range larger than 8 V. Furthermore, the SF results have a high yield, but the devices in the quadrant with highest voltage adjustment dose show the largest output offset. This contradicts the observation of other circuits that perform best in this quadrant.

Single die measurements on three dies are performed and show operating thermometer encoders. Unfortunately, the comparator array has a too low yield to be successfully measured. Additionally, the FCO and SF measurement results on wafer-scale could not be replicated in the single die measurements. It is concluded this is due to wire bonding difficulties or differences in measurement setup. In future work in the BICMOS process, wafer-scale measurements should have priority which limits the maximum amount of probe connections of each test block.

8

Conclusions and Recommendations

This chapter lists the obtained research conclusions of all design stages. These conclusions are then applied to the research questions. Finally, the research work is closed by posing several recommendations for future work.

8.1. Summary of Research Conclusions

The proposed Pirani sensor fabrication method does not incorporate a wafer-to-wafer transfer step. The graphene is implemented by selective CVD growth on patterned Mo, which is front end and BEOL compatible. The cavity depth is defined by the thickness of a SiO_2 layer, which allows for tuning the gap to design for a specific operating range. In this research work a constant cavity gap of 0.6 μm is used. The graphene-based Pirani devices can be made smaller than current state-of-the-art implementations due to the high area-to-mass ratio.

The operational pressure range of a Pirani pressure sensor is determined by Knudsen's number which indicates the heat transfer regime. The found limits of Knudsen's numbers are used in the derived equation for the pressure such that the operational pressure range limits are obtained. This equation is furthermore dependent on the gas composition and the Pirani sensor gap depth. The cavity depth in this work results in an operating pressure range of $1.5 \cdot 10^1$ mbar to $1.5 \cdot 10^3$ mbar. The Pirani pressure sensor resistance is defined by an analytical model and the model parameters are grouped.

Two batches of graphene-based Pirani pressure sensors without integration with electronics are measured. This led to world's first graphene-based Pirani pressure sensors. The largest maximum resistance change that is observed is 2.8 % at a bias voltage of 15 V. Furthermore, the lowest power consumption is 0.9 mW at a bias voltage of 9 V and a maximum resistance change of 0.8 %. The sheet resistance was found to differ significantly between batches, although Raman spectroscopy revealed that the process itself does not damage the graphene. The thermal conductivity of graphene is left undetermined and therefore the analytical model could not be used to fit to the measurement data.

The BICMOS process is a simple five mask process used in educational purposes at the university. For this reason, it is common practice to incorporate four different implantation doses that shift the threshold voltages of the CMOS devices. This phenomena was clearly observed on a reference wafer, with the most symmetric threshold voltages in the quadrant with highest adjustment dose. In attempt to implement the first metal layer before graphene growth, the metal layer material is investigated. Unfortunately, both Ti and Mo that have high melting points gave negative results and are therefore discarded. The graphene growth step itself was observed to significantly shift the threshold voltages. It is concluded that this is due to a higher fixed charge for surface states after graphene growth in the gate oxide. Furthermore, the SN and SP sheet resistance reduce as result of the graphene growth step. It is concluded that the high temperature at which the growth occurs, activates the dopant atoms in the SN and SP further than is standard in the BICMOS process.

The read-out electronics design consists of a sensor topology, differential amplifier and 4-bit flash ADC. The sensor topology is a Wheatstone half bridge. Equations are derived that allow for the calculation of the temperature increase of suspended and non-suspended graphene and could be used to determine the quality of the design. Furthermore, various test structures are included to determine or correct mismatch errors. The designed opamp in the differential amplifier consists of a folded cascode opamp that provides voltage gain with a source follower at its output to provide current gain. This combination is cascaded with another similar combination to achieve a high

enough open-loop gain of ~ 69 dB, bandwidth of ~ 60 kHz and output range of $\sim 8\ V$ according to simulations. With this opamp, the differential amplifier is set to a gain of ~ 32 dB with an error of 0.4 %, a bandwidth of 200 kHz, output range of ~ 8.4 V and offset of ~ 17 mV according to simulations. Additionally, the 4-bit flash ADC is designed with a tunable input range and has offsets below 10 % of the step size. No bubble correction mechanism is incorporated. The complete layout design and test structures are placed on a 10 mm x 10 mm die design.

The design is fabricated on a reference batch without graphene processes and on wafers that do incorporate the graphene process steps. It is concluded that PECVD TEOS deposited SiO_2 does not destroy the graphene and can thus be used as dielectric between the first and second metal layers. Furthermore, stacking TiN on top of AlSi induces stress issues causing the metal traces to curl up and should not be used. The difference in required field oxide thickness for the Pirani pressure sensors and the CMOS devices is solved by PECVD TEOS deposited SiO_2 followed by thermal oxidation. The Mo and graphene stack is protected by photoresist during the first metal implementation and proved to be difficult to remove afterwards leaving residues on the CMOS areas. Furthermore, the second metal layer is implemented by a stack of Ti with AlSi on top. However, the Ti is concluded to potentially induce stress that damages the gate oxide and shifts the threshold voltages. Finally the cavities under the graphene strips are implemented and inspection reveals that the graphene is covered in debris. Nonetheless the graphene strips seem to be suspended, although the cavity depth is not as designed. It is concluded that thermal oxide formed under the TEOS deposited SiO_2, which etches much slower.

Circuit analysis of the fabricated wafers revealed operating single devices and logic gates on the wafer processed with graphene, although the yield is significantly lower compared to the reference wafer. The switching voltages and NW resistor value are lower as designed. On the reference wafer, larger circuits are measured. The comparator is concluded to operate, but the comparator array does not. The digital thermometer encoder operates as intended. Furthermore, the folded cascode opamp as well as the source follower are not operational after dicing. This contradicts the observed operational devices in wafer-scale measurements.

8.2. Answers to the Research Questions

The additional research question is to be answered first. During this research work, world's first graphene-based Pirani pressure sensors are fabricated and characterized. This means that it is indeed possible to implement graphene-base Pirani pressure sensors. It has the advantage of miniaturization and the low power consumption that follows from this. Both advantages pose new possibilities in the pursuit of a world with smarter devices. This work resulted in a publication, which is listed on page 123-126.

Furthermore, operating logic gates are implemented alongside graphene. Unfortunately, time did not allow for full characterization and inspection. The fabrication process results reveal a solid possibility for the integration of graphene in the BICMOS process. Future work based on the obtained insights in this research could lead to a higher fabrication yield, as well as better reproducibility.

Unfortunately, the analytical model could not be used to fit to the measurement data as too many parameters were left undetermined. The Wheatstone half bridge could be used to determine the temperature increase, which allows for characterization of the difference in ohmic heating of suspended and non-suspended graphene. The result allows for attempts to fit the analytical model to the measurement results.

8.3. Future Work and Recommendations

It was found that the final processing steps regarding the etching of the cavity under the graphene strips landed on thermal oxide, which has a different etch rate compared to PECVD TEOS deposited oxide. In future work, the elevated Pirani sensor oxide could also be implemented by thermal oxide, by implementing this oxide layer before the NW implementation.

Furthermore, it is highly recommended to implement methods to allow for better cleaning after the graphene growth step. Since PECVD TEOS deposited oxide was concluded to not destroy the graphene, it could be used as a protection layer deposited on top of the graphene after the growth step. This should allow for resist stripping in oxide plasma as well as nitric acid cleaning steps. Additionally, a protection layer of PECVD TEOS deposited oxide could be deposited over the CMOS electronics in order to reduce damage during dicing, wire bonding and handling afterwards.

The Wheatstone half bridge allows for the determination of the temperature increase of suspended and non-suspended graphene induced by an electrical current. Attempts can be made to fit the analytical model to the measurement data using the temperature increase results.

A

List of Acronyms

Acronym	Meaning
3mE	Mechanical, Maritime and Materials Engineering
ADC	Analog-to-digital converter
AlSi	99% aluminum and 1% silicon
As^+	Arsenic ion
AS	Applied Sciences
Au	Gold
a.u.	Arbitrary units
B^+	Boron ion
BEOL	Back-end of line
BHF	Buffered hydrofluoric acid
BICMOS	Bipolar junction and CMOS technology
CA	Patterned cavity layer
CMOS	Complementary metal-oxide-semiconductor
CNT	Carbon nanotubes
CO	Contact openings
CPD	Critical point drying
CT	Contacts from the first metal to the silicon
Cu	Copper
CVD	Chemical vapor deposition
DUV	Deep ultra-violet
ECTM	Electronic Components Technology and Materials
EEMCS	Electrical Engineering, Mathematics and Computer Science
EKL	Else Kooi Laboratory
FCO	Folded cascode opamp
FWHM	Full width at half maximum
GR	Graphene layer
H_2O_2	Hydrogen peroxide
HF	Hydrofluoric acid
IC	metal interconnect
M1	First metal layer
M2	Second metal layer
Mo	Molybdenum
N_2	Nitrogen
Ni	Nickel
NMOS	N-type metal-oxide-semiconductor
NW	N-well

The list of acronyms continues on the next page.

Acronym	Meaning
OF	Overflow
P^+	Phosphorus ion
PECVD	Plasma-enhanced chemical vapor deposition
PME	Precision and Microsystems Engineering
PMOS	P-type metal-oxide-semiconductor
RE	Thermal oxide region
QN	Quantum Nanoscience
SEM	Scanning electron microscopy
SF	Source follower
Si	Silicon
SiC	Silicon carbide
SiO_2	Silicon dioxide
SMU	Source-and-measurement unit
SN	Shallow n-type
SP	Shallow p-type
TCD	Thermal conductivity detector
TCR	Temperature coefficient of resistance
TEOS	Tetraethylorthosilicate
Ti	Titanium
V1	Contacts from the second metal to the first metal

B

Background Theory

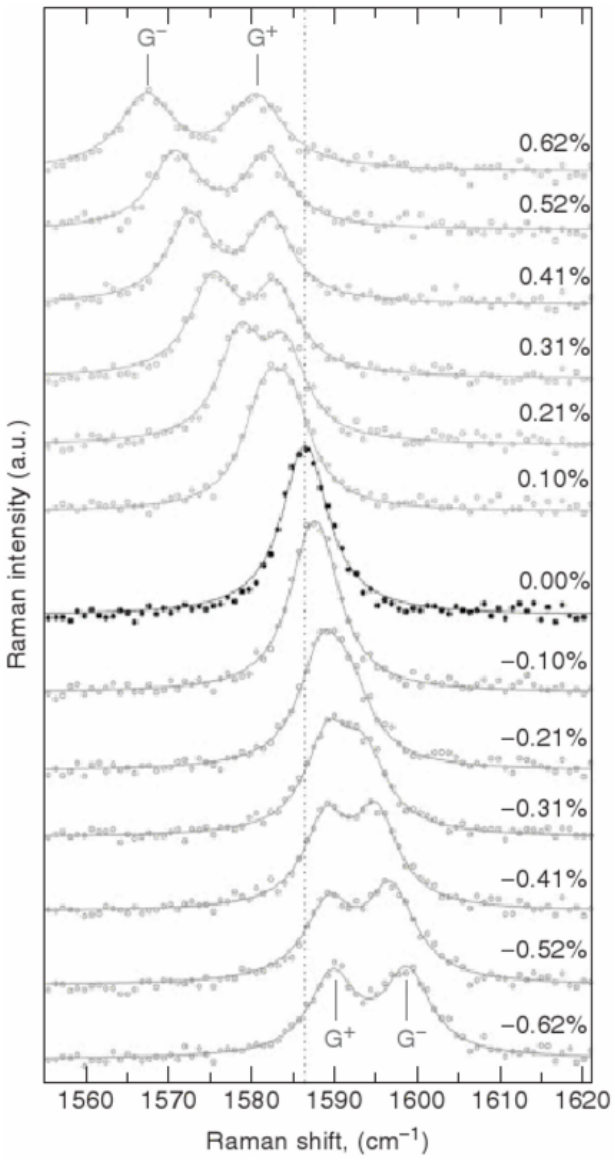
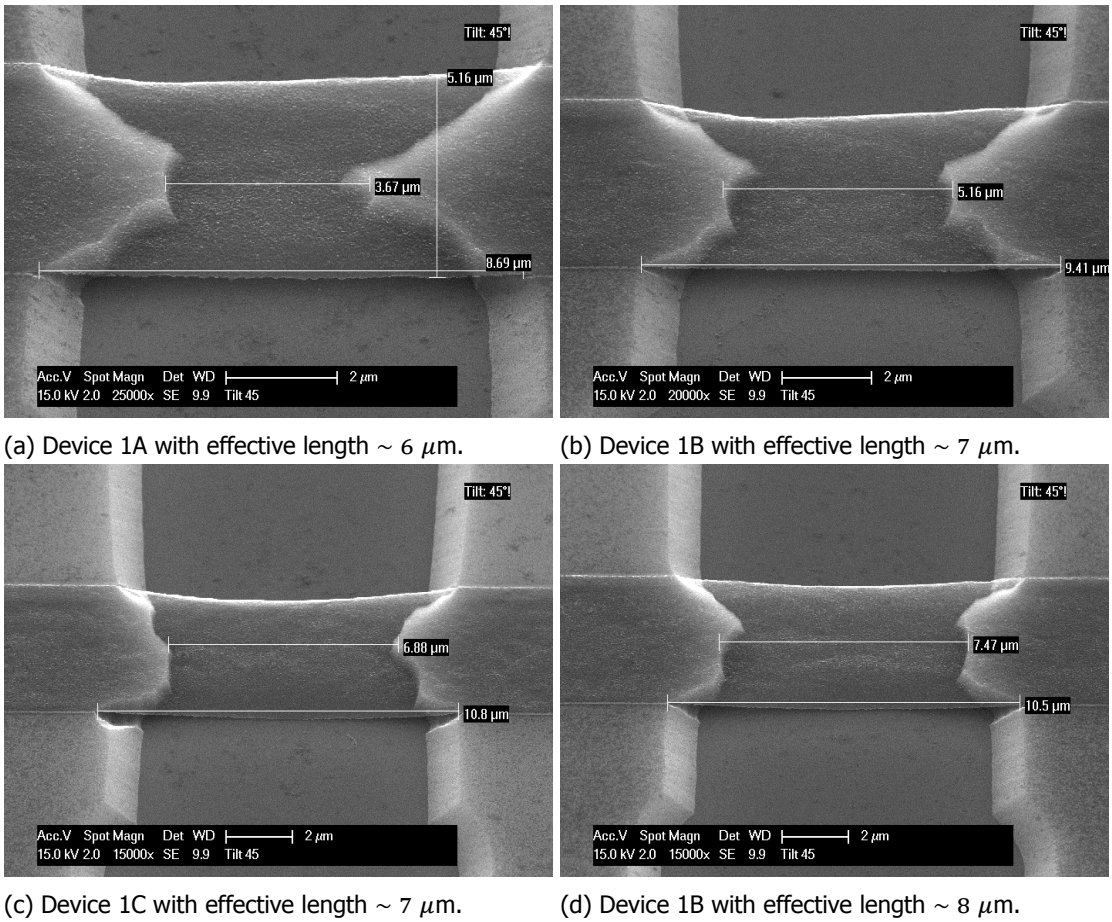


Figure B.1: Moved and split G-peak for different levels of induced tensile or compressive strain. Probed with a 785 nm laser [2]. Note that this is a different laser compared to the Raman spectrum in Figure 2.8.

C

Graphene-Based Pirani Pressure Sensor Characterization



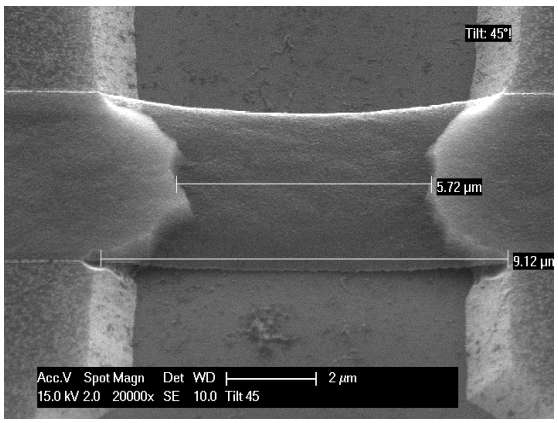
(a) Device 1A with effective length $\sim 6\ \mu$m.

(b) Device 1B with effective length $\sim 7\ \mu$m.

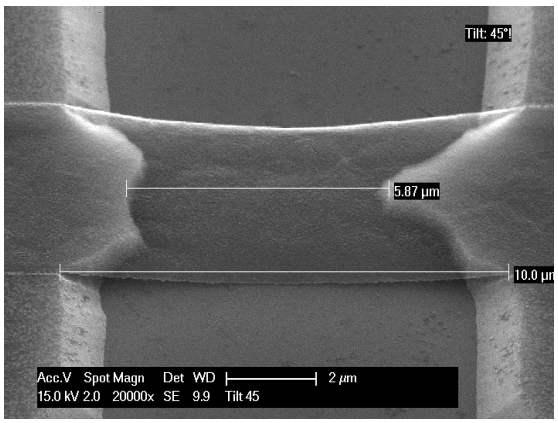
(c) Device 1C with effective length $\sim 7\ \mu$m.

(d) Device 1B with effective length $\sim 8\ \mu$m.

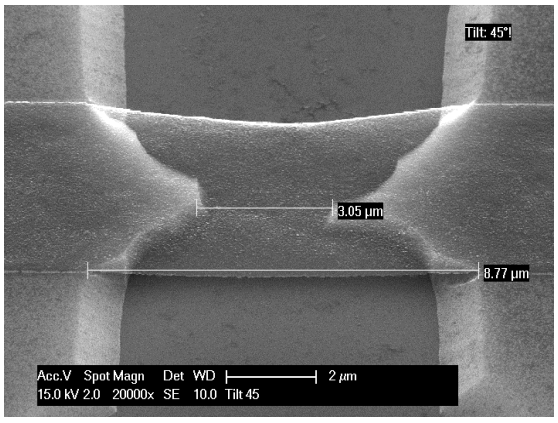
Figure C.1: SEM images of the suspended Pirani pressure sensors on die 1 in the first batch at a tilt of $45°$. All devices have a graphene bridge width of $5\ \mu$m.



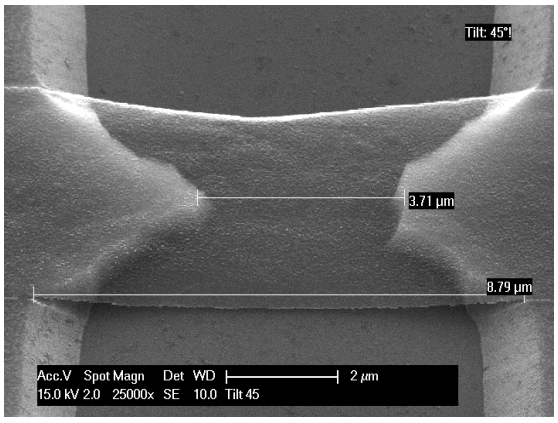
(a) Device 2A with effective length ~ 7 μm.



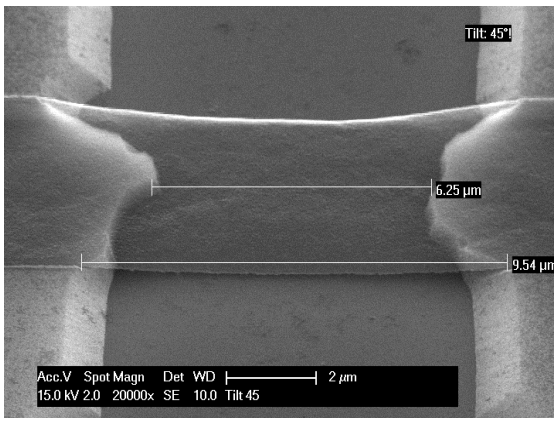
(b) Device 2B with effective length ~ 7 μm.



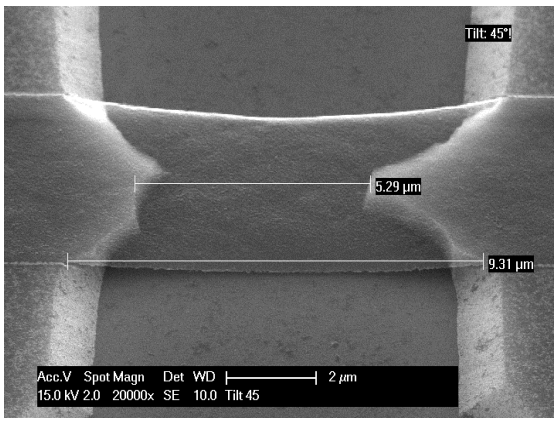
(c) Device 2C with effective length ~ 6 μm.



(d) Device 2D with effective length ~ 6 μm.



(e) Device 2E with effective length ~ 7 μm.



(f) Device 2F with effective length ~ 7 μm.

Figure C.2: SEM images of the suspended Pirani pressure sensors on die 2 in the first batch at a tilt of 45°. All devices have a graphene bridge width of 5 μm.

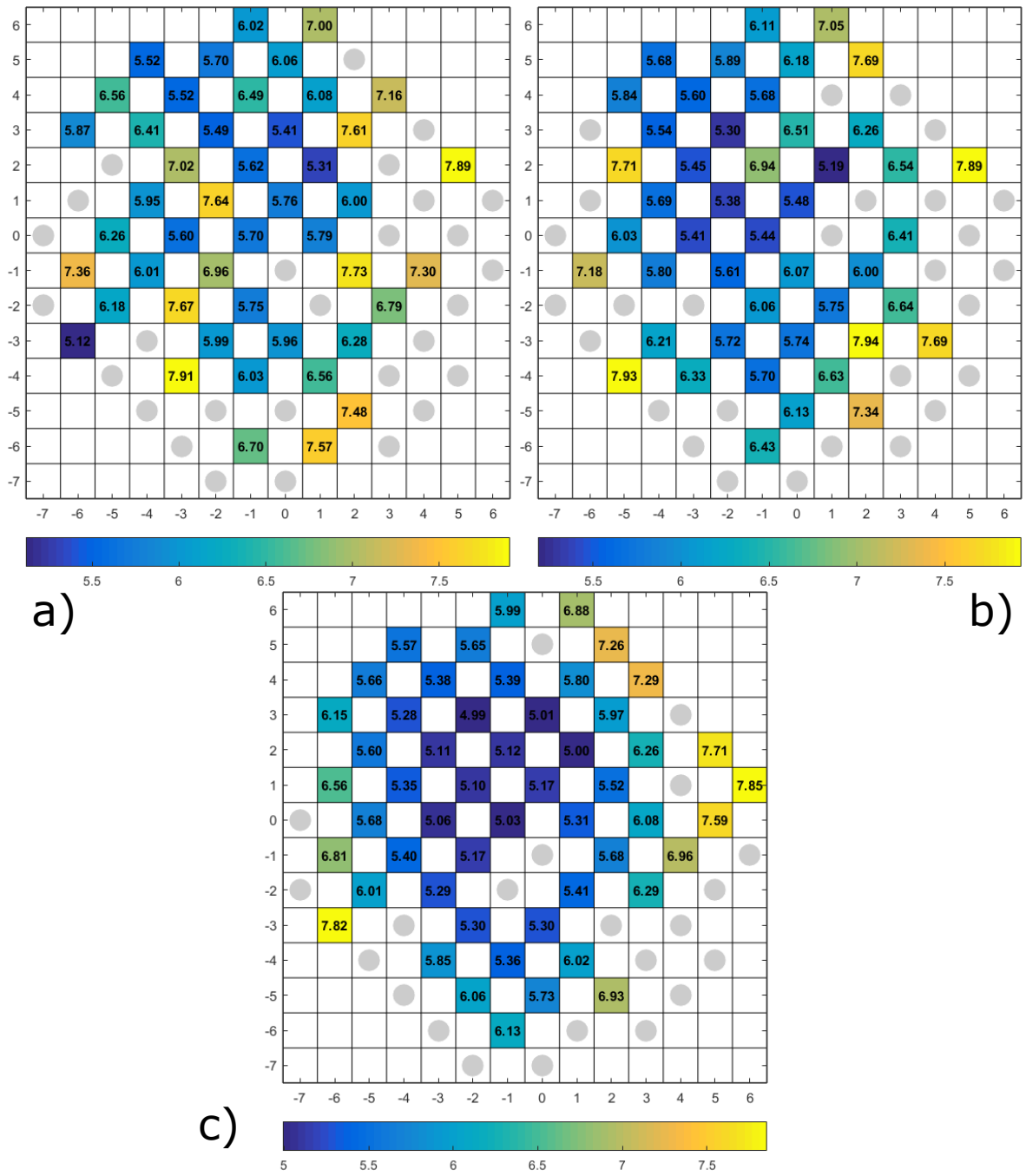


Figure C.3: Wafermaps depicting the sheet resistance $R_{\square}$ of graphene measured on three different aspect ratios during the training run. The strips have a length $206\ \mu$m and width $2\ \mu$m in (a), $5\ \mu$m in (b) and $10\ \mu$m in (c). Broken devices are marked with a grey circle. Measured on W4 in training run batch.

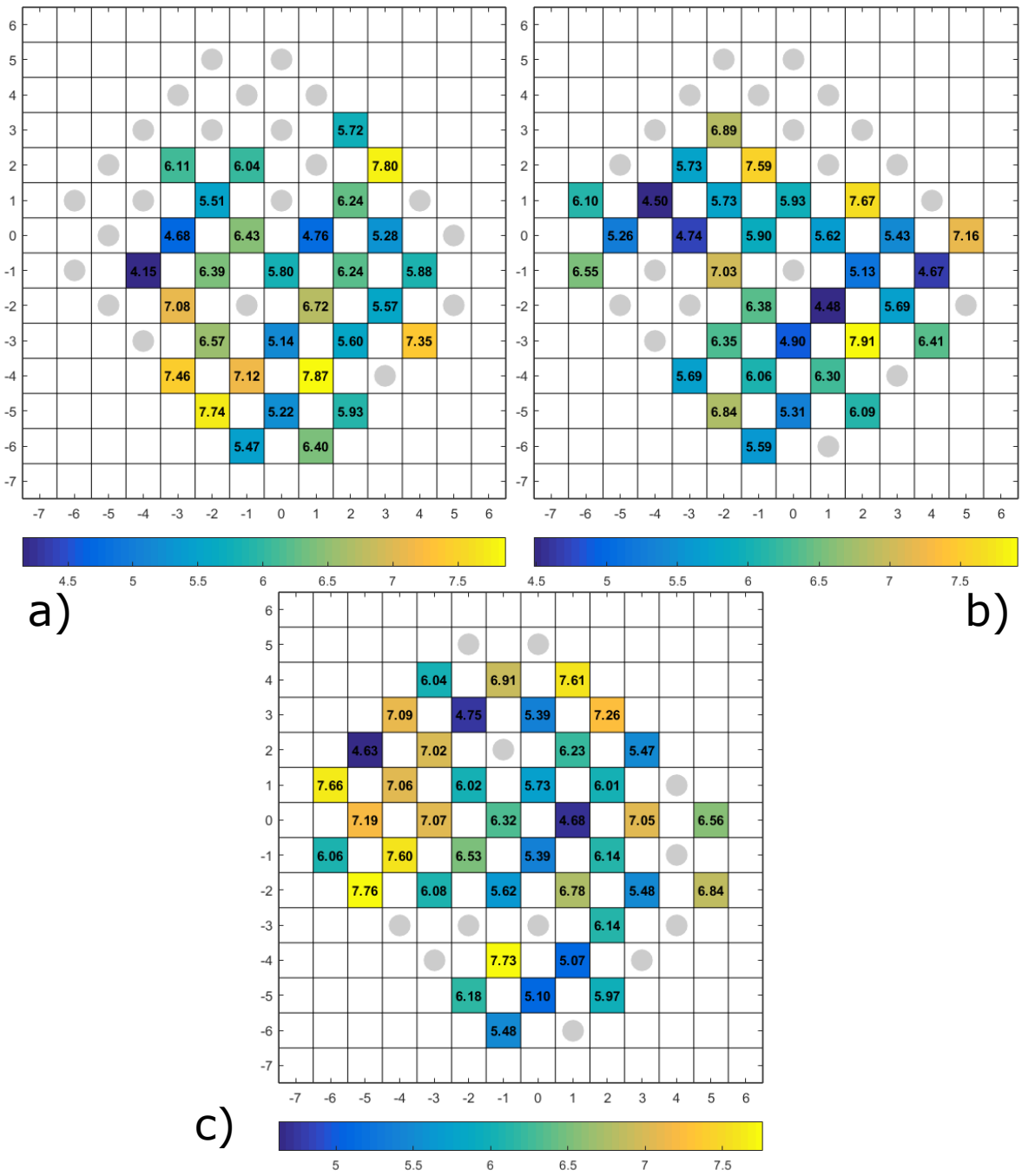


Figure C.4: Wafermaps depicting the sheet resistance $R_{\square}$ of graphene at 60 °C measured on three different aspect ratios during the training run. The strips have a length 206 μm and width 2 μm in (a), 5 μm in (b) and 10 μm in (c). Broken devices are marked with a grey circle. Measured on W4 in training run batch.

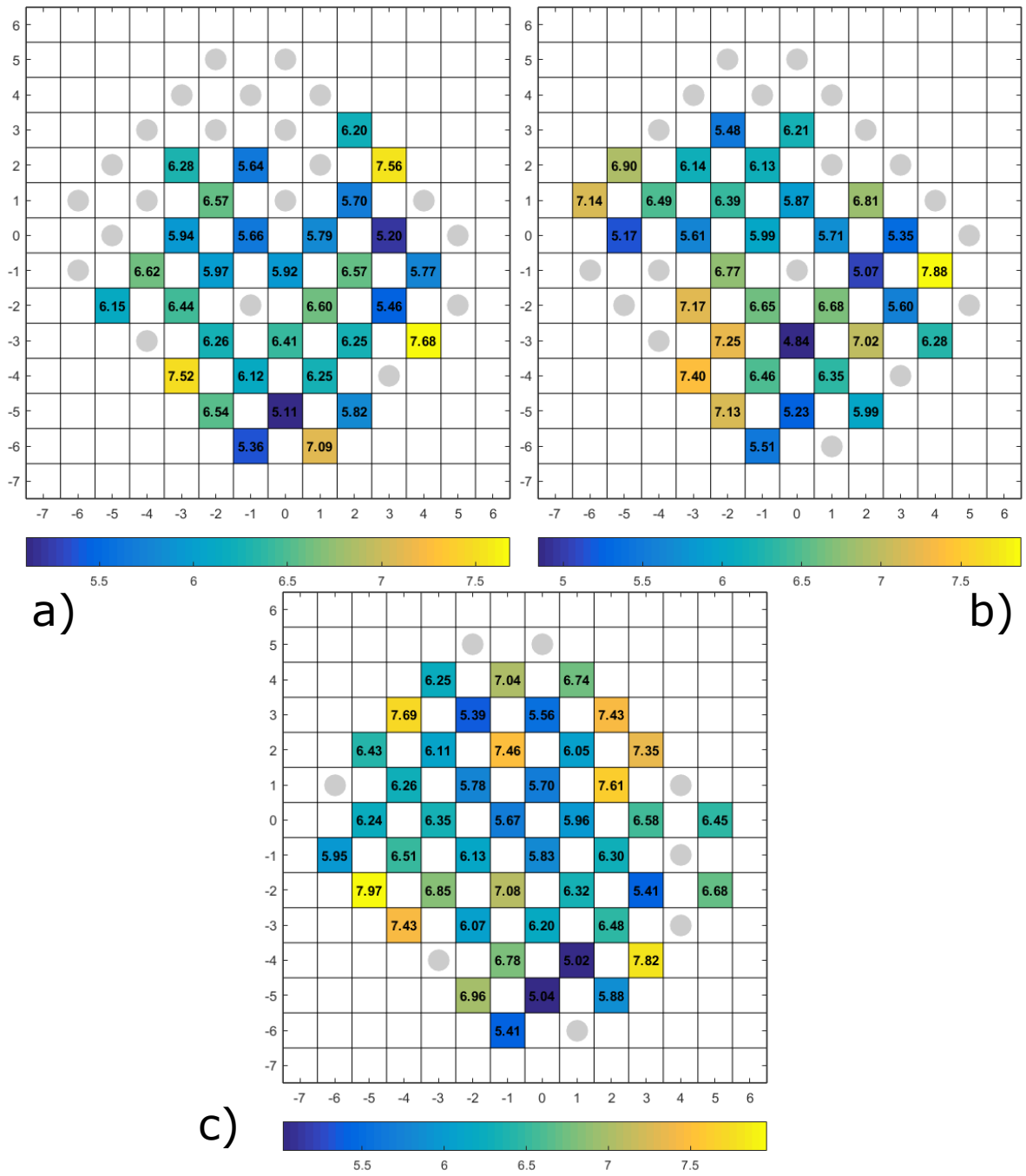


Figure C.5: Wafermaps depicting the sheet resistance $R_{\square}$ of graphene at 100 °C measured on three different aspect ratios during the training run. The strips have a length 206 μm and width 2 μm in (a), 5 μm in (b) and 10 μm in (c). Broken devices are marked with a grey circle. Measured on W4 in training run batch.

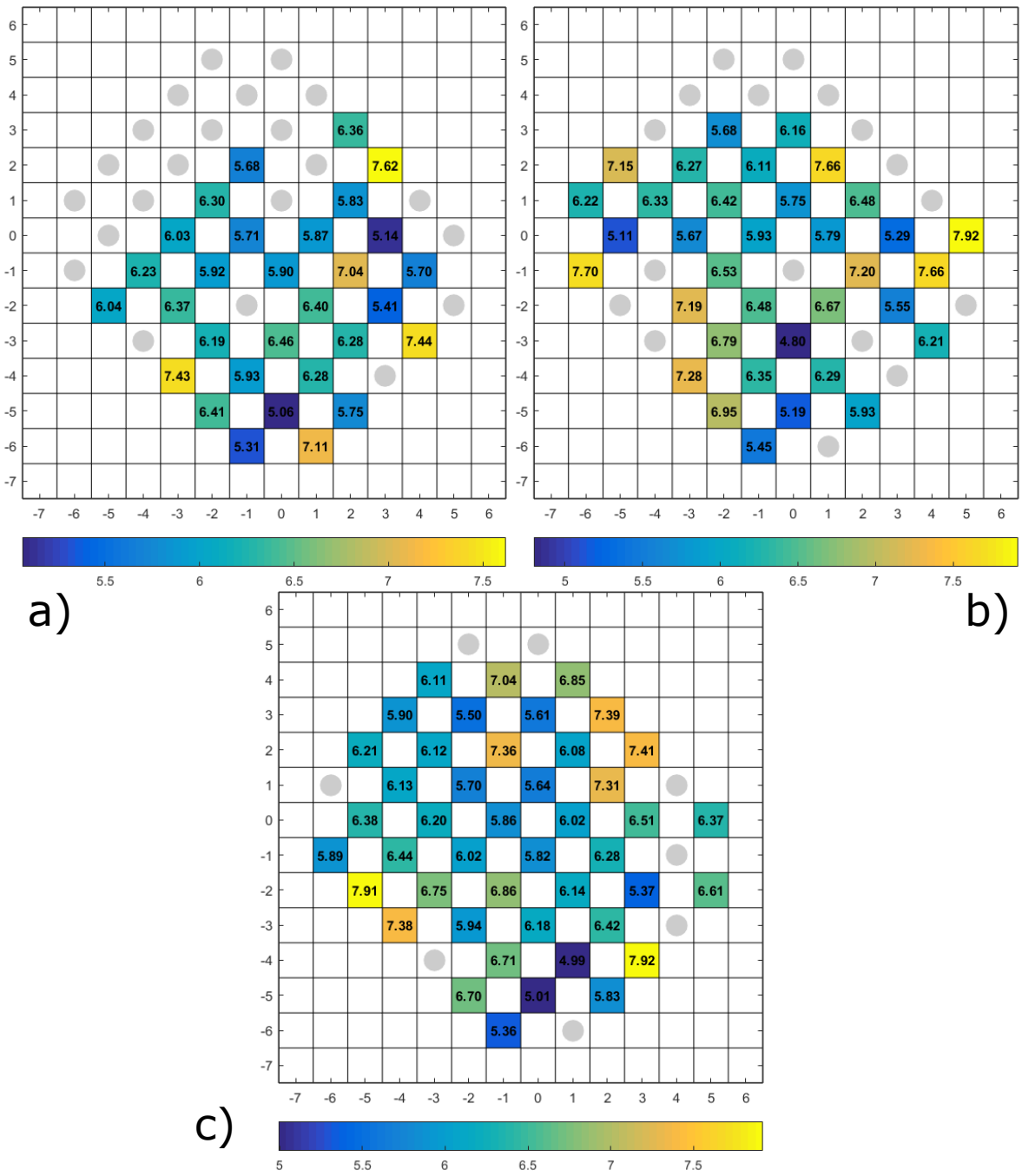


Figure C.6: Wafermaps depicting the sheet resistance $R_{\square}$ of graphene at 130 °C measured on three different aspect ratios during the training run. The strips have a length 206 μm and width 2 μm in (a), 5 μm in (b) and 10 μm in (c). Broken devices are marked with a grey circle. Measured on W4 in training run batch.

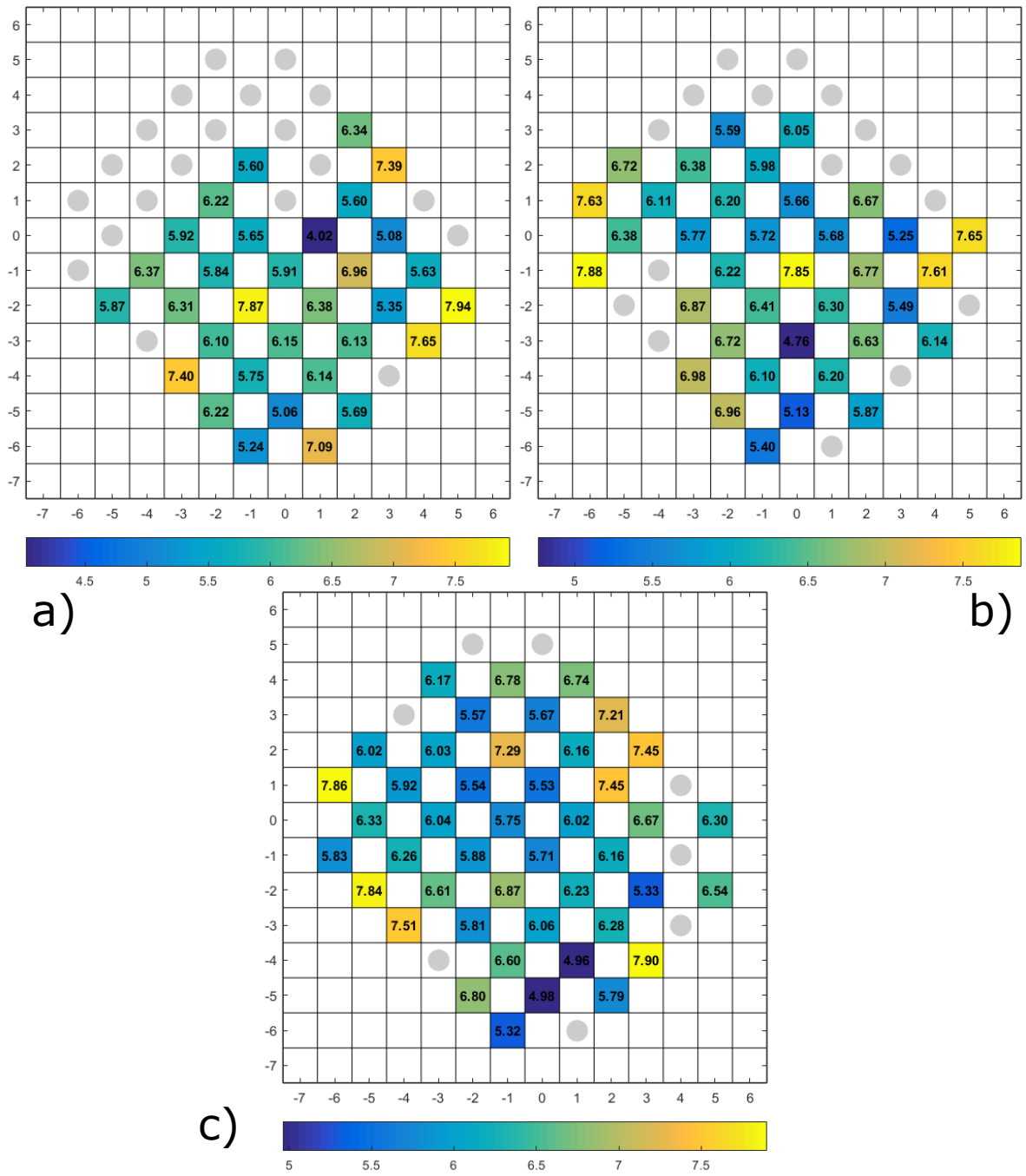


Figure C.7: Wafermaps depicting the sheet resistance $R_{\square}$ of graphene at 160 °C measured on three different aspect ratios during the training run. The strips have a length 206 μm and width 2 μm in (a), 5 μm in (b) and 10 μm in (c). Broken devices are marked with a grey circle. Measured on W4 in training run batch.

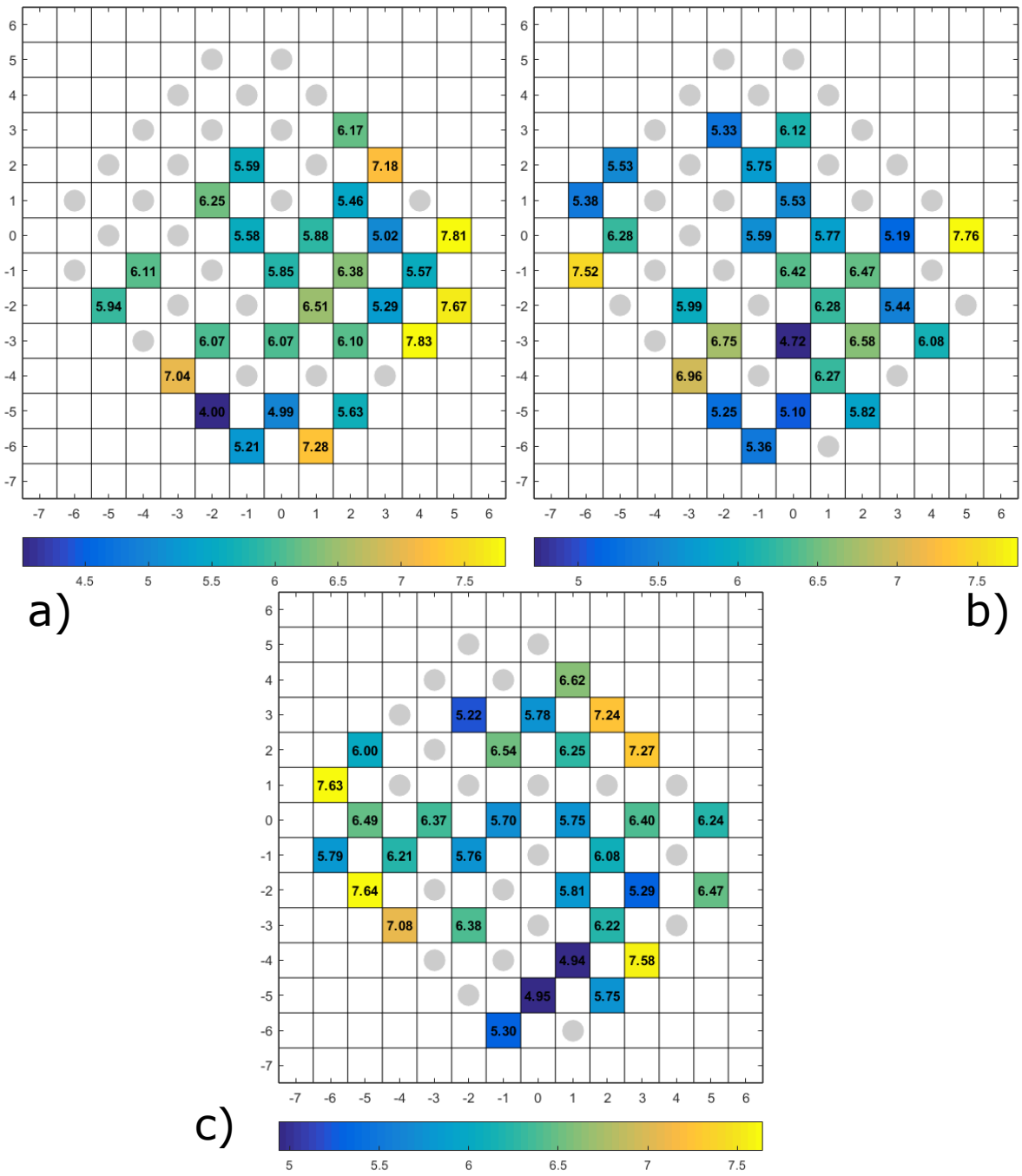
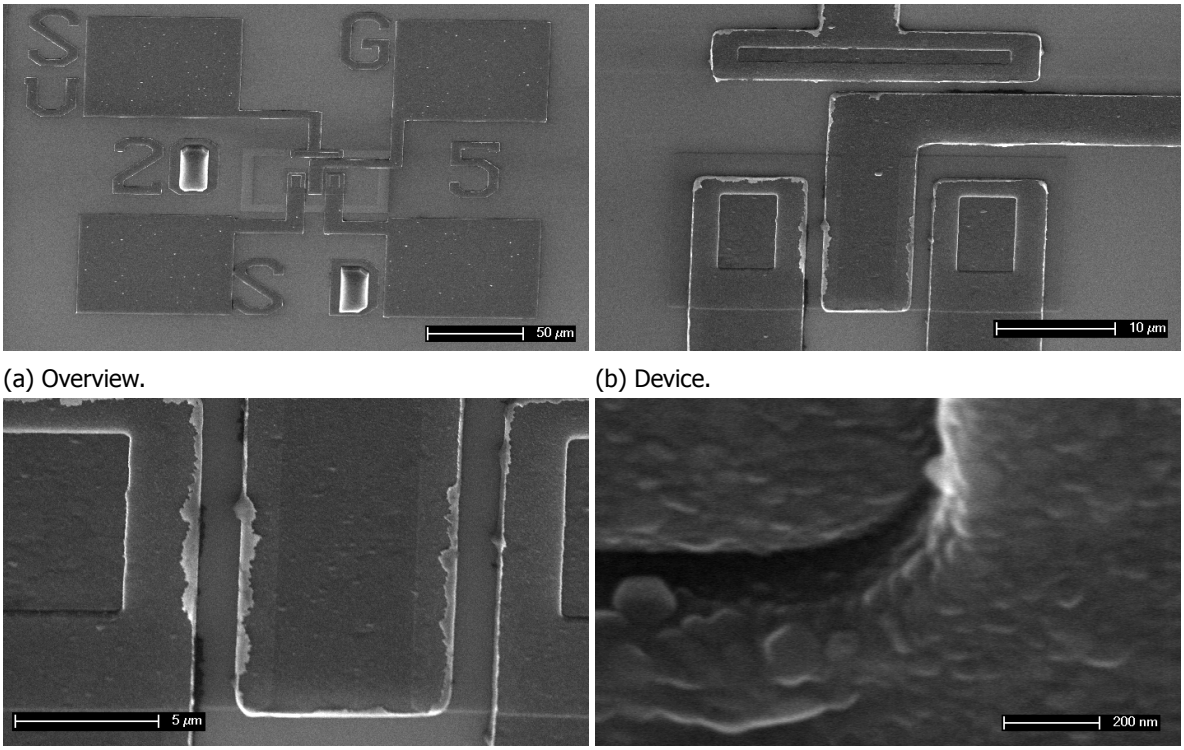


Figure C.8: Wafermaps depicting the sheet resistance $R_{\square}$ of graphene at 190 °C measured on three different aspect ratios during the training run. The strips have a length 206 μm and width 2 μm in (a), 5 μm in (b) and 10 μm in (c). Broken devices are marked with a grey circle. Measured on W4 in training run batch.

D

BICMOS Characterization



(a) Overview.

(b) Device.

(c) Gate.

(d) Contact opening.

Figure D.1: SEM images depicting the contact of an NMOS 20x5 device with the device overview in (a), device without the bondpads in (b), the gate area of the device in (c) and the metal layer on the corner of a contact opening in (d). Images taken at an angle of 45° on W4 in training run batch. Note that the original images were taken at a 180° rotation.

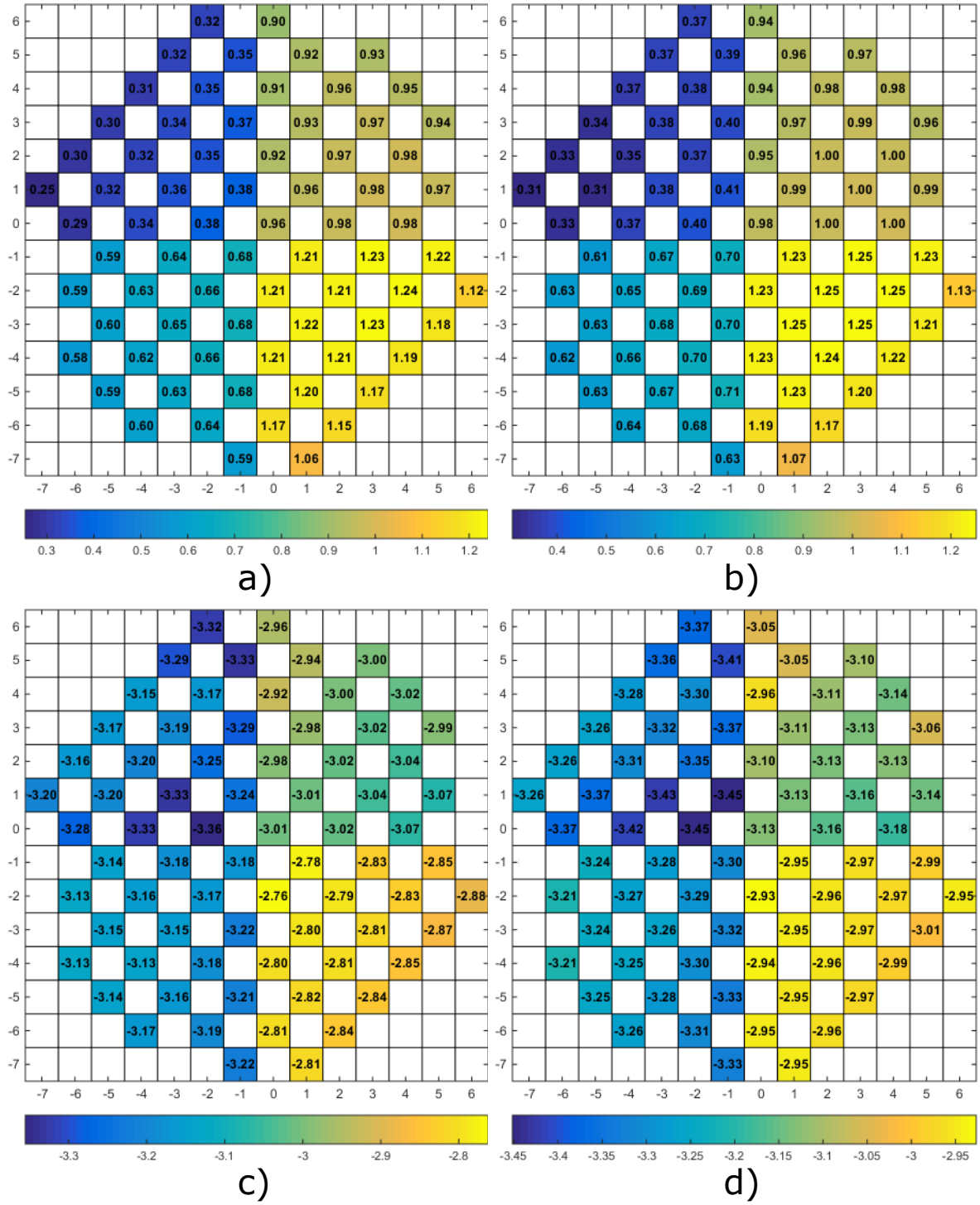


Figure D.2: Wafermaps depicting threshold voltage [V] of NMOS 20x2 in a) and 20x10 in b) and of PMOS 20x2 in c) and 20x10 in d). Broken devices are marked with a grey circle. Measured on W8 in training run batch.

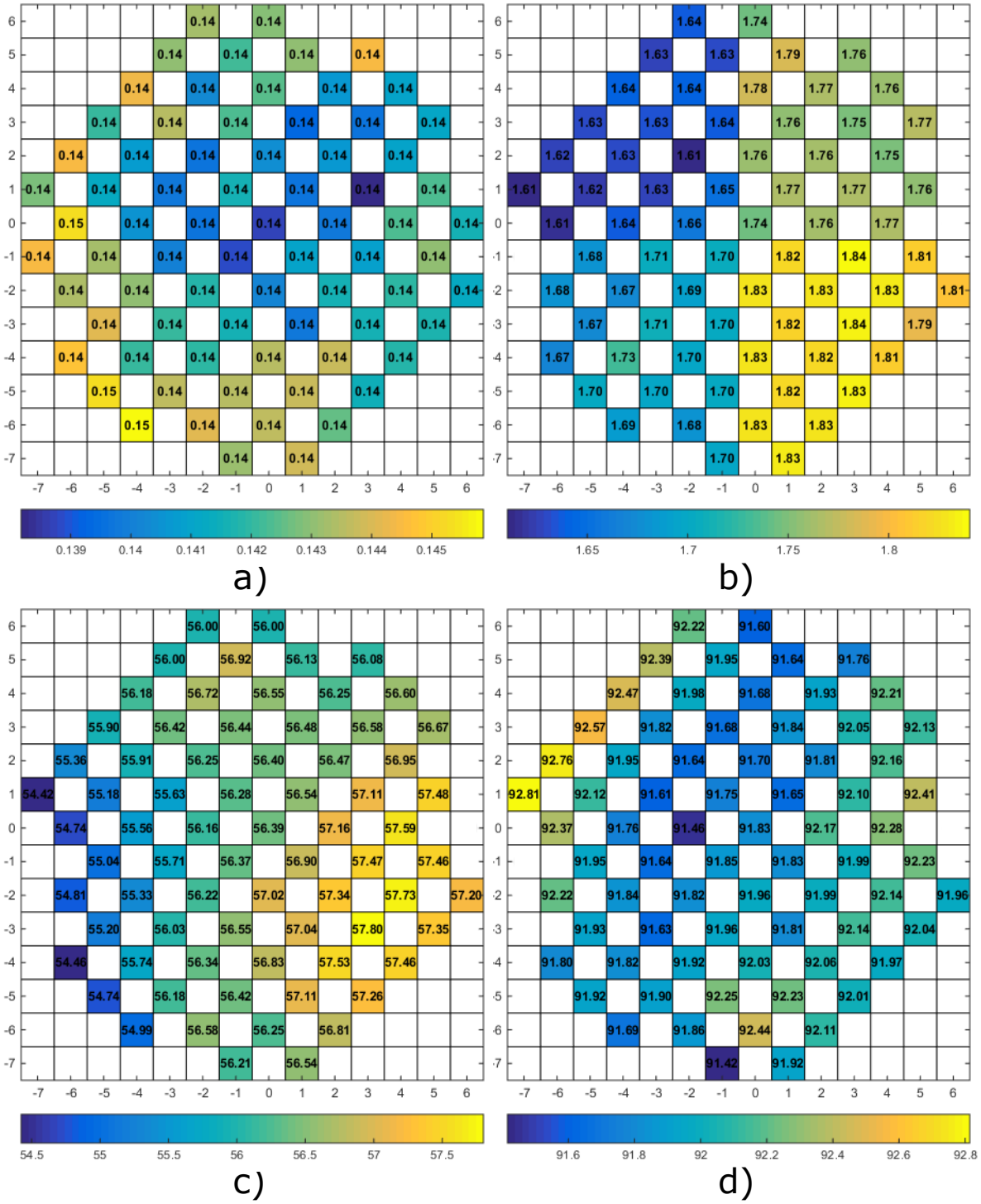


Figure D.3: Wafermaps depicting sheet resistance of IC [Ω] in a), NW [kΩ] in b), SN [Ω] in c) and SP [Ω] in d). Broken devices are marked with a grey circle. Measured on W8 in training run batch.

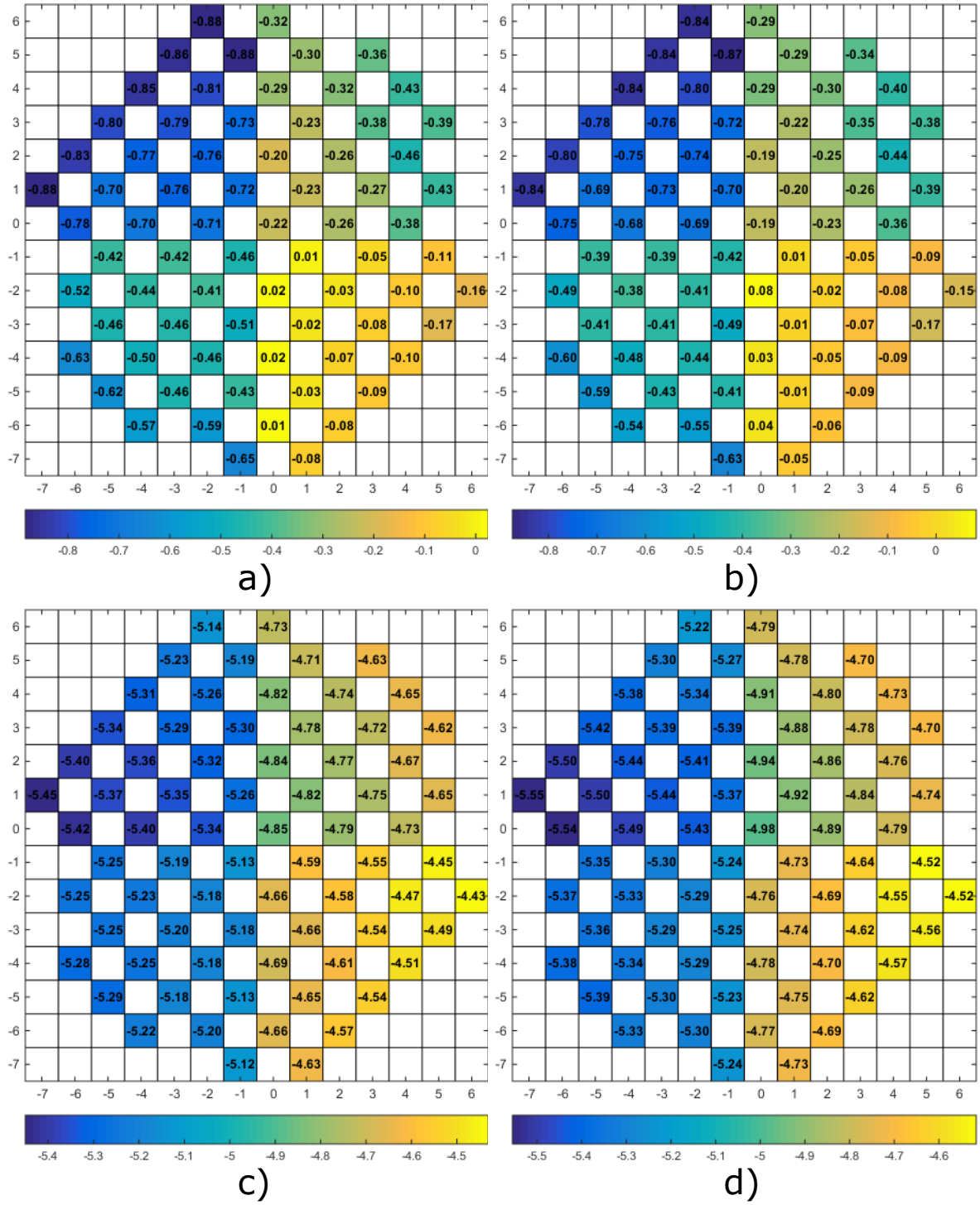


Figure D.4: Wafermaps depicting threshold voltage [V] of NMOS 20x2 in a) and 20x10 in b) and of PMOS 20x2 in c) and 20x10 in d). Broken devices are marked with a grey circle. Measured on W7 in training run batch.

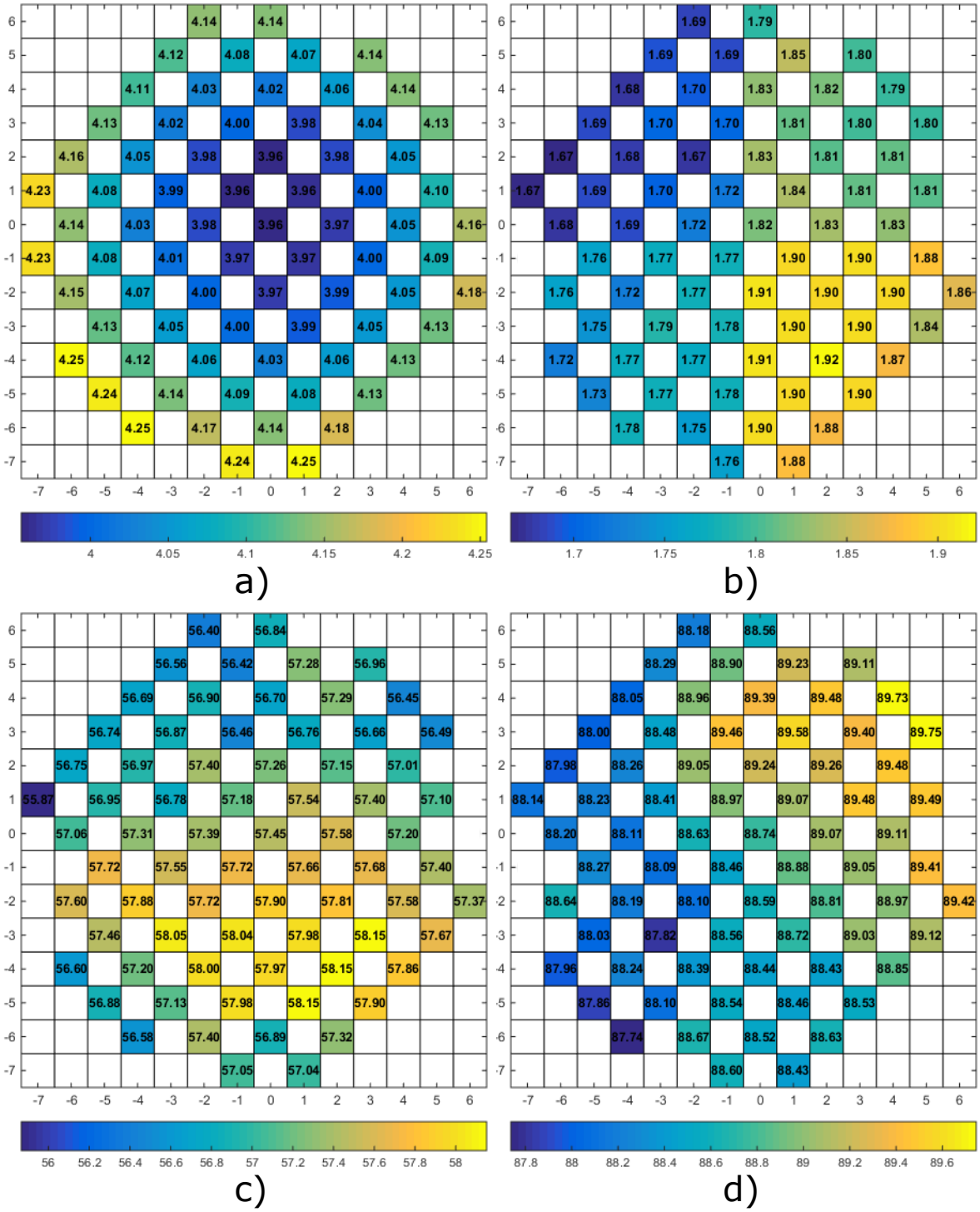


Figure D.5: Wafermaps depicting sheet resistance of IC [Ω] in a), NW [kΩ] in b), SN [Ω] in c) and SP [Ω] in d). Broken devices are marked with a grey circle. Measured on W7 in training run batch.

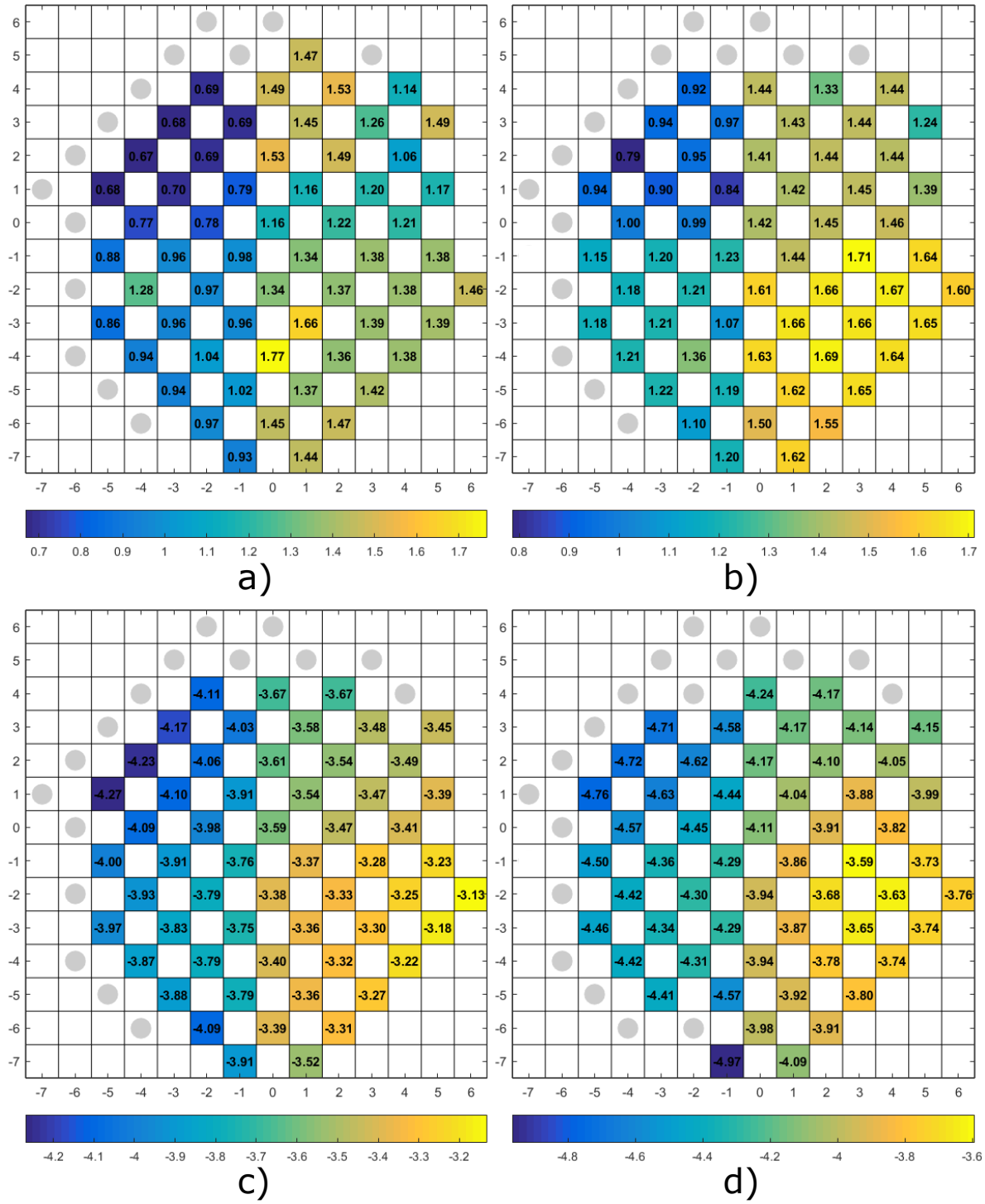


Figure D.6: Wafermaps depicting threshold voltage [V] of NMOS 20x2 in a) and 20x10 in b) and of PMOS 20x2 in c) and 20x10 in d). Broken devices are marked with a grey circle. Measured on W6 in training run batch.

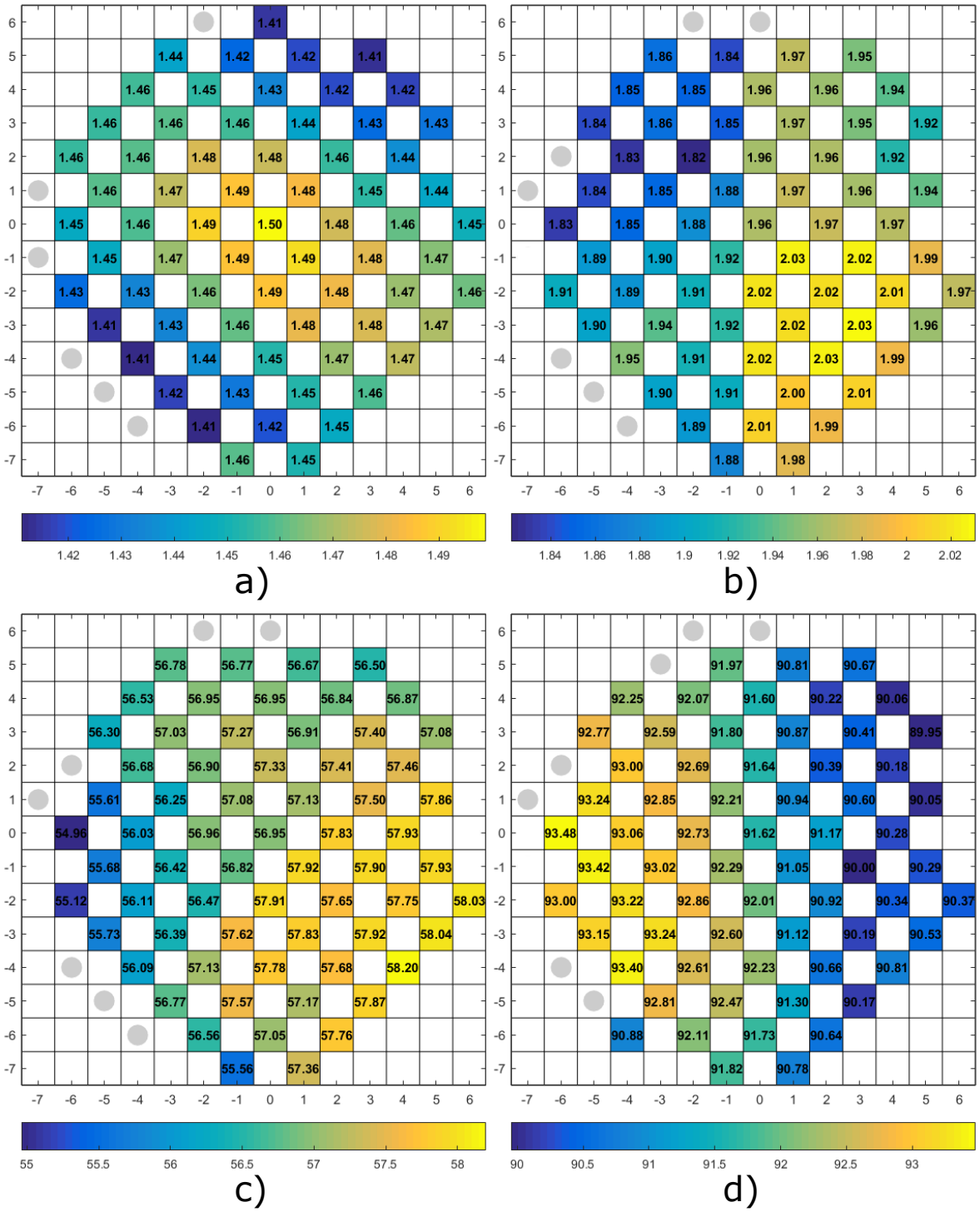


Figure D.7: Wafermaps depicting sheet resistance of IC [Ω] in a), NW [kΩ] in b), SN [Ω] in c) and SP [Ω] in d). Broken devices are marked with a grey circle. Measured on W6 in training run batch.

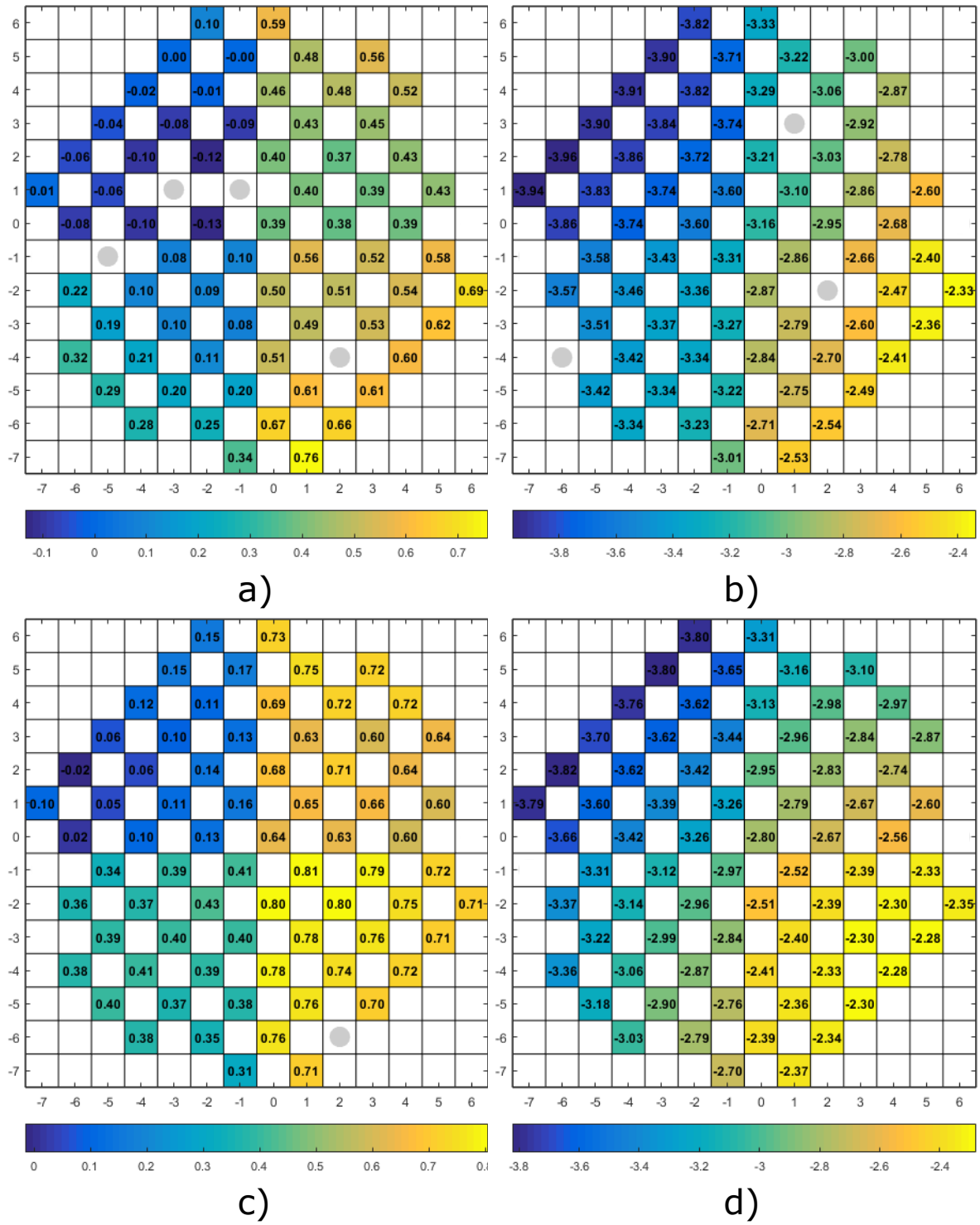


Figure D.8: Wafermaps depicting threshold voltage [V] of 20x5 devices on wafer 3 with the V_{Tn} of NMOS devices in a) and the the V_{Tp} of PMOS devices in b). Wafermaps depicting threshold voltage [V] of 20x5 devices on wafer 2 with the V_{Tn} of NMOS devices in c) and the the V_{Tp} of PMOS devices in d). Broken devices are marked with a grey circle.

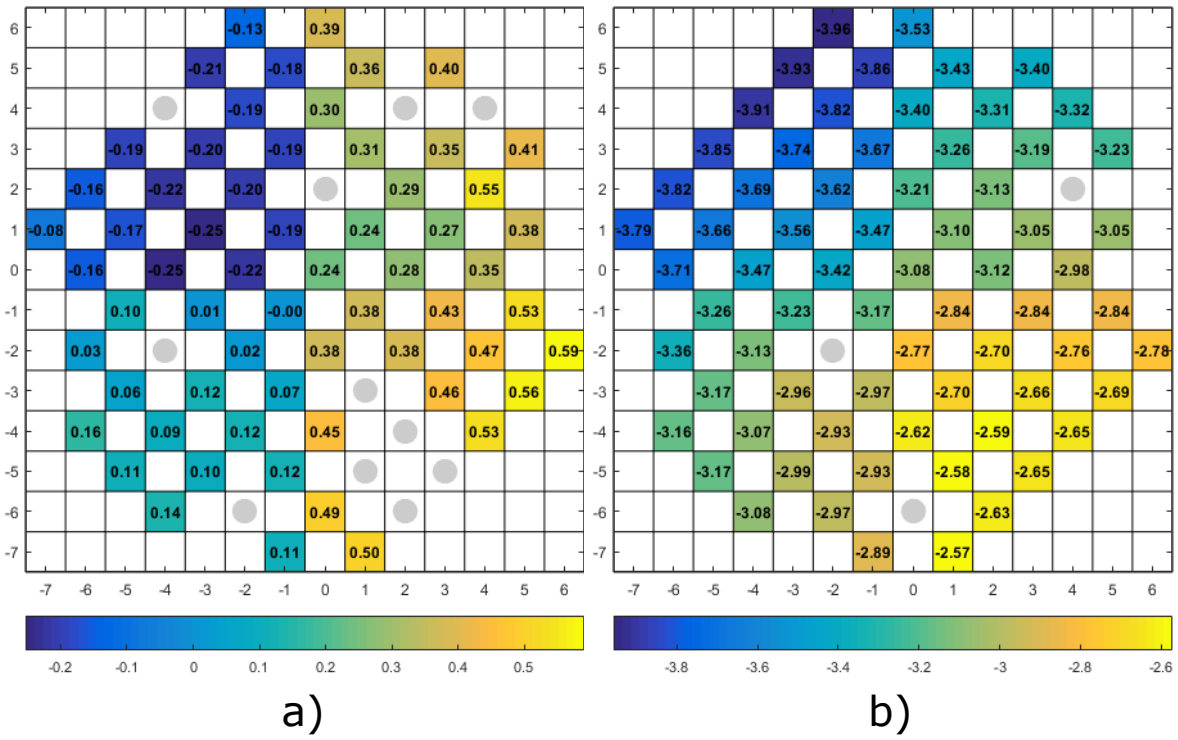


Figure D.9: Wafermaps depicting threshold voltage [V] of 20x5 devices on wafer 1 with the V_{Tn} of NMOS devices in a) and the the V_{Tp} of PMOS devices in b). Broken devices are marked with a grey circle.

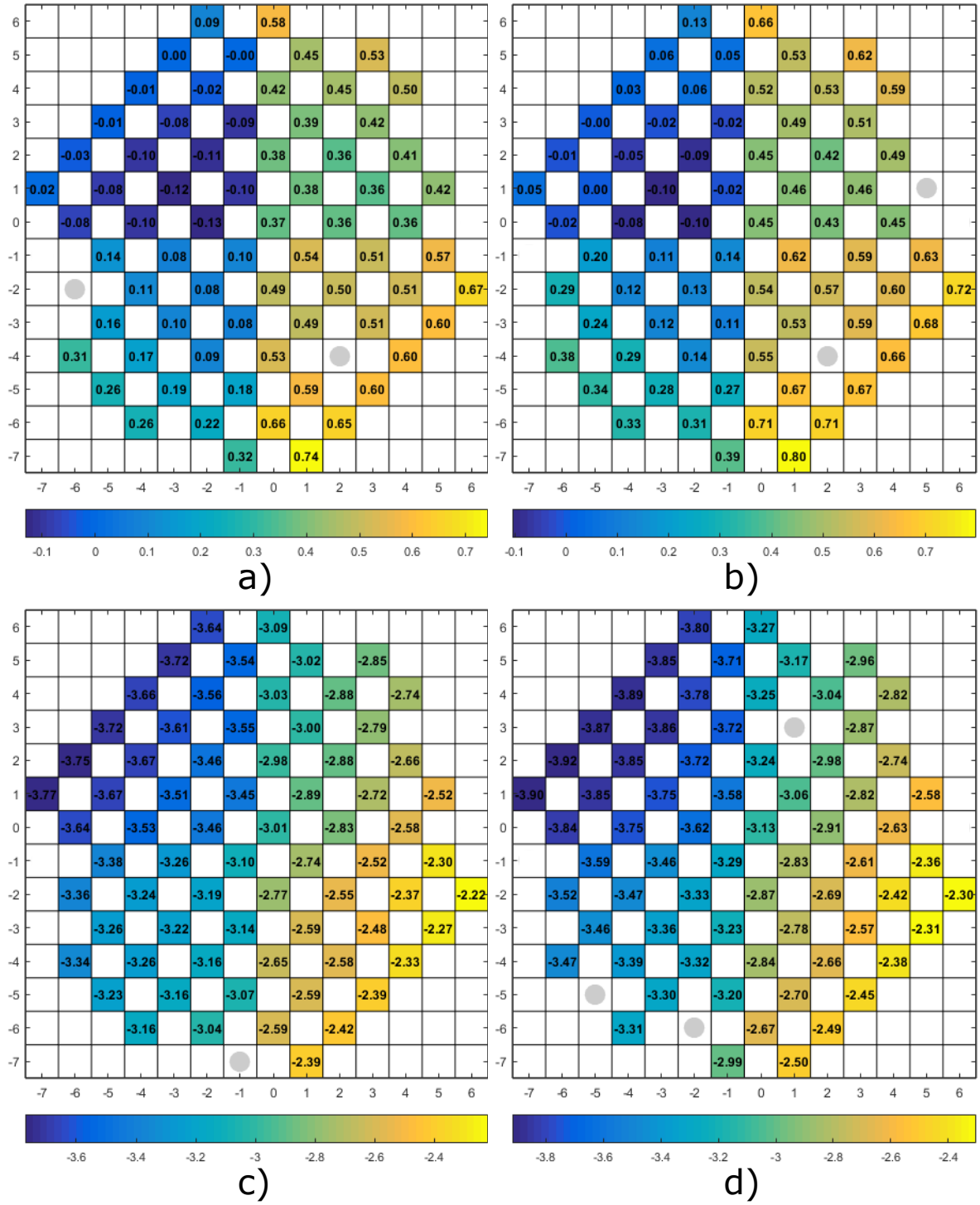


Figure D.10: Wafermaps depicting threshold voltage [V] of NMOS 20x2 in a) and 20x10 in b) and of PMOS 20x2 in c) and 20x10 in d). Broken devices are marked with a grey circle. Measured on W3 in training run batch.

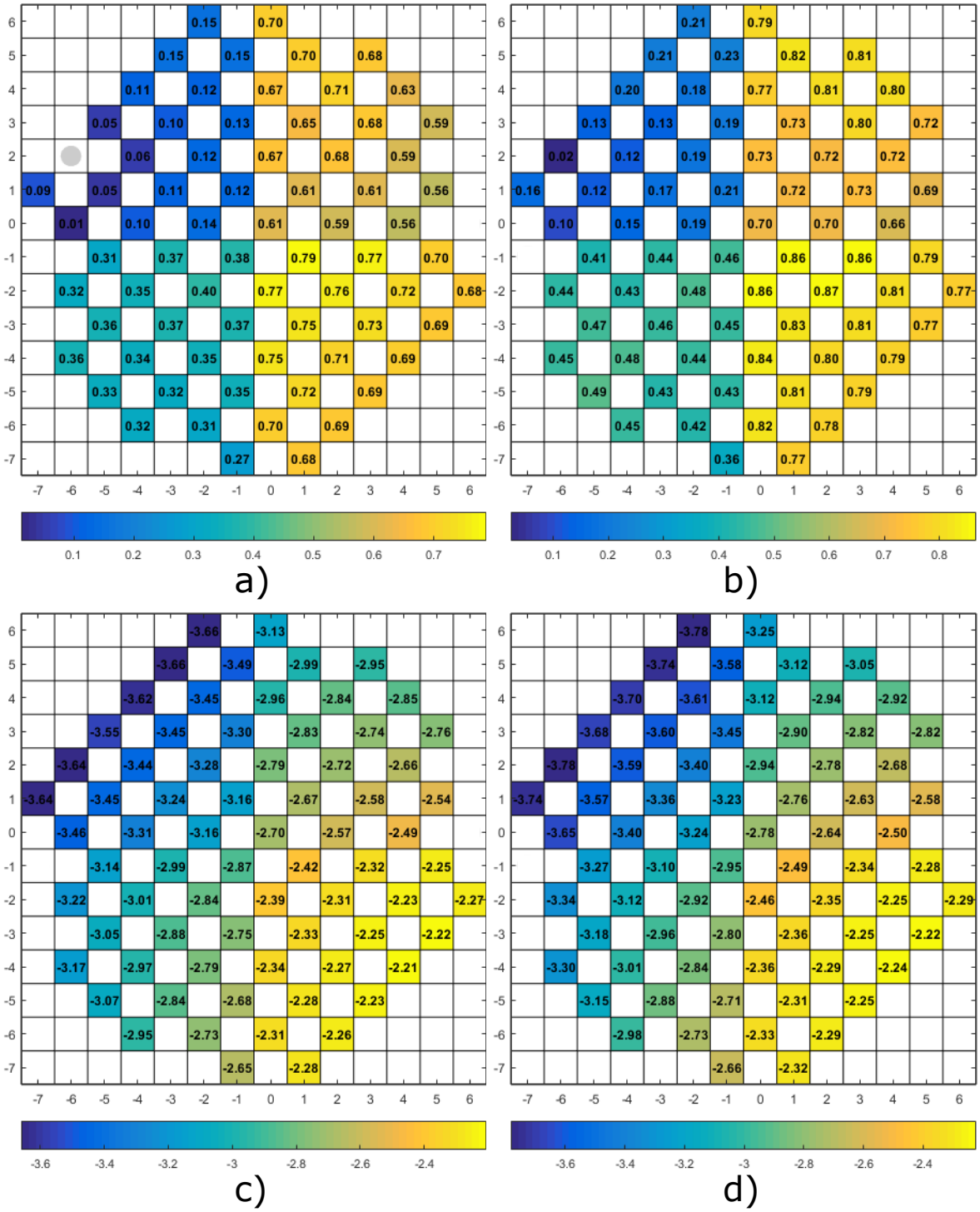


Figure D.11: Wafermaps depicting threshold voltage [V] of NMOS 20x2 in a) and 20x10 in b) and of PMOS 20x2 in c) and 20x10 in d). Broken devices are marked with a grey circle. Measured on W2 in training run batch.

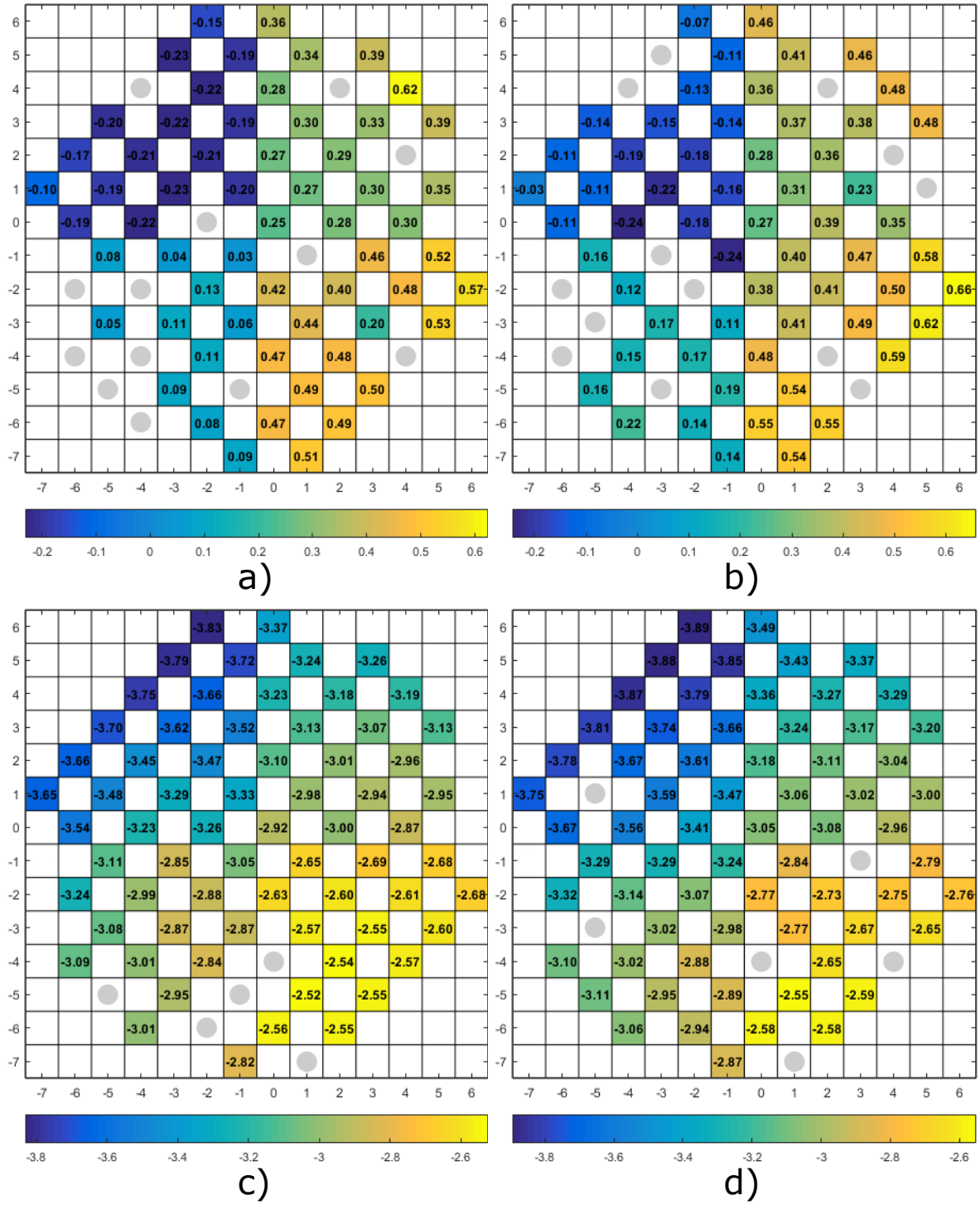


Figure D.12: Wafermaps depicting threshold voltage [V] of NMOS 20x2 in a) and 20x10 in b) and of PMOS 20x2 in c) and 20x10 in d). Broken devices are marked with a grey circle. Measured on W1 in training run batch.

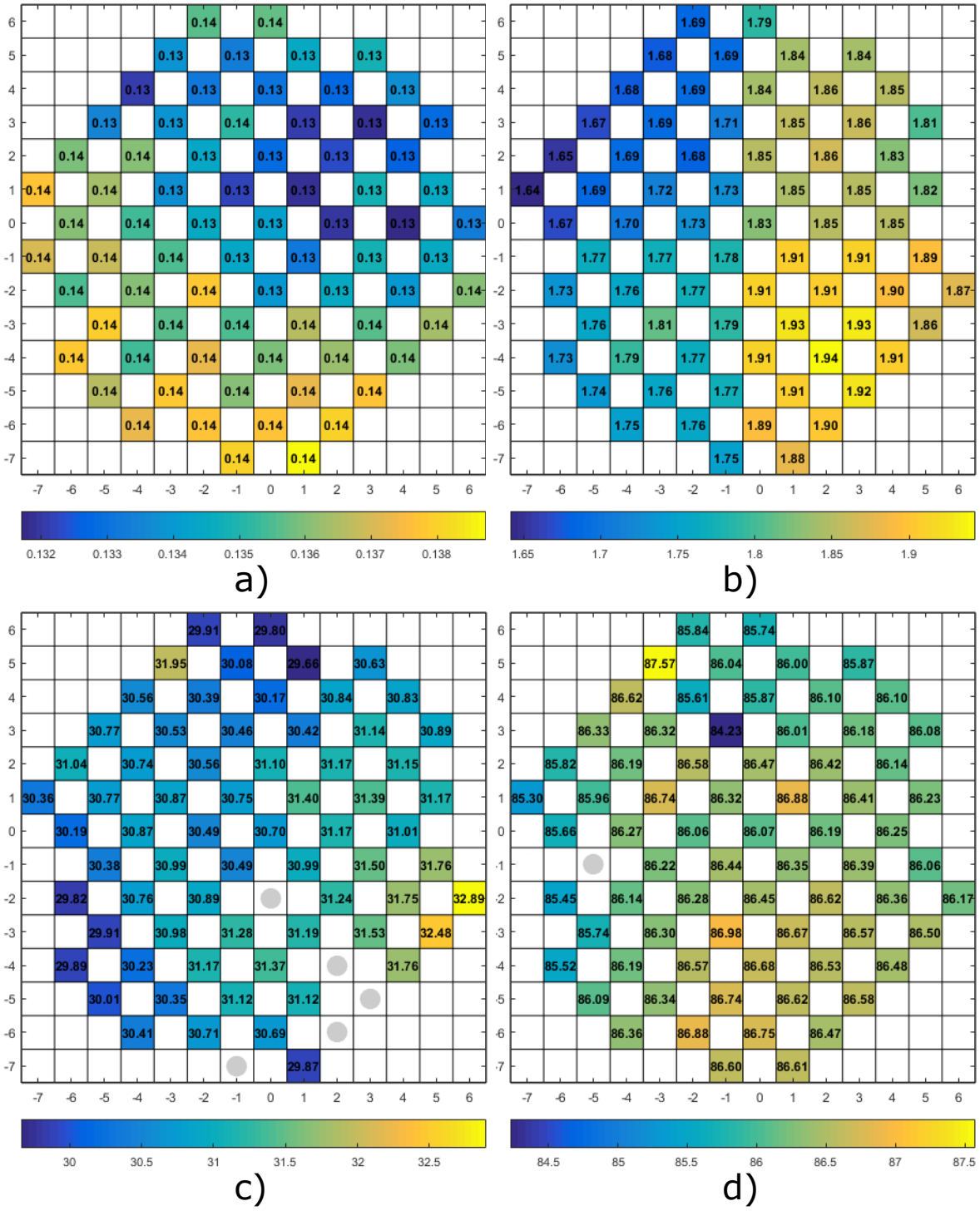


Figure D.13: Wafermaps depicting sheet resistance of IC [Ω] in a), NW [kΩ] in b), SN [Ω] in c) and SP [Ω] in d). Broken devices are marked with a grey circle. Measured on W3 in training run batch.

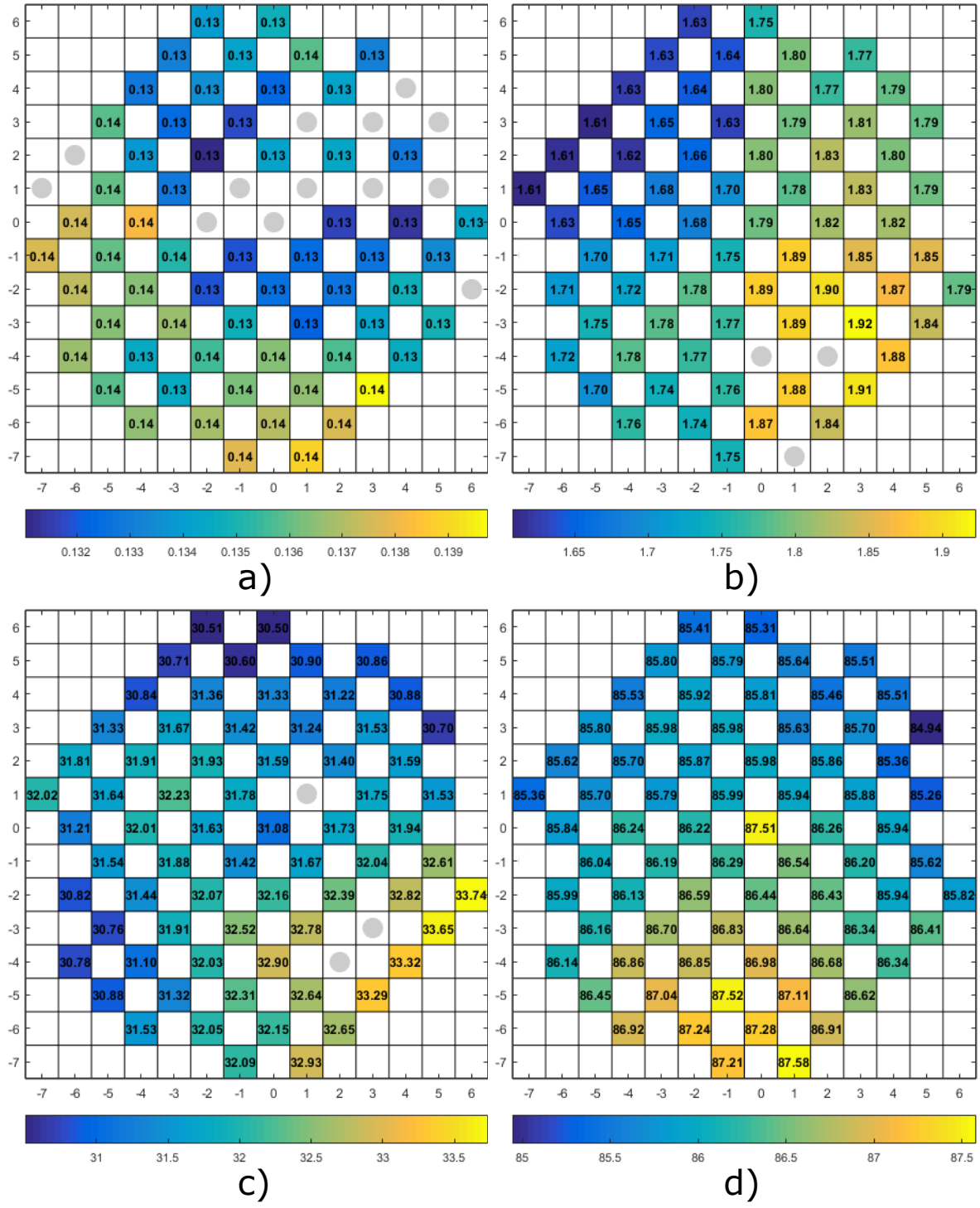


Figure D.14: Wafermaps depicting sheet resistance of IC [Ω] in a), NW [kΩ] in b), SN [Ω] in c) and SP [Ω] in d). Broken devices are marked with a grey circle. Measured on W2 in training run batch.

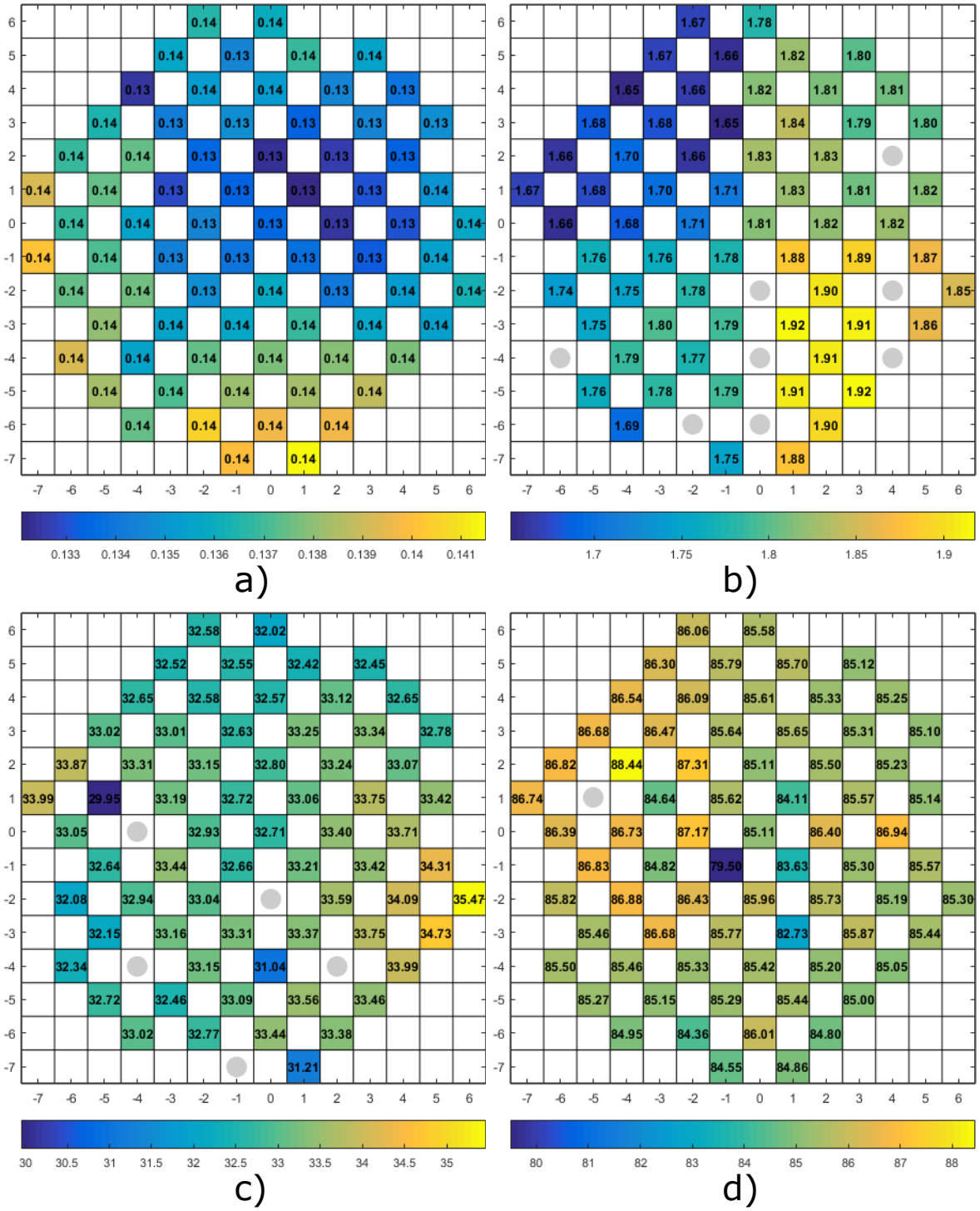


Figure D.15: Wafermaps depicting sheet resistance of IC [Ω] in a), NW [kΩ] in b), SN [Ω] in c) and SP [Ω] in d). Broken devices are marked with a grey circle. Measured on W1 in training run batch.

E

Read-Out Electronics and Complete Layout Design

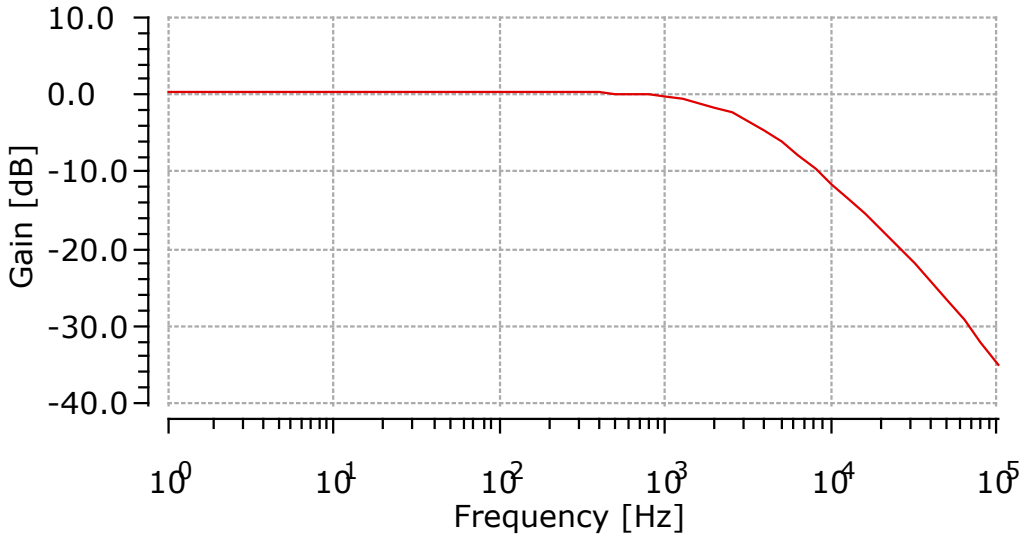


Figure E.1: AC analysis of the open-loop unity voltage gain of the SF with the gain results in dB.

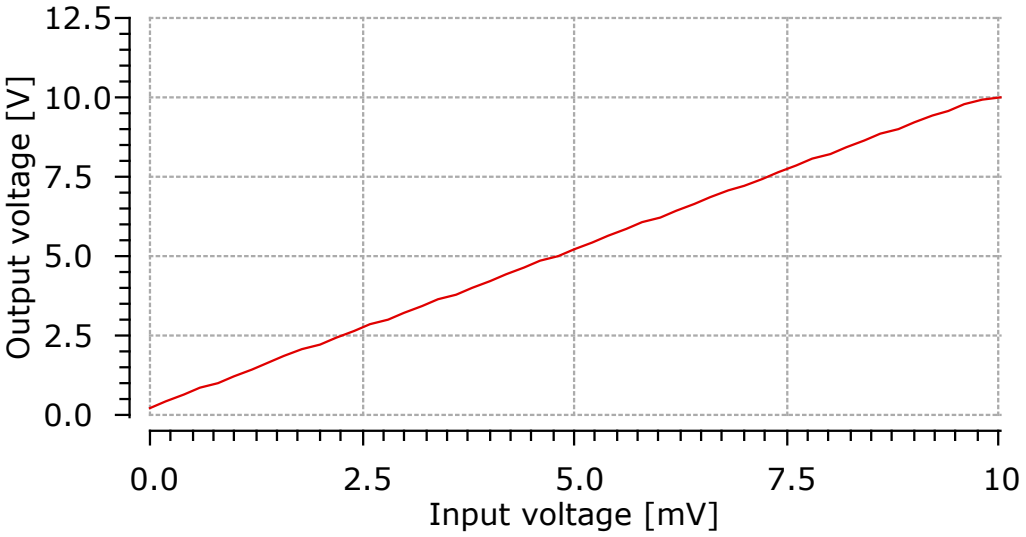


Figure E.2: DC analysis of the open-loop voltage gain of the SF from which the offset and linearity are derived.

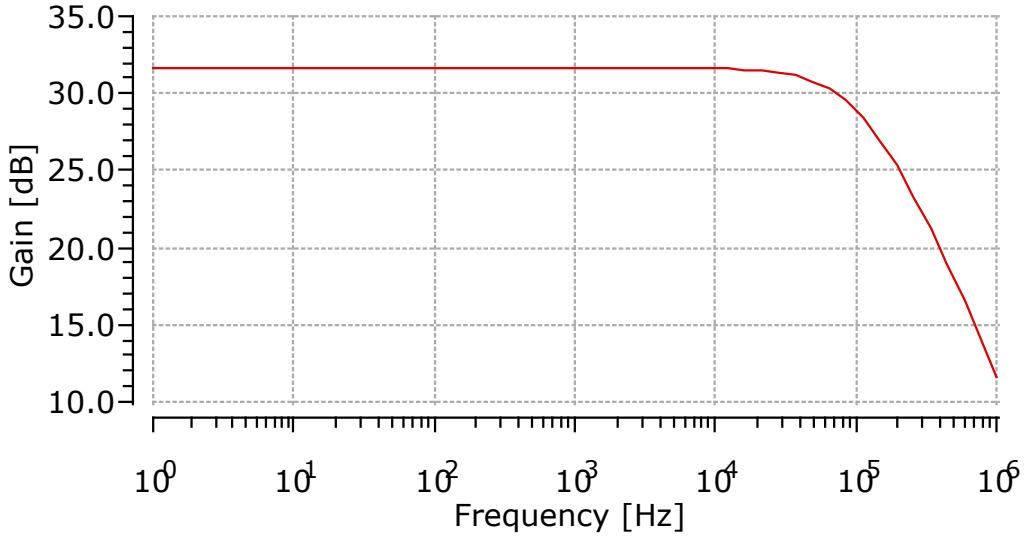


Figure E.3: AC analysis of the open-loop voltage gain of the FCO and SF combination with the gain results in dB.

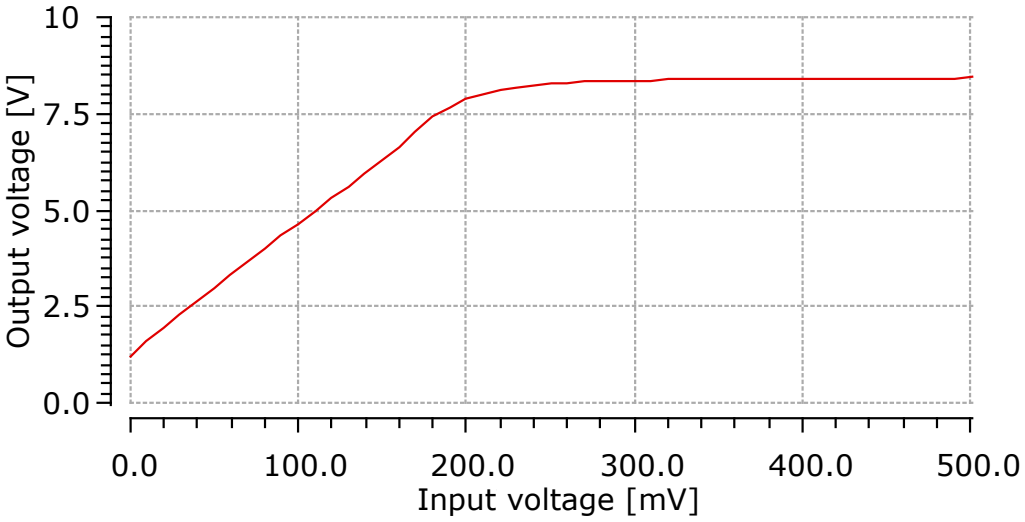


Figure E.4: DC analysis of the open-loop voltage gain of the FCO and SF combination from which the offset and linearity are derived.

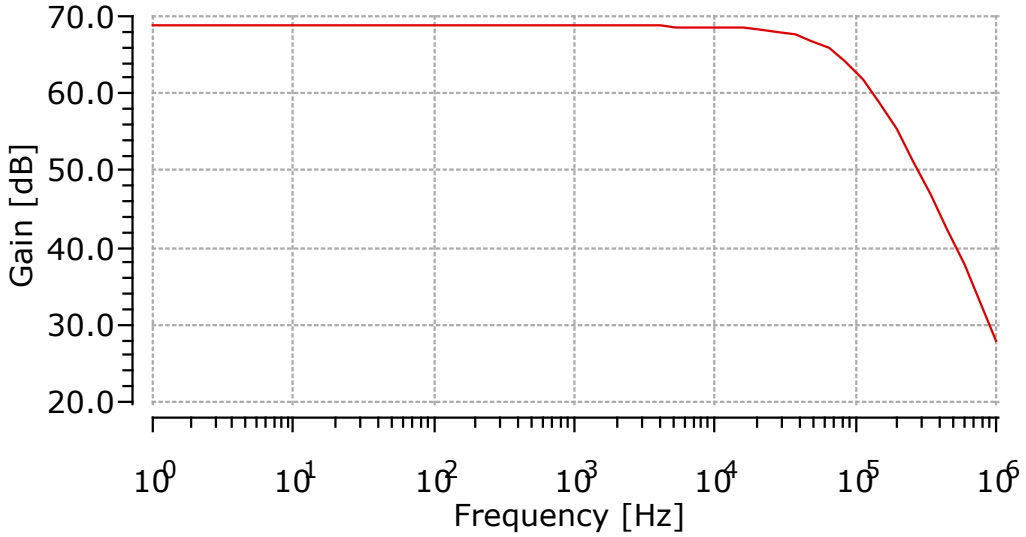


Figure E.5: AC analysis of the open-loop voltage gain of the cascaded FCO and SF combination with the gain results in dB.

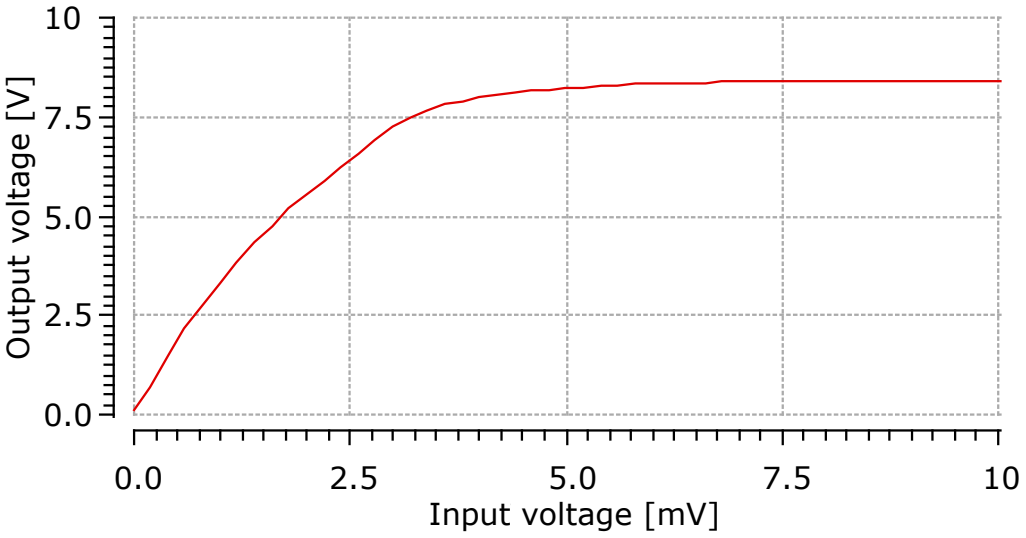


Figure E.6: DC analysis of the open-loop voltage gain of the cascaded FCO and SF combination from which the offset and linearity are derived.

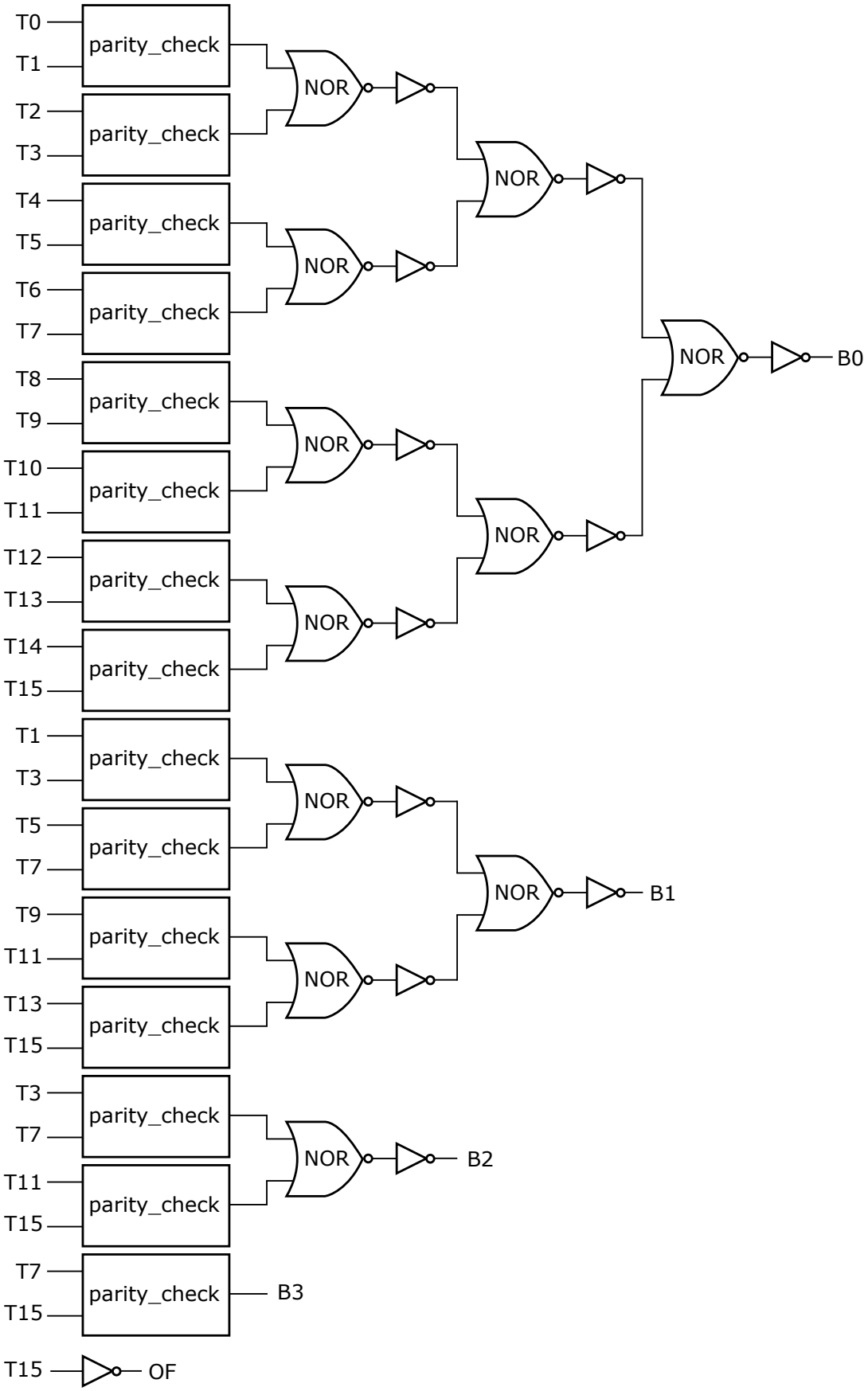


Figure E.7: The complete thermometer encoder logic circuit.

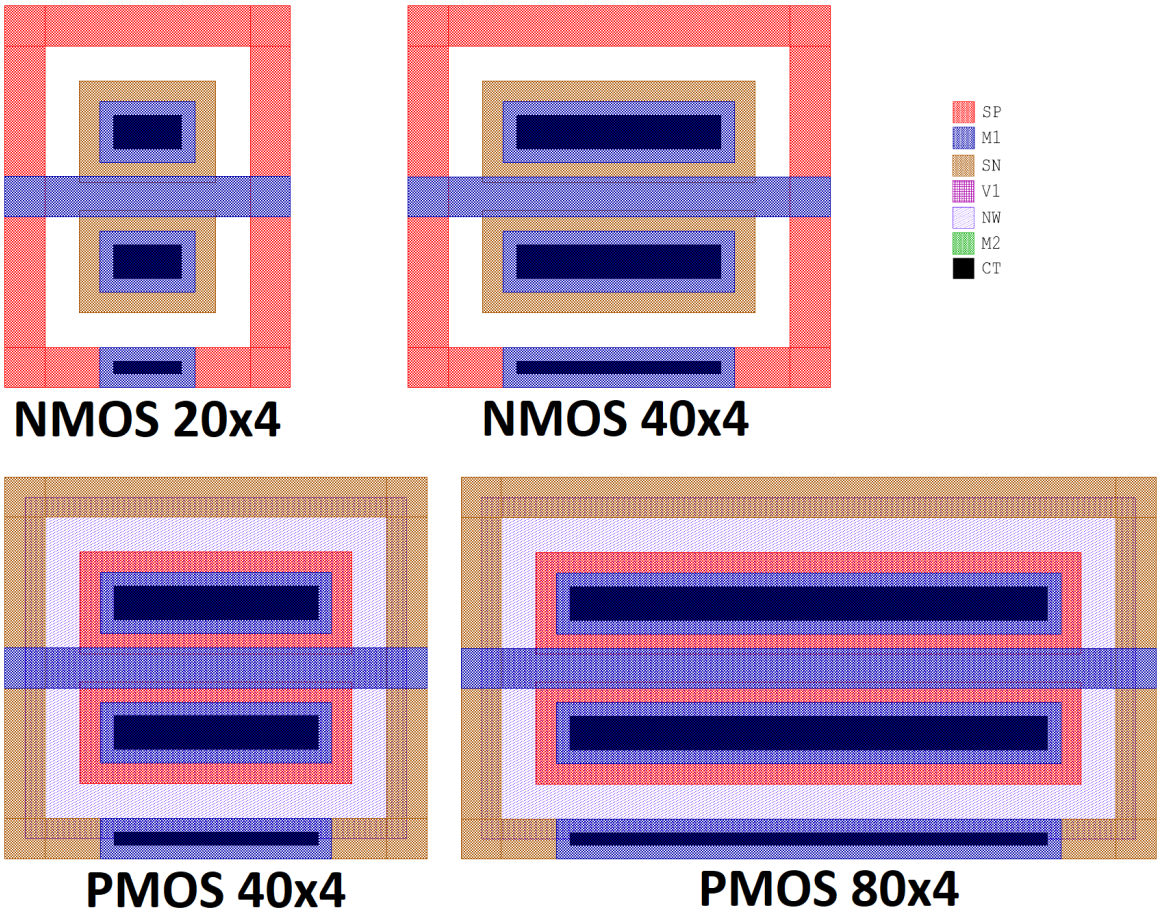


Figure E.8: Layout designs of NMOS and PMOS devices used in digital logic with the 7 stacked layers. The legend includes indicates the different layers. Note that M2 and V1 are not required in the layout.

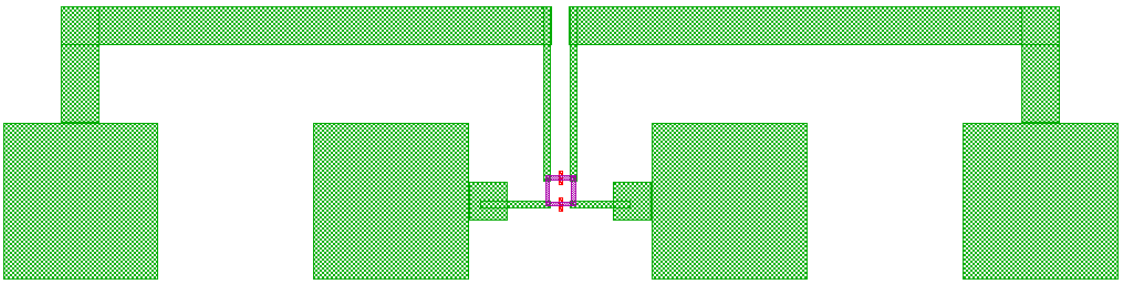


Figure E.9: Layout design of graphene-based Pirani pressure sensors in a Wheatstone half bridge. Purple represents the graphene strip, red the patterned cavity and green the second metal layer.

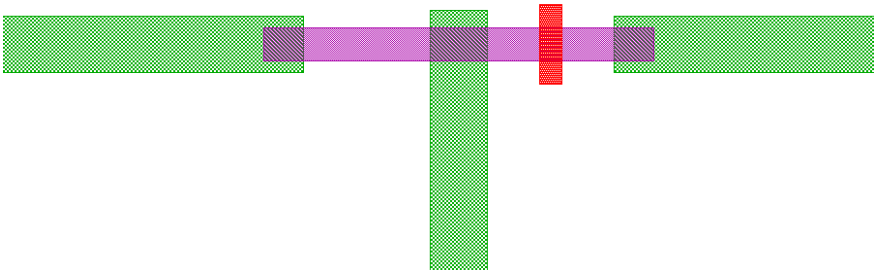


Figure E.10: Layout of a single leg of the Wheatstone bridge to be used if resistor matching problems occur. Purple represents the graphene strip, red the patterned cavity and green the second metal layer.

F

Fabrication Results

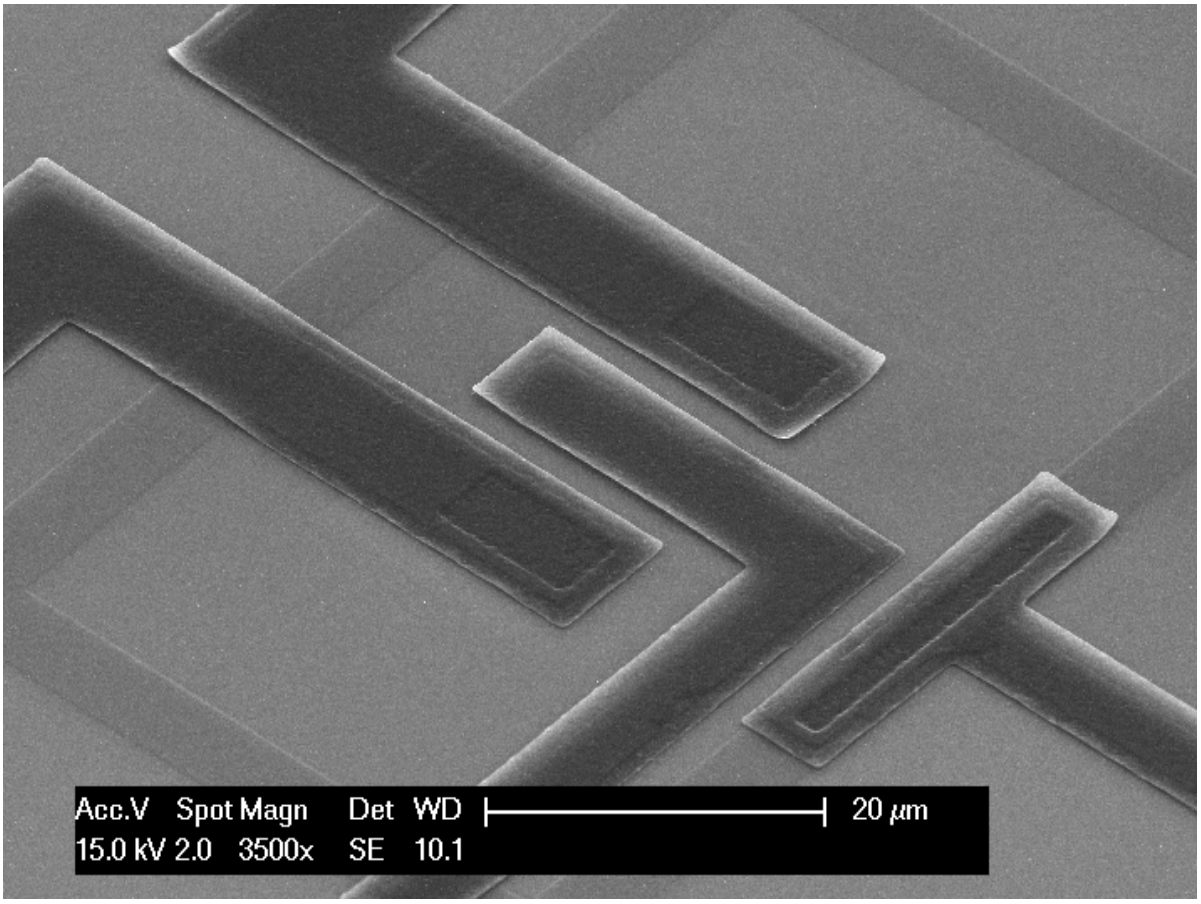


Figure F.1: SEM image of an NMOS device depicting stress issues in the M1 layer implemented on W1 by depositing 150 nm of AlSi with 50 nm of TiN on top.

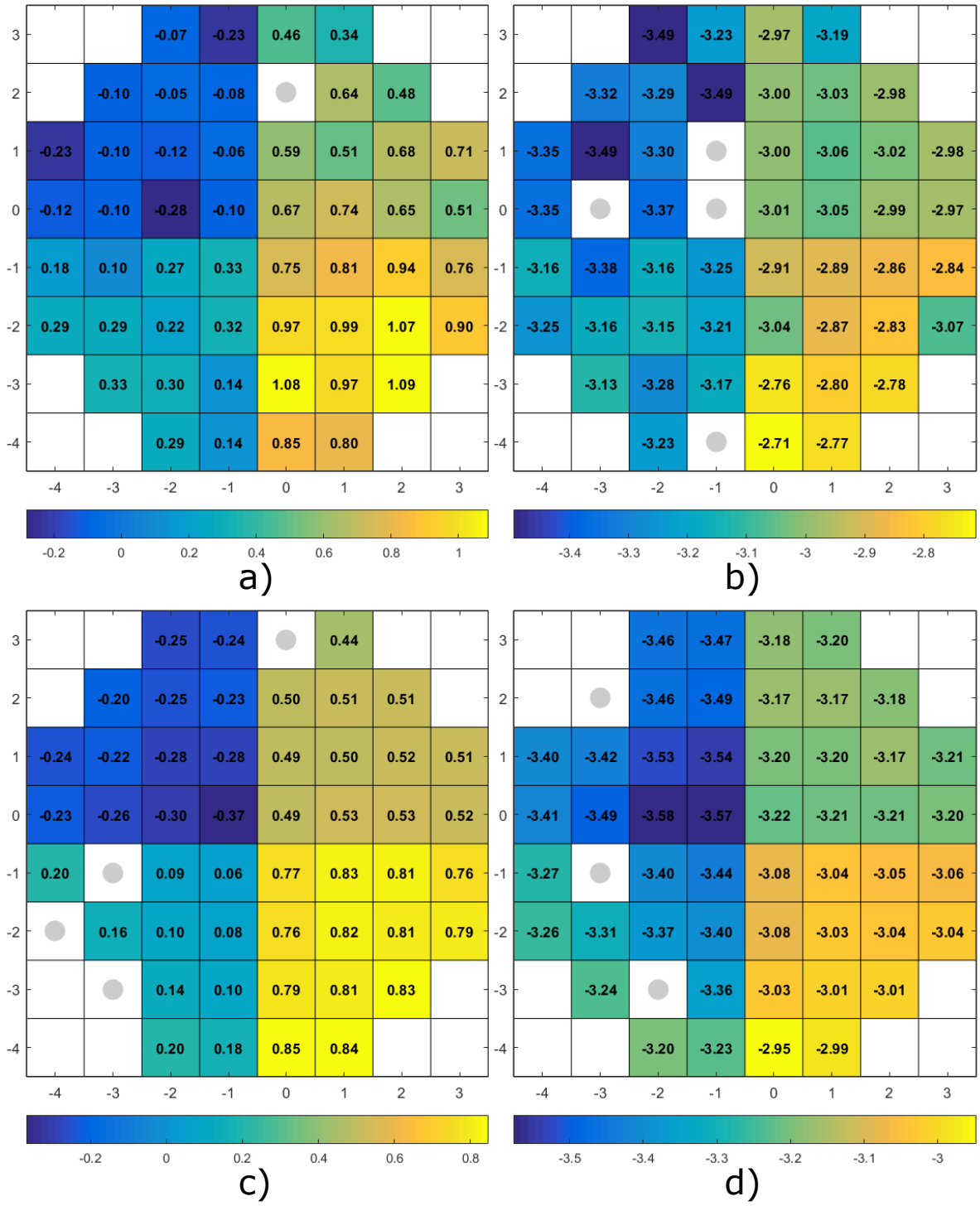


Figure F.2: Wafermaps depicting threshold voltage [V] of NMOS 20x5 in a), PMOS 20x5 in b), NMOS 400x4 in c) and PMOS 400x4 in d) after M2 implementation. Broken devices are marked with a grey circle. Measured on W1 in fabrication run batch.

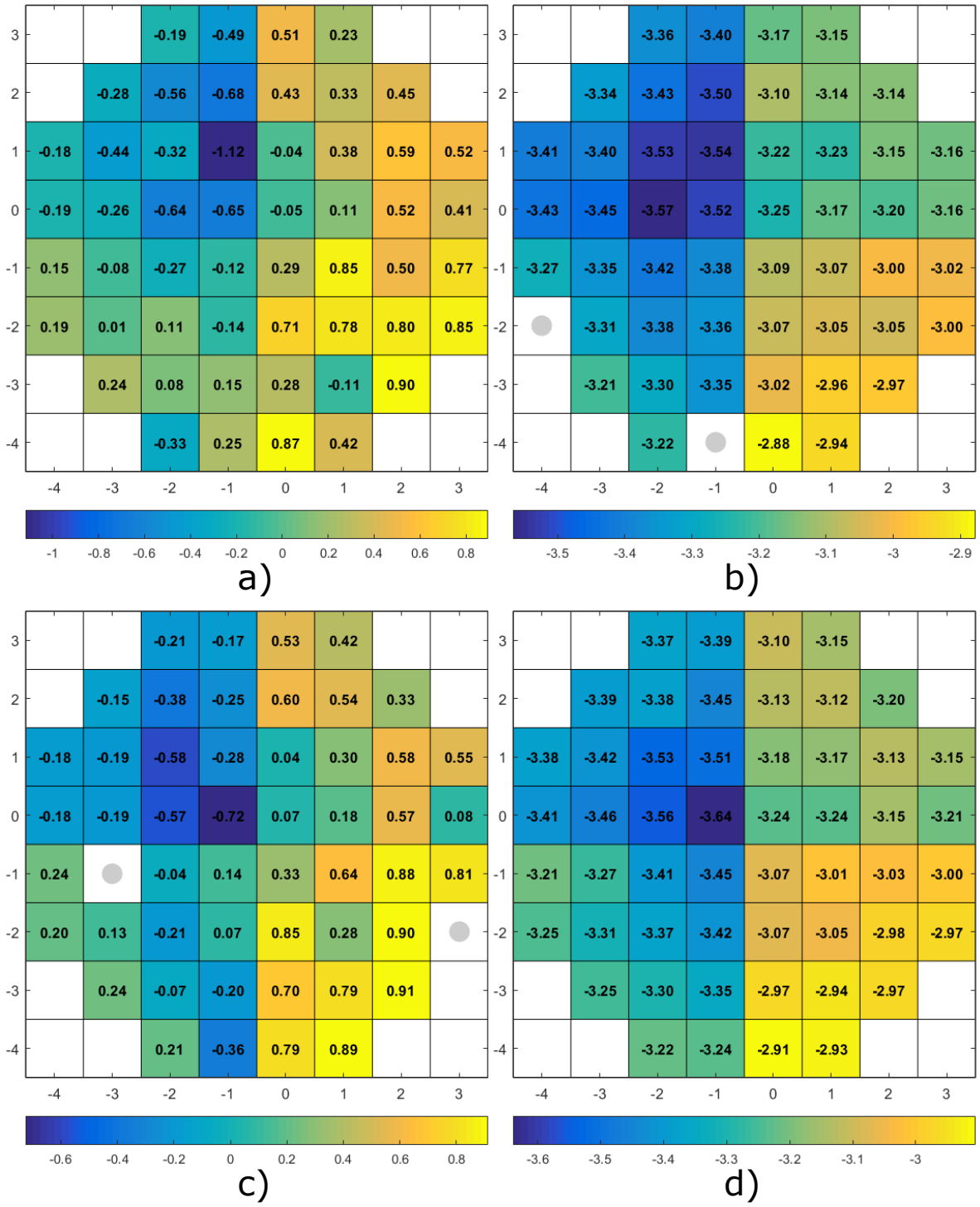


Figure F.3: Wafermaps depicting threshold voltage [V] of NMOS 20x4 in a), PMOS 40x5 in b), NMOS 40x4 in c) and PMOS 80x4 in d) after M2 implementation. Broken devices are marked with a grey circle. Measured on W1 in fabrication run batch.

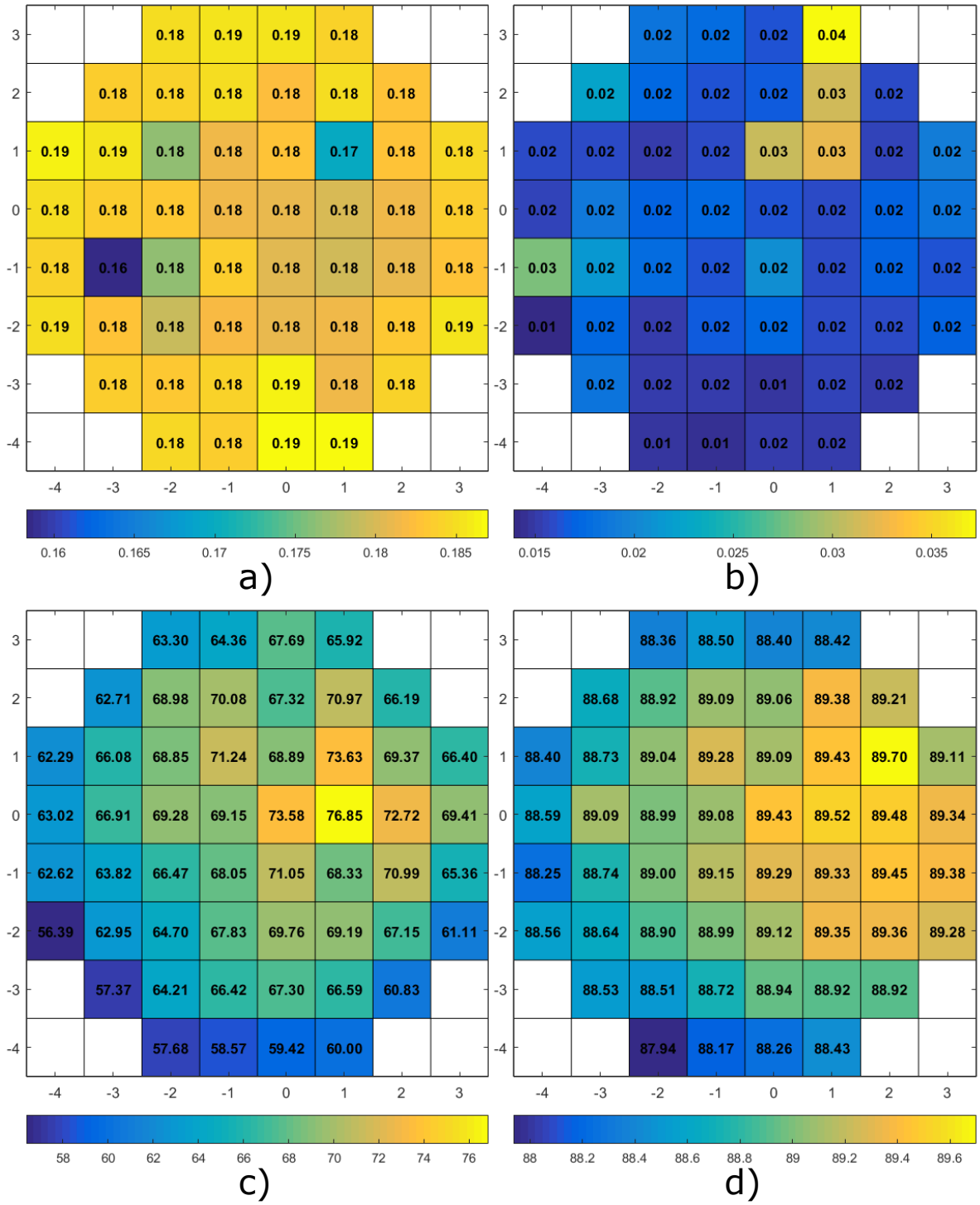


Figure F.4: Wafermaps depicting sheet resistance of M1 [Ω] in a), M2 [Ω] in b), SN [Ω] in c) and SP [Ω] in d). Broken devices are marked with a grey circle. Measured on W1 in fabrication run batch.

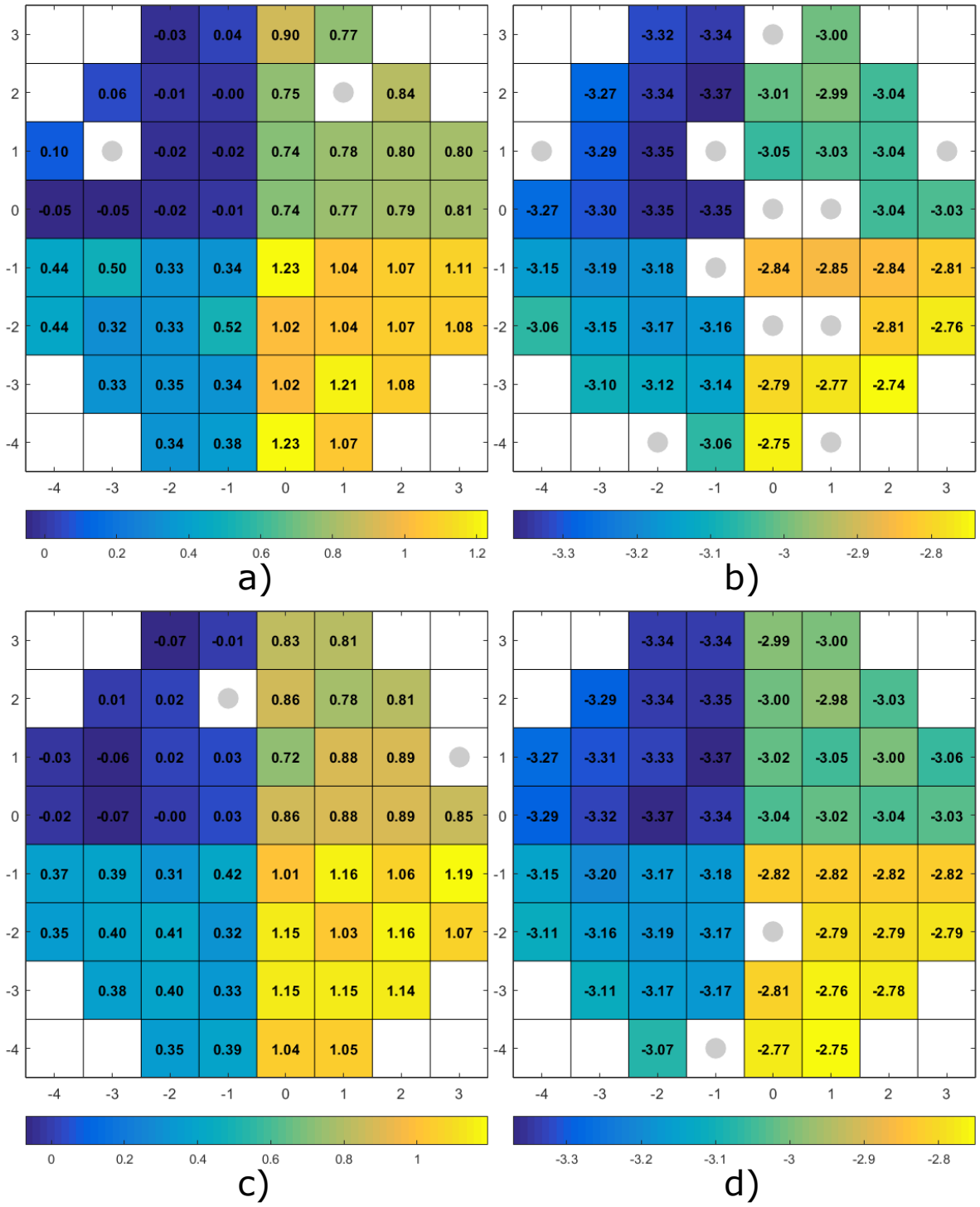


Figure F.5: Wafermaps depicting threshold voltage [V] of NMOS 20x5 in a), PMOS 20x5 in b), NMOS 400x4 in c) and PMOS 400x4 in d) after M2 implementation. Broken devices are marked with a grey circle. Measured on W3 in fabrication run batch.

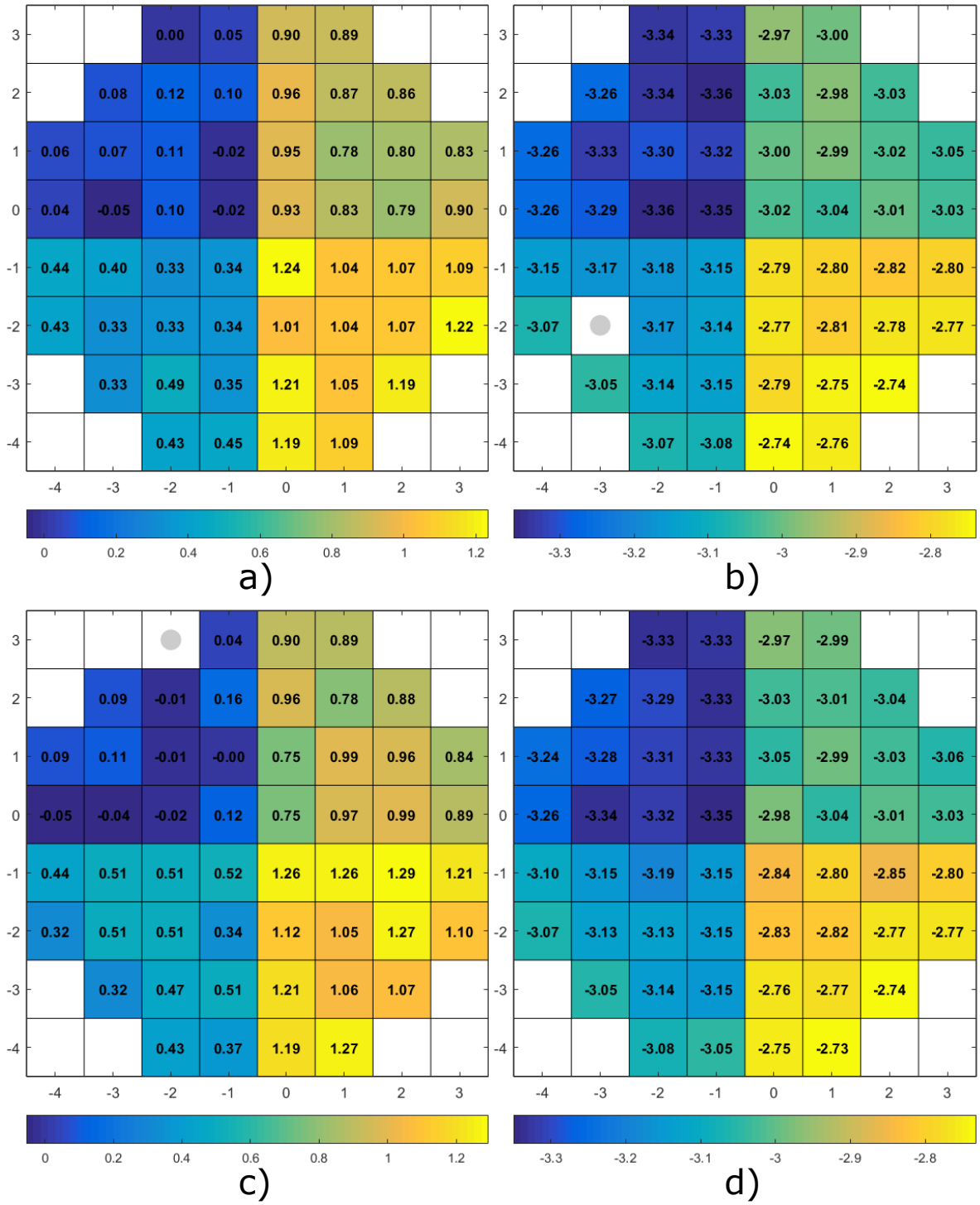


Figure F.6: Wafermaps depicting threshold voltage [V] of NMOS 20x4 in a), PMOS 40x5 in b), NMOS 40x4 in c) and PMOS 80x4 in d) after M2 implementation. Broken devices are marked with a grey circle. Measured on W3 in fabrication run batch.

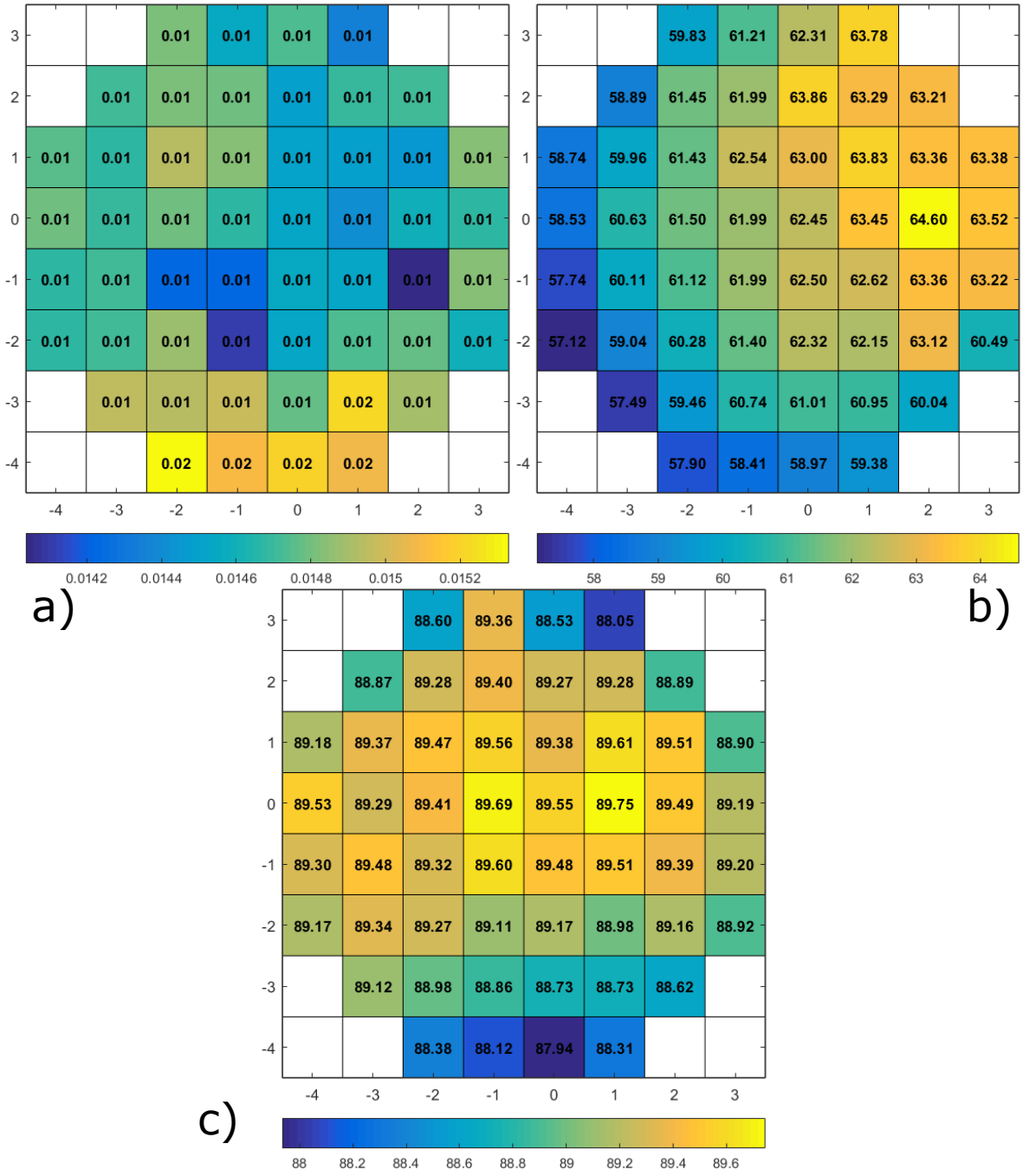


Figure F.7: Wafermaps depicting sheet resistance of M2 [Ω] in a), SN [Ω] in b) and SP [Ω] in c). Broken devices are marked with a grey circle. Measured on W1 in fabrication run batch.

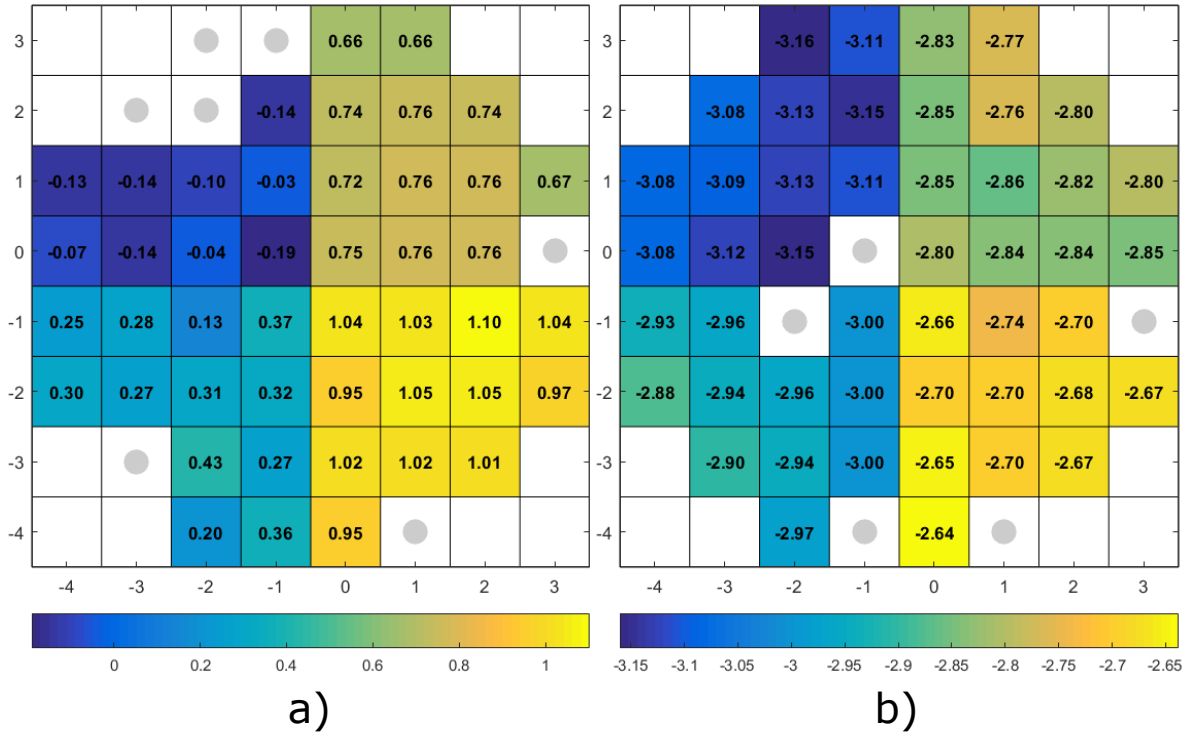


Figure F.8: Wafermaps depicting threshold voltage [V] of NMOS 20x5 in a) and PMOS 20x5 in b) after M1 implementation. Broken devices are marked with a grey circle. Measured on W7 in fabrication run batch.

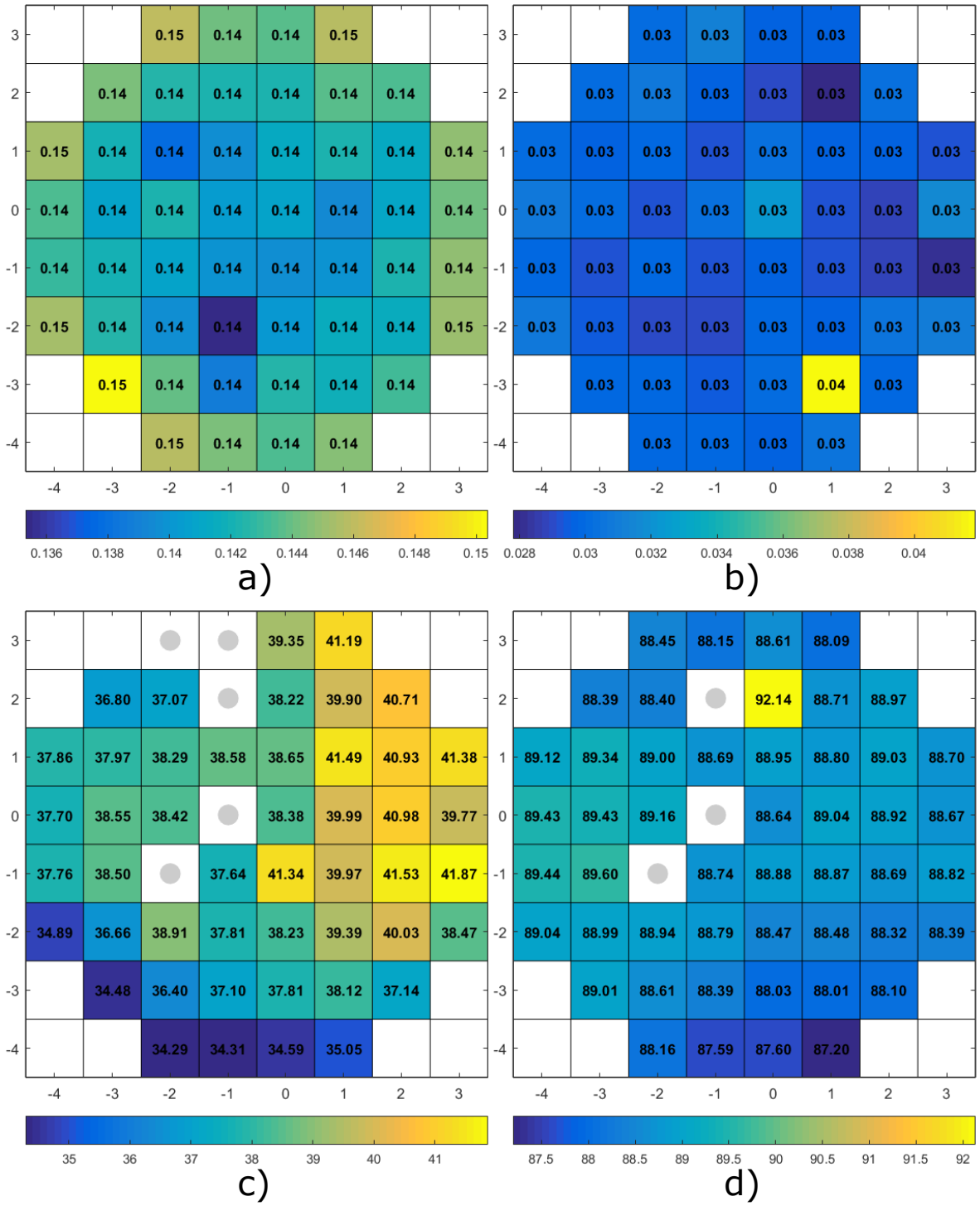


Figure F.9: Wafermaps depicting sheet resistance of M1 [Ω] in a), M2 [Ω] in b), SN [Ω] in c) and SP [Ω] in d). Broken devices are marked with a grey circle. Measured on W7 in fabrication run batch.

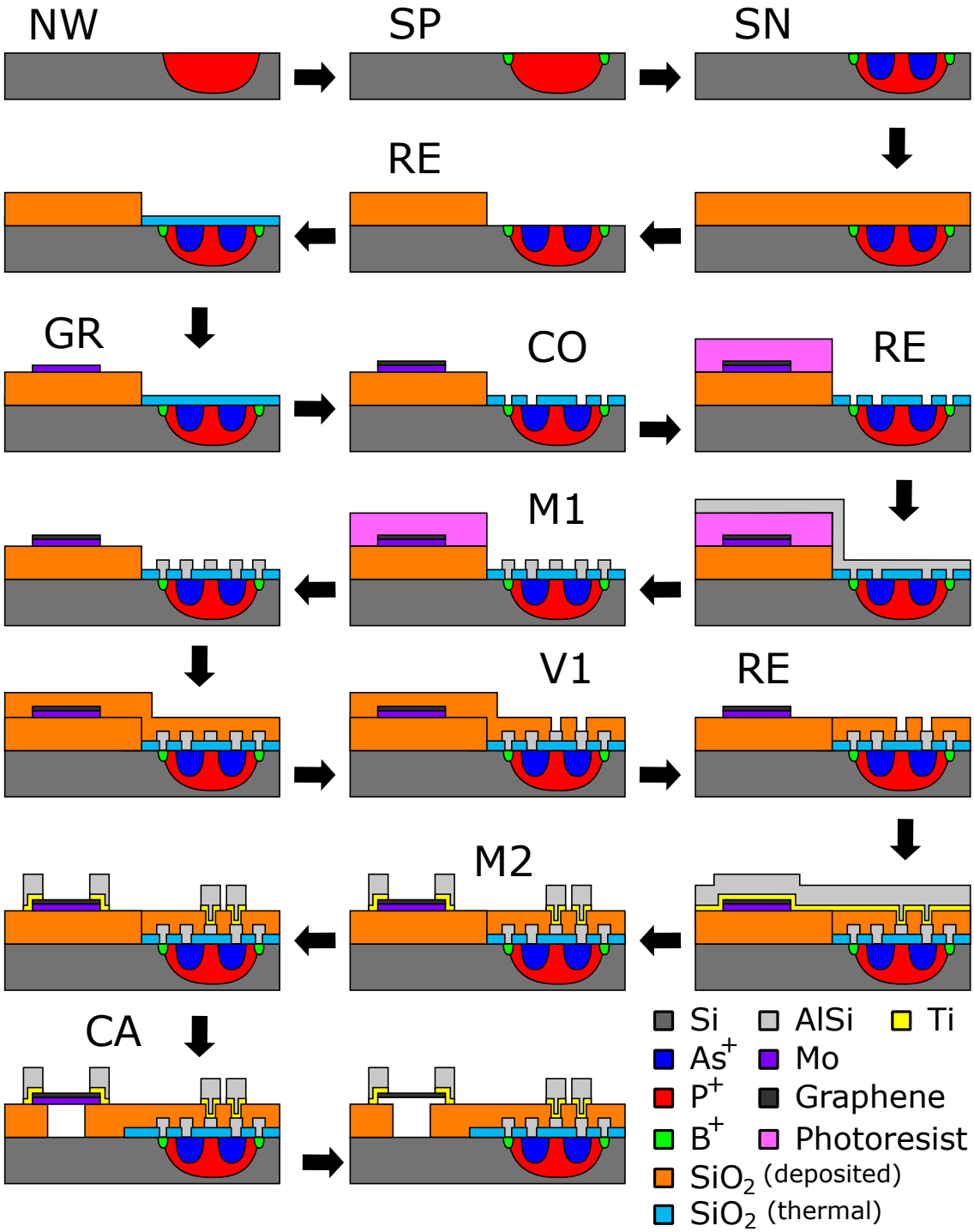


Figure F.10: Schematic illustration of all process steps in the integrated graphene-based Pirani pressure sensor with BICMOS process.

Table F.1: Full fabrication process flowchart of wafer 7. The listed recipes are specific for EKL systems and tools. Note that additional steps are performed after the final listed step in the flowchart to release the graphene strips.

ZERO LAYER		
Step	**Action**	**Remarks**
1.	Cleaning.	4 minutes Marangoni cleaning in 0.5 % HF.
2.	Epitaxial Growth.	2 μm, 1050 °C, 60 Torr.
3.	Coating.	EVG120, CO-3012-1.4um.
4.	Exposure.	COMURK0.0, energy 120, focus 0.
5.	Numbering.	Number wafers with quartz pen.
6.	Development.	EVG120, DEV-SP.
7.	Inspection.	Inspect if correctly developed.
8.	Dry etching.	Trikon Omega 201, URK_NPD at 20 °C.
9.	Resist strip.	Tepla Stripper, program 01.
10.	Cleaning.	Non-metals cleaning line.
NW LAYER		
Step	**Action**	**Remarks**
11.	Oxidation.	Furnace A1, DIBARVAR.
12.	Thickness.	Measure oxide thickness, target 20 nm.
13.	Coating.	EVG120, CO-3027-3.1um.
14.	Exposure.	Mask 1, IMAGE 1, energy 420, focus −1.
15.	Development.	EVG120, DEV-SP.
16.	Inspection.	Inspect overlay and if correctly developed.
17.	Implantation.	Ion P^+, energy 150 keV, dose 6E12 cm^{-2}.
18.	Resist strip.	Tepla Stripper, program 01.
19.	Cleaning.	Non-metals cleaning line.
20.	Anneal.	Furnace A1, OA002.
21.	Thickness.	Measure oxide thickness, target 230 nm.
22.	Oxide strip.	BHF wetbench, 3 minutes.
23.	Cleaning.	Non-metals cleaning line.
24.	Oxidation.	Furnace A1, DIBARVAR.
25.	Thickness.	Measure oxide thickness, target 20 nm.
SN LAYER		
Step	**Action**	**Remarks**
26.	Coating.	EVG120, CO-3012-1.4um.
27.	Exposure.	Mask 1, IMAGE 2, energy 120, focus 0.
28.	Development.	EVG120, DEV-SP.
29.	Inspection.	Inspect overlay and if correctly developed.
30.	Implantation.	Ion As^+, energy 40 keV, dose 5E15 cm^{-2}.
31.	Resist strip.	Tepla Stripper, program 01.
32.	Cleaning.	Non-metals cleaning line.
SP LAYER		
Step	**Action**	**Remarks**
33.	Coating.	EVG120, CO-3012-1.4um.
34.	Exposure.	Mask 1, IMAGE 3, energy 120, focus 0.
35.	Development.	EVG120, DEV-SP.
36.	Inspection.	Inspect overlay and if correctly developed.
37.	Implantation.	Ion B^+, energy 15 keV, dose 5E15 cm^{-2}.
38.	Resist strip.	Tepla Stripper, program 01.
39.	Cleaning.	Non-metals cleaning line.
Flowchart continues on next page		

VT ADJUST		
Step	**Action**	**Remarks**
40.	Coating.	EVG120, CO-3012-1.4um.
41.	Exposure.	Job g10a-3, energy 150, focus 0.
42.	Development.	EVG120, DEV-SP.
43.	Inspection.	Inspect if correctly developed.
44.	Implantation.	Ion B^+, energy 25 keV, dose 3E11 cm^{-2}.
45.	Resist strip.	Tepla Stripper, program 01.
46.	Cleaning.	Non-metals cleaning line.
47.	Coating.	EVG120, CO-3012-1.4um.
48.	Exposure.	Job g10a-5, energy 150, focus 0.
49.	Development.	EVG120, DEV-SP.
50.	Inspection.	Inspect if correctly developed.
51.	Implantation.	Ion B^+, energy 25 keV, dose 6E11 cm^{-2}.
52.	Resist strip.	Tepla Stripper, program 01.
53.	Cleaning.	Non-metals cleaning line.
OXIDE DEPOSITION		
Step	**Action**	**Remarks**
54.	Oxide strip.	BHF non-metals, etch 20 seconds.
55.	Cleaning.	Non-metals cleaning line.
56.	Deposition.	Novellus Concept One, xxnmstdteos, 600 nm.
57.	Thickness.	Measure oxide thickness, target 600 nm.
58.	Coating.	EVG120, CO-3012-1.4um.
59.	Exposure.	Mask 3, IMAGE 1, energy 150, focus 0.
60.	Development.	EVG120, DEV-SP.
61.	Inspection.	Inspect overlay and if correctly developed.
62.	Wet etching.	BHF non-metals, etch rate $\sim$ 200 $nm{\cdot}s^{-1}$.
63.	Resist strip.	Acetone 40 °C, 1 minute.
64.	Cleaning.	Non-metals cleaning line.
65.	Anneal.	Furnace C1, ICTOXA.
66.	Thickness.	Measure oxide thickness, target 100 nm.
GRAPHENE		
Step	**Action**	**Remarks**
67.	Catalyst.	Trikon Sigma, Mo_50nm_50C.
68.	Coating.	EVG120, CO-3012-1.4um.
69.	Exposure.	Mask 2, IMAGE 3, energy 140, focus 0.
70.	Exposure.	Job g10a_edge(full), energy 150, focus 0.
71.	Development.	EVG120, DEV-SP.
72.	Inspection.	Inspect overlay and if correctly developed.
73.	Dry etching.	Trikon Omega 201, Mo_test2, 25 °C.
74.	Resist strip.	NMP bath at SAL, 70 °C, $>$ 10 min.
75.	Deposition.	AIXTRON BM, Mo_NEW_915C_20minCH4.
76.	Backside cap.	Trikon Sigma, Ti10TiN_100nm_25C.

Flowchart continues on next page

CONTACT OPENINGS		
Step	**Action**	**Remarks**
77.	Coating.	EVG120, CO-3012-2.1um.
78.	Exposure.	Mask 2, IMAGE 1, energy 315, focus 0.
79.	Development.	EVG120, DEV-SP.
80.	Inspection.	Inspect overlay and if correctly developed.
81.	Dry etching.	Drytek, STDOXIDE, 35 seconds.
82.	Inspection.	Inspect if correctly etched.
83.	Resist strip.	NMP bath at SAL, 70 °C, > 10 min.
METAL 1		
Step	**Action**	**Remarks**
84.	Coating.	EVG120, CO-3012-2.1um.
85.	Exposure.	Mask 3, IMAGE 1, energy 340, focus 0.
86.	Exposure.	Job g10a_edge(full), energy 340, focus 0.
87.	Development.	EVG120, DEV-SP.
88.	Inspection.	Inspect if correctly developed.
89.	Bake.	Hotplate, 115 °C, 10 min.
90.	Test.	Trikon Sigma, leak-up rate test.
91.	Etch dip.	Use 0.55 % HF bath in SAL for 8 minutes.
92.	Metal deposition.	Trikon Sigma, AlSi_200nm_1kW_25C.
93.	Coating.	EVG120, SpeCO-3012-2.1um no HMDS.
94.	Exposure.	Mask 1, IMAGE 4, energy 340, focus -1.
95.	Development.	EVG120, DEV-SP.
96.	Inspection.	Inspect overlay and if correctly developed.
97.	Dry etching.	Trikon Omega 201, recipe Al02_25.
98.	Resist strip.	NMP bath at SAL, 70 °C, > 10 min.
DIELECTRIC		
Step	**Action**	**Remarks**
99.	Thickness.	Measure oxide thickness
100.	Deposition.	Novellus Concept One, xxnmstdteos, 600 nm.
101.	Thickness.	Measure oxide thickness, target 600 nm.
102.	Coating.	EVG120, CO-3012-2.1um.
103.	Exposure.	Mask 3, IMAGE 4, energy 315, focus 0.
104.	Development.	EVG120, DEV-SP.
105.	Inspection.	Inspect overlay and if correctly developed.
106.	Dry etching.	Drytek, STDOXIDE, 75 seconds.
107.	Resist strip.	NMP bath at SAL, 70 °C, > 10 min.
108.	Coating.	EVG120, CO-3012-2.1um.
109.	Exposure.	Mask 3, IMAGE 2, energy 340, focus 0.
110.	Development.	EVG120, DEV-SP.
111.	Wet etching.	BHF bath at SAL, etch rate ~ 200 nm·s^{-1}.
112.	Resist strip.	NMP bath at SAL, 70 °C, > 10 min.

Flowchart continues on next page

METAL 2		
Step	**Action**	**Remarks**
113.	Etch dip.	Use (1:7) BHF bath in SAL for 15 seconds.
114.	Metal deposition.	Trikon Sigma, 200 nm Ti and 1 μm AlSi.
115.	Coating.	EVG120, CO-3012-2.1um.
116.	Exposure.	Mask 2, IMAGE 2, energy 340, focus -1.
117.	Development.	EVG120, DEV-SP.
118.	Inspection.	Inspect overlay and if correctly developed.
119.	Dry etching.	Trikon Omega 201, custom recipe.
120.	Wet etching.	HF bath at SAL, etch Ti.
121.	Resist strip.	NMP bath at SAL, 70 °C, $>$ 10 min.
CAVITY		
Step	**Action**	**Remarks**
122.	Coating.	Manual coating, CO-3012-2.1um.
123.	Exposure.	Mask 2, IMAGE 4, energy 300, focus 0.
124.	Development.	Manual development, post bake 2 min.

G

Design Characterization

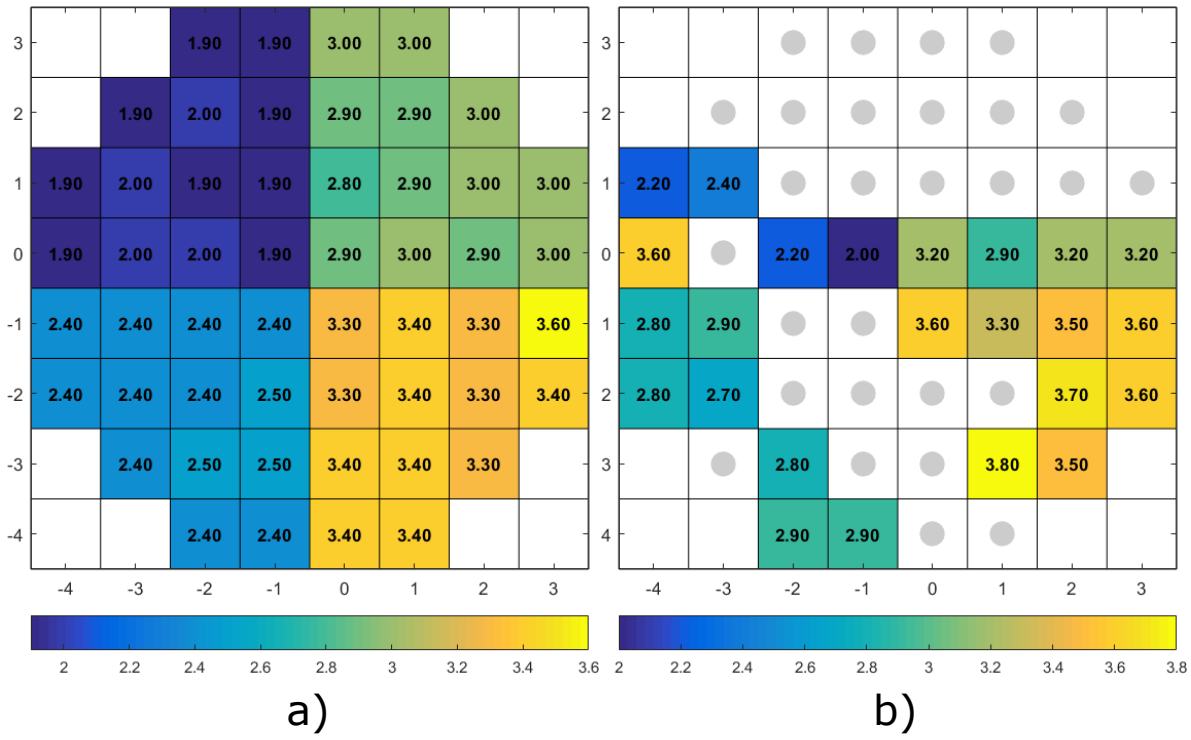


Figure G.1: Wafermaps depicting NOR switching voltage values [V] of wafer 3 in a) and wafer 7 in b). Broken devices are marked with a grey circle.

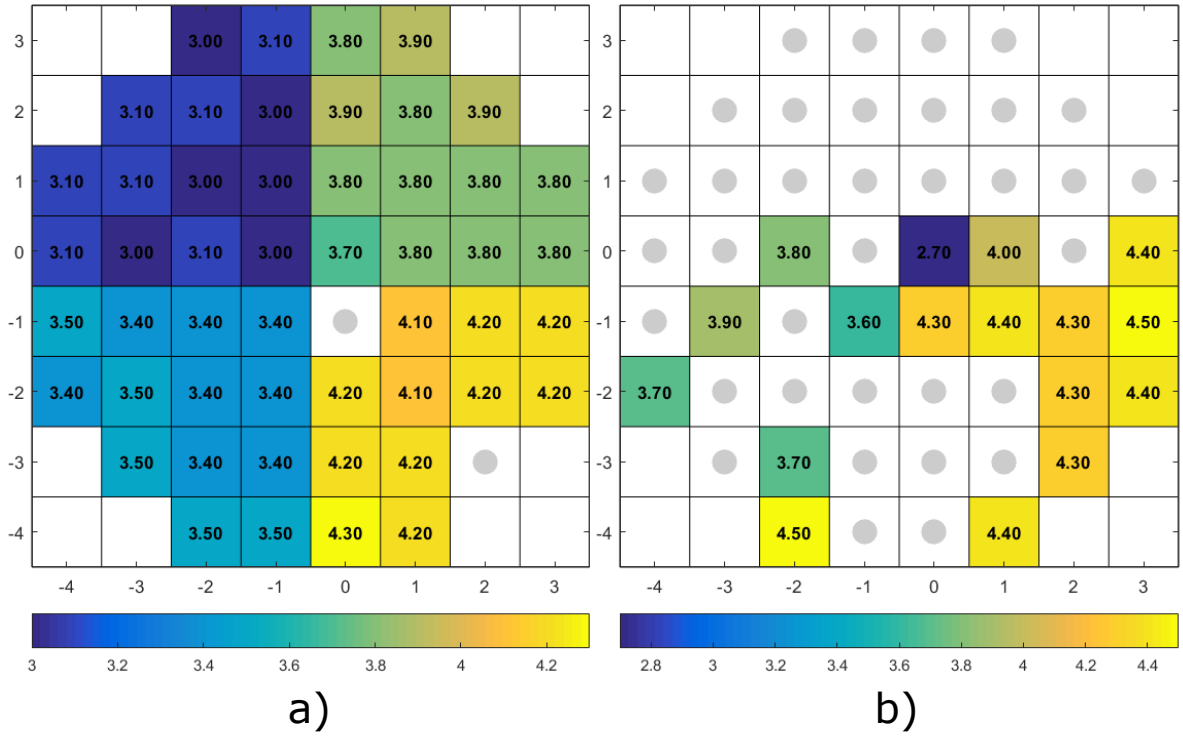


Figure G.2: Wafermaps depicting parity check gate switching voltage values [V] of wafer 3 in a) and wafer 7 in b). Broken devices are marked with a grey circle.

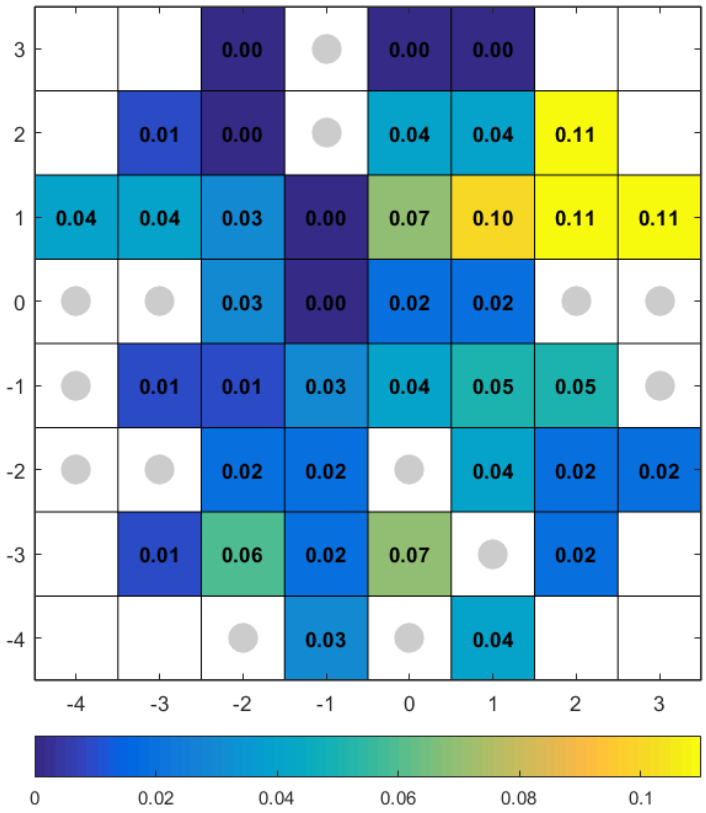


Figure G.3: Maximum offset of the comparator on wafer 3.

A Miniaturized Low Power Pirani Pressure Sensor Based on Suspended Graphene

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***Abstract*—Worlds first graphene-based Pirani pressure sensor is presented. Due to the decreased area and low thickness, the graphene-based Pirani pressure sensor allows for low power applications down to 0.9 mW. Using an innovative, transfer-free process, suspended graphene beams are realized. This allows for up to 100x miniaturization of the pressure sensor area, while enabling wafer-scale fabrication. The response of the miniaturized pressure sensor is similar to that of the much larger state-of-the-art Si-based Pirani pressure sensors, demonstrating the potential of graphene-based Pirani sensors.**

I. Introduction

Pressure sensors are one of the most widely used MEMS devices integrated in various systems and circuits and are a vital member of the sensor family. They require constant improvement to facilitate more functionalities. Nowadays, the trend of miniaturization is still very active and recent years awakened a trend of reducing power consumption and device dimensions. These trends are also relevant for MEMS devices and in this case, pressure sensors.

Pirani pressure sensors are an attractive and often used pressure sensor architecture due to their simplicity and robustness as no hermetic cavity, moving parts or accurate deflection measurement methods are required. Current Pirani implementations have typical dimensions of 100 μm x 200 μm with a power consumption of $\sim$1 mW or more [2]–[4]. The sensitivity and pressure range of these devices is limited as the gap can not be reduced to the nm range. A scaling law for the required power and dimensions for equal power consumption is taken from a widely used and confirmed analytical model for Pirani pressure sensors [5]. Moreover, the defined ohmic heating of the conductive bridge material is given by Equation 1, where I_b is the electric current forced through the conductive bridge, R_0 the bridge resistance at ambient temperature and pressure, κ_b the bridge thermal conductivity and w, L and t the bridge width, length and thickness respectively. It is clear that smaller dimensions require less power to obtain similar ohmic heating. This is where graphene has a huge advantage, as it is only a few nm thick.

$$\delta = \frac{I_b^2 R_0}{\kappa_b w L t} \tag{1}$$

A nano Pirani pressure sensor based on a CNT implementation exists [1], but it does not have a selective fabrication process. In this research, world's first graphene-based Pirani pressure sensors with a selective fabrication process [6] are presented that are significantly smaller then current implementations and therefore consume less power. Furthermore, their sensitivity is comparable to current state-of-the art Pirani pressure sensors.

By using graphene as the conductive bridge material, the footprint of the Pirani pressure sensor could be reduced by a factor 100x compared to existing micro-Piranis [2]. This is beneficial for many applications, such as in situ pressure monitoring inside vacuum sealed cavities for MEMS devices.

Furthermore, graphene-based Pirani pressure sensors with tuned nano-gap sizes will allow operation at ambient pressures and could be used for applications such as barometers for altitude measurements, as the gap size determines the operation range [5].

II. Experimental

The main fabrication steps are illustrated in Fig. 1. The first step (Fig. 1a) starts with bare silicon (Si) on which thermal wet oxidation is performed to create a silicon dioxide (SiO_2) layer of 600 nm. This is followed by the sputter deposition of a 50 nm thick molybdenum (Mo) layer that functions as a catalyst in the graphene growth process. The Mo layer is patterned by dry etching through a photoresist mask in a chlorine and hydrogen bromide gas mixture (Cl/HBr). The photoresist mask is stripped in n-methylpyrrolidon (NMP) at 70°C, since conventional organic cleaning involves nitric acid (HNO_3) which etches Mo.

In the second step (Fig. 1b), graphene is deposited by chemical vapor deposition (CVD) at 915 °C for 20 minutes. The carbon source is methane (CH_4), which reacts at the Mo surface so that carbon solutes in the Mo. During cooling the carbon solubility of Mo drops, which selectively forms multilayer graphene of $\sim$8 nm thick on its surface [7].

In the next step (Fig. 1c), metal interconnect is deposited by a lift-off process using evaporated gold/chromium (Cr/Au) as this material provides a good contact resistance to the multilayer graphene. This is followed by the cavity formation. The graphene/Mo stack is suspended by selectively removing the SiO_2 layer in a buffered hydrofluoric acid (BHF) wet etch. By controlling the cavity depth through the oxide thickness, the pressure range of the Pirani pressure sensor can be tuned.

In the final step (Fig. 1d), the Mo layer is removed by wet etching in hydrogen peroxide (H_2O_2). After critical point drying (CPD), the graphene adheres to the SiO_2 creating the heater bridge over the cavity. The absence of any graphene transfer steps combined with selective CVD graphene deposition enables wafer-scale fabrication of new devices with high yield [6].

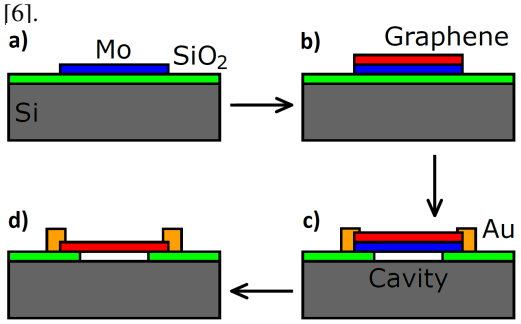

Fig. 1. Fabrication process overview of the suspended graphene pressure sensor [6] consisting of; a) deposition and patterning of 50 nm Mo on a 600 nm SiO_2 layer; b) selective CVD of graphene on Mo; c) 100 nm Au/Cr contact deposition and wet etching of the cavity using a photoresist mask; d) wet etching of Mo and CPD, resulting in a suspended graphene Pirani pressure sensor.

III. Results and Discussion

Scanning electron microscope (SEM) images in Fig. 2 show suspended ∼8 nm thick multilayer graphene bridge used in the Pirani pressure sensor. Different aspect ratios L/w up to 8 have been realized. High aspect ratios allow either higher sensitivity or lower power consumption. The devices are upto 100x smaller in area than current implementations [2].

The wet SiO_2 etching of the cavity under the graphene bridge does not result in straight cavity sidewalls. This influences the effective length of the bridge and is more dominant for the aspect ratio L/w = 6/5 presented in Fig. 2b. The aspect ratio of L/w = 8 in Fig. 2a shows a bridge that significantly sags towards the substrate. For aspect ratios above L/w = 8 the graphene bridges came in contact with the substrate. The graphene forms on the rough catalyst surface. As a consequence, the graphene is corrugated after removal of the Mo and extension of these corrugations could cause the graphene bridge to be larger than the gap and result in the observed sagging of the bridge. This effect could reduce the effective gap distance between the graphene bridge and the silicon substrate.

No visual damage to the graphene bridges due to processing is observed. Raman spectroscopy is performed during three stages of the process to investigate this further. The results in Fig. 3 show identical D/G peak ratios before and after release, which indicates no change in defect density [8], [9]. This provides evidence that the processing does not affect the graphene quality.

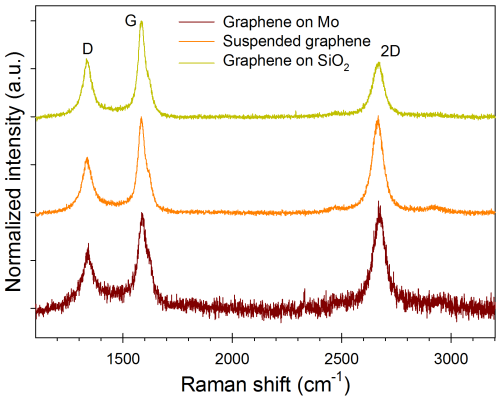

Fig. 3. Raman spectroscopy of graphene strips at three stages of the process. Including before release on Mo, after release on SiO_2 and suspended. Identical D/G ratios indicate no change in defect density. A Renishaw inVia Raman spectroscope with a red 633 nm laser is used.

The sensitivity of the Pirani pressure sensor is related to the gap depth. In the presented fabrication process, the gap depth can be varied by changing the thickness of the SiO_2. Furthermore, the sagging bridge is an disadvantageous result when attempting to control the gap depth. Careful control over the process is necessary to guarantee a reproducible and high yield fabrication.

A. Thermal Coefficient of Resistance

The sensitivity of the Pirani pressure sensor depends on the TCR of the heater material. The TCR of non-suspended graphene was determined by heating a sample on a temperature controlled chuck in a probe station to different temperatures while measuring its electrical resistance. The electrical resistance measurements are done at low bias voltage conditions to minimize the effect of resistive self-heating.

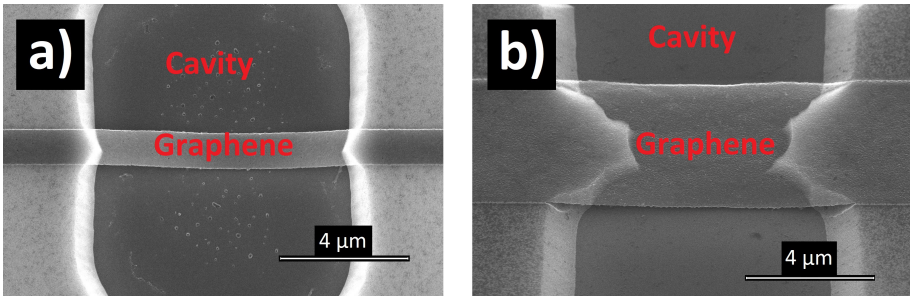

Fig. 2. SEM images of suspended graphene bridges, a) high aspect ratio (width of 1 μm and length of ∼8 μm) and b) low aspect ratio (width of 5 μm and length of ∼6 μm). Images taken under a 45° angle. The devices were visualized through a FEI XL50 SEM.

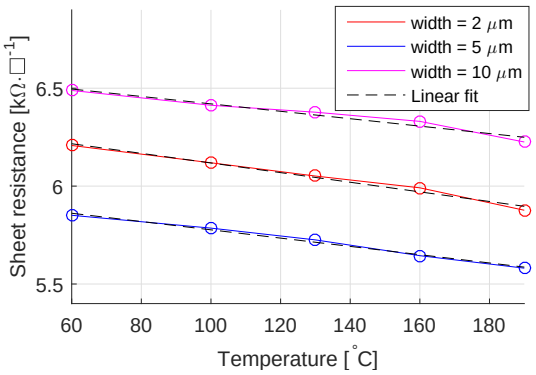

Fig. 4. Sheet resistance measurement results of non-suspended graphene strips 206 μm long and with different widths at different chuck temperatures. The difference in sheet resistance between the different strip widths is $\sim$5% and is considered due to process variations. The figure includes linear fits of which the largest fit error is 0.5%.

In Fig. 4 the results of non-suspended graphene strips of different widths are depicted. The TCR is constant over this temperature range. An average of (-3.6 $\pm$ 0.5) $\cdot 10^{-4}$ K^{-1} is found for the graphene strip, which matches values reported in literature [10].

B. Pressure Dependency

The pressure dependency of the electrical resistance of suspended and non-suspended graphene-based Pirani pressure sensors was investigated. The samples were placed in a pressure controlled vacuum chamber. The experimental setup is depicted in Fig. 5. The source and measurement unit (SMU) and pump controller are perform the measurements and drive the pressure controller, which sets the pressure in the vacuum chamber using a nitrogen (N_2) gas source. The SMU performs 4-wire current and voltage measurements on the sample.

The pressure controller was set to the desired value and reaches a stable pressure before measuring the resistance. A bias voltage sweep that incorporates both positive and negative voltage values, is performed by the SMU. The sample remains biased during pressure adjustments to reduce possible variations in temperature of the graphene pressure sensor. An upward and downward pressure sweep is performed to monitor drift and hysteresis of the resistance. Neither was observed in the reported measurement results.

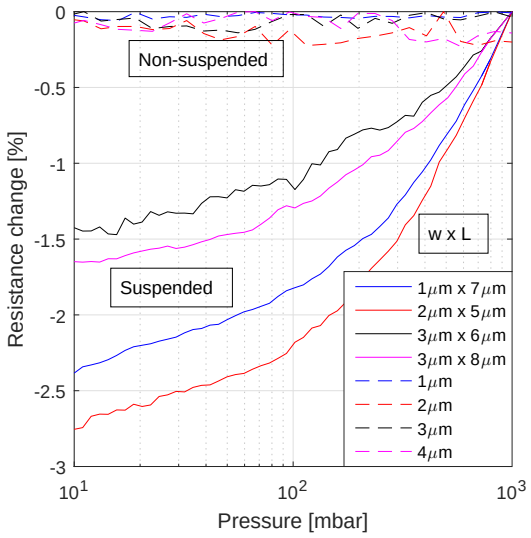

Fig. 6. Resistance pressure dependency of suspended and non-suspended graphene strips, marked in solid and dashed lines respectively, with different geometries, biased at 7.5 V. Total graphene strip length is 20 μm. Average sheet resistance is 830 Ω.

$$\Delta R = \frac{R(p) - max(R(p))}{max(R(p)} * 100 \qquad (2)$$

The resistance measurement results of suspended and non-suspended devices with different aspect ratios at different pressures are depicted in Fig. 6 as defined in Equation 2. Note that these devices have a significantly lower sheet resistance than the sample used to determine the TCR. A clear pressure dependence of the resistance is observed for the suspended devices, while the non-suspended devices show no measurable change. The maximum change in resistance is typically observed for narrow devices, which are thus more sensitive. However, a direct quantitative model for the relation between device geometry and resistance change is not derived.

The largest measured maximum resistance change (in Fig. 6) of the devices is approximately -2.75% at a power consumption of 8.5 mW. This maximum change is higher than that of

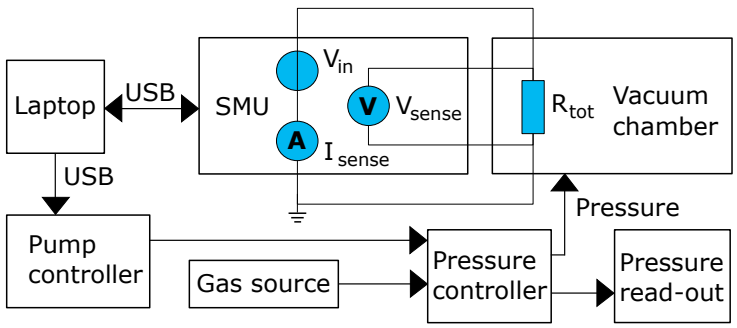

Fig. 5. Schematic illustration of the automatic pressure dependency measurements. A Keysight B2901A SMU, Rigol DP832A voltage source pump controller, Proportionair PA2254 dual-valve pressure controller and Keithey 199 pump readout are used in the experimental setup.

traditional Piranis found in literature with comparable power consumption [11]. Therefore, these graphene-based Pirani pressure sensors provide an improved performance compared to state-of-the-art implementations using other materials.

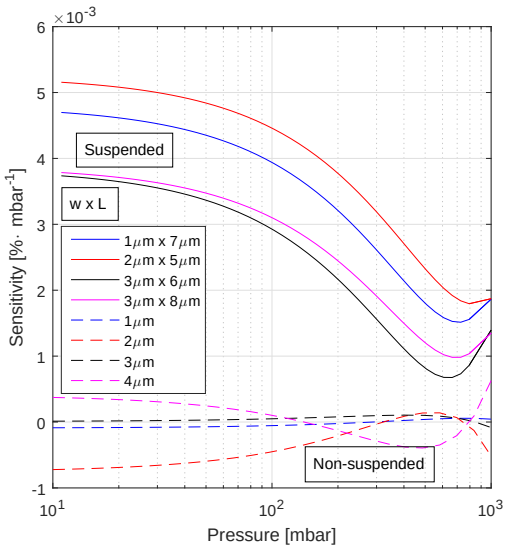

Fig. 7. Sensitivity of suspended and non-suspended graphene strips, marked in solid and dashed lines respectively. Different geometries biased at 7.5 V and total graphene strip length of 20 μm. Average sheet resistance is 830 Ω.

The sensitivity of the responses depicted in Fig. 6 is calculated by fitting a third order polynomial to the measurement data and taking the derivative. The results are given in Fig. 7. The non-suspended devices show a negligible sensitivity compared to the suspended devices. The maximum sensitivity for all suspended devices is measured at 10 mbar or lower. The sensitivity appears to rise again around ambient pressure, but this is an artifact caused by the third order polynomial fit.

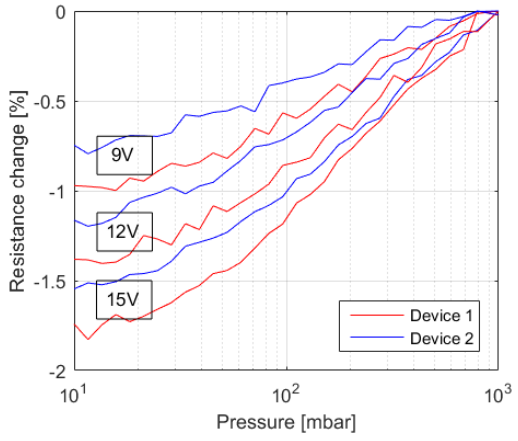

Fig. 8. Resistance pressure dependency of two suspended graphene strips with equal geometry and different bias conditions. The average sheet resistance is 10.6 kΩ due to more defects and the graphene strips are 5 μm wide and $\sim$7 μm long with a total strip length of 42 μm.

Another batch of graphene-based Pirani pressure sensors was fabricated which incorporates graphene with a higher sheet resistance (a factor of $\sim$13x) compared to the first batch. A single geometry is measured in this batch, with an aspect ratio of $\sim$1.4 that corresponds best with the geometry 3μm x 6μm of the first batch. The pressure dependent resistance change measurement results of this batch are depicted in Fig. 8. The devices biased at 9 V have a power consumption of 0.9 mW, which is a reduction with a factor of $\sim$9x compared to the first batch. In contrast, the maximum resistance change is reduced by a factor of $\sim$1.5x. These results indicate that graphene with more defects is favored for low power applications.

IV. Conclusions

We have demonstrated the feasibility of fabricating high-sensitivity graphene Pirani pressure sensors by a wafer-scale fabrication process. The fabrication process does not influence graphene quality. The TCR of the implemented multilayer graphene was found to be of the same order as reported in literature. Devices have been reduced by 100x compared to current implementations. The electrical resistance of suspended graphene bridges showed a pressure dependency, compared to a negligible pressure dependency for non-suspended graphene strips. A maximum resistance change of -2.75% was achieved, which is higher compared to traditional Pirani pressure sensors. A low power consumption of 0.9 mW was achieved while only reducing the sensitivity by a factor $\sim$1.5x. The excellent device performance, high volume wafer-scale fabrication process and the potential of tuning the device gap enable a wide range of future applications for suspended graphene-based Pirani pressure sensors.

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