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Mo, Jiarui; Li, Jinglin; May, Alexander; Rommel, Mathias; Vollebregt, Sten; Zhang, Guoqi

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Temperature Sensing Elements for Harsh Environments in a 4H-SiC CMOS Technology

Jiarui Mo, Jinglin Li, *Graduate Student Member, IEEE*, Alexander May, Mathias Rommel, Sten Vollebregt, *Senior Member, IEEE*, and Guoqi Zhang, *Fellow, IEEE*

***Abstract*— The demand for accurate temperature sensing in extreme temperatures is increasing. Traditional silicon-based integrated temperature sensors usually cannot survive above 200 °C. Many researchers have started to focus on semiconductors with a large bandgap. Among them, silicon carbide (SiC) is the most promising one. Nevertheless, most reported SiC sensors are in the form of discrete components and are not compatible with integrated electronics. In this work, we demonstrate an open 4H-SiC CMOS technology, and the fabrication steps are detailed. The temperature sensing elements in this technology, including resistors based on different implanted layers and MOSFETs, are characterized up to 600 °C. At room temperature, the resistive-based elements demonstrate large negative temperature coefficients of resistance (TCRs). With increasing temperature, the TCR starts to decrease and even becomes positive. The TCR change is due to the interplay between increasing dopant ionization rate and decreasing mobility as a function of temperature. The resistance change with temperature fits well into the Steinhart–Hart model and second-order polynomial equation. The p-type diode-connected MOSFET has a sensitivity of 4.35 mV/°C with a good linearity. The nMOS-based sensor has a maximum sensitivity of −9.24 mV/°C but a compromised linearity. The characterization of these sensing elements provides important results for potential users who will work on SiC integrated temperature sensing with this technology.**

***Index Terms*— Complementary metal–oxide–semiconductor, high temperature, sensor, silicon carbide (SiC).**

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Jiarui Mo, Jinglin Li, Sten Vollebregt, and Guoqi Zhang are with the Electronic Components, Technology and Materials (ECTM) Group, Department of Microelectronics, Delft University of Technology, 2628 CD Delft, The Netherlands (e-mail: mojiarui2017@gmail.com; g.q.zhang@tudelft.nl).

Alexander May and Mathias Rommel are with the Fraunhofer Institute for Integrated System and Devices Technology (IISB), 91058 Erlangen, Germany.

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I. Introduction

ACCURATE temperature sensing is crucial for numerous applications from consumer electronics to industrial fields [1], [2]. Traditional temperature sensors, such as thermocouples, thermistors, and resistive temperature detectors (RTDs), are accurate and reliable [3]. Nevertheless, they are relatively large in dimension. When a measurement system needs to be highly integrated and miniaturized, these bulky sensors are unsuitable. Thanks to the rapid development of silicon (Si) technology, people can make use of temperature-dependent layers or Si components in the mature Si technology as temperature sensing elements. For example, in a Si CMOS process, resistors based on different layers (metal layer, poly-Si layer, diffusion layer, and silicide), p-n diode, and MOSFET are commonly used for temperature sensing. Due to the continuous scaling down of the technology node, Si sensors can be fabricated in increasingly smaller dimensions compared to their macroscopic counterpart. Another advantage of the Si temperature sensor is that it can be incorporated with desired on-chip signal conditioning circuits to fit different applications. Such an integrated sensor is very attractive in terms of cost, dimension, and performance [4].

In recent years, the demand for high-temperature sensing, e.g., for combustion control and chemical processing, has grown rapidly. In these emerging applications, the operation temperature of the sensor usually needs to be far beyond the limit for bulk Si CMOS technology and even silicon-on-insulator (SOI) technology. As a result of the narrow bandgap of Si, the intrinsic carrier concentration of Si is high and increases rapidly with elevated temperatures [5]. As summarized by Makinwa [6], the maximum operation temperature of most Si technology-based temperature sensors is below 200 °C. Due to this limitation, many researchers have now turned to devices that are based on wide bandgap materials to obtain reliable performances at elevated temperatures [5].

Silicon carbide (SiC) is one of the most important materials in the family of wide bandgap semiconductors. Thanks to its large bandgap, it has a much lower intrinsic carrier concentration than Si. The mechanical and chemical stability also makes it suitable for harsh environment applications. In recent years, many researchers have put much effort into developing temperature sensors with SiC for high temperatures by taking

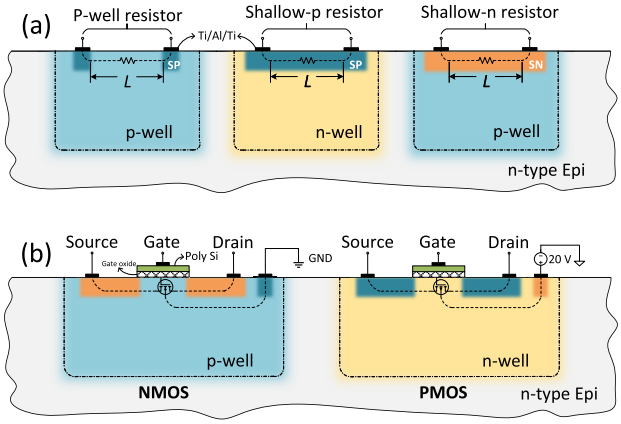

Fig. 1. Cross-sectional view of temperature sensing element studied in this work. (a) Resistive elements. (b) MOSFET devices. (Some layers, such as field oxide, silicide, intermetal isolation, second metallization, and passivation, are omitted in the schematic.)

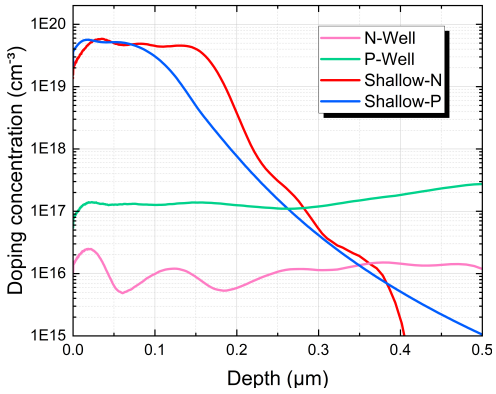

Fig. 2. Doping profiles of NW, PW, SN, and SP layers.

advantage of its excellent physical properties; however, most work focuses on discrete components, and few of them are compatible with existing SiC IC technologies. In the past decade, there have already been some low-voltage IC technologies based on SiC reported in the literature, such as SiC bipolar junction transistor (BJT) technology developed by the KTH Royal Institute of Technology and SiC CMOS technology developed by the University of Arkansas and Raytheon, U.K. [7], [8], [9]. These reported SiC circuits showed a much higher operation limit than the Si-based circuit despite the complexity being far less than the Si counterpart. This proves the great potential of implementing the integrated temperature sensor system for high-temperature applications. However, the temperature sensing elements compatible with the corresponding technology were not comprehensively studied in the previous work.

In this article, we report the characterization of various CMOS-compatible temperature sensing elements in an emerging SiC CMOS technology. This technology is developed by the Fraunhofer Institute for Integrated Systems and Device Technology IISB and is available through Europractice. The resistors based on different layers in this technology and diode-connected MOSFETs are characterized up to 600 °C. The temperature response of these sensing elements is discussed. The reported characteristics of different temperature sensing elements are relevant for IC designers who plan to work on SiC integrated temperature sensors in this SiC CMOS technology.

II. Temperature Sensing Element in the SiC CMOS Technology

The resistor is the most basic component in any IC technology. These resistors can be used as temperature sensors by taking advantage of their temperature-dependent resistance. In traditional Si CMOS technology, various resistors are available for temperature sensing, including metal resistors, polysilicon resistors, diffusion resistors, and silicide resistors. In our SiC CMOS technology, the metal layer, poly-Si layer, silicide layer, and implantation layer are potential options for temperature sensing; however, we will focus on SiC implanted layers, which are unique in this process. The cross section of these devices is given in Fig. 1(a).

TABLE I
Implantation Parameter Used in the Fraunhofer IISB's SiC CMOS Process

Layer	Dose ($1/cm^2$)	Ion energy (keV)	Layer	Dose ($1/cm^2$)	Ion energy (keV)
NW	2.0×10^{11}	380	PW	5.0×10^{12}	540
	1.5×10^{11}	270		2.0×10^{12}	450
	1.0×10^{11}	180		1.2×10^{12}	320
	1.0×10^{11}	80		1.0×10^{12}	200
	1.0×10^{11}	20		1.0×10^{12}	140
				7.0×10^{11}	75
				4.0×10^{11}	35
SN	4.0×10^{14}	90	SP	2.8×10^{14}	90
	2.3×10^{14}	50		1.8×10^{14}	60
	2.0×10^{14}	25		1.4×10^{14}	30

The SiC CMOS technology contains four implantation layers, i.e., n-well (NW), p-well (PW), shallow-n (SN), and shallow-p (SP) layers. All implantations are performed into an n-type SiC epitaxial layer with a thickness of 9 μm and a doping concentration of $\sim 1 \times 10^{15}$ cm^{-3}. First, the NW layer is formed by five overlapping implantations with nitrogen (N). Similarly, the PW is formed by seven implantations of aluminum (Al) dopants. Based on NW and PW layers, the highly doped regions, i.e., SN and SP layers, are defined by three additional implantations with nitrogen and aluminum, respectively. The ion energy and dose of every ion implantation are listed in Table I. After implantation, a 30-min annealing step at 1700 °C is done to restore the crystal lattice damage and activate the dopants. During the post-implantation annealing, the SiC wafer is encapsulated by a carbon cap to prevent Si sublimation and the formation of step bunching. The resulting doping profiles of different layers are plotted in Fig. 2.

Poly-Si (n-type) is patterned on top of thermally grown gate oxide as the gate terminal, and the minimum length of the gate is 2 μm. Then, by fabricating the ohmic contact on both sides of a stripe, resistors based on different implantation layers can be produced. NiAl and Ti/Al are used to make ohmic contact with SN and SP regions, respectively. For contacting lightly doped layers (PW and NW), the corresponding heavily doped layer is fabricated at the contact region to ensure proper ohmic

contact. Finally, the wafer is patterned with Ti/Al/Ti stack to interface with instruments. It needs to be mentioned that in this technology, all the n-wells are shorted together via the n-type epi layer and are biased at the supply voltage. As a result, the NW-based resistor is not feasible for practical use and will not be discussed. In this work, all resistors' dimensions are kept the same: the width of the resistor (w) is 30 μm and the length (l) is 200 μm.

Apart from the resistor-based temperature sensors, MOSFET devices are widely used as temperature sensors. The performance of the MOSFET device strongly depends on temperature, and a diode-connected MOSFET is a common way for temperature sensing applications. In this configuration, the gate/drain and source/bulk terminals are shorted together. Under the constant current bias (I_{bias}), the voltage drop (V_F) across the device is monitored. The expression of V_F can be written as

$$V_F = \left(\frac{2I_{\text{bias}}L}{\mu_c C_{\text{ox}} W}\right)^{1/2} + V_{\text{th}} \tag{1}$$

where W and L are the width and channel length of the MOSFET, respectively; V_{th} is the threshold voltage; and μ_c and C_{ox} are channel mobility and gate oxide capacitance per unit area, respectively. As both V_{th} and μ_c are temperature-dependent, V_F can reflect the temperature. Here, diode-connected SiC nMOS and pMOS are measured, and again, different types of devices are with the same dimension, i.e., W/L equals 100/6 μm. The schematic of the SiC MOSFET is shown in Fig. 1(b). The n-wells are shorted together as mentioned before, while the p-wells can be biased individually.

It is worth mentioning that a diode-based temperature sensor is also available in this technology, and this is detailed in our previous work [10].

III. Results and Discussion

A. Methodology

All the devices are characterized on chip level with a Nextron microprobe station. The microprobe station is equipped with multiple rhodium probes for high-temperature measurement. The probes are connected to Keithley 2612B Sourcemeter to measure the electrical characteristics. For resistive devices, the four-probe method is performed to eliminate the wire resistance. The device under test can be heated up by the ceramic chuck up to 750 °C. Nevertheless, the devices are only measured until 600 °C because the metallization layer melts above 600 °C. Due to the high temperature, the chamber is pumped in a rough vacuum to prevent the oxidization of the probes and devices' pads during measurement. For each type of device, five samples are chosen from different locations on a SiC wafer, i.e., from the center, left, right, top, and bottom of the wafer.

B. Resistor-Based Temperature Sensor

The I–V curves of resistors based on different layers are plotted in Fig. 3(a)–(c). For SN, SP, and PW resistors, linear I–V relations can be observed at all measured temperature points up to 600 °C. This confirms that the contact from the heavily doped layer to the metallization is ohmic. At room temperature, the sheet resistance of SN, SP, and PW layers are 1.04 ± 0.01 kΩ/sq, 39.36 ± 0.19 kΩ/sq, and 400.66 ± 3.40 kΩ/sq, which aligns with the values reported in [11]. The standard deviation is lower than the previous run, indicating a better uniformity across the wafer even with the 6-in substrate. Fig. 3(d)–(f) demonstrates the sheet resistance and resistivities of different layers as a function of temperature.

In Fig. 3(d), the resistivity of the SN layer experiences a drop from room temperature to 250 °C. In this temperature range, the temperature coefficient of resistance (TCR) varies from −1965 to −173 ppm/°C. The Steinhart–Hart equation is applied to approximate the nonlinear temperature response of this region [12]. This equation is an empirical model that has the best mathematical fit with a thermistor with a negative TCR, and it is expressed as follows:

$$\frac{1}{T_k} = A + B\ln R(T_k) + C[\ln R(T_k)]^3 \tag{2}$$

where A, B, and C are Steinhart–Hart coefficients and need to be extracted for different devices. $R(T_k)$ is the resistance in ohm at a certain temperature in kelvin T_k. For SN resistor operating below 250 °C, the best fit is obtained when $A = -0.84$, $B = 0.14$, and $C = -5.88 \times 10^{-4}$, as shown by the solid curve between room temperature and 250 °C in Fig. 3(d).

Above 250 °C, the TCR of the SN resistor becomes positive. For a more linear temperature response, the resistance can be modeled as follows [13]:

$$R(T) = R_{\text{ref}}\left(1 + \alpha_1\Delta T + \alpha_2\Delta T^2\right) \tag{3}$$

where α_1 and α_2 are the first- and second-order temperature coefficients, respectively; R_{ref} is the resistance at reference temperature (250 °C in this case); and ΔT is the temperature difference compared to the reference. Here, the best fit is obtained when $\alpha_1 = 188$ ppm/°C, $\alpha_2 = 0.93$ ppm/(°C)^2, and $R_{\text{ref}} = 5601$ Ω. At temperatures above 400 °C, the resistor demonstrates excellent linearity with a positive TCR of 614 ppm/°C. This makes it a suitable element for high-temperature monitoring applications.

The SP device has a monotonically decreasing resistance with increasing temperature, as shown in Fig. 3(e). The observed trend is similar to the heavily Al-doped SiC layer reported in [14]. The resistance of the SP resistor is much larger than that of the SN resistor, though they have a similar doping profile. This is partly due to the high ionization energy of the p-type dopant. The ionization energies of Al acceptors occupying hexagonal sites (ΔE_{A_h}) or cubic sites (ΔE_{A_k}) are 180 and 260 meV, respectively [15]. On the contrary, the nitrogen donor has a much lower ionization energy of around 61 meV (ΔE_{D_h}) and 126 meV (ΔE_{D_k}) at the corresponding sites [16], [17]. In addition, the lower mobility of holes in 4H-SiC is also responsible for the larger resistivity of the SP layer [17]. Near room temperature, the SP resistor has the largest sensitivity to temperature (TCR = −8581 ppm/°C), and the absolute value of TCR keeps decreasing with the temperature and reaches its minimum of −803 ppm/°C at 600 °C. Since the TCR is negative in the full measured range, only the Steinhart–Hart model is applied to describe

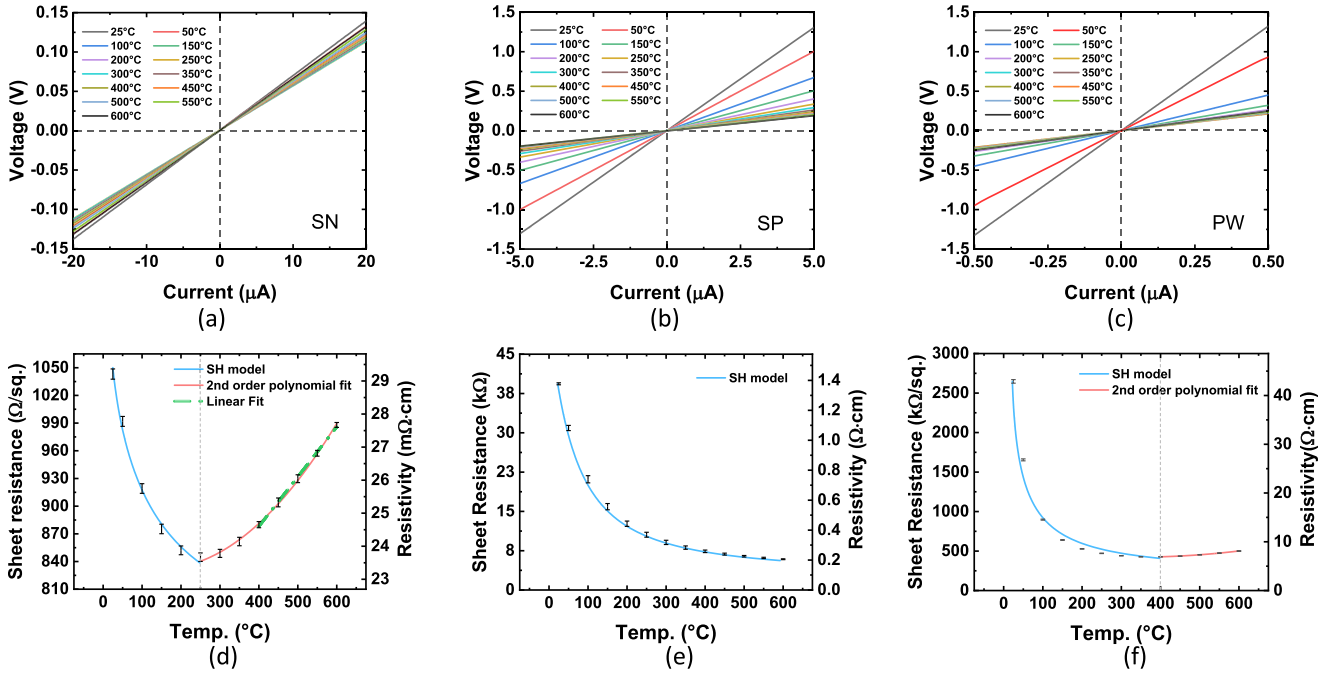

Fig. 3. *I–V* characteristics of (a) SN, (b) SP, and (c) PW resistor from room temperature to 600 °C. Sheet resistance and layer resistivity of (d) SN, (e) SP, and (f) PW from room temperature to 600 °C (the error bars represent the standard deviation from five devices).

the resistor with negative TCR. The fitting curve is given in the solid line in Fig. 3(e), where $A = -0.018$, $B = 2.08 \times 10^{-3}$, and $C = -2.35 \times 10^{-6}$.

Fig. 3(f) demonstrates the temperature-dependent resistance of the PW resistor. Similar to the SN resistor, TCR changes from negative to positive. The resistor has very similar resistance at 350 °C and 400 °C, which indicates that the TCR changes from negative to positive between 350 °C and 400 °C. When the TCR is negative, the Steinhart–Hart model has the best fit to the measured data when $A = -0.066$, $B = 6.89 \times 10^{-3}$, and $C = -1.02 \times 10^{-5}$. Above 400 °C, the resistance can be predicted by applying (3), given that $\alpha_1 = 335$ ppm/°C, $\alpha_2 = 2.66$ ppm/(°C)^2, and $R_{\text{ref}} = 426.6$ kΩ.

The transmission line method (TLM) is used to determine the contact resistance of the resistive device at room temperature. For n-type and p-type resistors, the contact resistances are 285 Ω and 21.8 kΩ, respectively. It is expected that these resistances decrease as a function of temperature [18], [19]. Compared to the enormous resistance of the device, the contact resistance is negligible.

To better understand the change of resistance with respect to temperature for different layers, we express the resistance as follows:

$$R = \frac{1}{\sigma} \cdot \frac{l}{wd} = \frac{1}{e(\mu_n n + \mu_p p)} \cdot \frac{l}{wd} \tag{4}$$

where σ is the layer conductivity; d is the depth of the layer; e is the elementary charge; μ_n and μ_p stand for the mobilities of free electrons and holes, respectively; and n and p are the concentrations of free electrons and holes, respectively. Due to the wide bandgap of 4H-SiC, the intrinsic carrier concentration (n_i) is approximately 10^{11} cm^{-3} even at 600 °C, i.e., our highest measured temperature [20], [21]. Considering the doping concentration given in Fig. 2, the minority carriers are negligible and have a limited contribution to the conduction. Hence, σ can be simplified to $e\mu_n n$ for the SN layer and $e\mu_p p$ for the SP and PW layers. n and p can be approximated as the density of ionized donors and acceptors, which can be calculated using the neutrality equation [15], [22], [23]

$$n = \frac{N_{D_h}}{1 + g_D \frac{n}{N_C} \exp\left(\frac{\Delta E_{D_h}}{k_B T_k}\right)} + \frac{N_{D_k}}{1 + g_D \frac{n}{N_C} \exp\left(\frac{\Delta E_{D_k}}{k_B T_k}\right)} \tag{5}$$

and

$$p = \frac{N_{A_h}}{1 + g_A \frac{p}{N_V} \exp\left(\frac{\Delta E_{A_h}}{k_B T_k}\right)} + \frac{N_{A_k}}{1 + g_A \frac{p}{N_V} \exp\left(\frac{\Delta E_{A_k}}{k_B T_k}\right)} \tag{6}$$

where N_D and N_A represent the donor and acceptor density in n-type and p-type material, respectively, and the subscript indicates the hexagonal site (h) and cubic site (k). For 4H-SiC, the impurity occupies both sites equally [15], [22], [24]. As the doping density is not a constant in the implanted layers, N_D and N_A are approximated by averaging the net doping concentration from the surface to the junction depth. Parameters g_D and g_A, with a typical value of 2 and 4, are degeneracy factors of the donor and acceptor in 4H-SiC. k_B is Boltzmann's constant. N_C and N_V are the effective densities of states in the conduction and valence bands and have a temperature dependency of $\sim T^{(3/2)}$. We consider $N_C = 1.7 \times 10^{19}$ cm^{-3} and $N_V = 2.5 \times 10^{19}$ cm^{-3} at room temperature. The ionization energies have a strong dependency on the doping concentration due to the screening effect, which can

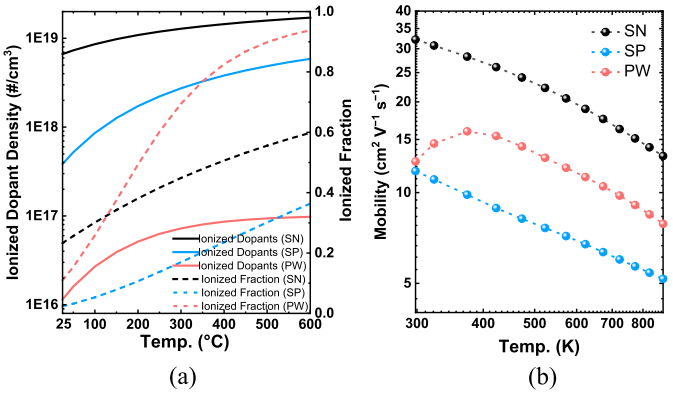

Fig. 4. (a) Number/fraction of the ionized dopants with respect to temperature is expressed with double y-axis. (b) Extracted mobility of different layers from room temperature to 600 °C. The 1st-order derivative of the curves is equal to $-m$.

TABLE II
PARAMETERS USED FOR ESTIMATING DOPING-DEPENDENT IONIZATION ENERGY

Dopant [Ref.]	E_0 (meV)	α (meV · cm)
N (h) [16]	64	1.2×10^{-5}
N (k) [16]	125.6	2.5×10^{-5}
Al (h) [24]	205	1.7×10^{-5}
Al (k) [25]	265	3.6×10^{-5}

be written as [16], [16], [24], [25], [26]

$$\Delta E_D = \Delta E_{D0} - \alpha_D N_D^{\frac{1}{3}} \tag{7}$$

$$\Delta E_A = \Delta E_{A0} - \alpha_A N_A^{\frac{1}{3}} \tag{8}$$

where ΔE_{D0} and ΔE_{A0} denote the ionization energy of lightly doped 4H-SiC, and α_D and α_A are parameters describing the doping dependency. The parameters used to estimate the ionization energy are summarized in Table II. In our calculation, the influence of doping level spreading and the density of state smearing on the ionization are neglected because the impact was found to be minor. The more extensive theoretical model of ionization considering these effects can be found elsewhere in [27].

The densities of ionized dopants in different implanted layers at elevated temperatures are given by solid lines in Fig. 4(a), and the broken line indicates the ionization rates (n/N_D and p/N_A). The calculation results show that none of these layers reaches complete ionization even at 600 °C. Therefore, at the low-temperature region, the negative TCR is attributed to the increasing ionized dopants. However, the layer conductivity does not keep increasing because the carrier mobility decreases as a result of scattering. The impact of temperature-dependent ionization and carrier mobility on TCR can be expressed as

$$\frac{\partial \sigma}{\partial T} \sim \mu_n \frac{\partial n}{\partial T} + n \frac{\partial \mu_n}{\partial T} \text{ or } \frac{\partial \sigma}{\partial T} \sim \mu_p \frac{\partial p}{\partial T} + p \frac{\partial \mu_p}{\partial T} \tag{9}$$

where $(\partial\sigma/\partial T)$ that equals zero is the temperature when the TCR changes from negative to positive. Equation (9) reveals the competing mechanism between the increasing ionization and mobility degradation with respect to temperature.

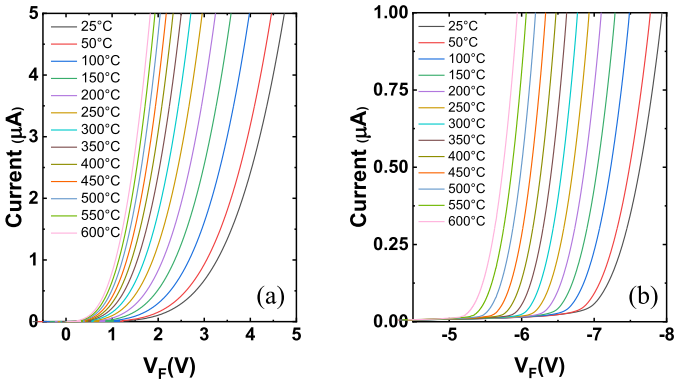

Fig. 5. I–V characteristic of diode-connected (a) nMOS and (b) pMOS from room temperature to 600 °C.

For both SN and PW resistors, the TCR changes from negative to positive at a certain temperature. For SN resistors, the increase of ionization tends to have less increase rate at a higher temperature, which is indicated by the monotonical decrease of $\partial n/\partial T$ with increasing temperature. This is more obvious when looking at the PW resistor, where ionized dopant density rises rapidly with temperature and then tends to saturate. In these situations, the carrier mobility reduction induced by the scattering effect starts to dominate, which turns the TCR positive. The SP resistor, however, has a negative TCR and does not turn positive as the SN and PW resistors do. From Fig. 4(a), the ionization ratio of the SP layer is still less than 0.4 even at 600 °C due to the high doping concentration and large ionization energy. It suggests that there are still a large number of dopants that can be ionized and can compensate for the decrease in mobility. It can be inferred that the TCR will become positive if a higher temperature is applied to the SP resistor.

The extracted mobility of different charge carriers is plotted in Fig. 4(b). The temperature dependency of mobility can be described by $\mu \sim T_k^{-m}$, where m is a parameter depending on the scattering mechanism. It can be seen from Fig. 4(b) that m changes with temperature, implying a combination of different scattering mechanisms. For heavily doped layers (SN and SP), m keeps increasing with the temperature. This indicates that the scattering is more influenced by the acoustic phonon, and neutral impurity scattering is less pronounced at higher temperatures [28]. A mobility drop can be observed for the PW layer with decreasing temperature. This might be due to the effect of ionized impurity scattering, where the temperature dependency follows $\sim T_k^{1.5}$ [29], [30].

C. MOSFET-Based Temperature Sensor

The I–V_F curves of the diode-connected NMOS and PMOS are given in Fig. 5(a) and (b). From room temperature to 600 °C, both types of MOSFETs show characteristics similar to a diode, where the current increases significantly after a threshold. As mentioned in (1), the variation of V_F with respect to temperature depends on the channel mobility and the transistor's threshold voltage. Unfortunately, in SiC MOSFETs, these two parameters do not follow a linear relationship with temperature, especially for the channel mobility [31], [32],

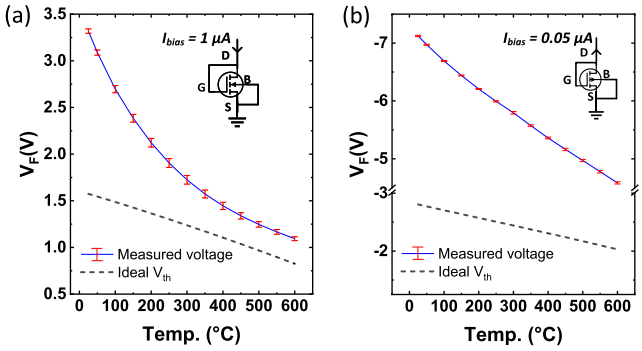

Fig. 6. Ideal V_{th} and temperature response (V_F versus temperature) of diode-connected (a) nMOS and (b) pMOS from room temperature to 600 °C (the error bar shows the standard deviation of the output voltage).

[33], [34]. The channel mobility dominates the temperature dependency of V_F when I_{bias} is large. Conversely, when I_{bias} is small so that V_F approaches the threshold voltage, the threshold voltage will dominate the change of V_F [35], [36]. In the measurement, the bias current is kept low to minimize the effect of channel mobility as well as the voltage drop on the series resistance (mainly contributed by the contact resistance) to V_F. By doing this, we assume that the change in the first term of (1) becomes negligible. The ideal expression for V_{th} of a nMOS can be written as

$$V_{th} = \phi_{ms} + 2\psi_B + \frac{\sqrt{4e\varepsilon_{SiC}N_A\psi_B}}{C_{ox}} \tag{10}$$

where ϕ_{ms} is the work function difference of the SiC substrate and the n-type poly-Si gate, ψ_B represents the temperature-dependent Fermi potential of the substrate, and ε_{SiC} stands for the permittivity of SiC. When the temperature increases, ψ_B decreases due to the increase of the intrinsic carrier concentration. Despite the increase of ϕ_{ms} with temperature, the ideal V_{th} experiences a drop with increasing temperature in general, as reported in literature [31], [37], [38], [39], [40]. For V_{th} of pMOS transistors, a similar expression can be written, and the magnitude of the threshold voltage also decreases with temperature [41]. The ideal V_{th} of SiC MOSFETs is calculated and plotted in Fig. 6.

The measured I–V_F curves of the diode-connected nMOS and pMOS are also given in Fig. 6(a) and (b), respectively. The bias current for the diode-connected nMOS is 1 μA, and for the diode-connected pMOS, it is 0.05 μA. The chosen bias current is lower for pMOS because the p-type device has weaker driving capability for current. From room temperature to 600 °C, both types of MOSFETs show characteristics similar to a diode, where the current increases significantly after a threshold. In comparison to the ideal V_{th} calculated by (1), the measured V_F has a lower magnitude as well as a smaller slope. The reason is that the charge carrier trapped at interface states Q_{it} and fixed oxide charge Q_f is not included in (1). Although Q_f is often considered as a constant with respect to temperature [42], Q_{it} is sensitive to the temperature. At low temperatures, charge carriers in the conductive channel are trapped by the interface states, which makes the threshold voltage higher than the theoretical value. As the temperature increases, these trapped charge carriers are released due to the movement of the Fermi level toward the center of the forbidden band, and this contributes to the drop of threshold voltage. The observed effect of trapped charges on V_{th} is similar to [31].

The sensitivity of the n-type MOSFET experiences a continuous drop from −9.24 mV/°C at room temperature to −1.44 mV/°C. The pMOS-based sensor presents a more linear temperature response than nMOS devices, and the linear fit suggests an overall sensitivity of 4.35 mV/°C in the measured range, with a coefficient of determination (R^2) of 99.6%. The measured V_F versus T of the pMOS and nMOS devices show a similar trend of V_{th} versus T as reported in [41], where V_{th} of the nMOS seems to decrease exponentially with temperature, while V_{th} of the pMOS has a more linear trend. This confirms that V_{th} plays a major role in V_F under this bias condition.

IV. Conclusion

This work introduces the 4H-SiC CMOS technology as a promising platform to realize temperature sensing in high-temperature environments. The technology features a double-well process with a minimum gate length of 2 μm. Resistors based on different implanted layers and diode-connected MOSFETs, which are commonly used for temperature sensing in IC technology, are characterized at elevated temperatures up to 600 °C. A transition where the TCR changes from negative to positive can be observed in the measured temperature range. This is due to the interplay between incomplete ionization and carrier mobility degradation. The SP resistor has a negative TCR up to 600 °C due to the large ionization energy and the high doping density. The temperature dependency of the implanted layers can be well fitted by combining the Steinhart–Hart model and first-/second-order temperature coefficients. The MOSFET-based temperature sensors are also measured. V_F of n-type MOSFET showed a large temperature sensitivity up to −9.24 mV/°C; however, the response has poor linearity. The temperature response of the pMOS device is more linear. The linear fit of the result indicates a sensitivity of 4.35 mV/°C with R^2 of 99.6% across the measurement range.

References

[1] D. G. Senesky, B. Jamshidi, K. B. Cheng, and A. P. Pisano, "Harsh environment silicon carbide sensors for health and performance monitoring of aerospace systems: A review," *IEEE Sensors J.*, vol. 9, no. 11, pp. 1472–1478, Nov. 2009.

[2] G. Brezeanu et al., "High temperature sensors based on silicon carbide (SiC) devices," in *Proc. Int. Semiconductor Conf. (CAS)*, Oct. 2015, pp. 3–10.

[3] A. Feteira, "Negative temperature coefficient resistance (NTCR) ceramic thermistors: An industrial perspective," *J. Amer. Ceram. Soc.*, vol. 92, no. 5, pp. 967–983, May 2009.

[4] K. A. A. Makinwa, "Smart temperature sensors in standard CMOS," *Proc. Eng.*, vol. 5, pp. 930–939, Jan. 2010.

[5] P. French, G. Krijnen, and F. Roozeboom, "Precision in harsh environments," *Microsyst. Nanoeng.*, vol. 2, no. 1, pp. 1–12, Oct. 2016.

[6] K. Makinwa. *Temperature Sensor Performance Survey*. Accessed: Oct. 2018. [Online]. Available: http://ei.ewi.tudelft.nl/docs/TSensor_survey.xls

[7] S. Kargarrazi, H. Elahipanah, S. Saggini, D. Senesky, and C.-M. Zetterling, "500 °C SiC PWM integrated circuit," *IEEE Trans. Power Electron.*, vol. 34, no. 3, pp. 1997–2001, Mar. 2018.

[8] A. Rahman et al., "A family of CMOS analog and mixed signal circuits in SiC for high temperature electronics," in *Proc. IEEE Aerosp. Conf.*, Mar. 2015, pp. 1–10.

[9] A. Rahman et al., "High temperature data converters in silicon carbide CMOS," *IEEE Trans. Electron Devices*, vol. 64, no. 4, pp. 1426–1432, Apr. 2017.

[10] J. Mo et al., "A highly linear temperature sensor operating up to 600 °C in a 4H-SiC CMOS technology," *IEEE Electron Device Lett.*, vol. 44, no. 6, pp. 995–998, Jun. 2023.

[11] J. Romijn et al., "Integrated digital and analog circuit blocks in a scalable silicon carbide CMOS technology," *IEEE Trans. Electron Devices*, vol. 69, no. 1, pp. 4–10, Jan. 2022.

[12] T. Dinh et al., "Thermoresistance of p-type 4H–SiC integrated MEMS devices for high-temperature sensing," *Adv. Eng. Mater.*, vol. 21, no. 3, Mar. 2019, Art. no. 1801049.

[13] C.-H. Weng, C.-K. Wu, and T.-H. Lin, "A CMOS thermistor-embedded continuous-time delta-sigma temperature sensor with a resolution FoM of 0.65 pJ °c^2," *IEEE J. Solid-State Circuits*, vol. 50, no. 11, pp. 2491–2500, Nov. 2015.

[14] Y. Negoro, T. Kimoto, H. Matsunami, F. Schmid, and G. Pensl, "Electrical activation of high-concentration aluminum implanted in 4H-SiC," *J. Appl. Phys.*, vol. 96, no. 9, pp. 4916–4922, Nov. 2004.

[15] M. Berthou, P. Godignon, and J. Millán, "Monolithically integrated temperature sensor in silicon carbide power MOSFETs," *IEEE Trans. Power Electron.*, vol. 29, no. 9, pp. 4970–4977, Sep. 2014.

[16] T. Takase, M. Sakaino, Y. Sun, and T. Miyasato, "Measurement of ionization energies of nitrogen in 4H-SiC by traveling-wave method," *Jpn. J. Appl. Phys.*, vol. 52, no. 9R, Sep. 2013, Art. no. 091301.

[17] T. Kimoto and J. A. Cooper, *Fundamentals of Silicon Carbide Technology: Growth, Characterization, Devices and Applications*. Hoboken, NJ, USA: Wiley, 2014.

[18] S. Liu, X. Cheng, R. Pan, X. Liu, L. Zheng, and Y. Yu, "A method to improve the specific contact resistance of 4H-SiC ohmic contact through increasing the ratio of sp^2-carbon," *Appl. Phys. Lett.*, vol. 117, no. 2, Jul. 2020, Art. no. 023503.

[19] T. Abi-Tannous et al., "A study on the temperature of ohmic contact to p-type SiC based on Ti_3SiC_2 phase," *IEEE Trans. Electron Devices*, vol. 63, no. 6, pp. 2462–2468, Jun. 2016.

[20] L. Middelburg, W. van Driel, and G. Zhang, "From Si towards SiC technology for harsh environment sensing," in *Sensor Systems Simulations: From Concept to Solution*. Switzerland: Springer, 2020, pp. 1–15.

[21] B. J. Baliga, *Wide Bandgap Semiconductor Power Devices: Materials, Physics, Design, and Applications*. Sawston, U.K.: Woodhead, 2018.

[22] T. Ayalew, "SiC semiconductor devices technology, modeling and simulation," Ph.D. thesis, Inst. Microelectron., Technische Universität Wien, Vienna, Austria, 2004.

[23] N. Donato and F. Udrea, "Static and dynamic effects of the incomplete ionization in superjunction devices," *IEEE Trans. Electron Devices*, vol. 65, no. 10, pp. 4469–4475, Oct. 2018.

[24] J. Pernot, S. Contreras, and J. Camassel, "Electrical transport properties of aluminum-implanted 4H–SiC," *J. Appl. Phys.*, vol. 98, no. 2, Jul. 2005, Art. no. 023706.

[25] A. Koizumi, J. Suda, and T. Kimoto, "Temperature and doping dependencies of electrical properties in Al-doped 4H-SiC epitaxial layers," *J. Appl. Phys.*, vol. 106, no. 1, Jul. 2009, Art. no. 013716.

[26] H. Matsuura et al., "Dependence of acceptor levels and hole mobility on acceptor density and temperature in Al-doped p-type 4H-SiC epilayers," *J. Appl. Phys.*, vol. 96, no. 5, pp. 2708–2715, Sep. 2004.

[27] C. Darmody and N. Goldsman, "Incomplete ionization in aluminum-doped 4H-silicon carbide," *J. Appl. Phys.*, vol. 126, no. 14, Oct. 2019, Art. no. 145701.

[28] N. S. Saks, A. V. Suvorov, and D. C. Capell, "High temperature high-dose implantation of aluminum in 4H-SiC," *Appl. Phys. Lett.*, vol. 84, no. 25, pp. 5195–5197, Jun. 2004.

[29] A. Hidaka et al., "Comparison of temperature-dependent resistivity of heavily Al- and N-codoped 4H-SiC grown by physical vapor transport and heavily al-doped 4H-SiC grown by chemical vapor deposition," *Jpn. J. Appl. Phys.*, vol. 62, no. 10, Oct. 2023, Art. no. 101001.

[30] S. M. Sze, Y. Li, and K. K. Ng, *Physics of Semiconductor Devices*. Hoboken, NJ, USA: Wiley, 2021.

[31] S. Harada et al., "Temperature dependences of channel mobility and threshold voltage in 4H- and 6H-SiC MOSFETs," *MRS Online Proc. Library*, vol. 640, no. 1, p. 37, 2000.

[32] S. L. Rumyantsev et al., "Channel mobility and on-resistance of vertical double implanted 4H-SiC MOSFETs at elevated temperatures," *Semicond. Sci. Technol.*, vol. 24, no. 7, Jul. 2009, Art. no. 075011.

[33] X. Chi, K. Tachiki, K. Mikami, M. Kaneko, and T. Kimoto, "Different temperature dependence of mobility in n- and p-channel 4H-SiC MOSFETs," *Jpn. J. Appl. Phys.*, vol. 62, no. 11, Nov. 2023, Art. no. 110906.

[34] J. Mo et al., "An analog to digital converter in a SiC CMOS technology for high-temperature applications," *Appl. Phys. Lett.*, vol. 124, no. 15, 2024, Art. no. 152105.

[35] F. Udrea, S. Santra, and J. W. Gardner, "CMOS temperature sensors—Concepts, state-of-the-art and prospects," in *Proc. Int. Semiconductor Conf.*, vol. 1, 2008, pp. 31–40.

[36] J. Altet, W. Claeys, S. Dilhaire, and A. Rubio, "Dynamic surface temperature measurements in ICs," *Proc. IEEE*, vol. 94, no. 8, pp. 1519–1533, Aug. 2006.

[37] X. Jiang et al., "Online junction temperature measurement for SiC MOSFET based on dynamic threshold voltage extraction," *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 3757–3768, Apr. 2021.

[38] S. L. Rumyantsev et al., "Si-like low-frequency noise characteristics of 4H-SiC MOSFETs," *Semicond. Sci. Technol.*, vol. 26, no. 8, Aug. 2011, Art. no. 085015.

[39] H. Yano, T. Hirao, T. Kimoto, and H. Matsunami, "A cause for highly improved channel mobility of 4H-SiC metal–oxide–semiconductor field-effect transistors on the (11$\bar{2}$0) face," *Appl. Phys. Lett.*, vol. 78, no. 3, pp. 374–376, Jan. 2001.

[40] W. Wondrak, R. Held, E. Niemann, and U. Schmid, "SiC devices for advanced power and high-temperature applications," *IEEE Trans. Ind. Electron.*, vol. 48, no. 2, pp. 307–308, Apr. 2001.

[41] A. May, M. Rommel, A. Abbasi, and T. Erlbacher, "Threshold voltage adjustment on 4H-SiC MOSFETs using P-doped polysilicon as a gate material," *Key Eng. Mater.*, vol. 947, pp. 57–62, May 2023.

[42] M. Du, J. Xin, H. Wang, Z. Ouyang, and K. Wei, "Estimating junction temperature of SiC MOSFET using its drain current during turn-on transient," *IEEE Trans. Electron Devices*, vol. 67, no. 5, pp. 1911–1918, May 2020.