DESIGN OF A DIGITAL CONTROLLED OSCILLATOR FOR BLUETOOTH BLE/EDR COMBO WITH HIGH TOLERANCE TOWARDS AM-FM INTERFERENCE

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This is to certify that the report entitled **"Design of a Digital Controlled Oscillator for Bluetooth BLE/EDR combo with high tolerance towards AM-FM interference."** submitted by **Jelle Wilhelmus van der Pas** to the Delft University of Technology in partial fulfilment of the requirements for the award of the Degree of Master of Science in Electrical Engineering is a bonafide record of the project work carried out by him under our guidance and supervision. This report in any form has not been submitted to any other University or Institute for any purpose.

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ABSTRACT

As technology is scaling down by reducing the lateral and vertical dimensions of transistors. It becomes necessary to reduce the supply voltage, enhancing lower power dissipation and to maintain device reliability. This scaling makes the digitally controlled oscillator (DCO) more susceptible to interference between systems on the chip (SoC). For instance, the coupling from the power amplifier(PA) leads to injection pulling of the DCO. Especially in the non-constant envelope modulation schemes, e.g. $\pi/4$-DQPSK and DQPSK, the frequency pulling is extremely troublesome causing severe disrupted output spectrum. Now that Bluetooth provides, besides the Bluetooth Basic Rate(BR) also Enhanced Data Rate (EDR) and Bluetooth Low Energy (BLE) a radio with multiple purposes becomes more complex. Especially in the case where EDR uses $\pi/4$-DQPSK or DQPSK and the BLE only GFSK modulation. Therefore in this thesis a dual frequency DCO at 4.8GHz and 9.6GHz is designed to mitigate the coupling issues with the PA. It also includes a study in AM-FM, where an optimal amplitude of oscillation shows minimal variation of frequency. An overall low power is maintained at 1V supply and a current of 308μA and 765μA for BLE and EDR respectively. Moreover, the thesis shows an attempt to leave out the Low Dropout Regulator to address future scaling challenges ahead. The DCO is simulated in 22nm-FDSOI occupying a core area of 0.0543 mm^2 and achieves a Phase Noise of -116 dBc/Hz after dividing the frequencies 5.06 GHz and 10.74 GHz into the 2.4 GHz band.

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Chapter 1

Introduction

1.1 Bluetooth

Bluetooth has been known for decades as the standard in short-range communication technology, with an expected 6 billion device shipments in 2024 [1]. It has become the standard because of the flexible and adaptive wireless technology that streams data in the 2.4 GHz unlicensed industrial, scientific, and medical (ISM) frequency band. Communication is diverse for all sorts of needs with its various modes such as the Bluetooth Classic with Enhanced Data Rate (EDR) or the Low Energy (LE) mode. Take, for example, the market of hearable products that account for more than 20% of the 6 billion Bluetooth shipments [2]. Bluetooth Classic is mainly used for audio, where the Bluetooth LE (BLE) mode can do all the other work that has to be done in wireless audio, such as pairing, media control, and tracking earbuds. Even in the newest Core specification 5.4 [3], high-precision measurements can be performed in BLE with the new channel-sounding link. These functionalities on these chips are expected to enable a whole new market, for example, where audio transmitters can broadcast to an unlimited number of receivers [2]. In the research shown in [2], the chip vendors aim for a dual-mode solution with EDR plus BLE in the upcoming years. This maintains vendors' market share in wireless audio while facilitating all the upcoming features BLE provides. In addition, manufacturing a chip with both modes available will not limit their product to one specific solution.
EDR uses the $\pi/4$-DQPSK or DPSK modulation scheme, achieving a data rate of 2Mbs and 3Mbs, respectively. The BLE mode uses a GFSK modulation scheme achieving 1Mbs. 2Mbs is optional at very close ranges. This means that EDR is required to perform Amplitude Modulation(AM), while BLE only performs frequency modulation. The different specifications between EDR and BLE are given in table 1.1. It is important to note that both modes can use a maximum transmission power P_{out} of 20dBm. However, the BLE is designed for low-power operation [1], especially as the Internet of Things (IoT) has been setting foot on the ground. Therefore, this thesis assumes a P_{out} of 10 dBm and 0 dBm for EDR and BLE, respectively. A different Bit Error Rate (BER) is also specified with a different modulation scheme, resulting in a different performance requirement. Although both modes allow a receiver to have a -70 dBm sensitivity, realistic designs take a safe margin to take into account non-idealities that deteriorate the BER [4].

These functionalities must be incorporated across all current devices, such as phones, headphones, and speakers, as well as emerging IoT devices. Bluetooth achieves these enhancements via improved communi-

Feature	EDR	BLE
Frequency band	ISM band with range of 2.4000GHz to 2.4835GHz	
Targeted Output Power	10 dBm	4 dBm
Channels	79	37
Channel bandwidth	1MHz	2MHz
Modulation	$\pi/4\,DQPSK, 8\,DPSK$	GFSK
Data rate	2,3Mbs	1Mbs(2Mbs*)
Bit error rate (BER)	0.01%	0.1%
Receiver sensitivity	$\leq -70dBm$	
Maximum frequency drift during transmission	$\pm 10kHz$	$\pm 50kHz$
In-band SI** ($\geq$ 3MHz)	-40dB	-27dB
Out-band blocker (3MHz)***	-27dBm	-35dBm
Network topology	Point-to-point	Point-to-point Broadcast Mesh
Applications	Headphones/speakers/watches	Headphones/speakers/watches Location tracking/Navigation Long range communication Broadcast audio

*The optional data rate 2Mbs can achieved by doubling the symbol rate.
*The Signal to Interfernce(SI) ratio inside the ISM band.
***Maximum Interfering power level 3 MHz outside the ISM band.

Table 1.1: Comparison between EDR and BLE conducted from [3] .

cation protocols and, more critically, through scaling in chip design while preserving its energy efficiency. The key challenges for these small devices are battery life and signal interference. Although moving to finer technology nodes creates computational benefits, the analog part of the chip becomes the bottleneck.

1.2 Technology scaling and process

The integrated chip industry must allow the hardware to meet the expected BLE features. With such a growing need, radio designers and researchers are challenged to find new ways to facilitate the ever-growing systems such as Bluetooth.

Modern processes enable great integration of digital circuits as devices get smaller, reducing power consumption and creating smaller parasitic capacitance. The thinner the gate length in CMOS process, the larger the unity gain frequency f_T becomes, which provides faster switching capabilities [5]. Yet, for the Radio Frequency (RF) analog end, the small processes of CMOS have their limitations. While the f_T increases, its intrinsic gain A_o degrades severely [6], making amplification at the RF front end more difficult. Moreover, the excess noise factor γ increases with the finer CMOS technologies, meaning more thermal noise is created [7]. Furthermore, with short-channel devices, the current leakage becomes more and more of an issue. There is a subthreshold leakage, where the transistor still burns current when turned OFF. To increase the current driving capability of transistors, the vertical dimensions, such as the thickness of the oxide, are scaled with the gate length. However, when the oxide becomes too small, the small-channel devices will encounter the

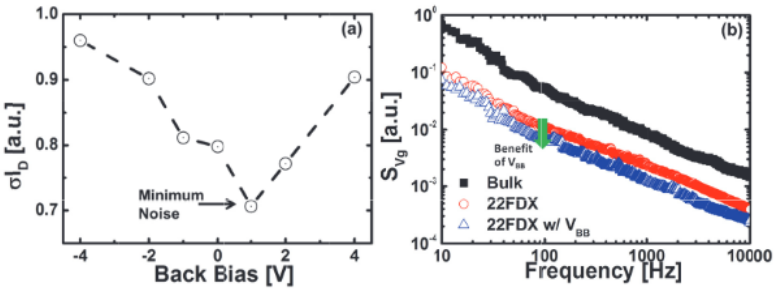


Figure 1.1: (a) Drain current standard deviation σI_d. (b) Gate bias power spectrum S_{Vg} of 22FDX and 28nm bulk devices. Conducted from [9]

gate-tunneling leakage [8].

Therefore to improve leakage current a Full-Depletion Silicon on Insulator (FD-SOI) process can be used [9]. This process technology isolates the channel, causing less leakage to the bulk. Because of this insulator the FD-SOI can improve its performance by forward back biasing (FBB). In contrast, the short channel effect is improved by reverse back biasing (RBB) the substrate [10]. Figure 1.1 shows that the current deviation can be set to minimal noise performance when back-gate biasing is applied. This is because the free carriers are pushed towards the middle of the silicon channel. It also shows a lower gate power spectrum S_{V_g} at low frequencies because of its carrier distribution. This makes FD-SOI significantly better for low voltage low power applications as it creates less low-frequency noise for a given transconductance g_m at lower drain currents [11]. In this thesis, the Global Foundries (GF) 22FDX® FD-SOI process node will be used to maximize its RF performance and the additional possibilities of tuning the transistor in both NMOS and PMOS by FBB/RBB.

However, even in 22FDX®, the minimum gate length of 22nm is designed to operate at a maximum 0.8-V supply voltage to maintain its functionality. For higher voltages, extra thick oxide devices can be used for higher voltage operations, but this degrades performance for RF design. Yet operating at this 0.8-V supply means that RF design is limited with the voltage headroom where the RF signals can operate in [12].

Therefore, to continue to maintain the demanding performance in Bluetooth chips, more and more analog RF design is supported with digital computational power in ways such as on-chip calibration and nonlinear trimming [13, 14, 15].

1.3 Transceivers in Bluetooth

To enhance easy integration with Bluetooth and smaller devices, it is preferred to create a complete SoC that can be directly interfaced with an antenna. Therefore, a fully integrated transceiver is preferred. This includes the receiver (RX), transmitter (TX), and frequency synthesizer(LO). It also includes RF matching and its TX/RX switching happening on the same die. The state-of-the-art transceivers will therefore always

trade-off their power consumption with area and number of external components to achieve the desired performance.

1.3.1 RX

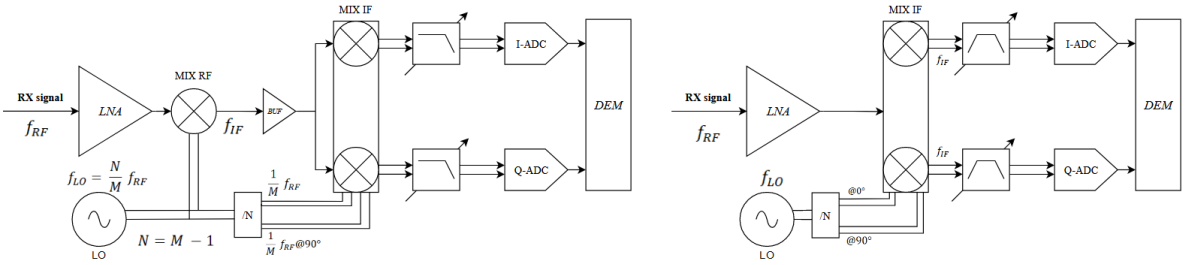


Figure 1.2: Receiver with the sliding- and low- IF architectures shown in left and right respectively.

The RX normally consists of a low-noise amplifier(LNA) followed by 1,2, or 3 mixers, depending on the RX architecture. After the RF signal is downconverted, it is extensively filtered, and the analog-to-digital converter (ADC) converts the signal to the digital domain. The choice for direct downconversion, whereby the incoming signal is directly mixed with the same frequency, is only seen in a few state-of-the-art transceivers since it conventionally suffers from even harmonics, DC offset, and flicker noise, although implementation is simple. However, in these RX single channel structures [16, 17, 18, 19], phase tracking loops, as figure 1.3, are designed. It converts the analog I/Q to a digital phase and loops back to track this phase by adjusting the LO accordingly. This solves the self-corruption and its DC offset problem. This proves to be a useful RX low-power method, although, for an EDR and BLE combination where both frequency and amplitude modulation are expected, the phase-tracking RX is not enough

However, a clear choice of using a sliding- or low- *intermediate frequency*(LIF/SIF) design at the RX part is not set. Initially, it said that the SIF RX as in figure 1.2 is lower in power because it does not need quadrature generation from the high-frequency LO, where high-frequency LO is assumed to be more power-consuming because it is set at twice the signal frequency f_{RX} as in [20]. In [20], a high-volume production transceiver is published where low-power mixers are achieved using charge-reusing mixers. In more recent work [21, 22, 23], a low IF RX is still proven to have low power with 3.6, 2.3, and 1.6 mW, respectively. [21] solves the IQ mismatch problem by adding dynamic latches controlled by the signal whose phase is 90 deg ahead. In addition, it added a tunable RF matching for various antennas. [22] gained very low power because it removed the two ADC and the Q-channel, resulting in a one-channel modulation, illustrated in figure 1.4. [23] shows a very low supply of 0.5V operation but at the cost of 1.9mm^2 of the RF core area compared to 0.59mm^2 of [21]. The major advantage of these LIF architectures is that they have less susceptibility to out-of-band blockers compared to the SIF.

Although the sliding IF has no image problem from an adjacent channel, it does suffer from the susceptibility of out-of-band blockers. This can be seen in [25], where the LNA cannot filter the image frequency.

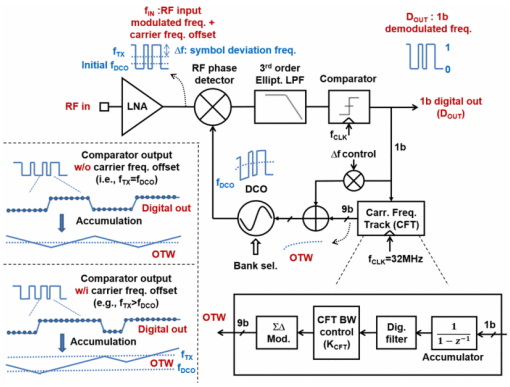


Figure 1.3: Zero-IF with phase tracking. Conducted from [18]

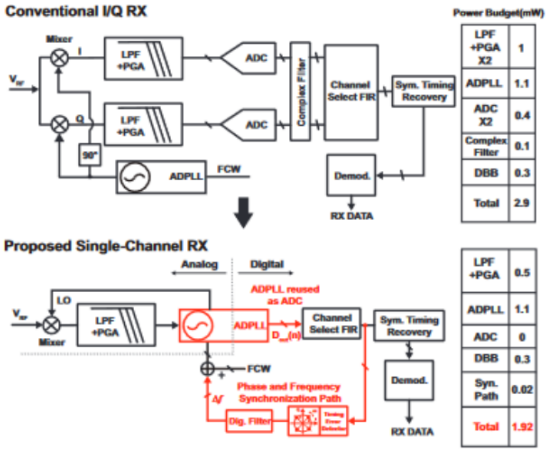


Figure 1.4: Low-IF with hybrid loop. Conducted from [24]

Adding an RF notch filter at this exact frequency allows the image to be blocked better [26]. This comes at the cost of extra area, while the low-IF [20] still shows a significantly better (20dB) out-of-band blocking.

We also need to focus on the demanding dual mode principle in RX. Recent work [27] shows, in low-IF, that the passive mixer and LNA are swapped to relax the power consumption of the LNA. Moreover, it shows two LO generations. One at the $2f_{RX}$ for high power mode and the other at $2/3f_{RX}$ for low power mode (BLE). In this way the overall power in BLE can be guaranteed as a low power LO is guaranteed. Which, on the downside, still requires filtering for a synthesizer operating at $2/3f_{RX}$. Unfortunately, it also requires double the area as each LO is designed separately.

A phase-tracking and sliding IF combination is shown in [28], where amplitude fluctuations and frequency offsets in the mixer are compensated by a phase-to-digital converter with feedback. And because of this converter, the digital baseband complexity and power are reduced significantly. However, it still seems to lack an improvement in the blocker rejection.

However, the high IF provides a new perspective on this problem. Where LIF mainly consists of the variable gain amplifiers and complex bandpass filters (BPF), in [29] shows that discrete-time (DT) operation provides many advantages. In short, the DT current-sharing BPF provides only one spectrum peak compared to traditional RC and complex N-path filters, making it free from replicas. By the high sampling frequency and two additional cascoding filters (DT-CS-BPF), with a lower sampling frequency, the blocker level is significantly improved compared to the other BLE SIF RX discussed above.

1.3.2 TX

In BLE, the TX part in transceivers facilitates direct modulation with a phase-locked loop (PLL) connected to a power amplifier (PA) that is usually designed for high efficiency and low harmonic distortion. In almost all state-of-the-art designs, high efficiency is achieved by using the class-D PA. Yet, to tackle the second harmonic distortion (HD2), almost all require additional calibration circuits, such as DC replicas in [26]. [29] tops the efficiency by applying a class E/F2 PA. Demanding for a higher modulation, as for EDR, the

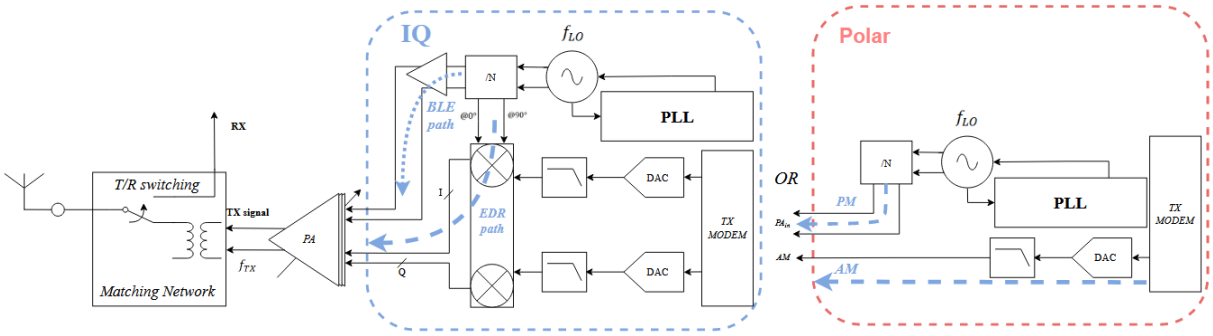


Figure 1.5: Transmitter with IQ mixer and polar on the left and right respectively for 8-DPSK modulation

transceivers apply a more linear PA such as class AB in [30] and push-pull class AB [31], where HD2 of -58 dBc is achieved without calibration. Moreover, the matching network connected to the antenna decides how much of its nonlinear output power will be transmitted. A balun is often used to facilitate transmission with the best match between the PA and the antenna. Additional filtering at the RF output can facilitate HD2 suppression, creating a class-F PA [22].

More importantly, to facilitate EDR, the TX needs more than frequency modulation, as described in most low-power BLE transceivers. It also needs envelope modulation. [32] and [31] propose a transmitter with IQ mixer as described in figure 1.5(blue). This approach to creating more than a two-point constellation is very power-hungry. A more suitable approach is the polar transmitter. Where the amplitude is controlled by the modem as in figure 1.5(red). One way of facilitating this amplitude control is to control the supply of the PA. However, this requires a high bandwidth supply regulator to meet the spectral mask [30]. Therefore, the most used envelope modulation is achieved by creating digitally modulated PA (DPA), which consists of a driver amplifier and an array of tuneable amplifiers.

1.3.3 PLL

For direct frequency modulation, the modulating data is injected into two points of a PLL. The phase frequency detector(PFD) in conventional PLLs creates a pulse when the reference frequency and phase are shifted with respect to the divided f_{LO} and ϕ_{LO}. The charge pump (CP) aims to determine the linear output relation of these PFD pulses. With a capacitor at its output, these generated charges after the low pass filter(LPF) generate a controlled voltage, which then changes the voltage-controlled oscillator (VCO), resulting in a change in f_{LO}. The feedback is then done by the divider to provide stability. The analog PLLs, shown in figure 1.6(blue), are known to be fractional-N PLLs as a multiple modulus divider is used to create finer tuning [33]. These fractional-N PLL are controlled with the $\Sigma\Delta$ modulator [34] to overcome fractional spurs, and quantization noise is set to higher frequencies so that the LPF can filter it out in a later stage.
To overcome the trade-off between its loop bandwidth and gain, spur cancellation schemes can be added [35], where in [36], a digital cancellation is used.

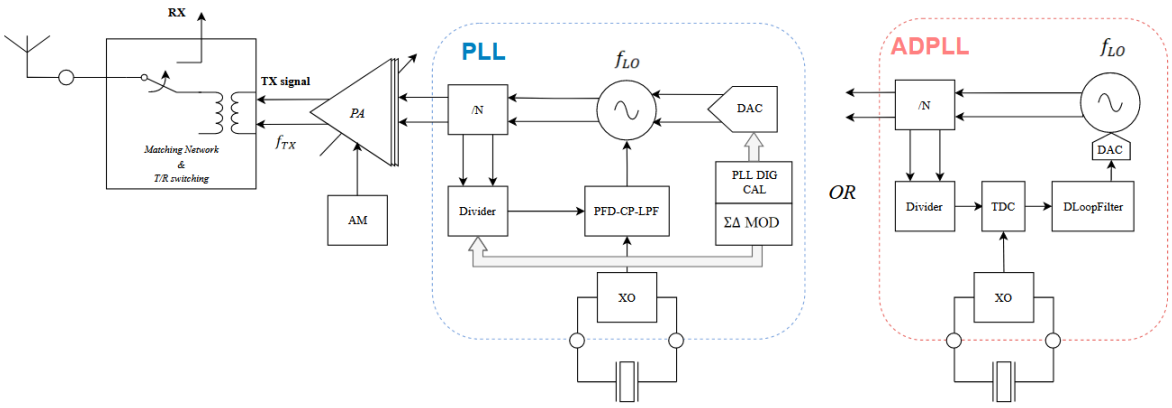


Figure 1.6: transmitter with direct frequency modulation created by the analog PLL or all digital PLL.

More recent designs are All Digital PLL (ADPLL) consisting of a time-to-digital converter (TDC) that creates a digital phase error from the time difference between the reference (XO) and the variable clocks. The digital loop filter (implemented in the discrete domain) integrates the frequency error signal to compute a word to the DAC of the oscillator. The digital loop filter has less current leakage compared to a conventional charge pump at a reduced area. Moreover, the TDC power consumption and resolution scale with the technology [29]. Several TDC implementations are shown in [37].

The easiest way to control a conventional LC oscillator is to use a DAC, as is drawn in figure 1.6(red). To improve the resolution of setting the correct f_{LO}, $\Sigma\Delta$ dithering is used [38]. An illustration is given in figure 1.7. It splits the input (word) into high- and lower-order bits. The $\Sigma\Delta$ modulator creates a dithering stream where its average is the fractional part of the fixed input.

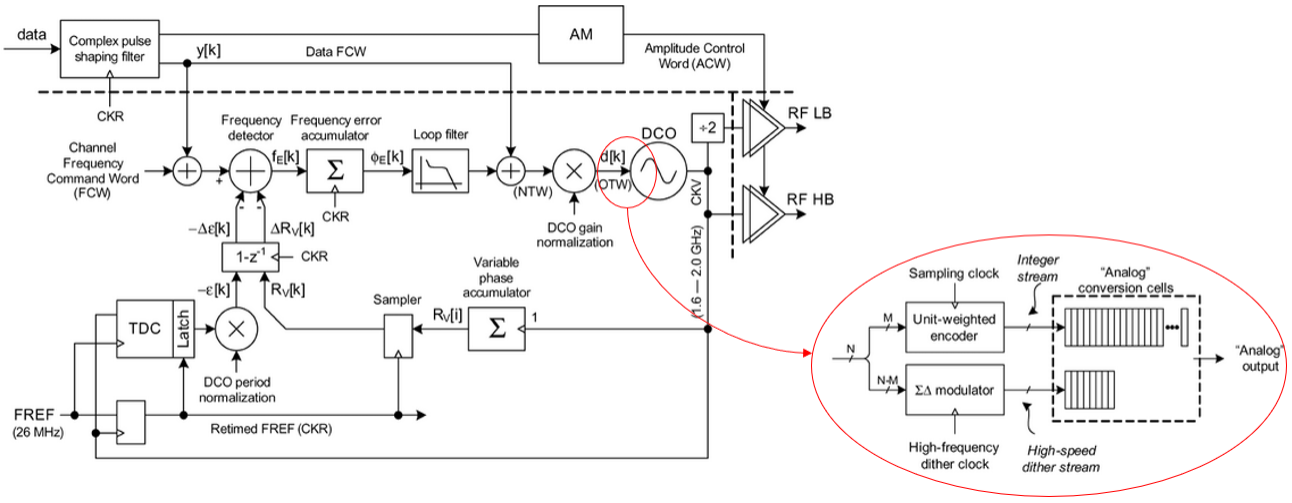


Figure 1.7: Polar transmitter based on ADPLL with described DAC for the DCO [38]

With the elimination of analog tuning in the ADPLL, the only remaining analog elements in a transceiver

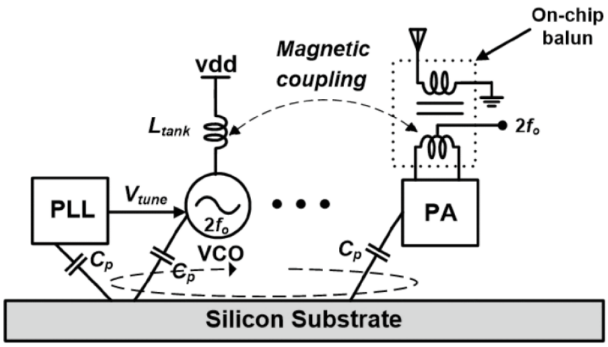


Figure 1.8: Illustration of oscillator pulling in transceivers [43].

include the PA with filters, and the matching network connecting the antenna to the TX/RX. These elements being closer to each other introduces obstacles to further integrating the transceiver.

1.4 SoC bottlenecks

Technology scaling enables more digital back- and foreground calibration for almost all RF components. Full integration devices are in demand more than ever, and the RF components start to interfere with each other. The RF signal enters the antenna, and all its signals are processed on the same small die. During each process, non-ideal harmonics and mixing signals make the SoC devices become their own antagonist, known as self-interference. With a higher complexity SoC, various paths of the created interference need to be considered [39, 40, 41]

However, these interferences are only identified in the post-silicon stage and, therefore, can increase the time to market [42]. With more digital processing power, software-based solutions are more viable. An example is described in [13], which uses a high-level control in which each RF component can be tuned to set its system to optimal operating conditions.

The most studied self-interference is between the DCO and the PA (Figure 1.8). This self-interference problem is commonly addressed with the PA as the aggressor and the DCO as the victim, which are closely placed with each other. Where the aggressor signal has various paths to interfere with the victim. These different couplings can be distinguished as follows [39]

1. electrically through the common substrate;
2. magnetically between the on-chip inductors;
3. magnetically through the bonding wires of both circuits;
4. capacitively between the traces of both circuits.

Where the first two are set to be the most dominant ones [44]. These coupling paths are closely related to the floor planning of each RF block and the manner of protection.
Over the years few adaptive techniques and mitigations of the pulling mechanisms have been applied [45,

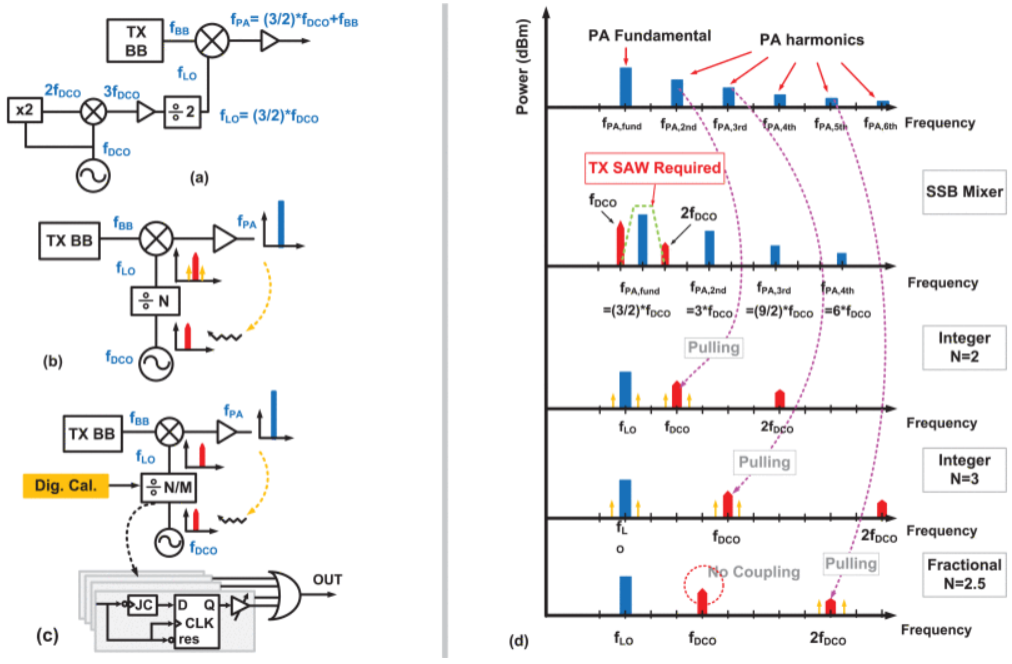


Figure 1.9: Convential synthesizers ideas: (a) SSB mixer [50], (b) Integer divider, (c) Fractional divider [51].

46, 47, 48, 49]. [45] proposes a correction voltage at the LO by using a built-in detection mechanism of the pulling from where calibrations can automatically correct the pulling. [46] also shows that in addition to phase noise, the pulling can also be improved with self-injection signals. This self-injected signal is created by feedback with a phase shifter, delay line, and a programmable amplifier. [47] shows a high abstract algorithm to estimate compensation factors to create its necessary compensation signals.

[48] uses two dither-assisted pulling mitigations by applying a Least Mean Square (LMS) loop for the reference interference and the DCO-PA. [49] shows that adding a calibrated delay improves the oscillator pulling and, thus, BER. [43] applies only phase compensation when the PLL is out of lock and tries to adjust the current in the charge pump stage until locking is achieved again. Although proven very useful mitigation, these transceiver designs sum up to highly complex calibration and algorithmic schemes in the digital domain, creating significant overhead. A more fundamental approach is to change the operating frequency of the DCO with respect to the desired TX frequency. This can alleviate this well-known self-interfere. The normal frequency synthesizer has a divider of 2 (N = 2). But operating even at twice the operating frequency ($f_{LO} = 2f_{TX}$) creates pulling by the second harmonic of the high-power PA. The illustration of the conventional pulling mitigation for the synthesizer is shown in figure 1.9, Where the f_{LO} is generated below the $f_{TX/RX}$ and still suffering from image problems and requiring excessive filtering (i.e., SAW filter) [50]. With a conventional integer N divider, pulling is still created by the Nth harmonic of the PA. The most recent work focused on the use of fractional dividers of the frequency synthesizers are [51, 52]. [51], applies instead of an integer divider, a 2.5 divider consisting of 6 latches and a duty-cyle corrector controlled by an output voltage of an Op-Amp. [52], uses a multi-modulus fractional divider with a successive approximation algorithm for calibration. Besides being quite power-hungry dividers, the spur

reduction effect by this divider is only really useful at high TX output powers (> 12dBm). Furthermore, suppression inductor traps are also shown in [53, 54]. These focus on creating shorts of the f_{LO} frequency at the supply and ground of the PA.

1.5 Aim and scope

As frequency pulling is the most studied self-interference in RF SoC and the LO still shows its limit in the PLL noise performance, which also depends on the loop bandwidth, its design still plays an important role. The $\pi/4$-DQPSK and 8-DPSK in EDR mode apply amplitude modulations that cause significantly more frequency pulling of LO than in the BLE mode where no amplitude modulation scheme is applied. Therefore, the thesis aims to decrease pulling effects in the EDR mode while maintaining low power operation in the BLE mode. The thesis concentrates only on the design of the DCO and not on the already proven pulling effects. Provided that the DCO is operating in a classic low-IF transceiver [20]. The TX-part uses two different PAs for each BLE/EDR mode. With an aim for different output power $P_{TX} = 4\,\text{dBm}$ and 10 dBm for BLE and EDR, respectively. Also, the power consumption for each mode is different, where the BLE PA can consume not more than 10mA, and the EDR PA has to facilitate amplitude modulation, consuming between 40mA and 80mA. This sets the DCO current consumption in BLE more stringent than for the EDR

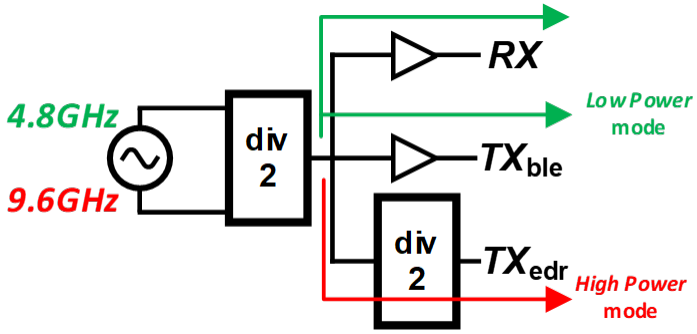


Figure 1.10: The implementations of a dual-mode design with an additional divider

mode.

For that reason, the DCO will use two frequency modes, as illustrated in figure 1.10. In one frequency band, the non-linearity effects from the PA will be significantly reduced, while in the second frequency band, less operation power is required. By following the BER and in-band blocker requirements of EDR from table 1.1, the phase noise requirement will be set for both EDR and BLE:

$$\mathcal{L}(\Delta\omega) = P_{signal} - P_{blocker}(\Delta\omega) - SNR - 10\log(BW) \tag{1.1}$$

Assume a state-of-the-art RX sensitivity of -90 dBm and a blocker of -40 dBm at a 3.5 MHz offset, ideal SNR of 14 dB for BER 0.01% [55] with channel bandwidth of 1 MHz results in phase noise minimum of -124 dBc/Hz. In the BLE, the same phase noise is aimed at reducing current consumption, which is a prerequisite.

Within the DCO design, susceptibility phenomena will be addressed, and the goal is to design the DCO to be robust from unwanted injected currents. A tuning range between 2.208 and 2.678 GHz ($TR = 19.5\%$) is aimed to guarantee Process, Voltage, and Temperature(PVT) variations.
This means that besides aiming for low phase noise at minimum power consumption, the optimum points of operation for amplitude and supply changes are also investigated. As the scope is limited to only the DCO design, full integration of the frequency synthesizer remains off, and more focus will be on assessing whether a dual-mode DCO is worth implementing in future ADPLLs.

1.6 Thesis organisation

In Chapter 2, the fundamentals of LC oscillators will be shown, including noise analysis. In addition, state-of-the-art dual frequency mode designs will be discussed to understand various methods of application. A small study on the capacitance of the cross-coupled devices and its effect on optimal phase noise performance and amplitude sensitivity for low-power oscillators is delivered. In Chapter 3, the proposed DCO design is shown in detail, and in Chapter 4 an attempt is also made to improve the supply robustness. Chapter 5 concludes the design and its performance and discusses future work.

Chapter 2

Oscillator fundamentals

The chapter covers the general theory of LC oscillators. Considering the broad spectrum of topologies to discuss, the thesis will be limited to only the class B topology. The other topologies, such as Colpitts,class-C/D/F, and switching current source, will be briefly summarised and referenced to show that their main functionalities have been studied. Moreover a literature study on the different approaches of dual mode oscillator will be provided to understand the limitations of state-of-the-art dual mode designs. Several dual-mode principles will be analysed that form a foundation of the proposed design later on. Furthermore, the study of active devices in class B topology will be addressed, where their parasitic capacitance plays a crucial role in frequency sensitivity over amplitude and phase noise performance at low power.

2.1 Oscillation theory & performance

The frequency synthesizer LO, both used in RX and TX, consists of a VCO or DCO depending on the analog and digital control of the PLL. This crucial component consists of an LC tank, where ideally a continuous exchange of energy between L and C is preserved. The tank impedance with losses is illustrated in figure 2.1 and can be described as

$$Z_{tank} = \frac{j\omega L R_p}{(1-\omega^2 LC)R_p + j\omega L}, \tag{2.1}$$

Where it peaks at the parallel losses of the tank R_p at the oscillation frequency of

$$\omega_{L0} = \frac{1}{\sqrt{LC}}. \tag{2.2}$$

The losses need to be compensated with a negative resistance. According to the Barkenhausen criteria, a loop gain of 1 and a phase shift around the loop of 0 (or 2π) must be maintained. The actual compensating resistance comes from the transconductance G_m of the active devices. To initiate oscillation in the LC tank, it is necessary that

$$G_m \cdot R_p \geq 1 \tag{2.3}$$

To assess the performance of an oscillator, the phase noise (PN) is defined as the single sideband power

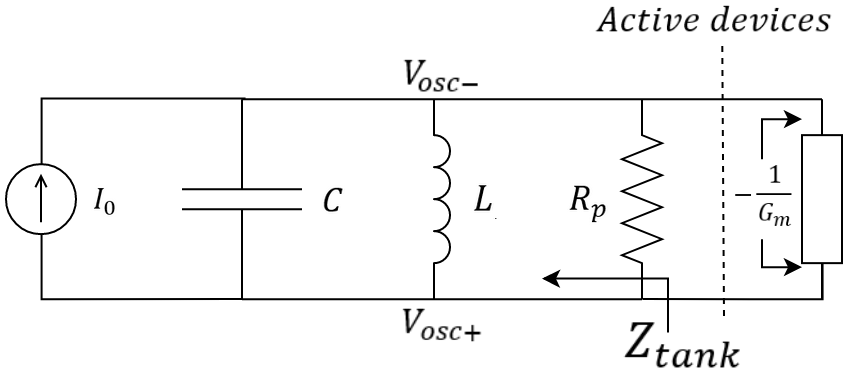


Figure 2.1: LC tank with R_p losses compensated by positive feedback by the active devices.

at a frequency offset $\Delta\omega$ from ω_{LO} with a bandwidth of 1 Hz:

$$\mathcal{L}(\omega) = 10\log\left(\frac{0.5\overline{v_n^2}}{0.5V_{osc}^2}\right)[\text{dBc/Hz}] \tag{2.4}$$

With V_{osc} as the differential oscillation amplitude and the spectral density of the mean square noise voltage can be described as

$$\frac{\overline{v_n^2}}{\Delta\omega} = |Z_{tank}|^2 \cdot \frac{\overline{i_n^2}}{\Delta\omega}, \tag{2.5}$$

The quality factor of the tank is mostly determined by the inductor $Q = R_p/(\omega L)$. Considering where for $\Delta\omega << \omega_0$, the impedance of the LC tank in figure 2.1 can be approximated as:

$$|Z_{tank}(\omega_{L0} + \Delta\omega)|^2 \simeq \left(\frac{\omega_{LO}R_t}{2Q\Delta\omega}\right)^2 \tag{2.6}$$

And the spectral density of the mean square noise current of the LC tank

$$\frac{\overline{i_n^2}}{\Delta\omega} = \frac{4k_BT}{R_p}, \tag{2.7}$$

where k_B is the Boltzmann's constant and T temperature. Combining (2.7), (2.6) in (2.5) can already describe the PN as

$$\mathcal{L}(\Delta\omega) = 10\log\left[\frac{4k_BTR_p}{V_{osc}^2} \cdot \left(\frac{\omega_{LO}}{2Q\Delta\omega}\right)^2\right] \tag{2.8}$$

From this, it can be seen that the PN improves with increased oscillation amplitude V_{osc} and quality factor Q, which are roughly determined by power consumption and area, respectively.

Yet up till now, only losses of the tank are assumed, where actually the active devices and the current sources also add noise. Moreover equation (2.8) does not take into account the noise floor that will be reached when $\Delta\omega$ is far enough from ω_{LO}. And more importantly the flicker noise of the different sources is

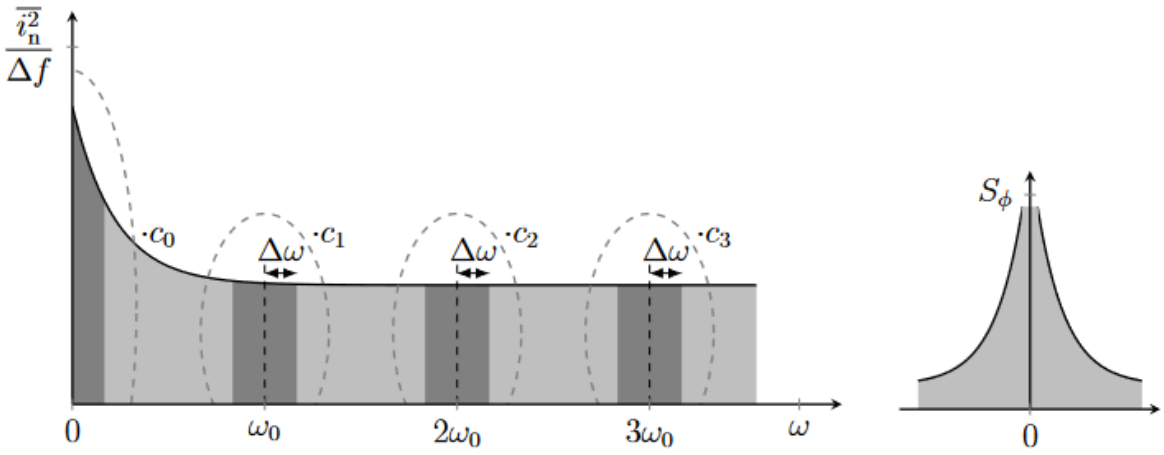


Figure 2.2: Noise folding principle from [57]

not taken into account. The mean square flicker noise has an actually inverse relation with ω:

$$\frac{\overline{i_{n\ 1/f}^2}}{\Delta\omega} \propto \omega^{-1},$$

compared to equation (2.7), giving rise to an additional region $1/f^3$ at lower frequencies. This region reduces with $-30\,dBc/decade$. To fit this region with the $1/f^2$ region, equation (2.8) is rewritten:

$$\mathcal{L}(\Delta\omega) = 10log\left[\frac{4k_BTR_p}{V_{osc}^2}\cdot F\cdot\left\{1+\left(\frac{\omega_{LO}}{2Q\Delta\omega}\right)^2\right\}\left\{1+\frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right\}\right] \tag{2.9}$$

Different from equation (2.8) is the additional noise factor F in $1/f^2$ region for other sources, the first factor is to set the noise floor, and the factor of the second bracket sets the $1/f^3$ region. This PN definition is defined as the Linear Time Invariant (LTI) model or Leeson's model [56].

To take a more accurate model, a Linear Time Variant (LTV) approach is needed which considers the timing of injection of the noise current i_n. Because at the peak of oscillation, the injection noise only changes the amplitude V_{osc}, while at the zero crossing of the oscillation, it only changes the phase ϕ_n. Thus PN is dependent on the moment of the current injection. To describe at which point during oscillation, the system is sensitive to a current injection, an Impulse Sensitivity Function (ISF) is created and can be described in Fourier Series

$$\Gamma(\omega_{LO}\tau) = \frac{c_0}{2} + \sum_{n=1}^{\infty} c_n\cos(n\omega_{L0}\tau + \theta_n), \tag{2.10}$$

where c_n are real coefficients that tell how much of the $\overline{i_n^2}$ is "collected" and adds to the spectrum impurity as illustrated in figure 2.2. θ_n is the relative phase between uncorrelated sources.

The caused phase shift ϕ_n can therefore by superposition integral be seen as

$$\phi_n(t) = \frac{1}{q_{max}} \int_{-\infty}^{t} \Gamma(\omega_{LO}\tau) i(\tau) d\tau \tag{2.11}$$

where the current injections and its harmonics can be represented as

$$i(t) = I_n \cos((n\omega_{LO} + \Delta\omega)t) \tag{2.12}$$

This will eventually give the general phase noise theorem [58]

$$\mathcal{L}(\Delta\omega) = 10 \log \left[\frac{1}{8q_{max}^2 \Delta\omega^2} \frac{\overline{i_n^2}}{\Delta\omega} \sum_{n=0}^{\infty} c_n \right] \tag{2.13}$$

With rewriting $q_{max} = C \cdot V_{osc}$, $C = Q/(\omega_{LO} R_p)$ and with Parseval's relation results in

$$\mathcal{L}(\Delta\omega) = 10 \log \left[\frac{R_p^2}{4Q^2 V_{osc}^2} \left(\frac{\omega_{LO}}{\Delta\omega} \right)^2 \cdot \frac{\overline{i_n^2}}{\Delta\omega} \cdot \frac{1}{2\pi} \int_0^{2\pi} \Gamma(\omega)^2 d\omega \right] \tag{2.14}$$

which represents the phase noise spectrum in $1/f^2$ region. To extend this PN to multiple sources, the noise factor F is added, where each source i has its own mean squared spectral density and ISF:

$$F = \sum_{i=1} \frac{R_p}{2k_B T} \cdot \frac{1}{2\pi} \int_0^{2\pi} \Gamma_i(\omega)^2 i_{n,i}(\omega)^2 d\omega \tag{2.15}$$

and thus results in

$$\mathcal{L}(\Delta\omega) = 10 \log \left[\frac{k_B T R_p}{2Q^2 V_{osc}^2} \cdot F \cdot \left(\frac{\omega_{LO}}{\Delta\omega} \right)^2 \right] \tag{2.16}$$

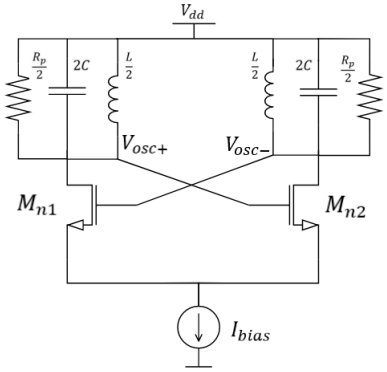
So consider only the LC tank with an ideal oscillation $\cos(\omega_{LO} t)$ and losses R_p generates a $\Gamma(\omega t) = -\sin(\omega_{LO} t)$ [58]. And knowing the current noise spectral density $\frac{\overline{i_n^2}}{\Delta\omega} = \frac{4k_B T}{R_p}$ results in a noise factor of

$$F = \frac{R_p}{2k_B T} \cdot \frac{1}{2\pi} \cdot \pi \cdot \frac{4k_B T}{R_p} = 1 \tag{2.17}$$

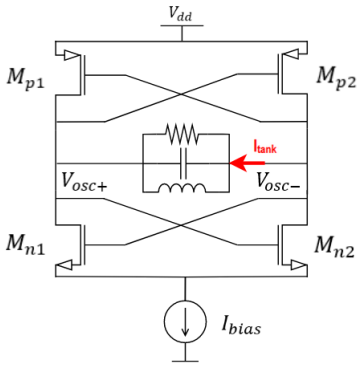
Assessing other noise sources and wave composition different than a $\cos(\omega t)$ relies on the topology employed and the operation of each component.

2.1.1 Class B

The most known method to create the negative resistance is to create a cross-coupled pair of NMOS devices (figure 2.3a) or by taking its complementary form (CMOS) with NMOS and PMOS devices (figure 2.3b). Indeed, at least two transistors are needed to facilitate the $0\,\text{deg}(360\,\text{deg})$ phase shift as a single transistor



(a) NMOS only topology



(b) NMOS and PMOS topology

Figure 2.3

only shifts 180 deg from gate to drain. Its transconductance in time can be described as

$$G_m(t) = \begin{cases} \dfrac{g_{mn1}(t)g_{mn2}(t)}{g_{mn1}(t)+g_{mn2}(t)} & \text{for NMOS only} \\ \dfrac{g_{mn1}(t)g_{mn2}(t)}{g_{mn1}(t)+g_{mn2}(t)} + \dfrac{g_{mp1}(t)g_{mp2}(t)}{g_{mp1}(t)+g_{mp2}(t)} & \text{for CMOS} \end{cases} \tag{2.18}$$

But also these devices contain small losses $G_{ds}(t)$ that counteract the negative $G_m(t)$:

$$G_{ds}(t) = \begin{cases} \dfrac{g_{dsn1}(t)g_{dsn2}(t)}{g_{dsn1}(t)+g_{dsn2}(t)} & \text{for NMOS only} \\ \dfrac{g_{dsn1}(t)g_{dsn2}(t)}{g_{dsn1}(t)+g_{dsn2}(t)} + \dfrac{g_{dsp1}(t)g_{dsp2}(t)}{g_{dsp1}(t)+g_{dsp2}(t)} & \text{for CMOS} \end{cases} \tag{2.19}$$

Where to preserve oscillation

$$G_m(t) = -(G_{ds}(t) + \frac{1}{R_p}) \tag{2.20}$$

However, these additional losses at low amplitudes $V_{osc} \leq V_{th}$ are insignificant when the g_m devices do not enter the triode region. It is important to note that these topologies use a common current source at the common node. This is to control oscillation amplitude V_{osc} with the current (current limited) as otherwise being fully dependent on the supply V_{dd} (voltage limited). Using no current source, is a topology called class D [59].

To analyze the topology completely, one needs to understand how each transistor conducts its current with respect to the oscillation voltage applied to its gate and drain. So starting with an arbitrary phase ϕ, the two voltage nodes of the tank can be described as

$$V_{osc+}(\phi) = V_{osc}\sin(\phi), V_{osc-}(\phi) = -V_{osc}\sin(\phi) \tag{2.21}$$

Naming I_1 and I_2 the drain currents of M_{n1} and M_{n2} in the NMOS case only:

$$I_{bias} = I_1(\phi) + I_2(\phi) \begin{cases} I_1(\phi) = \frac{\beta}{2}(V_{osc}|sin(\phi) + V_s(\phi))^2 \\ I_2(\phi) = \frac{\beta}{2}(-V_{osc}|sin(\phi) + V_s(\phi))^2 \end{cases} \tag{2.22}$$

where β is the sum of physical characteristics and because of the ideal square law relation between I_{ds} and V_{gs}, the source voltage V_s can be determined as

$$V_s(\phi) = \sqrt{\frac{I_{bias}}{\beta} - V_{osc}^2 \sin\phi^2} \tag{2.23}$$

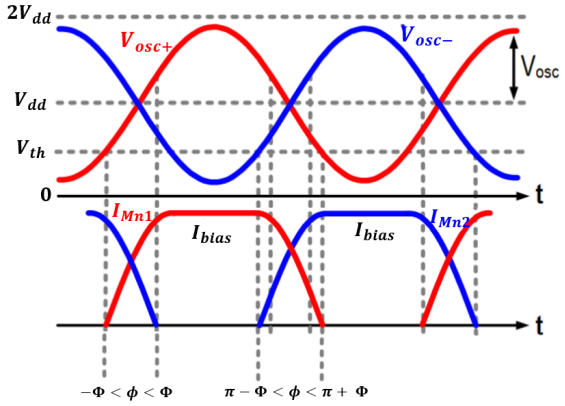
Where by substituting 2.23 back to 2.22 tells that there is a limit angle Φ:

$$\Phi = \arcsin\sqrt{\frac{I_{bias}}{2\beta V_{osc}^2}}, \tag{2.24}$$

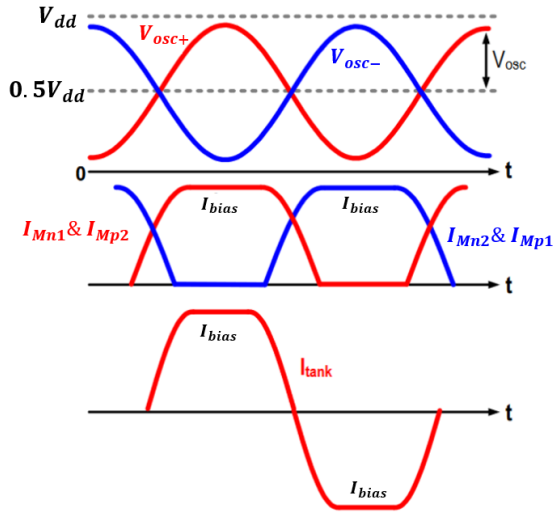
describing two regions for M_{n1} and M_{n2} to be both in saturation

$$-\Phi < \phi < \Phi \text{ or } \pi - \Phi < \phi < \pi + \Phi \tag{2.25}$$

and otherwise one of them is ON and OFF.



(a) NMOS voltage and current waveforms



(b) CMOS voltage ande current waveforms

Figure 2.4

Note that between these limit angles, Φ, the devices are commuting. Where M_{n1} transitions from the triode region to the saturation region, whereas M_{n2} starts conducting in saturation once the gate voltage equals V_{th}. This can be observed in the region $\pi - \Phi < \phi < \pi + \Phi$ in figure 2.4a. Moreover, both devices are charging the tank capacitance at its drain, and due to small voltage variations between these drains,

noise is injected into the LC tank, contributing a noise factor of $F = 1 + \gamma$ [60]. To also include the noise contribution of a non-ideal current source and the effective losses of the devices $G_{ds,eff}$, we have

$$F_{classB} = \begin{cases} (1 + \gamma_n + \frac{1}{2}\gamma_n g_{mn,CS} R_p) \cdot (1 + R_p G_{ds,eff}) \text{ for NMOS only} \\ \\ (1 + \frac{\gamma_n + \gamma_p}{2} + \frac{1}{2}\gamma_{cs} g_{mn,CS} R_p) \cdot (1 + R_p G_{ds,eff}) \text{ for CMOS} \end{cases} . \tag{2.26}$$

The phase noise contribution of the active devices is represented by the excess noise factor γ and is technology-dependent. For the 22nm SOI technology, the long channel noise factor of 2/3 is not valid anymore, based on the GF 22FDX design guide the γ varies up to 3 in these short-channel transistors.

The same mechanism applies to the CMOS class-B oscillator where now the current generated by I_{bias} is used by two devices. Since the tank is fully differential, the current that goes through the tank is twice as efficient as NMOS only. However the maximum oscillation swing $V_{osc,max}$ cannot go above $V_{dd} - V_{ds,CS}$ decreasing its maximum voltage efficiency. In the ideal case, the drain current has a square waveform, whereby using the Fourier expression, the ideal oscillation amplitude can be estimated as

$$V_{osc} = R_p \cdot I_{\omega_o} \begin{cases} \frac{2}{\pi} R_p I_{bias} \text{ for NMOS only} \\ \\ \frac{4}{\pi} R_p I_{bias} \text{ for CMOS} \end{cases} \tag{2.27}$$

However, the current source itself cannot be assumed ideal since it also has limited output impedance and significant capacitance, which results in a low ohmic path that is created from the tank via one of the active devices to the ground, creating extra loss during oscillation. Moreover, the common node must be at least $V_{dsat,CS}$, leaving even less oscillation amplitude for the CMOS topology. That low ohmic path is created when one of the two g_m devices is in triode while the other one is OFF. And since this path goes through a common node the second harmonic will leak into it. In [61], a filtering technique for a class B oscillator is proposed. Creating a high impedance path at this common node by placing an inductor in between the current source and the common node. Which, together with a large capacitor, creates additional filtering of second harmonic noise from the current source. Implementing this requires a lot of area due to the second inductor.

Another idea is to introduce degenerative resistors at the drains of the g_m devices, making the tank less susceptible to the modulation of "on-resistance" of the devices. This only improves the upconverted $1/f^3$ noise, although the thermal noise of the resistors itself does cause worse $1/f^2$ noise. Overall, these ideas are useful for creating fewer losses at higher amplitudes while still improving the PN. However, in low-power applications, operating at maximum oscillation amplitude is not always preferred due to power consumption.

2.1.2 Other topologies

Focusing on the local oscillator, the supply is provided on the chip with a 1V DC-DC converter, where an additional Low Dropout regulator(LDO) is used to provide a clean 0.8V supply. Deviating from these values is therefore not assumed. Therefore, a practical class-D topology [59, 57] creates a too-high output swing resulting in oxide breakdown. Moreover, the use of a voltage-dependent topology makes the design rather susceptible to corners and PVT variations. Furthermore the design cannot be tuned such that it operates at optimal performance. Moreover, this supply in real Soc is layered close to other subblocks, so any coupling to the DCO supply will result in common mode variations if the output of the DCO (V_{osc+}, V_{osc-}) is supply biased. This makes a complementary design almost a predetermined choice. Besides the double current efficiency, it can provide more robustness against supply. Besides, aiming for a low amplitude $V_{osc} \approx 400mV$ offers better PN for CMOS structures compared to NMOS only for the same current consumption [62]. With a 1V/0.8V supply this means a complementary will easily suffice the maximum obtainable amplitude.

Different types of Colpitts designs have shown to be great options as it is very current efficient, but they lose tuning range because of the capacitor feedback [63]. Furthermore, its lack of transconductance g_m to start oscillation has been tackled by creating different G_m-boosted Colpitts [64, 65, 66, 67].

Biasing the gate to a lower voltage than the drain and adding a large capacitance allows the class-C to improve PN at higher amplitudes, This because the devices will generate a more pulse-shaped current and does not leave saturation when $V_{osc} > V_{th}$. In a standard LC oscillator, when $V_{osc} > V_{th}$, the devices enter triode region, creating a high conductance G_{ds} for that part of the oscillation. Which temporarily loads the LC tank and thus degrades the PN performance [68, 69]. However, the theoretical 3.9dB PN improvement with the additional power consumption of biasing the gates, the feedback circuitry [70, 71] and self-biasing circuits [72, 73, 74] will not trade-off against the current efficient CMOS structure. Almost all class C biasing schemes need (adaptive) biasing to start up oscillation.

This is also the case with switching current sources, which in [75] is being biased below the threshold voltage. Switching current sources causes less additional noise caused by the current source [76, 77, 78] or it lets the noise circulate [79]. The start-up is not always guaranteed, where in [80] amplitude control feedback was required.

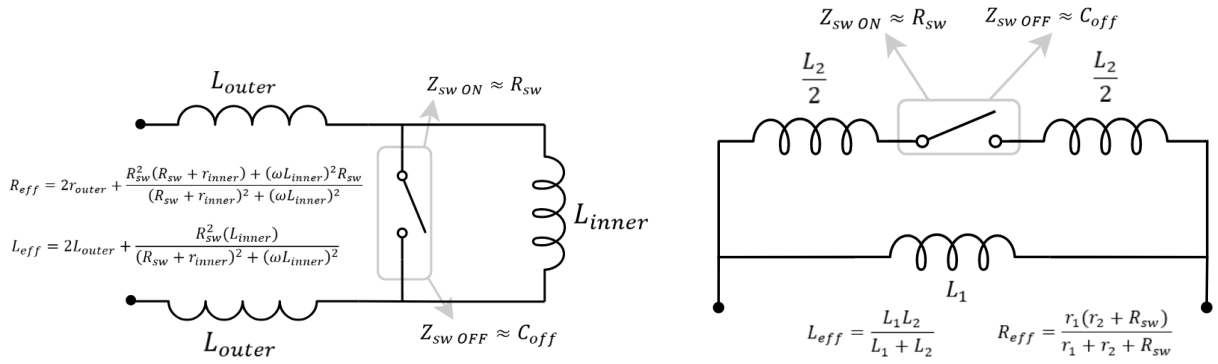
For state-of-the-art phase noise performance, class F tackles to minimize the ISF [7, 81]. It generates currents at the 2nd and/or 3rd harmonic referred to as class-F2 and class-F3 oscillators [81, 82]. Recent works [83, 84] show inverse class F designs achieving slightly worse phase noise but are lower in power compared to class-F2/F3. However, the class-F literature shows that the area required for implementation is significant, although designs with decent low current have been demonstrated, $I_{DC} = 700\mu$A at $0.018mm^2$ [85].
Consequently, for the rest of the thesis, a complementary class B will be used at a minimal oscillation amplitude that still meets the PN performance. Furthermore, class B can also use the large capacitance to improve PN as shown in [68], which is also subject to loss and quality of the tank.

2.2 Dual-Mode tank desgin

This section will focus more on the implementation of the tank. Where in general oscillation theory only in class-F a real variation of the LC tank is needed to achieve its PN performance. Yet, to narrow more on the BLE and EDR application, one might be interested to see how with a dual mode tank where on one hand limited current consumption is given while in the other robustness against interference is the main goal. Therefore a summary of state-of-the-art dual mode designs will be provided to conclude on a well thought implementation in Chapter 3.

The dual mode principal is normally used to extend the tuning range (TR) of the oscillator(or as class-F). This is not only necessary to facilitate wide bandwidth for the channels to transmit or receive but also to overcome the change in center frequency of the device over PVT and corners. Where in conventional (low-IF) synthesizers the DCO operate at $2f_{PA}$. One might consider to extend the integer divider illustrated in figure 1.9 to $f_{LO} = N \cdot f_{PA}$. However operating at higher frequency normally asks for even more power. Therefore an interesting design would be if the DCO can operate in two frequency bands where by the EDR mode would be the in higher mode as the PA harmonics is lower at the higher frequency band [51]. Various methods to alternate betweeen the low (LB) and high frequency band(HB) are showed here.

2.2.1 Switched inductor



(a) Serie Inductors, with parallel switch.

(b) Parrallel Inductors, with serie switch.

Figure 2.5

Whereas normally the capacitors are used to tune because of their high Q factor at low frequencies with low area occupation and really fine tuning capabilities. For switching modes from higher band (HB) to lower band (LB) such as going from 9.6GHz to 4.8GHz, capacitor switching would diminish the impedance and thus increase the power required for the same oscillation amplitude. Therefore the simplest solution would be to implement inductor switching. The problem is that the series resistance R_{sw} and its capacitance C_{sw} cause severe degradation. This because the dominant Q_L is affected.

$$Q_L = \frac{\omega_{LO} L}{r_s + R_{sw}} \tag{2.28}$$

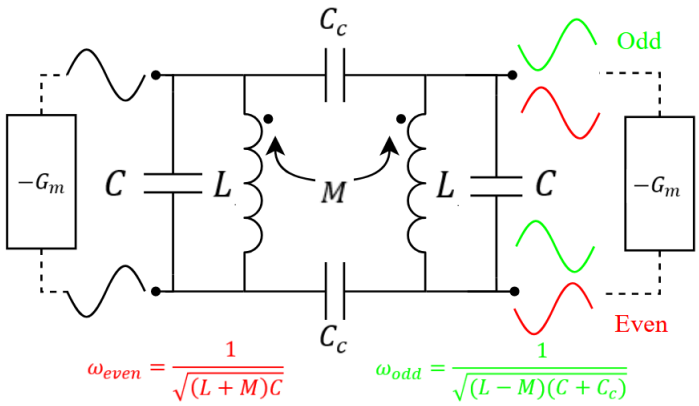


Figure 2.6: Coupling of two identical tanks via C_c and M

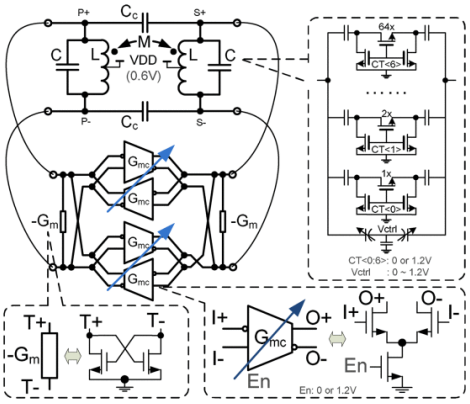
Where in high Q inductors the switch becomes the dominant loss of the LC tank. The C_{sw} is mostly a bottleneck for the TR when it is turned OFF and will add capacitance to the tank. In [86, 87] a switch in parallel with the inner winding of an inductor L_{inner} is used. This means the switch conducts when aiming for maximal inductance and thus for the lower band. The R_{sw} increases power consumption in LB, which has a low power constrain (BLE). In its HB the effective inductance L_{eff} would not consider the losses of the switch and therefore would result in maximal Q_L. Which is all vice versa of what is aimed for in this thesis.

In [88] the extra inductance with switch is taken in parallel to overcome this problem. In this case, when the switch is ON, its effective inductance L_{eff} is taken as in figure 2.5b, where if $4L_2 \approx L_1$, $L_{eff} \approx \frac{1}{5}L_1$ making it suitable for high frequencies.

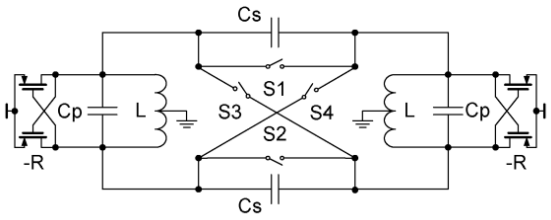
2.2.2 Odd and even mode

To explain the understanding of a two identical LC tank that are electrically C_c and/or magnetically coupled M, two modes are given in figure 2.6. As in one case the phases over C_c are forced to be the same, the system sees C_c as a short, taking its capacitance not into account. Moreover as the current in the inductor are in phase the effective inductance becomes $L + M$ for both inductors. In the second case, the phases over C_c are 180 deg out of phase, meaning the capacitance C_c contributes like a fully differential capacitance. But as the current flow in the inductors is counteracting, the M will lower the effective inductance.

In order to correctly select your mode, extra G_{mc} cells are needed[89]. This to suppress and initiate the unwanted and desired mode. The resonator described in figure 2.7a has two peaks because of the capacitive coupling C_c and mutual coupling M and in order to create the odd(even) mode the right side of the resonator has swapped(same) polarity by connecting the first(last) two G_{mc} such that it will add negative(positive) G_{mc} to left side of the resonator while the other two adds positive(negative) G_{mc} to the right side. This extra add-on ensures that the other mode is not excited. Important to see is that here the aim was to create two equal peaks $R_{p,even}, R_{p,odd}$, while in this thesis a preferable asymmetry must be created as the power limit in the BLE/EDR mode is different. In [90] two $-G_m$ cells with four switches are used. Two switches $G_{e,sw}$



(a) Dual band oscillator with four G_m cells [89]



	S1	S2	S3	S4
Even Mode	On	On	Off	Off
Odd Mode	Off	Off	On	On

(b) Dual band oscillator with four switches [90]

Figure 2.7

are cross-coupled and are ON(OFF) in odd(even)mode, and the other two parallel switches $G_{o,sw}$ work vice versa. Because these switches are only turned ON to add positive G_m to the unwanted side and thus do not reduce the desired peak impedance. Of course, how well the suppressing is depends on the transconductance of the switch. In [91] there are odd and even mode for both the coupling capacitors C_m and the coupling between inductors M. It uses two inductors with each 4-ports that coupled with C_m. This shows how a quad core could be implemented. The switch array similar to [90] is used to dampen the unwanted mode and prevent unwanted oscillation. This means oscillation does not observe losses from R_{sw}.

It should be noted that to optimally make use of the above cases an additional mux with additional buffers are needed to combine the two oscillations output voltages since two $-G_m$ stages are used. In [92, 93, 94] only one $-G_m$ cell and one G_m cell is used. Whereby, creating a positive feedback loop ($-G_m$ cell), the lower frequency band (LB) will initiated. And creating a negative feedback loop(G_m cell) builds oscillation in the high frequency band (HB). This approach is more energy conservative as LB or HB is chosen based on the initiated feedback loop. However, just as in class F, the ratio X is very important to maintain the desired oscillation throughout TR.

2.2.3 Switched Gm devices

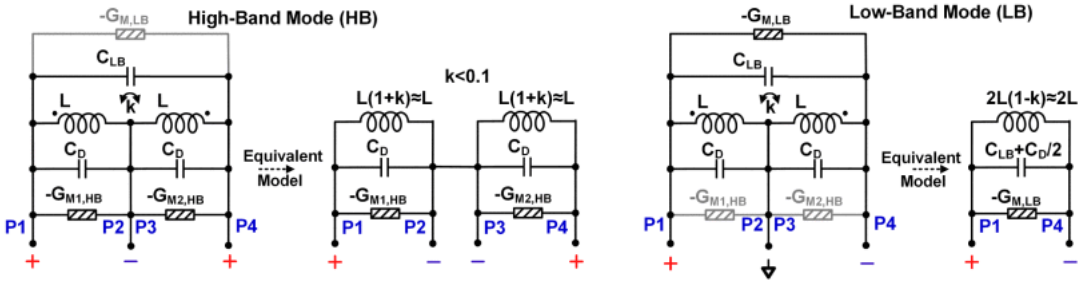


Figure 2.8: (Left) HB mode where two $-G_m$ are activated. (Right) LB mode where one $-G_m$ is activated [95].

To overcome the losses of the switches R_{sw} and to maintain a high impedance peak, changing the $-G_m$ cells might be a solution.
In [95] three $-G_m$ cells are used, with two inductors and two capacitor C_d in series. In LB, both inductors can be considered in serie, $L_{LB} \approx 2L$ and its capacitance $C_{LB} + C_d/2$. In HB, each inductor and capacitor is used by an individual $-G_m$ cell. Generating two oscillators that are connected by a common node. Its illustration is given in figure 2.8. To apply this to low power application, a significant higher inductance is needed. For $f_{LB} \approx 4.8$GHz a $2L \approx [3nH, 4nH]$ would be needed. Technically, the area efficiency is already reduced as the total inductance $2L$ needs to be split up in two L, whereas normally the inductance of an inductor easily doubles when adding one extra outer winding. In other words, more metal is needed for the same $2L$ and thus the not optimal Q will be achieved. Furthermore, [95] uses only one of the two G_m cells in HB as the output oscillation, losing 3dB in PN. The biggest disadvantage is the actual implementation of the three capbanks. In LB mode, both C_d have to be tuned with the same code to facilitate the same oscillation frequency, which thus requires two identical capbanks. In HB mode the C_d accounts only single ended, which can function as fine tuning, but an additional coarse tuning bank is still necessary in C_{LB}.

Four $-G_m$ cells are shown in [96], where each $2-G_m$ cells generate a different path in the asymmetrical 8-shaped inductor and thus generates extra difference between LB and HB as the coupling M between the 8-shaped L_p is swapped. This method of using only $-G_m$ cells instead of positive G_m cells [89] or even and odd switches [90] is advantageous as a guarantee of the right mode is created, where for the other a minimal size G_m of the cell and switches must be created to suppress the unwanted, which could add capacitance or load the LC tank. What is important in this design is that the flow in current in inductor can be changed and thus alter different M and thus different modes. Examples of dual/triple core inductor designs are shown in [97, 98, 99, 100], although their inductance values are not suitable for low power implementations. More switching techniques for LC oscillators can be found [101], but the methods described above describe the common methods to implement a dual-mode LC oscillator.

To conclude on the dual-mode methods, the use of multiple G_m cells and special inductors design show no

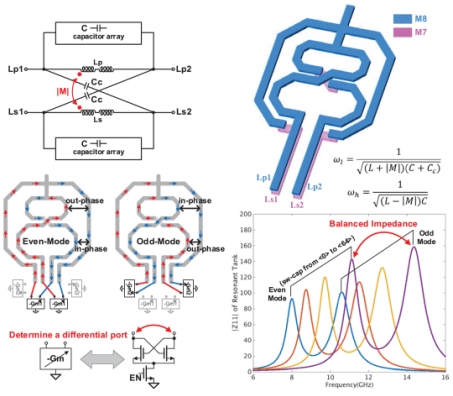


Figure 2.9: (left) Schematic of the resonator with change in current for even and odd mode. (right) Illustration of the inductor with its resulting impedance peaks [96].

losses, yet the efficiency in area and its low value in inductance make a low-power solution not yet applicable. For the even and odd mode, the positive G_m cells require too much power before being useful. Furthermore all these connections to the tank will still charge the LC tank. The method of using four switches looks more suited, but its ask for capacitor divider to ensure the switches do not leak current. Which adds significant capacitance ($\sim 150fF$) to the tank [90]. The simple method to use switched inductor is a guarantee of losses. However, with scaled CMOS, the loss of the switch can be further minimized.

2.3 Active devices and their frequency modulation

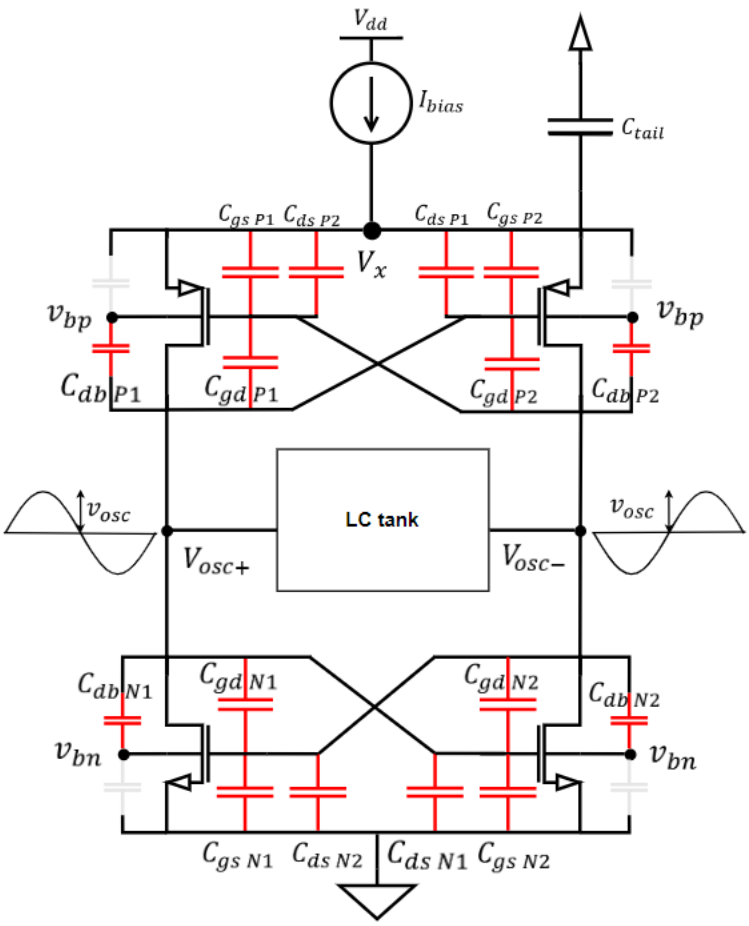


Figure 2.10: CMOS with all the considered parasitic capacitance showed in red.

To minimize current consumption at a supply of 0.8 V, the oscillator is set in the current-limited regime, using a current source. In this study, a class B CMOS topology will be used, to analyse the PN performance at low amplitudes. Moreover, to prevent any interference from affecting the f_{LO}, frequency sensitivity must be minimized. Hence, any variations in amplitude or current must not influence the f_{LO} otherwise the oscillator becomes highly susceptible to noise from e.g. the current source or supply.

To understand the frequency sensitivity over amplitudes, the effects that influence the amplitude modulation(AM) will first be described. This issue may arise due to supply interference, which affects the current generated by the current source. Secondly, this AM will be subject to an up-conversion mechanism that modulates the frequency. A part subset of the non-ideal capacitances within the oscillator will be characterised and proven to be an important factor of this up-conversion. Consequently, active devices will be selected to minimise the sensitivity of AM-FM, which also ensuring low phase noise (PN) at a low amplitude. Additionally, implementing calibration idea to determine the optimal amplitude over PVT.

2.4 AM-FM by non-linear capacitance

As shown in equation (2.27), any fluctuation in I_{bias}, will result in amplitude change ΔV_{osc}. Besides ΔV_{osc} also the common mode voltage in case of class B CMOS topology will be effected [102, 103]. The fluctuations are mostly caused by flicker noise but also supply variations, which will be explored in more detail in Chapter 4. Due to the flicker noise, a PMOS current source is typically implemented as it inherently creates less flicker noise. Any repetitive AM noise (at ω_m) can be described as the noise from the current source being single-balanced mixed by each cross-coupled device resulting in up-conversion to $\omega_{LO}+\omega_m$ [104]. This results a noise-to-carrier ratio defined as

$$\Big(\frac{K_A}{2\omega_m}\Big)^2 \hat{V}_n^2$$

where $\hat{V}_n^2$ is the RMS spectral density of its specific AM output noise and K_A is the sensitivity of amplitude [105].

Various mechanisms of up-conversion to PN are described in the literature, such as the modulation of tail capacitance [104] and the Groszkowski effect [106, 107, 108]. The latter mechanism focuses on the harmonics of the current, which modulates the frequency, and as flicker noise modulates the harmonic composition, it ultimately results in PN at $1/f^3$ region [107]. The AM-FM mechanism is well known when applying non-linear varactors [109, 103, 105]. However, even in a DCO, still nonlinear capacitances are at work [65, 110].

The sensitivity of the frequency with respect to the amplitude can be described as

$$K_A = \frac{\partial \omega_{LO}}{\partial V_{osc}} = \frac{\partial \omega_{LO}}{\partial C_{t\ ,eff}} \frac{\partial C_{t\ ,eff}}{\partial V_{osc}} \tag{2.29}$$

where $\omega_{LO} = \frac{1}{\sqrt{LC_{t,eff}}}$ and $C_{t,eff}$ as effective capacitance. Which is according to [61], described as:

$$C_{t,eff} = C_t[0] - \frac{1}{2} C_t[2] \tag{2.30}$$

Where the $C_t[0]$ and $C_t[2]$ are the Fourier series being the time-averaged and second harmonic components of the total capacitance C_t, where the latter has negligible effect [61], setting

$$C_{t,eff} = C_t = C_{capbank}(t) + C_{par}(t) \tag{2.31}$$

Although $C_{capbank}$ contains switched capacitors, whose parasitics can affect its effective capacitance, for the purposes of this research on active devices, digitally controlled $C_{capbank}$ is considered constant over oscillation time. As illustrated in figure 2.10, the capacitance of the gate-source, gate-drain, drain-source, and drain bulk labeled $C_{gs}, C_{gd}, C_{ds}, C_{db}$ for each device are considered, setting C_{par} as:

$$\begin{aligned} C_{par} = &(\frac{1}{C_{gsN2}} + \frac{1}{C_{gsP1}})^{-1} + (\frac{1}{C_{dsN2}} + \frac{1}{C_{dsP2}})^{-1} + (\frac{1}{C_{dbN2}} + \frac{1}{C_{dbP2}})^{-1} + C_{gdn1+2} \\ &+ (\frac{1}{C_{gsN1}} + \frac{1}{C_{gsP2}})^{-1} + (\frac{1}{C_{dsN1}} + \frac{1}{C_{dsN1}})^{-1} + (\frac{1}{C_{dbN1}} + \frac{1}{C_{dbP1}})^{-1} + C_{gdp1+2} \end{aligned} \tag{2.32}$$

The dominant capacitances C_{gs} and C_{gd} are determined by the following equations:

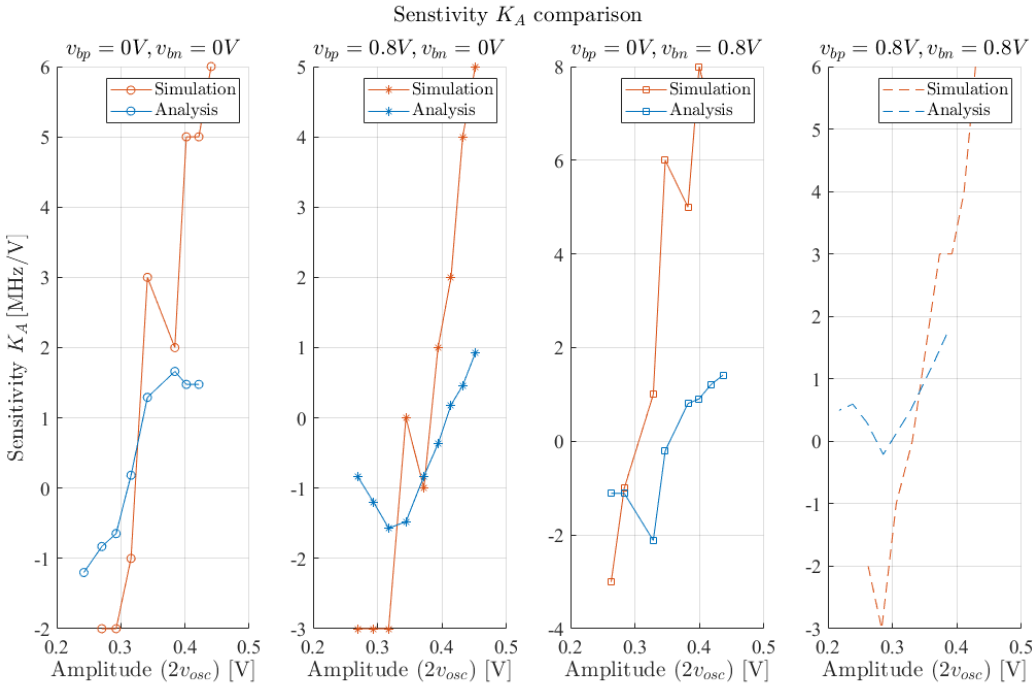


Figure 2.11: Sensitivity K_a as function amplitude for different v_{bp} for PMOS and v_{bn} NMOS.

$$C_{gs} = \begin{cases} WC_{ov}, & \text{if } |V_{gs}| < V_{th} \\ \frac{2}{3}WLC_{ox} + WC_{ov}, & \text{if } 0 \leq |V_{gs}| - |V_{th}| < |V_{ds}| \\ \frac{1}{2}WLC_{ox} + WC_{ov}, & \text{if } 0 \leq |V_{gs}| - |V_{th}| > |V_{ds}| \end{cases} \tag{2.33}$$

$$C_{gd} = \begin{cases} WC_{ov}, & \text{if } |V_{gs}| < V_{th} \\ WC_{ov}, & \text{if } 0 \leq |V_{gs}| - |V_{th}| < |V_{ds}| \\ \frac{1}{2}WLC_{ox} + WC_{ov}, & \text{if } 0 \leq |V_{gs}| - |V_{th}| > |V_{ds}| \end{cases} \tag{2.34}$$

Where the W and L are the width and length of the devices and C_{ox} the gate oxide capacitance that is $27.6[mF/m^2]$ and $23.8[mF/m^2]$ for NMOS and PMOS devices. And C_{ov} is the overlapping gate oxide with the gate and the drain/source. Both equations illustrate that during the oscillation v_{osc} of the gate or drain, the parasitic capacitance changes. Important here is that when $2v_{osc}$ surpasses V_{th}, the C_{gs} starts to decrease instead of increasing. Additionally, C_{gd} begins to rise as the device enters the triode region.

These effects on C_{gs} and C_{gd} will affect the sensitivity analysis. Using (2.31) in (2.29):

$$K_A = -\frac{1}{2}\frac{\omega_{LO}}{C_{t\ ,eff}}\frac{\partial C_{par}}{\partial V_{osc}} \tag{2.35}$$

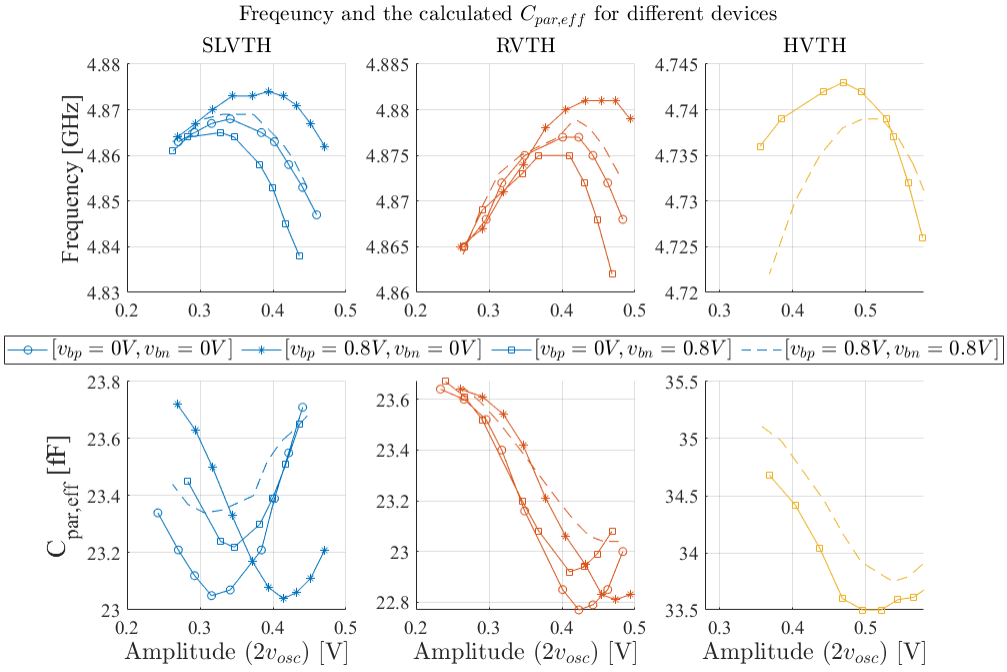


Figure 2.12: Different type of devices with its oscillating frequency at the top and its effective capacitance on the bottom. Different bulk biasing v_{bn}, v_{bp} are simulated over the various amplitudes.

describes that as long as C_{par} remains constant over $V_{osc}(2v_{osc})$, any noise that affects the amplitude, will result in no FM or is not up converted by the non-linear capacitances.
By using the whole equation (2.32) and simulate the parasitics of the CMOS structuture over various amplitudes, an comparison between the $\frac{\partial \omega_{LO}}{\partial V_{osc}}$ and equation (2.35) can be made. Results for various v_{bn} and v_{bp} are shown in figure 2.11.
The simulations used an EMX inductor model of $L = 3.9\,\text{nH}$ with $Q_L = 16.5$ and an ideal capacitor bank with $C_{capbank} = 238\,\text{fF}$ with $Q_c = 50$.

The analysed values show less sensitivity than the simulated ω_{LO} over V_{osc}. A possible reason is disclosed in section 2.4.2, although, both lines cross the zero sensitivity close to the same amplitude. Observe how for $v_{bp} = 0.8V, v_{bn} = 0V$ the zero-crossing is at maximum amplitude. This occurs as the bulk-source voltage V_{bs} increases for both PMOS and NMOS devices. Where the V_{bs} and V_{th} relation is characterized by

$$V_{th} = V_{th0} + \gamma\left(\sqrt{|-V_{bs} + 2\phi_F|} - \sqrt{|2\phi_F|}\right) \tag{2.36}$$

with V_{th0} is the zero substrate threshold, γ the body factor and ϕ_F the Fermi potential. When applying 0.8 V to the bulk to only one of the two devices, only a slight increase of the zero-crossing is observed.

The sensitivity functions show that the zero-crossing is related to the V_{th}. The figure 2.11 used Super-Low-VTH(SLVTH) devices in where the $V_{th} \approx 0.3\,\text{V}$ and can be tuned by the v_{bp} and v_{bn}. When operating

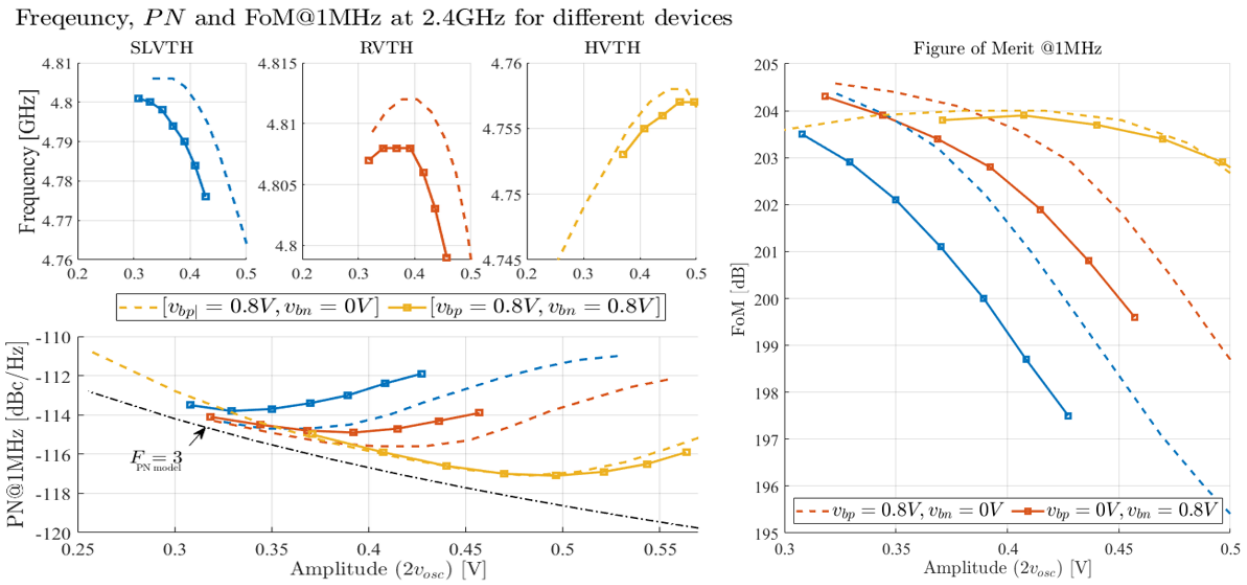


Figure 2.13: Frequency and phase noise results over amplitude on the left and on the right its resulting FoM. For the LTV PN model (equation (2.9)) an $R_p = 1490\Omega$ and $F = 3$ are chosen.

the DCO at this V_{th} oscillation amplitude, the noise-to-carrier ratio should be minimised [104].

2.4.1 Different devices and its effect on PN

The V_{th} has showed to be the amplitude where $K_A = 0$ and thus shows minimal frequency variation. This implies that the PN performance at this amplitude will also be positively impacted. Furthermore, the analysis can be extended by using higher V_{th} devices. In 22nm FDX process, besides the option to apply backgate biasing also Regular-VTH(RVTH) and High-VTH(HVTH) are options. The frequency and $C_{par,eff}$ over amplitude for each device are given in figure 2.12.

It should be noted that in the case of the HVTH devices, its sizing had to be increased to start oscillation and thus also more parasitic capacitance are created.

The simulated frequency shows that sensitivity is minimal at the V_{th} oscillation amplitude. And as the RVTH and HVTH have a higher V_{th} the optimal oscillation amplitude $V_{osc\ opt}$ is set higher. Moreover the RVTH and HVTH devices are less prone to current leakage as the SLVTH.

To actually prove that higher V_{th} devices can be useful, the PN and the Figure of Merit(FoM) are given in figure 2.13 for each device type. The FoM is given as

$$FoM = |PN| + 20\log\left(\frac{\omega_{LO}}{\Delta\omega}\right) - 10\log\left(\frac{I_{bias}V_{dd}}{1mW}\right) \tag{2.37}$$

Again, the EMX inductor model with the same capacitance is used. Observe how the FoM is higher for a wider range of amplitudes when using HVTH devices. The SLVTH is limited to small amplitudes. This is because the PN decreases with amplitude as demonstrated with Leeson's model (equation (2.9)). However, this reduction ceases once the devices reach the triode region, causing a PN penalty, as discussed in Chapter 2.1.2.

Normally, one prefers to use the minimum amount of width $W_{n1,2}$ for the active devices [111]. The overkill of g_{mn} and g_{mp} can slightly increase the amplitude, but it simultaneously reduces the common source node V_x and the DC level of the output nodes $V_{osc+,-}$. The effect on PN and the DC level of the output nodes are shown in figure 2.14. The observed degradation of 4 dB in PN at maximum amplitude is due to the devices operating within the triode region. Scaling $W_{n1,2}$, will therefore result in an increase g_{ds} in the triode region, thus forming a lower resistance path. This path allows the current source to add noise to the LC tank.

This is substantiated by the noise summary in table 2.1. The table shows at the highest amplitude the noise contributions of the cross-coupled devices and the current source. Where the cross-coupled devices stay almost the same but the current source noise contribution increases significantly. This makes scaling the devices an important design choice between a guaranteed start-up and PN performance.

Sizing	Spotnoise @1MHz [fV^2]					
	Thermal noise			Flicker noise		
	M_{p1+p2}	M_{n1+n2}	M_{cs}	M_{p1+p2}	M_{n1+n2}	M_{cs}
W	204	245	501	39	70	152
$4W$	269	296	1679	27	53	960

Table 2.1: The noise contributions of each device at 0.5 amplitude swing for different sizing. $W_{p1,2}/W_{n1,2} = 2.6$

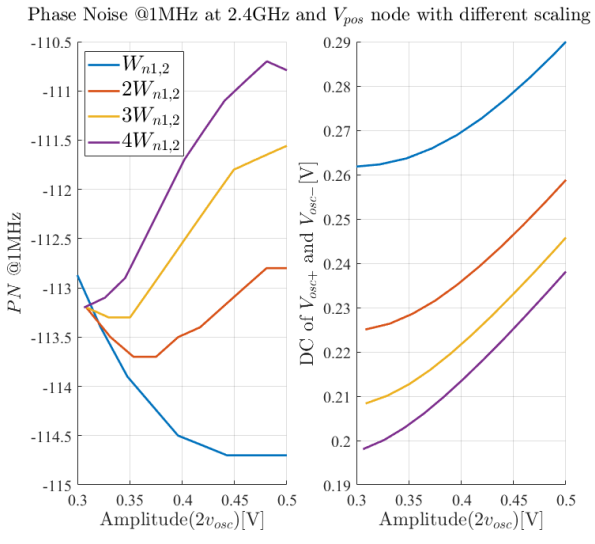


Figure 2.14: PN performance over various for different multiplication factors. $W_{p1,2}/W_{n1,2} = 2.6$

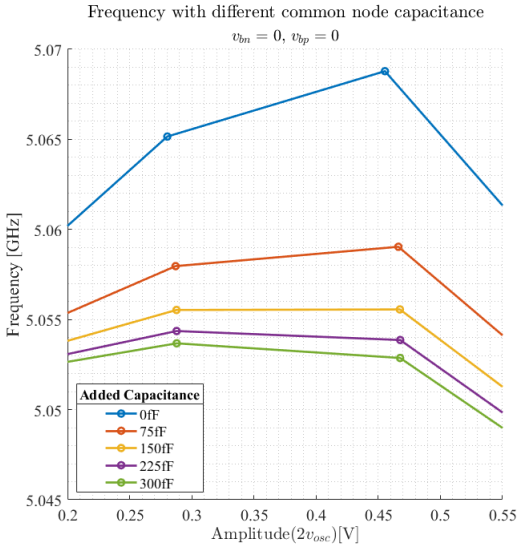


Figure 2.15: Oscillation frequency for various added common node capacitance C_{tail}

2.4.2 Common node capacitance

To elaborate further on the mismatch of K_A from figure 2.11, the capacitance contributions of the common node,V_x also influence the effective capacitance. The common node capacitance in figure 2.10 is given

as C_{tail}. This capacitance consists of the gate-drain and drain-source capacitance of the current source. Additional capacitance can be introduced to achieve a current pulse shape as in a class C topology [69]. However, this added capacitance contributes to loading the tank capacitance [112]. Yet in [112] no clear effective contribution is shown. The contribution of the common node capacitance is only described up to an amplitude smaller than V_{th}. At higher amplitudes ($2v_{osc} > V_{th}$), [112] states that the decreasing frequency is caused by the increased harmonic composition of the current (Groszkowski effect [106]) and not by the parasitics of the active devices. When adding different capacitances to the common node as in figure 2.15, shows that the frequency peak shifts to a lower amplitude. However, the flatness of the curve and thus less sensitivity K_A is obtained up to an added capacitance of 225 fF. Consequently, the sensitivity K_A remains low for amplitudes ranging from 0.3 V to 0.45 V when compared to the scenario without C_{tail}. If the capacitance of the common node is accurately considered both before and after $2v_{osc} = V_{th}$, it may enhance the precision of the sensitivity analysis shown in figure 2.11.

2.4.3 Optimal amplitude for AM-FM

To come towards an AM-FM robust oscillator, it has been shown that there is an optimal amplitude $V_{osc\ opt}$ that can cause minimal frequency drift. One can reacon that $V_{osc\ opt} \approx V_{th}$. To guarantee that the DCO will be operating at this optimal AM-FM amplitude,regardless of the change in V_{th}, a simple calibration method can be applied. The DCO uses the closed loop ADPLL that at first will lock at the frequency $f(V_{osc\ min})$ at the $V_{osc\ min}$. Creating n steps in amplitude by a code of bits b_n, the f_{LO} will increase(decrease) with each step. In closed loop, the DCO will increase(decrease) its capacitance with C_{step} to counteract the $+(-)\Delta f_{L0}$. As the C_{step} is digitally controlled, the amount of bits used for this can be easily retrieved. When sweeping all b_n, one will find the maximum step that was needed to bring the frequency down to where it was locked. The biggest positive C_{step} will correspond to the code b_{opt} where the frequency will be highest and where its K_A will be minimal, resulting in the optimal PN at small offsets due to the AM-FM up-conversion. In [113] a similar method is used to calibrate to the optimal amplitude. It should be noted that to further reduce PN at small offsets, the c_0 component of the ISF function (equation (2.10)) should be minimised.

So, even in a complementary form, a mininum in AM-FM is observed. To match V_{thn} and V_{thp}, the backgate biases are set to $v_{bn} = 0\,\text{V}(V_{bs} = 0)$ and $v_{bp} = 0\,\text{V}(V_{bs} \approx 0.6\,\text{V})$. The RVTH devices will be used as it provides the perfect balance between good PN and sufficient TR as too large devices require too much $C_{t\ par}$. Furthermore, the HVTH devices require a minimal supply that almost exceeds 0.8 V [7], meaning that only operating directly to the DC-DC supply is possible. The AM-FM up-conversion is minimized showing robustness against any amplitude modulation at maximal FoM.

Chapter 3

Analysis and design of Dual Mode Switch Oscillator

Building upon the foundational principles of LC oscillators presented in Chapter 2, which includes noise analysis, the effect CMOS cross-coupled devices have on PN and the exploration of state-of-the-art dual-mode designs, this chapter will outline the proposed DCO design that fits the Bluetooth BLE/EDR combo application.

In the BLE/EDR combo transceiver, the use of two separate PAs is used to provide low-power amplification in the BLE mode and envelope modulation in the EDR mode. To maintain low power and easy mitigation between the PA and DCO pulling for BLE and EDR, the DCO will also operate at two frequency modes.

The DCO is used in a low IF transceiver, operating at twice the transmitting and receiving frequency band in the BLE mode. This is done to already prevent any direct coupling with the transmitting and receiving signals. To extend this and thus further reduce interference on the chip, the DCO will be operated at four times the transmitting and receiving frequencies (f_{TX}) in the EDR mode. The illustration of the TX side in the proposed transceiver is given in figure 3.1. The figure shows that an additional divider is required for the EDR path. Yet the coupling between the PA output and the DCO will be inherently lower because of the lower fourth harmonic compared to the second harmonic [114]. A crucial aspect of the TX illustration is the variation in power consumption and output power between BLE and EDR modes. As the BLE mode transmits less power, the consumption of the transceiver and, thus, the oscillator have to be inherently lower

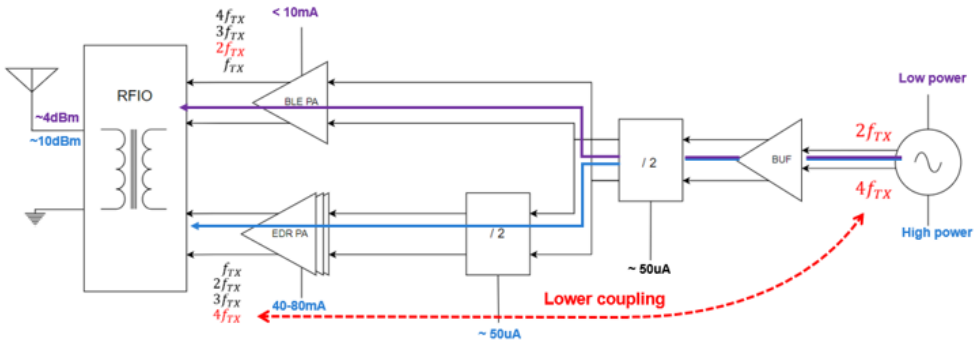


Figure 3.1: Proposed transmitter where the oscillator changes mode with the BLE and EDR mode. A lower coupling between EDR PA and DCO is achieved when operating $f_{LO} = 4f_{TX}$.

compared to the EDR mode.

This chapter provides an estimate of current consumption in BLE mode using the PN requirements outlined in Chapter 1. This estimate, along with the given tuning range of 19.5% for each frequency band is set in section 3.1. Based on that, the development of the dual-mode oscillator design will follow.
This chapter will also discuss the design process of the dual-mode oscillator. An oscillator capable of controlling both frequency modes with low power consumption comes with certain drawbacks. To demonstrate these issues, the chapter begins with an LC tank, highlighting that solely capacitor tuning does not meet the low power requirements in BLE mode. Subsequently, inductor tuning will be introduced. Two approaches to implement inductor tuning will be demonstrated, along with an alternative method involving a magnetically coupled resonator.
Based on analysis of basic inductor tuning and resonator functionality, the proposed tank design will be revealed. Analysis of the proposed design will be provided in Section 3.4. Three distinct inductor layouts will be presented in Section 3.5 to achieve minimal area. Section 3.6 will discuss the design of capacitor tuning for each type of capacitor bank required to overcome PVT variations and tracking the oscillation frequency. In Section 3.7, the performance of the final DCO design will be provided.

3.1 PN and current consumption

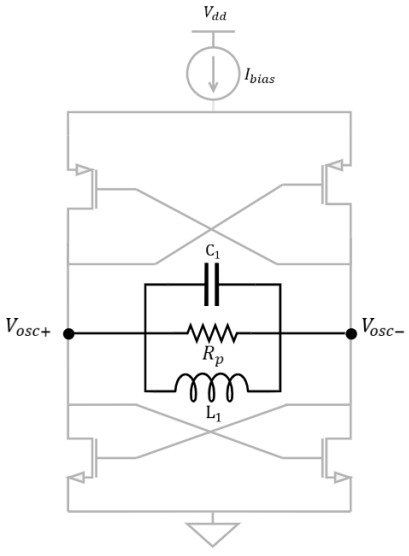


Figure 3.2: The LC tank in CMOS cross-coupled configuration.

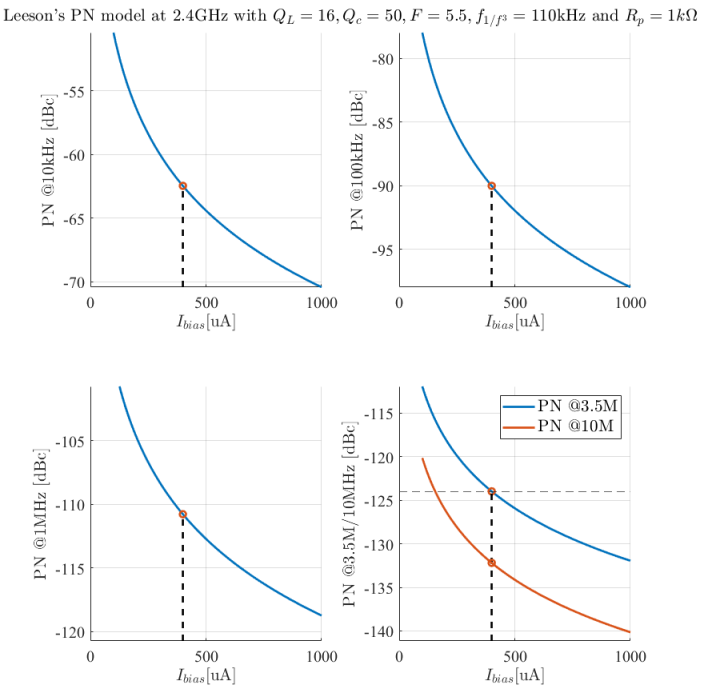


Figure 3.3: Leeson's PN model as a function of I_{bias} based on equation (2.9)

To estimate the current required to achieve the PN requirements given by equation (1.1), both equation

(2.16)(2.9) will be followed. The important design variables in these equations are the parallel losses of the tank R_p, the oscillation amplitude V_{osc}, and the tank quality factor Q_{tank}. These variables can be explained using the cross-coupled CMOS topology and an LC tank, depicted in figure 3.2. The LC tank consists of an inductor L_1 and a capacitor C_1. The current consumption relationship with V_{osc} described in (2.27) states

$$V_{osc} = V_{osc+} - V_{osc-} = \frac{4}{\pi} I_{bias} R_p$$

Given that a minimal amplitude $V_{osc,min} = 0.3\,\mathrm{V}$ is required for the dividers to operate sufficiently in the transceiver. Use equation (2.16) and the goal to achieve $-124\,\mathrm{dBc/Hz}$ @ $3.5\,\mathrm{MHz}$ offset makes

$$\mathcal{L}(\Delta\omega) = -124\,\mathrm{dBc/Hz} = \frac{kT \cdot R_p}{\left(V_{osc} Q_{tank}\right)^2} \cdot F \cdot \left(\frac{\omega_{LO}}{\Delta\omega}\right)^2$$

Assuming a noise figure of $F = 5.5$ [7] and considering

$$Q_{tank} = \left(\frac{1}{Q_L} + \frac{1}{Q_C}\right)^{-1} = \left(\frac{1}{16} + \frac{1}{50}\right)^{-1} = 12.12, \tag{3.1}$$

where Q_L and Q_C are quality factors for the inductor and capacitor, respectively. To achieve $-124\,\mathrm{dBc/Hz}$, makes that for the BLE, a minimum parallel loss of $R_{p\,min} \approx 1000\,\Omega$ is required. The $V_{osc,min}$ is for nominal operation sufficient, but to guarantee oscillation also over corners and temperature variations, a $V_{osc} \approx 0.4\,\mathrm{V}$ is aimed at. Moreover, based on Chapter 2.3, RVTH devices are used and accordingly optimised for this $0.4\,\mathrm{V}$ oscillation amplitude.

In figure 3.3, the other PN offsets are determined based on Leeson's equation (2.9) with $R_{p\,min} \approx 1000\Omega$, $Q_{tank} = 12.12$ and an assumed $f_{1/f^3} \approx 130\,\mathrm{kHz}$. The figure describes how the PN decreases with increasing current consumption as the V_{osc} increases linearly. The important offset $3.5\,\mathrm{MHz}$ determines the current expected for the other offsets. So, since the offset $3.5\,\mathrm{MHz}$ requires a $I_{bias} = 340\,\mu A$, the PN goal for $10, 10^2, 10^3$ and 10^4 kHz will be set at the same I_{bias} and are therefore $-63, -90, -111, -132\,\mathrm{dBc/Hz}$ respectively.

Now that the BLE current is estimated and the tank's minimum loss is quantified, an estimate for the EDR mode has to be determined. As the PN requirements are the same for both BLE and EDR, but EDR has a more relaxed current consumption, the losses R_p are allowed to be less than $1000\,\Omega$. Since the EDR mode is twice the frequency of the BLE mode, a R_p close to half of $1000\,\Omega$ will be targeted for this mode.

3.2 Capacitor tuning only

With the estimation of I_{bias} and the minimal parallel losses R_p in BLE that achieve the required PN, now the focus will be on how to accomplish the two frequency bands while guaranteeing the estimated I_{bias} and R_p.

Both the BLE and the EDR modes require each having a TR of 19.5%, setting the minimum and maximum frequency (f_{min}, f_{max}) to 4416 and 5356 MHz for BLE with 4800 MHz center frequency (f_{LO}) and 8832 and

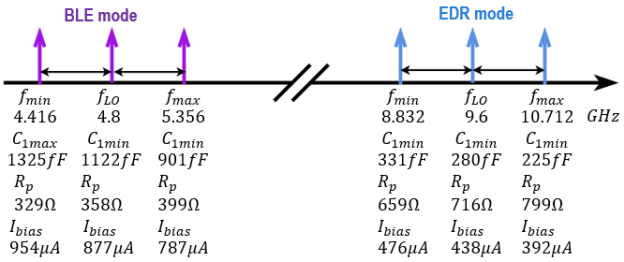


Figure 3.4: Illustration of the frequency band of BLE and EDR, with its required capacitance and expected R_p and I_{bias} with $Q_{tank} = 12.12$ and $L_1 = 0.98\,\text{nH}$.

10712 MHz for EDR with 9600 MHz center frequency. For simplicity, assume an LC tank as figure 3.2. The oscillation frequency is given as

$$f_{LO} = \frac{1}{2\pi}\frac{1}{\sqrt{L_1 C_1}} \tag{3.2}$$

When using a capacitor bank for frequency tuning, minimum capacitance from the parasitics of the switches and active devices always has to be taken into account. We assume, therefore, a minimum capacitance $C_{1\,min} = 225fF$. With this minimum capacitance and equation (3.2), the maximum inductance value of L_1 can be calculated. If only capacitor tuning is assumed, the inductance L_1, has to be chosen such that it can at least achieve the highest f_{max} of both modes. This makes $L_1 = 0.98\,\text{nH}$.

In figure 3.4, an illustration is given on achieving the frequency tuning using only capacitance and constant $L_1 = 0.98\,\text{nH}$. The figure also shows how for a lower frequency band (BLE) more current will be required to faciliate a constant 0.4V oscillation amplitude. This is derived by the following equations:

$$R_p = \left(\frac{1}{R_L} + \frac{1}{R_C}\right)^{-1} \tag{3.3}$$

Where R_p can be represented as the parallel combination of the losses of capacitance C_1:

$$R_C = \frac{Q_C}{2\pi f C_1} \tag{3.4}$$

and the parallel losses of the inductor L_1:

$$R_L \approx Q_L \cdot 2\pi f L_1 \tag{3.5}$$

By substitute (3.4), (3.5) in (3.3) and using (3.1), we have:

$$R_p = \sqrt{\frac{L_1}{C_1}} \cdot Q_{tank} \tag{3.6}$$

And since aiming for the same quality factor as in (3.1) and the maximum inductance is known, the parallel

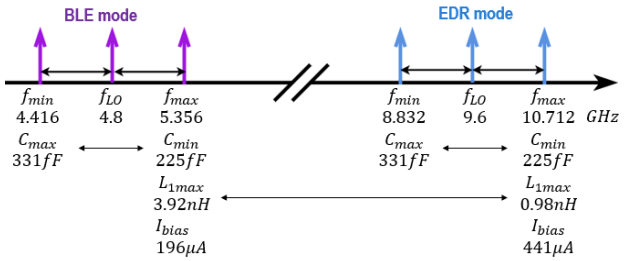


Figure 3.5: Illustration of the frequency band of BLE and EDR, with its required capacitance and expected I_{bias} with $Q_{tank} = 12.12$ for tuning the inductance from $L_1 = 0.98\,\text{nH}$ to $L_1 = 3.92\,\text{nH}$.

losses will decrease with increasing C_1(lower f_{LO}). Combining (2.27) and (3.6):

$$I_{bias} = \frac{\pi}{4}\frac{V_{osc}}{Q_{tank}}\sqrt{\frac{C_1}{L_1}} \tag{3.7}$$

Describes that the current required increases when using a large amount of C_1.
It shows that using capacitor tuning over a wide spectrum is not beneficial as it requires a large amount of current at the lower spectrum, which is the opposite of our goal.

3.3 Inductor tuning

A better method in dual-mode oscillators is to tune the inductance value for each mode as it saves power consumption [89]. Using the same scenario as in Section 3.2, with $C_{1\,min} = 225fF$ but now the, inductance value changes when changing Bluetooth mode. Again, we use (3.2) for each f_{max} with $C_{1\,min}$ to determine the maximum required inductance. Figure 3.5 shows that based on the same equation 3.7, the I_{bias} will significantly improve compared to capacitor tuning only. This comes from the fact that Q_L is taken constant while its inductance value has quadrupled, meaning that the R_L increases and therefore R_p too.
The calculated values of I_{bias} show ultra-low current consumption compared to what is required to achieve the PN specifications. This comes at the cost of the amount of area required for a $L_1 = 3.92\,\text{nH}$, compared to the capacitor-only tuning ($L_1 = 0.98\,\text{nH}$). Now that it has been shown that the inductance value has to be changed to meet the aimed low current consumption specification in BLE, the bottleneck is with the method of changing this inductance value. Compared to capacitance tuning, inductance tuning can severely degrade the performance of the oscillator, as shown in the literature in Chapter 2.2. Two simple methods of inductor tuning will be addressed to prove the severe degradation in dual-mode oscillators.

3.3.1 Parallel inductor

The simplest method to create an inductor tuning is to add an inductor L_2 with a switch in parallel to L_1. An illustration of the tank is given in figure 3.6. Turning the switch ON and choosing $L_2 \leq L_1$ creates a

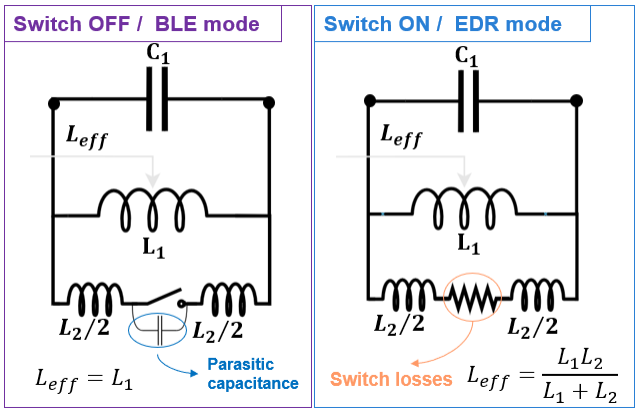


Figure 3.6: Illustration of the LC tank with an additional L_2 in parallel, that can be turned OFF or ON.

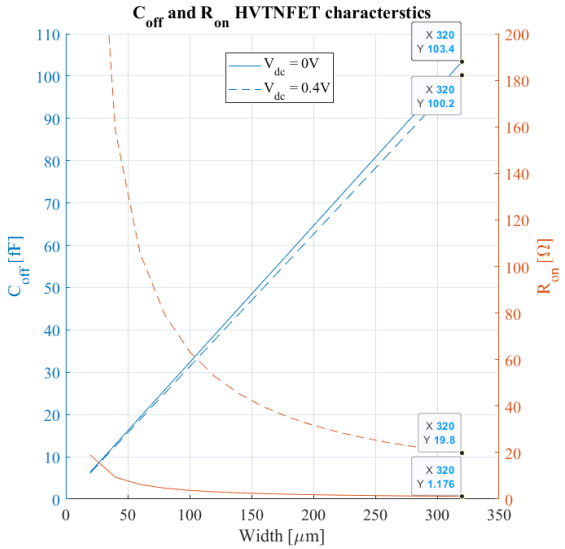


Figure 3.7: R_{ON} and C_{off} as function of scaling the HVTH at a DC of 0V and 0.4V

total effective inductance of

$$L_{eff} = \frac{L_1 L_2}{L_1 + L_2} \tag{3.8}$$

that will be lower compared to L_1, which creates the possibility of tuning accordingly.
The problem in this implementation is the switch that creates severe losses when turned ON. To limit the losses along the propagation path, the switch must offer low resistance losses when ON and high isolation in the OFF-state. As discussed in Chapter 2, adding this switch will degrade the inductor design. Yet, it can be possible to keep the degradation within the limit by sizing the switch large enough. Figure 3.7 shows the simulated losses R_{ON} and the parasitic capacitance C_{off} by scaling the width of the HVTH device. In CMOS topology the switch in the LC tank is biased at around 0.4V, creating a 17 times more R_{ON} than when the switch would be connected to ground.

The R_{ON} is added to the serie resistance r_{L_2} of L_2, decreasing the parallel resistance of L_2

$$R_{L_2} \approx \frac{(\omega L_2)^2}{r_{s2} + R_{ON}} \tag{3.9}$$

Ultimately effecting the quality factor of the effective inductance L_{eff}

$$Q_{L_{eff}} = \frac{R_{L_1} R_{L_2}}{R_{L_1} + R_{L_2}} \frac{1}{\omega L_{eff}} \tag{3.10}$$

In figure 3.8, equation (3.10) with equation (3.1) describes how scaling the switch affects the quality factor of the LC tank. The figure shows that even up to 560 μm the Q_{tank} is more than halved compared to (3.1). Following the Leesons equation (2.9), compensating this Q_{tank} degradation would require twice the V_{osc} which is not feasible.

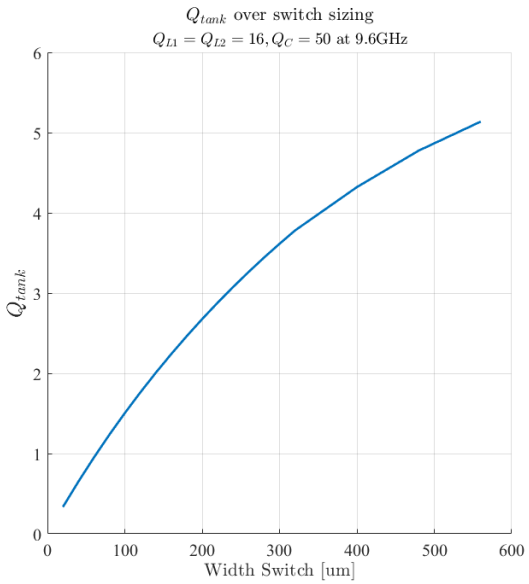


Figure 3.8: Q_{tank} calculated with the added R_{ON} from the HVTH switch. With $L_1 = 3.92\,\text{nH}$ and $L_2 = 0.98\,\text{nH}$.

One might consider switching the size in the order of millimeters, but C_{off} will increase linearly and thus decreases the f_{max} and TR.

3.3.2 Inductor magnetically coupled

The other method to decrease from $L = 3.92\,\text{nH}$ in BLE to $L = 0.98\,\text{nH}$ in EDR is by magnetically coupling a second inductor. By using the magnetically coupling factor k defined as

$$k = \frac{M}{\sqrt{L_1 L_2}} \tag{3.11}$$

where M is the mutual inductance between L_1 and L_2. The LC tank is depicted in figure 3.9. When the switch is turned ON, and no losses are assumed [115], the coupling allows the effective inductance to change to

$$L_{eff} = L_1\left(1 - k^2\right) \tag{3.12}$$

Since the inductance difference between BLE and EDR is roughly 3 nH, the required $k = 0.86$. This requires that L_1 and L_2 need to be interwind and require a transformer-like structure. Furthermore L_2 has to be in the same order of L_1 to achieve the wanted k. The quality factor, so far assumed to be equal to 16, will not hold anymore if aiming for transformer design with $k = 0.86$. Even if considering an $Q_L = 16$ and unlimited area, the high k reduces the effective quality factor [115]. Following equations from [115] makes

$$Q_{L_{eff}} = \omega \cdot \frac{(R_{ON} + r_{L2})^2 L_1 + \omega^2 L_1 L_2^2 (1 - k^2))}{r_{L1}(R_{ON} + r_{L2})^2 + \omega^2 L_2 (k^2 L_1 (R_{ON} + r_{L2}) - r_{L1} L_2)} \tag{3.13}$$

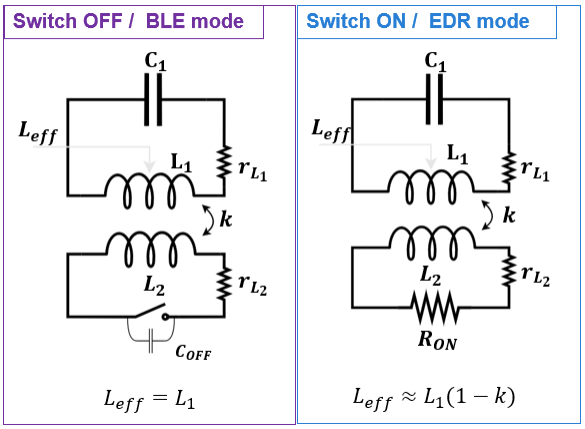


Figure 3.9: Illustration of the LC tank with an additional L_2 magnetically coupled, that can be turned OFF or ON.

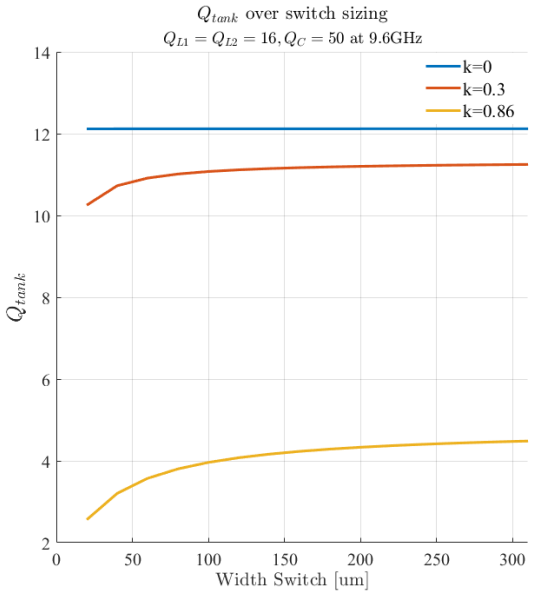


Figure 3.10: Q_{tank} calculated with the added R_{ON} from the HVTH switch, biased at 0V. With $L_1 = 3.92\,\text{nH}$ and $L_2 = 0.98\,\text{nH}$.

where r_{L_1,L_2} are the series resistances of $L_{1,2}$ respectively. Use equation (3.13) with equation (3.1) makes figure 3.10. The Figure 3.10 verifies the severe degradation of Q_{tank} at high k, even at large scaling of the switch.

3.3.3 Resonator

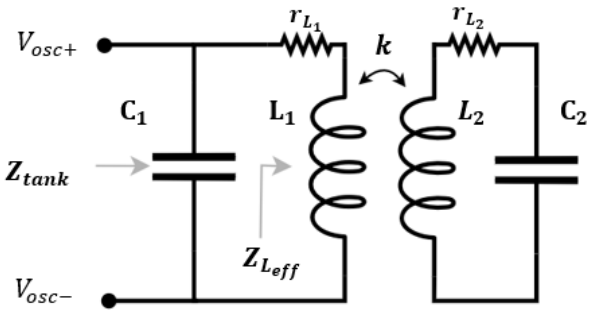


Figure 3.11: Illustration of a resonator with the output of the oscillator at the primary side.

Whereas in previous section, the resistance R_{ON} effects the effective inductance as

$$Z_{Leff} = j\omega L_1 - \frac{k^2 L_1 L_2 \omega^2}{R_{ON} - j\omega L_1} \approx j\omega L_1(1 - k^2) \tag{3.14}$$

replacing the R_{ON} with a second capacitor bank C_2, creates a resonator as illustrated in figure 3.11.

The tank impedance Z_{tank} can be set as

$$Z_{tank} = \left(\frac{1}{Z_{C1}} + \frac{1}{Z_{L_{eff}}}\right)^{-1} \tag{3.15}$$

Where $Z_{C_1} = \frac{1}{j\omega C_1}$. Use (3.14), with C_2 instead of R_{ON} and substitute into (3.15) creates a quadratic equation where the roots determine the oscillation frequency as shown in [81]:

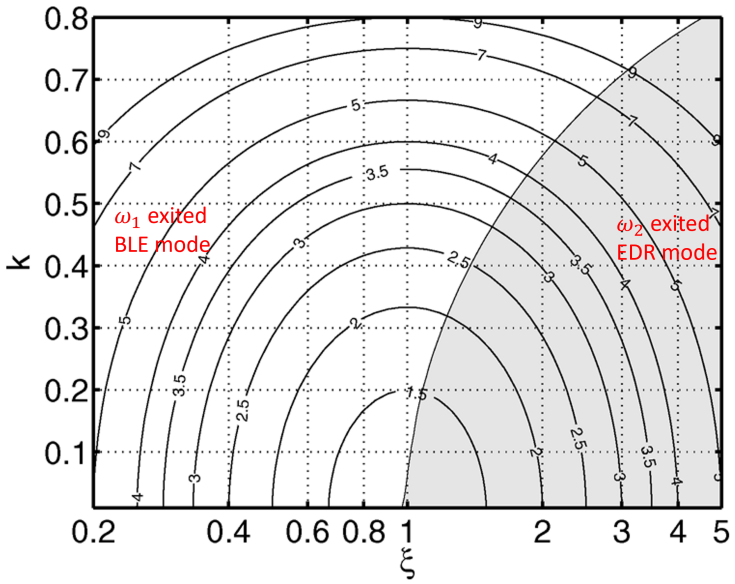


Figure 3.12: Contour plot of $\left(\omega_2/\omega_1\right)^2$ as a function of ξ and k. The shaded area represents when R_{p2} will be exited and otherwise the R_{p1}. Conducted from [92]

$$\omega_{1,2}^2 = \frac{1 + \xi \pm \sqrt{1 + \xi^2 - \xi(4k - 2)}}{2L_2C_2(1 - k^2)} \tag{3.16}$$

with ξ as the ratio between the primary and secondary side.

$$\xi = \frac{L_2C_2}{L_1C_1} \tag{3.17}$$

Based on the equations (3.16) and (3.17) the figure 3.12 illustrates the increase of ratio $\left(\omega_2/\omega_1\right)^2$ for both ξ and k.

Note that this resonator does not require any switch to select the BLE or EDR mode. This is different than the trivial inductor tuning described in Sections 3.3.1 and 3.3.2. In this resonator, two frequencies are created at the same instant. As in [92, 93], one can select the first frequency ω_1 or the second ω_2. However as will be shown in this section, realizing the specific frequencies $\omega_1 = 2\pi \cdot 4.8\,\text{GHz}$ and $\omega_2 = 2\pi \cdot 9.6\,\text{GHz}$ has limitations and requires significant current.

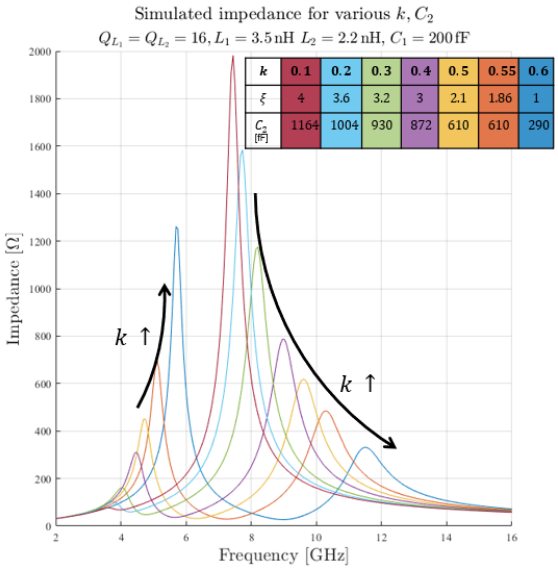


Figure 3.13: Simulated tank impedance for $\omega_1^2/\omega_2^2 = 4$, as a function of k and C_2

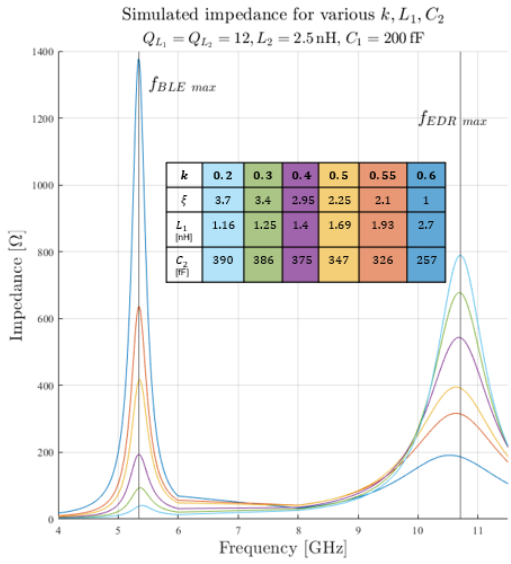


Figure 3.14: Simulated tank impedance for $\omega_1^2/\omega_2^2 = 4$ and at the tuned at f_{max} for each mode, as a function of k, C_2 and L_1.

To understand the resonator with two LC tanks that are magnetically coupled, figure 3.12 is conducted from [92]. It shows the contour plot of the ratio $\left(\omega_2/\omega_1\right)^2$. In this thesis, the ratio should be aimed at 4, as EDR mode must operate at twice the frequency band of BLE. Following contour line of 4, shows that for every k, a different ξ is required. A simulation is shown in figure 3.13, where C_2 is adjusted to set ξ to the exact required frequency ratio. The figure shows the real part of the tank impedance. The figure shows clearly that, thus, R_p reduces with the k. Observe in the added table that only C_2 reduces to adjust to the correct ξ. It shows that even though high values of L_1 and L_2 are used, k and ξ determine R_p.
To show a better comparison at the same frequency a more exact simulation of the tank impedance is shown in figure 3.14. It shows a constant frequency for different k in which both L_1 and C_2 are adjusted accordingly. The figure shows again that k improves the R_p for the lower frequency.

To meet $R_{p\ min} \approx 1000\,\Omega$ for the BLE mode, a coupling $k \geq 0.56$ would be needed. The figure 3.14 shows how volatile the values of R_p and L_1 are for k between 0.55 and 0.6. Furthermore, R_p for the EDR frequency in $k = 0.6$ is only $190\,\Omega$ and would result in 5 times more current compared to the BLE required $R_p \approx 1000\Omega$. In addition, the quality factor taken here is only 12 instead of 16, which is based on the optimizer for 22nm FDX inductor layouts. When designing transformers opposed to stand-alone spiral or symmetrical inductors, the aim for a quality factor of 16 becomes significantly more challenging. Opting for a quality factor of 12 would therefore offer a much more realistic interpretation of the tank impedance.

Even if, in EDR mode, a fivefold increase in current consumption is allowed, the challenge of excite oscillation at the higher frequency band(ω_2) rather than the lower frequency band (ω_1) demands a substantial

amount of additional current. This stems from the inherent characteristic that, typically, the frequency with the highest peak impedance is excited by a cross-coupled device($-G_m$). Yet to also oscillate at ω_2 with a lower peak than ω_1, which is, the case for $k \geq 0.56$, an additional G_m stage should be added. Otherwise both oscillation frequencies are excited. This G_m stage allows the higher frequency to oscillate [92]. The downside here is that the current required for the G_m is significant. Following [93], showing a tank impedance peak of 160 Ω with $Q_{tank} = 12$, an additional current between 5.5 mA and 8.2 mA is required at 3.6 GHz and 4.77 GHz. Therefore, using the resonator with a $k = 0.56$, would require a significant amount of current and a notably reduced quality factor in the EDR mode.

3.4 Proposed tank design

With analysis given about the inductor tuning options that require a switch and the resonator requiring an additional G_m stage, the proposed tank design facilitates a combination between inductor tuning with the switch and the coupling between two LC tanks.
Instead of having the secondary winding and its switch floating as in Section 3.3.2, one could connect it to the primary winding creating two parallel inductors, where L_2 can be turned ON and OFF. As shown in figure 3.7, it is important to have the DC of the switch to ground to minimize the degradation of the second inductor. Therefore, large coupling capacitors C_c are used in figure 3.15. The proposed resonator shows a combination of the dual-mode oscillator, like [89], and the inductor switching as in [88], both discussed in Chapter 2.2. And because of this combination the R_{on} of the switch is minimized compared to a normal parallel inductor from Chapter 3.3.1.

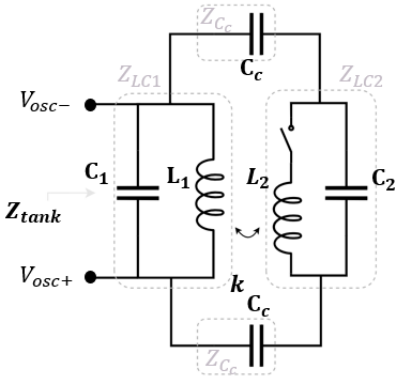


Figure 3.15: Proposed dual-mode resonator with electrically coupled capacitance, creating parallel inductors at high frequency.

3.4.1 Switch OFF/BLE mode

The LC tank, when the switch is turned OFF can be illustrated as figure 3.16. The switch that is in series with L_2 created a high isolation allowing no current to flow into L_2, and thus, only L_1 contributes to the inductance in BLE. Moreover, C_2 in series with two C_c still allows for capacitive tuning. Important is that

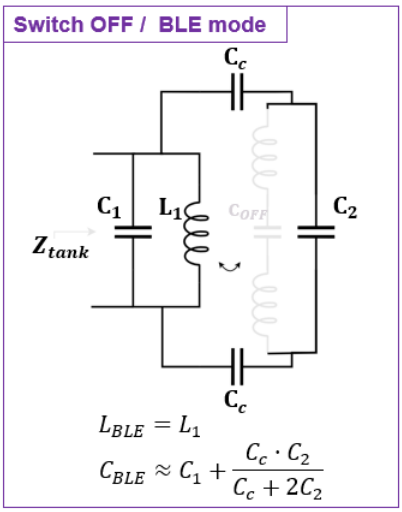


Figure 3.16: Illustration of the proposed tank when the switch is turned OFF.

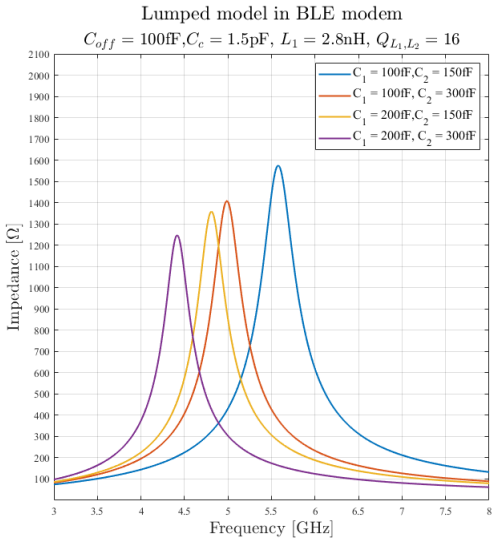


Figure 3.17: Z_{tank} at different C_1 and C_2 ($Q_C = \infty$) when the switch is OFF and sized at 320 μm

the $C_c >> C_2$, resulting in a total capacitance in BLE of

$$C_{BLE} \approx C_1 + \frac{C_c \cdot C_2}{C_c + 2C_2} \tag{3.18}$$

Because of this C_c, C_2 contributions will be less than tuning with the C_1. However, as the capacitance tuning can now be split up between C_1 and C_2, the parasitic capacitance of each capacitor bank will be less and thus the minimum $C_{1\ min}$ and $C_{2\ min}$ can be lowered to 100 fF and 150 fF. Although no current is expected to flow through L_2, the C_{off} of the switch will still contribute to a lower oscillation frequency. For that reason, the $L_1 = 3.2$ nH is set lower than the maximum inductor value in Section 3.2.2. The figure 3.17 shows the Z_{tank} for various C_1 and C_2. The figure shows that the R_p will meet the BLE requirement of $R_{p\ min} \geq 1000\,\Omega$.

3.4.2 Switch ON/ EDR mode

In EDR mode still, two modes can be exited because of the two individual tanks coupled by C_c and k. The analysis of the tank impedance in EDR mode can be determined as:

$$Z_{tank} = \left(\frac{1}{Z_{LC1}} + \frac{1}{Z_{LC2} + 2Z_{C_c}}\right)^{-1} \tag{3.19}$$

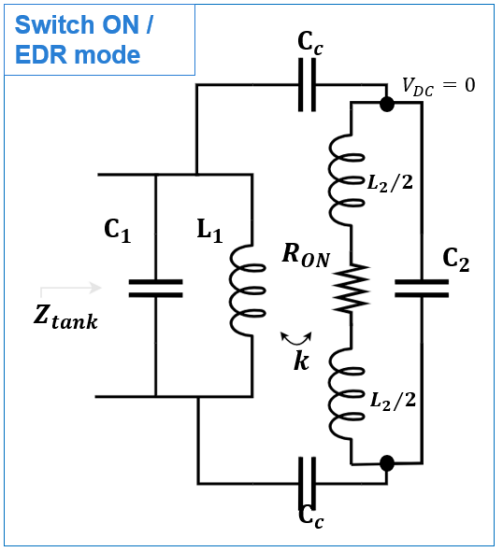


Figure 3.18: Illustration of the proposed tank when the switch is turned ON

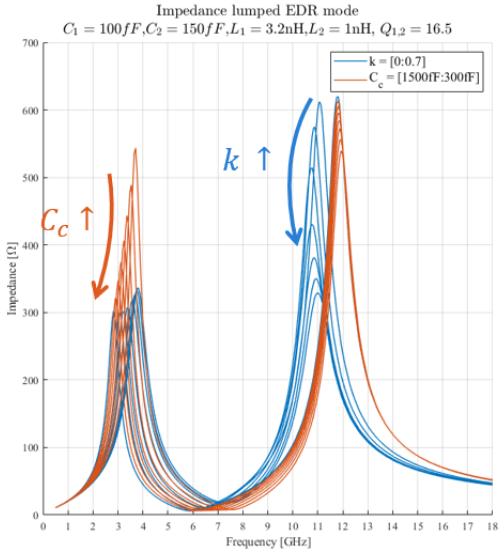


Figure 3.19: Z_{tank} at various k and C_c when the switch is ON and is sized at $W = 320\,\mu$m

where with taken into account the series losses of both inductors r_{L_1}, r_{L_2}, $Z_{LC1,2}$ and Z_{C_c}

$$\begin{aligned} Z_{LC1} &= \frac{j\omega L_1(1-k^2) + r_{L_1}}{1 - \omega^2 L_1(1-k^2)C_1 + j\omega C_1 r_{L_1}} \\ Z_{LC2} &= \frac{j\omega L_2 + r_{L_2}}{1 - \omega^2 L_2 C_2 + j\omega C_2 r_{L_2}} \\ Z_{C_c} &= \frac{1}{j\omega C_c} \end{aligned} \tag{3.20}$$

are based on the impedance illustrated in figure 3.15. Resulting in the complete tank impedance Z_{tank} [1] where C_2', C_1' and C_x are the combination of the capacitances:

$$\begin{aligned} C_1' &= C_1 + 0.5C_c \\ C_2' &= C_2 + 0.5C_c \\ C_x &= C_1C_2 + 0.5C_cC_1 + 0.5C_cC_2 \end{aligned} \tag{3.22}$$

Resulting in a similar quadratic equation [116]

$$\omega^4(L_1L_2(C_x)(1-k^2) - \omega^2(L_1(C_1') + L_2(C_2')) + 1 = 0 \tag{3.23}$$

[1]

$$Z_{tank} = \frac{(1-k^2)L_1L_2(C_2')j\omega^3 - (L_2r_{L_1} + L_1r_{L_2})(C_2')\omega^2 + (L_1 + r_{L_1}r_{L_2}(C_2'))j\omega + r_{L_1}}{(1-k^2)L_1L_2(C_x)\omega^4 + (L_2r_{L_1} + L_1r_{L_2})(C_x)j\omega^3 - (L_1(C_1') + L_2(C_2') + r_{L_1}r_{L_2}(C_x))\omega^2 + (r_{L_1}(C_1') + r_{L_2}(C_2'))j\omega + 1} \tag{3.21}$$

which again results in two resonance frequencies:

$$\omega^2_{1_{EDR},2_{EDR}} = \frac{L_1C_1' + L_2C_2' \pm \sqrt{(L_1C_1')^2 + (L_2C_2')^2 + 2L_1L_2C_1'C_2' - 4(1-k^2)L_1L_2C_x}}{2L_2L_1C_x(k^2-1)} \tag{3.24}$$

where $C_x = C_1'C_2' - \frac{1}{4}C_c^2$ and creates an extra factor in the square-root and denominator compared to [7, 92]:

$$\omega^2_{1_{EDR},2_{EDR}} = \frac{L_1C_1' + L_2C_2' \pm \sqrt{(L_1C_1')^2 + (L_2C_2')^2 + (4k^2-2)L_1L_2C_1'C_2' + (1-k^2)L_1L_2C_c^2}}{2L_2L_1C_1'C_2'(1-k^2) + 0.5(1-k^2)L_1L_2C_c^2} \tag{3.25}$$

From research in Chapter 2.2, it is known that in one of the two frequencies, the C_c contributes due to the even mode. Or intuitively speaking, the C_c acts as an open at low frequencies, and thus, the higher C_c, the better, the lower mode will be suppressed. And at higher frequencies the C_c acts as a short resulting that both the inductors L_1 and L_2 can be assumed to be parallel.

To also take into account the losses of the switch R_{on}, the series losses of L_2 can be rewritten as

$$r'_{L_2} = r_{L_2} + R_{on} \tag{3.26}$$

and thus lowering the Q_{L_2}. To show exactly how sizing the switch affects the resonator, the model based on equation (3.21) with r'_{L_2} is used. The Z_{tank} and Q_{tank} are shown in figure 3.20, where an increase in Z_{tank} and Q_{tank} is expected, with a maximum $Q_{tank} = 8.12$ for $W = 320\,\mu$m. Compared to the other qualities of previously shown inductor tuning (figure 3.10 and 3.8), at least an improvement of 25% is created. A further improvement to $Q_{tank} = 9$, can be achieved by doubling the C_c or scaling the switch further. The first option, also decreases the impedance at the lower frequency peak, at the cost of increased area. The second simply creates lower losses in the signal path. Yet since equation (3.21) does not include the C_{off} of the switch, the true disadvantage of scaling the switch cannot be observed.

To correctly take into account the C_{off}, a lumped model as illustrated in figure 3.16 and 3.18 is simulated and its Z_{tank} is shown in figure 3.21. It used switch losses of $R_{on} = 1.17\,\Omega$ and $C_{off} = 103\,$fF (figure 3.7). The increase in C_c slightly affects the total capacitance in BLE mode by the definition of C_{BLE} in equation (3.18).

Furthermore, the trajectory of k in figure 3.21 shows that a small coupling does not have a significant effect on the impedance peak for EDR. The increase in $\omega_{1,EDR}$ and decrease $\omega_{2,EDR}$ are in line with the literature [89] that approximates the frequencies as:

$$\omega^2_{1,EDR} = \frac{1}{L(1-k)(C+C_c)} \tag{3.27}$$

and

$$\omega^2_{2,EDR} = \frac{1}{L(1+k)(C)}, \tag{3.28}$$

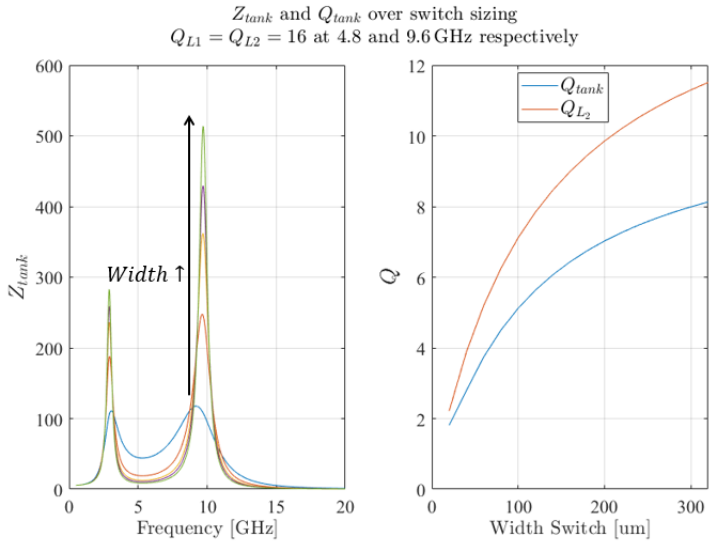


Figure 3.20: The effect of scaling the switch on the Z_{tank},Q_{tank} and Q_{L2}. $C_c = 1.5\,\text{pF}$,$C_1 = 100\,\text{fF}$,$C_2 = 330\,\text{fF}$,$L_1 = 2.8\,\text{nH}$,$L_2 = 0.8\,\text{nH}$.

where $L = L_1 = L_2$,$C = C_1 = C_2$ and using positive mutual coupling $M = k\sqrt{L_1 L_2}$. The reason why the $\omega_{2,EDR}$ frequency increases again at high k is due to the asymmetric capacitive and magnetic coupling, which is described in the appendix of [89].

Overall by comparing the tank impedance of the resonator from Section 3.3.3 (figure 3.13) and the impedance of the proposed design (figure 3.21), the latter easily achieves the required impedance, $R_{pmin} \approx 1000\,\Omega$ at the 4.8GHz band, whereas the resonator would require a very specific L_1 and high k. Lowering the minimum capacitance C_1 enhances the peak of the higher frequency mode, $R_{2,EDR}$, with respect to the lower frequency mode $R_{1,EDR}$. This is important in the EDR mode because ensuring that the $R_{1,EDR} << R_{2,EDR}$ will also guarantee that the oscillation will be at the higher frequency mode. And since C_2 also tunes in BLE mode a very large capacitor bank in C_1 would not be necessary. Moreover, the inductance of L_2 compared to the L_2 used in the resonator in Section 3.3.3 is 3 times smaller and will thus save area, without deterioration of the Q factor.

Lumped Variables	BLE mode		EDR mode		
	R_p	C_{min}	R_{p1}	R_{p2}	C_{min}
$L_1 \uparrow$	↑	↓	↑	↓	↓
$L_2 \uparrow$	–	–	↓	↑	↓
+k ↑	∼↑	↑	–	↓	∼↓
-k ↑	∼↓	↑	–	↓	↑
$C_c \uparrow$	–	↓	↓	–	–

Table 3.1: A summary of how the lumped variables effect the impedance of the tank and it required minimal capacitance to achieve the TR. (small) Increased/decreased value: (∼) ↑ / ↓.

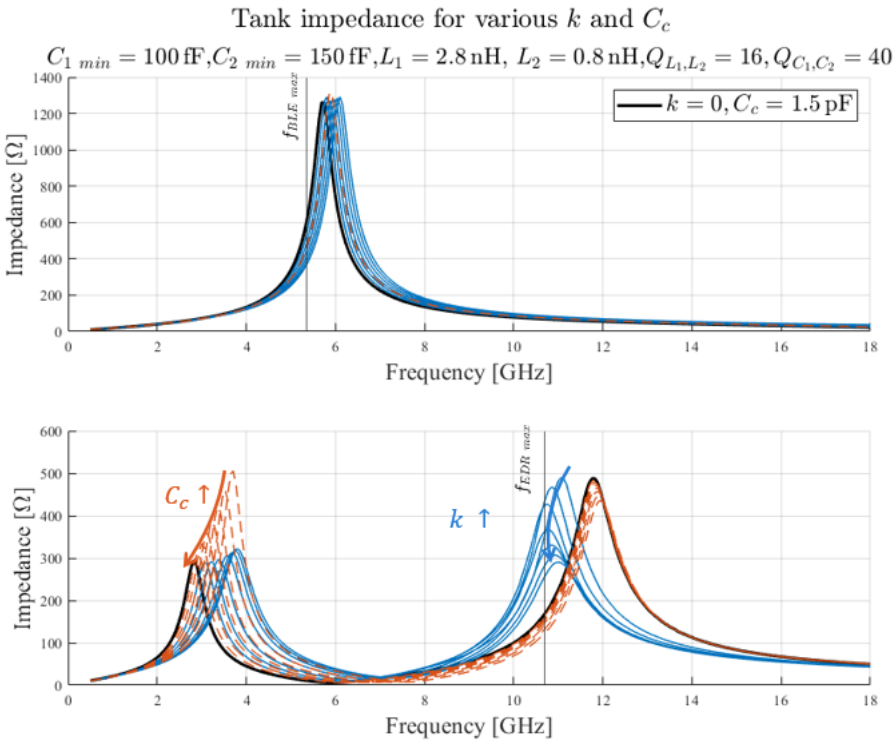


Figure 3.21: Simulated tank impedance for each BLE/EDR mode with lumped components, orange describes the increase of C_c, while the blue describes the increase in k.

To summarize and clarify on each design variable, their effects are summarized in table 3.1. An important design choice is the amount of coupling. As with a lower L_2 one can allow a high k that is roughly maintained in the same frequency range. This would reduce the needed area. Yet a too-high coupling between the two inductors will result in $R_{1,EDR} \geq R_{2,EDR}$. Thus, a more thorough analysis of the relationship between the inductor design and coupling is necessary.

3.5 Inductor layout

To show the implementation and layout of the inductors, three different k layouts will be discussed. By understanding and comparing these three situations, a clear estimated design choice can be made on what best suits this dual-mode application based on area and TR.

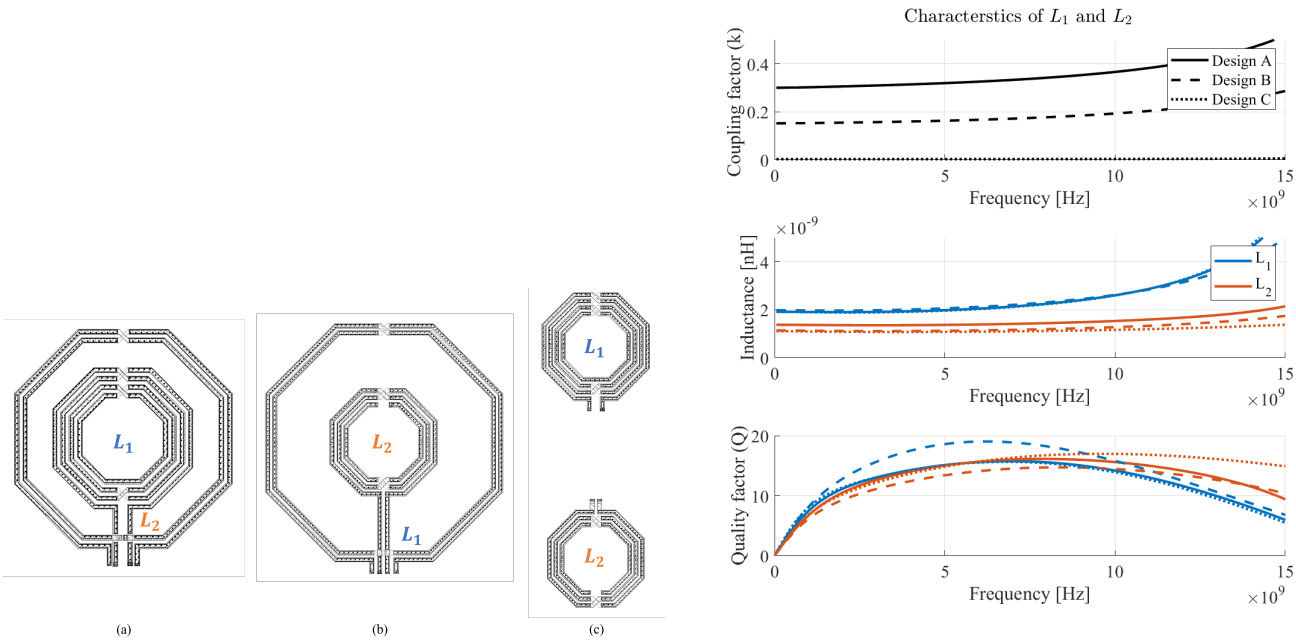


Figure 3.22: Three inductors designs(A,B,C) with each their k,L and Q_L over frequency. Layout figures are not equally scaled.

The two inductors L_1 and L_2, for fair comparison, have in each design the same inductance 2.2 nH and 1.53 nH, respectively.

In design A (figure 3.22a) L_2 is around the L_1 ,where due to the spacing between them and the number of windings, a coupling $k \approx 0.3$ is realized. In design B (figure 3.22b), L_2 is the inner inductor. The outer inductor L_1 has fewer windings and a radius even wider than that of design A, resulting in $k \approx 0.15$. In design C (figure 3.22c) L_2 and L_1 are separated by roughly 100μm resulting in $k \approx 0$. Because in design A and B a specific k is created, deviations from its optimal Q of the inductor cannot be prevented. The exact characteristic of each design is given in figure 3.22. Observe how in design B the L_1 achieves a high Q due to its expensive area layout. For L_2 the design C shows the best Q factor due to low coupling. Aiming for the low area for a low k is difficult. Take, e.g. figure 3.22b, when one wants to increase the L_1 inductance, it can add a number of winding, which easily doubles the inductance value. As double inductance is too high, a smaller inner radius is needed, which results in a higher coupling with the inner inductor L_2, and thus further degrades the EDR mode.

Figure 3.23 compares the design layouts with its lumped model and the switch, illustrated as figure 3.18. The model shows higher impedance peaks because of the constant serie resistance across frequency, yet the lumped model generally aligns well with the coupling effect observed in the EMX designs.
Yet, comparing the inductor area, design A and B use up to 0.034 and 0.060 mm^2, respectively, whereas design C, excluding the 100μm spacing, uses 0.031mm^2. Areawise design A would be the best choice, which is inline with what would be expected as higher k ask the inductors to be closer and thus results in less area.

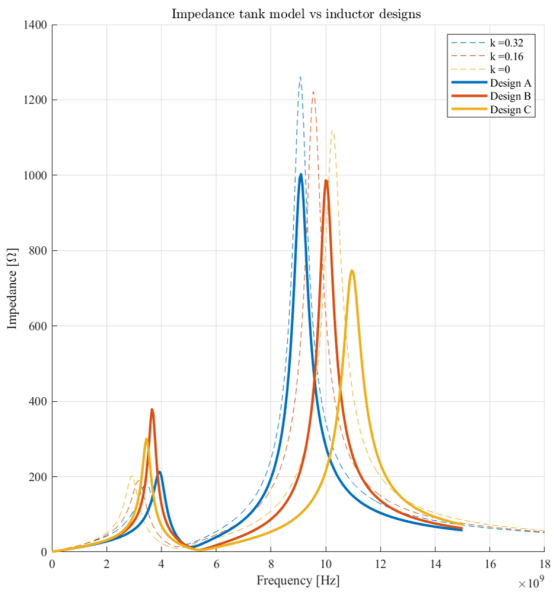


Figure 3.23: Tank impedance compared with EMX inductor designs and a lumped model with similar k.

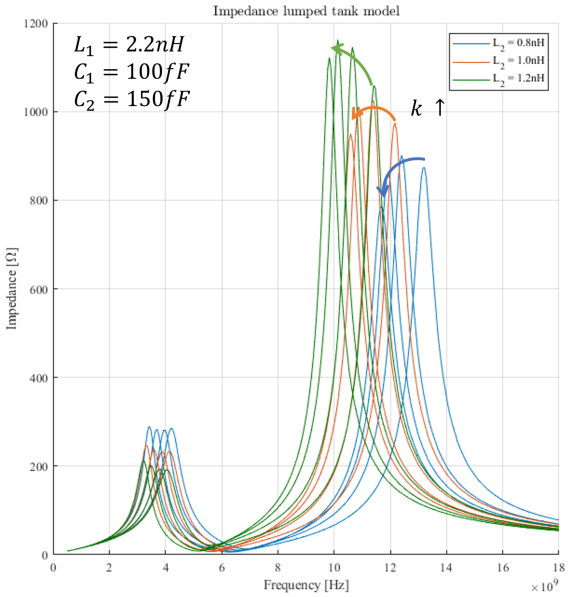


Figure 3.24: Tank impedance with lumped model for various L_2 as a function of k.$Q_{C1,2} = \infty$

However, observe in figure 3.23 how a small coupling already decreases the frequency, requiring a further decrease of L_2, to correct to f_{LO}.

In the case of design A, lowering L_2 requires a decrease in the inner radius, bringing it closer to L_1, resulting in a slightly increased k, which again reduces f_{LO}. This effect is also simulated with lumped models in figure 3.24. Another drawback that can be seen when aiming for design A is when lowering L_2, its increase of $R_{1,EDR}$ and decrease of $R_{2,EDR}$ will violate the $R_{1,EDR} < R_{2,EDR}$ requirement in EDR easily.

Besides that, design A is considerable limited by the Self-Resonance Frequency(SRF). When two inductors are placed near each other to accommodate a high k, excessive parasitic capacitances are created, thereby forming an LC tank by its own. Therefore, the best option is C. Aiming for two seperate inductors, makes that L_1 and L_2 are each optimized on area while reaching a quality factor of at least 16. Although the total area seems larger than that of design A, the space in between can be used by the active devices, biasing and the capacitor bank, making the actual DCO layout smaller than that of design A. The comparison above shows that even though a small coupling can benefit the required impedance peaks, the reality of creating a low coupling remains area intensive, and thus splitting the inductor all the way and optimizing them individually on area is more beneficial.

To keep in mind the BLE mode and its low-power specification, a higher L_1 and lower L_2 is chosen compared to the three inductor comparisons from above. The proposed design consists of $L_1 = 2.65\,\text{nH}$. An illustration is given in figure 3.25. For symmetrical purposes and minimal C_{off} contribution, it is important to place the switch evenly from the two output nodes of the L_2. Therefore, L_2 will be a symmetric inductor at all times. Yet in design C, L_1 does not have to be in or around the switch inductor L_2, and therefore, a spiral inductor is preferred because of its slightly better Q. This better Q comes from the less cross-over metal of a spiral inductor than the symmetrical inductor.

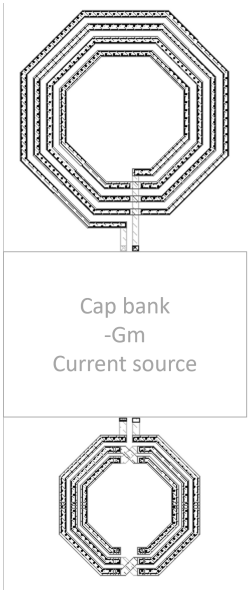


Figure 3.25: Proposed layout with a spiral $L_1 = 2.80$nH and symmetrical inductor $L_2 = 0.8$nH, with $(143.7\mu m \times 162.7\mu m)$ and $(104.8\mu m \times 111.4\mu m)$ respectively.

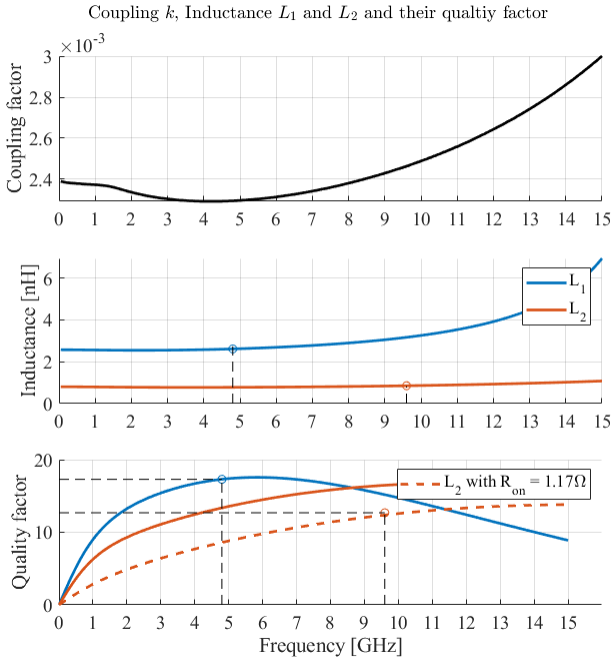


Figure 3.26: Characteristics k,Q_L and $L_{1,2}$ for the proposed design.

3.6 Capacitor bank

The capacitors in the LC tank should be set so that $f_{min} = [4.41, 8.82]$GHz and $f_{max} = [5.35, 10.7]$GHz for BLE and EDR, respectively, can be achieved. By achieving the oscillation with this range, PVT variations can be overcome and calibrated to the correct f_{LO}. However, to ensure the specific channel, the acquisition mode with finer frequency resolution is required [38, 15]. Where after a channel is chosen, the maintaining of this frequency has to be tracked. This centralization over variations and corners is mostly done by the coarse and medium banks. The fine-tuning bank can, with its finer resolution, provide the acquisition mode. In addition, to facilitate frequency locking, a modulation bank is required.

3.6.1 Coarse & Medium tuning bank

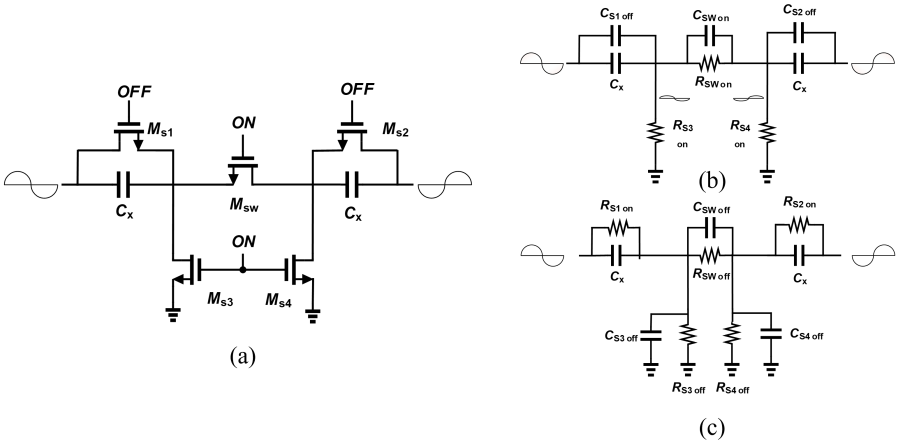


Figure 3.27: Schematic and lumped model of the coarse and medium tuning bank(a), in ON(b) and OFF(c) mode.

The large steps in frequency occur by using a large differential capacitance. However, to correctly tune this differential capacitance, the switch M_{sw} has to act symmetrically, and thus two separate C_x are needed. Figure 3.27a shows that besides M_{sw} also $M_{s1,2}$ and $M_{s3,4}$ are added. The NMOS devices in parallel with C_x are ON when M_{sw} is OFF and vice versa. This is to ensure that the source and drain for M_{sw} are not floating and create a short for C_x, ensuring that no energy will be stored in this capacitor. $M_{s3,4}$ functions similarly but makes the source and drain not float when M_{sw} is ON [117]. When turned ON, the switch is thus biased to ground. M_{s1-4} are only small devices that create a high-impedance. Their small parasitic are shown in figure 3.27b/c.
To ensure each unit of the bank adds not too much losses to the tank, the Q_{on} of each bank can be calculated as

$$Q_{on} = \frac{1}{\omega C_{unit\ ON} \cdot r_{SW\ on}} \tag{3.29}$$

here $r_{SW\ on}$ are again the losses of the switch M_{sw} as in figure 3.7. Although $r_{SW\ on}$ reduces with scaling M_{sw}, the amount of minimal capacitance increases linearly with the size, and thus, your ΔC_{diff} decreases.

Therefore, C_x has to be set sufficiently large to accommodate the needed ΔC_{diff} defined as

$$\Delta C_{diff} = C_{unit\ ON} - C_{unit\ OFF} \tag{3.30}$$

where $C_{unit\ ON}$ can be estimated by

$$C_{unit\ ON} \approx 0.5(C_x + C_{s1,2OFF}) \tag{3.31}$$

and $C_{unit\ OFF}$ can be estimated by

$$C_{unit\ OFF} \approx \frac{C_x C_{SWoff}}{(2C_{SWoff} + C_x)} \tag{3.32}$$

The small capacitance $C_{S3,4off}$ of $M_{s3,4}$ are negligible to $C_{unit\ OFF}$.

The schematic described in figure 3.27 for various C_x and scaling of M_{sw} is shown in figure 3.28 and shows exactly how much ΔC_{diff} and Q_{ON} can be achieved.

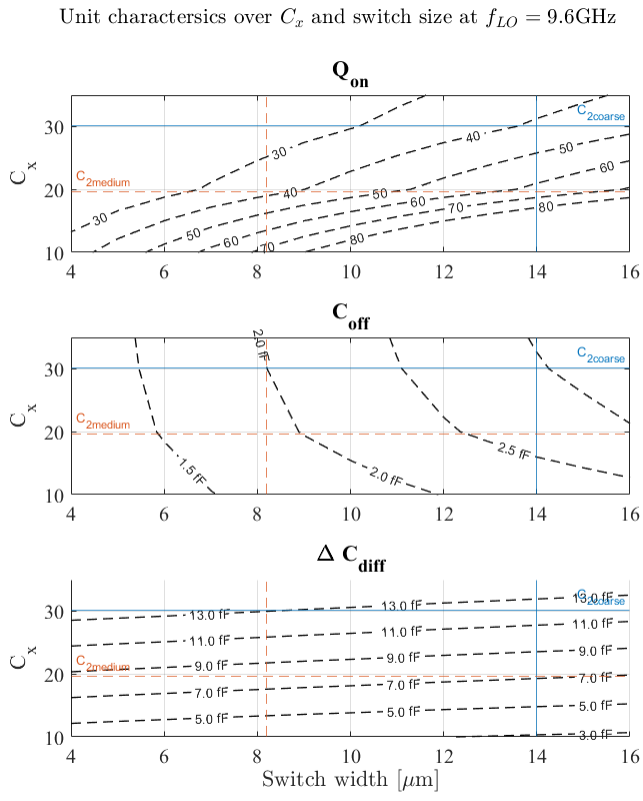


Figure 3.28: Contour plot of Q_{on},$C_{unit\ OFF}$ and ΔC_{diff} for C_x and width sizes of M_{SW}.

	Coarse		Medium
$C_{s1,2\ ON/OFF}$ [aF]	60/230		
$r_{s1,2\ ON/OFF}$ [Ω]	1.4/16		
$C_{s3,4\ OFF}$ [aF]	100		
$r_{s3,4\ OFF/ON}$ [kΩ]	2.6E6/2.6		
$r_{SW\ on}$ [Ω]	14.6(W=24.6μm)	55.9(W=14μm)	83(W=8.2μm)
$C_{SW\ off}$ [fF]	6.5	3.8	2.15
	$C_{1\ coarse}$	$C_{2\ coarse}$	$C_{2\ med}$
C_x [fF]	108.4	30.5	19.62
$C_{unit\ OFF}$ [fF]	5.43	2.93	1.91
$C_{unit\ ON}$ [fF]	54.76	15.1	9.7
ΔC_{diff} [fF]	49.33	12.17	7.79
$Q_{on}BLE/EDR$ [fF]	40/NA	80/40	80/39.9

Table 3.2: Unit values for Coarse and Medium banks

Note that the peak,$R_{2,EDR}$, in EDR mode is very C_1 dependent. Therefore, in EDR mode, tuning is

only done in C_2, such that the $R_{1,EDR} < R_{2,EDR}$. To provide a large step for PVT corrections with a coarse bank from 8.82GHz up to 10.7GHz, 16 coarse units are created, each with $C_x = 30.5\,\text{fF}$. Adding 192fF to C_2, which with $C_{2\ min} = 200fF$, already achieves the full TR required. For BLE, this $C_{2\ coarse}$ will only achieve half the required TR. Therefore, in BLE mode, another coarse $C_{1\ coarse}$ is required. To minimize $C_{1\ min}$, only 3 units with an $C_x = 108.4\,\text{fF}$ are used with a $C_{SW,off} \approx 6.5\,\text{fF}$, such that $Q_{C_{1\ coarse}} \approx 40$ at 4.8 GHz.

$C_{2\ med} = 19.62\,\text{fF}$ has been chosen so that for each 4 (of the 16) $C_{2\ coarse}$ steps, 6 steps of $C_{2\ med}$ achieve a similar frequency range. The overall design characteristics of the tune bank can be observed in table 3.2. The capacitor banks are simulated with the dual mode switch inductor showing TR of 26.76% and 27.86% for BLE and EDR respectively. One can observe that in case of the BLE the actual f_{min} is 138 MHz short. This is because the capacitance created by the TX and RX path and the dividers are not taken into account. In a full implemented ADPLL these would roughly add around 50 fF shifting the whole TR into the desired TR. Even in that case the TR of 19.5% can be easily met.

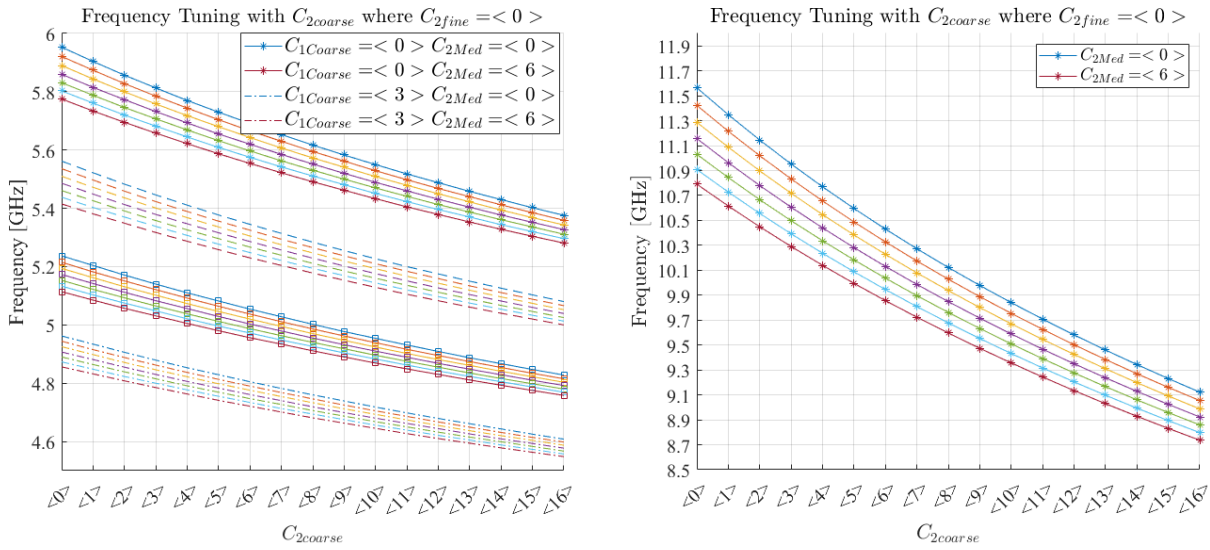


Figure 3.29: Oscillation frequency BLE and EDR over tuning each $C_{1coarse}$ and C_{1med} code over various large $C_{2coarse}$ steps.

3.6.2 Fine tuning bank

The fine-tuning bank works in a single-ended manner on each output node. Meaning that if one of the 64 codes turns on a capacitance difference of $\Delta C_{diff} = 0.5\Delta C_{se}$ is added to the C_2. The fine-tuning bank is given in figure 3.30. The additional capacitance before the switches is used to not directly connect the drain of the switch to the output nodes. A HVTH device with an $r_{on} = 24\,\Omega$ and $C_{off} = 4.26\,\text{fF}$ is used. When ON, $C_{unit\ ON} = C_{sx} = 6\,\text{fF}$, where in case of OFF, $C_{unit\ OFF}$ is C_{sx} in parallel with the $C_{sy} + C_{off}$ resulting

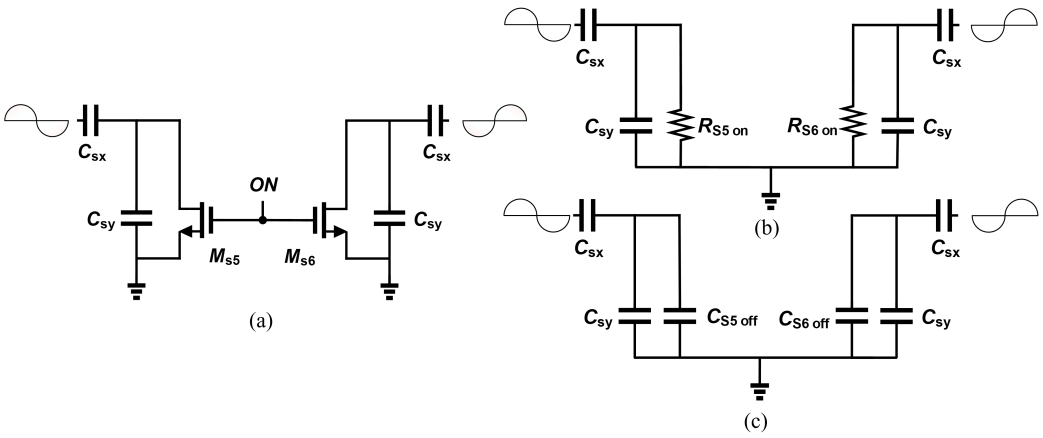


Figure 3.30: Schematic and lumped model of the fine-tuning bank(a), in ON(b) and OFF(c) mode

in an single ended capacitance:

$$\Delta C_{se} = C_{sx} - (C_{sx}||(C_{sy} - C_{off})) \tag{3.33}$$

Taking an $C_{sy} = 3C_{sx}$ creates roughly a $\Delta C_{diff} \approx 0.75\,\text{fF}$. Which means a minimum capacitance of 41 fF is added to the total C_2. For both the EDR and BLE, the tuning will be used, as can be observed in figure 3.31.

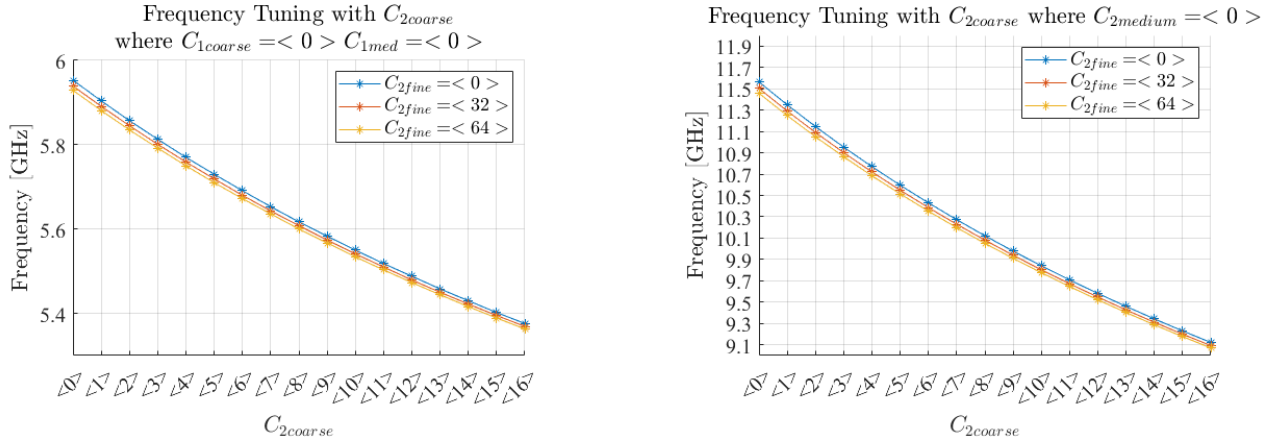


Figure 3.31: Oscillation frequency BLE and EDR over tuning C_{fine} over various large $C_{2coarse}$ steps.

The figure shows the start, middle, and end code of the fine-tuning bank. These 32 steps cause, depending on the $C_{2coarse}$ between 10.1 en 6 MHz for BLE and between 61.2 en 29.5 MHz for EDR. Resulting in the lowest $\Delta C_{fine\ step} \approx 188\,\text{kHz}$ and 921 kHz for BLE and EDR, respectively. Where again the effect of ΔC_2 is less in BLE than EDR. The fine steps could have been larger to ensure overlap at high frequency with the next $C_{2medium}$ code.

Where to describe a fully digital oscillator the tracking of the frequency as also described in chapter 1 requires integer and fractional bits that select the correct capacitance value based on a select matrix based on row and column logic. As the lower integer bits are encoded to control the column and the upper bits the

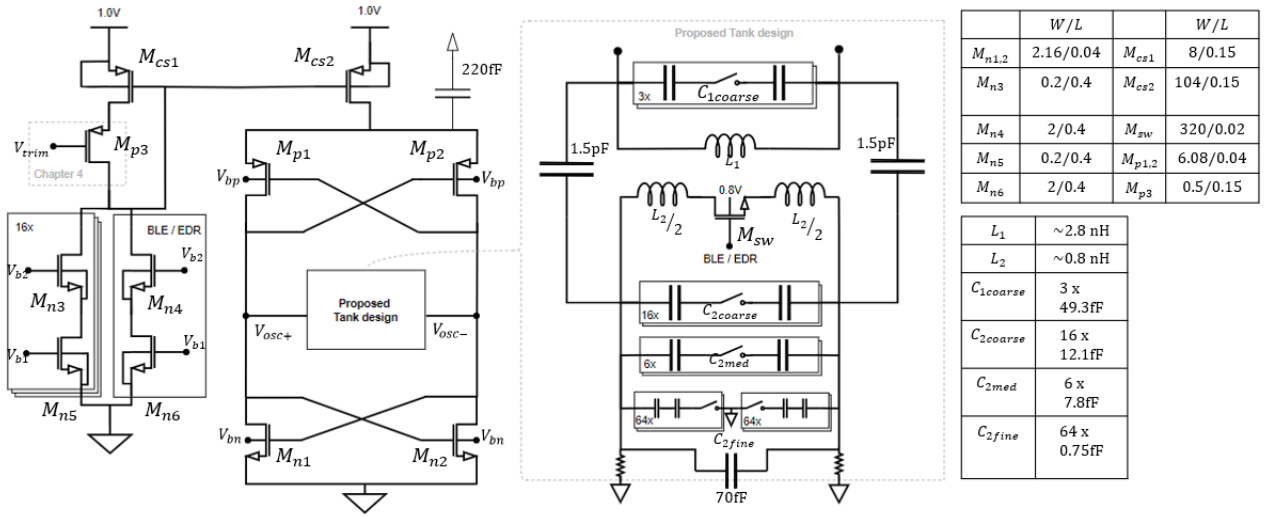
row, a binary-to-unit weight encoder is created [118]. This requires very small fine-tuning units to be in that matrix manner to minimize mismatch. The fully functionality and exact design of the modulation bank are therefore not investigated and only a minimal capacitance of $C_{mod} = 70\text{fF}$ with a $Q_{on} = 50$ is assumed.

To conclude on the capacitors used in this design and verify the assumptions made in Chapter 3, the minimal and maximal capacitance for C_1 and C_2 can be estimated as

$$\begin{aligned} C_{1min} &= C_{par} + C_{1\ coarse} < 0 > \approx 43fF \\ C_{1max} &= C_{par} + C_{1\ coarse} < 3 > \approx 191\,\text{fF} \\ C_{2min} &= C_{2\ coarse} < 0 > + C_{2\ med} < 0 > + C_{2\ fine} < 0 > + C_{mod} \approx 169\,\text{fF} \\ C_{2max} &= C_{2\ coarse} < 16 > + C_{2\ med} < 6 > + C_{2\ fine} < 64 > + C_{mod} \approx 458.8\,\text{fF} \end{aligned} \tag{3.34}$$

where $C_{par} \approx 26.8\,\text{fF}$ are the parasitic capacitance of the cross-coupled devices. Keep in mind that the off parasitic of the switch $C_{SW,OFF}$ also contributes to the C_{2min}, but its contribution is already considered when designing the inductors.

3.7 Performance



	W/L		W/L
$M_{n1,2}$	2.16/0.04	M_{cs1}	8/0.15
M_{n3}	0.2/0.4	M_{cs2}	104/0.15
M_{n4}	2/0.4	M_{sw}	320/0.02
M_{n5}	0.2/0.4	$M_{p1,2}$	6.08/0.04
M_{n6}	2/0.4	M_{p3}	0.5/0.15

L_1	~2.8 nH
L_2	~0.8 nH
$C_{1coarse}$	3 x 49.3fF
$C_{2coarse}$	16 x 12.1fF
C_{2med}	6 x 7.8fF
C_{2fine}	64 x 0.75fF

Figure 3.32: Proposed design with current source, CMOS cross coupled devices and the tank.

With the capacitor bank implemented with the dual mode switch oscillator, the performance of the tank can be assessed. To faciliate oscillation, the CMOS cross-coupled devices are used. Illustration of the proposed DCO is shown in figure 3.32. The $M_{n1,2}$ and $M_{p1,2}$ are sized to generate equal $G_m = g_{mn1,2}/2 + g_{mp1,2}/2$ and to leave enough V_{ds} for the M_{cs2}. RVTH devices with $V_{bp} = 0\,V, V_{bn} = 0\,\mathrm{V}$ are set to have $V_{thn1,2} \approx V_{thp1,2}$ creating the $V_{osc\ opt}$ around 0.42 V.

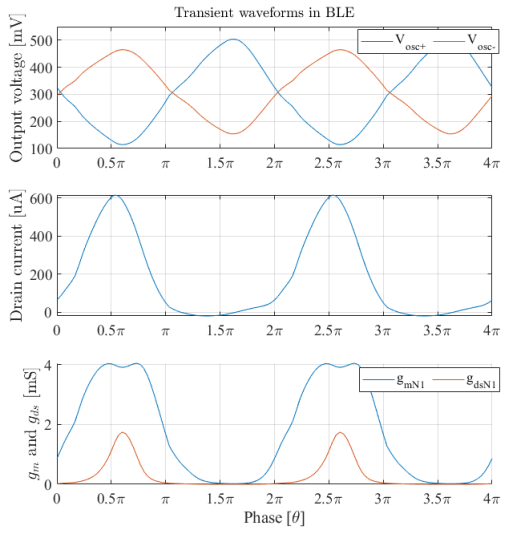


Figure 3.33: Transient PEX simulation BLE at 5.02 GHz with $I_{dco} = 352\,\mu\mathrm{A}$

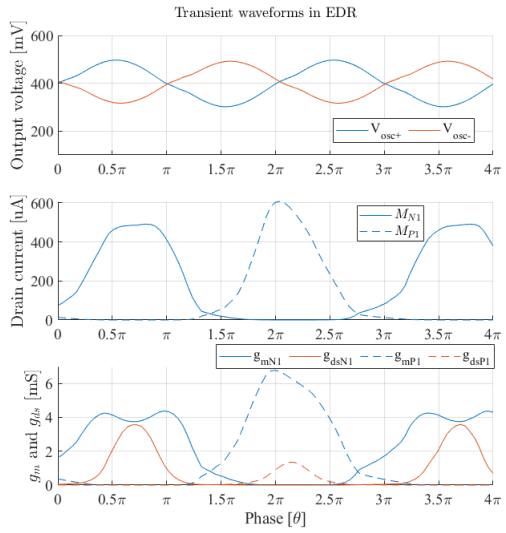


Figure 3.34: Transient PEX simulation EDR at 10.75 GHz with $I_{dco} = 312\,\mu\mathrm{A}$

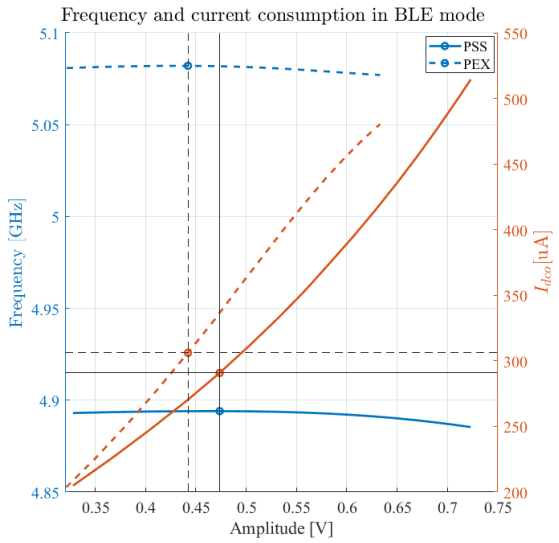


Figure 3.35: BLE frequency and current consumption as function of the amplitude. With active devices biased at $V_{bp} = 0\,\mathrm{V}$ and $V_{bn} = 0\,\mathrm{V}$

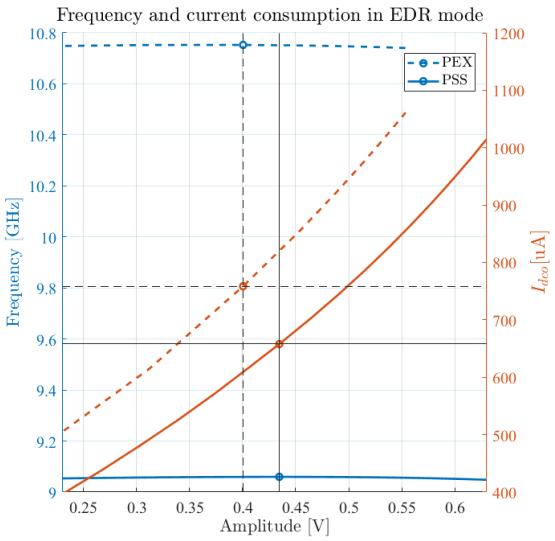


Figure 3.36: EDR frequency and current consumption as function of the amplitude. With active devices biased at $|V_{bp}| = 0\,\mathrm{V}$ and $V_{bn} = 0\,\mathrm{V}$

The figure also illustrates the tunable current source ($M_{n3,4}, M_{n5,6}$) to facilitate various V_{osc} for each mode. The use of M_{p3} will be explained in Chapter 4. The figures 3.33 and 3.34 show the transient simulation of the outputs $V_{osc+,-}$ and the active devices drain current I_{ds} and transconductace g_m and g_{ds}.

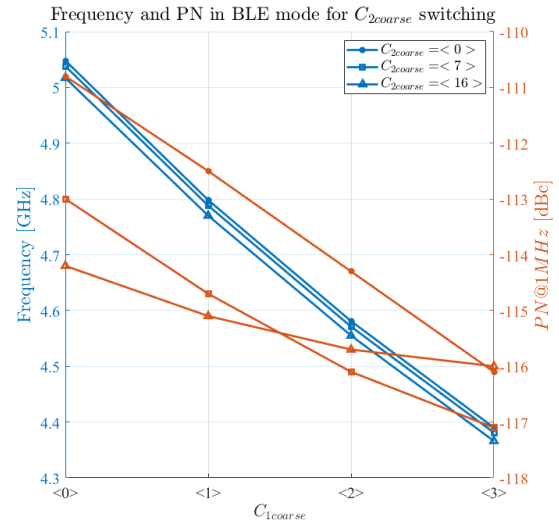


Figure 3.37: BLE frequency and PN as function of the $C_{1coarse}$ and $C_{2coarse}$.

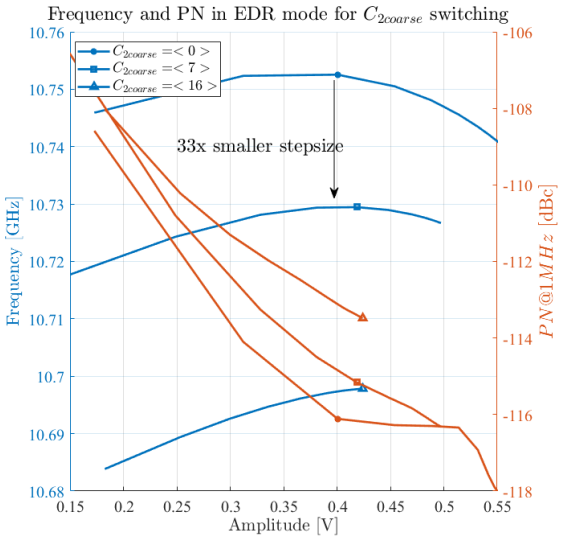


Figure 3.38: EDR frequency and PN as function of the amplitude and $C_{2coarse}$.

The dual mode tank consists of a switch in L_2, which is degraded by the large switch resulting in a $Q_{L_2} = 12.4$. Magnetic coupling has been minimized to save area. Furthermore, C_1 has been minimized to guarantee oscillation at the high frequency band. Each component in the DCO is Layout Versus Schematic (LVS) checked. The layout is not production clean, resulting in layout choices made that in practical design are not possible and might cause more parasitic or losses in the design. For that reason, the LVS designs, referred to as PEX, are compared with the periodic steady-state analysis (PSS) based on the schematic.

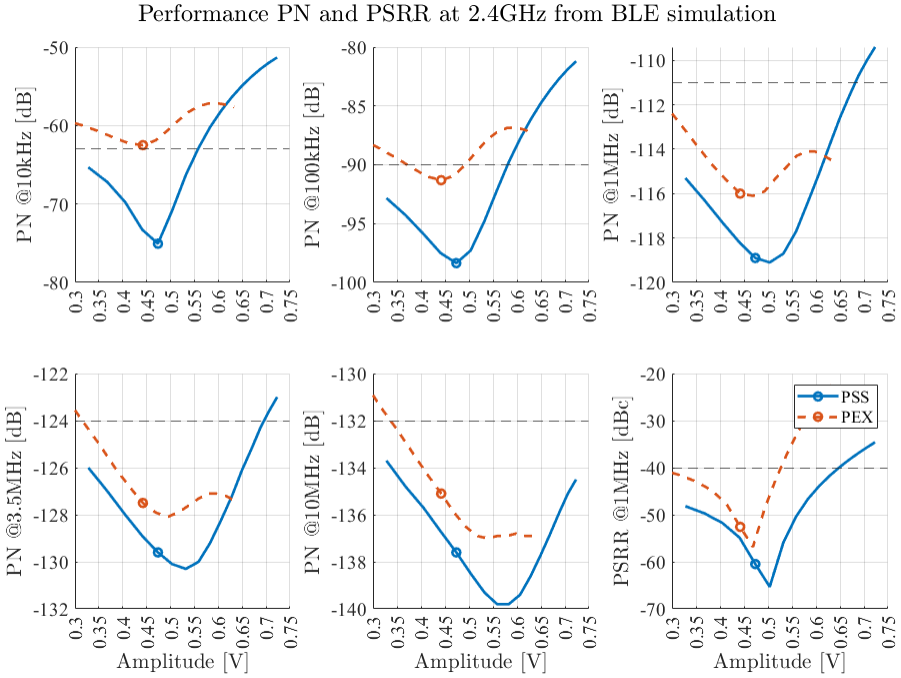


Figure 3.39: BLE PN refereed to 2.4 GHz band at various offsets. Dotted line describes the minimum PN spec

The figures 3.35 and 3.36 show the oscillation frequency over the amplitude for BLE and EDR, respectively. The post-layout simulation shows an approximate 14% increase in power consumption, which is expected to increase further when f_{LO} are equalized. The dot in the figures represent the $V_{osc\ opt}$ at which f_{LO} is maximum and AM-FM is minimized. This optimum is slightly lower than anticipated. A justification could be that all the non-linear capacitance in PEX at the common node or at the output nodes will set the peak frequency at a lower amplitude. The relative large frequency difference in EDR is caused by the problem within C_2. In figure 3.37 and 3.38, the code step from $C_{2\ coarse}$ from 0 to 7 and 16 are shown in PEX. With each code step only a frequency change of around 20 MHz is observed. This does not align with the PSS simulations from Chapter 3.2, which illustrates a change of 660 MHz.

Furthermore, the f_{max} in PSS is set at 11.65 GHz (figure 3.29), while PEX shows an 950 MHz decrease to 10.75 GHz. Similar behavior can be observed in the BLE mode, figure 3.37, where f_{max} is decreased by roughly 900MHz compared to figure 3.29.
When analyzing this reduced f_{max} and compare it with the lumped model, an approximated additional 50 fF

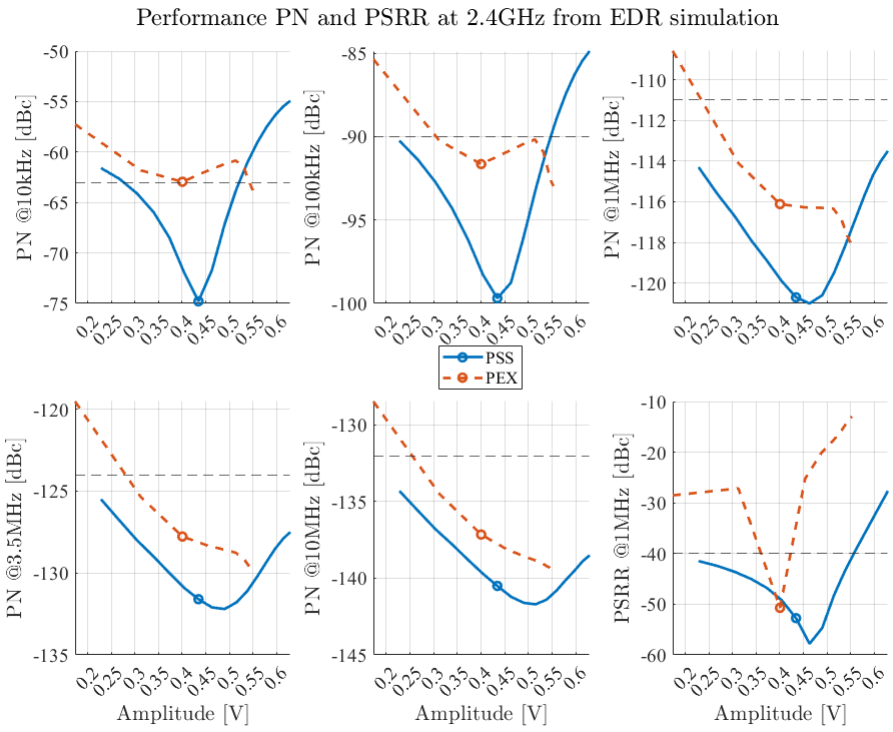


Figure 3.40: EDR PN refereed to 2.4GHz band at various offsets. Dotted line describes the minimum PN spec

has been created in the layout. The significant small step from code 0 to code 7 translates to approximately a step of 2fF. This significantly deviates from the expected $\Delta C_{diff} = 7 \cdot 12.17\,\text{fF}$ (table 3.2) in Chapter 3.2. And since the $C_{1\ coarse}$ steps, shown in figure 3.37, aligns with the PSS step (figure 3.29). Therefore the degraded TR, originates from the C_2 PEX design.
The PN and PSSR performance at the expected 2.4 GHz frequency band is shown in figure 3.39 and 3.40 for BLE and EDR respectively. In these figures, the PEX and PSS designs are compared for various amplitudes. The PEX simulations deviate severely at small offsets and only 1 or 2 dB at higher offsets. The $V_{osc\ opt}$ proves to be truly optimum at low offsets but is still worse than expected by PSS. The large mismatch in $1/f^3$ region could be explained by the PEX taking into account a more uncorrelated modulation functions of low frequency (microscopic) noise sources, where the PSS simulation might take an average modulation response [5]. Yet a more likely mismatch of the PN can come the increased harmonics and non-linear capacitance created by the devices and layout. One could analyze the ISF function Γ and derive the DC component(c_0), to evaluate the extent of the up-conversion factor.
On the other hand the f_{LO} in figure 3.39 and 3.40 is not aligned and is 180 MHz and 1.7 GHz higher in PEX for BLE and EDR respectively, also justifying the increased PN.
PEX simulation show that the increase in PN after $V_{osc\ opt}$ is significantly less. Especially at large offsets. Moreover, the PSRR in BLE seems to align, but not so much in EDR. A close alignment is observed at $V_{osc\ opt}$, which is related to the circuit design of the current source. The exact analysis of the PSRR is addressed in Chapter 4.

To summarize the performance at optimal amplitude between PSS and PEX table 3.3 is given. This

Table 3.3: DCO performance summary at $V_{osc\ opt} = 0.44\,\text{V}$

	BLE		EDR	
	PSS	PEX	PSS	PEX
f_{LO} [GHz]	4.89	5.06	9.05	10.74
I_{dco} [μ A]	290	306	670	765
PN@1MHz [dBc]	-113	-110	-109	-104
PN@1MHz 2.4GHz [dBc]	-119	-116	-121	-116
FoM @ 1MHz	195.87	197.68	189.66	185.58
FoM$_A$ @ $1MHz$ *	208.52	210.33	202.31	198.23
TR [%]	26.76	14.24	27.86	≤ 1

*$FoM_A = FoM + 10log(1mm^2/Area)$

includes the FoM (equation (2.37)). To guarantee the PN requirements, oscillating at amplitude $V_{osc\ opt}$ is preferred. Table 3.3, shows that the 4 dB and 6 dB degradation for PSS and PEX respectively in EDR is caused by the losses of the switch. Yet due to the additional division in EDR mode, the PN performance has an additional -6 dB PN at the 2.4 GHz frequency band. And thus the derived Bluetooth specification (equation (1.1)), is met. However the performance has not been assessed over corners and PVT variations. Furthermore since the required TR for EDR is not achieved in PEX, a full guarantee to achieve the PN over the whole frequency range stays off.

To put the proposed dual mode switched oscillator in perspective comparison is done with state-of-the-art dual mode designs. Only designs with similar frequencies are compared. This design achieves the best FoM with the lowest power consumption and area.

Table 3.4: Dual-mode Oscillator comparison

	This Work	JSSC2011 [119]	ISSCC2008[120]	TCAS2007 [92]	JSCC2009 [93]	JSSC2012 [89]	CECE2011[121]	TCAS2009[122]
Process	22nm FDSOI	90nm CMOS	90nm CMOS	0.13 CMOS	0.25 CMOS	65 CMOS	0.13 CMOS	0.13 CMOS
Frequency[GHz]	5.06-4.38 10.75-10.7	2.55-4.08 4.9-5.75	3.1-4.0 8.8-11.2	3.7-5.5 5.5-7.8	1.94-2.55 3.6-4.77	2.48-3.93 3.31-5.62	4.07-5.52 9.2-12.5	1.28-2.27,2.34-4.03 3.65-6.06
$I_{dco}[mA]$	[0.25-0.47]/[0.5-1.05]	19-21	[1.8-3.5]/[5.6-8.3]	1-8	[1.8-1],[7.5-10.1]	16-24	4	2.8-6.1
$V_{dd}[V]$	1	1.2	1.2	1	1.8	0.6	1.2	1.5
Carrier [GHz]	5.06/10.74	3.31/5.32	3.9/10.9	4.93/6.59	1.94/3.6	3.7/5.52	4.8/10.4	2.26/4.5
PN@1MHz [dBc]	-110/-104	-128/-120	-122*/-117*	-102/-104	-120/-122	-128/-121	-101/101	-120/-117
FoM@1MHz	198/186	194/191	181/181.2	173/173	181/182	189/186	169/175	181/183**
Area $[mm^2]$	0.0543	NA	0.06	NA	$2\cdot(0.35)^2$	0.294	0.076	1
FoM_A@1MHz	210/198	NA	193/193	NA	187/188	195/191	180/186	181/183

*Assumed PN before divided by 2, **Estimated current 4 and 5mA

Chapter 4

Current Source with cascoded ripple replication

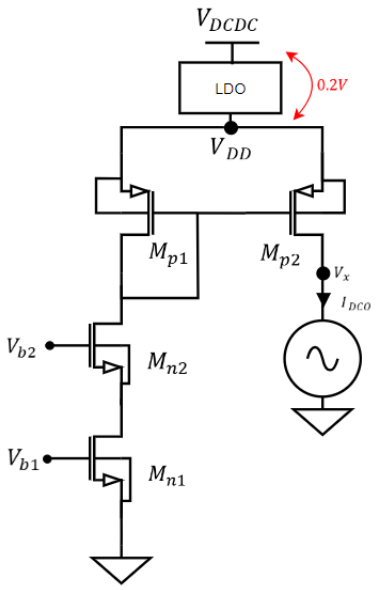


Figure 4.1: Conventional Current mirror topology with cascoded current source (M_{n1}, M_{n2}) with LDO.

Supply lines are distributed across the entire chip system. Fluctuations in the supply voltage can affect every building block in the SoC, including the DCO.
In a conventional supply design, the LDO, depicted in figure 4.1, is used on top of the current mirror of the DCO. This LDO is designed to withstand the noise from the DC-DC supply V_{DCDC}. The noise from V_{DCDC} is due to the switching operation of the converters. This causes a ripple $v_{ripple} = 10\,mV_{pp}$ at $f_{ripple} = 1\,\text{MHz}$ on the V_{DCDC}. Since the LDO consists of a PMOS pass transistor and error amplifier, a supply reduction is imminent. This reduces the supply with 0.2 V from 1 V, resulting in a supply of $V_{dd} = 0.8\,V$. Besides this reduced voltage efficiency, future design supplies will also aim for lower DC-DC voltages to reduce power and scale with technology. This will result in even less supply for the DCO. Therefore, in this Chapter, the focus is on the interference on the supply lines and how, without an LDO still, protection can be maintained. The purpose is to create the power supply rejection ratio (PSRR), in which a spur, not higher than -40 dB

with respect to the carrier, is maintained. Ultimately, this chapter investigates some techniques to enhance the overall resilience of the DCO against variations in the supply and to operate without an LDO regulator.

Other work on supply rejection of the DCO proves rejection by using a replica circuit of the active devices and comparing the common node voltages of the outputs to determine the adjustment of current from the current source. Significant current consumption is required for the replica circuit and the two Operational Transconductance Amplifiers (OTA), resulting in only a supply sensitivity of -30 dB at 1 MHz [123]. In [124], a common mode feedback circuitry is used, resulting in severe loading of the tank, reaching a PSRR of 22 dBc at 1 MHz. In [125], an additional negative feedback, based on a replica load, within the LDO is used to improve supply sensitivity up to -46dB for a ring oscillator. The calibration technique in [126] uses two constant-gm bias circuits, resulting in a high power cancellation for only a spur improvement of 8 dB at 1 MHz. In this work, the fundamental idea of the supply ripple replication from [127] will be adopted, demonstrating excellent PSRR of -54 dBc at $v_{ripple} = 25\,\text{mV}, f_{ripple} = 1\,\text{MHz}$ after foreground calibration.

In this Chapter, first the implications of supply ripple on the DCO will be briefly discussed. Secondly, the cancellation approach will be explained. Third, the replication circuit, different than [127], for cancellation will be discussed. Here, the exact scaling and the analysis of the current source for the dual-mode oscillator will be shown. At last, the Chapter will discuss its discrepancies over oscillation amplitudes and trimming voltages.

4.1 Noise on the Supply and its Pushing effect

Having any change on the supply ΔV_{dd}, as in figure 4.2, results in a change in V_{gs} of the current source M_{p2}, and therefore changes the current I_{dco}. With the known AM-FM effect from Chapter 2.3, both V_{osc} and f_{LO} are also changing. The frequency change by supply variations can be described as

$$\frac{\Delta f_{LO}}{\Delta V_{dd}} = \frac{\Delta f_{LO}}{\Delta I_{dco}} \frac{\Delta I_{dco}}{\Delta V_{dd}}, \tag{4.1}$$

where the first factor has to do with the up-conversion mechanism, described with the effective parasitic capacitance C_{effpar} in Chapter 2.3, and thus plays a crucial role in the case of supply rejection. The second factor has to do with the manner of the current source robustness against the supply, which will be discussed here. Especially in the case of getting the supply directly from the DC-DC converter V_{DCDC}, where the periodic ripple from the charging and discharging of its capacitors disrupts the output spectrum of the oscillator at its relative frequency ($f_{LO} \pm f_{ripple}$).

4.2 Cancelation mechanism

The mechanism to strengthen the DCO against periodic noise from its supply is to cancel it via the current source of the DCO. The equivalent model is illustrated at 4.2.
The aim of the cancelation is to maintain the stability of I_{dco} ($i_{dco} = 0$) across small variations v_{dd}. Instead of applying feedback with a differential amplifier such as in the LDO, one can replicate the same small signal

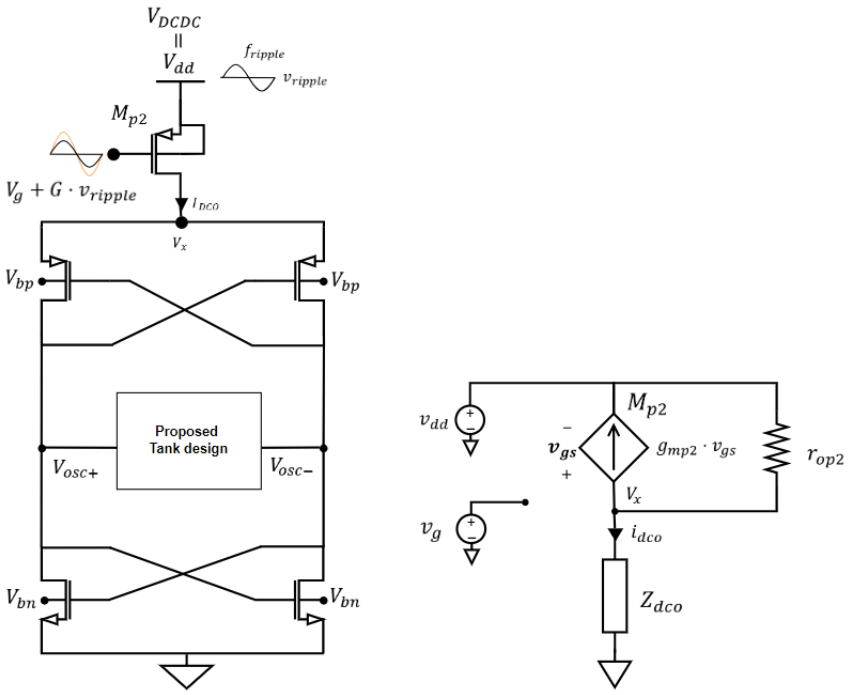


Figure 4.2: The supply ripple replicated on the gate with a gain G on the current source (left) and equivalent model of the current source (right).

on the supply and feed it through the gate V_{gate} of M_{p2}. From the equivalent model of figure 4.2, its supply created current i_{dco} is calculated as follows:

$$i_{dco} = \frac{v_{dd} - v_x}{r_{op2}} - g_{mp2} \cdot v_{gs} \tag{4.2}$$

where v_x, g_{mp2} and r_{op2} are the drain voltage, effective transconductance, and the output resistance of the PMOS M_{p2}, respectively. Given that $v_x = Z_{dco} \cdot i_{dco}$ where Z_{dco} is the equivalent impedance of the cross coupled transistors M_{1-4} and the LC tank [127]. Rewrite (4.2) shows the following relation with v_{dd} and V_{gate}:

$$i_{dco} = \frac{(1 + g_{mp2} \cdot r_{op2})}{r_{op2} + Z_{dco}} v_{dd} - \frac{(g_{mp2} \cdot r_{op2})}{r_{op2} + Z_{dco}} V_{gate} \tag{4.3}$$

One can easily see that still a current is generated when V_{gate} exactly replicates its supply signal ($v_{gs} = 0$) as $r_{op2} \neq \infty$:

$$V_{gate} = G \cdot v_{dd} = v_{dd} \tag{4.4}$$

Described intuitively, M_{p2} experience the channel length modulation described with the square law equation:

$$I_{dco} = \mu_p C_{ox} \frac{W}{2 \cdot L} (|V_{gs}| - V_{thp})^2 \cdot (1 + \lambda |V_{ds} - v_{dd}|) \tag{4.5}$$

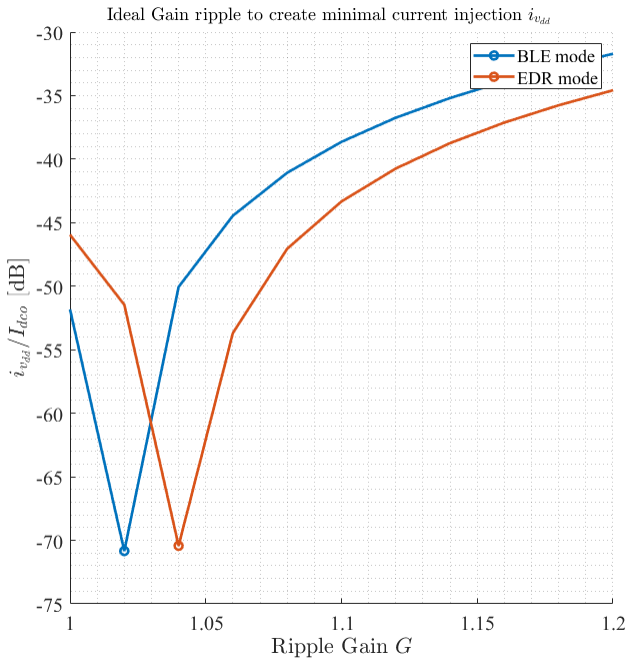


Figure 4.3: Ideal current injection by a 1MHz, 10mV_{pp} supply ripple, with ideal ripple gain on V_{gate}.

Where in the ideal situation $G = 1$, the channel length modulation still causes a small signal current determined by the channel-length modulation parameter λ and its $|V_{ds}|$. To fully cancel the induced current by the supply i_{dco}, caused by V_{ds} variation, the gain optimum G_{opt} is given by

$$G_{opt} \approx 1 + \frac{1}{g_{mp2} \cdot r_{02}} \tag{4.6}$$

Assuming $g_{mp2} \cdot r_{02} \geq 10$ [127] makes that the optimum is only slightly higher than 1. To validate this cancellation, an ideal setup where the normalized current injection ($\frac{i_{dco,v_{dd}}}{I_{dco}}$) caused by supply is simulated and shown in figure 4.3. The figure illustrates that the current induced by the supply ripple reduces up to -70dB for both modes at $G_{opt} = 1.018$ and 1.04 for BLE and EDR, respectively. Following equation (4.6), with the simulated G_{opt} describes that $g_{mp2} \cdot r_{op2} = 55$ and 25 for BLE and EDR respectively.

4.3 Replication circuit

4.3.1 Scaling

The conventional method to bias the current source is illustrated on the left of figure 4.4. Important here is that the current source M_{p2} should be able to generate sufficient current in both BLE and EDR mode. From simulations in Chapter 3.5, the minimum current of I_{DCO} is the order of 300 μA for BLE and at maximum amplitude for EDR, $I_{DCO} = 1000\,\mu$A.
Furthermore, M_{p1} and M_{p2} are thick-oxide (EGSLVT) devices to withstand the 1V power supply, providing

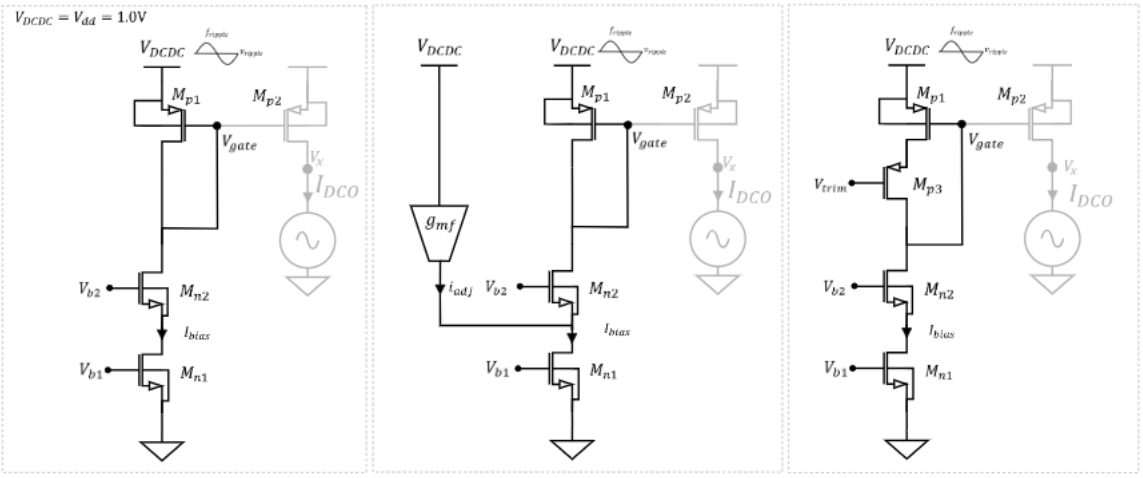


Figure 4.4: Replication circuit containing current mirror (M_{p1}, M_{p2}) with cascoded current source (M_{n1}, M_{n2}): Conventional (left), Circuit from [127] (middle), proposed circuit with M_{p3} (right).

$\mu_p C_{ox} \approx 70 \cdot 10^{-6}[A/V^2]$, which is lower than normal SLVT devices ($\approx 90 \cdot 10^{-6}[A/V^2]$). Moreover, for EGSLVT the V_{thp2} increases to 470 mV.
Use these parameters in equation (4.5) and aiming for a maximum $|V_{ds2}| = 0.25\,\mathrm{V}$, the scaling ratio can be determined

$$\frac{W}{L} = \frac{I_{DCO}}{\mu_p C_{ox} \cdot V_{ov}^2} \approx 550. \tag{4.7}$$

where the overdrive voltage V_{ov} corresponds to 0.12 V and 0.23 V for the minimum and maximum current. From simulations, operating the oscillation amplitude around 0.4 V at each mode approximately doubles the current consumption from BLE to EDR. Resulting in $g_{mp2} = 4.8\,\mathrm{mS}$ and 6.8 mS respectively.

To minimize its power consumption, a mirror ratio of 13 is established. This sets the needed bias current I_{bias} to 23 μA with $g_{mp1} \approx 370\,\mu\mathrm{S}$ for BLE and 42 μA with $g_{mp1} \approx 520\,\mu\mathrm{S}$ for EDR.

4.3.2 Analysis

To replicate the supply ripple on the gate of M_{p2}, the analysis commences with an equivalent current mirror with supply as the input source, as shown in figure 4.5. The voltage gain G from the supply to the V_{gate} starts with KCL:

$$\frac{V_{gate}}{Z_{cs}} - g_{mp1}(V_{gate} - V_{dd}) = \frac{V_{dd} - V_{gate}}{r_{op1}} \tag{4.8}$$

and by rewriting (4.8) results in

$$\frac{V_{gate}}{V_{dd}} = \frac{1 + g_{mp1} \cdot r_{op1}}{1 + g_{mp1} \cdot r_{op1} + \dfrac{r_{op1}}{Z_{mn1,2}}} \tag{4.9}$$

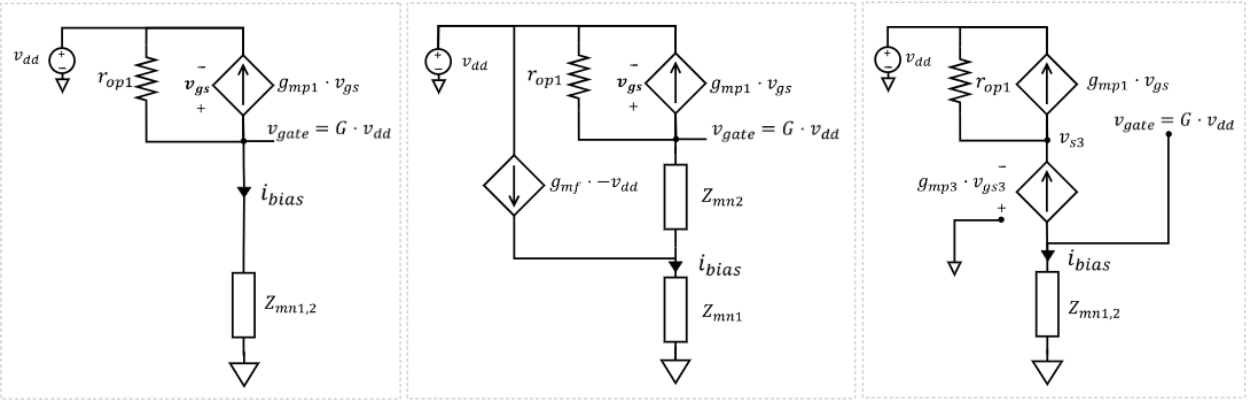


Figure 4.5: Equivalent circuits of the conventional current mirror (left), the circuit from [127] (middle), the proposed circuit with M_{p3} (right).

Equation (4.9) shows that voltage gain $G = 1$ is only achieved when $Z_{mn1,2} \to \infty$. This justifies the advantage of using a cascoded NMOS devices to create the bias currents instead of resistors as there impedance seen from the V_{gate} is significantly higher.

The cascoded current source is used to increase this $Z_{mn1,2}$ to

$$Z_{mn1,2} = (1 + g_{mn2} \cdot r_{on2}) \cdot r_{on1} + r_{on2} \tag{4.10}$$

Yet even with a cascoded current source $G > 1$ is not achieved. In [127] a small tuning current, $i_{adj} \approx g_{m,f} \cdot v_{dd}$, adds an additional gain which in total approximates to

$$G \approx 1 + \frac{g_{m,f}}{g_{mp1}} \tag{4.11}$$

As illustrated in the middle circuit in figure 4.4, I_{adj} marginally reduces the current generated for M_{p1}, which requires extensive calibration to find the correct amount of i_{adj} to get $G = G_{opt}$.

The proposed replica circuit, illustrated on the right of figure 4.4, does not reduce the current of M_{p1}. Instead the M_{p1} is cascoded by transistor M_{p3}. By rough calculation, it can be shown that the voltage gain also achieves the G_{opt} and its gain will always be higher than 1, which is not the case in [127], and therefore a lower supply induced current $i_{v_{dd}}$ can be guaranteed.
The analysis starts with KCL at node V_{gate} from the right equivalent model of figure 4.5

$$\frac{V_{gate}}{Z_{mn1,2}} = g_{mp3} \cdot V_{s3}, \tag{4.12}$$

where for simplicity M_{p3} output resistance r_{op3} is neglected. Together with KCL at node V_{s3}

$$g_{mp1} \cdot (V_{gate} - V_{dd}) = g_{mp3}(-V_{s3}) - \frac{V_{s3} - V_{dd}}{r_{op1}} \tag{4.13}$$

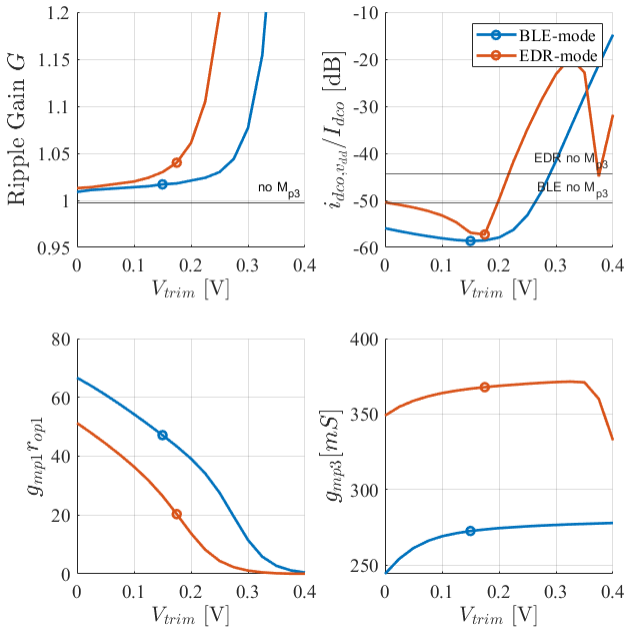


Figure 4.6: The effect on gain ripple G, current injection ratio $\frac{i_{dco,v_{dd}}}{I_{dco}}$, the $g_{mp1}r_{op1}$ product and the g_{mp3} over various gate voltages at M_{p3}.

creates the following voltage gain by replacing V_{s3} from (4.13) with (4.12):

$$\frac{V_{gate}}{V_{dd}} = \frac{g_{mp3} \cdot Z_{mn1,2} + g_{mp1} \cdot r_{op1} \cdot g_{mp3} \cdot Z_{mn1,2}}{g_{mp3} \cdot r_{op1} + 1 + g_{mp1} \cdot r_{op1} \cdot g_{mp3} \cdot Z_{mn1,2}} \tag{4.14}$$

which approximates to

$$\frac{V_{gate}}{V_{dd}} \approx 1 + \frac{1}{g_{mp1} \cdot r_{op1}} \tag{4.15}$$

given that $g_{mp3} \cdot Z_{mn1,2} >> (g_{mp3} \cdot r_{op1} + 1)$. Based on the G_{opt} from equation (4.6) and the approximation made in (4.15):

$$g_{mp1} \cdot r_{op1} \approx g_{mp2} \cdot r_{op2} \tag{4.16}$$

With the mirror ratio of 13, whereby the g_{mp1} is reduced by a factor of 13 compared to g_{mp2}, r_{op1} must be increased by a factor of 13 relative to r_{op2} to satisfy equation (4.16).

In the conventional current mirror situation, M_{p1} is typically diode-connected. Consequently, its product given by $g_{mp1} \cdot r_{op1} \approx 80$ due to the large $|V_{ds1}|$. Yet by implementing the M_{p3} transistor, a difference between the $|V_{ds1}|$ and $|V_{gs1}|$ is created. Meaning that with the same overdrive voltage of M_{p1}, a lower $|V_{ds1}|$ is created, which lowers the r_{op1}. This can be observed in figure 4.6.

In where the two top figures show again the gain G and the ratio $i_{dco,v_{dd}}/I_{dco}$ for increasing V_{trim}. The minimal ratio $i_{dco,v_{dd}}/I_{dco}$ for each mode corresponds to ideal gain as shown in figure 4.3. The simulated product $g_{mp1} \cdot r_{op1}$ proves the decrease with V_{trim} and corresponds to the optimum with a value of 48 and 20 for BLE and EDR, respectively. Driving it with too much gate voltage or size M_{p3} too large results in

$g_{mp1} \cdot r_{op1}$ so low, $G > G_{opt}$ and will bring M_{p1} and M_{p2} out of saturation.

More intuitively, M_{p3} acts like a "tuner" of the $|V_{ds1}|$ as can be seen in equation (4.12). Since M_{p3} operates in saturation region, a $V_{ds3} \geq 0.1\,\mathrm{V}$ is required. Consequently, as V_{trim} is increased, the V_{gate} experiences a slight decrease. This results in an increased overdrive voltage for both M_{p1} and M_{p2}, thereby lowering $g_{mp1,2}$ and increasing the current I_{dco}. Meanwhile, in small-signal conditions, M_{p3} enhances the supply ripple.

As shown in equation (4.16), the simulations show that the products of M_{p1} and M_{p2} (48 and 55 for BLE, and 20 and 25 for EDR) are roughly aligned. The slight discrepancy is expected, as both equations are approximations. The deviations arise due to the exact determination of $g_{mp2} \cdot r_{op2}$, which fluctuates with oscillation amplitudes.

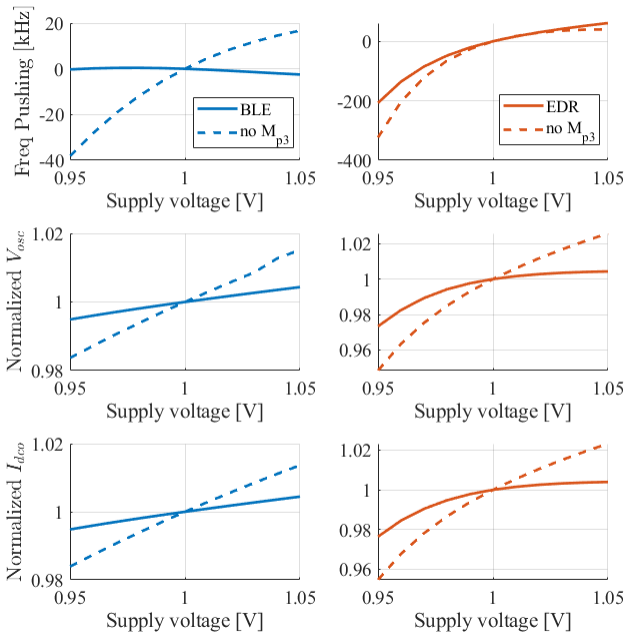
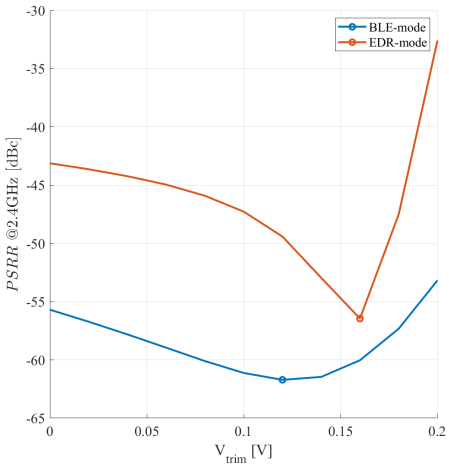


Figure 4.7: The change in frequency, oscillation amplitude and current over supply change.

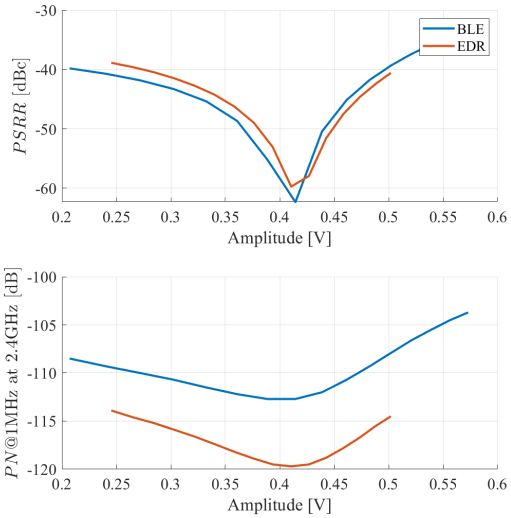
This validates that G_{opt} indeed results in the minimal injected current caused by the ripple in the DCO. It improves the $i_{dco,v_{dd}}$ with 8.1 dB to -58.1 dB and 12.9 dB to -57.3 dB for BLE and EDR respectively. This G_{opt} is ascertained by $g_{mp2} \cdot r_{op2}$ and is achieved by reducing the $g_{mp1} \cdot r_{op1}$ product.

To further demonstrate its additional capabilities instead of using a standard current mirror, the supply in figure 4.7 is altered to exhibit its variations in frequency (frequency pushing), amplitude(V_{osc}) and its current (I_{dco}). It shows an improved frequency pushing from 0.593MHz/V to 0.025MHz/V in BLE and 0.363MHz/V to 0.268MHz/V in EDR.

4.4 Amplitude dependency



(a) PSRR as a function of gate voltage of M_{p3}.



(b) PSRR and PN as a function of different oscillation amplitudes. M_{p3} is biased at optiaml V_{trim}. $V_{bp} = 0\,V$ and $V_{bn} = 0\,V$

Figure 4.8

Creating the lowest injected current $i_{dco,v_{dd}}$ does not guarantee a low power supply rejection ratio (PSRR). The PSRR in this work is notated as the spur relative to the output amplitude:

$$PSRR = 20\log\left(\frac{V_{osc,v_{dd}}(f_{LO} \pm f_{ripple})}{V_{osc}(f_{LO})}\right)[dBc] \tag{4.17}$$

Here, the V_{osc} and $V_{osc,v_{dd}}$ are determined by the current I_{bias} and i_{bias} respectively. However, it is important that the generated ripple current does not get up-converted to $f_{osc} \pm f_{rippel}$ frequency. Known from Chapter 2.3 is that this up-conversion is determined by the optimal amplitude $V_{osc,opt}$. So, to actually minimize PSRR, one should consider

$$PSRR_{min} \propto MIN\Big(K_{AM-FM}(V_{osc,opt}), i_{dco,v_{dd}}(G_{opt})\Big) \tag{4.18}$$

where K_{AM-FM} is the up-conversion factor described in equation (2.29). Equation (4.18) describes with the K_{AM-FM} both the oscillation amplitude and replica gain need to be optimal to create the best PSRR. In figure 4.8a its PSRR is shown over the V_{trim} and aligns with figure 4.6. However, figure 4.8b, where the PSRR differs per amplitude, shows, even though it is optimized by V_{trim}, a significant increase in PSRR before and after $V_{osc\ opt}$. It describes that $V_{osc\ opt}$ is more crucial to PSRR than achieving the exact gain ripple G_{opt}. In other words, the up-conversion factor K_{AM-FM} at 1 MHz remains substantial in this LC tank.

In summarizing the performance of the proposed replica circuit, it surpasses the required PSRR of -40dBc.

However, when operating at a frequency of 10GHz, the PSRR experiences degradation due to the higher g_{mp2}. The significance of this ripple replication implementation lies in its dependency on the oscillation amplitude. Any deviation from the AM-FM optimum results in a reduction of its supply rejection. This effect worsen when the replica circuit is layed out(PEX) as was observed in the figures 3.40 and 3.39 from Chapter 3.7. Moreover the layout will most likely cause more parasitic capacitance, which causes mismatch between the gate and source of M_{p2} to effectively cancel the ripple of the supply. By applying trimming, the exact G_{opt} can be guaranteed through the adjustment of the gate voltage M_{p3}. This shows the design has identical functionalities as those proposed in [127], where also calibration is implemented. In this particular circuit, the assurance of $G > 1$ is advantageous. Although its performance is not better than that of [127] since that current source does not have to facilitate a wider range of currents and uses an implicit common mode resonance tank that minimizes the up-conversion. It demonstrates a proven utility for future developments when the V_{DCDC} is set below 1V, and thus, an LDO takes up too much voltage headroom.

Chapter 5

Conclusion and future work

In this thesis, the design of a DCO for Bluetooth BLE/EDR is provided. With all sorts of state-of-the-art LC oscillator designs and different classes, a complementary class B provides sufficient amplitude at a relatively high current efficiency at a supply of 0.8 or 1.0 V. A detailed analysis of active devices revealed their contribution to the AM-FM up-conversion. Analysis shows besides the C_{gs} and C_{gd} of the cross-coupled devices, the contribution of capacitance at the common node also contribute to the frequency change over amplitude. Moreover, the study showed that the oscillation amplitude at V_{th}, provides maximal tolerance to AM-FM. Based on the V_{th}, the active devices have been designed and adjusted by the backgate bias to create a minimal PN performance at very low power dissipation.

To mitigate the well-known self-interference, PA-to-DCO pulling, a dual-mode oscillator is designed. Where in the first mode (BLE), the frequency of the DCO is at twice the receiving frequency $f_{LO} = 4.8\,\text{GHz}$. To further mitigate the PA-to-DCO pulling, the second mode (EDR) operates at 4 times the receiving signal $f_{LO} = 9.6\,\text{GHz}$. To maintain low power in both modes, a decoupled switch, capacitance and inductor have been added to the LC tank. The decoupling capacitors enabled minimal switch loss and allowed minimal capacitance at the output. Different inductor layouts have been attempted to minimize area. As a low coupling required a too-large area and a high coupling increased the power in BLE mode, the two inductors have been separated. The separation left enough space to accommodate the tuning capacitors, current source and active devices. This eventually led to the smallest area of $0.0543mm^2$ compared to other dual-mode operating in the same frequency range. The switch degraded the inductors quality factor by 4.1 but nonetheless the current consumption at a 1V supply for BLE and EDR mode are $306\,\mu A$ and $765\,\mu A$ respectively. This is also the lowest simulated current consumption compared with published dual-mode designs.

Furthermore, an attempt to leave out the LDO is shown, whereby the current source tries to cancel the low-frequency supply ripple. It provides sufficient PSRR (-51.5/-50.5 dBc for BLE/EDR) as long as the optimal AM-FM amplitude is guaranteed. The PN performance of the dual mode at optimal amplitude achieved -110 and -104 dBc/Hz at 1MHz offset with a carrier frequency of 5.06 and 10.74GHz, respectively. The layout that is done, degraded the PN and TR severely; The TR was expected to be 26.76% and 27.86% but resulted in only a 14.24% and 1% for BLE and EDR mode respectively. These unfortunate post-layout results should in future work be resolved to have this dual mode DCO meet the requirements for further

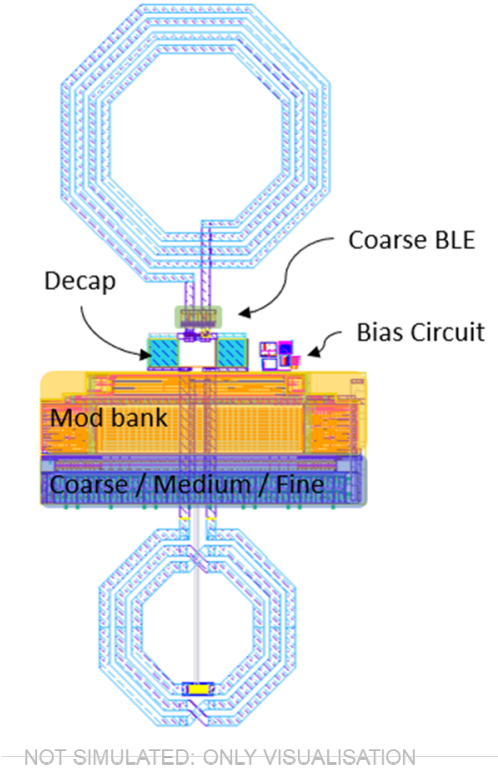


Figure 5.1: Visualization of a possible layout, where all the components fit in between the inductors.

implementation in a Bluetooth Transceiver.

In future work, the completion of the DCO should include designing the modulation bank to enable frequency locking. An illustration of its expected layout is given in figure 5.1. Then design the two dividers and integrate them with the PAs and RFIO to verify the reduced PA-DCO coupling in EDR mode. Additionally, integrating the design with the ADPLL will validate the calibration method to operate at $V_{osc\ opt}$.

Bibliography

[1] *2022 Market Update — Bluetooth® Technology Website*. URL: https://www.bluetooth.com/2022-market-update/.

[2] Andrew Zignani. *LE Audio: The Future of Bluetooth® Audio*. Tech. rep. 2022, p. 19.

[3] *Bluetooth Specification Core amended v5.4*. Tech. rep. Bluetooth SIG, 2024, p. 3141.

[4] Alessandra Pipino et al. "Bluetooth Low Energy Receiver System Design". In: ().

[5] Neda Nouri. *A low Phase-Noise MM-wave oscillator and its application in a low-power polar transmitter*. Tech. rep. 2011. DOI: 10.14288/1.0072418. URL: https://open.library.ubc.ca/soa/cIRcle/collections/ubctheses/24/items/1.0072418.

[6] Mark Pude et al. "Maximum intrinsic gain degradation in technology scaling". In: *2007 International Semiconductor Device Research Symposium, ISDRS*. 2007. ISBN: 1424418917. DOI: 10.1109/ISDRS.2007.4422541.

[7] Masoud Babaie, Mina Shahmohammadi, and Robert Bogdan Staszewski. *RF CMOS oscillators for modern wireless applications*. River Publishers Series in Circuits and Systems. URL: www.riverpublishers.com.

[8] Gordon Moore. "Chapter 7 • MOSFETs in ICs-Scaling, Leakage, and Other Topics". In.

[9] Jan Hoentschel et al. *22FDX ® Technologies for Ultra-Low Power IoT, RF and mmWave Applications Technologies 22FDX® pour les Applications très basse puissance IoT, RF et Ondes Millimétriques*. Tech. rep. 2019.

[10] Qian Xie et al. "Comprehensive analysis of short-channel effects in ultrathin SOI MOSFETs". In: *IEEE Transactions on Electron Devices* 60.6 (2013), pp. 1814–1819. ISSN: 00189383. DOI: 10.1109/TED.2013.2255878.

[11] Tim Seiler et al. "Investigation of advanced FDSOI CMOS devices for analog/mixed signal applications". In: ().

[12] Gabriele Manganaro and Domine Leenaerts. *Advances in Analog and RF IC Design for Wireless Communication Systems*. Elsevier Inc., 2013. ISBN: 9780123983268. DOI: 10.1016/C2011-0-08437-5.

[13] Roman Staszewski et al. "Software assisted digital RF processor (DRP) for single-chip GSM radio in 90 nm CMOS". In: *IEEE Journal of Solid-State Circuits* 45.2 (Feb. 2010), pp. 276–288. ISSN: 00189200. DOI: 10.1109/JSSC.2009.2036763.

[14] Khurram Muhammad, Robert Bogdan Staszewski, and Dirk Leipold. "Digital RF processing: Toward low-cost reconfigurable radios". In: *IEEE Communications Magazine* 43.8 (Aug. 2005), pp. 105–113. ISSN: 01636804. DOI: 10.1109/MCOM.2005.1497564.

[15] Robert Bogdan Staszewski et al. "All-digital TX frequency synthesizer and discrete-time receiver for Bluetooth radio in 130-nm CMOS". In: *IEEE Journal of Solid-State Circuits*. Vol. 39. 12. Dec. 2004, pp. 2278–2291. DOI: 10.1109/JSSC.2004.836345.

[16] Ming Ding et al. "A 0.8V 0.8mm2 bluetooth 5/BLE digital-intensive transceiver with a 2.3mW phase-tracking RX utilizing a hybrid loop filter for interference resilience in 40nm CMOS". In: *Digest of Technical Papers - IEEE International Solid-State Circuits Conference*. Vol. 61. Institute of Electrical and Electronics Engineers Inc., Mar. 2018, pp. 446–448. ISBN: 9781509049394. DOI: 10.1109/ISSCC.2018.8310376.

[17] Akihide Sai et al. "A 5.5 mW ADPLL-Based Receiver with a Hybrid Loop Interference Rejection for BLE Application in 65 nm CMOS". In: *IEEE Journal of Solid-State Circuits* 51.12 (Dec. 2016), pp. 3125–3136. ISSN: 00189200. DOI: 10.1109/JSSC.2016.2603993.

[18] Yao Hong Liu et al. "A 770pJ/b 0.85V 0.3mm2 DCO-based phase-tracking RX featuring direct demodulation and data-aided carrier tracking for IoT applications". In: *Digest of Technical Papers - IEEE International Solid-State Circuits Conference*. Vol. 60. Institute of Electrical and Electronics Engineers Inc., Mar. 2017, pp. 408–409. ISBN: 9781509037575. DOI: 10.1109/ISSCC.2017.7870434.

[19] Yao-Hong Liu et al. "Design and Analysis of a DCO-Based Phase-Tracking RF Receiver for IoT Applications". In: *IEEE Journal of Solid-State Circuits* 54.3 (2019), p. 785. DOI: 10.1109/JSSC.2018.2883398.

[20] Jan Prummel et al. "A 10 mW Bluetooth Low-Energy Transceiver with On-Chip Matching". In: *IEEE Journal of Solid-State Circuits* 50.12 (Dec. 2015), pp. 3077–3088. ISSN: 00189200. DOI: 10.1109/JSSC.2015.2469674.

[21] Kenichi Shibata et al. "A 22nm 0.84mm2BLE Transceiver With Self IQ-Phase Correction Achieving 39dB Image Rejection and on-Chip Antenna Impedance Tuning". In: *Digest of Technical Papers - IEEE International Solid-State Circuits Conference*. Vol. 2022-February. Institute of Electrical and Electronics Engineers Inc., 2022, pp. 398–400. ISBN: 9781665428002. DOI: 10.1109/ISSCC42614.2022.9731558.

[22] Zheng Sun et al. "A 0.85mm2 BLE Transceiver with Embedded T/R Switch, 2.6mW Fully-Passive Harmonic Suppressed Transmitter and 2.3mW Hybrid-Loop Receiver". In: *ESSCIRC 2018 - IEEE 44th European Solid State Circuits Conference*. Institute of Electrical and Electronics Engineers Inc., Oct. 2018, pp. 310–313. ISBN: 9781538654040. DOI: 10.1109/ESSCIRC.2018.8494276.

[23] Masahisa Tamura et al. "A 0.5V BLE Transceiver with a 1.9mW RX Achieving -96.4dBm Sensitivity and 4.1dB Adjacent Channel Rejection at 1MHz Offset in 22nm FDSOI". In: *Digest of Technical Papers - IEEE International Solid-State Circuits Conference*. Vol. 2020-February. Institute of Electrical and Electronics Engineers Inc., Feb. 2020, pp. 468–470. ISBN: 9781728132044. DOI: 10.1109/ISSCC19947.2020.9063021.

[24] Hanli Liu et al. “An ADPLL-centric bluetooth low-energy transceiver with 2.3mW interference-tolerant hybrid-loop receiver and 2.9mW single-point polar transmitter in 65nm CMOS”. In: *Digest of Technical Papers - IEEE International Solid-State Circuits Conference* 61 (Mar. 2018), pp. 444–446. ISSN: 01936530. DOI: 10.1109/ISSCC.2018.8310375.

[25] Yao Hong Liu et al. “A 1.9nJ/b 2.4GHz multistandard (Bluetooth low energy/Zigbee/IEEE802.15.6) transceiver for personal/body-area networks”. In: *Digest of Technical Papers - IEEE International Solid-State Circuits Conference*. Vol. 56. 2013, pp. 446–447. ISBN: 9781467345132. DOI: 10.1109/ISSCC.2013.6487808.

[26] Tomohiro Sano et al. “A 6.3mW BLE transceiver embedded RX image-rejection filter and TX harmonic-suppression filter reusing on-chip matching network”. In: *Digest of Technical Papers - IEEE International Solid-State Circuits Conference*. Vol. 58. Institute of Electrical and Electronics Engineers Inc., Mar. 2015, pp. 240–241. ISBN: 9781479962235. DOI: 10.1109/ISSCC.2015.7063015.

[27] Ahmed Magdy et al. “Low power, dual mode bluetooth 5.1/bluetooth low energy receiver design”. In: *Proceedings - IEEE International Symposium on Circuits and Systems*. Vol. 2021-May. Institute of Electrical and Electronics Engineers Inc., 2021. ISBN: 9781728192017. DOI: 10.1109/ISCAS51556.2021.9401748.

[28] Yao Hong Liu et al. “A 1.2nJ/b 2.4GHz receiver with a sliding-IF phase-to-digital converter for wireless personal/body-area networks”. In: *Digest of Technical Papers - IEEE International Solid-State Circuits Conference*. Vol. 57. Institute of Electrical and Electronics Engineers Inc., 2014, pp. 166–167. ISBN: 9781479909186. DOI: 10.1109/ISSCC.2014.6757384.

[29] Feng Wei Kuo et al. “A Bluetooth low-energy (BLE) transceiver with TX/RX switchable on-chip matching network, 2.75mW high-IF discrete-time receiver, and 3.6mW all-digital transmitter”. In: *IEEE Symposium on VLSI Circuits, Digest of Technical Papers*. Vol. 2016-September. Institute of Electrical and Electronics Engineers Inc., Sept. 2016. ISBN: 9781509006342. DOI: 10.1109/VLSIC.2016.7573480.

[30] Ruifeng Liu and Russell Mohn. “A +12dBm Output Power and-97.5dBm Sensitivity 2.4G/5.8GHz BLE/BT Compliant Transceiver with RX/TX Co-Matching using Bondwires”. In: *Proceedings - IEEE International Symposium on Circuits and Systems*. Vol. 2022-May. Institute of Electrical and Electronics Engineers Inc., 2022, pp. 236–239. ISBN: 9781665484855. DOI: 10.1109/ISCAS48785.2022.9937793.

[31] Wei Yang et al. “A +8dBm BLE/BT transceiver with automatically calibrated integrated RF bandpass filter and -58dBc TX HD2”. In: *Digest of Technical Papers - IEEE International Solid-State Circuits Conference*. Vol. 60. Institute of Electrical and Electronics Engineers Inc., Mar. 2017, pp. 136–137. ISBN: 9781509037575. DOI: 10.1109/ISSCC.2017.7870298.

[32] Alireza Zolfaghari et al. “A multi-mode WPAN (Bluetooth, BLE, IEEE 802.15.4) SoC for low-power and IoT applications”. In: *IEEE Symposium on VLSI Circuits, Digest of Technical Papers*. Institute of Electrical and Electronics Engineers Inc., Aug. 2017, pp. C74–C75. ISBN: 9784863486065. DOI: 10.23919/VLSIC.2017.8008554.

[33] Brian Miller and Robert J. Conley. "A Multiple Modulator Fractional Divider". In: *IEEE Transactions on Instrumentation and Measurement* 40.3 (1991), pp. 578–583. ISSN: 15579662. DOI: 10.1109/19.87022.

[34] Michael H. Perrott, Theodore L. Tewksbury, and Charles G. Sodini. "A 27-mW CMOS fractional-N synthesizer using digital compensation for 2.5-Mb/s GFSK modulation". In: *IEEE Journal of Solid-State Circuits* 32.12 (Dec. 1997), pp. 2048–2059. ISSN: 00189200. DOI: 10.1109/4.643663.

[35] Manoj Gupta and Bang Sup Song. "A 1.8-GHz spur-cancelled fractional-N frequency synthesizer with LMS-based DAC gain calibration". In: *IEEE Journal of Solid-State Circuits*. Vol. 41. 12. Dec. 2006, pp. 2842–2850. DOI: 10.1109/JSSC.2006.884829.

[36] Chun Ming Hsu, Matthew Z. Straayer, and Michael H. Perrott. "A low-noise wide-BW 3.6-GHz digital $\Delta\Sigma$ fractional-N frequency synthesizer with a noise-shaping time-to-digital converter and quantization noise cancellation". In: *IEEE Journal of Solid-State Circuits*. Vol. 43. 12. Dec. 2008, pp. 2776–2786. DOI: 10.1109/JSSC.2008.2005704.

[37] Michael H Perrott. *Tutorial on Digital Phase-Locked Loops CICC 2009*. Tech. rep. 2009.

[38] Robert Bogdan Staszewski et al. "All-digital PLL and transmitter for mobile phones". In: *IEEE Journal of Solid-State Circuits*. Vol. 40. 12. Dec. 2005, pp. 2469–2480. DOI: 10.1109/JSSC.2005.857417.

[39] Stephane Bronckers et al. "Experimental analysis of the coupling mechanisms between a 4 GHz PPA and a 5-7 GHz LC-VCO". In: *IEEE Transactions on Instrumentation and Measurement*. Vol. 58. 8. 2009, pp. 2706–2713. DOI: 10.1109/TIM.2009.2015705.

[40] Nisha Checka, Anantha Chandrakasan, and Rafael Reif. "Substrate noise analysis and experimental verification for the efficient noise prediction of a digital PLL". In: *Proceedings of the Custom Integrated Circuits Conference*. Vol. 2005. Institute of Electrical and Electronics Engineers Inc., 2005, pp. 473–476. ISBN: 0780390237. DOI: 10.1109/CICC.2005.1568709.

[41] Tony Yeung et al. "Noise coupling in heavily and lightly doped substrate from planar spiral inductor". In: *Proceedings - IEEE International Symposium on Circuits and Systems*. Vol. 2. IEEE, 1997, pp. 1405–1408. DOI: 10.1109/iscas.1997.622158.

[42] Oren Eytan Eliezer et al. "A phase domain approach for mitigation of self-interference in wireless transceivers". In: *IEEE Journal of Solid-State Circuits*. Vol. 44. 5. May 2009, pp. 1436–1453. DOI: 10.1109/JSSC.2009.2014941.

[43] Nagarajan Mahalingam et al. "A Fully Integrated Pulling Mitigation Synthesizer for NB-IoT Transmitter". In: *IEEE Transactions on Microwave Theory and Techniques* 71.12 (Dec. 2023), pp. 5221–5232. ISSN: 15579670. DOI: 10.1109/TMTT.2023.3277966.

[44] Jonathan P. Comeau et al. "An exploration of substrate coupling at K-band between a SiGe HBT power amplifier and a SiGe HBT voltage-controlled-oscillator". In: *IEEE Microwave and Wireless Components Letters* 17.5 (May 2007), pp. 349–351. ISSN: 15311309. DOI: 10.1109/LMWC.2007.895703.

[45] Ahmad Mirzaei and Hooman Darabi. "Pulling mitigation in wireless transmitters". In: *IEEE Journal of Solid-State Circuits* 49.9 (2014), pp. 1958–1970. ISSN: 00189200. DOI: 10.1109/JSSC.2014.2325556.

[46] Chieh Hsun Hsiao et al. "Analysis and improvement of direct-conversion transmitter pulling effects in constant envelope modulation systems". In: *IEEE Transactions on Microwave Theory and Techniques*. Vol. 58. 12 PART 2. Dec. 2010, pp. 4137–4146. DOI: 10.1109/TMTT.2010.2087351.

[47] Giuseppe Li Puma, Rotem Avivi, and Christophe Carbonne. "Adaptive techniques to mitigate oscillator pulling in radio transmitters". In: *IEEE Transactions on Circuits and Systems II: Express Briefs* 64.2 (Feb. 2017), pp. 121–125. ISSN: 15583791. DOI: 10.1109/TCSII.2016.2552143.

[48] Cheng Ru Ho and Mike Shuo Wei Chen. "A digital frequency synthesizer with dither-assisted pulling mitigation for simultaneous DCO and reference path coupling". In: *Digest of Technical Papers - IEEE International Solid-State Circuits Conference*. Vol. 61. Institute of Electrical and Electronics Engineers Inc., Mar. 2018, pp. 254–256. ISBN: 9781509049394. DOI: 10.1109/ISSCC.2018.8310280.

[49] Imran Bashir et al. "A novel approach for mitigation of RF oscillator pulling in a polar transmitter". In: *IEEE Journal of Solid-State Circuits* 46.2 (Feb. 2011), pp. 403–415. ISSN: 00189200. DOI: 10.1109/JSSC.2010.2096110.

[50] Hooman Darabi et al. "A 2.4-GHz CMOS transceiver for bluetooth". In: *IEEE Journal of Solid-State Circuits* 36.12 (Dec. 2001), pp. 2016–2024. ISSN: 00189200. DOI: 10.1109/4.972152.

[51] Jaewon Choi and Nam Seog Kim. "A Spurious and Oscillator Pulling Free CMOS Quadrature LO-Generator for Cellular NB-IoT". In: *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 29.12 (Dec. 2021), pp. 2098–2109. ISSN: 15579999. DOI: 10.1109/TVLSI.2021.3105819.

[52] Litong Liu et al. "A Multi-Modulus Fractional Divider with TDC Free Calibration Scheme for Mitigation of TX-VCO Pulling". In: *IEEE Transactions on Circuits and Systems II: Express Briefs* 67.12 (Dec. 2020), pp. 2848–2852. ISSN: 15583791. DOI: 10.1109/TCSII.2020.2983785.

[53] Yue Wu et al. "Suppression of VCO pulling effects using even-harmonic quiet transmitting circuits". In: *European Solid-State Circuits Conference*. Vol. 2015-October. IEEE Computer Society, Oct. 2015, pp. 128–131. ISBN: 9781467374705. DOI: 10.1109/ESSCIRC.2015.7313845.

[54] Zaid Aboush et al. "Integrated circuit field canceller system suitable for highly integrated connectivity transceivers". In: *EuMIC 2016 - 11th European Microwave Integrated Circuits Conference*. Institute of Electrical and Electronics Engineers Inc., Dec. 2016, pp. 5–8. ISBN: 9782874870446. DOI: 10.1109/EuMIC.2016.7777474.

[55] Rishad Ahmed Shafik et al. "On the Extended Relationships Among EVM, BER and SNR as Performance Metrics". In: ().

[56] D. B. Leeson. "A Simple Model of Feedback Oscillator Noise Spectrum". In: *Proceedings of the IEEE* 54.2 (1966), pp. 329–330. ISSN: 15582256. DOI: 10.1109/PROC.1966.4682.

[57] Andrea Bevilacqua and Luca Vettorello. *Co-design of a Class-D Oscillator and Dedicated DC-DC Power Converter Supervisor Master Candidate*. Tech. rep.

[58] Ali Hajimiri and Thomas H. Lee. "A general theory of phase noise in electrical oscillators". In: *IEEE Journal of Solid-State Circuits* 33.2 (Feb. 1998), pp. 179–194. ISSN: 00189200. DOI: 10.1109/4.658619.

[59] Luca Fanori and Pietro Andreani. "Class-D CMOS oscillators". In: *IEEE Journal of Solid-State Circuits* 48.12 (Dec. 2013), pp. 3105–3119. ISSN: 00189200. DOI: 10.1109/JSSC.2013.2271531.

[60] David Murphy, Jacob J. Rael, and Asad A. Abidi. "Phase noise in LC oscillators: A phasor-based analysis of a general result and of loaded Q". In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 57.6 (2010), pp. 1187–1203. ISSN: 15498328. DOI: 10.1109/TCSI.2009.2030110.

[61] Emad Hegazi, Henrik Sjöland, and Asad A. Abidi. "A filtering technique to lower LC oscillator phase noise". In: *IEEE Journal of Solid-State Circuits* 36.12 (Dec. 2001), pp. 1921–1930. ISSN: 00189200. DOI: 10.1109/4.972142.

[62] Ali Hajimiri and Thomas H. Lee. "Design issues in CMOS differential LC oscillators". In: *IEEE Journal of Solid-State Circuits* 34.5 (1999), pp. 717–724. ISSN: 00189200. DOI: 10.1109/4.760384.

[63] Pietro Andreani et al. "A study of phase noise in colpitts and LC-tank CMOS oscillators". In: *IEEE Journal of Solid-State Circuits* 40.5 (May 2005), pp. 1107–1118. ISSN: 00189200. DOI: 10.1109/JSSC.2005.845991.

[64] Xiaoyong Li, Sudip Shekhar, and David J. Allstot. "Gm-boosted common-gate LNA and differential Colpitts VCO/QVCO in 0.18-μm CMOS". In: *IEEE Journal of Solid-State Circuits*. Vol. 40. 12. Dec. 2005, pp. 2609–2618. DOI: 10.1109/JSSC.2005.857426.

[65] Jong Phil Hong and Sang Gug Lee. "Low phase noise G m-boosted differential gate-to-source feedback colpitts CMOS VCO". In: *IEEE Journal of Solid-State Circuits* 44.11 (Nov. 2009), pp. 3079–3091. ISSN: 00189200. DOI: 10.1109/JSSC.2009.2031519.

[66] Mohammad Jafar Hemmati and Sepehr Ebrahimi Mood. "Design of Low-Power Differential CMOS LC Voltage Controlled Oscillator using Genetic Algorithm". In: *2022 30th International Conference on Electrical Engineering, ICEE 2022*. Institute of Electrical and Electronics Engineers Inc., 2022, pp. 896–899. ISBN: 9781665480871. DOI: 10.1109/ICEE55646.2022.9827174.

[67] Mohammad Jafar Hemmati and Sepehr Ebrahimi Mood. "Low power and low phase noise complementary voltage controlled oscillator optimised by a meta-heuristic algorithm". In: *IET Microwaves, Antennas and Propagation* 17.14 (Nov. 2023), pp. 1073–1081. ISSN: 17518733. DOI: 10.1049/mia2.12424.

[68] Andrea Mazzanti and Pietro Andreani. "Class-C harmonic CMOS VCOs, with a general result on phase noise". In: *IEEE Journal of Solid-State Circuits*. Vol. 43. 12. Dec. 2008, pp. 2716–2729. DOI: 10.1109/JSSC.2008.2004867.

[69] Babak Soltanian and Peter R. Kinget. "Tail current-shaping to improve phase noise in LC voltage-controlled oscillators". In: *IEEE Journal of Solid-State Circuits*. Vol. 41. 8. Aug. 2006, pp. 1792–1802. DOI: 10.1109/JSSC.2006.877273.

[70] Zhangming Zhu, Liang Liang, and Yintang Yang. "A Startup Robust Feedback Class-C VCO with Constant Amplitude Control in 0.18 μm CMOS". In: *IEEE Microwave and Wireless Components Letters* 25.8 (Aug. 2015), pp. 541–543. ISSN: 15311309. DOI: 10.1109/LMWC.2015.2440871.

[71] Xiao Xu et al. “18-GHz band low-power LC VCO IC using LC bias circuit in 56-nm SOI CMOS”. In: *Asia-Pacific Microwave Conference Proceedings, APMC*. Institute of Electrical and Electronics Engineers Inc., June 2017, pp. 938–941. ISBN: 9781538606407. DOI: 10.1109/APMC.2017.8251604.

[72] Luca Fanori and Pietro Andreani. “A high-swing complementary class-C VCO”. In: *European Solid-State Circuits Conference*. 2013, pp. 407–410. ISBN: 9781479906437. DOI: 10.1109/ESSCIRC.2013.6649159.

[73] Luca Fanori and Pietro Andreani. “Highly efficient class-C CMOS VCOs, including a comparison with class-B VCOs”. In: *IEEE Journal of Solid-State Circuits* 48.7 (2013), pp. 1730–1740. ISSN: 00189200. DOI: 10.1109/JSSC.2013.2253402.

[74] Massoud Tohidian et al. “High-swing class-C VCO”. In: *European Solid-State Circuits Conference*. 2011, pp. 495–498. ISBN: 9781457707018. DOI: 10.1109/ESSCIRC.2011.6045015.

[75] Jian Yu Hsieh and Kuei Yu Lin. “A 0.7-mW LC voltage-controlled oscillator leveraging switched biasing technique for low phase noise”. In: *IEEE Transactions on Circuits and Systems II: Express Briefs* 66.8 (Aug. 2019), pp. 1307–1310. ISSN: 15583791. DOI: 10.1109/TCSII.2018.2886171.

[76] Masoud Babaie, Mina Shahmohammadi, and Robert Bogdan Staszewski. “A 0.5V 0.5mW switching current source oscillator”. In: *Digest of Papers - IEEE Radio Frequency Integrated Circuits Symposium*. Vol. 2015-November. Institute of Electrical and Electronics Engineers Inc., Nov. 2015, pp. 183–186. ISBN: 9781479976416. DOI: 10.1109/RFIC.2015.7337735.

[77] Ali Mostajeran, Mehrdad Sharif Bakhtiar, and Ehsan Afshari. “A 2.4GHz VCO with FOM of 190dBc/Hz at 10kHz-to-2MHz offset frequencies in 0.13μm CMOS using an ISF manipulation technique”. In: *Digest of Technical Papers - IEEE International Solid-State Circuits Conference*. Vol. 58. Institute of Electrical and Electronics Engineers Inc., Mar. 2015, pp. 452–453. ISBN: 9781479962235. DOI: 10.1109/ISSCC.2015.7063121.

[78] Eric A.M. Klumperink et al. “Reducing MOSFET 1/f noise and power consumption by switched biasing”. In: *IEEE Journal of Solid-State Circuits* 35.7 (July 2000), pp. 994–1001. ISSN: 00189200. DOI: 10.1109/4.848208.

[79] Fei Wang and Hua Wang. “A noise circulating oscillator”. In: *IEEE Journal of Solid-State Circuits* 54.3 (Mar. 2019), pp. 696–708. ISSN: 00189200. DOI: 10.1109/JSSC.2018.2886321.

[80] Byung Hun Min, Seok Bong Hyun, and Hyun Kyu Yu. “Low voltage CMOS LC VCO with switched self-biasing”. In: *ETRI Journal* 31.6 (Dec. 2009), pp. 755–764. ISSN: 12256463. DOI: 10.4218/etrij.09.1209.0046.

[81] Masoud Babaie and Robert Bogdan Staszewski. “A class-F CMOS oscillator”. In: *IEEE Journal of Solid-State Circuits* 48.12 (Dec. 2013), pp. 3120–3133. ISSN: 00189200. DOI: 10.1109/JSSC.2013.2273823.

[82] Mina Shahmohammadi, Masoud Babaie, and Robert Bogdan Staszewski. “A 1/f noise upconversion reduction technique applied to Class-D and Class-F oscillators”. In: *Digest of Technical Papers - IEEE International Solid-State Circuits Conference*. Vol. 58. Institute of Electrical and Electronics Engineers Inc., Mar. 2015, pp. 444–445. ISBN: 9781479962235. DOI: 10.1109/ISSCC.2015.7063117.

[83] Chee Cheow Lim et al. “An inverse-class-F CMOS oscillator with intrinsic-high-Q first harmonic and second harmonic resonances”. In: *IEEE Journal of Solid-State Circuits* 53.12 (Dec. 2018), pp. 3528–3539. ISSN: 00189200. DOI: 10.1109/JSSC.2018.2875099.

[84] Jianglin Du et al. “A Compact 0.2–0.3-V Inverse-Class-F23 Oscillator for Low 1/f3 Noise Over Wide Tuning Range”. In: *IEEE Journal of Solid-State Circuits* 57.2 (Feb. 2022), pp. 452–464. ISSN: 1558173X. DOI: 10.1109/JSSC.2021.3098770.

[85] David Murphy, Hooman Darabi, and Hao Wu. “Implicit Common-Mode Resonance in LC Oscillators”. In: *IEEE Journal of Solid-State Circuits* 52.3 (Mar. 2017), pp. 812–821. ISSN: 00189200. DOI: 10.1109/JSSC.2016.2642207.

[86] Bodhisatwa Sadhu, Umaikhe E. Omole, and Ramesh Harjani. “Modeling and synthesis of wide-band switched-resonators for VCOs”. In: *Proceedings of the Custom Integrated Circuits Conference*. 2008, pp. 225–228. DOI: 10.1109/CICC.2008.4672064.

[87] Seong Mo Yim and Kenneth K. O. “Demonstration of a switched resonator concept in a dual-band monolithic cmos lc-tuned vco”. In: *Proceedings of the Custom Integrated Circuits Conference* (2001), pp. 205–208. ISSN: 08865930. DOI: 10.1109/CICC.2001.929756.

[88] Jie Ying Zhong and Sen Wang. “An 11/19-GHz VCO using switchable transformer in 0.18-μm CMOS”. In: *CSQRWC 2012 - 2012 Cross Strait Quad-Regional Radio Science and Wireless Technology Conference*. 2012, pp. 78–81. ISBN: 9781467318679. DOI: 10.1109/CSQRWC.2012.6294977.

[89] Guansheng Li et al. “A low-phase-noise wide-tuning-range oscillator based on resonant mode Switching”. In: *IEEE Journal of Solid-State Circuits* 47.6 (2012), pp. 1295–1308. ISSN: 00189200. DOI: 10.1109/JSSC.2012.2190185.

[90] Guansheng Li and Ehsan Afshari. “A distributed dual-band LC oscillator based on mode switching”. In: *IEEE Transactions on Microwave Theory and Techniques* 59.1 (Jan. 2011), pp. 99–107. ISSN: 00189480. DOI: 10.1109/TMTT.2010.2091203.

[91] Yiyang Shu, Huizhen Jenny Qian, and Xun Luo. “A 18.6-to-40.1GHz 201.7dBc/Hz FoMT Multi-Core Oscillator Using E-M Mixed-Coupling Resonance Boosting”. In: *Digest of Technical Papers - IEEE International Solid-State Circuits Conference*. Vol. 2020-February. Institute of Electrical and Electronics Engineers Inc., Feb. 2020, pp. 272–274. ISBN: 9781728132044. DOI: 10.1109/ISSCC19947.2020.9063100.

[92] Christoph Sandner et al. “Transformer-Based Dual-Mode Voltage-Controlled Oscillators”. In: *IEEE Transactions on Circuits and Systems II: Express Briefs* 54.4 (Apr. 2007), pp. 293–297. ISSN: 15583791. DOI: 10.1109/TCSII.2006.889734.

[93] Burak Çath and Mona Mostafa Hella. “A 1.94 to 2.55 GHz, 3.6 to 4.77 GHz tunable CMOS VCO based on double-tuned, double-driven coupled resonators”. In: *IEEE Journal of Solid-State Circuits* 44.9 (Sept. 2009), pp. 2463–2477. ISSN: 00189200. DOI: 10.1109/JSSC.2009.2023155.

[94] Yue Chao and Howard C. Luong. “Analysis and Design of Wide-Band Millimeter-Wave Transformer-Based VCO and ILFDs”. In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 63.9 (Sept. 2016), pp. 1416–1425. ISSN: 15580806. DOI: 10.1109/TCSI.2016.2577683.

[95] Abhishek Agrawal and Arun Natarajan. "Series Resonator Mode Switching for Area-Efficient Octave Tuning-Range CMOS LC Oscillators". In: *IEEE Transactions on Microwave Theory and Techniques* 65.5 (May 2017), pp. 1569–1579. ISSN: 00189480. DOI: 10.1109/TMTT.2016.2647723.

[96] Yizhuo Wang et al. "A 7.9-14.3GHz -243.3dB FoMTSub-Sampling PLL with Transformer-Based Dual-Mode VCO in 40nm CMOS". In: *Proceedings - A-SSCC 2021: IEEE Asian Solid-State Circuits Conference*. Institute of Electrical and Electronics Engineers Inc., 2021. ISBN: 9781665443500. DOI: 10.1109/A-SSCC53895.2021.9634839.

[97] Jiang Gong et al. "A 0.049mm2 7.1-to-16.8GHz Dual-Core Triple-Mode VCO Achieving 200dB FoM_A in 22nm FinFET". In: *Digest of Technical Papers - IEEE International Solid-State Circuits Conference*. Vol. 2022-February. Institute of Electrical and Electronics Engineers Inc., 2022, pp. 152–154. ISBN: 9781665428002. DOI: 10.1109/ISSCC42614.2022.9731752.

[98] Seongwoog Oh and Jungsuek Oh. "A novel miniaturized tri-band VCO utilizing a three-mode reconfigurable inductor". In: *Digest of Papers - IEEE Radio Frequency Integrated Circuits Symposium*. Vol. 2021-June. Institute of Electrical and Electronics Engineers Inc., June 2021, pp. 187–190. ISBN: 9781665425490. DOI: 10.1109/RFIC51843.2021.9490477.

[99] Mayank Raj et al. "A 7-to-18.3GHz compact transformer based VCO in 16nm FinFET". In: *IEEE Symposium on VLSI Circuits, Digest of Technical Papers*. Vol. 2016-September. Institute of Electrical and Electronics Engineers Inc., Sept. 2016. ISBN: 9781509006342. DOI: 10.1109/VLSIC.2016.7573539.

[100] Omar El-Aassar and Gabriel M. Rebeiz. "Octave-Tuning Dual-Core Folded VCO Leveraging a Triple-Mode Switch-Less Tertiary Magnetic Loop". In: *IEEE Journal of Solid-State Circuits* 56.5 (May 2021), pp. 1475–1486. ISSN: 1558173X. DOI: 10.1109/JSSC.2021.3059442.

[101] Pei Qin, Quan Xue, and Wenquan Che. "Microwave LC Oscillators: Multimode Switching Techniques". In: *IEEE Microwave Magazine* 24.4 (Apr. 2023), pp. 63–81. ISSN: 15579581. DOI: 10.1109/MMM.2022.3233511.

[102] C. Samori, S. Levantino, and V. Boccuzzi. "A -94dBc/Hz@100kHz, fully-integrated, 5-GHz, CMOS VCO with 18% tuning range for bluetooth applications". In: *Proceedings of the Custom Integrated Circuits Conference*. 2001, pp. 201–204. DOI: 10.1109/cicc.2001.929755.

[103] Salvatore Levantino et al. "AM-to-PM conversion in varactor-tuned oscillators". In: *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing* 49.7 (July 2002), pp. 509–513. ISSN: 10577130. DOI: 10.1109/TCSII.2002.804051.

[104] J. J. Rael and A. A. Abidi. "Physical processes of phase noise in differential LC oscillators". In: *Proceedings of the Custom Integrated Circuits Conference*. IEEE, 2000, pp. 569–572. DOI: 10.1109/cicc.2000.852732.

[105] Emad Hegazi and Asad A. Abidi. "Varactor characteristics, oscillator tuning curves, and AM-FM co0nversion". In: *IEEE Journal of Solid-State Circuits* 38.6 (June 2003), pp. 1033–1039. ISSN: 00189200. DOI: 10.1109/JSSC.2003.811968.

[106] Janusz Groszkowski. "The interdependence of frequency variation and harmonic content, and the problem of constant-frequency oscillators". In: *Proceedings of the Institute of Radio Engineers* 21.7 (1933), pp. 958–981. ISSN: 07315996. DOI: 10.1109/JRPROC.1933.227821.

[107] Andrea Bevilacqua and Pietro Andreani. "On the bias noise to phase noise conversion in harmonic oscillators using Groszkowski theory". In: *Proceedings - IEEE International Symposium on Circuits and Systems*. 2011, pp. 217–220. ISBN: 9781424494736. DOI: 10.1109/ISCAS.2011.5937540.

[108] Andrea Bevilacqua and Pietro Andreani. "An analysis of 1/f noise to phase noise conversion in CMOS harmonic oscillators". In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 59.5 (2012), pp. 938–945. ISSN: 15498328. DOI: 10.1109/TCSI.2012.2190564.

[109] Andrea Bonfanti et al. "A varactor configuration minimizing the amplitude-to-phase noise conversion in VCOs". In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 53.3 (2006), pp. 481–488. ISSN: 10577122. DOI: 10.1109/TCSI.2005.858764.

[110] Babak Soltanian and Peter Kinget. "AM-FM conversion by the active devices in MOS LC-VCOs and its effect on the optimal amplitude". In: *Digest of Papers - IEEE Radio Frequency Integrated Circuits Symposium* 2006 (2006), pp. 105–108. ISSN: 15292517. DOI: 10.1109/RFIC.2006.1651102.

[111] Rafaella Fiorelli, Eduardo J. Peralías, and Fernando Silveira. "LC-VCO design optimization methodology based on the gm/I D ratio for nanometer CMOS technologies". In: *IEEE Transactions on Microwave Theory and Techniques* 59.7 (July 2011), pp. 1822–1831. ISSN: 00189480. DOI: 10.1109/TMTT.2011.2132735.

[112] Ting Wu, Un-Ku Moon, and Kartikeya Mayaram. "Dependence of LC VCO Oscillation Frequency on Bias Current". In: ().

[113] Yi Chieh Huang et al. "A 2.4GHz ADPLL with digital-regulated supply-noise-insensitive and temperature-self-compensated ring DCO". In: *Digest of Technical Papers - IEEE International Solid-State Circuits Conference*. Vol. 57. Institute of Electrical and Electronics Engineers Inc., 2014, pp. 270–271. ISBN: 9781479909186. DOI: 10.1109/ISSCC.2014.6757430.

[114] Sam Chun Geik Tan et al. "An ultra-low-cost high-performance bluetooth SoC in 0.11-μm CMOS". In: *IEEE Journal of Solid-State Circuits* 47.11 (2012), pp. 2665–2677. ISSN: 00189200. DOI: 10.1109/JSSC.2012.2211672.

[115] Tai You Lu et al. "Wide tunning range 60 GHz VCO and 40 GHz DCO using single variable inductor". In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 60.2 (2013), pp. 257–267. ISSN: 15498328. DOI: 10.1109/TCSI.2012.2215795.

[116] Ali Basaligheh et al. "A 65-81 GHz CMOS Dual-Mode VCO Using High Quality Factor Transformer-Based Inductors". In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 67.12 (Dec. 2020), pp. 4533–4543. ISSN: 15580806. DOI: 10.1109/TCSI.2020.3004859.

[117] Chi Zhang and Michael Otto. "A low power 4-GHz DCO with fine resolution and wide tuning range in 22 nm FDSOI CMOS technology". In: *IEEE Radio and Wireless Symposium, RWS*. IEEE Computer Society, Mar. 2017, pp. 156–158. ISBN: 9781509034451. DOI: 10.1109/RWS.2017.7885974.

[118] Robert Bogdan Staszewski et al. "Digitally Controlled Oscillator (DCO)-Based Architecture for RF Frequency Synthesis in a Deep-Submicrometer CMOS Process". In: *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing* 50.11 (Nov. 2003), pp. 815–828. ISSN: 10577130. DOI: 10.1109/TCSII.2003.819128.

[119] Pietro Andreani et al. "A TX VCO for WCDMA/EDGE in 90 nm RF CMOS". In: *IEEE Journal of Solid-State Circuits* 46.7 (July 2011), pp. 1618–1626. ISSN: 00189200. DOI: 10.1109/JSSC.2011.2144030.

[120] J. Borremans et al. "A single-inductor dual-band VCO in a 0.06mm2 5.6GHz multi-band front-end in 90nm digital CMOS". In: *Digest of Technical Papers - IEEE International Solid-State Circuits Conference* 51 (2008). ISSN: 01936530. DOI: 10.1109/ISSCC.2008.4523188.

[121] Wanghui Zou et al. "An area-efficient 5GHz/10GHz dual-mode VCO with coupled helical inductors in 0.13-UM CMOS technology". In: *Canadian Conference on Electrical and Computer Engineering* (2011), pp. 000512–000515. ISSN: 08407789. DOI: 10.1109/CCECE.2011.6030503.

[122] Zahra Safarian and Hossein Hashemi. "Wideband multi-mode CMOS VCO design using coupled inductors". In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 56.8 (2009), pp. 1830–1843. ISSN: 15498328. DOI: 10.1109/TCSI.2009.2028414.

[123] Weilin Xu et al. "A CMOS LC-VCO with enhanced PSR based on common-mode replica compensation". In: *ICCASM 2010 - 2010 International Conference on Computer Application and System Modeling, Proceedings*. Vol. 8. 2010. ISBN: 9781424472369. DOI: 10.1109/ICCASM.2010.5619329.

[124] Sebastian Magierowski, Krtysztof Iniewski, and Stefan Zukotynski. "A wideband LC-VCO with enhanced PSRR for SoC applications". In: *Proceedings - IEEE International Symposium on Circuits and Systems*. Vol. 1. 2004. DOI: 10.1109/iscas.2004.1328159.

[125] Elad Alon et al. "Replica compensated linear regulators for supply-regulated phase-locked loops". In: *IEEE Journal of Solid-State Circuits* 41.2 (Feb. 2006), pp. 413–424. ISSN: 00189200. DOI: 10.1109/JSSC.2005.862347.

[126] Che Wei Yeh, Cheng En Hsieh, and Shen Iuan Liu. "A 3.2GHz digital phase-locked loop with background supply-noise cancellation". In: *Digest of Technical Papers - IEEE International Solid-State Circuits Conference*. Vol. 59. Institute of Electrical and Electronics Engineers Inc., Feb. 2016, pp. 332–333. ISBN: 9781467394666. DOI: 10.1109/ISSCC.2016.7418042.

[127] Yue Chen et al. "A supply pushing reduction technique for LC oscillators based on ripple replication and cancellation". In: *IEEE Journal of Solid-State Circuits* 54.1 (Jan. 2019), pp. 240–252. ISSN: 00189200. DOI: 10.1109/JSSC.2018.2871195.