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In-situ reliability monitoring of power packages using a Thermal Test Chip

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Abstract— With an increasing demand for high-power electronics, the need to meet stringent automotive norms and better understand the critical failure mechanisms are crucial in order to improve their reliablity. To that end, we developed an in-situ reliability monitoring setup capable of actively measuring the thermal performance of the package during lifetime testing. A Thermal Test Chip (TTC) assembled into a Power Quad Flat No-lead (PQFN) package was employed as a test vehicle for non-destructive reliability assessment. The TTC comprises resistive heaters as a heat source and resistive temperature elements for measuring the thermal response. The transient thermal behavior was evaluated based on the contribution of heat source to a temperature field, and the temperature distribution was measured at multiple spatial positions. The experimental results provide insights into the thermal properties' influence on the thermal behavior of the package. A compact electro-thermal model based on analogies was developed to deconvolute and analyze the transient thermal measurements. The results of the compact model correlate with the experimental measurements, and the model's accuracy was verified using finite element simulations. The development of such thermal characterization experiments and computationally inexpensive models assist in further understanding the impact of failures in advancing high-power density electronics.

Keywords—Reliability of power electronics, In-situ analysis on reliability monitoring, Transient thermal measurements, Thermal Test Chips, Thermal Compact Modelling, Cauer electro-thermal model, Von-Neumann stability criterion.

INTRODUCTION

Packaging technologies play a vital role in the development of high-power electronics, critical to applications like automotive (EVs), and the failures pertaining to the thermal (or) thermo-mechanical domain within power electronics are commonly attributed to its packaging. Consequently, there is a strong drive to improve package reliability (1). The current practice for reliability assessment is passive identification i.e., identifying the failures after lifetime testing, which typically involves destructive means. Non-destructive techniques such as acoustic imaging (2) are also commonly used but the images are prone to acoustic artifacts. Several researchers have investigated alternative methods to actively monitor package reliability. Yu-Yao et. al. (3) designed a piezoresistive stress sensor for measuring the stresses due to CTE mismatch and hygroscopic swelling mismatch on PBGA packaging; Likewise, Wunderle et. al. (4) designed a Thermal Pixel (Thixel) chip for identifying delamination of the interfaces in a package. Such novel characterization techniques facilitate understanding the failure mechanisms during lifetime testing.

Interface delamination due to thermo-mechanical instabilities (5) is a critical failure mode in power electronics, buried within layer stacks that are difficult to identify without destructive methods. The concept of in-situ reliability monitoring is to locally heat the device and measure the transient thermal response. Any discrepancy in the package would cause a shift in the measured transient response due to its dependence on the underlying material thermal properties. This technique is similar to the classical T3ster® equipment developed by Székely (6), where the thermal response of the device is measured until it reaches steady-state. Székely (6) was able to identify the resistances in-between multiple layers through the thermal impedance measurements and dynamic 1-Dimensional compact modeling. The in-situ reliability monitoring method proposed in this paper was inspired by Székely (6), and the transient response is measured during thermal cycling for lifetime monitoring. An advantage of this method is the application of Thermal Test Chips (TTC) for characterization, which provides spatial information of the thermal performance of a package thereby discrepancies can be correlated to failure origination location. European Center for Power Electronics (ECPE) guideline (7) for

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qualification of power modules mentions that the Thermal Shock Test (TST) (or) thermal cycling tests is to validate the far-field failures i.e., the resistance to mechanical stresses from temperature changes. In earlier times, TSTs were different from thermal cycling because of quick transfer time (< 30s), but the ECPE guideline 2021 states that the transfer time is not relevant anymore, and the temperature slope is around 8-10 K/min. The ultimate goal of this research is to assess the thermo-mechanical failures in a package during accelerated lifetime testing (thermal cycling) based on ECPE guidelines, and the primary focus of this paper is the In-situ reliability monitoring methodology and the thermal properties influence on the measured transient response validated with compact models.

With rising reliability issues on power packages, test chips serve as an alternative to functional power devices to assess the package performance. The test chips developed and manufactured by Thermal Engineering Associates (8) in the size of a unit cell contains heating resistors and diode temperature sensors. Likewise, Sattari et. al. (9) designed and fabricated a multi-functional TTC shown in figure 1a, which consists of three Resistance-based Temperature Detectors (RTD) with a 4-point sensing method. The maximum sensitivity of these devices are in the range of ∼11-12 Ω/ °C. The resistance sensitivity for any given temperature is relatively dependent on its base resistance, which if normalized provides the Temperature Coefficient Resistance (TCR) of the base material i.e., TCR of Titanium (0.0035 [1/^{o}C]). The TTC by Sattari et. al., (9) has the advantage of multiple RTDs and heaters, and hence it was chosen as the test vehicle for this research.

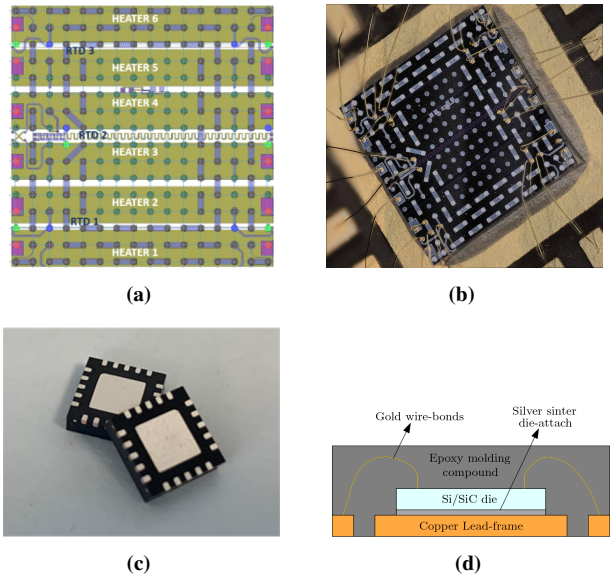

Fig. 1: **(a)** A TTC (9) with two Linear RTDs (RTD 1 & 3) positioned on the edges, one Spiral RTD (RTD 2) positioned at the center and six micro heaters. **(b)** A TTC (9) wire-bonded on a 20 quad pad lead frame. **(c)** Power Quad Flat No-lead (PQFN) package for surface mount technology. **(d)** A schematic representation of a PQFN along its cross-section.

The test chip was assembled in a Power Quad Flat No-lead (PQFN) package, and the electrical connections were established by wire bonds as shown in figure 1b. PQFN is a high-power version of QFN packages, and it is widely used in the industries mainly because of the surface mount technology instead of through-hole leads. PQFN packages are normally made thin but in this research, the overmold was made sufficiently thick (∼1mm) above the die surface because of wire bonds. An actual picture of the PQFN packages is shown in figure 1c and the cross-sectional details is shown in figure 1d.

The transient thermal response of the PQFN was simulated using a compact modeling approach based on thermal to electrical analogies. Székely (6) described the two conventional compact model types (i.) The Cauer thermal model and (ii.) The Foster thermal model. The Cauer circuit also known as the transmission line model includes the resistance and capacitance of multiple layers in a package. The intermediate layer temperatures can be determined in the Cauer circuit because the resistance and capacitance network is connected to the thermal ground. The simplified 1D Cauer model is shown in figure 2a, where Tj is the junction temperature, T_n represents the temperature at the intermediate locations, Tc is the ambient temperature, R_n and C_n are the resistance and capacitance of the intermediate layers.

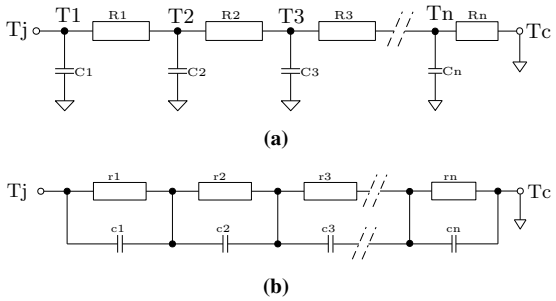

Fig. 2: **(a)** Cauer model (or) transmission line model with grounded capacitor network (10). **(b)** Foster model with non-grounded capacitors. (10).

The Cauer circuit shown in figure 2a is an electrical equivalent circuit of the thermal domain. In the electrical domain, the total capacitance of the capacitors connected in series is the reciprocal of the summation of the reciprocals of the individual capacitance. However, the heat transfer physics dictates that the total capacity in the thermal domain is the summation of all capacity. Hence, the electrical equivalent of the thermal network is a circuit with capacitance connected in parallel i.e., the grounded capacitor ladder network explained by Omid Alavi (10). In contrast, the Foster circuit doesn't include the layer sequence. Foster models are derived by fitting the model to the experimentally measured impedance curve. Hence, they don't have a physical meaning because the individual block components don't correspond to the actual material properties. The Foster circuit is shown in figure 2b with the model parameters r_n and c_n.

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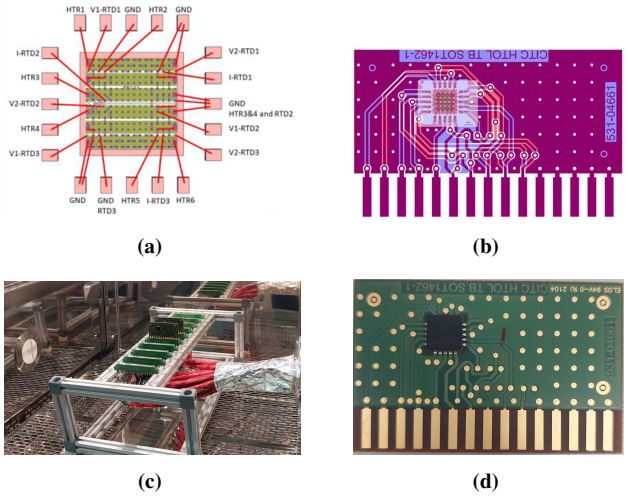
In the next section, the In-situ reliability monitoring methodology is explained, and followed by the 2-Dimensional Cauer modeling approach is detailed with finite element simulations for verification.

IN-SITU RELIABILITY MONITORING

For in-situ monitoring, the silicon backside of the TTC (9) was plated with nickel-palladium-gold (NiPdAu) alloy and was assembled with pressure-less silver sinter material on a copper lead frame with silver metallization. The Bond Line Thickness (BLT) of the die-attach material was $\sim 50\mu$m after sintering. The electrical connections to the TTC were established by gold wire bonds, and the wire-bond layout is shown in figure 3a. The wires are 99.99% pure gold, and the diameter of the wire is 25um with a bond bump diameter of around $\sim$50um. The wire-bond layout was designed to fit within the 20 quad pads copper lead frame. Once wire-bonded, the TTC was encapsulated with Sumitomo EME-G700LA epoxy molding compound, and the package was soldered to a Printed Circuit Board (PCB) with Tin-Silver-Copper (SAC305) solder paste as shown in figure 3d. The PCB layout for TTC configuration is shown in figure 3b. The front side of the test board was patterned for connections to PQFN, and the backside has a copper ground plane for Electromagnetic Interference (EMI) reduction. The core of the PCB contains glass fiber reinforced Polyimide Laminate.



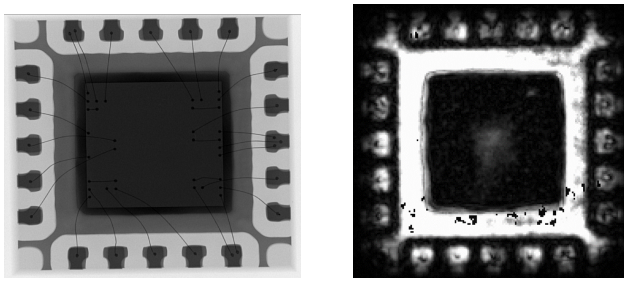
(a) (b)

(c) (d)

Fig. 3: **(a)** Wirebond layout designed for PQFN to provide electrical connections to the TTC. **(b)** PCB layout designed for TTC with double side metallic tracks for external electrical connections. **(c)** A Test setup inside an industrial thermal cycling oven with 10 PCB edge connectors and CAT 7 cables to extend the electrical connections to the measuring equipment's. **(d)** Actual PQFN package re-flow soldered on a PCB for in-situ measurements.

A test setup accomodating 10 test boards were built inside a TMCL T/270/70/20 thermal cycling oven as shown in figure 3c. The test boards were connected to a Keithley 3706A multiplexer for switching between different test boards and different heaters/RTDs in the TTC. Twisted pairs with double shield CAT 7 cables were used to reduce the electromagnetic interference. The input current to the TTC was sourced using Keithley 2602B Source Measuring Unit (SMU), and the output voltage was measured using Keithley DMM7510. The Number of Power Line Cycles (NPLC) for the SMU was set to 1, and the DMM was set to measure at high speed with a timestep of $\sim$1ms (NPLC DMM $<$ 1). The output measurements were influenced by the 50hz frequency due to high measuring speed, which is not in sync with the power line frequency, but the magnitude of the interference was significantly lower because of the shielded cables.

The integrity of the PQFN packages after assembly was analyzed with X-ray imaging and Computed Scanning Acoustic Microscopy (CSAM) as shown in figure 4. Low atomic number materials such as silicon and polymers are transparent to X-rays, which facilitates the evaluation of the pressure-less silver sinter material's uniformity and voids. The X-radiation (X-ray) inspection was performed with a 160kV transmissive X-ray tube with up to 10W target power, providing 0.5μm feature recognition. It can be observed from figure 4a that the die-attach material has uniform coverage without any voids, but the silver sinter material is expected to be porous (approx. 85% dense) due to the pressure-less process. The package assembly optimization of the PQFN with the pressure-less sintering process will not be discussed in this paper. The X-ray image also shows that the wire bonds are well separated.



(a) (b)

Fig. 4: **(a)** X-ray inspection for die-attach and wire-bond reliability of the PQFN LF4 34. **(b)** CSAM inspection for die planarity and interface bond reliability of the PQFN LF4 34. The white spot at the center could be poor adhesion near to the die interface. Hence, we chose the sample PQFN LF4 34 as the DUT.

To further evaluate the die planarity and the interface bonding, CSAM analysis was performed. Due to the presence of a PCB, a Transmission Through (TT) scan was not possible. Hence, a sequential lateral scan (X-scan) was performed from the molding compound side using a 30Mhz transducer. Unfortunately, the mold compound attenuates the acoustic signal, and as a consequence, the underlying interfaces were less clear. Any irregularity in the sample would cause a reflected echo signal for the region of interest, which would result in dark and white features in the obtained image. The integrity of multiple PQFN packages was assessed, and the PQFN

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LF4 34 was chosen as the Device Under Test (DUT) due to its discrepancy observed on the CSAM and is shown in figure 4b. The CSAM inspection of the DUT (PQFN LF4 34) indicates a white spot at the center closer to the die interface, which could be poor adhesion. However, it is difficult to be conclusive at this point. The lifetime reliability assessment of the DUT (PQFN LF4 34) and the thermo-mechanical failures associated to it will not be addressed in this paper.

For reliability assessment, the JEDEC standards (11) for temperature cycling and the automotive grade-1 semiconductors AEC-Q101 guidelines (12) were followed. Based on the qualification test definitions mentioned in AEC-Q101 (12), the minimum and maximum temperature range are -55^{o}C and $+150^{o}$C. The component cycle rate for delamination assessment was maintained at $\sim$1-2 cycles per hour as per JEDEC standards. The thermal cycling profile for reliability assessment is shown in figure 5, and the parameters for the thermal cycling temperature curve are given in table 1.

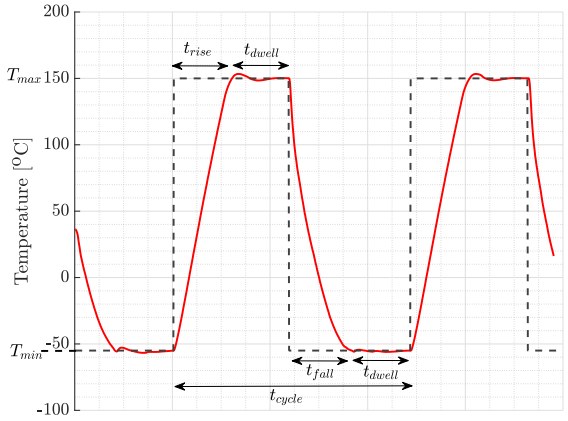

Fig. 5: Thermal cycling temperature curve for lifetime reliability assessment as per JEDEC and automotive grade-1 standards.

Table 1: Thermal cycling test parameters

Lowest temperature value (i.e.,) Measurement point 1	T_{min} (or) $M1$	-55°C
Highest temperature value (i.e.,) Measurement point 2	T_{max} (or) $M2$	150°C
Dwell time	t_{dwell}	$\sim$10mins
Rise time	t_{rise}	$\sim$10mins
Fall time	t_{fall}	$\sim$10mins
Cycles per hour	cph	$\sim$1-2

The thermal response of the DUT was measured at T_{min} and T_{max} for In-situ monitoring, considering that the maximum thermal barrier will be at the extreme temperatures. During measurements, the input currents can cause undesirable self-heating effects on the device, which is commonly known as Joule or Ohmic heating. Hence, the RTD of the device was tested with a range of input currents, and the output voltage was measured for five seconds. Figure 6 shows the Voltage-Current curve of the DUT in comparison to the voltage difference ΔU measured overtime at each input current, and ΔU becomes negligible for low input currents. The self-heating effects are assumed sufficiently low for the input current in the range of $\pm$0.3mA, and accordingly, the measurement current for the device was chosen to be 0.3mA.

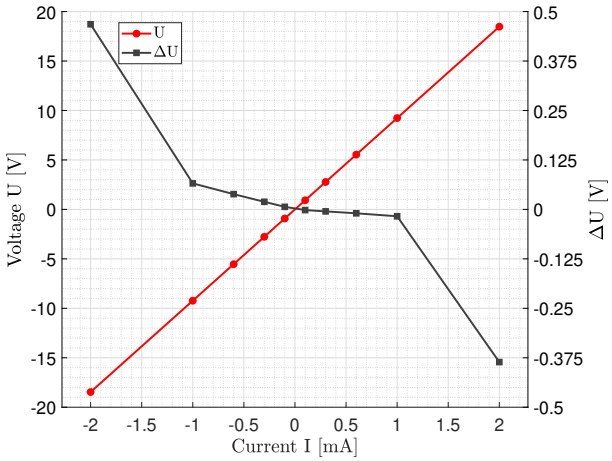

Fig. 6: Ohmic heating measurements of the RTD for a range of input current. U denotes the voltage measured for each input current I, and ΔU denotes the voltage difference. Lower ΔU indicates lower self heating effects.

To accurately characterize the thermal performance of the package, it is critical to verify the accuracy of the device and the measuring equipment. For measurements in the range of 10V, the resolution of the DMM7510 is 1μV, and the accuracy of the equipment was calculated to be $\Delta V = \pm$0.1mV from the manufacturers' datasheet.

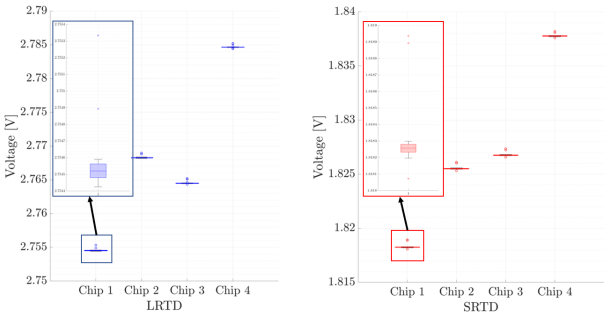

Fig. 7: Repeatability and Reproducibility measurements of Linear RTD and Spiral RTD measured at 25°C for 4 different TTCs. Repeatability indicates the variation in the measurements, which are within the accuracy of the measuring equipment ($\Delta V = \pm$0.1mV). Reproducibility indicates the dissimilarities from device to device.

To verify the variability in the device and the measuring equipment, the repeatability and the reproducibility of four test chips were analyzed. The voltage response of the Linear RTD (LRTD) and the Spiral RTD (SRTD) were measured twenty times repeatedly at room temperature (25°C), and the results of the measurements are shown in

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figure 7. The box chart shows that the measurements are repeatable, and the deviation is within the accuracy of the measuring device ± 0.1mV. From figure 7, the percentage of outliers for a sample size of twenty is around 20%, and the outlier percentage will be lower for a larger sample size. However, the reproducibility of the measurements depends solely on the device being tested. Figure 7 signifies minute differences from device to device. Hence, it is crucial to calibrate the devices before the start of the measurements and also to identify the temperature sensitivity of the DUT.

The DUT was calibrated at eight measurement points from -55^{o}C to $+150^{o}$C and a perfectly linear relation was observed with a sensitivity of $\sim 11\ \Omega/^{o}$C for LRTD and $\sim 9\ \Omega/^{o}$C for SRTD. The calibration plots are shown in figure 8.

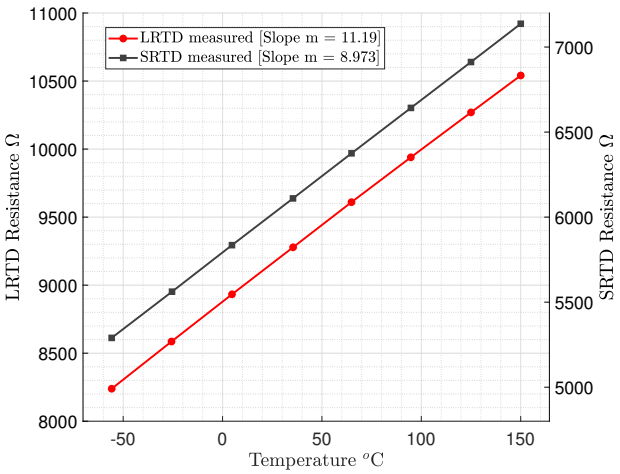

Fig. 8: The plot denotes the resistance of the device measured at eight different temperatures for Linear RTD and Spiral RTD. The sensitivity of the device [$\Omega/^{o}$C] was determined using a first order polynomial fit.

Once the DUT is calibrated, a short heat pulse of $\sim$0.7W$\pm$0.03 is applied at T_{min} and T_{max} using the central heaters i.e., either heater 3 or heater 4 shown in figure 1a for a pulse time of 0.1s, and the response is measured for 3s using the RTDs 1, 2, & 3. The transient thermal response of all three RTDs measured at -55^{o}C and $+150^{o}$C are shown in figures 9 and 10. The concept of in-situ reliability monitoring is that with accelerated life time testing i.e., continuous thermal cycling, the transient response would drift due to the package degradation over time. To evaluate the drifted thermal response, the rate of temperature change during heating and cooling must be calculated for every cycle as mentioned in the equations 1 and 2. From figures 9 and 10, the magnitude of RTD 2 is higher than RTDs 1 and 3, which is because of the physical positioning of RTDs from the heat source location. RTDs 1 and 3 are approx. $\sim$1.6mm far from the heat source, whereas RTD 2 is right next to the source. Also, it can be observed that ΔT for the same input power shows strong temperature dependence i.e., ΔT of RTD 2 increases from 0.9K at -55^{o}C to 1.4K at $+150^{o}$C during ramp-up and likewise during decay.

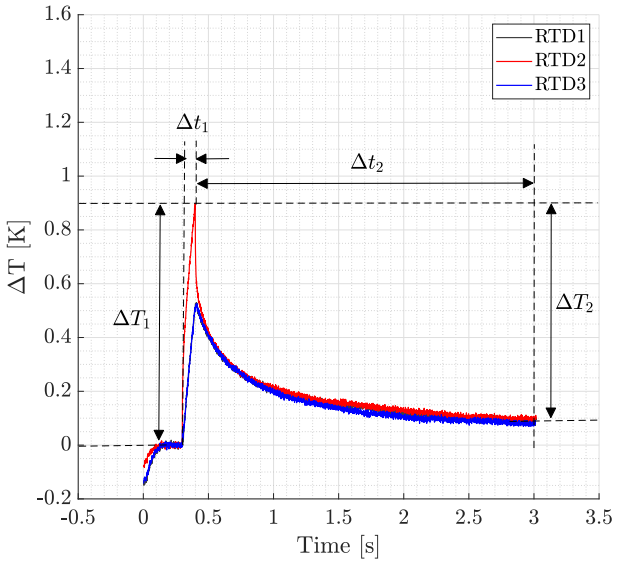

Fig. 9: Transient thermal response of all three RTDs measured for 3s at -55^{o}C is shown along with the components of the monitoring parameters. RTD 2 is next to the heat source, and RTDs 1 & 3 are $\sim$1.6mm from the heat source. $\dot{T}_{ramp}$ of RTD 2 is 9K/s for an input power of $\sim$0.7W$\pm$0.03.

$$\text{Rampup monitoring } \dot{T}_{ramp} = \frac{\Delta T_1}{\Delta t_1}\ \text{[K/s]} \qquad (1)$$

$$\text{Decay monitoring } \dot{T}_{decay} = \frac{\Delta T_2}{\Delta t_2}\ \text{[K/s]} \qquad (2)$$

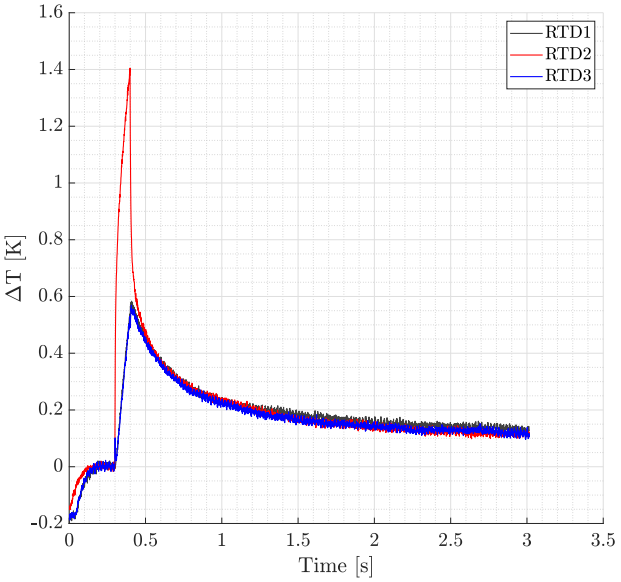

Fig. 10: Transient thermal response of all three RTDs measured for 3s at 150^{o}C. RTD 2 is next to the heat source, and RTDs 1 & 3 are $\sim$1.6mm from the heat source. $\dot{T}_{ramp}$ of RTD 2 is 14K/s for an input power of $\sim$0.7W$\pm$0.03.

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The temperature dependent behavior of the measurements can be explained with the temperature dependence of the material thermal properties. Thermal conductivity is the ability of a material to conduct heat, and specific heat is the property of a material that dictates the amount of energy required to cause per degree change in temperature for a given unit mass. The temperature change ΔT is directly proportional to the rate of energy i.e., input power P, the thickness t, and inversely proportional to the surface area A, and thermal conductivity k as given in equation 3.

$$\Delta \mathbf{T} = \frac{Pt}{A\mathbf{k}} \tag{3}$$

The input power P, the thickness t, and the surface area A are temperature independent i.e., constant, whereas the thermal conductivity k decreases with an increase in temperature. Hence, ΔT in equation 3 will increase with decrease in conductivity k, i.e., ΔT at $+150^{o}$C will be larger than ΔT at -55^{o}C, which is inline with the measurement results shown in figure 9 and 10. However, the influence of the specific heat property c_p over ΔT must also be taken into account. The temperature change ΔT is directly dependent on the heat transfer energy Q, and inversely proportional to the mass m and specific heat capacity c_p as given in equation 4.

$$\Delta \mathbf{T} = \frac{Q}{m\mathbf{c_p}} \tag{4}$$

The amount of input energy Q and the mass of the material m remains constant. It is well known that the specific heat property c_p of metals and semiconductors increases with an increase in temperature. Hence, ΔT will decrease with increase in temperature.

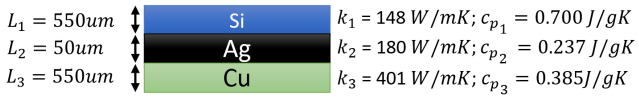

Fig. 11: The thermal properties of Silicon were obtained from Glassbrenner, C. J. (13), and Okhotin, A. S. (14). The properties of copper were obtained from Simon, N. (15), and the properties of Silver were obtained from Andrew A. (16) considering 85% density. The properties shown are at room temperature 25^{o}C. The temperature dependent properties can be found in (13), (14), (15), & (16).

Let L_1, L_2, L_3 be the thicknesses, k_1, k_2, k_3 be the thermal conductivity's, m_1, m_2, m_3 be the masses and c_{p_1}, c_{p_2}, c_{p_3} be the specific heat capacities of Silicon, Silver sinter and Copper. The equivalent properties k_{eq} and $c_{p_{eq}}$ of all three materials can be calculated from equation 5 and 6.

$$k_{eq} = \frac{k_1 k_2 k_3 \left(L_1 + L_2 + L_3\right)}{L_1 \left(k_2 k_3\right) + L_2 \left(k_1 k_3\right) + L_3 \left(k_1 k_2\right)} \tag{5}$$

$$c_{p_{eq}} = \frac{\left(c_{p_1} m_1\right) + \left(c_{p_2} m_2\right) + \left(c_{p_3} m_3\right)}{\left(m_1 + m_2 + m_3\right)} \tag{6}$$

The temperature-dependent equivalent thermal properties of Silicon, Silver sinter, and Copper was calculated from the above equations, and the following conclusions were made:

- With an increase in temperature, the percentage drop in equivalent conductivity k_{eq} was much higher than the percentage increase in equivalent capacity $c_{p_{eq}}$.
- By normalizing the equivalent thermal properties with the constant parameters in equation 3 and 4,
  - ΔT tends to decrease by $\sim 14\%$ due to the increasing specific heat.
  - On the other hand, ΔT increases by $\sim 75\%$ due to the decreasing thermal conductivity.
- A theoretical approximation of percentage rise in ΔT at the heat source is around $\sim 60\%$, which seems reasonably comparable to the 55% increase observed at RTD 2 location in the transient measurements shown in figures 9 and 10.

The transient measurements and the relative contribution of the effective thermal properties' influence were detailed in this section. The remainder of this paper will explain the theory behind thermal compact modeling with verification using finite element simulations. The results of the compact model will also be validated with the experimental measurements.

Thermal Compact Modelling

The test-driven approach needs scientific models to accurately characterize the processes that facilitate further experiments. The in-situ experiments detailed in the previous chapter need modeling to deconvolute and analyze further. Numerical methods such as finite element simulations are mostly used for complex simulations by taking non-linear effects into account, but these methods are computationally expensive. On the other hand, circuit simulators don't need high computational power, and industries are using such tools in the development and optimization processes (17), (18). To that end, an electrothermal model was developed based on thermal to electrical analogies. The electrical and thermal networks are mutually related because the voltage components of the electrical domain are the heat source of the thermal domain, and the temperature component of the thermal network influences the electrical parameters (19).

In any system, heat transfer can happen only in three ways: Conduction, Convection, and Radiation. During reliability assessment, all three forms of heat transfer happen inside the oven's closed chamber. However, for simplicity, convection and radiation are neglected, assuming that the heat propagates only through conduction within the package. The following one-dimensional equation describes the temperature distribution by conduction, where c_p is the specific heat capacity, ρ is the density, k is

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the thermal conductivity of the material, and x denotes the spatial coordinates at which the temperature is evaluated. The inverse of the parameters in the brackets given in equation 7 denotes thermal diffusivity α, which is the rate of heat transfer over a surface.

$$\frac{\partial^2 T}{\partial x^2} = \left(\frac{c_p \cdot \rho}{k}\right) \cdot \frac{\partial T}{\partial t} = \left(\frac{1}{\alpha}\right) \cdot \frac{\partial T}{\partial t} \tag{7}$$

Likewise, the electrical equivalent to the thermal model is expressed with capacitance, resistance, inductance, and transverse conductance per unit area. However, based on the assumption that heat propagates only through conduction leads to a more simplified electrical model expressed only with Capacitance and Resistance, which is given in equation 8.

$$\frac{\partial^2 U}{\partial x^2} = CR\frac{\partial U}{\partial t} \tag{8}$$

where U denotes voltage as a substitute for temperature T, C denotes electrical capacitance as a substitute for thermal capacitance C_{th}, and R denotes electrical resistance as a substitute for thermal resistance (inverse of thermal conductance). The transient heat flow by conduction can be modeled by the electrical equivalent Cauer circuit as shown in figure 2a. The analogous thermal and electrical elements required for the compact model are given in table 2.

Table 2: Analogous thermal and electrical elements

Elements		Resistance	Capacitance
Thermal	Symbol	R_{th}	C_{th}
	Unit	K/W	J/K
Electrical	Symbol	R	C
	Unit	Ω	F

The electrical equivalent circuit of the PQFN and the PCB was designed in LTspice simulator based on the Cauer network shown in figure 2a and the analogies given in table 2. The electrical equivalent heat transfer components of a PQFN with multiple layers were designed in two dimensions i.e., lateral and medial (thickness) directions as shown in figure 12a, and the PCB components were modeled in three dimensions as shown in figure 12b. The geometrical dimensions of the PQFN with PCB and its thermal material properties are given in table 3 and 4. The electrical equivalent circuit of the PQFN was designed by normalizing along the surface XY-plane, whereas the three-dimensional PCB equivalent circuit was designed by normalizing along the thickness z-direction.

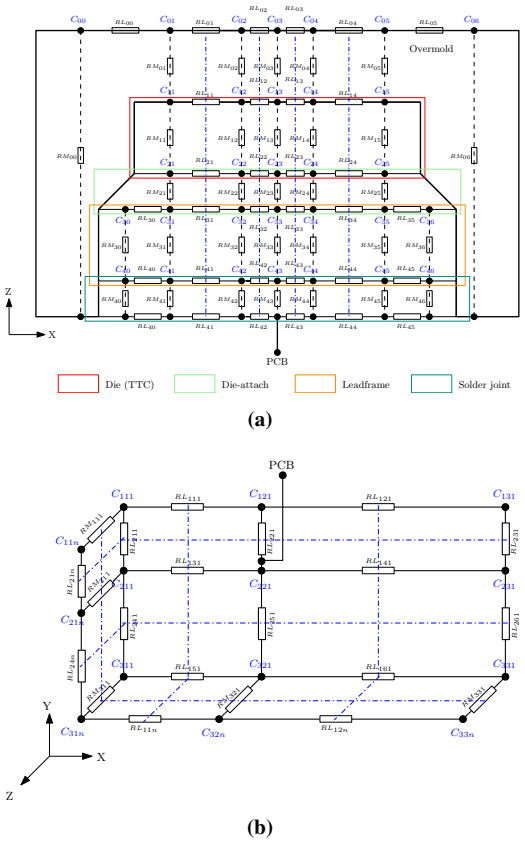

Fig. 12: **(a)** Electrical equivalent two-dimensional circuit of a PQFN. The electrical parameters R and C were obtained using analogous relation from thermal parameters c_p, ρ, and k. **(b)** Electrical equivalent three-dimensional circuit of a PCB with electrical parameters obtained using analogies.

Table 3: Geometrical dimensions

Material	Width [mm]	Length [mm]	Thickness [mm]
Die	4.2	4.2	0.55
Die-attach	4.2	4.2	0.05
Leadframe	6	6	0.55
Solder joint	6	6	0.04
PCB laminate	40	63	1.65
Overmold	8	8	0.94

Table 4: The thermal properties of Silicon, Copper, and Silver Sinter (85% density) at room temperature was obtained from (13), (14), (15), & (16). The PCB design was simplified by assuming the properties of Polyimide (PCB laminate core). Standard properties of SAC305 was taken. Epoxy Molding Compound properties were taken from the data-sheet of Sumitomo EME-G700LA.

Material	Density $(\rho)[g/mm^3]$	Conductivity (k) [W/mmK]	Specific heat (c_p) [J/gK]
Silicon	$2.32e^{-3}$	0.148	0.7
Silver	$8.92e^{-3}$	0.180	0.237
Copper	$8.96e^{-3}$	0.401	0.385
SAC	$7.32e^{-3}$	0.06	0.232
Polyimide	$1.88e^{-3}$	0.00173	1.13
Epoxy	$0.95e^{-3}$	0.00096	1.9

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The transient thermal analysis using the compact electrothermal model on package level was evaluated based on the heat source contribution to a temperature field, and the temperature distribution was calculated at different spatial points and the results are shown in figure 13. The electrothermal model was discretized into multiple elements as shown in figure 12a with heat source and sensing locations the same as the actual device shown in figure 1a.

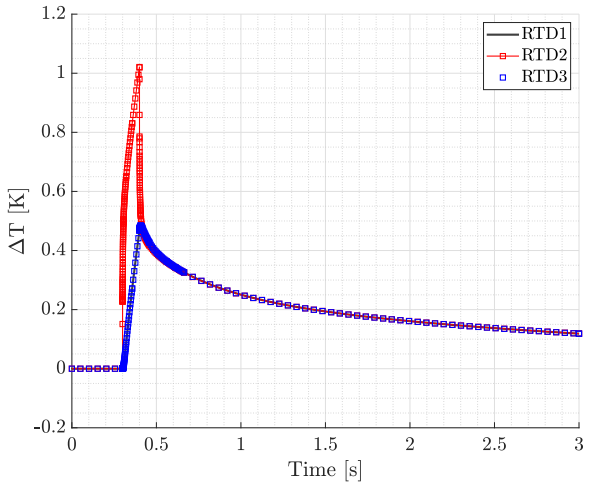


Fig. 13: Transient thermal response of the PQFN obtained from the electrothermal model with material thermal properties at room temperature given in table 4.

The results from the electrothermal model shown in figure 13 are only as accurate as the model is, and hence, the model's accuracy was evaluated by finite element methods. The Von-Neumann stability criterion for thermal diffusivity plays a vital role in thermal diffusion finite element simulations. S. B. Yuste (20) explains in detail, the stability analysis for the fractional diffusion equations. S. B. Yuste (20) discretized the one-dimensional heat conduction expression given in equation 7 using Forward Time Central Space (FTCS) method and is given as follows

$$\frac{T_n^{i+1} - T_n^i}{\Delta t} = \frac{\alpha}{\Delta x^2}\left(T_{n+1}^i - 2T_n^i + T_{n-1}^i\right) \tag{9}$$

where α is the thermal diffusivity given in equation 7. The mesh ratio r for numerical simulation is obtained by rearranging the above equation 9

$$T_n^{i+1} = T_n^i + r\left(T_{n+1}^i - 2T_n^i + T_{n-1}^i\right) \tag{10}$$

$$r = \frac{\alpha \Delta t}{\Delta x^2} \tag{11}$$

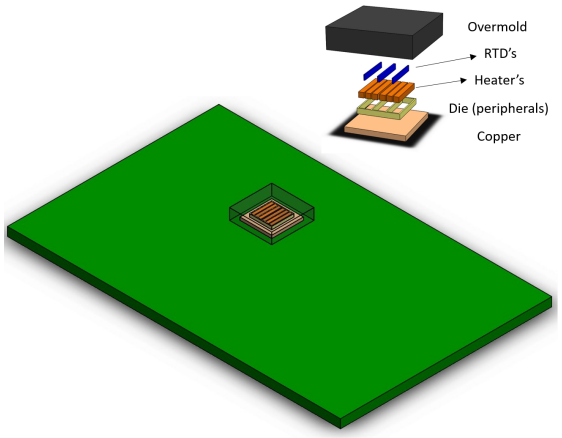
To achieve numerical stability, the mesh ratio r must be less than or equal to the critical mesh ratio r_c, which has to be determined. Assume at iteration i, the nodes n+1 and n-1 have a temperature T, while node n has zero temperature;

$$T_n^{i+1} = 0 + r_c(T + 0 + T) = r_c(2T) \tag{12}$$

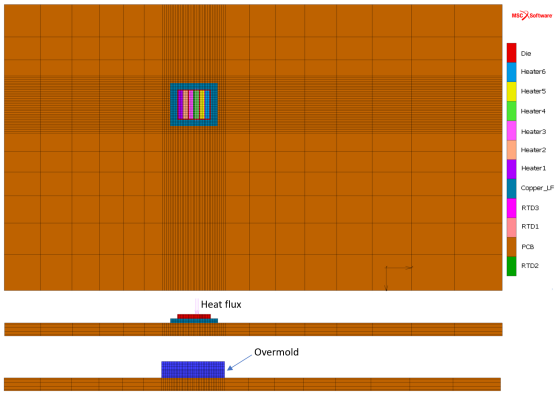
From equation 12, for r_c values greater than 0.5, the temperature of the node n at iteration i+1 will be greater than the surrounding nodes, which cannot be true. Hence, to achieve a numerically stable solution, the critical mesh ratio r_c must be less than or equal to 0.5 which is also shown using numerical techniques in (20).

$$r \leq r_c = 0.5 \tag{13}$$

A 3D model of the PQFN with PCB is shown in figure 14a, and the finite element mesh is shown in figure 14b. Although the simulations are conditionally stable, the element size Δx scales to the power of two as the time step Δt, which increases computational time. Hence, very thin interfaces ($\leq$50um) i.e., die-attach and solder-joints are modeled as contact interactions with interface heat transfer coefficients, which primarily depend on contact area, interface thickness, and thermal conductivity of the interface material. The total time for simulation was set to 2.7s with a constant timestep Δt of 1e^{-4}s, and the input power of 0.7W is applied for 0.1s. The timestep Δt of 1e^{-4}s was chosen because it meets the stability criterion $r \leq r_c$. The results of the finite element simulation and the compact model are shown in comparison with the experimental output of all three RTDs measured at +25^{o}C in figure 15.



(a)



(b)

Fig. 14: **(a)** An exploded view of the PQFN attached to a test board. The die-attach and the solder interface were modelled as contact interactions with heat transfer coefficients. **(b)** A finite element Hexahedron mesh for transient thermal simulations. The mesh ratio r is calculated for every layer, and it is less than the critical mesh ratio r_c.

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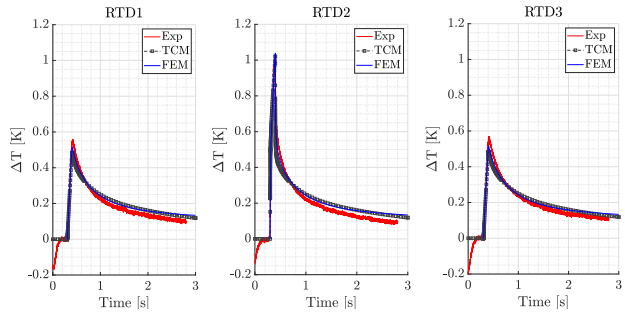

Fig. 15: Transient thermal response obtained from the electro-thermal model and finite element simulations in comparison to the experimental data measured at $+25^{o}$C. The results of the 2D compact model nicely fits the result of the finite element simulations. Also, the experimental data validates the compact model with some discrepancy during cooling.

The compact model gives good co-relation with the results of finite element simulation, which verifies the accuracy of the model. Also, the model predicts well the transient response measured at $+25^{o}$C with some discrepancy during cooling. The mismatch during heat dissipation can be because of the various assumptions in the model.

The compact model and the transient thermal measurements proposed in this paper facilitate in identifying the thermal degradation of the package. Associating thermal degradation to a fracture, the sensitivity of the transient thermal measurements to identify a fracture depends on

- The distance from the heat source to the fracture location.
- The distance between the heat source and the sensing elements, which must be as small as possible, and
- The minimum distance between two sensing points at the fracture location, which is the minimum fracture length that can be identified.

Likewise, simulating the drifted thermal response due to a fracture with a compact thermal model also depends on the above mentioned points.

Summary and Conclusions

The global power electronics market has been rapidly growing, and the industry has a clear need for active monitoring during lifetime testing. To that end, we have proposed an in-situ experimental method for reliability assessment, which follows the guidelines of the JEDEC standards for temperature cycling and the AEC-Q101 automotive grade 1 semiconductors. The lifetime reliability of power packages associated with the thermo-mechanical challenges can be monitored by evaluating the thermal performance of the package.

- The experimental method proposed in this paper evaluates the thermal properties influence on the device thermal performance and the transient thermal behavior was evaluated by measuring the temperature distribution at different spatial locations within the die surface.
- A compact modelling approach was further developed for simulating the transient thermal response by using thermal to electrical analogies and the model's accuracy was verified with finite element simulations.
- The outcome of the compact model provides a comprehensive co-relation with the in-situ experimental results thereby validating the model's accuracy.
- The sensitivity of the compact model to simulate a failure and the transient measurements to identify a failure relatively depends on the distance from the heat source to the failure location, the minimum distance between the heat source and the sensing elements, and the minimum distance between two sensing elements.
- Development of such computationally inexpensive models can be further used in optimizing the package thermal performance.

The experimental approach proposed in this paper was inspired from Székely (6) and in comparison, the evaluation of the thermal drift by monitoring the rate of temperature change ($\Delta T/\Delta t$ [K/s]) for every cycle will detect the thermal barriers during thermal cycling.

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