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Package-Level Electro-Thermal Simulation With Transient Thermal Resistance Model for Surge Stress Failure Analysis of SiC MOSFET

Zaiman Xiang, Tao Luo, Wenbo Wang, Bo Sun, *Member, IEEE*, Botao Sun, Qingchun Zhang, Guoqi Zhang, *Fellow, IEEE*, and Jiajie Fan, *Senior Member, IEEE*

***Abstract*— This paper investigates the surge reliability of commercial 1200V SiC MOSFETs through a combined approach of experimental testing and multiphysics simulation, elucidating the failure mechanisms under both step and repetitive surge current stress. The innovative integration of package-level electro-thermal coupling simulation with transient junction temperature estimation overcomes the limitations of conventional methodologies that rely solely on decapsulation analysis and Technology Computer Aided Design (TCAD) simulation. Experimental evaluations on six Devices Under Test (DUTs) with distinct structural configurations, employing surge testing and failure analysis techniques including C-mode Scanning Acoustic Microscopy (C-SAM), optical microscopy, and Scanning Electron Microscope (SEM), confirm that device failure primarily originates from gate-source short circuits caused by aluminum bonding wire melting. COMSOL multiphysics simulations further replicate the transient thermal characteristics of bonding wire regions, demonstrating rapid temperature escalation to the Aluminum melting point within 5-6 ms during surge events. A transient thermal resistance-based junction temperature characterization method is proposed, revealing an inverse proportionality between thermal resistance and chip area.**

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***Index Terms*— SiC MOSFET, surge current, bonding wire, electro-thermal simulation, thermal resistance.**

I. Introduction

SILICON carbide (SiC), as a wide-bandgap semiconductor material, has emerged as an ideal candidate for high-voltage, high-temperature, and high-frequency power devices due to its superior properties, including a high critical breakdown electric field, exceptional thermal conductivity, and elevated electron saturation drift velocity [1], [2], [3], [4]. Compared to traditional silicon-based devices, SiC metal-oxide-semiconductor field-effect transistors (MOSFETs) demonstrate significant advantages in power density, switching losses, and high-temperature stability. These superior characteristics have led to their widespread adoption in applications such as renewable energy generation, electric vehicles, and smart grids [5], [6], [7]. However, during third-quadrant operation (reverse conduction), the body diode of SiC MOSFETs is subjected to extreme surge current stress. This reliability challenge has emerged as a critical bottleneck limiting their ability to replace external SiC Schottky Barrier Diodes (SBDs) in practical applications, due to the inherent vulnerability of the body diode under high-current transient conditions [8], [9].

In recent years, numerous studies have focused on addressing the surge reliability challenges of SiC MOSFET body diodes. Reference [10] demonstrated through capacitor discharge experiments that SiC MOSFETs outperform Silicon (Si) Insulated Gate Bipolar Transistors (IGBTs) in surge performance for pulsed power applications, highlighting their suitability for high-frequency, high-power scenarios. Reference [11] compared the surge capabilities of SiC MOSFET body diodes and SBDs under 10 ms pulse width surge tests, revealing that the body diode exhibits marginally superior performance under extreme surge currents due to the larger thermal capacity of its p-n junction.

Following these validations of the body diode's potential to replace SBDs, extensive research has delved deeper into its surge reliability. For SiC MOSFETs with different structures, planar designs demonstrate significantly enhanced surge tolerance compared to trench structures owing to their lower thermal resistance and more uniform current distribution [8], [12], [13]. Symmetric double-trench structures, constrained by deep-trench process defects and termination layout limitations, are prone to thermal breakdown, resulting

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in inferior surge capability relative to planar and asymmetric configurations [13], [14]. Single-pulse surge tests indicate no degradation in threshold voltage or on-resistance prior to reaching surge current limits, with degradation primarily manifesting as increased leakage current and reduced blocking capability [12], [15]. Conversely, repetitive surge tests reveal that degradation arises from gate oxide charge trapping, with a competitive mechanism in on-resistance degradation: gate oxide degradation reduces R_{DSON}, while packaging degradation increases it [8], [16], [17].

To elucidate these degradation phenomena, studies have investigated surge conduction mechanisms under both first-quadrant and third-quadrant operations (reverse conduction, body diode forward conduction). Under positive gate bias, surge current transitions from the channel to the body diode path in stages, with conductivity modulation dominating voltage variations [18]. For third-quadrant operation, optimizing gate voltage is critical to managing the competition between channel and body diode conduction [19], [20]. Research on surge failure mechanisms and thermal effects consistently attributes device failure to localized aluminum metallization melting caused by excessive current density, leading to gate-source short circuits or terminal region burnout [14], [21], [22], [23]. Bonding wire fatigue or damage from high current density accelerates degradation [24], [25]. Technology Computer Aided Design (TCAD) simulations confirm that failure originates from junction temperatures exceeding the aluminum melting point [8].

While post-surge decapsulation analysis combined with TCAD can explain failure mechanisms at the device level, it inadequately characterizes transient temperature rise processes caused by electrothermal coupling at the packaging level. Although electrothermal simulations have been applied to study failure mechanisms in 4H-SiC SBDs under non-repetitive surge tests [26], transient temperature dynamics in SiC MOSFETs during surge events remain insufficiently explored. This gap is critical for understanding packaging degradation induced by bonding wire thermal effects.

In this paper, the failure mechanisms of six 1200V SiC MOSFETs were systematically investigated through single and repetitive surge current stress tests combined with multiple failure analysis methods. By integrating package-level electrothermal simulations and transient junction temperature analysis, the melting of aluminum bonding wires was identified as the primary failure trigger. COMSOL simulations were employed to characterize the junction temperature variation during surge events. A novel junction temperature characterization method based on transient thermal resistance was proposed. Furthermore, the inverse proportionality between thermal resistance and chip area was demonstrated through analyzing the relationship among chip area, thermal resistance, and surge capability, providing a theoretical foundation for optimizing device design and packaging processes.

II. Test Samples and Test Setups

A. Test Samples

As illustrated in Fig. 1(a) and (b), SiC MOSFETs with the TO-247-4L packaging have been widely adopted in power

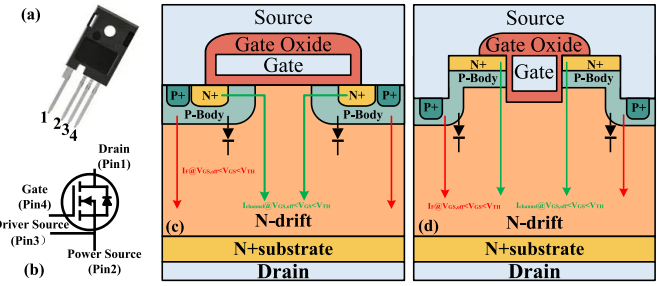


Fig. 1. (a) SiC MOSFETs in TO-247-4L Package. (b) Circuit symbol for TO247-4L package. (c) Cross section of symmetrical Planar Gate. (d) Cross section of symmetric Double Trench Gate.

TABLE I
Primary Parameters of DUTs

DUT	V_{TH}	Rated Current	$R_{DS,ON}$	Device Type
DUT75-A	2.80V	44A	75mΩ	PG
DUT80-B	2.70V	31A	80mΩ	DT
DUT80-C	2.75V	29A	80mΩ	PG
DUT40-D	2.80V	76A	40mΩ	PG
DUT40-E	2.70V	55A	40mΩ	DT
DUT40-F	2.90V	54A	40mΩ	PG

electronics applications. Experimental observations reveal a surge current flowing from the source to the drain I_{SD}, while the gate-to-Kelvin-source voltage V_{GS} is utilized to regulate the channel turn-off. Under the specified surge current pulse period of 10 ms, the V_{GS} applied between the gate and Kelvin source terminals remains equivalent to the gate-to-power-source voltage in terms of channel deactivation control effectiveness. The I_{SD} waveform comprises two dominant components, formulated as [16]:

$$I_{\mathrm{SD}} = I_{\mathrm{F}} + I_{\mathrm{channel}} \tag{1}$$

where I_{F} denotes the body diode forward current and I_{channel} represents the residual channel conduction current. As indicated by the red arrows in Fig. 1(c) and (d), the I_{F} conduction paths differ significantly between symmetrical Planar Gate (PG) and symmetric Double Trench (DT) SiC MOSFET. When the gate-source voltage V_{GS} drops below the threshold voltage V_{TH}, the channel enters a quasi-blocking state, causing I_{SD} to be dominated by I_{F}. However, the accumulation of gate charge induced by SiC/SiO_2 interface defects generates a non-negligible I_{channel}, as evidenced by the green arrow trajectories in Fig. 1(c) and (d). This interfacial degradation mechanism leads to compromised surge current controllability.

The principal operational parameters of the Device Under Tests (DUTs), as tabulated in Table I, were acquired under standard laboratory conditions (300 K). The devices were classified into two discrete groups based on nominal drain-source on-resistance (80 mΩ and 40 mΩ), while maintaining comparable threshold voltage V_{TH}. To evaluate the disparity in surge current tests between planar-gate and trench-gate configurations, this study conducted comparative electrical characterization on six 1200V commercial SiC MOSFETs.

B. Test Setups

The simplified surge current test schematic and experimental setup are illustrated in Fig. 2 and Fig. 3 respectively. The

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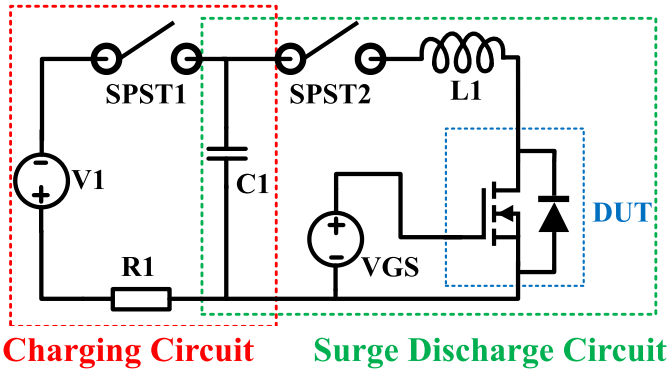


Fig. 2. Simplified schematic of the surge current test circuit.

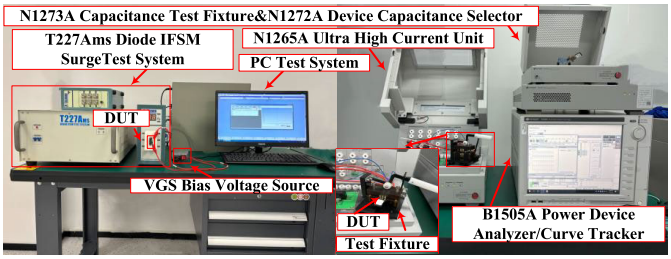


Fig. 3. Photograph of the surge current test platform.

circuit comprises two functional modules: (1) a charging loop for energy storage and (2) a surge discharge loop for transient current injection. A gate bias voltage V_{GS} is employed to maintain the DUT in the off-state during testing. The T227Ams IFSM Test System enables configurable surge testing with programmable pulse characteristics (width: 0.7–10 ms, waveform: sinusoidal, interval: 1–60 s). Electrical characterization is conducted using a Keysight B1505A Power Device Analyzer integrated with an N1265A high-current expander (10kA pulse capability), N1273A/N1272A capacitance measurement subsystems, and application-specific test fixtures.

A sinusoidal half-wave surge current with 10 ms pulse width (50 Hz line frequency synchronized) is adopted to emulate industrial fault conditions. Gate-source bias configurations of $V_{GS} = 0$ V and $V_{GS} = -5$ V are applied through Kelvin connections to investigate the voltage-dependent surge robustness. Post-stress electrical parameter analysis, including threshold voltage (V_{TH}), on-resistance (R_{DSON}), and leakage current, is systematically performed to assess device degradation in accordance with AEC-Q101 qualification standards.

III. Test Results and Discussion

A. Pre-Experimental Results

As illustrated in Fig. 4, two gate-source bias configurations ($V_{GS} = 0$ V and $V_{GS} = -5$ V) were implemented to evaluate surge withstand capabilities under half-open state and closed state. Experimental results demonstrate that the maximum surge current (I_{Max}) of all six DUTs remains independent of channel conduction states, with the body diode current constituting the dominant surge current path. The gate bias voltage exhibits negligible influence on surge performance.

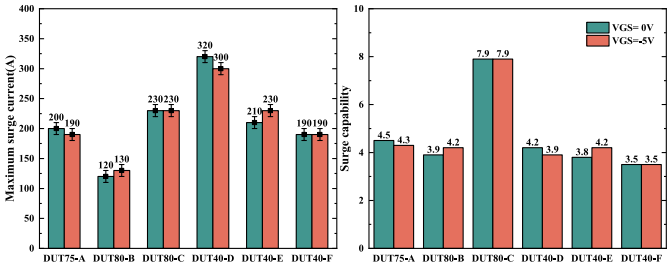


Fig. 4. Maximum surge currents and surge capabilities of SiC MOSFETs.

The surge capacity is defined as [23]:

$$\text{Surge capacity} = \frac{I_{\text{Max}}}{I_{\text{Rated}}} \tag{2}$$

where I_{Rated} denotes the nominal current from Table I. DUT80-C demonstrates surge capability of 7.9, whereas other devices cluster around 4. This disparity correlates with structural parameters including body diode forward recovery characteristics, current density, active chip area, and thermal impedance of the devices.

B. Step Surge Current Test and Results

The surge current step length was optimized through pre-experimental characterization with test intervals exceeding two hours to ensure sufficient cooling of DUTs. As shown in Fig. 5 and Fig. 6, surge current transient analysis reveals a 10ms sinusoidal surge activation window spanning 6000–16000 μs. During the initiation subphase (6000–6300 μs), abrupt source-drain voltage transitions synchronize with body diode operation mode switching from reverse-blocking to forward-conduction. Experimental measurements demonstrate that the on-voltage of the body diode in the off state is higher than that in the half-open state, indicating divergent conduction mechanisms during surge inception. This operational behavior originates from source-to-P-body potential gradient induced body effect, which progressively attenuates threshold voltage. Premature channel conduction occurs when forward-biased PN junction conditions coincide with threshold voltage reduction below critical levels, as governed by [23]:

$$V_{TH} = V_{TH0} + \gamma(\sqrt{2\phi_F + |V_{SB}|} - \sqrt{2\phi_F}) \tag{3}$$

where V_{TH0} denotes the zero-bias threshold voltage, the body effect coefficient γ, the bulk Fermi potential ϕ_F, and the body-source voltage V_{SB}.

When the surge current exceeds the rated value, the body diode predominantly conducts the majority of the surge current. For PG SiC MOSFETs such as DUT75-A, DUT80-C, DUT40-D, and DUT40-F in their off-state, the maximum surge current exhibits only marginal superiority compared to their half-open state. Notably, the surge current conducted through the channel remains negligible when contrasted with that carried by the body diode.

However, the surge waveforms of DT SiC MOSFETs DUT80-B and DUT40-E exhibit significant differences compared to those observed in the other four PG SiC MOSFETs,

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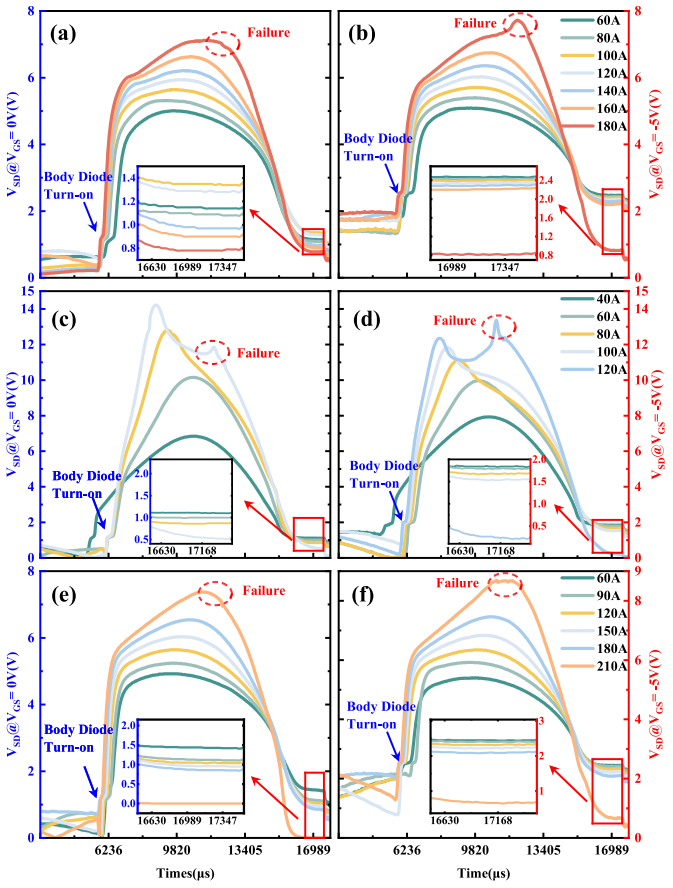


Fig. 5. Step surge current V_{SD}-Time waveforms (a) DUT75-A at $V_{GS} = 0$ V. (b) DUT75-A at $V_{GS} = -5$ V. (c) DUT80-B at $V_{GS} = 0$ V. (d) DUT80-B at $V_{GS} = -5$ V. (e) DUT80-C at $V_{GS} = 0$ V. (f) DUT80-C at $V_{GS} = -5$ V.

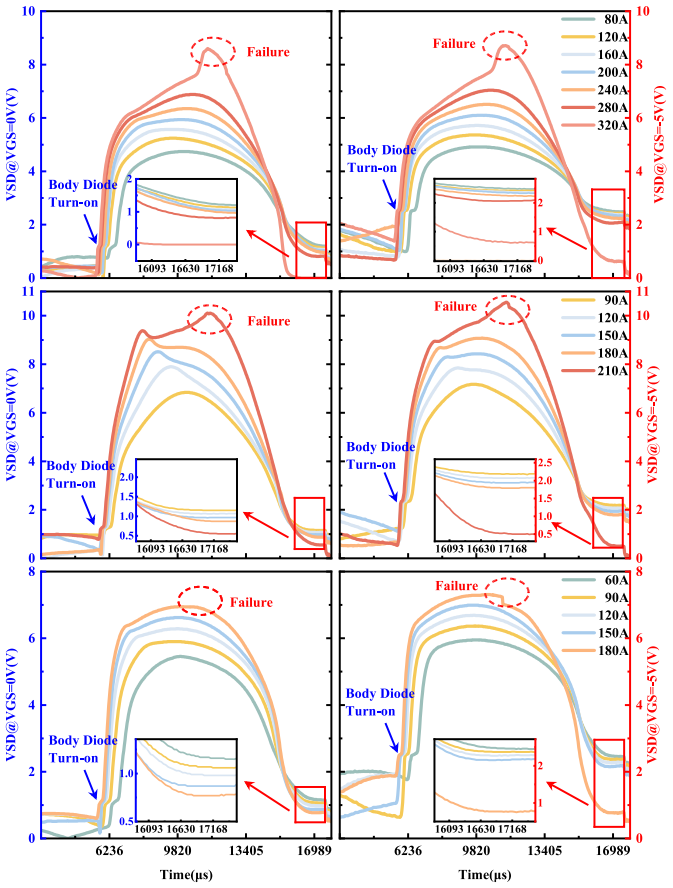


Fig. 6. Step surge current V_{SD}-Time waveforms (a) DUT40-D at $V_{GS} = 0$ V. (b) DUT40-D at $V_{GS} = -5$ V. (c) DUT40-E at $V_{GS} = 0$ V. (d) DUT40-E at $V_{GS} = -5$ V. (e) DUT40-F at $V_{GS} = 0$ V. (f) DUT40-F at $V_{GS} = -5$ V.

with distinct characteristics primarily manifested in the following aspects.

Firstly, the V_{SD} exhibits both a higher peak magnitude and a shorter time to reach maximum value, indicating weaker suppression capability on V_{SD} rise compared to PG SiC MOSFETs with equivalent on-resistance specifications. As shown in Figures 7(a) and (b), the $T_{VSD,MAX}$ (time required to reach V_{SD} peak) demonstrates a progressively increasing trend for all PG SiC MOSFETs, whereas DT SiC MOSFETs exhibit the opposite characteristic. This originates from the conductivity modulation effect-induced electron accumulation: intensive electron storage in the N-drift region significantly reduces body diode resistance, thereby effectively suppressing further V_{SD} elevation. The deeper P-Body and P+ regions diminish the doping concentration gradient, resulting in trench-type devices manifesting higher resistive characteristics in the body diode current path. Consequently, the body diode current proportion increases rapidly with significantly elevated V_{SD} peak values.

Secondly, when subjected to the same surge current, V_{SD} takes slightly longer to reach its maximum value at $V_{GS} = 0$ V compared to $V_{GS} = -5$ V, while also attaining a higher peak magnitude. At $V_{GS} = 0$ V, the surge current is predominantly composed of a larger channel current, which prolongs the transition period for the body diode current to become the dominant conduction path. The interplay between channel current and body diode current is more pronounced than in the off-state, coupled with slower resistivity variations, resulting in a higher V_{SD} peak under identical surge currents. Implementing $V_{GS} = -5$ V effectively mitigates the surge current impact on the body diode, thereby enhancing the surge reliability of DT SiC MOSFETs.

Thirdly, under both off-state and half-open state operating conditions, the time required for devices to reach V_{SD} peak values shows a decreasing trend with increasing surge current. This phenomenon stems from dual mechanisms induced by surge current density enhancement: (1) device temperature rise causes carrier mobility degradation, leading to increased body diode forward voltage drop; (2) elevated temperatures promote the generation of high-energy, high-mobility hot carriers, thereby accelerating the current peaking process.

Fourthly, during the final failure stage experiments, measurement data reveal a dual-peak in the V_{SD} temporal response of DT SiC MOSFETs. The initial peak originates from instantaneous resistivity variation between source-drain terminals during surge current application, while the subsequent peak corresponds to thermally-dominated phase transitions exhibiting delayed response relative to current variations. This bimodal temperature-dependent behavior demonstrates a multi-stage warming process during device failure.

Fig. 7(c) and (d) illustrate the effect of setting different V_{GS} on the device diode turn-on voltage. As the surge

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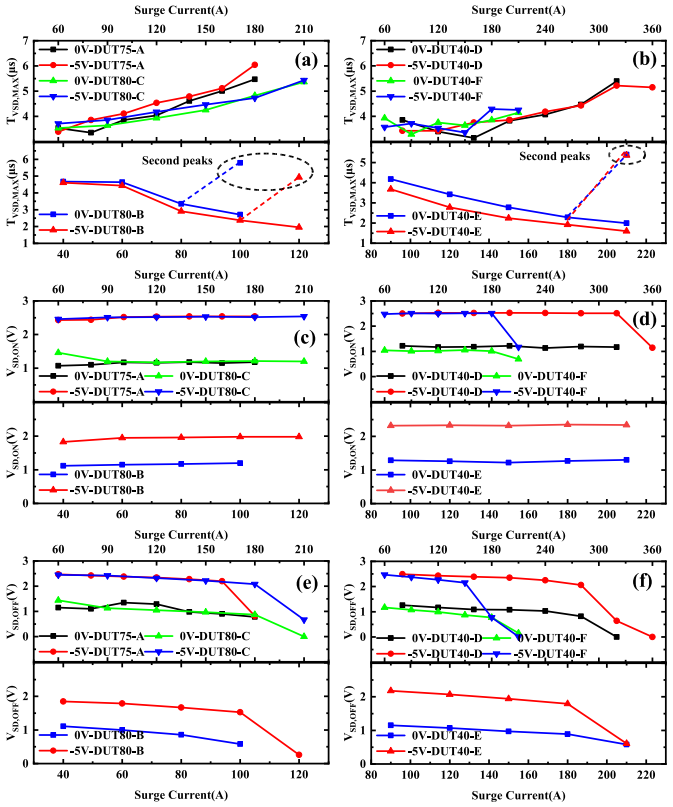


Fig. 7. Time to $V_{SD,MAX}$ (a) 80 mΩ. (b) 40 mΩ. Body diode turn-on voltage $V_{SD,ON}$ (c) 80 mΩ. (d) 40 mΩ. Body diode voltage $V_{SD,OFF}$ at end of surge current test (e) 80 mΩ. (f) 40mΩ.

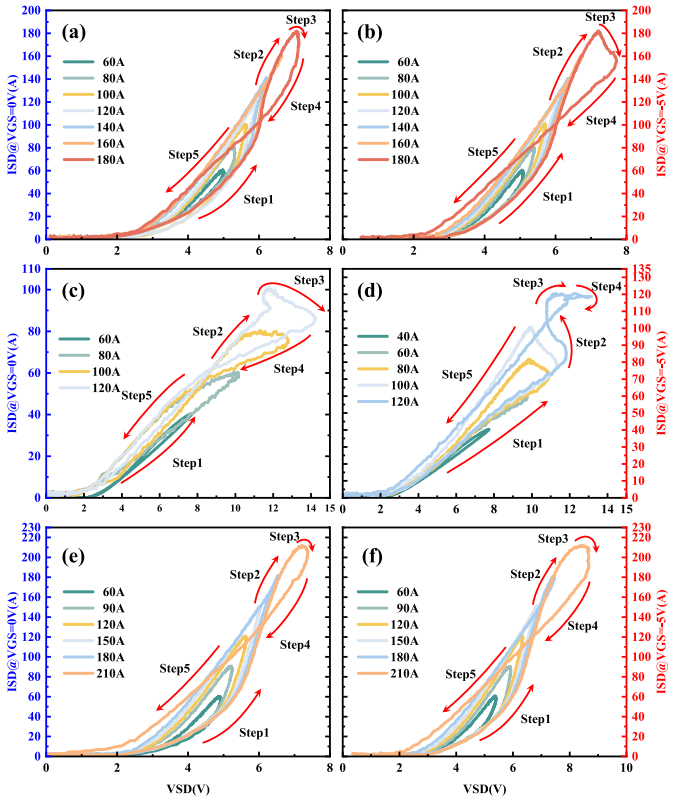


Fig. 8. Step surge current I_{SD}-V_{SD} waveforms (a) DUT75-A at $V_{GS} = 0$ V. (b) DUT75-A at $V_{GS} = -5$ V. (c) DUT80-B at $V_{GS} = 0$ V. (d) DUT80-B at $V_{GS} = -5$ V. (e) DUT80-C at $V_{GS} = 0$ V. (f) DUT80-C at $V_{GS} = -5$ V.

current increases, $V_{SD,ON}$ does not produce a significant change. Setting $V_{GS} = 0$ V significantly reduces $V_{SD,ON}$ compared to $V_{GS} = -5$ V. When $V_{GS} = -5$ V, the channel is in a completely off-state and the surge current is effectively isolated. The body diode requires a higher turn-on voltage to be applied to turn it on due to the higher built-in electric field.

Fig. 7(e) and (f) clearly illustrate that as the surge current increases, the body diode barrier voltage reduces $V_{SD,OFF}$ decreases after the surge impact. The enhancement of surge stress has a positive effect on the degradation of the body diode until the device fails completely.

C. Temperature Effect on Step Surge Current Test

During surge tests, the current flowing through the body diode exceeds their rated operational current, leading to a substantial rise in junction temperature. The temperature variation during surge tests can be inferred from the I_{SD}-V_{SD} curves. Fig. 8 and Fig. 9 present the I_{SD}-V_{SD} curves of six DUTs, where the observed hysteresis in the curves is attributed to thermal hysteresis during temperature fluctuations. This phenomenon arises from the junction temperature disparity between the surge current's rising and falling phases, ultimately manifesting as asymmetric voltage waveforms.

The waveforms prior to applying maximum surge current stress exhibit a counterclockwise hysteresis loop in the I_{SD}-V_{SD} curves. Throughout the testing, the DUTs operated in bipolar mode, with surge current primarily conducted through the body diode. As the surge current increased, the V_{SD} became clamped. Among the six tested DUTs, four PG DUTs demonstrated clamping voltages below 8 V, while the remaining two DT DUTs exhibited clamping voltages exceeding 8 V.

Fig. 8 and Fig. 9 reveal a distinctive "figure-eight hysteresis" pattern in all tested devices following the attainment of peak surge current. During this phase, V_{SD} no longer exhibits clamping behavior, suggesting that the SiC MOSFETs are not operating exclusively in bipolar mode. The observed transition implies the presence of additional physical mechanisms driving unipolar-mode operation, necessitating further analysis to elucidate the underlying causes of this bipolar-to-unipolar mode shift.

The I_{SD}-V_{SD} characteristic curve serves as an indicator of R_{SD} (defined as the reciprocal of the I_{SD}-V_{SD} slope) variations in SiC MOSFETs during surge events. The stages of change in I_{SD}-V_{SD} curve can be divided into the following steps [16].

Step1: During the initial surge current phase (0–2 ms), the body diode operates in partial activation mode, where current conduction primarily relies on minority carriers, resulting in a high-resistance state. The elevated V_{SD} stems from this resistive behavior. The initial temperature rise enhances electron mobility, inducing positive temperature coefficient (PTC) characteristics, while thermal accumulation remains insufficient to dominate device behavior.

Step2: In the conductivity modulation-dominated phase (2–4 ms), full activation of the body diode enables intense conductivity modulation. Hole injection from the P-Body into the n-drift region dramatically increases minority carrier

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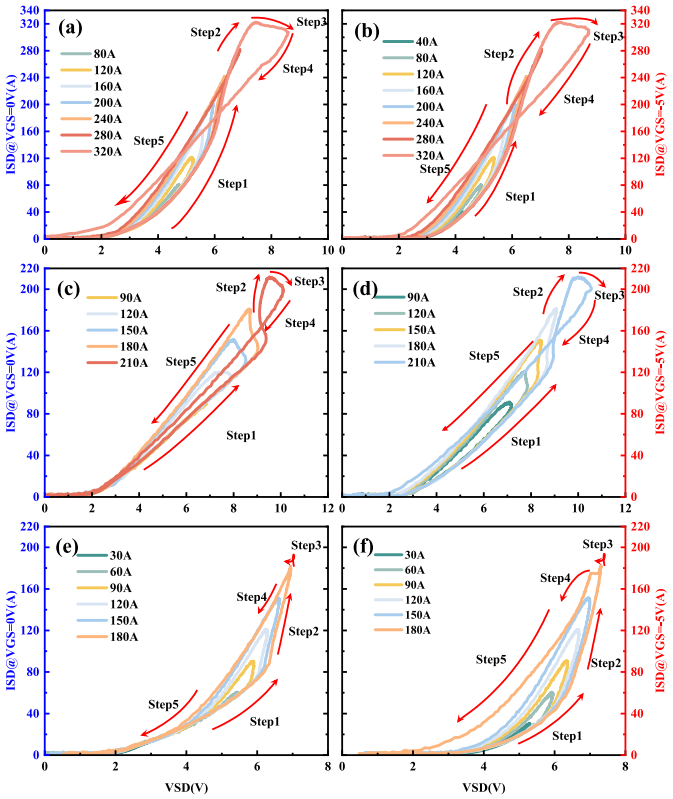


Fig. 9. Step surge current I_{SD}-V_{SD} waveforms (a) DUT40-D at $V_{GS} = 0$ V. (b) DUT40-D at $V_{GS} = -5$ V. (c) DUT40-E at $V_{GS} = 0$ V. (d) DUT40-E at $V_{GS} = -5$ V. (e) DUT40-F at $V_{GS} = 0$ V. (f) DUT40-F at $V_{GS} = -5$ V.

concentration. To preserve charge neutrality, electron density in the n-drift region rises correspondingly, leading to a sharp reduction in resistivity. The delayed junction temperature rise begins to further decrease resistance by lowering the PN junction barrier potential, thereby limiting the voltage from increasing any further.

Step3: During the thermal-induced negative resistance phase (4–5.5 ms), accelerated junction heating causes exponential growth in intrinsic carrier concentration, overriding mobility degradation effects and reinstating PTC behavior. Synergy between hot carrier effects and conductivity modulation triggers negative differential resistance (NDR), manifested as V_{SD} reduction with increasing current. The delayed thermal response amplifies this nonlinear characteristic.

Step4: In the initial current recession phase (5.5–6.5 ms), the surge current starts declining while junction temperature remains near its peak. The device enters a negative temperature coefficient (NTC) regime. The efficacy of the current began to diminish, while the influence of the temperature persisted. The device is no longer in the state of negative resistance. At equivalent current levels, resistance exceeds that observed in Step 2, forming the ascending branch of a thermal-electrical hysteresis loop.

Step5: During the recovery phase (6.5–10 ms), as current decays to steady-state levels, thermal relaxation governs device behavior. PTC effects regain dominance, though residual heat delays resistance recovery. The resistivity trajectory demonstrates asymmetry between current ascending and descending

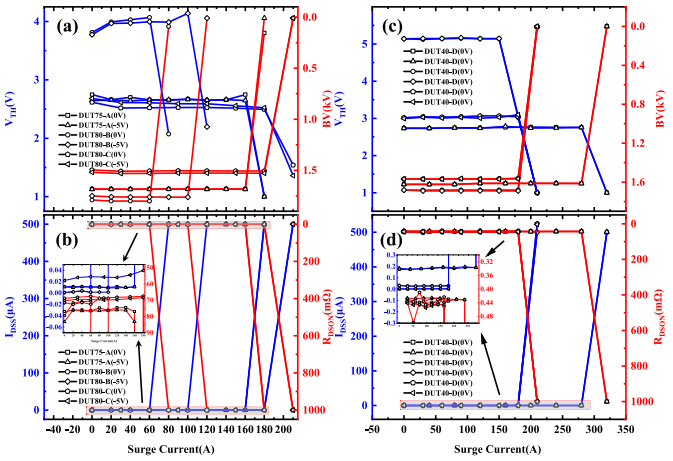


Fig. 10. Static characteristic parameters. (a) 80 mΩ SiC MOSFETs V_{TH} & BV. (b) 80 mΩ SiC MOSFETs I_{DSS} & R_{DSON}. (c) 40 mΩ SiC MOSFETs V_{TH} & BV. (d) 40 mΩ SiC MOSFETs I_{DSS} & R_{DSON}.

phases, attributable to coupled effects of decaying conductivity modulation and temperature gradient relaxation,ensuring that the decline phase maintains a lower resistance than Step 1.

R_{SD} exhibits a negative correlation with carrier concentration, where elevated carrier density substantially reduces resistivity. During the current descent phase (Step 5), the carrier concentration surpasses that of the initial ascent phase (Step 1) due to thermal hysteresis and prior carrier accumulation, resulting in lower R_{SD}. The delayed recovery of minority carriers in the body diode region to equilibrium concentration creates persistent high carrier density during current recession, maintaining low resistance and forcing the current path to follow body diode-dominated conduction, thereby mimicking diode-like I-V characteristics. Under excessive surge current stress, partial current flow through the vulnerable channel region induces localized junction temperature escalation, ultimately triggering thermal runaway-induced failure mechanisms such as source metal melting and gate-source short-circuiting.

As shown in Fig. 10, V_{TH}, I_{DSS}, BV and R_{DSON} revealed consistent failure signatures across all devices: $V_{TH} = 1$ V, $I_{DSS} = 500\mu$A, BV $= 0$ V and $R_{dson} = 1000$ Ω (attributed to instrument-protected clamping). The sharp V_{TH} reduction indicates gate control failure, while BV collapse to 0 V signifies V_{SD} breakdown. I_{DSS} exceeding the datasheet threshold (>1 μA) confirms device failure, and anomalous R_{dson} elevation suggests alternative conductive pathways between source-drain terminals. Unaltered parameters under sub-maximal surge stress demonstrate robust surge immunity of the DUT.

D. Repetitive Surge Current Test and Results

Repeated surge current tests constitute the thermal fatigue assessment method, in which subcritical surge currents (i.e., 60% and 90% of the maximum failure current) are cyclically applied. Systematically change the pulse intervals (0.5 s and 1 s) to adjust the heat dissipation efficiency, thereby studying the degradation mechanism dominated by heat accumulation. This scheme emphasizes that the

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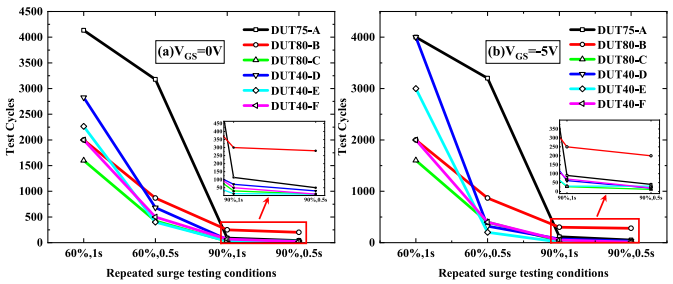


Fig. 11. Relationship between repetitive surge current and the number of surges corresponding to the pulse interval (a) $V_{GS} = 0$ V. (b) $V_{GS} = -5$ V.

TABLE II
EXPERIMENTAL ARRANGEMENT FOR REPEATED SURGE TEST

Device Name	60% Surge Current	90% Surge Current	Pulse Interval
DUT75-A	108A	162A	0.5s
			1s
DUT75-B	72A	108A	0.5s
			1s
DUT75-C	140A	180A	0.5s
			1s
DUT40-D	180A	270A	0.5s
			1s
DUT40-E	138A	207A	0.5s
			1s
DUT40-F	114A	171A	0.5s
			1s

temperature lag phenomenon is no longer the main driving factor for device deterioration under repeated electrical stress. The detailed experimental configuration is shown in Table II. Since the device needs to be cooled to room temperature for the test of static characteristic parameters, the changes of V_{TH}, BV, I_{DSS} and R_{DSON} after repeated surges all show that they remain basically unchanged before failure and undergo sudden changes after failure, which is similar to the experimental results of step surge current.

Repetitive surge current testing reveals that incomplete inter-pulse cooling induces progressive thermal accumulation, thereby attenuating temperature hysteresis effects. The parametric synergy between current amplitude and pulse interval critically governs thermal dynamics: elevated current magnitudes and reduced intervals synergistically intensify joule heating, precipitating nonlinear reduction in operational lifetime. Sub-threshold current stresses (e.g., 60% of maximum rating) coupled with extended pulse intervals enhance cycle tolerance by mitigating thermal transients, whereas high-current conditions (e.g., 90%) exacerbate thermal fatigue through accelerated energy deposition. These interactions constitute critical determinants of cumulative degradation under cyclic electrical overstress.

IV. SURGE CURRENT TEST FAILURE ANALYSIS

Initial non-destructive inspection of the die, lead frame, and interconnects within TO247-4L packaging SiC MOSFETs was conducted using C-mode Scanning Acoustic Microscopy (C-SAM), as illustrated in Fig. 12. Based on the variations in internal die defects identified through C-SAM analysis, the chip failure modes were categorized into two distinct groups.

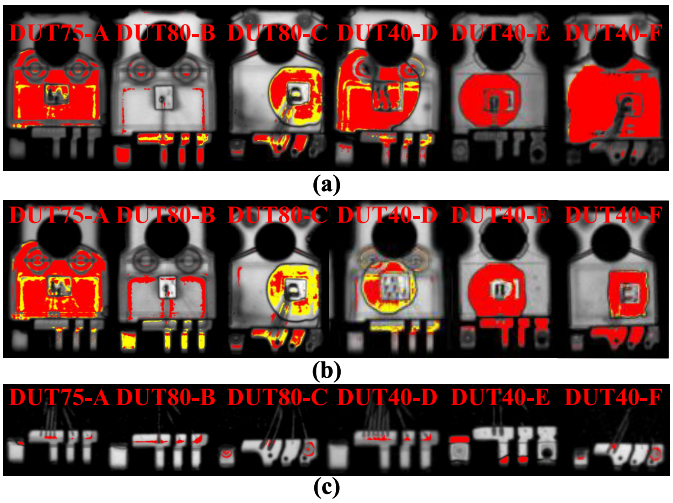


Fig. 12. C-SAM of each DUT (a) Base island layer (b) Chip layer (c) Pin layer.

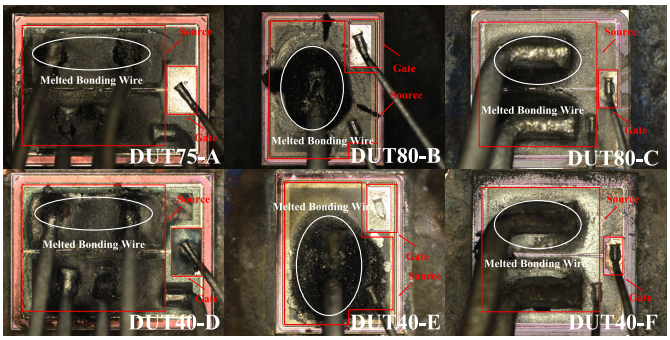


Fig. 13. Optical microscopy of 6 DUTs after decapsulation.

Primary Failure Mode (Type I Defects): C-SAM analysis revealed macro-scale delamination voids at die encapsulation interfaces, as shown in Fig. 12(a) and (b), predominantly localized at chip/molding compound and lead frame/molding compound boundaries. These defects critically compromise hermetic sealing integrity while creating localized thermal bottlenecks due to the substantial thermal conductivity contrast between trapped air and molding compound. Under surge current operation, synergistic heating effects between these thermal hotspots and intrinsic junction temperature induce temperature gradient amplification. Catastrophic thermal runaway occurs.

Secondary Phenomenon (Type II Defects): Micro-scale delamination features were observed at pin/lead bonding interfaces, exhibiting low signal-to-noise ratios in C-SAM imaging, as shown in Fig. 12(c). These defects negligibly influence thermal runaway as they preserve primary heat dissipation pathways within the package architecture.

Decapsulated chips were examined via optical microscopy to determine failure mechanisms. All DUTs exhibited distinct melting and burnout of the aluminum bonding wires at the source terminals under surge stress, as shown in Fig. 13. This observation confirms that the localized temperatures generated during surge stress exceeded the melting point of aluminum (660°C), directly correlating with thermal overstress-induced interconnect failure.

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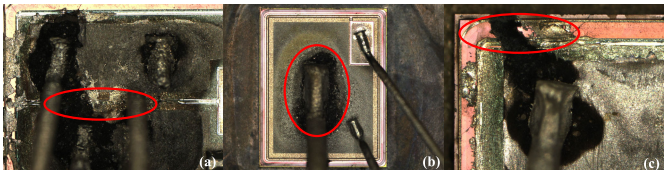


Fig. 14. Different burn-out scenarios (a) Aluminum melting of the bonding wire metal followed by penetration into the gate (b) Source bonding wire metal melting only (c) Burn-out of the terminal region.

Failure modes are categorized into three types based on burn-out locations.

Type I (Fig. 14(a)): Molten aluminum bonding wires at the source penetrate into the gate and drain, creating a three-terminal (gate-source-drain) short circuit.

Type II (Fig. 14(b)): Exclusive to DT DUTs, thermal expansion coefficient (CTE) mismatch between the polysilicon gate, SiO_2 gate oxide, and aluminum induces gate oxide cracks. Molten aluminum infiltrates these cracks, forming a gate-source short while preserving isolation integrity.

Type III (Fig. 14(c)): Termination region burnout arises from surge current crowding. The p-doped termination (connected to the source) allows parallel current flow through both the cell body diode and termination diode. Current convergence near the termination generates extreme current density. In trench-gate devices, compact overlap between termination and cell metals restricts current spreading, elevating R_{SD} and accelerating thermal runaway via localized joule heating.

Cross-sectional Scanning Electron Microscope(SEM) analysis reveals distinct failure characteristics: In Fig. 15(a), breakdown-type burn traces are observed spanning from the source electrode on the chip surface to the drain electrode at the bottom, with the burn size progressively increasing along the source-to-drain path. Fig. 15(b) demonstrates that molten aluminum infiltrates and erodes the gate oxide passivation layer, inducing gate-source short-circuiting. In Fig. 15(c) and (d), breakdown occurs between the N+ and P+ regions of adjacent cells, attributed to the narrow spacing between N+ source regions in neighboring cells, where lateral electric field concentration triggers forward-biased p-n junction breakdown in the structure.

The results indicate that the surge failure mechanism originates from device overheating during the surge test, which melts the aluminum bonding wires. The molten metal not only compromises the hermeticity of the packaging, inducing delamination and void formation, but also infiltrates and erodes the gate oxide passivation layer. This leads to thermal damage on the chip surface, bonding wires, and termination regions, ultimately causing simultaneous short-circuiting of the gate, source, and drain.

V. Verification and Analysis of Surge Failure Mechanisms

A. Package Level Surge Failure Simulation

Section III demonstrates that the device failures originated from bonding wire package degradation in the DUTs. Package level electro-thermal transient distribution simulations under surge conditions were conducted on TO-247-4L packaged SiC MOSFETs to validate the failure analysis results.

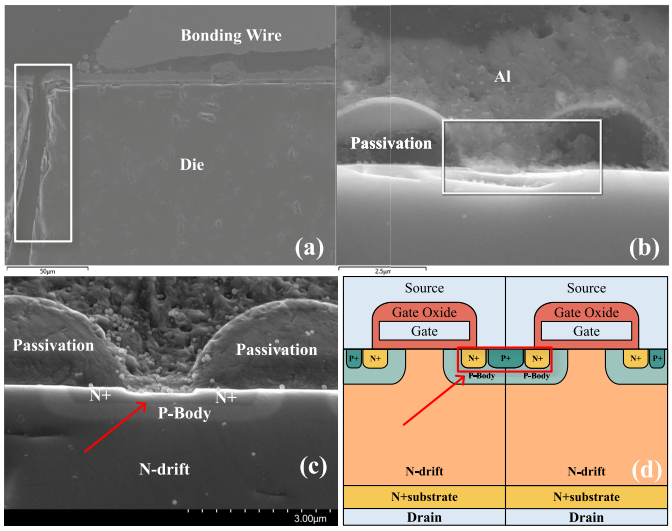


Fig. 15. SEM results (a) DS breakdown burnout morphology (b) metallic aluminum erosion of the gate oxygen passivation layer (c) Breakdown in P+and N+regions (d) schematic of the metastructure of the P+ region breakdown.

The 3D thermal simulation model incorporates the chip structure (SiC die), gate-source-drain metallic bonding wires, solder layer, and lead frame. Transient temperature field distribution, driven by Joule heating generation, was simulated through the coupling of the "Solid heat transfer" and "Electric field current" modules. The governing equation for "Solid heat transfer" is:

$$\rho c_p \frac{\partial T}{\partial t} + \rho c_p \mathbf{u} \cdot \nabla T + \nabla \cdot \mathbf{q} = Q + Q_{ted} \tag{4}$$

$$\mathbf{q} = -k \nabla T \tag{5}$$

where ρ is the density, c_p is the specific heat capacity at constant pressure, T is the temperature, t is the time, $\mathbf{u}$ is the velocity vector, ∇ is the nabla operator, $\mathbf{q}$ is the heat flux vector, k is the thermal conductivity, Q is the volumetric internal heat generation rate, and Q_{ted} is the thermal energy generated by radiation.

The governing equation for "Electric field current" is:

$$\nabla \cdot \mathbf{J} = Q_{i,v} \tag{6}$$

$$\mathbf{J} = \sigma \mathbf{E} + \frac{\partial \mathbf{D}}{\partial t} + \mathbf{J}_e \tag{7}$$

$$\mathbf{E} = -\nabla V \tag{8}$$

where $\mathbf{J}$ is the current density vector, $Q_{i,v}$ is the volumetric charge generation rate, σ is the electrical conductivity, $\mathbf{E}$ the electric field intensity vector, $\frac{\partial \mathbf{D}}{\partial t}$ is the time derivative of the electric displacement vector, $\mathbf{J}_e$ is the external source current density, and V is the electric potential.

The material parameters for different packaging structures at room temperature are assigned as listed in Table III. During surge testing, σ of the SiC die varies with the injection of surge current. The surge current induces Joule heating, while temperature simultaneously alters σ, resulting in mutual coupling between surge current and temperature. Failure analysis results

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TABLE III
MATERIAL PARAMETERS

Layer	Material	k(W/(m·K)	c_p(J/K)	$\sigma(T, J)$(S/m)	ρ(g/cm^3)	ε_r
Die	SiC	280	650	sigma	3.2	9.7
Die-Attch	$PbSn_5$	44	150	1.10×10^6	/	/
Lead	Cu	397	385	5.96×10^6	8.94	/
Bonding Wires	Al	230	897	3.77×10^7	2.7	/

reveal transient high-temperature variations during the surge test, with the conductivity-temperature relationship expressed as [27]:

$$\sigma(T) = \sigma_0 \left(\frac{T_0}{T(t)} \right)^{\beta} \tag{9}$$

where σ_0 is the initial electrical conductivity (at $T = T_0$), β is a material-dependent constant typically ranging from 1.5 to 2.5, and T_0 represents the ambient temperature. The Joule heating generated by the surge current leads to temperature rise, and its dynamic equation under the adiabatic approximation (transient heating with negligible thermal dissipation) is expressed as [27]:

$$C_{\text{th}} \frac{\mathrm{d}T}{\mathrm{d}t} = \frac{I_{\text{surge}}^2 L}{A\sigma(T(t))} \tag{10}$$

where C_{th} denotes the thermal capacitance, L is the thickness of the SiC die, and A is the chip area.

Combining equations (9) and (10), the time-dependent function of σ with respect to the surge current can be derived as:

$$\sigma(t) = \sigma_0 \left[1 + \frac{(\beta+1) I_{\text{surge}}^2 L}{C_{\text{th}} A \sigma_0 T_0^{\beta+1}} t \right]^{-\frac{\beta}{\beta+1}} \tag{11}$$

The transient thermal distribution of the metal layer on the SiC die surface and the gate-source bonding wires is simulated without considering the thermal influence of the package molding compound. The current density $I = 200\sin(2\pi \cdot 50 \cdot t)$ is applied to simulate surge-induced failure in the DUT75-A, with current flowing from the Source to the Drain. The lead frame is set as the initial boundary condition at room temperature (295 K). As shown in Fig. 16, the transient thermal distribution at different surge stages is illustrated. The device reaches its peak temperature 5–6 ms after the surge event, which is sufficient to melt the bonding wires and cause device failure.

B. Transient Junction Temperature Characterization

During surge tests, heat transfers from the high-temperature region (device junction) to the low-temperature region (ambient environment). The rise in junction temperature originates from the conversion of power dissipation generated during device operation into thermal energy, which is transferred to the ambient environment through the thermal resistance. Based on the transient thermal resistance concept, the junction temperature is calculated by accounting for the ambient

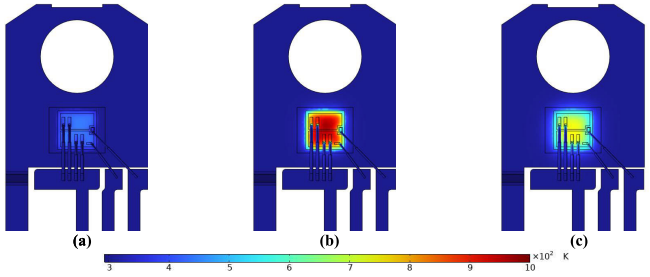


Fig. 16. TO247 package surge simulation at different moments (a) t = 2ms (b) t = 6ms (c) t = 9ms.

TABLE IV
EXPERIMENTAL ARRANGEMENT OF THERMAL RESISTANCE TEST

DUT	Length	Width	Test Current	Pressure
DUT75-A	3.4 (mm)	2.7 (mm)	15/20/25A	0.3/0.4/0.5/0.6 (N/m)
DUT80-B	3.0 (mm)	2.4 (mm)	12/15/18A	0.3/0.4/0.5/0.6 (N/m)
DUT80-C	2.9 (mm)	2.9 (mm)	12/15/18A	0.3/0.4/0.5/0.6 (N/m)
DUT40-D	4.1 (mm)	3.7 (mm)	20/25/30A	0.3/0.4/0.5/0.6 (N/m)
DUT40-E	4.5 (mm)	3.1 (mm)	20/25/30A	0.3/0.4/0.5/0.6 (N/m)
DUT40-F	2.9 (mm)	2.9 (mm)	10/12/15A	0.3/0.4/0.5/0.6 (N/m)

temperature, transient thermal resistance, and device power dissipation. The governing equation is:

$$T_{\text{J}} = T_0 + Z_{\text{TH}} \times P \tag{12}$$

where T_{J} refers to the temperature of the junction, T_0 is ambient temperature, Z_{TH} is transient thermal resistance from the junction to the surroundings, P is power loss of the device.

To calculate transient thermal resistance, the device thermal resistance must first be experimentally characterized. This study employed the dual-interface thermal resistance testing method to measure the device thermal resistance. To ensure consistency in testing results, experiments were conducted under varying pressures (applied to press the SiC MOSFET onto the cooling plate) and different body diode heating currents, as summarized in Table IV. The heating currents were adjusted across devices to maintain a uniform temperature starting point during cooling. Each device underwent 12 experimental trials, combining three heating currents and four pressures. The heating duration was 60s, followed by a 70s cooling phase with a coolant flow rate of 6.9 L/s, ensuring the device returned to ambient temperature. Representative thermal resistance values for each DUT are illustrated in Fig. 17.

After determining the thermal resistance, the transient thermal resistance is calculated using (13), where P_{H} represents the pulse power applied to the body diode heating, r_θ is the transient thermal resistance. Fig. 18(a) illustrates the temperature evolution of bond wires and surface metal layers in the COMSOL package-level simulation for the DUT75-A case. The simulated results are fitted with temperatures calculated using the transient junction temperature method. Both the peak temperature magnitude and its timing exhibit close agreement, validating the accuracy of the package simulation. This analysis also characterizes the temperature dynamics during

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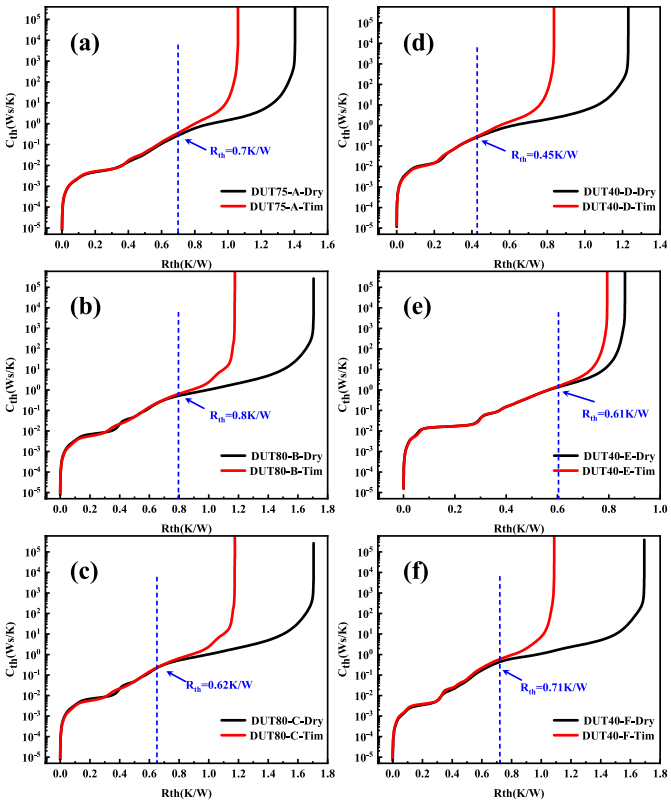


Fig. 17. Typical Steady-State Thermal Resistance for Each Device (a) DUT75-A (b) DUT80-B (c) DUT80-C (d) DUT40-D (e) DUT80-E (f) DUT80-F.

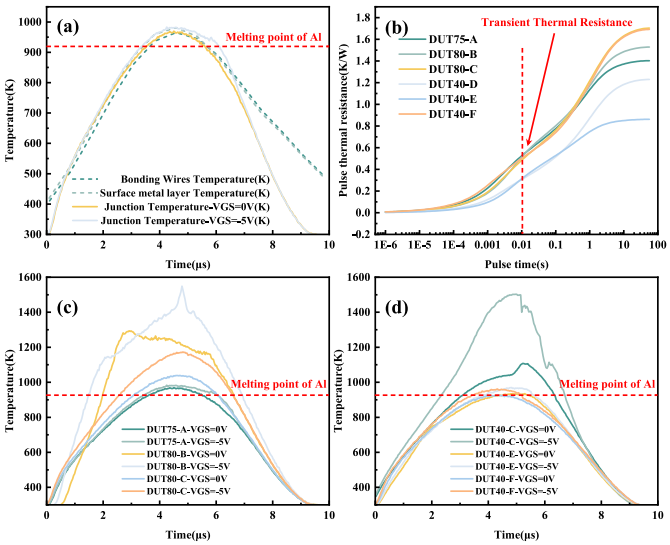


Fig. 18. (a) Plot of package simulation temperature versus transient junction temperature estimation fit (b) Transient thermal resistance of six DUTs (c) Transient junction temperature estimation for 80mΩ SiC MOSFETs (d) Transient junction temperature estimation for 40mΩ SiC MOSFETs.

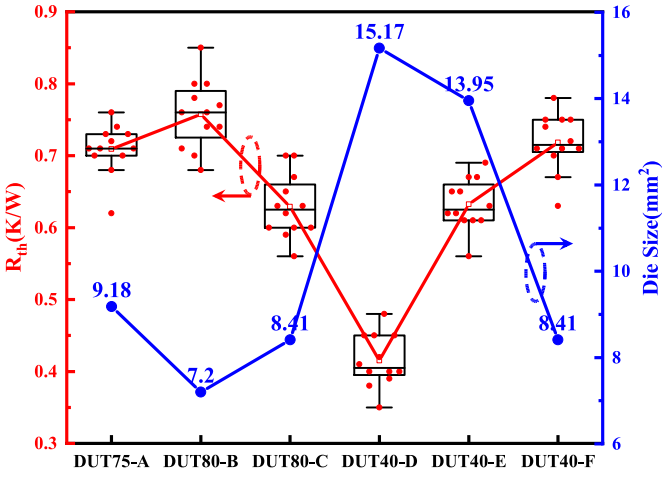


Fig. 19. Device steady-state thermal resistance versus chip area.

the surge process, confirming that device failure originates from aluminum bond wire melting (exceeding the melting point) during the surge, leading to structural burnout. The results are shown in Fig. 18(b). Based on stepped surge current experiments, the transient thermal impedance with a pulse width of 10ms is selected to compute the instantaneous junction temperature during surge testing, as illustrated in Fig. 18(c) and (d). The results indicate that the device exceeds the melting point of aluminum during the surge process, with a duration of 4–6 ms. Within this interval, the test current reaches its maximum value, and the instantaneous power dissipation peaks, causing the aluminum bond wires to melt. Prolonged exposure beyond the aluminum melting point enables molten aluminum to flow and contaminate critical regions such as the gate oxide passivation layer and termination rings, ultimately leading to device failure.

$$r_\theta = \frac{\Delta T_j}{P_{\mathrm{H}}} \tag{13}$$

C. Thermal Resistance and Surge Capacity Correlation Analysis

At the packaging level, the junction temperature of the device depends on the instantaneous power dissipation and transient thermal resistance. The instantaneous power dissipation is determined by the magnitude of the surge current applied experimentally, while the transient thermal resistance correlates with the steady-state thermal resistance and chip area. This relationship holds true for both PG and DT structures under various surge test parameters, confirming that larger chip areas substantially enhance surge reliability by reducing thermal impedance regardless of specific surge test characteristics.

Material variations between devices exhibit negligible impact on surge performance differences. Fig. 19 illustrates the relationship between steady-state thermal resistance and chip area, revealing an inverse proportionality where larger chip areas correspond to lower thermal resistance. Comparing thermal resistance with the results in Fig. 4, thermal resistance also inversely correlates with the maximum surge current, indicating a dependency between surge capability and thermal resistance. For instance, 80 mΩ devices have smaller chip areas than 40 mΩ devices. The thermal resistance variation among 80 mΩ devices is less pronounced compared to 40 mΩ devices, yet their surge capability disparity is more significant. This suggests that for smaller-area chips, minor

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thermal resistance adjustments can substantially enhance surge capability. In TO-247 package design, optimizing chip area and thermal resistance parameters can significantly improve surge reliability.

VI. Conclusion

Through experimental testing, failure analysis, and multiphysics simulation, this paper systematically evaluates the reliability of 1200V PG and DT SiC MOSFETs under single and repetitive surge. Experimental results reveal that DT devices exhibit inferior surge performance compared to PG counterparts under single surge, while repetitive surge testing identifies thermal accumulation as a critical failure accelerator, with short pulse intervals significantly reducing device lifespan. Failure analysis confirms that the physical failure mechanisms involve bond wire melting-induced gate-source short circuits and terminal region burnout. By establishing an electrothermal coupling model of TO247-4L packaging via COMSOL, the transient temperature field during surge events is reconstructed, revealing that bond wire temperatures exceed the melting point of aluminum within 5–6 ms. A transient thermal resistance model is proposed to elucidate junction temperature dynamics, demonstrating an inverse correlation between thermal resistance and chip area. Enlarging the chip area substantially enhances surge reliability by reducing thermal impedance.

The superiorities of our method over existing approaches include: (1) it enables real-time estimation of junction temperature under surge conditions through transient thermal resistance, whereas traditional steady-state models fail to capture rapid thermal transients. (2) the package-level simulation accounts for bonding wire and encapsulation effects, providing a more realistic failure analysis compared to device-level TCAD simulations. (3) the combination with surge tests and failure analysis ensures high accuracy and practicality, addressing gaps in previous studies that focused narrowly on device physics.

Future work will focus on advanced packaging materials, thermal design improvements, and long-term reliability validation under practical operating conditions to further enhance model robustness.

References

[1] M. Buffolo et al., "Review and outlook on GaN and SiC power devices: Industrial state-of-the-art, applications, and perspectives," *IEEE Trans. Electron Devices*, vol. 71, no. 3, pp. 1344–1355, Mar. 2024, doi: 10.1109/TED.2023.3346369.

[2] K. Puschkarsky, T. Grasser, T. Aichinger, W. Gustin, and H. Reisinger, "Review on SiC MOSFETs high-voltage device reliability focusing on threshold voltage instability," *IEEE Trans. Electron Devices*, vol. 66, no. 11, pp. 4604–4616, Nov. 2019, doi: 10.1109/TED.2019.2938262.

[3] M. R. Nielsen et al., "High-power electronic applications enabled by medium voltage silicon-carbide technology: An overview," *IEEE Trans. Power Electron.*, vol. 40, no. 1, pp. 987–1011, Jan. 2025, doi: 10.1109/TPEL.2024.3442483.

[4] H. Lee, V. Smet, and R. Tummala, "A review of SiC power module packaging technologies: Challenges, advances, and emerging issues," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 239–255, Mar. 2020, doi: 10.1109/JESTPE.2019.2951801.

[5] X. She, A. Q. Huang, Ó. Lucía, and B. Ozpineci, "Review of silicon carbide power devices and their applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8193–8205, Oct. 2017, doi: 10.1109/TIE.2017.2652401.

[6] X. Yuan, I. Laird, and S. Walder, "Opportunities, challenges, and potential solutions in the application of fast-switching SiC power devices and converters," *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 3925–3945, Apr. 2021, doi: 10.1109/TPEL.2020.3024862.

[7] W. Zhou, X. Zhong, and K. Sheng, "High temperature stability evaluation of SiC MOSFETs," in *Proc. 26th Int. Symp. Power Semicond. Devices*, Jun. 2014, pp. 305–308, doi: 10.1109/ISPSD.2014.6856037.

[8] X. Jiang et al., "Investigation on degradation of SiC MOSFET under surge current stress of body diode," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 77–89, Mar. 2020, doi: 10.1109/JESTPE.2019.2952214.

[9] F. Carastro, J. Mari, T. Zoels, B. Rowden, P. Losee, and L. Stevanovic, "Investigation on diode surge forward current ruggedness of Si and SiC power modules," in *Proc. 18th Eur. Conf. Power Electron. Appl.*, Sep. 2016, pp. 1–10, doi: 10.1109/EPE.2016.7695685.

[10] S. Yin, Y. Gu, S. Deng, X. Xin, and G. Dai, "Comparative investigation of surge current capabilities of si IGBT and SiC MOSFET for pulsed power application," *IEEE Trans. Plasma Sci.*, vol. 46, no. 8, pp. 2979–2984, Aug. 2018, doi: 10.1109/TPS.2018.2849778.

[11] X. Jiang et al., "Comparison study of surge current capability of body diode of SiC MOSFET and sic Schottky diode," in *Proc. IEEE Energy Conversion Congress Expo.*, Sep. 2018, pp. 845–849, doi: 10.1109/ECCE.2018.8558388.

[12] Z. Gao, Q. Guo, N. Ren, and K. Sheng, "Experimental investigation of the single pulse surge current ruggedness of the body diode of SiC power MOSFETs," in *Proc. 17th China Int. Forum Solid State Lighting Int. Forum Wide Bandgap Semiconductors China (SSLChina: IFWS)*, Nov. 2020, pp. 77–80, doi: 10.1109/SSLChinaIFWS51786.2020.9308775.

[13] W. Huang et al., "Investigation of surge current reliability of 1200 V planar and trench SiC MOSFET," in *Proc. IEEE 15th Int. Conf. Solid-State Integr. Circuit Technol. (ICSICT)*, Nov. 2020, pp. 1–3, doi: 10.1109/ICSICT49897.2020.9278173.

[14] Z. Zhu, H. Xu, L. Liu, N. Ren, and K. Sheng, "Investigation on surge current capability of 4H-SiC trench-gate MOSFETs in third quadrant under various VGS biases," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 5, pp. 6361–6369, Oct. 2021, doi: 10.1109/JESTPE.2020.3028094.

[15] M. Zhang et al., "Degradation analysis of double trench-gate SiC MOSFETs under single surge current stress," in *Proc. 25th Int. Conf. Electron. Packag. Technol.*, Aug. 2024, pp. 1–4, doi: 10.1109/ICEPT63120.2024.10668775.

[16] H. Wu et al., "Reliability analysis for commercial SiC MOSFETs in single pulse and repetitive surge current test," in *Proc. 11th Int. Conf. Prognostics Syst. Health Manage.*, Oct. 2020, pp. 481–485, doi: 10.1109/PHM-Jinan48558.2020.00093.

[17] Z. Wang et al., "Reliability investigation on sic trench MOSFET under repetitive surge current stress of body diode," in *Proc. IEEE Workshop Wide Bandgap Power Devices Appl. Asia*, Aug. 2020, pp. 1–4, doi: 10.1109/WIPDAASIA49671.2020.9360249.

[18] Z. Cheng, L. Sang, Y. He, X. Niu, Z. Li, and R. Jin, "Surge current behavior analysis of planar-gate SiC MOSFET under positive gate bias using tcad simulations," in *Proc. 21st China Int. Forum on Solid State Lighting, 10th Int. Forum Wide Bandgap Semiconductors*, Nov. 2024, pp. 130–133, doi: 10.1109/SSLCHINAIFWS64644.2024.10835287.

[19] M. Zhang, H. Li, Z. Yang, S. Zhao, and L. Ding, "Surge current conduction mechanisms of SiC MOSFETs under third-quadrant operation," in *Proc. IEEE Energy Convers. Congr. Expo.*, Oct. 2024, pp. 6749–6753, doi: 10.1109/ECCE55643.2024.10861518.

[20] M. Zhang, H. Li, Z. Yang, S. Zhao, X. Wang, and L. Ding, "Surge current distribution in paralleled SiC MOSFETs under third-quadrant operation," *IEEE Trans. Power Electron.*, vol. 40, no. 2, pp. 3077–3089, Feb. 2025, doi: 10.1109/TPEL.2024.3485730.

[21] J. Caoet al., "Surge current failure mechanism of 650V double-trench SiC MOSFETs," in *Proc. 16th Int. Conf. Solid-State Integr. Circuit Technol.*, Aug. 2022, pp. 1–3, doi: 10.1109/ICSICT55466.2022.9963338.

[22] X. Zhan et al., "Investigation on degradation of 1200-V planar and trench SiC MOSFET under surge current stress of body diode," *IEEE Trans. Electron Devices*, vol. 71, no. 1, pp. 709–714, Jan. 2024, doi: 10.1109/TED.2023.3335892.

[23] Y. Lin, Y. Q. Chen, K. Geng, and B. Hou, "Degradation mechanism and failure analysis of planar type SiC MOSFETs under cyclic stress of surge current," in *Proc. 13th Int. Conf. Rel., Maintainability, Saf.*, Aug. 2022, pp. 135–139, doi: 10.1109/ICRMS55680.2022.9944567.

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[24] B. Heinze, J. Lutz, M. Neumeister, R. Rupp, and M. Holz, "Surge current ruggedness of silicon carbide Schottky- and merged-pin-schottky diodes," in *Proc. 20th Int. Symp. Power Semicond. Devices IC's*, May 2008, pp. 245–248, doi: 10.1109/ISPSD.2008.4538944.

[25] D. Ma et al., "Degradation evaluation and defects analysis for 1.2-kV planar-gate SiC MOSFETs under repetitive surge current stress," *IEEE Trans. Electron Devices*, vol. 70, no. 12, pp. 6473–6479, Dec. 2023, doi: 10.1109/TED.2023.3323912.

[26] B. Zhang et al., "The surge current failure and thermal analysis of 4H-SiC Schottky barrier diode," *IEEE Trans. Electron Devices*, vol. 71, no. 6, pp. 3805–3810, Jun. 2024, doi: 10.1109/TED.2024.3385389.

[27] M. Bhatnagar and B. J. Baliga, "Comparison of 6H-SiC, 3C-SiC, and si for power devices," *IEEE Trans. Electron Devices*, vol. 40, no. 3, pp. 645–655, Mar. 1993, doi: 10.1109/16.199372.



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