MSc. Thesis

High Aspect Ratio Surface Micromachining using Carbon Nanotubes

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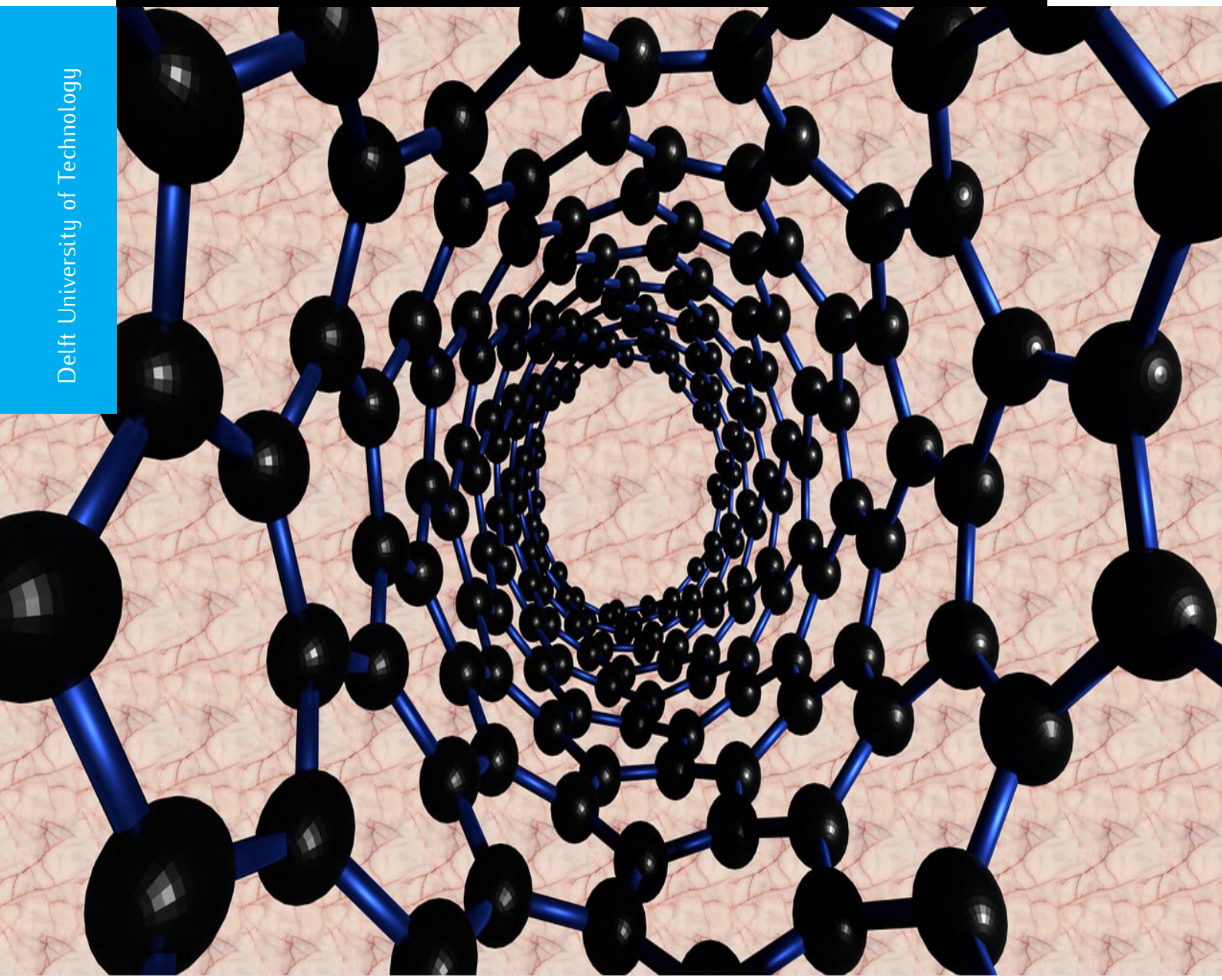

TU Delft Delft University of Technology

HIGH ASPECT RATIO SURFACE MICROMACHINING USING CARBON NANOTUBES

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ABSTRACT

Silicon-based MEMS technology has been the standard for developing 2D and 3D micro-structures for many years. There are 2 main classifications of MEMS manufacturing technologies, viz. bulk micro-machining, and surface micro-machining. These techniques have its own set of drawbacks. Bulk micro-machining affects the structural integrity of the wafer because bulk silicon is being etched. Surface micro-machining is limited by the maximum thickness of the method of thin-film deposition (usually a few microns). The current silicon-based MEMS sensors also can fail when it comes to harsh environment sensing. Due to this, the sensors would require many supporting infrastructures such as radiation shield, cooling system and shock-proof packaging.

One way to circumvent this problem is by designing sensors using materials that would not require as much supporting infrastructure. Silicon carbide (SiC) has proved to be a viable candidate to be used in such harsh environments. This is because it is found to be mechanically robust, chemically inert and with good wear resistance. However, bulk micro-machining with SiC is extremely challenging due to the high difficulty in etching. Many techniques have been tested to etch SiC, but they all have considerable drawbacks or low etch rates. Thus, to make high aspect ratio structures using SiC we will require a new technique. This is where carbon nanotubes (CNT) can be used as a framework in the fabrication process for high aspect ratio surface micro-machining. CNTs are structures made from rolled up cylinders of graphene. They can be grown to lengths of several micrometres to millimetres while their diameter is in the order of a few nanometres. Bundles of these tubes were found to have excellent conductance with maximum current densities of up to $10^9 A/cm^2$, and their behaviour can be either metallic or semiconducting depending on their chiral vector. Individual CNT are stiff, showing a Young's modulus of approximately 1 TPa.

These unique properties make CNTs a very interesting material to be integrated into conventional MEMS technology. Although a single nanotube has excellent properties, bundles of nanotubes show a 'foam-like' property since they are held together by weak van der Waals' forces. Thus, to realize mechanical structures with CNTs, we will have to coat the nanotube bundles with a filler material. This has previously been demonstrated to allow tuning of the mechanical properties of the composite. SiC would be an attractive filler candidate for harsh environment sensors. Due to the porous nature of nanotubes, it is possible to infiltrate the forest by deposition of a nanoscale coating. The deposition of the filler material is done by means of low pressure chemical vapor deposition (LPCVD) since a low pressure and deposition rate will enable the nanotube forest to get completely infiltrated and more uniformly coated. The goal of this research is to fabricate the first sensor using this technique, viz. a comb type capacitive accelerometer and test its performance and resilience to harsh environments by using SiC as coating. This technique will enable the user of a thicker layer for the proof mass and combs, resulting in a higher performance and potentially, resistance to harsh environments.

Keywords : Carbon nanotubes, Silicon carbide, nano-composite, micro-machining

ACKNOWLEDGEMENTS

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I have been interested in the integration of exotic materials in microelectronics since before I started my masters. This led me to approach Dr. Ir. Sten Vollebregt for my thesis project. Sten has been one the most inspiring and enthusiastic professors I've met. His energy and dedication has been extremely motivating which made this project a success. He was always approachable and even took time off his busy schedule to help me process my samples outside EKL. All my doubts were clarified during the weekly meetings and helped me plan out my work in the cleanroom more efficiently. I am eternally grateful to him for taking me under his wing and enlightening me about the joy in conducting research about a topic. I would also like to thank Jiarui Mo, my daily supervisor for helping me in the cleanroom related work and clarifying the doubts that I had at the time.

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Shreyas Shankar
October 2021

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ACRONYMS

MEMS Micro-Electro-Mechanical Systems . . . xiii
CNT Carbon nanotubes . . . xiii
SiC Silicon Carbide . . . xiii
IC Integrated circuit . . . 1
IMU Inertial measurement unit . . . 1
KOH potassium hydroxide . . . 3
SiO_2 Silicon-di-oxide . . . 2
Si_3N_4 Silicon Nitride . . . 2
Al_2O_3 Aluminum Oxide . . . x
TiN Titanium nitride . . . 38
VACNT Vertically aligned carbon nanotubes . . . 22
HF Hydrofluoric acid . . . 3
LPCVD Low pressure chemical vapour deposition . . . 4
PECVD plasma enhanced chemical vapour deposition . . . 19
SWCNT Single-walled carbon nanotubes . . . 5
MWCNT Multi-walled carbon nanotubes . . . 5
CTE Co-efficient of thermal expansion . . . xiii
RIE Reactive ion etching . . . 15
Al Aluminium . . . 16
O_2 Oxygen . . . 56
Ni Nickel . . . 16
Cu Copper . . . 16
Co Cobalt . . . 18
Fe Iron . . . 18
Pd Palladium . . . 19
CVD Chemical vapour deposition . . . 18
He Helium . . . 18
CMOS Complementary metal oxide semiconductor . . . 1
TEM transmission electron microscopy . . . 5
SOG silicon-on-glass . . . 27
DGM-SOG double glass modified silicon-on-glass . . . 27
TLM transmission line measurement . . . 40
ELM electrical line-width measurement . . . 40
VdP Van der Pauw . . . 40
NMP N-methyl pyrrolidone . . . 47
ALD atomic layer deposition . . . 51
SEM scanning electron microscope . . . 53
GFR gas flow ratio . . . 55
SiH_2Cl_2 dichlorosilane . . . 55

1 INTRODUCTION

Technology has been rapidly advancing ever since the invention of the first Integrated circuit (IC) in the 1950s. This was a huge milestone for the progress of humanity as it enabled miniaturization of circuits. Sensors and computing devices that once occupied a whole room were now less bulky and easy to move around. This reduction is size also made it possible to have more circuits and functionalities of the same chip. Thus, increasing the performance drastically. This trend of miniaturization also found its place in mechanical systems. Through silicon technology it was possible to create structures with moving parts which could interact and communicate with the surroundings. These structures were able to sense stimuli such as motion, light and chemicals and send this information to a readout circuit. Thus, came the MEMS technology.

MEMS is the technology that has enabled us to create a hybrid of multiple domains such as mechanical and electrical components on a micro scale. The concept was first theorized in the 1960s and has now come a long way. Previously, the measurement, control systems and the readout of sensors were all independent and required complex wiring. As the sensors became more and more complex it proved difficult to manage these independent connections to a control module. 'Smart-sensors' made it possible to combine the sensing element with the readout circuitry on a single chip through planar technology [16]. These smart sensors in addition to Complementary metal oxide semiconductor (CMOS) process make use of silicon technology as it is highly robust and low cost when mass produced. However, we are beginning to see a sort of saturation of the capabilities of silicon technology. It is no longer beneficial to just brute force the miniaturization of devices. Thus, came the need to develop new techniques and measurement schemes. One new technique has been the use of materials that can withstand harsh environments. Harsh environment refers conditions such as large temperature excursions, long operating times at high temperatures, intense radiation exposure and high shock and vibrations.

Harsh environment sensors find applications in many industries such as aerospace, oil dredging, medicine and so on. In the aerospace industry, the launch vehicles require extremely precise navigation and measurement systems. Rockets, space shuttles, rovers and satellites have a number of devices that are constantly monitoring the surroundings in real time with a high degree of accuracy and course-correcting if necessary. This course correction is performed using the Inertial measurement unit (IMU) installed within the vehicles. The IMU consists of gyroscopes, accelerometers and sense electronics which is used to accurately gather information of upto 6 degrees of freedom (Roll, Pitch and Yaw axes from the gyroscope and the X, Y, Z axes from the accelerometer). This information is fed to the position control thrusters which would then takes the necessary decisions to course-correct. Sensors employed in such systems are exposed to a variety of harsh conditions. The launch and landing impact of these vehicles is found to exceed 100,000 g [1]. Thus, high shock resistance is required. Radiation is another major problem for electronics in space. This is why the current IMUs are bulky with a sufficiently large power source and radiation shielding.

The current silicon-based MEMS technology, although has many advantages compared to bulky traditional sensors, it is not compatible for use in harsh environments. The supporting infrastructures such as radiation shield, cooling system and shock-proof packaging adds extra weight and size to the sensors thus negating its advantage of being small and less power consuming over traditional sensors. For most space missions involving smaller payloads, size and weight is a major factor to be considered as it dictates the overall cost of the mission; i.e bigger the size and more weight would require more fuel and thrusters during launch thus increasing the mission cost. One way to circumvent this problem is by designing sensors using materials that would not require as much supporting infrastructure as silicon-based sensors. SiC has proved to be a viable candidate to be used in such harsh environments. This is due to the fact that it is found to be mechanically robust, chemically inert and with good wear resistance. However, fabricating devices with SiC is extremely challenging due to the difficulties in etching. The current SiC based technology is mostly limited to thin films. Thus, in order to make high aspect ratio structures SiC, we will need to investigate new processes. This is where, CNTs can be used as a 3D scaffold to make high aspect ratio structures.

Before proceeding further, it is important to understand some basic concepts that will be used extensively in this work. These are presented in section 1.1. This is followed by the formulation of the research question in section 1.2 and the research goals in section 1.3.

1.1 BACKGROUND

There are certain concepts to be familiar with before proceeding further in this work. We will first have a brief look at the different MEMS manufacturing technologies (1.1.1). This is followed by an overview of Silicon Carbide (1.1.2) and Carbon nanotubes (1.1.3).

1.1.1 MEMS manufacturing technologies

Silicon-based MEMS technology has been the standard for developing 2D and 3D micro-structures for a number of years. This is due to the technique of *micromachining* which allows us to create such structures on a micro-meter scale. There are 2 main classifications of MEMS manufacturing technologies, viz. bulk micromachining and surface micro-machining.

Bulk micro-machining

This technique involves selective removal of sections of the silicon substrate. This is done by defining etch windows using a masking layer followed by removal of these layers at lateral positions by using a specific etchant[1]. The steps of bulk micromachining is shown below in Figure 1.1. Typically, the substrate is first coated with a thin layer which is resistant to the etchant used for substrate etch later on. This thin flim layer is usually either Silicon-di-oxide (SiO_2) or Silicon Nitride (Si_3N_4). The thin film layer is then coated with a photoresist that can withstand the etchant used later. Photo-lithography is used to define patterns on the photoresist which is then baked and developed. The structure is then exposed to the etchant which removes the underlying layer at specific resist defined areas. Finally, the resist is removed and the wafer now has patterned thin film at areas we want to etch the

1 A chemical, vapor or plasma that selectively removes sections of the substrate without affecting the mask layer.

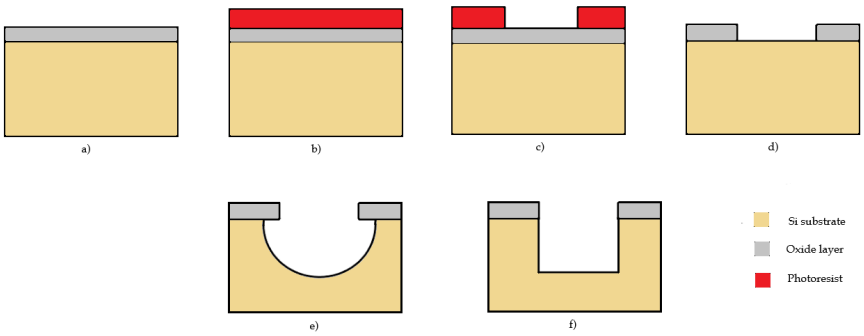


Figure 1.1: Bulk micro-machining process. a) Si substrate with oxide layer. b) Photresist layer added. c) Photo-lithography to pattern the photoresist. d) Oxide layer etched and photoresist stripped. e) Isotropic etching silicon substrate. f) Anisotropic etching silicon substrate.

substrate. The sustrate etching can be either isotropic[2] or anisotropic[3] depending on the etchant used. The most commonly used etchant for bulk micro-machining silicon is potassium hydroxide (KOH) solution which helps create structures like membranes and suspended masses. Over the years many modifications have been made to improve the bulk micro-machining technique such as using a combination of isotropic and anisotropic plasma etching to create vertical walled structures[16]. But, this technique had problems of integration with electronics. It is clear that although bulk micro-machining is the most widely used technique of MEMS manufacturing, it has a couple of drawbacks. The major drawback being the fact that bulk silicon is being removed which would affect the structural integrity of the wafer and make it less resistant to mechanical shock. The devices are also quite bulky due to the limited aspect ratios that are possible through this technique.

Surface micro-machining

In order to overcome the drawbacks of bulk micro-machining as mentioned in the previous section, surface micro-machining was developed. Here, instead of etching bulk silicon, structures are formed by deposition, patterning and removal of selective layers of the substrate. Doing so, we preserve the structural integrity of the substrate. Typically, we make use of two masking layers and one type of etchant that is selective to only one of these layers. The layer we want our structure to be made with is called the *structural layer* and the layer that is used to pattern and remove with the etchant is called the *sacrificial layer*. The most widely used sacrificial layer is SiO_2 with poly-silicon (or certain metals) as the structural layer and Hydrogen flouride (HF) as the etchant. Figure 1.2 shows the steps in surface micro-machining process. The substrate is usually coated with a very thin film of nitride for protection against the etchant. In order to have electrical contact between the structure and the substrate, contact holes are made on the nitride layer. It is clear from the figure that the maximum width of the structural layer is limited the rate at which the etchant can under-etch the sacrificial layer. This can be resolved by having numerous perforations on the structure to give the etchant more access to the sacrificial layer.

2 Even removal of substrate in all directions.
3 Removal of substrate in one particular direction.

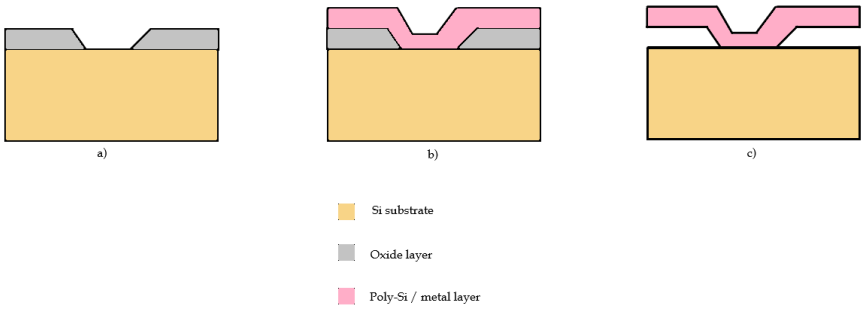


Figure 1.2: Surface micro-machining process. a) Silicon substrate with a patterned oxide layer. b) Deposition of the structural layer. c) Release of the structure by etching the oxide layer.

It is clear the that structures made through surface micro-machining have several advantages such as, maintaining the wafer strength and being more CMOS compatible. There is more space for on-chip electronics due to the small size of surface micro-machined chips. However, one major disadvantage of surface micro-machining is the fact that the thickness of the structure is limited by the maximum thickness of the method of deposition. For Low pressure chemical vapour deposition (LPCVD) of Poly-silicon this is usually around $0.5 - 3\mu m$ [17]. This greatly limits the structures such as accelerometers which require a thick seismic mass to have good performance.

1.1.2 Silicon Carbide

Silicon Carbide (SiC) which is a semiconductor material that contains silicon and carbon, is a material with some very interesting properties. It has been studied for more than 25 years as a material for micro-electronic devices. This is due to its outstanding chemical and mechanical properties. SiC occurs in over 200 poly-types. However, when it comes to device fabrication only 2 types are of concern to us. They are -

- *$\alpha - SiC$ (4H-SiC & 6H-SiC)*
  The primitive cell here is hexagonal. Commercially they are available in wafer form. However, fabricating structures on these wafers is a huge challenge due to the extreme difficulty in etching bulk SiC [6]. More details on this will follow in the upcoming chapter.
- *$\beta - SiC$ (3C-SiC)*
  This type has a cubic structure similar to diamond. This is the only polytype that can be grown in a single crystal form on substrates other than SiC. Thus, it can be deposited on a silicon wafer to form MEMS structures. It is also chemically inert to most wet etchants thus making it an ideal candidate to be used as an etch stop in bulk micro-machining[18].

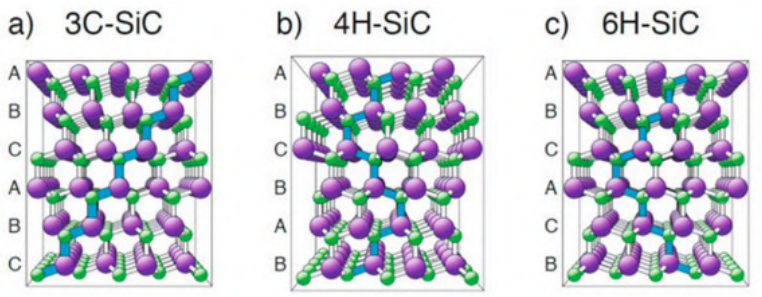


Figure 1.3: Crystal structure of SiC poly-types [1]. a) 3C-SiC b) 4H-SiC c) 6H-SiC

Figure 1.3 shows the different crystal structures of SiC. It was found that the properties such as wide band gap energy, high thermal conductivity and good mechanical strength comparable to diamond, this is discussed further in section 2.2.1. The technology of electronics made by diamond is extremely expensive and still in its early research stages. Thus, SiC makes for an excellent candidate to be used in harsh environment devices.

1.1.3 Carbon nanotubes

Carbon is the most abundant element in the universe. It is a fascinating element due to its ability to form long chains of covalent bonds. The various degrees of hybridization of carbon atoms allows carbon to have many allotropes[4]. Graphite which is one of the allotropes, was the main focus of study for carbon-based electronics in the 1950s. In 1962, monolayer graphene was discovered by H.P. Boehm. This structure was a network of sp^2 hybridized hexagonal carbon atoms. However, no development was made until the 1970s where research was made to separate and modify individual graphene layers. A few years later, fullerenes were discovered by Kroto et al. Fullerene is formed by clusters of large numbers carbon atoms forming highly symmetric molecules. C_{60} atom cluster was found to be preferred due to the fact that in this icosahedral structure, all carbon atoms could be sp^2 hybridized without any dangling bonds. This discovery led to the idea that an elongated fullerene or a rolled up graphene cylinder could be formed which came to be called Single-walled carbon nanotubes (SWCNT). In 1991, S. Iijima published the idea of having multiple cylinders of graphene in a nested structure and called it Multi-walled carbon nanotubes (MWCNT). He later observed and analyzed these structures using transmission electron microscopy (TEM). These tubes had an interlayer spacing of 3.4$\mathring{A}$ which was a little higher than that of graphite. This difference was thought to be due to the van der Waals interactions between the nested tubes [19].

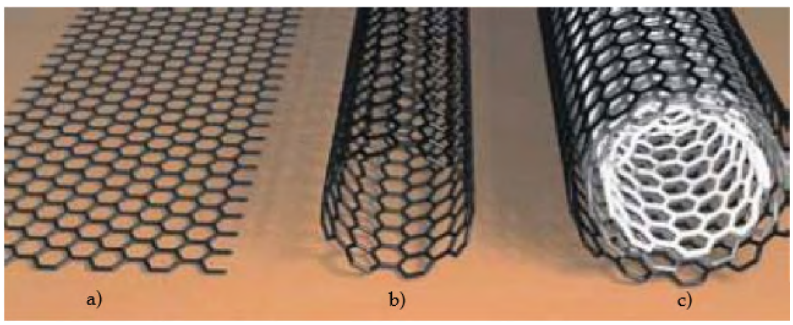


Figure 1.4: a) Graphene mono-layer b) SWCNT c) MWCNT [2]

4 A property of the same element to occur in two or more different forms but the same physical state.

CNT can be grown to lengths of several micrometers while their diameter being in the order of a few nanometers. Bundles of these fibres were found to have very high conductance with high current densities of upto $10^9 A/cm^2$. They are highly stiff, showing a Young's modulus of approx 1 TPa and their behaviour can be either metallic or semiconducting depending on their chiral vector [20]. These unique properties make CNTs a very interesting material to be integrated into conventional MEMS technology. [21]

Although the properties of a single nanotube may seem quite enticing, when bundled up the properties vary significantly. This is due to the fact that the nanotube bundles are held together by weak van der Waals' forces. This makes nanotube bundles to have a 'foam-like' property. Thus, mild stress is enough to break these bonds and destroy any realizable structure. Therefore, it is safe to conclude that in order to realize mechanical structures with CNTs, we will have to coat the nanotube bundles with a filler material [7].

1.2 RESEARCH QUESTION

Now that we understand the fundamentals of what is used in this work, we can now formulate a research question. We know that in order to realize mechanical structures with CNTs a coating material is required. Since, SiC is an excellent material for harsh environment sensors, it would make it an ideal candidate for a filler material in these structures. Thus, I have formulated my research question as follows -

"Is it possible to use a Carbon nanotube - Silicon Carbide composite to create high aspect ratio structures on top of a wafer through surface micro-machining?"

If this is possible, the technique may be used to create sensors and not just actuators as done previously [9]. Thus, the follow up questions would be -

"Is it possible to create harsh environment sensors using the CNT - SiC nanocomposite?"
"What are the electro-mechanical properties of the nanocomposite?"
"What is the maximum operating temperature of this sensor?"

1.3 RESEARCH GOALS

In order to investigate the research question, this work will mainly focus on creating a *CNT/SiC nano-composite MEMS capacitive accelerometer with a comb drive*. Since, the previous work has only focused on creating actuators made with the nanocomposite, it will be interesting to see if it is possible to make sensors such as capacitive accelerometers. An accelerometer made using this technique could show higher sensitivity from the increase in aspect ratio and potentially, resistance to harsh environments. The main objectives of the thesis would be as follows -

- Investigate the process of deposition of silicon carbide on carbon nanotubes and study the properties of the nano-composite.
- Design a simple capacitive accelerometer with a comb drive to be able to fabricate with the above technique.
- Fabricate the accelerometer using the CNT - SiC nano-composite technique.
- Study the electro-mechanical properties of the designed sensor.
- Test the resilience of the sensor in harsh environment conditions.

1.4 THESIS OUTLINE

The thesis *High aspect ratio surface micromachining using carbon nanotubes* is divided into 6 chapters. Following the introduction in Chapter 1, the subsequent chapters are as follows -

Chapter 2 consists of previous literature that has been investigated on the topic. Understanding the theory behind the topic will help make a flowchart for fabrication in the design process.

Chapter 3 deals with the modelling and simulation of the device. This helps us define the constraints. The theoretical results can be obtained for the design using the *COMSOL Multiphysics* simulator.

Chapter 4 involves the mask design and the fabrication of the device. The mask design helps define the flowchart used during cleanroom fabrication.

Chapter 5 consists of device performance analysis and electrical measurements.

Chapter 6 gives an overview of the thesis and the research goals that were achieved. This is followed by recommended future work.

2 LITERATURE REVIEW

In this chapter we will have a deeper look into the previous literature that has been published on our topic. This will help us better understand the process and motivate the design. We shall first have a look at the current MEMS accelerometers made using standard silicon technology and their limitations in Section 2.1. This is followed by understanding the properties and limitations of silicon carbide in Section 2.2. Carbon nanotubes (CNT) as discussed previously have very useful properties that could help solve the shortcomings of using SiC. This is discussed in detail in Section 2.3 and Section 2.4.

2.1 STANDARD SILICON MEMS ACCELEROMETERS

The measurement of acceleration is pivotal in any system that is in motion. Acceleration is just simply the rate of change of velocity of an object. Since this work will focus on harsh environment sensors, we shall consider inertial measurement units (IMUs) used in spacecrafts. An IMU usually is made up of an accelerometer and a gyroscope with some support electronics. There are various types of accelerometers such as capacitive, piezo-resistive and piezo-electric. However, capacitive accelerometers are more widely used due to its low power consumption and high sensitivity. In this section we will first understand the working principle of a simple accelerometer in section 2.1.1. This is followed by the a review of the standard fabrication process used in section 2.1.2. The limitations of accelerometers are then discussed in section 2.1.3.

2.1.1 Working principle

A simple comb type capacitive accelerometer is shown below in Figure 2.1. The main parts of an accelerometer are the proof mass, the fixed fingers, movable fingers, folded spring and an anchor.

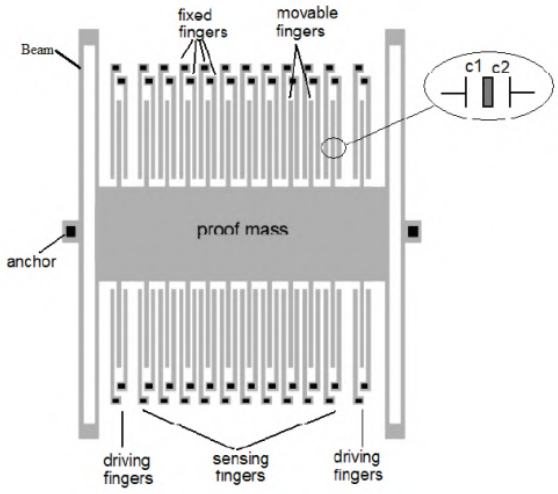


Figure 2.1: A MEMS comb type capacitive accelerometer [3]

The working principle of a capacitive accelerometer is simple - *When subjected to an acceleration, a displacement in the proof mass causes a change in capacitance between the fixed and movable fingers. Sensing this capacitance change can help calculate the acceleration.* [3]

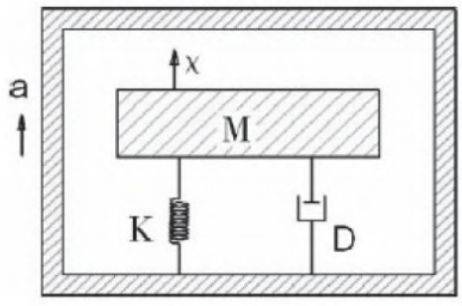


Figure 2.2: Mathematical model of the acceleromter [3]

The mathematical modelling of the comb acceleromter can be made using the mass, spring and damper model as shown in Figure 2.2.

- Using the mass, spring and damper model we can write the inertial force (F) on the proof mass (M) with acceleration (a) as $F = -M * a$. But this force can be equated to the damping force according to Hooke's law as $F_{damp} = K_{spring} * x$, where - K_{spring} is the spring constant of the folded beam. Thus, equating the two force equations we get ,

$$x = \frac{-M * a}{K_{spring}} \tag{2.1}$$

- This equation 2.1, can help us calculate the mechanical sensitivity (S_{mech}) as shown below. Here, g is the acceleration due to gravity and M is the effective mass, ie density times the volume ($M = \rho$V)

$$S_{mech} = \frac{-M * g}{K_{spring}} \tag{2.2}$$

- The effective spring constant for the folded spring structure can be calculated using Figure 2.3. This has been taken from the book *Microsystems design* by Stephen D. Senturia [4] where a more detailed derivation of the formula can be found. Here, E is the Young's modulus of the material used, w is the beam width, h is the height of the beam and L_1, L_2 are the length of the folds of the spring on the top and bottom. typically we can just assume $L_1 = L_2$. Since there are two springs on either side, the effective spring constant would be doubled.

$$K_{spring} = (\frac{\pi^4}{6})\frac{E * h * w^3}{(2L_1)^3 + (2L_2)^3} \tag{2.3}$$

$$K_{eff1} = 2 * K_{spring} \tag{2.4}$$

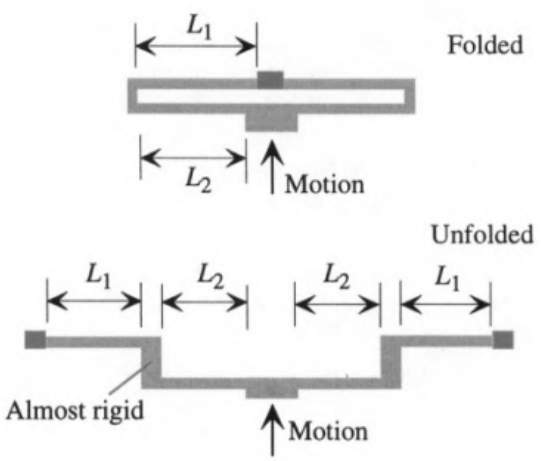


Figure 2.3: Folded spring and its equivalent structure [4]

- Now, from figure 2.1 we can see that when there is no acceleration applied, $C_1 = C_2$. Where C1 and C2 are the left and right comb capacitance respectively. The capacitance in this condition can be calculated as shown below, d is the distance between the adjacent fingers, N_f is the total number of fingers, L_f is the length of the fingers and h is the device thickness.

$$C_0 = \frac{\epsilon * A}{d} = \frac{\epsilon * N_f * L_f * h}{d} \tag{2.5}$$

- When subjected to an acceleration, $C1 \neq C2$. If x is the displacement caused, we can write the capacitances as -

$$C_1 = \frac{\epsilon * N_f * L_f * h}{(d + x)} = \frac{\epsilon * N_f * L_f * h}{d(1 + \frac{x}{d})} \approx C_0(1 - \frac{x}{d}) \tag{2.6}$$

$$C_2 = \frac{\epsilon * N_f * L_f * h}{(d - x)} = \frac{\epsilon * N_f * L_f * h}{d(1 - \frac{x}{d})} \approx C_0(1 + \frac{x}{d}) \tag{2.7}$$

The differential capacitance (dC) will then be,

$$dC = C_1 \sim C_2 = 2 * C_0(\frac{x}{d}) = \frac{2 * \epsilon * N_f * L_f * h * x}{d} \tag{2.8}$$

- The electrical sensitivity (S_{elec}) due to lateral movement can then be calculated as shown below, where - h is the height of the fingers, d is the distance between the fixed electrode and the finger, N_f is the total number of fingers and ϵ is the permittivity of air.

$$S_{elec} = \frac{2 * \epsilon * N_f * h}{d} \tag{2.9}$$

- Using equations 2.2 and 2.9 we can write the total sensitivity of the device as shown below [22],

$$S_{tot} = S_{mech} * S_{elec} \tag{2.10}$$

- The range of the accelerometer can also be determined as follows,

$$Range = \frac{Distance\ between\ fingers}{Mechanical\ sensitivity} = \frac{d}{S_{mech}} \tag{2.11}$$

- Typically, the rest capacitance (C_0) is in the order of pico-farads, while the differential capacitance (dC) is a few femto farads (fF). Thus, in order to detect such a small change in capacitance, a proper signal detection circuit is required. This can be achieved in a variety of ways by using chopper stabilized amplifiers and correlated double sampling circuits [4].
- Understanding the relationship between the dimensions and the sensitivity of the acceleromter is crucial since this is useful while designing the accelerometer to meet the specifications of the user.

2.1.2 Fabrication process

Capacitive accelerometers as stated earlier are low cost, low power and quite robust sensors. Bulk micromachining of capacitive accelerometers have been developed over the years with new innovative techniques such as dissovled wafer process (DWP), modified silicon-on-glass (M-SOG) and double glass modified silicon-on-glass (DGM-SOG) [23].

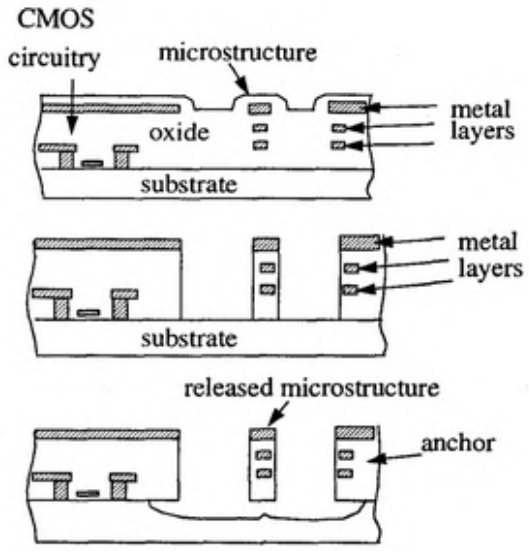


Figure 2.4: CMOS-MEMS process flow [5]

Surface micromachining techniques for capacitive accelerometers however, are much more beneficial due to the fact that it is possible to have the sensor and the readout on the same chip using CMOS-MEMS process flow as shown in Figure 2.4. It was found that it was possible to integrate the micro-structures as close as 12μm [5]. This can save a lot of chip area and thus help lower the production cost.

2.1.3 Limitations

The main drawback of surface micromachining capacitive accelerometers is the large internal stress developed due to the successive layers of the micro-structures. This would cause the structures to buckle. Another disadvantage is the limited thickness of the structures due to the limitation of the deposition method used. Thick structures are required to achieve a high dynamic range and sensitivity of operation [23].

One work investigated the radiation response of a standard capacitive accelerometer [24]. It was found that irradiating the sensor led to dielectric charging in the oxide layer which shifted the output voltage. Therefore, a standard capacitive ac-

celerometer cannot survive harsh environments and requires bulky supporting infrastructures for protection.

2.2 TREND TOWARD SILICON CARBIDE

The standard silicon technology being used in current day electronics have numerous advantages. However, it falls short when it comes to working in harsh environments. Harsh environments can be defined as conditions such as high temperature, high pressure, radiation, vibrations and harsh chemicals. Therefore, for electronics to be able to work in such conditions it is necessary to find new and ingenious ways to deal with the harsh environment. The approaches can be as follows [25]-

- The *packaging* used could be made with multiple layers for absorption. Special zones could be made that absorb thermal and mechanical loading.
- The *system* could be made with electronics that are isolated from areas that experience high temperatures. The operating modes of the system could be tuned to lower the self heating of the device.
- The *technology* used during fabrication could be changed by adding additives that increase the resilience of the structure to harsh environments.
- The *material* used could be one that has an inherent resistance to harsh environments. These materials or alloys are generally chemically inert, with a wide band gap and high density to absorb radiation.

This is where silicon carbide seems to be a very good option due to its excellent properties that make it resilient to harsh environments. Let us now review these properties and see how they compare to standard silicon.

2.2.1 Properties of Silicon carbide

We have already discussed the main polytypes of SiC in Section 1.1.2. We shall now review the electrical, mechanical and chemical properties of SiC. Silicon carbide is found to be high temperature resistant material. The sublimation point of SiC is found to be around 2830°C [1]. It is also resistant to corrosion due to its high chemical stability. We can see the comparison between SiC and standard silicon below in Table 2.1.

Table 2.1: Properties of Si and SiC. [1][26]

Property	Si	SiC
Density (kg/m^3)	2330	3210
Band gap (eV)	1.14	3.23
Thermal conductivity (W/(m.K))	140-150	330-490
Fracture strength (GPa)	7	21
Young's modulus (GPa)	160	390-690
Threshold energy (eV)	9	153
Stiffness-weight ratio E/σ (GN/kg.m)	72	130
Intrinsic carrier concentration (cm^{-3})	10^{10}	10^{-7}

Electrical properties

For a material to be viable for use in semiconductor electronics, the thermal stability of electrical parameters is of utmost importance. The intrinsic properties of the material plays a crucial role in temperature stability. The general principle is that increase in temperature of a semiconducting material leads to increase in carrier concentration and decrease in energy band gap which leads to a decrease in device performance. Therefore, having a material with high band gap and low intrinsic carrier concentration makes it suitable for use in high temperature applications.

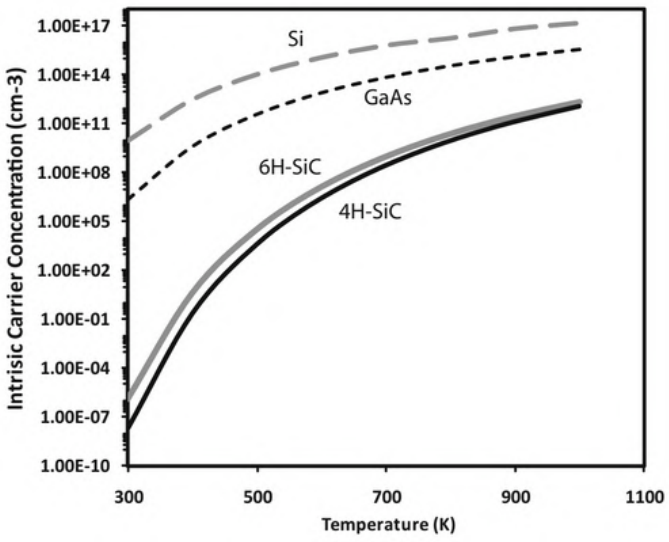


Figure 2.5: Intrinsic carrier concentrations as a function of temperature [1]

We can see from Table 2.1 that the energy band gap of SiC is much higher than standard silicon and from Figure 2.5 that the intrinsic carrier concentration is several orders of magnitude lower. This makes SiC a very good material for high temperature application. Radiation is another factor that can affect the electrical properties of a semiconducting material. Exposure to radiation causes a change in the carrier density of the conduction band which leads to a change in the material's conductivity. Prolonged exposure can lead to the material turning into an insulator. This process is known as 'carrier removal rate' and is dependent on the threshold energy of the material. It can be seen again from Table 2.1 that the radiation hardness of SiC extremely high compared to silicon due to its higher threshold energy.

Thermo-mechanical properties

The mechanical properties of a material plays a vital role in designing a MEMS device. The material needs to be able to withstand high mechanical shock and vibrations. Young's modulus is the parameter that defines the elastic property of the material. Mathematically, it is the ratio of uni-axial stress over the strain on the material. Any change in this parameter caused by change in temperature greatly affects the performance of the MEMS device. High temperature applications require the point of plastic deformation to be high with a high Young's modulus. It was found that plastic deformation occurred in silicon at a temperature of around 500°C which makes it unsuitable in harsh environments. Plastic deformation for SiC on the other hand starts above 1200°C [1].

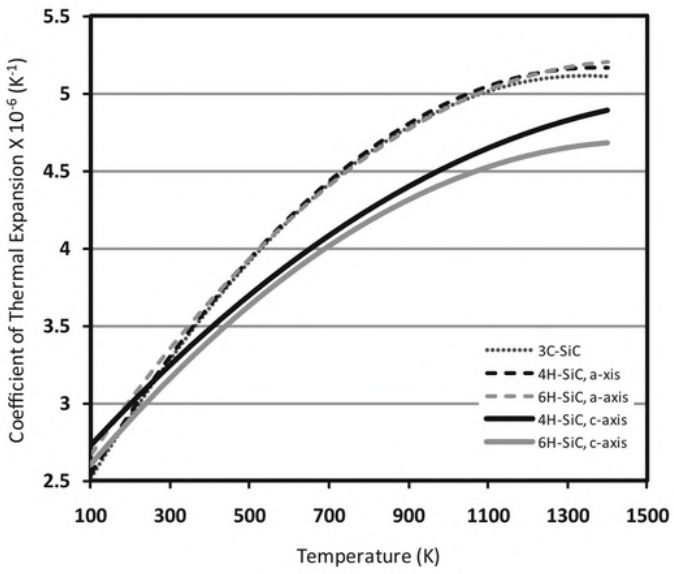


Figure 2.6: CTE of polytypes of SiC [1]

The CTE of polytypes of SiC in a/c-axis with respect to temperature is shown above in Figure 2.6. It can be seen that there is almost a 50% increase in CTE between room temperature and 600°C. Also, the CTE at room temperature for SiC is similar to that of silicon. This is an important factor to consider as it would alter the geometries of the device structure which leads to a change in response characteristics of the structure. Another parameter to consider for aerospace applications is the stiffness-weight ratio (E/σ). Having a high E/σ would reduce the probability of the material to undergo failure due to stiction or fracture. It can be seen from Table 2.1 that the E/σ and the fracture strength values of SiC is high compared to silicon which makes it a better candidate for harsh environments. In addition to this the thermal conductivity of silicon, SiC, and diamond has been investigated and compared in previous work [27].

2.2.2 Limitations of Silicon carbide

We have seen that SiC has favourable material properties for fabrication of harsh environment devices. Since the $\alpha - SiC$ is one that is commercially available in wafer form it would seem the best polytype to create MEMS structures. However, the problem with using $\alpha - SiC$ is the extreme difficulty in etching due to its chemical inertness. Thus, bulk micro-machining on SiC is quite difficult since the etch rate with standard etchants is very low. The current bulk micro-machining techniques for SiC is as follows [6] -

- Reactive ion etching (RIE)
- Molten KOH etching
- Photoelectro-chemical etching (PEC)
- Laser ablation

Reactive ion etching (RIE)

Reactive ion etching (RIE) is a plasma etching technique which makes use of a high frequency switched electrode on an appropriate gas mixture to etch away the target. The selection of masking material here is of utmost importance since it decides the selectivity and etch rate. The mask should only react to the physical bombardment

of the gas and not react chemically with it. Metal masks have shown to have the highest etch rates for SiC due to the fact that SF_6 and O_2 based chemistries can be used. The mechanism here is that the oxygen first reacts with the carbon atoms to form a volatile carbon monoxide gas. The oxygen then converts the unsaturated flouride into reactive flouride atoms.The etch rates obtained for 4H-SiC was approximately $0.27\mu m/min - 0.75\mu m/min$ [6] and the etch was highly anisotropic.

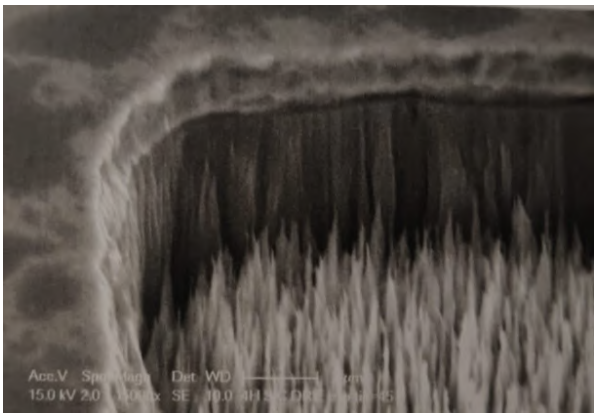


Figure 2.7: SEM image of etched SiC to show the effect of micro-masking [6]

Aluminium (Al), Nickel (Ni) and Copper (Cu) metal masks have shown the highest selectivity but are also very contaminating. However, a major disadvantage of using metal masks is the phenomenon called *micro-masking* where the metal can sputter back into the etch openings. The etched surface also shows a high degree of roughness as shown in Figure 2.7. Thus, RIE is not a viable option for etching SiC as it is quite challenging to etch structures of several microns.

Molten KOH etching

KOH solution is the most commonly used etchant in bulk micro-machining. However, for SiC due to its chemical inertness, a molten KOH solution in the temperature range of 400°C - 600°C is required. An isotropic etch is obtained through this technique. The etch rate obtained was also quite low and thus not feasible due to the high temperature requirement [6].

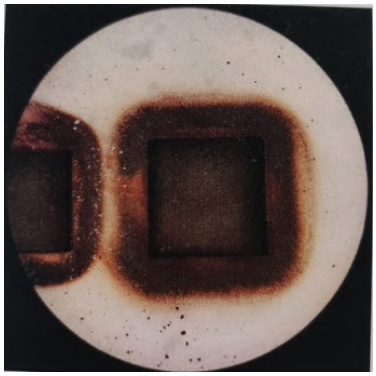
Photoelectro-chemical etching (PEC)

This technique makes use of KOH solution in combination with UV light with an electrical bias applied between the solution and the substrate. Doping concentration greatly affects the etch in this method. However, the etched surface was found to be quite rough with poor uniformity which is the main disadvantage of this technique. This technique also requires a dedicated setup [6].

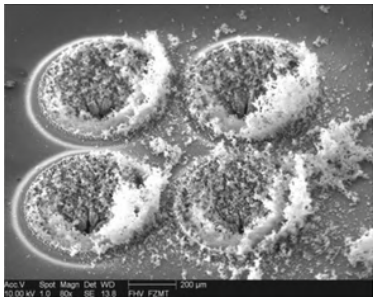
Laser ablation

This technique is an innovative way to etch 4H-SiC wafers using a femto-second laser. The device uses a high power laser to cut and micro-machine organic and ceramic materials through photo-thermal and photo-chemical reactions. One main advantage of this technique is that there is no need for reticle design since no lithography is needed. Thus, the process is quick and flexible.

(a) The femto-second laser setup with a 4H-SiC wafer on the chuck [6]



(b) Thermal loading damage on the edges of the etch window [6]



(c) Excess material around the etch holes due to lack of cleaning [28]

Figure 2.8: The laser ablation process

In the previous work as shown in Figure 2.8a, a Talon 355-15 femtosecond laser was used to etch a 360 μm thick, 400 μm square window using a 355 nm light source for 7 $mins$ [6]. It could be seen that there was extreme thermal loading on the edges of the etch opening due to the high energy laser used. This thermal damage as shown in Figure 2.8b affects the structural integrity of the wafer. Another disadvantage is the difficulty in removing the excess material from the etch window after the ablation process as shown in Figure 2.8c. This method is also not viable for batch production.

Although there have been bulk micro-machined structures made with SiC previously [29] [30], it is clear that bulk micro-machining of $\alpha - SiC$ is extremely difficult and not quite viable for creating high aspect ratio structures. Thus, surface micro-machining seems to be the safe option, but as discussed earlier the thickness of such structures are limited by the maximum thickness of the deposition method used. For deposition we use $\beta - SiC$ since it is the only polytype that can be grown in a single crystal form on substrates other than SiC. There have been many works on the deposition technique of SiC on a wafer [31], it is mainly with thin films. Thus, in order to make high aspect ratio structures of significant height we will need a

new technique. This is where carbon nanotubes can be used as a framework in the fabrication process for high aspect ratio surface micro-machining.

2.3 CARBON NANOTUBES IN MEMS

The history of CNT has been presented in Section 1.1.3. They have very interesting properties that can be integrated into MEMS fabrication process. We shall have a deeper look into these properties in this section. The process of CNT growth is first investigated in section 2.3.1. This is followed by the electrical and mechanical properties of CNTs in section 2.3.2 and section 2.3.3 respectively.

2.3.1 Growth of CNT

Carbon nanotubes have been researched to become viable material for large scale production for quite a number of years now. The problem faced here is the cost and reproducibility aspect of it. It is still very difficult to grow CNTs of the same electrical properties and chirality. Currently, the three main growth techniques for carbon nanotubes are [2] -

- Arc discharge
- Laser ablation
- Chemical vapour deposition (CVD)

Arc discharge

This was the method of growing nanotubes when they were first discovered in 1991. Two arc ignited carbon electrodes are placed in a Helium (He) chamber. The evaporated carbon formed by arc discharge can then condensate into MWCNT. For producing SWCNT a metal catalyst such as nickel and cobalt are used. Although this technique produced a reasonably good quality of SWCNT, the cost of production was quite high due to the high energy requirements of the machinery used.

Laser ablation

This method was invented for the production of SWCNT in the year 1996. A high power laser is used to evaporate a carbon/catalyst mixture placed in a furnace at 1200°C. The gases in the furnace help condense the evaporated carbon onto a cold surface to form nanotubes. Similar to arc discharge, this technique requires high power. Thus, increasing the cost of production and not compatible for growth on substrates. This led to the development of chemical vapour deposition methods for the growth of nanotubes.

Chemical vapour deposition (CVD)

CVD technique has been used in standard silicon technology for deposition of thin films on a substrate for many years now. The same technique can be applied to growth of nanotubes as well. A catalyst is always required when growing nanotubes by CVD methods. The requirements for the growth of nanotubes are -

- *Metal catalyst*
  This is usually transition metals such as Iron (Fe), Cobalt (Co), Nickel (Ni). The catalyst needs to be a nano-particle layer that is usually evaporated on a surface.

- *Carbon feedstock*
  The carbon feedstock is usually supplied by some form of hydrocarbon gas. The type of gas used affects the growth rate, the most popular ones being Methane (CH_4) and Acetylene (C_2H_2). Since acetylene is quite unstable, it has shown the good results due to the fact that it can decompose at lower temperatures.

- *Nucleation energy*
  The energy required for the growth to occur is usually supplied by either thermal energy or plasma - plasma enhanced chemical vapour deposition (PECVD). For PECVD it was observed that the temperature required for nanofibres[1] to grow is quite low (120°C) [2].

Many innovative methods have been invented to obtain better quality of CNTs such as ion irradiation in order to adjust the defects in structure [32], growing CNTs on carbon based substrates [33], growing nanotubes on a quartz substrate followed by transfer onto plastic in order to obtain flexible electronics [34]. It was shown that in order to obtain high density of nanotubes, a *lift-off* process can be used to replace traditional etching and cleaning to prevent catalyst damage [35]. It was also shown that using Palladium (Pd) as a catalyst gives high density of nanotubes but of lower quality [36]. These high density CNTs can be used as vertical interconnects in ICs. It is clear that the growth techniques for CNTs show promise for integration into standard technology. This is due to the amazing properties of nanotubes such as high surface area to volume ratio, high tensile strength, high porosity and nanometer scale sizes. We shall investigate these properties further in the coming sections.

2.3.2 Electrical properties of CNT

Carbon nanotubes CNTs exhibit a very interesting phenomena where the electrical properties of the nanotubes depend on the diameter and *chirality*[2]. Figure 2.9 shows how the chiral vectors of the nanotubes are named. The chirality is defined by a pair of chiral indices (n, m) which form the chiral vector defined by -

$$\overrightarrow{C_h} = n\overrightarrow{a_1} + m\overrightarrow{a_2} \tag{2.12}$$

Where, $\overrightarrow{a_1}$ and $\overrightarrow{a_2}$ are unit vectors on the crystal lattice. The diameter of the nanotubes can then be calculated by using the chiral indices by the relation where a = 2.46$\mathring{A}$ which is the lattice constant [37]-

$$d = |\overrightarrow{C_h}|/\pi = a\sqrt{n^2 + nm + m^2}/\pi \tag{2.13}$$

1 Tube-like carbon structures without graphite walls parallel to the tube axis.
2 The orientation in which the graphene plane is folded to create the nanotubes.

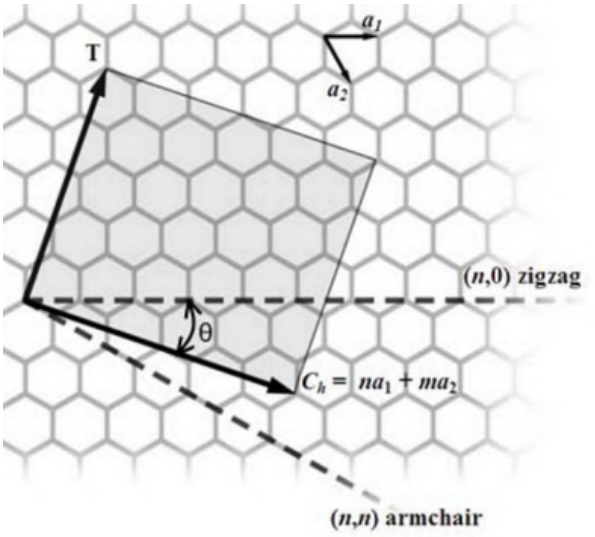


Figure 2.9: Chiral vectors of CNTs [2]

The importance of this calculation is that it was observed that CNTs show both metallic and semiconducting properties based on the diameter and chirality of the nanotubes. It was see that all *armchair*[3] structures show metallic properties, if $n - m$ is a multiple of 3 it shows semi-metallic properties and almost all other orientations show semiconducting properties. Thus, for a batch of SWCNTs approximately 1/3rd of the nanotubes would be metallic. For MWCNT however it is more difficult to predict the behaviour due to the interactions between the adjacent walls [37], but are generally considered to exhibit metallic behaviour.

Electromigration is one disadvantage of using traditional metals in high current density environments which would lead to failures. This occurs at current densities of around $10^6 - 10^7 A/cm^2$. CNTs however have shown no failure modes at current densities of even $10^9 - 10^{10} A/cm^2$, which is far superior than using traditional metals [38]. Thus, the properties of CNTs can be summarized in the Table 2.2.

Table 2.2: Properties of CNTs [2]

Property	Value
Current density (A/cm^2)	$10^9 - 10^{10}$
Specific heat (J/g.K)	0.7
Resistance (kΩ)	6.45
Thermal stability (°C)	> 2000
Thermal conductivity SWCNT (W/m.K)	2000 - 6000
Thermal conductivity MWCNT (W/m.K)	60 - 1000
Oxidizing point SWCNT (°C)	550 - 750
Oxidizing point MWCNT (°C)	800

2.3.3 Mechanical properties of CNT

When investigating the mechanical properties of CNTs it was found that a single nanotube is one of the strongest material, with tensile strength in the order of 100's of GPa. The Young's modulus is orders of magnitude higher than steel (in the order of TPa) and it also has a high surface area to volume ratio. The diameter of nanotubes are just a few nanometers wide while their lengths can be almost a millimeter long.

3 where chiral indices n = m. Thus, having chiral vector (n, n).

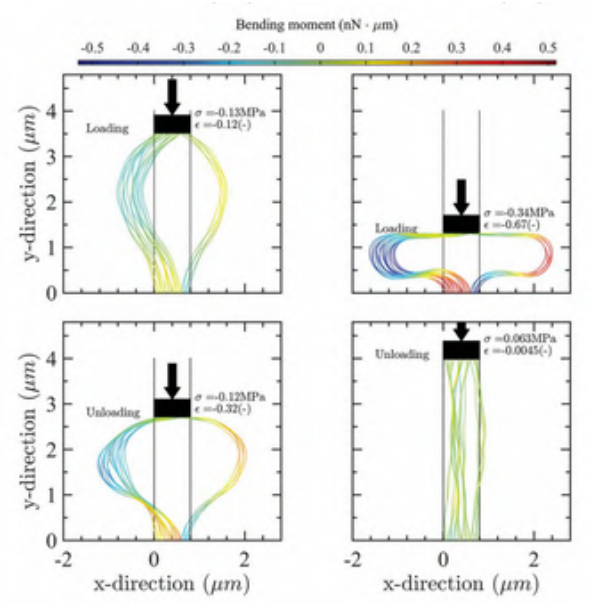


Figure 2.10: Compressive behaviour of CNTs after loading and unloading [7]

However, when nanotubes are in a bundle they are bonded to each other by weak van der Waals' forces. This force generates a weak attractive force between the atoms separated by a distance and a repulsive force when the atoms are compressed. Figure 2.10 shows simulations of an experimental setup to test the behaviour of nanotubes under stress using a flat punch nano-indentation setup. It showed that the van der Waals' interaction between individual tubes make them stick to eachother during loading and unloading [7]. This weak force make the CNTs bend, and even stick to the flat punch setup. This *foam-like* property of nanotube bundles make it clear that they are not able to fully make use of the intrinsic strength of a single nanotube. However, CNTs can be used as an extra material to increase the tensile strength of existing materials such as carbon fibres [39] or as a framework to hold up other structures. Thus, in order to realize mechanical structures with high aspect ratios, an extra coating material is required.

2.4 NANO-COMPOSITE OF CNT AND SIC

Now that we understand the shortcomings of the mechanical properties of CNTs, we will now see how using a filler material to form a *nano-composite* is useful. Due to the porous nature of nanotubes, it is possible to infiltrate the forest by deposition of a nanoscale coating. This technique is highly dependent on the density of the nanotubes made (should have good porosity) and the method of deposition used to infiltrate the forest.

One work by C. Silvestri et al. showed the effects of conformal coating of vertically aligned CNTs [8]. Micro-pins of CNTs were patterned and coated with SiC to study the thermal transport efficiency. This is shown below in Figure 2.11. One major advantage observed was that the defects formed by CVD grown CNTs provided bonding sites for the nucleation of the filler material. The penetration depth of LPCVD of SiC coated nanotubes was found to be around 66μm. It was found that there was a remarkable enhancement in heat dissipation and thermal conductivity of the nano-composite compared to the uncoated CNTs.

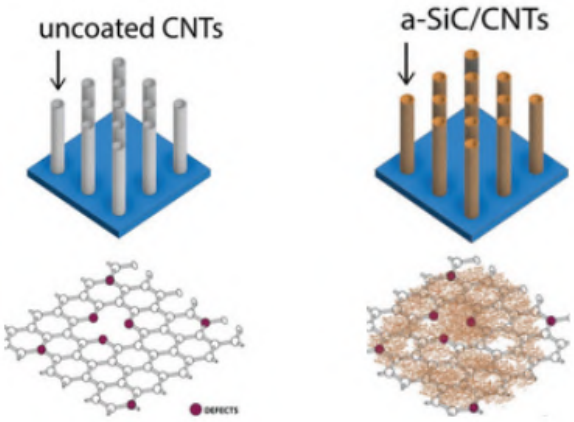


Figure 2.11: Conformal coating of CNT and SiC [8]

Fabrication process

In order to create high aspect ratio 3D structures, a framework of Vertically aligned carbon nanotubes (VACNT) infiltrated by a filler material by LPCVD can be used. This has been demonstrated in the work by Hutchison et al. [9]. The process diagram is shown below in Figure 2.12 and the fabrication involves three major steps -

- *CNT forest growth*
  We have already studied the growth process of CNTs previously. This is the step that helps provide the framework for the high aspect ratio structure to be fabricated. The substrate consists of a patterned film of Fe and Al_2O_3 to act as catalysts for the nucleation of nanotubes. The role of Al_2O_3 is to obtain a better quality of nanotubes and help prevent the Fe catalyst from being poisoned during growth[40]. Under the proper conditions, it was observed that the CNT growth rate was approximately $1\mu m/s$ at $750^{\circ}C$ [9].

- *CNT forest filling*
  After the growth of the nanotubes, the next step is to deposit the filler material and infiltrate the forest. In the work [9], the CNT forest was filled by polycrystalline silicon by LPCVD for $2\,hrs$ $50\,mins$ and silicon nitride for $3\,hrs$. It has been observed that LPCVD is the best method for filling the nanotube forest since it achieves the highest penetration depth. Another advantage of LPCVD is the fact that it can make use of the large internal surface area which are hundreds of micrometers tall by using very little of the filler material (less than a hundred nanometers) to completely fill the nanotube forests. For our work we will be depositing SiC on the nanotubes and this has been experimented in previous works such as [31].

- *Release of the structure*
  After depositing the filler material, it can be observed that the area above the substrate which is not part of the structure also gets coated. This is called the *floor layer* and needs to be removed before releasing the structure. Since this layer is only a few nanometers thick, it can be etched away by a simple RIE method. This would only take a few minutes and it was observed that this would also etch away the top layer of the nano-composite structure. Since this is only a few nanometers compared to the height of the nanotubes (order of microns), it does not affect the structure by much. This step is followed by the 'release' of the structure by removing the underlying oxide layer by using a buffered oxide etch (BOE) or Vapour HF.

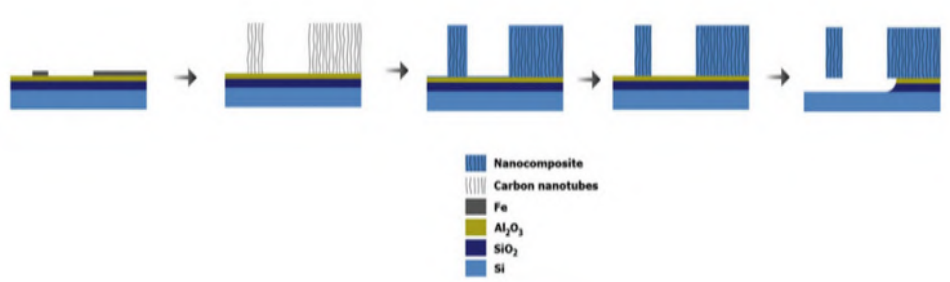


Figure 2.12: Process flow of CNT/SiC nano-composite technique [9]

Electrical properties

We have already studied the electrical properties of CNTs in a previous section. The properties of the nano-composite can be investigated using a collinear four-point measurement setup. In the work of Hutchison et al. this was studied using the *Magnetron Instruments 750-1* setup [9]. The results obtained are shown in the Figure 2.13.

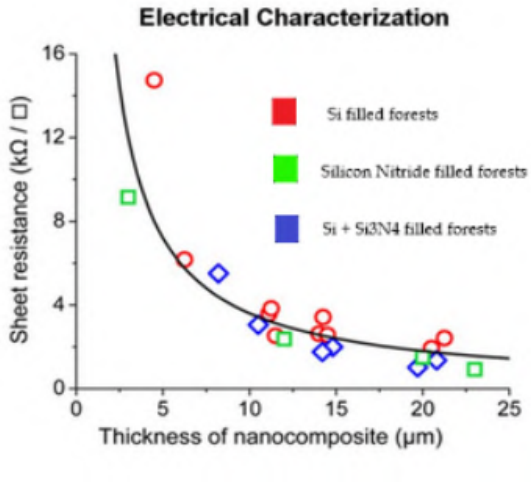


Figure 2.13: Electrical characterization of the nano-composite [9]

It can be observed from the results that the sheet resistance of the nano-composite is inversely proportional to the thickness. This was tested for three different filler materials - poly-silicon (red), Si_3N_4 (green) and a combination of poly-silicon and Si_3N_4 (blue). One astonishing thing observed was that an insulating material such as Si_3N_4 showed conductive properties. The resistivity of the poly-silicon nano-composite was found to be around 6 orders of magnitude lower than regular poly-silicon [9]. These enchancements in electrical properties is due to the underlying CNT framework. The nanotubes provide a conducting path through the nano-composite and thus increases the overall conductivity.

Mechanical properties

We have already learned that in order to realize mechanical structures with CNTs, a filler material is mandatory. The mechanical properties of the obtained nano-composite will be investigated in this section. The work by Rene Poelma et al. investigated the mechanical properties nano-composite using a flat punch nano-indentation setup [7]. This is shown below in Figure 2.14.

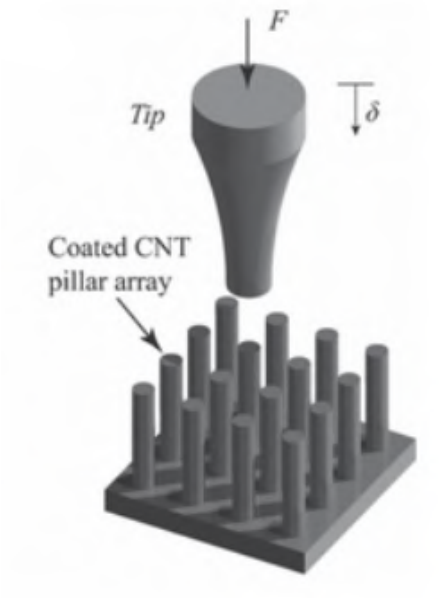


Figure 2.14: Flat punch nano-indentation setup [7]

One main conclusion from the work is that increasing the coating thickness of the nano-composite leads to an exponential increase in compressive strength and stiffness. This can be observed in Figure 2.15. We see that the Young's modulus of the coated CNT arrays are orders of magnitude greater than the uncoated pillars. The discrepancy between the simulated value and the experimental value of the thick coated pillar was due to errors in the simulations that lead to over estimation.

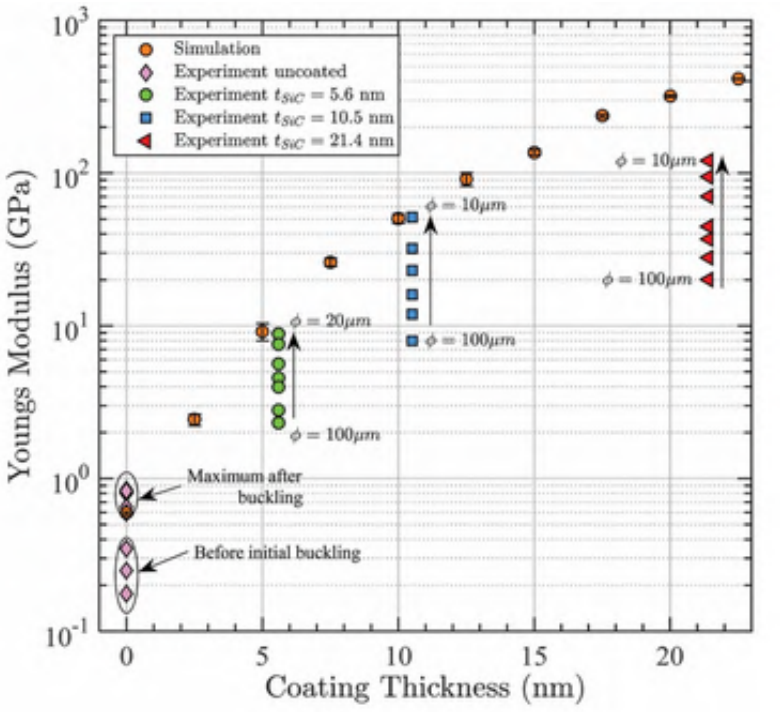


Figure 2.15: Young's modulus of coated and uncoated CNT arrays [7]

However, one main observation was made in the work [9] is that compared to the original filler material, there was not much increase in Young's modulus after using CNTs. This is due to the fact that the nanotubes contribute to only 1% of the total mass and about 7% of the total volume [9]. Therefore, we can conclude that the mechanical properties of the nano-composite depends entirely on the type of filler material used.

2.5 CONCLUSIONS

In this chapter, we have studied the previous literature that have been published on accelerometers, carbon nanotubes and silicon carbide. The working principle of a simple comb type capacitive accelerometer was studied and helped us understand the parameters to be considered while designing the structure. We also understood the limitations of the device especially under harsh environments. This was followed by investigating the properties and merits of silicon carbide (SiC) and carbon nanotubes (CNT). Having studied the literature we could conclude that the technique of incorporating a nanocomposite of SiC and CNT proves to be quite promising to create high aspect ratio surface micromachined structures.

3 MODELLING AND SIMULATION

Having studied the literature, a decision was made to create a mechanical sensor using the technique of CNT nano-composite. Understanding the limitations of the current MEMS based accelerometers it was clear that fabricating a resilient device that could survive harsh temperatures would be highly beneficial.
In this chapter, we will first investigate the state of the art, comb type accelerometer using the tool *COMSOL Multiphysics 5.4* in section 3.1. This is followed by modelling a spring to suit the specifications needed for our design in section 3.2. Section 3.3 consists of the detailed modelling and simulation of the high aspect ratio comb type accelerometer.

3.1 OVERVIEW OF THE GENERIC DESIGN

The current techniques of fabricating an accelerometer is by means of surface micro-machining. However, a few innovative methods have also been developed such as silicon-on-glass (SOG)[41] and double glass modified silicon-on-glass (DGM-SOG)[23]. These methods also make use of a combination of lateral and vertical accelerometers to make 3-axes sensing possible. Although the fabrication techniques are quite complicated, the devices made by these methods have shown excellent results.

Since we are experimenting on a new fabrication technique in this work, a decision was made to keep the design relatively simple. The design is motivated by the case study in the book *Microsystems design* [4]. An example of this design can be found as a template in the *COMSOL* website [10]. The specifications of the design is shown below in table 3.1.

Table 3.1: Simple accelerometer specifications

Specification	Value
Proof mass (length x width) [μm]	448 x 100
Device thickness [μm]	2
Etch hole area [$(\mu m)^2$]	16
Fingers (length x width) [μm]	114 x 4
Total fingers (sense + self test)	21 + 6
Finger overlap length [μm]	105
Spring (length x width) [μm]	280 x 2
Spring gap [μm]	1
Anchor (length x width) [μm]	20 x 20

The model consists of subsequences of the proof mass, spring and electrodes that are called into the main geometry. This makes assigning domain physics and boundary conditions easy. The model is entirely made of polysilicon material and also consists of a rectangular air domain surrounding it to simulate the damping. The *Electromechanics* multiphysics is used where the structure is subjected to acceleration through the 'Body load' physics. The fixed electrodes are set at constant potentials while the proof mass is at a floating potential. The value of this floating potential is determined by the position-dependent capacitance [10].

Simulating the normal operation, the displacement of the proof mass is swept from $-50g$ to $+50g$ as shown below in figure 3.1. We can see that the maximum displacement observed at $+50g$ is $\approx 70\,nm$.

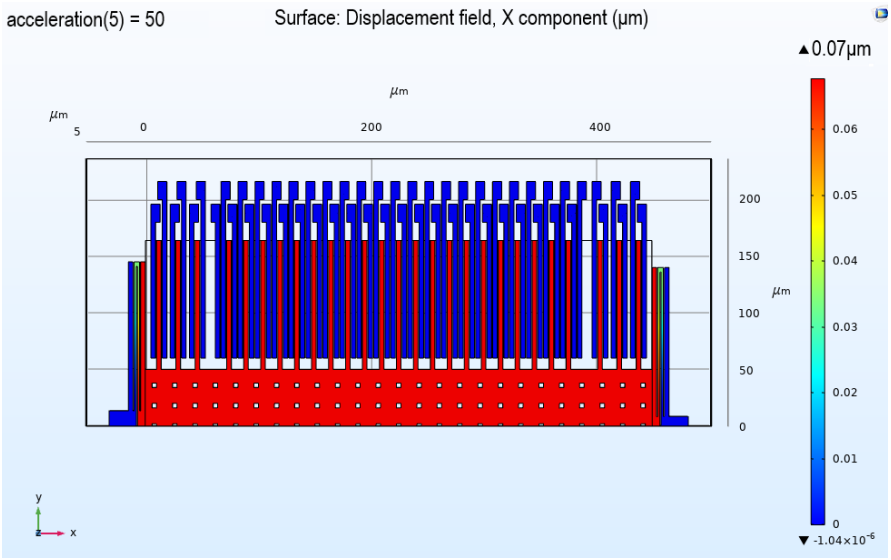


Figure 3.1: Surface micromachined accelerometer [10]

The simulation of displacement is done by directly measuring the distance moved by a single point on the proof mass. The results obtained for 5 different accelerations are linear fitted as shown in figure 3.2. Thus, plotting the result using the 2D plot group, the linear relationship between the applied acceleration and the observed displacement can be observed.

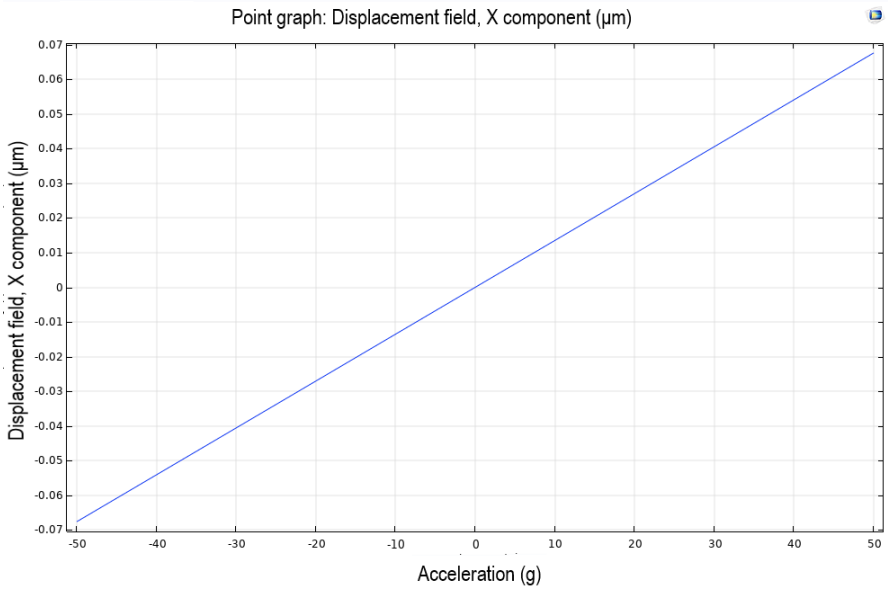


Figure 3.2: Displacement vs. applied acceleration

However, in reality this displacement is measured via the capacitive coupling between the fingers and the fixed sense electrodes. During the normal operation of the device, the entire proof mass is floating at approximately half the supply voltage. The fixed electrodes are connected to a high frequency square wave swinging from zero to full supply and opposite phase on both the sides. Thus, the movement of the proof mass induces an amplitude proportional to the displacement. The average electrostatic force between the fingers and the fixed electrodes is nulled by this

setup and helps have better signal processing [10].

In the simulation, the 'stationary' study makes it easy to model the square wave and obtain the sense voltage. The amplitude of the square wave is reduced by a factor of 1000 to make the simulation simpler. We can see the linear relationship between the sense voltage to the applied acceleration in figure 3.3. In practice, this signal is later fed to an amplifier for post-processing.

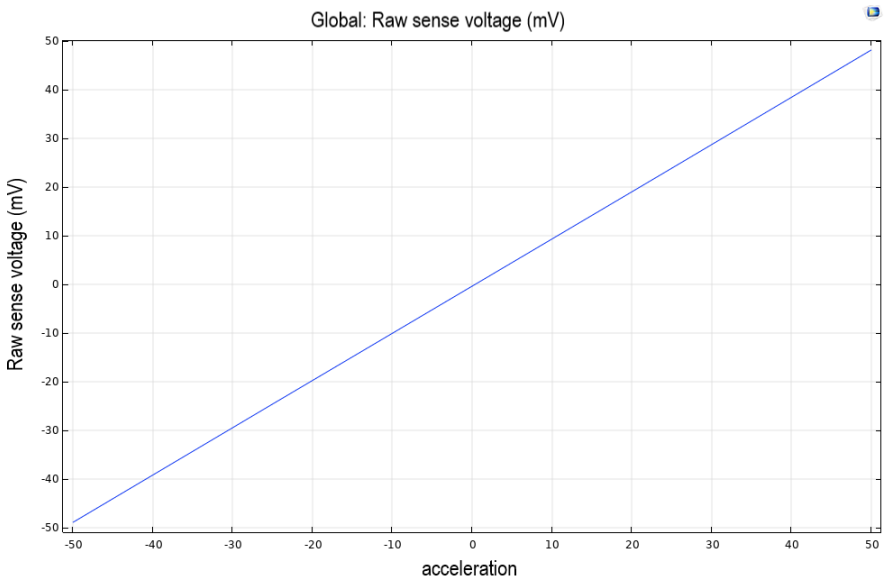


Figure 3.3: Sense voltage vs. applied acceleration

In order to calculate the sensitivity of this design we first calculate the effective spring constant using equation 2.4. Substituting the parameters E = 160 GPa (Polysilicon), w = h = 2 μm, $L_1 = L_2$ = 120 μm we can calculate this parameter.

The mechanical sensitivity as shown in equation 2.2 depends on the mass and effective spring constant. In order to obtain the effective mass we can use the simply multiply density with the effective volume as shown below in equation 3.1. Calculating this using the parameters shown in table 3.1 and $\rho_{Si} = 2330\ kg/m^3$, h = 2 μm., 'm' subscript refers to the proof mass, 'f' refers to the fingers and 'o' to the etch holes.

$$M_{eff} = \rho * h((w_m * l_m) + (N_f * w_f * l_f) - (N_o * w_o * l_o))\ [kg] \tag{3.1}$$

The electrical sensitivity on the other hand, can be calculated by substituting the parameters $\epsilon_{air} = 8.854 * 10^{-12}$ F/m, N = 21, h = 2 μm and d = 2 μm in the equation 2.9 and the total sensitivity can then be calculated using equation 2.10. Tabulating all these results we obtain the following as shown in table 3.2.

Table 3.2: Theoretical results of the generic design

Specifications	Value
Effective spring constant [K_{eff}]	3.006 N/m
Effective mass [M_{eff}]	$3.141 * 10^{-10}$ kg
Mechanical sensitivity [S_{mech}]	1.024 nm/g
Electrical sensitivity [S_{elec}]	0.372 $fF/\mu m$
Total sensitivity [S_{tot}]	$3.81 * 10^{-4}$ fF/g

We can clearly observe that the sensitivity of this design is quite low. *It is also important to note that there have been many innovations made to have a better performance*

of an accelerometer. This work is focusing on improving the generic design to obtain a large enough displacement that can easily be measured. One cause of this low sensitivity observed is due to the fact that we are limited by the constraints of maximum height and dimensions of the proof mass. Therefore, making a high aspect ratio structured design would provide higher electrical sensitivity. This can be proved as follows,

$$S_{tot} = S_{mech} * S_{elec} \tag{3.2}$$

We see that the height 'h' for the mechanical sensitivity gets cancelled out due to equations 2.4, 3.1. 2.2. Thus, the height has no effect on the mechanical sensitivity. But the electrical sensitivity is directly proportional to the height 'h' 2.9. Therefore,

$$S_{tot} \propto h \tag{3.3}$$

However, there is an upper limit to how high the structures can be made before bending of the CNTs become an issue [9]. Typically for unsupported structures, an aspect ratio [1] of greater than 6 leads to bending. Therefore, we now have our two constraints for designing our device.

3.2 DOUBLE MEANDER SPRING DESIGN

We have explained the modelling and performance of the traditional surface micromachined accelerometer in the previous section. However, one observation that can be made here is that mechanical sensistivity is inversely proportional to the stiffness (spring constant) of the spring (equation 2.2). The spring stiffness is directly proportional to the the height of the structure as seen in equation 2.4. Thus, increasing the height to make it a high aspect ratio structure would lead to an increase in spring stiffness. This increase in stiffness is compensated by an equivalent increase in the effective mass. Thus, incorporating a high aspect ratio is not a detriment to the mechanical sensitivity and in-fact leads to an increase in electrical sensitivity.

The high aspect ratio accelerometer now has a higher total sensitivity due to the increase in height. The mechanical sensitivity however can be further increased by decreasing the spring stiffness. This has been achieved by using a double meander spring structure as shown below in figure 3.4.

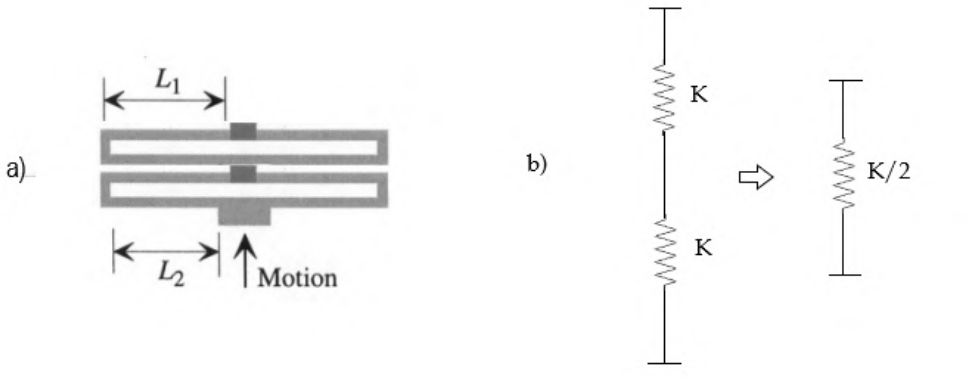


Figure 3.4: a) Double meander spring structure b) Equivalent spring constant

1 ratio of height to width

The spring constant of this structure would be half the spring constant of the single meander spring.

$$K_{dm} = \frac{K_{spring}}{2} \tag{3.4}$$

Since there are two springs on either side of the proof mass the effective spring constant is shown below. Here, we take the same approximation as before, $L_1 = L_2$.

$$K_{eff2} = 2 * K_{dm} = K_{spring} = (\frac{\pi^4}{6}) \frac{E * h * w^3}{(2L_1)^3 + (2L_2)^3} \tag{3.5}$$

We can see that the effective spring stiffness decreases by a factor of 2. It was decided to fabricate a variety of accelerometer designs in order to obtain sufficient data points during analysis. The variations of the springs used in the design in this thesis with their effective spring constant is shown below in table 3.3; here, we assume the Young's modulus of SiC (E_{SiC}) = 400 GPa, and the height (h) $\approx$ 15 μm (target height of the CNTs).

Table 3.3: Spring variations used in design

	Spring width (w) [μm]	Spring length (L_1,L_2) [μm]	Effective spring constant K_{eff} [N/m]
Single Meander	2	175	18.17
	3	175	61.34
	3	75	779.27
Double Meander	3	175	30.67
	4	175	72.70
	3	75	389.63

Having multiple variations of design will give us sufficient data points to then study the effects of varying parameters. After simulating multiple variants it was observed that spring widths of 2 μm show the highest displacement due to low spring stiffness but cannot be made too tall as the CNTs would begin to bend. Spring widths greater than 4 μm show extremely low mechanical sensitivity. Therefore, it was decided that single meander spring structures do not have the 4 μm variant and the double meander spring structures do not have the 2 μm. With the calculations shown above we can see that the double meander structure has a smaller spring stiffness compared to the single meander structure of the same spring width and naturally would show more displacement.

3.3 DESIGN SIMULATION

In this section we will model and simulate the various designs of comb type capacitive accelerometers that are to be fabricated. Having designed the double meander spring in the previous section, we see that there are 6 variations of the spring used. Each of these variations would also have another variant where the finger gap would be different. This would help us observe the variation of electrical sensitivity with finger gap. Thus, we will have 12 different types of accelerometers with varying performance. We will now study these designs by grouping them broadly as single meander spring structures 3.3.1 and double meander spring structures 3.3.2.

3.3.1 Single meander spring accelerometer variants

A single meander variant of the comb type accelerometer is the same as the state of the art design but with a higher aspect ratio. The figure 3.5 below shows the main parts of the design that include - the proof mass, fixed/moving electrodes and the spring. The fingers that are placed farther apart in the model are used for self test[2].

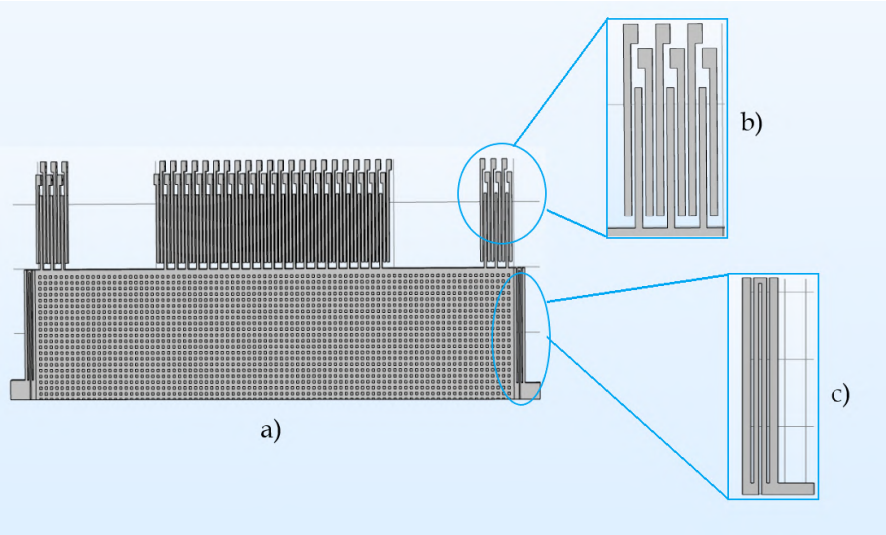


Figure 3.5: a) Single meander accelerometer b) Fixed/moving electrodes with gap d c) Spring with width w

There are 6 different variations of the single meander structures used in this work. These variants are made by changing the proof mass dimensions, the finger gap and the spring width; or a combination of these. The variants made are shown below in table 3.4.

Table 3.4: Single meander spring accelerometer variants

Proof mass dimensions [μm]	Finger dimensions [μm]	Spring length (L) [μm]	Spring width (w) [μm]	Finger gap (d) [μm]
800 x 400	120 x 4	175	2	2
800 x 400	120 x 4	175	2	3
800 x 400	120 x 4	175	3	2
800 x 400	120 x 4	175	3	3
400 x 200	60 x 4	75	3	2
400 x 200	60 x 4	75	3	3

These variants were simulated on *COMSOL Multiphysics 5.4*. The detailed results obtained are attached in Appendix A. The thickness of all the structures are assumed to be $H \approx 15\mu$m. The filler material to be used will be SiC with $\rho_{SiC} = 3210\ kg/m^3$.

The effective mass of the $800\,x\,400\,\mu m$ variants has been found to be $1.36 * 10^{-8}[kg]$ and that of the $400\,x\,200\,\mu m$ ones to be $0.34 * 10^{-8}[kg]$ using the equation 3.1. We shall now calculate the theoretical sensitivity of all the variants using the same equations as shown in section 3.1. The results obtained were as follows,

2 Applying a voltage to the fixed fingers causes the electrostatic force induced to make the proof mass move. Used for calibration.

Table 3.5: Theoretical results of single meander spring variants

Mechanical sensitivity (S_{mech}) [nm/g]	Electrical sensitivity (S_{elec}) [fF/μm]	Total sensitivity (S_{tot}) [fF/g]	Simulated mechanical sensitivity [nm/g]
7.320	3.453	0.0252	4.6
7.320	2.302	0.0168	4.6
2.170	3.453	0.0075	1.8
2.170	2.302	0.005	1.8
0.0428	1.726	$73.87 * 10^{-6}$	0.036
0.0428	1.151	$49.26 * 10^{-6}$	0.036

We can see that the total sensitivity of these high aspect ratio variants are much better than the generic surface micromachined accelerometer. Although the smaller variants show worse sensitivity, they have the highest probability of being structurally stable. Thus, it was decided to have these small variants as a backup during fabrication.

3.3.2 Double meander spring accelerometer variants

Since the spring stiffness of the double meander variants are half the value of the equivalent single meander structure, theoretically we can assume to get almost twice the sensitivity. The *COMSOL* model for the variant is shown below in figure 3.6.

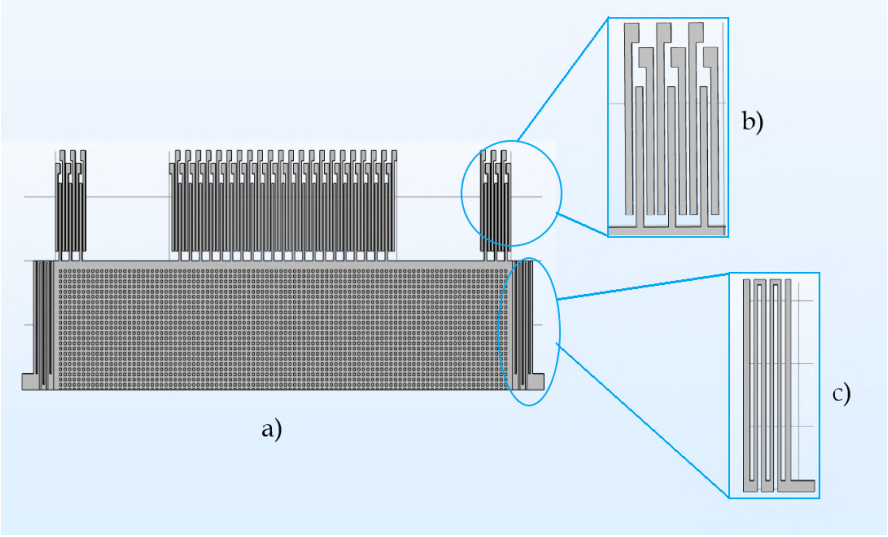


Figure 3.6: a) Double meander accelerometer b) Fixed/moving electrodes with gap d c) Spring with width w

Due to the nature of the spring design of the double meander structure, it was decided to not have a 2μm wide spring due to the fact that it could be structurally unstable.

Table 3.6: Double meander accelerometer spring variants

Proof mass dimensions [μm]	Finger dimensions [μm]	Spring length (L) [μm]	Spring width (w) [μm]	Finger gap (d) [μm]
800 x 400	120 x 4	175	3	2
800 x 400	120 x 4	175	3	3
800 x 400	120 x 4	175	4	2
800 x 400	120 x 4	175	4	3
400 x 200	60 x 4	75	3	2
400 x 200	60 x 4	75	3	3

The detailed simulated results are attached in Appendix B. Using the same theoretical values as the previous section, we obtain the results as tabulated below 3.7.

Table 3.7: Theoretical results of double meander spring variants

Mechanical sensitivity (S_{mech}) [nm/g]	Electrical sensitivity (S_{elec}) [fF/μm]	Total sensitivity (S_{tot}) [fF/g]	Simulated mechanical sensitivity [nm/g]
4.342	3.453	0.015	4.6
4.342	2.302	0.01	4.6
1.831	3.453	0.0063	2
1.831	2.302	0.0042	2
0.0856	1.726	$147.74 * 10^{-6}$	0.12
0.0856	1.151	$98.52 * 10^{-6}$	0.12

3.3.3 Observations

Having simulated the accelerometer variants, the results obtained were used to plot the dependence of dimensions on performance. The plots were generated using *MATLAB R2019b*. Using these plots, a few observations can be made.

The first plot is the variation of displacement at $+50g$ with the spring width used for both single meander and double meander variants. This is shown below in figure 3.7. We can see that since the mechanical sensitivity is inversely proportional to the spring width (equations 2.4, 2.2), a $1\,\mu m$ increase in the width of the spring leads to a significant decrease in the displacement. However, by utilizing a double meander spring of the same thickness we obtain the same displacement as observed by a single meander of lesser width.

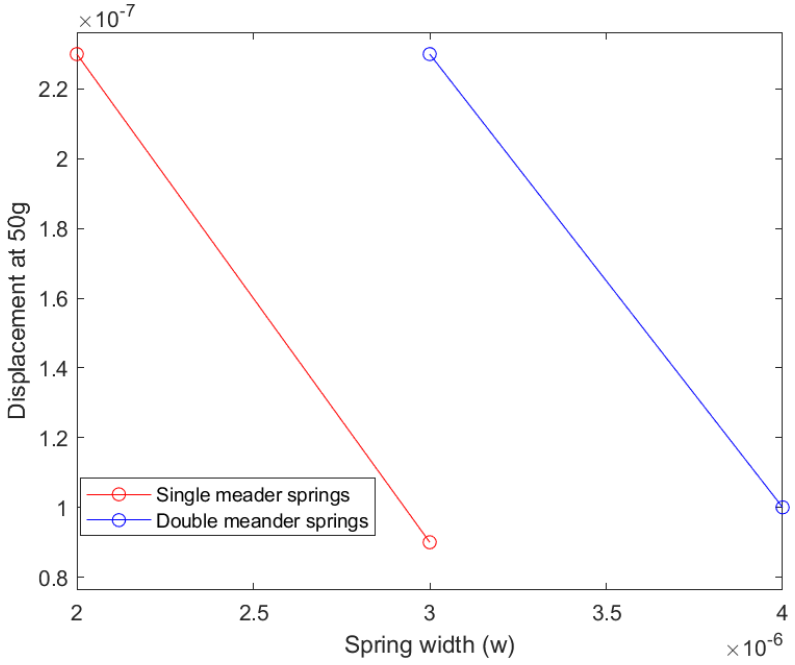


Figure 3.7: Displacement at 50g vs. spring width

The second plot is the variation of displacement at $+50g$ with the spring length used for both single meander and double meander variants, shown in figure 3.8. This compares the big variants ($800\,x\,400\,\mu m$) with the small ones ($400\,x\,200\,\mu m$) for the same spring width of $3\,\mu m$. The spring lengths are given in table 3.4, 3.6. Using the same equations 2.4, 2.2 we can see that the mechanical sensitivity is directly proportional to the spring length. Since the effective spring constant of the double meander structure is half that of the single meander, we can see this factor of 2 reflect on their slope in figure 3.8.

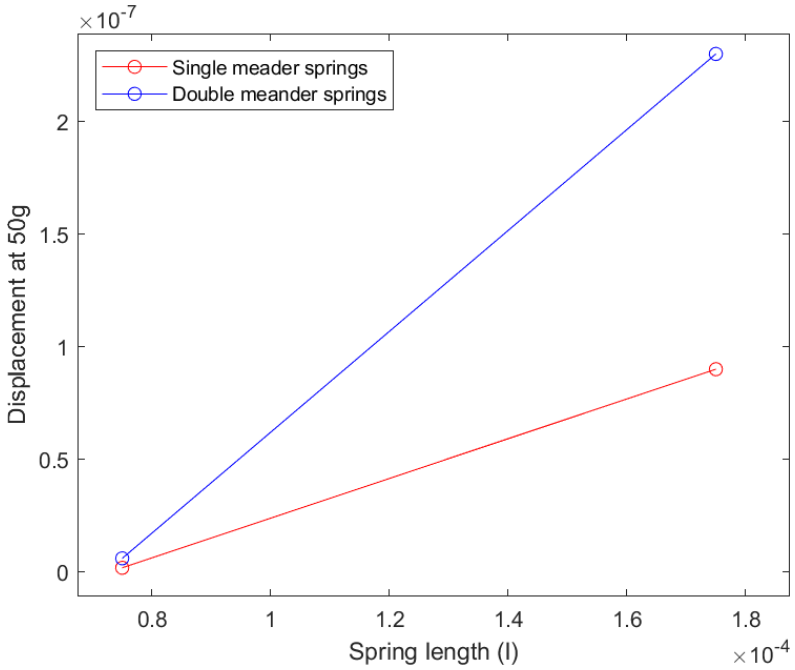


Figure 3.8: Displacement at 50g vs. spring length

3.4 CONCLUSIONS

In this chapter, we investigated the state of the art design of the comb type capacitive accelerometer using the *COMSOL Multiphysics 5.4* simulator. It was observed that the performance of this generic design was quite low. One reason can be attributed to the limited aspect ratio of the structure. Making a high aspect ratio structure required some modifications to be made to the spring. A double meander structure was incorporated which would effectively decrease the spring stiffness by half.

In order to have sufficient data points to analyze the effects of the parameters, multiple variations of the design was made. These can be broadly classified into single meander and double meander structures, each of which have variations in proof mass, spring width and finger gap. It is important to note that, the reason for the slight discrepancy in the theoretical and simulated mechanical sensitivity is due to the squeeze film damping beneath the proof mass implemented in the simulation. With the results obtained in the simulations we can make a couple of observations -

- The spring width is a very important parameter to be carefully chosen. Due to its cubic dependence to spring stiffness, it would make sense to make it as low as possible (increases aspect ratio).
- For higher aspect ratios, bending of nanotubes would become an issue and incorporating support beams is not an option for an accelerometer. Thus, there is a lower limit to how small the spring width can be made and an upper limit to how tall they can be made.
- The total sensitivity of the large structures (proof mass = 800 x 400 μm) 3.7, 3.5 is orders of magnitude greater than that of the generic design 3.2. The smaller variants (proof mass = 400 x 200 μm) although have poor performance, they have higher structural stability (due to smaller and thicker dimensions) and is kept as a safe option during fabrication.

4 MASK DESIGN AND PROCESSING

So far, we have understood the literature and the previous work done with respect to CNT nano-composites. This was followed by simulating the various structures on *COMSOL Multiphysics* to obtain a theoretical value of the performance.
In this chapter, the mask design using the *L-edit* tool is presented in section 4.1. This will help define the flowchart and the cleanroom processing which is discussed in detail in section 4.2.

4.1 MASK LAYOUT

Photolithography is the process where patterns are created on thin films on semiconductor wafers [12]. This process generally has three steps - coating, exposure and development. The thin films used are photosensitive polymers called *photoresist*. This is coated on the silicon wafer through spin coating. The patterns are created on this layer by exposure through a *photomask*[1]. There are two types of photomasks namely, the brightfield and the darkfield masks are shown below in figure 4.1.

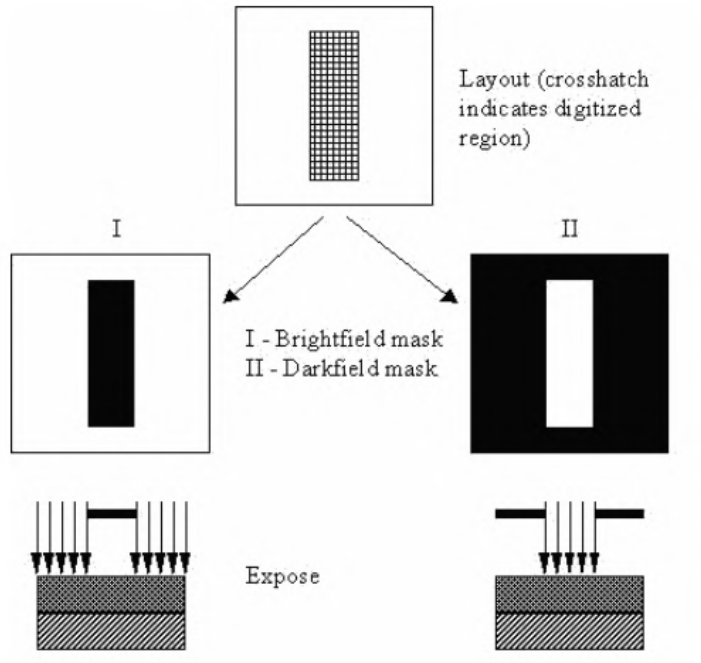


Figure 4.1: Illustration of types of photomasks [11]

The type of photoresist used decides the effect of the exposure. A positive photoresist makes the exposed parts of the layer soluble during development whereas a negative photoresist makes the parts of the layer insoluble. In general, the choice of photoresist depends upon whether we want a layer to be subtracted (etching) or added (lift-off) respectively. However, etching/subtraction of a layer can be performed using both types of photoresists. This is depicted in the figure 4.2.

1 A transparent chrome plate with opaque regions at specific places.

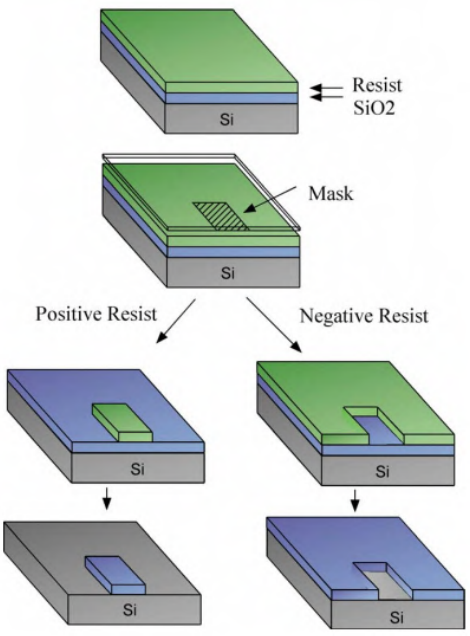


Figure 4.2: Effects of exposure of a positive and negative photoresist using a brightfield mask [12]

In this design we will be using four masks to fabricate the capacitive accelerometer. Each mask describes a particular layer (the Titanium nitride (TiN), the Al_2O_3, catalyst and contact pads). Another thing to note is the naming convention of the different variations used in my mask set. This was necessary to make it easier to identify the structures during characterization. There are 12 different variants of accelerometers with 4 structures per variant denoted by 2 numbers. The first number indicates the spring width and the second denotes the finger gap (eg - III-II indicates that the spring width = 3 μm and finger gap = 2 μm). Structures depicted by just one number indicates the finger gap only. Shown below in figure 4.3 is the top view layout of all the variants present in the mask. These will be discussed in detail in the upcoming sections.

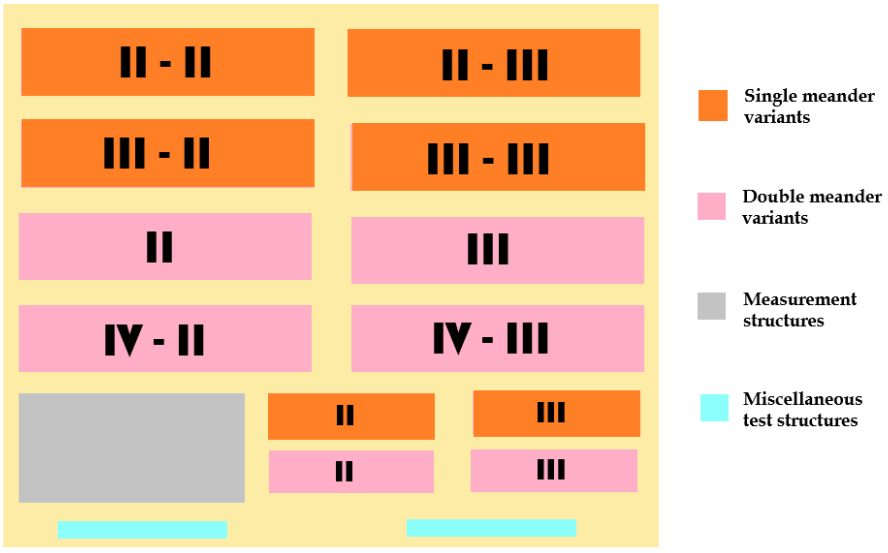


Figure 4.3: Top view layout of the mask set

4.1.1 Accelerometer variants

There are 12 different variants of accelerometers used in the mask set as seen in figure 4.3. Each variant has 4 individual accelerometers for the sake of redundancy. This can be seen in figure 4.4.

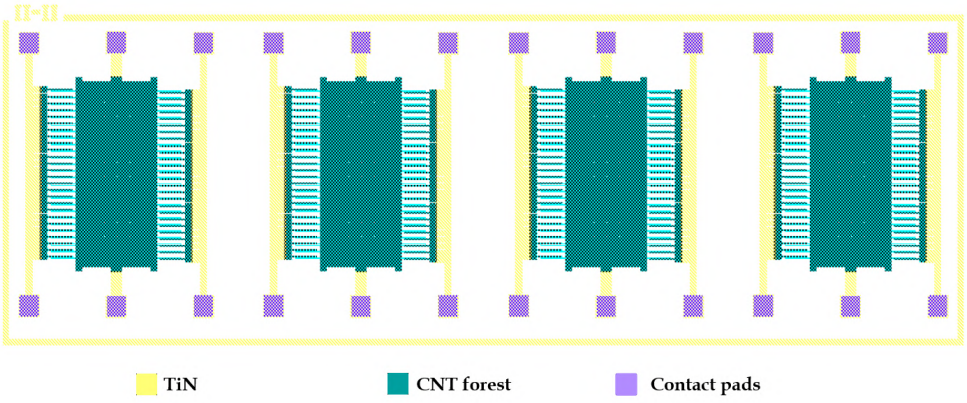


Figure 4.4: II-II variant of the single meander spring accelerometer

Having a closer look at one single accelerometer (figure 4.5), we see that one side of the proof mass has the fixed electrodes above while the other side has the fixed electrodes below. This is done avoid overlap and make fabrication easier without the need for two level metallization. Having such a design would also help measure the output diferentially since an increase in capacitance on one side would show a decrease in capacitance on the other side. TiN was chosen as the anchor for the fixed fingers since it known to be a good substrate for the growth of CNTs. The spring is either a single meander or a double meander with anchors on either side to prevent complete release of the entire structure.

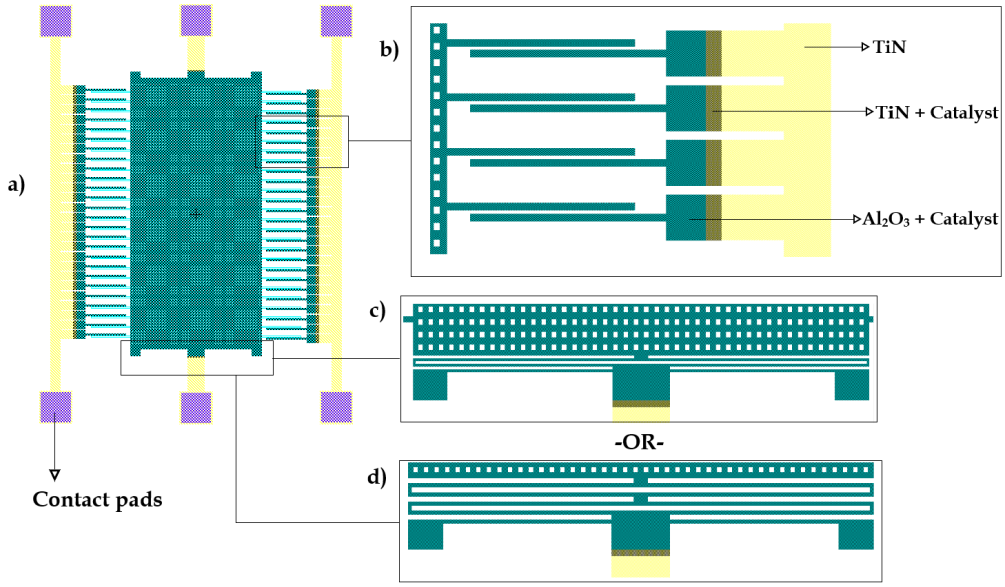


Figure 4.5: a) Top view of an accelerometer b) Fixed/moving electrodes c) Single meander spring d) Double meander spring

Another thing to note is that every junction between 2 different metal layers (TiN and Al_2O_3) has an protrusion of the catalyst. This is done to ensure that the current flow

is always from metal into the CNT, horizontally tunnelling through the nanotube forest and into the other metal. This, hypothetically should lead to lower contact resistance since the electrons can tunnel through the nanotubes directly. Contact pads have also been incorporated with a different metal layer (one that can be easily wire-bondable) on all sides.

4.1.2 Measurement structures

In order to check various electrical parameters of the design such as sheet resistance, resistivity and contact resistance, we incorporate a few measurement structures. There are 3 such structures used in this design, viz. transmission line measurement (TLM), Van der Pauw (VdP) and electrical line-width measurement (ELM) structures.
Sheet resistance ($R_\square$) is a very useful parameter to calculate since it is a measure of the lateral resistance through a thin square of material. The equation for sheet resistance is shown below in 4.1, where 'R' is the average resistance, 'ρ' is the resistivity of the material, 'L' is the length of the sample, 'W' is the width and 't' is the thickness.

$$R = \rho \frac{L}{W.t} = R_\square \frac{L}{W} \tag{4.1}$$

Transmission line measurement (TLM)

This type of measurement is typically used to obtain the contact resistance of an interface. It involves calculating the total resistance between two contacts of different lengths (l) and plotting the resistance as a function of length. An example is shown in figure 4.6. We know that the total resistance (R_T) can be written as shown below, where R_C is the contact resistance [42],

$$R_T = 2R_C + R_\square \frac{l}{W} \tag{4.2}$$

Using equation 4.2 we can observe that at the limit of $l = 0$, the total resistance would just be two times the contact resistance. Thus, contact resistance can be calculated using equation 4.3 . We can also see that the sheet resistance can be calculated using the slope of the plot, $R_\square = slope * W$, where 'W' is the width of the strip = 20 μm.

$$R_C = \frac{R_{T(l=0)}}{2} \tag{4.3}$$

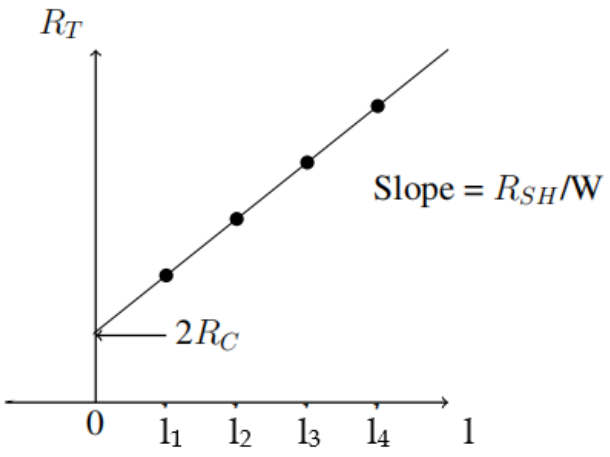


Figure 4.6: Plot to find contact resistance of TLM structure

Here, we measure the average resistance between two contacts of different lengths as shown in figure 4.7, $l_1 = 190\,\mu m$, $l_2 = 485\,\mu m$, $l_3 = 690\,\mu m$, $l_4 = 885\,\mu m$. A four point measurement is used to obtain more accurate results.

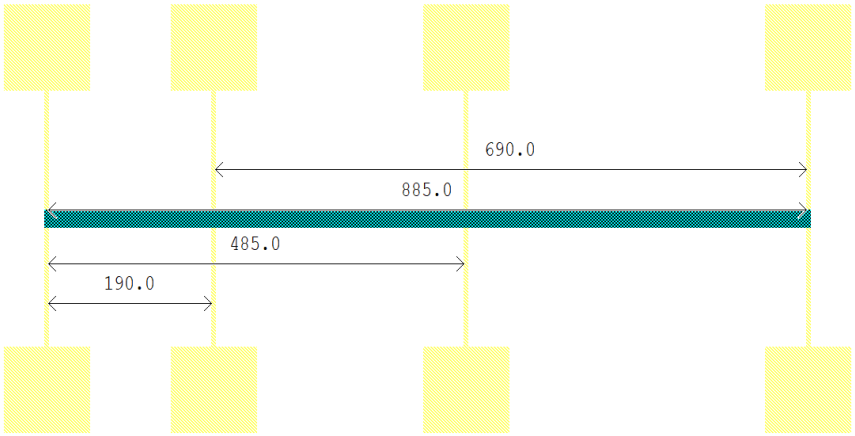


Figure 4.7: TLM structure with the various lengths chosen

There are two types of TLM structures used in this design. They are shown below in figure 4.8. We can see that the one on the left has TiN, Al_2O_3 and nanotubes as the type of contact. Thus, the electrons would pass through both the interfaces and then into the nanotubes, which hypothetically would mean higher contact resistance. The right TLM structure however does not have an overlap of TiN and Al_2O_3. The electrons would travel from the metal and tunnel through the nanotubes grown over the Al_2O_3 which would show lower contact resistance.

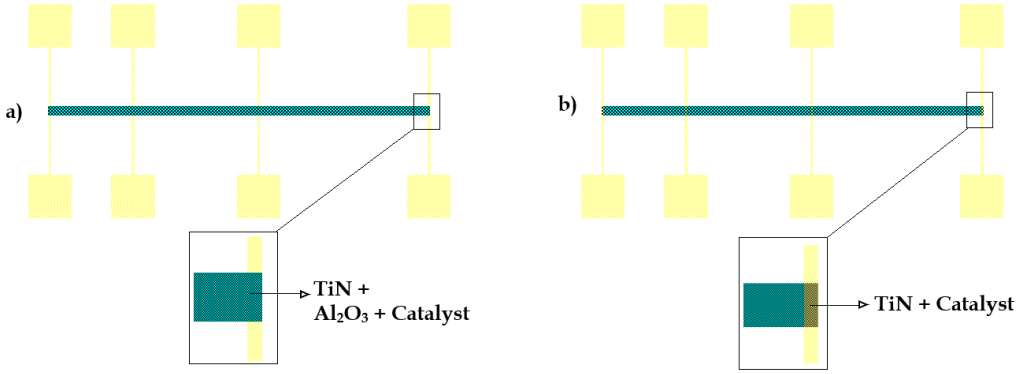


Figure 4.8: a) TLM with metal overlap b) TLM without metal overlap

Van der Pauw (VdP) structures

This technique is very useful in measuring the resistivity and sheet resistance of any arbitrary shape given that they satisfy certain criteria [43]-

- The sample thickness must be less than the width and length.
- The sample must be homogenous and isotropic.
- The sample must have uniform thickness.
- The contacts must be located at the edges of the sample.

It consists of a relatively large square area of the layer to be measured. Each corner of the square is connected to bond pads. A four probe measurement is carried out where two contacts are used to force a current while the other two are used to measure the voltage. Thus, eliminating the probe needle resistances.
This can be observed in the figure 4.9 shown below. A current is forced through pads A and B while the voltage is measured at C and D. The square in the middle has the dimensions $10\,\mu m\,x\,10\,\mu m$. The sheet resistance can be calculated using the equation below, where the first term is a correction factor for radial current flow, $R_{AB,CD}$ is the measured resistance -

$$R_{\square} = \frac{\pi}{ln\,2}\,R_{AB,CD} \tag{4.4}$$

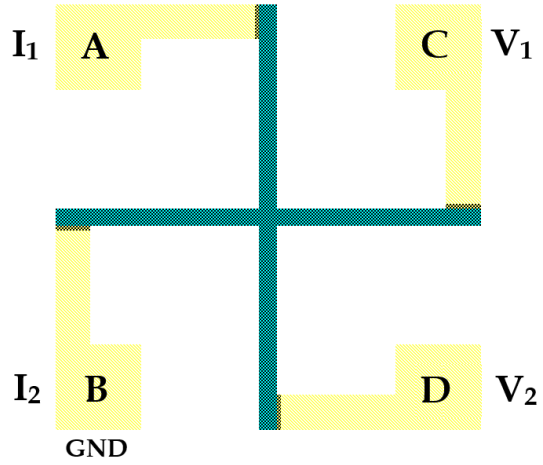


Figure 4.9: VdP structure with probe connections

We can observe that the interface between the TiN and the Al_2O_3 has a protrusion of nanotubes as discussed earlier to ensure lower contact resistance.
There are 3 different dimensions of VdP structures used in the design as shown in figure 4.10. The three variants used would help verify the fact that ideally, sheet resistance is independent of the dimensions of the layer for a VdP structure.

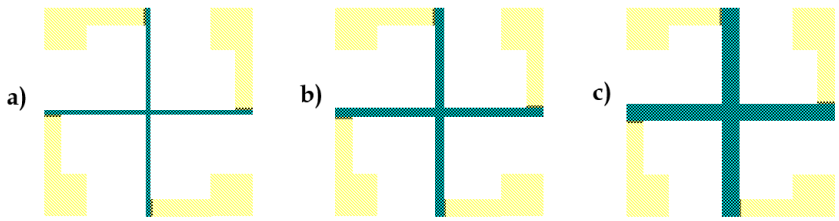


Figure 4.10: a) $5\,\mu m\,x\,5\,\mu m$ VdP structure b) $10\,\mu m\,x\,10\,\mu m$ VdP structure c) $20\,\mu m\,x\,20\,\mu m$ VdP structure

Electrical line-width measurement (ELM)

Similar to the VdP structures, the ELM is another way to measure the sheet resistance of a particular layer. We use a four point measurement to force a current through the outer most contacts and measure the voltage in the inner contacts of a strip of certain length. The length (L) chosen in the design is 290 μm. The width of the strip is varied to verify linearity [44]. Equation 4.1 can be used to calculate the sheet resistance. Figure 4.11 shows the probe connections for the ELM structure of width 10 μm.

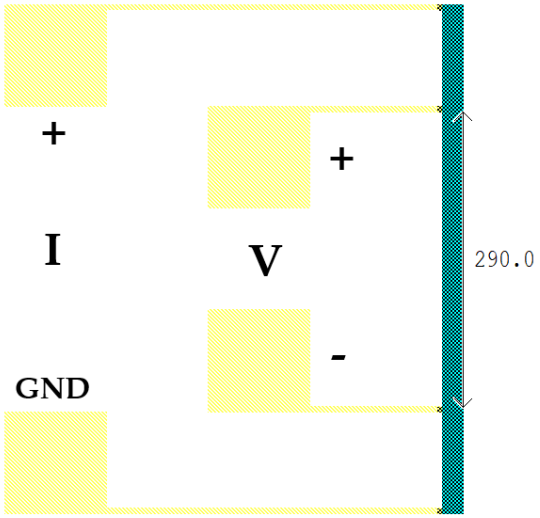


Figure 4.11: ELM structure with probe connections

The interface between TiN and Al_2O_3 has the same protrusion of catalyst to decrease the contact resistance. There are 3 variants of ELM structures implemented in the design with different widths as shown in figure 4.12.

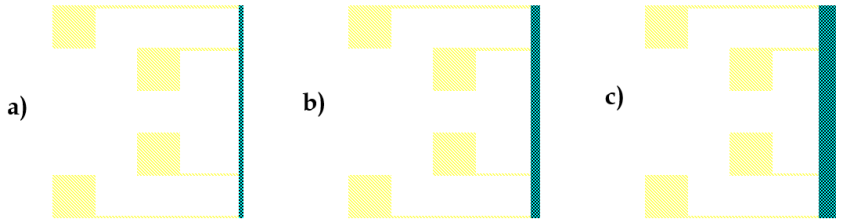


Figure 4.12: 5 μm width ELM structure b) 10 μm width ELM structure c) 20 μm width ELM structure

4.1.3 Miscellaneous test structures

There are 5 different types of miscellaneous test structures to verify various steps during fabrication. These are shown below in figure 4.13.

Figure 4.13: a) Release test b) Aspect ratios c) Etch hole test d) CNT growth test e) Contact pad test

Release test structures

This structure was designed to ensure the proper release of the fixed and moving fingers. The dimensions are shown below in figure 4.14, all the dimensions are in microns. The anchor dimensions dictate the upper limit to the etch depth during release. Since, the release is done using Vapour HF which is isotropic, we must ensure that we do not etch more than 12.5 μm.

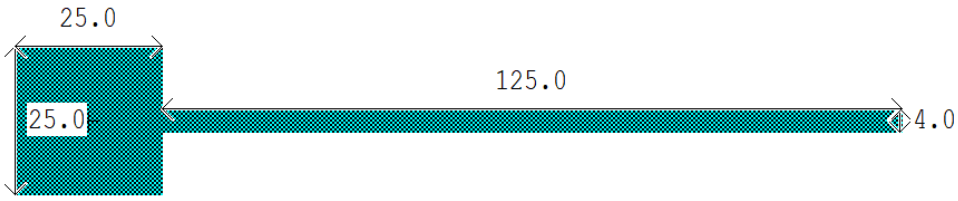


Figure 4.14: Dimensions of the release test structure

Aspect ratio structures

These structures help us decide the aspect ratio of the CNTs that can be grown. The dimensions shown in figure 4.15 are in microns. It was observed previously that this aspect ratio is approximately 6. This implies the height of the nanotubes can be 6 times the width before bending of the tubes become an issue. One thing to note that this aspect ratio limit is for bare nanotubes without any supporting structures as in the work by Hutchison et al. [9].

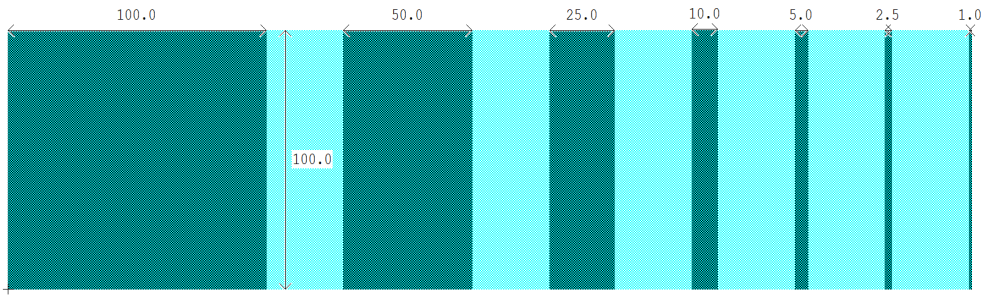


Figure 4.15: Dimensions of the aspect ratio structures

Etch hole test structures

The etch hole test structures were incorporated to check if the vapour access holes of the proof mass work as intended. This helps verify the conformal coating of the LPCVD SiC on the CNTs. The dimensions in figure 4.16 are in microns and we can see that there are two variants. The one without the Al_2O_3 base would get released at the very end and can be used to verify the release of the proof mass without any striction to the substrate.

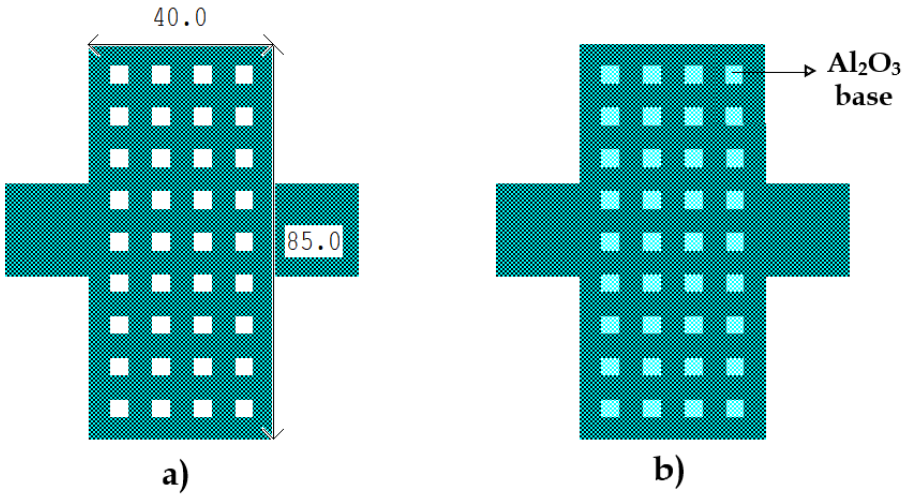


Figure 4.16: Dimensions of the etch hole test structures
a) Without the Al_2O_3 base b) With the Al_2O_3 base

CNT growth test structures

This is a very simple structure as shown in figure 4.17. It is useful to check the CNT growth on different metal layers. In our case, we can check the nanotube height on the Al_2O_3 layer and the TiN layer.

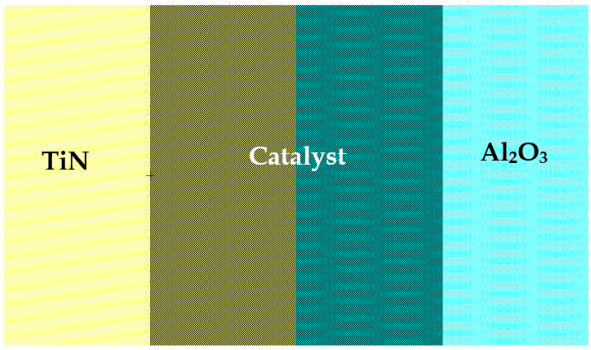


Figure 4.17: CNT growth test structure

Contact pad test structure

Since TiN is not a good wire-bondable material, a decision was made to use a different metal as a contact pad. This test structure helps verify proper adhesion of this metal with the TiN layer. The dimensions shown in figure 4.18 are in microns.

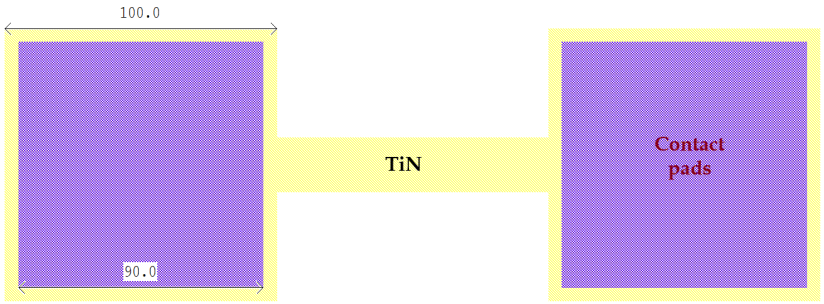


Figure 4.18: Dimensions of the contact pad test structure

4.2 PROCESSING

In this section we will investigate the various steps in fabrication of the CNT nanocomposite technique. The fabrication was carried out in the cleanroom of *Else Kooi laboratory*. The substrate used throughout the process is a standard $< 100 >$ P-type silicon wafer. Before fabricating the high aspect ratio CNT based accelerometer, we decided to test the process using an older mask set of a CNT based thermal actuator and make any modifications to the process if necessary. This thermal actuator is discussed in section 4.2.1, followed by the fabrication of CNT based accelerometer in section 4.2.2.

4.2.1 Process development

Theory :

A CNT based thermal actuator is based on the work by Vadiraj A.M et al. [13]. The thermal actuator is illustrated in figure 4.19. The working principle is based to the phenomena of Joule heating. As the device heats up, a deflection is caused in the y-direction due to thermal elongation in the s-axis.

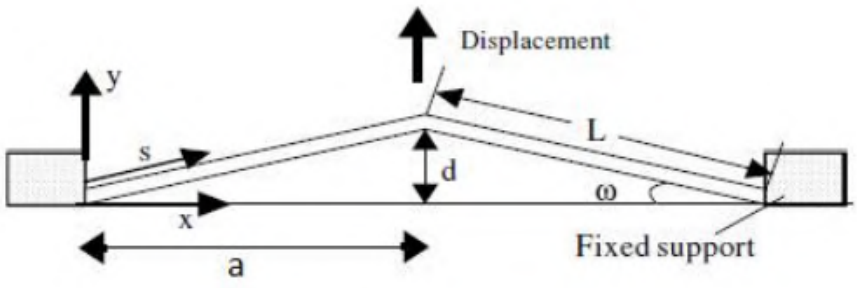


Figure 4.19: Chevron type thermal actuator [13]

The work focused on fabricating this thermal actuator using a CNT and Si_3N_4 nanocomposite. Although a very high aspect ratio of nanotubes was achieved by making use of clever supporting architectures, the release of the structure was unsuccessful.

The main cause being shielding of the floor layer by the tall structures. This caused large areas of Si_3N_4 to remain unetched during plasma etching. In order to prevent this, it was advised to keep the nanotubes short and to use less thick filler material. The general process flow is shown below in figure 4.20.

The first step is to deposit a thick oxide layer ($\approx 3\,\mu m$) using wet-oxidation in the *Tempress furnace (B1)*. The TiN layer is then sputtered using the *Trikon Sigma 204*, patterned using the *ASML PAS 5500/80* stepper and etched using the *Trikon Omega 201* to make the contact pads. The Al_2O_3 layer follows a similar lithography step to create the bridge and the shuttle mass at the centre. This is followed by the Fe layer patterning, evaporation using the *CHA Solutions std.* and lift-off using N-methyl pyrrolidone (NMP) solvent on a hotplate at 70°C. The CNTs are then grown on the patterned catalyst layer using the *Aixtron Blackmagic*. The CNTs are then coated using amorphous SiC in a *Tempress furnace (F3)*. The floor layer plasma etching is performed using the *Adixen AMS110*. The entire structure is released by etching the underlying oxide layer using the *Vapour HF tool*.

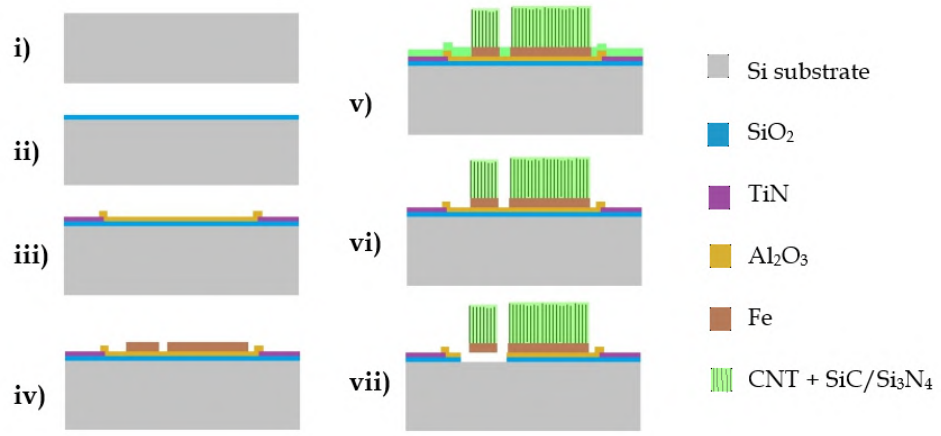


Figure 4.20: Process flow used in work [13]
i, ii) Si substrate with SiO_2
iii, iv) Patterned TiN, Al_2O_3 and Fe
v) Filler material deposition
vi) Floor layer removal
vii) Release of the structure

Using the findings obtained the the previous work, we can optimize the the process for our requirement. The flowchart used is attached in Appendix C. We can see there were a few changes made for the CNT - SiC thermal actuator compared to the original work. These are listed below -

- The TiN layer thickness was reduced ($50\,nm$) to enable proper growth of nanotubes. In the original work, this layer was $100\,nm$ thick. It was hypothesized that the cause for lack nanotube growth was the thickness of the layer hindering the sustenance of the catalyst nano-particles. Since sputtering of TiN is done by nitridizing the target, the ratio of Titanium (Ti) to Nitrogen (N) changes with thickness.

- The nanotube height was reduced to prevent plasma shielding during floor layer etch. The height was reduced from $250\,\mu m$ in the original work to approximately $10 - 40\,\mu m$ in our work.

- The filler material used in the original work was 1.25 μm of Si_3N_4. Which was quite an exorbitant amount and caused many issues during floor etch and release. Thus, it was decided to use about $20 - 50\,nm$ of amorphous SiC.

Observations :

The Al_2O_3 layer was originally planned to be sputtered using the *Trikon Sigma 204*. However, during fabrication of the first few samples it was observed that the layer being deposited was not Al_2O_3. Visual inspection shows that the layer is a thick shiny and reflective layer as opposed to a thin semi-transparent one. This is shown below in figure 4.21.

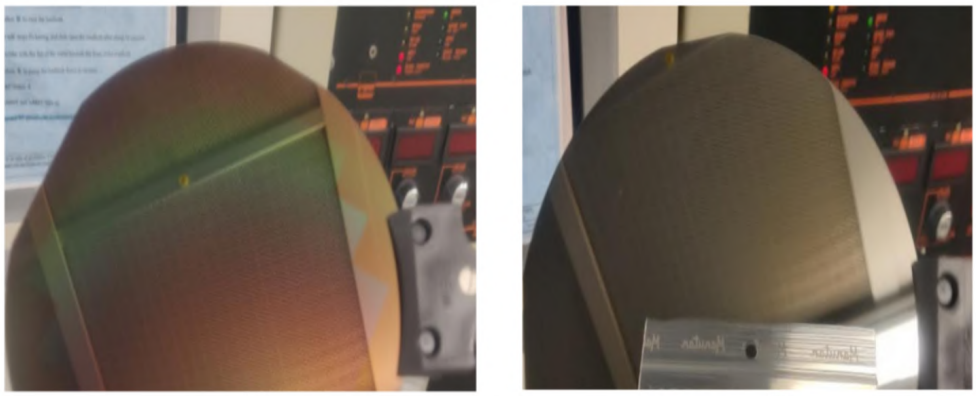


Figure 4.21: a) Before Al_2O_3 sputtering b) After Al_2O_3 sputtering

The sample was studied using the *Woollam M-2000UI ellipsometer* to determine what layer was deposited. The results did not match with any known layer. The layer seemed to be neither Al_2O_3 nor pure Al. Another test was conducted to try to etch this layer using the *Phosphoric acid Etching Solution (PES 77-19-04)*. The layer etched very slowly and it was found that after 10 minutes a black coloured border was formed on the edge of the wafer as shown in figure 4.22. Inspecting the sample using a microscope, it was also found that there were residues of the layer on the SiO_2 layer which looked like cracks.

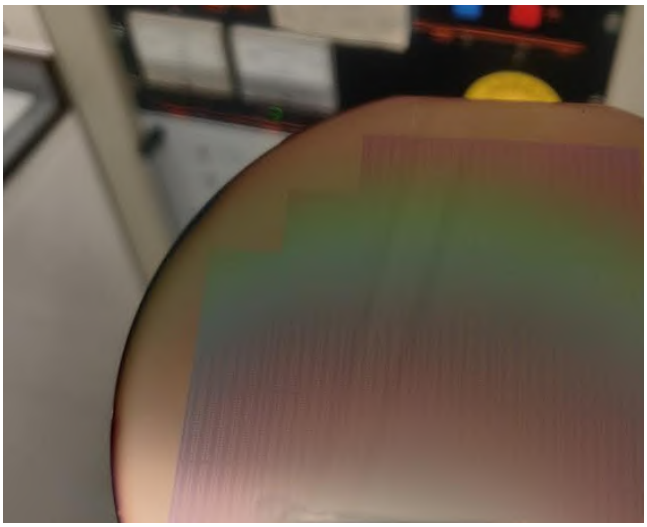


Figure 4.22: PES etch of the layer for 10min

Due to all these problems with the sputtering of Al_2O_3 and in view of time, it was decided to find an alternative way to deposit the layer. A decision was made to use the *CHA Solutions std.* to evaporate the Al_2O_3 together with the Fe layer and perform a lift-off instead. A $20nm$ Al_2O_3 + $2nm$ Fe layer was evaporated on a new sample and the results looked promising by visual inspection as shown figure 4.23. Lift-off was performed on the samples using NMP solvent and a hotplate at $70°C$. A $10 - 15min$ lift-off was sufficient to completely remove the negative photoresist.

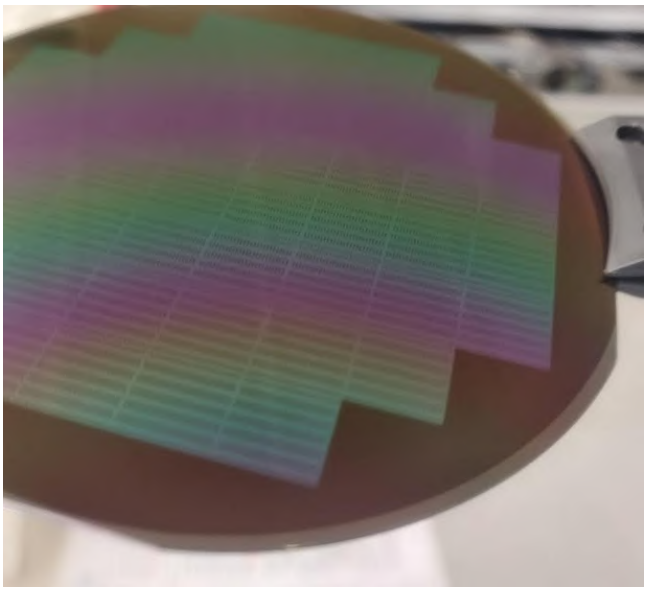


Figure 4.23: Sample with evaporated Al_2O_3 and Fe.

CNT forest growth

The CNTs were then grown using the *Aixtron Blackmagic*. The recipe involves an initial activation step in a H_2 environment at $500°C$ for $3\,min$, followed by the growth step in a H_2/C_2H_2 gas mixture of $700/50\,sccm$ respectively at $80\,mbar$ at $600°C$. The sample was cut into quarters to test different growth times and measure the height of the nanotubes. As a test, the 'bad' sample from the sputtered Al_2O_3 was also used to grow nanotubes.

The the CNTs grown on the sample from the sputtered Al_2O_3 is shown below in figure 4.24. The sample was observed using the *SEM Hitachi Regulus 8230* microscope. The growth time was $5\,min$ which gave an effective nanotube height $\approx 9.5\,\mu m$ which is quite low. It can be seen that there is almost no growth of nanotubes on the Al_2O_3 layer, except on the edges which created this 'well' like structure. It is clear that the layer was definitely not Al_2O_3 but an unusual mixture of AlO_X.

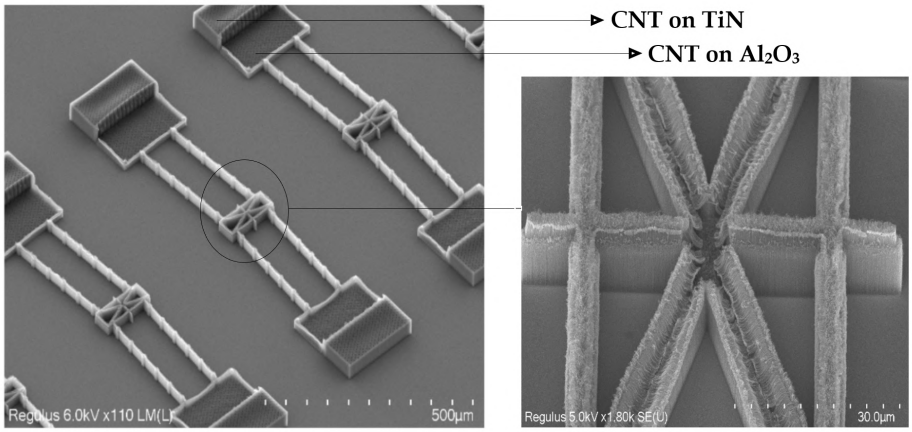


Figure 4.24: a) 45° tilt view of the structures b) CNT 'well' formed on the shuttle

The evaporated Al_2O_3 samples on the other hand showed promising results as shown below in figure 4.25. The growth time was 5 min which gave an effective nanotube height $\approx 96\,\mu m$.

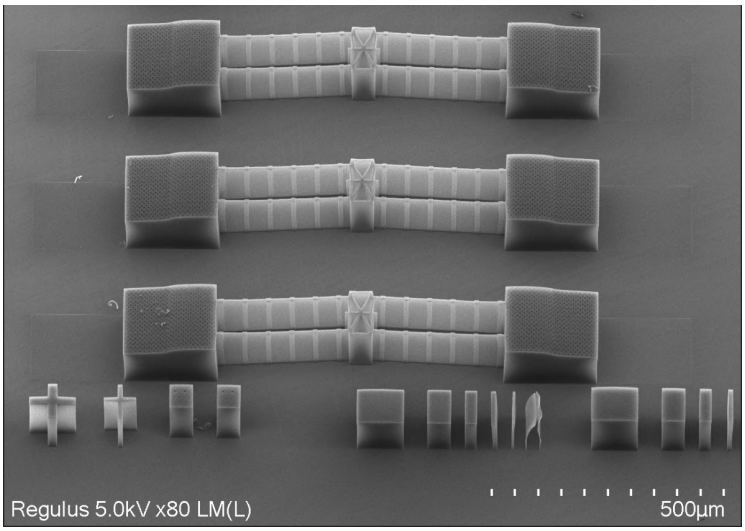


Figure 4.25: 45° tilt view of the structures

A number of growth times were tested to check the rate of CNT growth. The images of various growth heights are attached in Appendix D. The results obtained are tabulated below 4.1.

Table 4.1: CNT growth times and heights of various samples

Sample no.	Growth time (min)	Measured height (μm)	Actual height (μm)
1	1	23.8	33.65
2	2	43.2	61.09
3	3	51.1	72.26
4	5	68.1	96.3

It can be observed that the rate of CNT growth is around $0.5\,\mu m/s$ but gradually decreases for longer growth times. This is due to the depletion of nano-particles from the catalyst which would eventually stop the CNT growth [45]. Using the values obtained from the experiment, the CNT growth plot is shown below 4.26. Using the CNT growth rate obtained we can conclude that approximately 30 seconds of growth time is enough to obtain the target height required in this work.

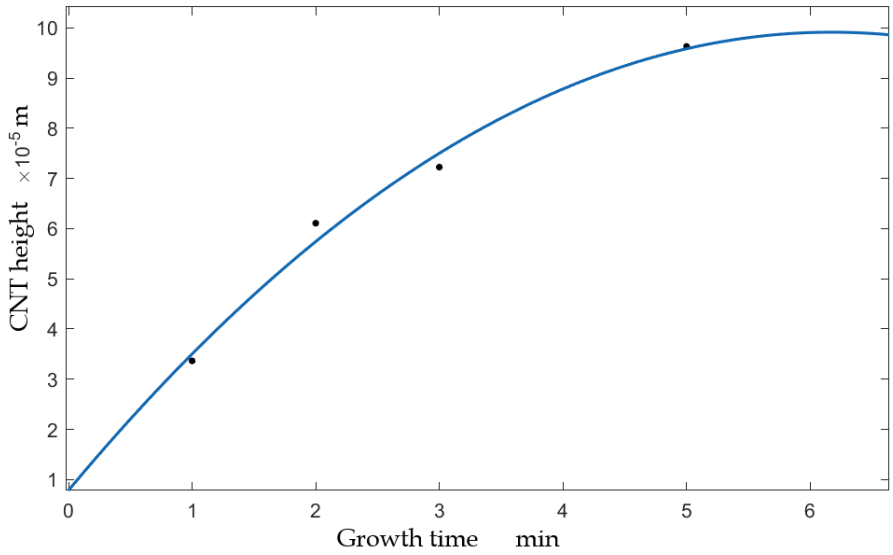


Figure 4.26: Growth time vs. CNT height

CNT forest filling

Due to technical issues with the *Tempress furnace* for LPCVD of SiC, the tool was unusable for a few months. Thus in view of time, a few other methods were tested such as PECVD of SiC and atomic layer deposition (ALD) of Al_2O_3 to check if they can be a viable replacement. We will first discuss the results of these two methods and later investigate the LPCVD technique.

PECVD of SiC

PECVD of SiC was performed using the *Novellus Concept1*. A carrier wafer was used and the sample was attached to this using Kapton tape. The sample after deposition is shown below in figure 4.27. The recipe used was $ls800nm\_2$ which uses a gas mixture of silane (SiH_4) and methane (CH_4) at a temperature of 400°C. A $5\,s$ deposition was performed to fill the nanotube forest with approximately $50\,nm$ of SiC.

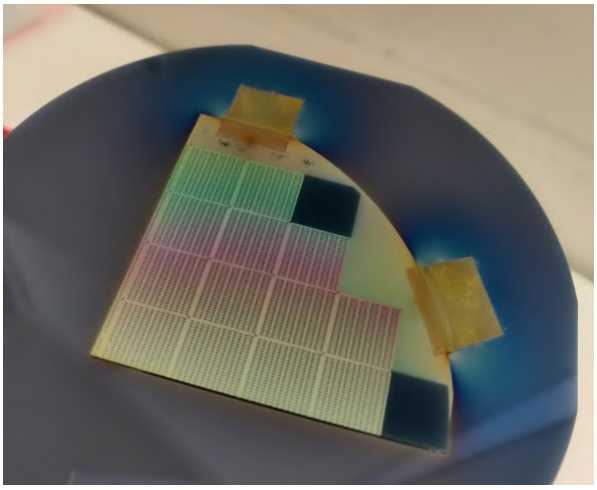


Figure 4.27: Sample with PECVD SiC

The samples were observed under a microscope and the results looked very promising at first glance. A 50 nm SiC deposition seemed to have completely filled the nanotube forest. The images obtained are shown below, figures 4.28, 4.29.

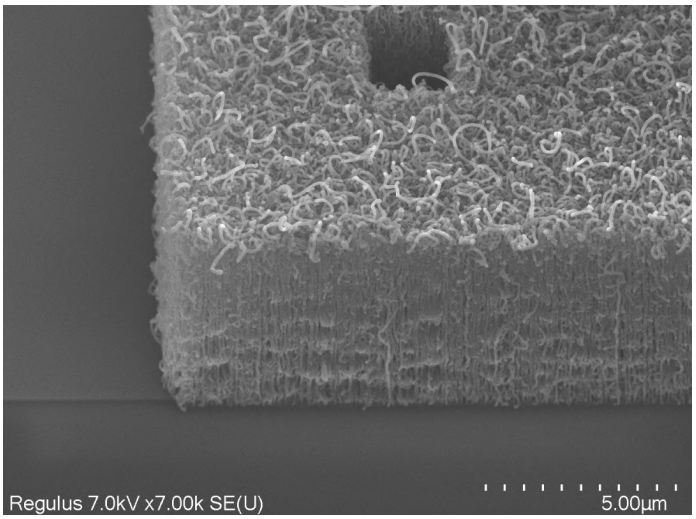
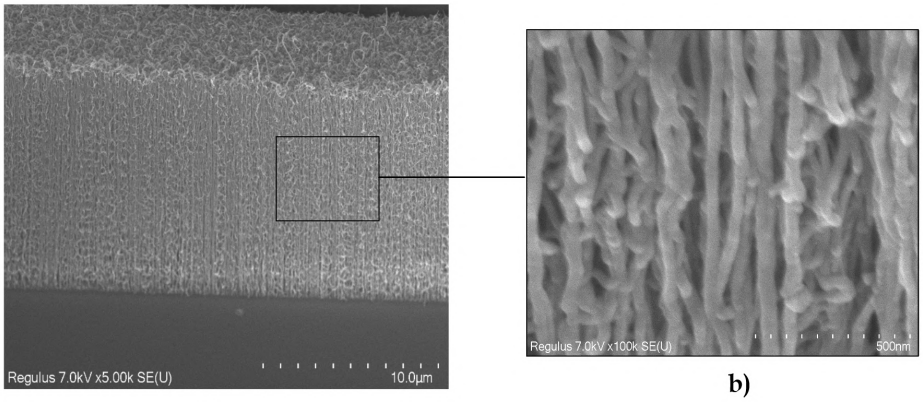


Figure 4.28: PECVD SiC coated structure observed at 30° tilt



a) **b)**

Figure 4.29: a) PECVD SiC coated bridge
b) Individual nanotubes coated with SiC

However, upon closer inspection it was found that the coated was only on the outer layer and had not penetrated into the forest. This was done by making small dissections on the structures using tweezers. Although this would destroy the structures, it helps us observe the inside of the structure. The images obtained are shown below in figure 4.30 with a few more attached in Appendix D.

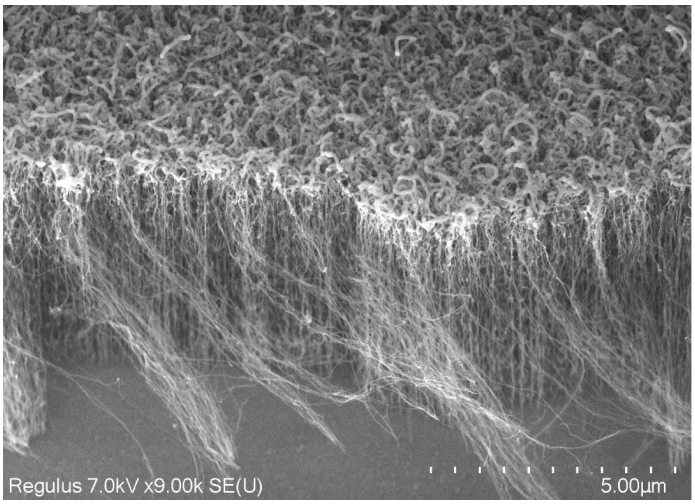


Figure 4.30: Dissected structure coated with PECVD SiC

The main reason for the coating not being conformal is the fact that PECVD is a very fast deposition at a comparatively higher pressure. In order to completely fill the nanotube forests, we require low pressure and slow rate of deposition as shown in the work by Fiorentino et al. [46]. This allows the gases to infiltrate the forest and conformally coat the structure. Thus, PECVD is not a good choice for CNT forest filling.

ALD of Al_2O_3

The ALD of Al_2O_3 was another option that was investigated as a filler material for the nanotube forest. Al_2O_3 is chosen as a filler material here due to similar properties compared to SiC such as superior hardness and large thermal conductivity ($25\,W\,m^{-1}\,K^{-1}$) [8]. A sample with CNT forests of height $\approx 34\,\mu m$, was sent to *Kavli NanoLab* to perform ALD using the tool *Oxford Instruments FlexAl*. Approximately, $20\,nm$ of Al_2O_3 was deposited on the sample. Preliminary observations on the scanning electron microscope (SEM) show that the deposition looks to be quite conformal as shown in figure 4.31. A few more images are attached in Appendix D.

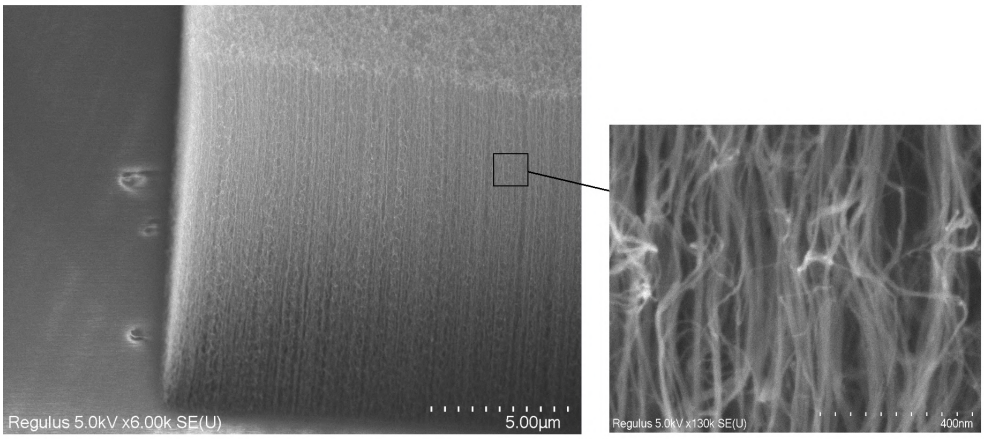


Figure 4.31: a) ALD of 20nm Al_2O_3 on CNT forest
b) Individual CNTs coated with Al_2O_3

However, dissecting the structure showed that the Al_2O_3 layer did not infiltrate the forest all the way through (figure 4.32). This affects the mechanical strength of the structure greatly as the base of the forest is just a nanotube bundle held by weak van der Waals' forces which are not mechanically strong. We could conclude that a $20\,nm$ deposition was not enough to completely fill the CNT forest of height $\approx 34\,\mu m$. In order to fill the forest completely we might require $50 - 100\,nm$ of Al_2O_3 based on current observations. This is not quite feasible since ALD is an extremely slow process which is generally used to deposit layers of a few nanometers.

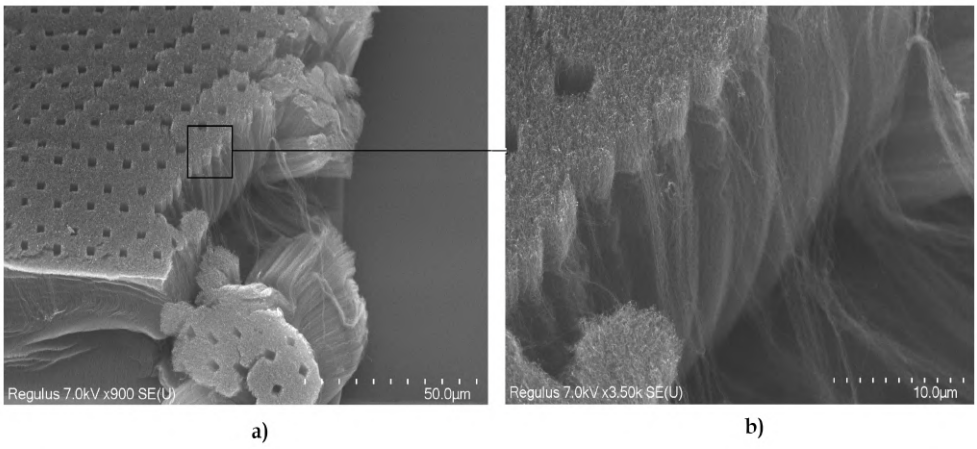


Figure 4.32: a) Dissected sample of CNT coated with ALD Al_2O_3
b) Non-conformality observed as the Al_2O_3 could not infiltrate the CNT forest

LPCVD of SiC

After having exhausted both our alternatives for CNT coating, we decided to go with the standard LPCVD coating of amorphous SiC once the tool became available again. This technique has previously shown very good results and conformal coating due to its controlled deposition. This has been demonstrated in the work by Rene Poelma et al.[47]. The *Tempress furnace (F3)* was used with the recipe *1st_SiC*. The recipe involves using dichlorosilane (SiH_2Cl_2) and acetylene (C_2H_2) gas mixture diluted with 5% hydrogen (H_2) at $760°C$ and $1\,mbar$. The flow rates are set to $65\,sccm$ for SiH_2Cl_2 and $435\,sccm$ for C_2H_2 which gives a gas flow ratio (GFR) of 3.

The deposition rate was found to be around $0.25\,nm/min$ based on previous depositions. As a preliminary test, $20.4\,nm$ of a-SiC was deposited on a quarter sample with a carrier wafer. The thickness deposited was measured using the carrier wafer on the *Woollam M-2000UI ellipsometer*. The spectra was observed at 5 different angles from $55°$ to $75°$ in the range $600 - 1250\,nm$ on a *cauchy* layer to obtain an MSE of < 50. The results obtained are shown below in figure 4.33. The coating seems to be conformal forming a stiff block.

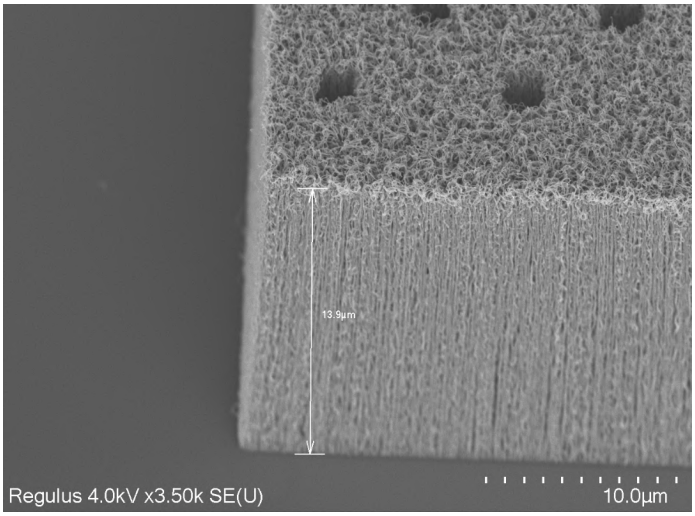
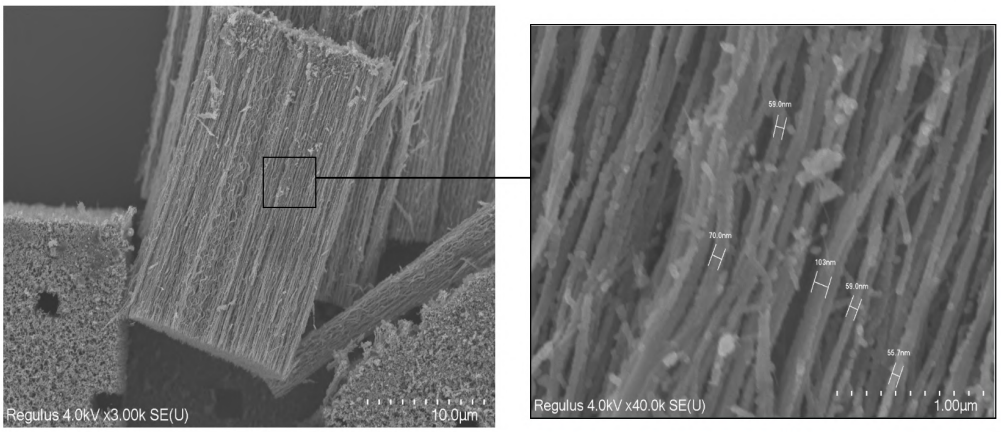


Figure 4.33: LPCVD a-SiC on CNT forest at 30° tilt

In order to observe the infiltration, the block was dissected using tweezers. Dissecting the structure proved to be slightly more difficult compared to the other tests done with the other filler materials. This agrees with the excellent mechanical properties of SiC [1]. It required a bit of force to obtain a clean cross-section as shown below in figure 4.34. It can be seen that the filler material has infiltrated all the way through to the bottom of the forest. The coated nanotube diameter varies from $50\,nm$ all the way to $100\,nm$ near junctions. A few more images are attached in Appendix D.



a) b)

Figure 4.34: a) Cross-section of LPCVD a-SiC on CNT forest
b) Individual nanotubes coated by a-SiC

Although the results obtained in this test are quite promising, it can be observed that voids still exist in-between the nanotube bundles. This would affect the mechanical properties of the final structure. This problem can be solved by just using more filler material since a few extra nanometers would not have a significant affect on the floor layer etching step that is required after.

Floor layer etch

We now have samples with CNTs that are completely coated with SiC. It is important to note that while depositing SiC on the structures, we also deposit a layer over the SiO_2 underneath. This carbide layer acts as a mask to the oxide and needs to be etched away since it would be impossible to release the structure otherwise. Since we are depositing just a few tens of nanometers of SiC, the layer can be etched away using RIE.

The first test to etch away the floor layer was performed using the *Adixen AMS110* plasma etcher. The recipe uses a mixture of Sulfur hexafluoride (SF_6) and Oxygen (O_2) at 200 $sccm$ and 20 $sccm$ respectively at a pressure of 14 μbar, 2000 W RF power (source) and 200 W RF power (chuck). The work by P. H. Yih et al [48] gives an approximate etch rate of the gas mixture on amorphous SiC. A 5 s etch would be sufficient to completely etch the approximately 40 nm of SiC. However, it is important to note that SF_6 also attacks the TiN. Thus, an overetch could completely remove the TiN pads. The result obtained before and after the RIE is shown below in figure 4.35. A few more results are attached in Appendix D where various recipe parameters were changed and tested.

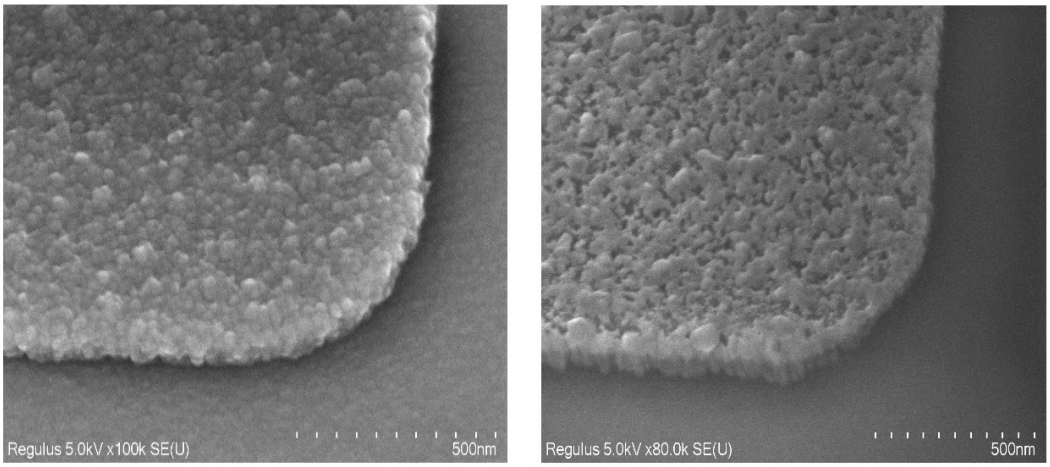


Figure 4.35: a) TiN pad coated with SiC before RIE
b) TiN pad after RIE in AMS110 for 5 *s*

It can be observed that most of the SiC over the oxide layer has been etched away without damaging the TiN layer too much. In fact, there are still residues of carbide on the pads. Increasing the etch time would be an obvious solution to completely remove the carbide, but it was observed that the recipe used in the AMS110 is quite aggressive on the CNTs. This was tested using one of the miscellaneous test structures of the main device (CNT growth test 4.1.3). The figure 4.36 shows that just a 5 *s* RIE has etched away approximately 8 μm of nanotubes, which is undesirable.

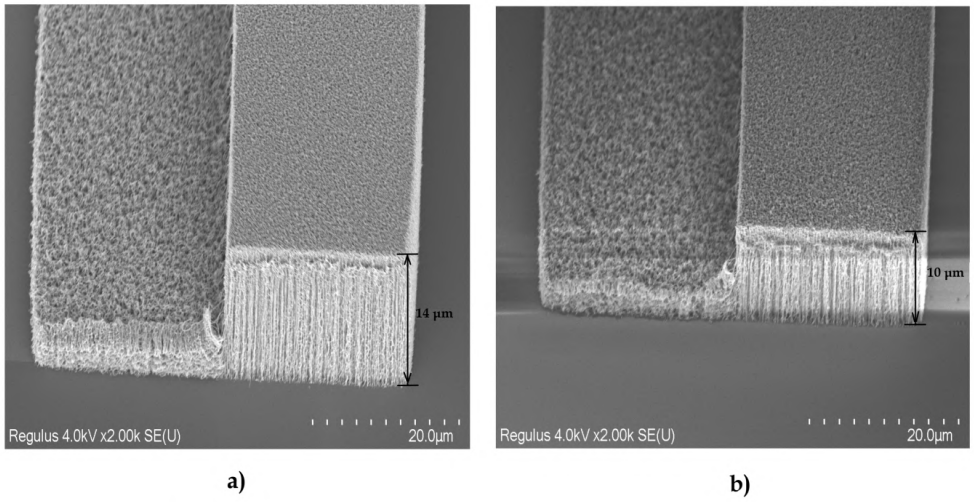


Figure 4.36: a) CNT height before RIE of SiC in AMS110
b) CNT height after RIE of SiC in AMS110
Tilt = 30°

A decision was made to use the *Sentech Etchlab 200* plasma etcher at *Kavli Nanolab*. This is a more mild etcher which could etch away the SiC without affecting the nanotube height too much. The recipe uses the gas mixture, 13.5 *sccm* of SF_6 and 3.5 *sccm* of O_2 at 8 μbar pressure and 50 *W* RF power. The recipe was tested on an actuator sample coated with 28.5 *nm* of SiC. A 90 *s* etch time was sufficient to remove all the SiC over the oxide layer. However, it was observed that a *shadowing* effect occurs due to the structures being too high. This can be seen below in figure

4.37. The carbide layer close to the edge of the base has not been etched away due to being shadowed by the nearby tall structure.

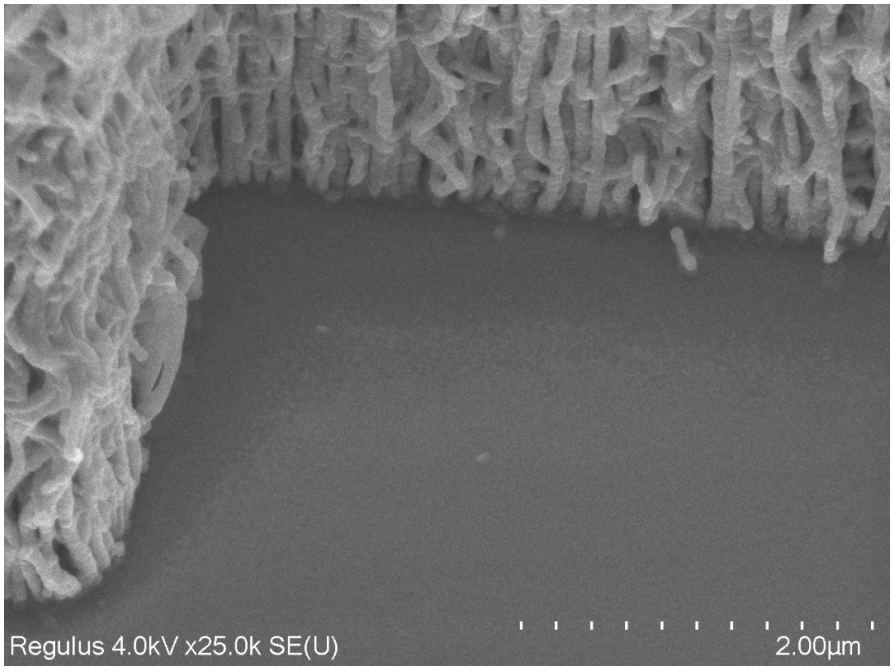
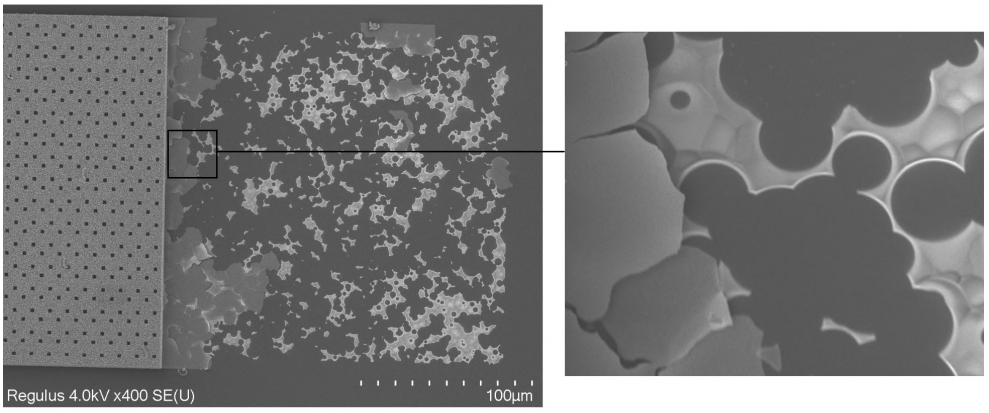


Figure 4.37: SiC residues near the base due to shadowing effect

The residues near the base don't really pose too much of a threat to proper release since we are sufficiently over-etching the oxide underneath the structure. The shadowing can also be prevented by either reducing the height of the structure or by performing multiple etches by tilting the sample a few different ways.

Release of the structure

In order to release the structure, the thermal oxide layer underneath has to be removed. This would make the entire structure free-standing that are anchored by the TiN pad. There are two ways to etch the oxide layer isotropically, the first method involves using buffered oxide etch (BOE) solution. The results obtained are shown below in figure 4.38.



a) **b)**

Figure 4.38: a) TiN pad after BOE
b) TiN peeling off due to corrosion

Wet etching to release a structure also has the inherent problem of striction[2]. Since BOE completely etched away the TiN pads, a decision was made to use Vapour HF (VHF) instead. This is also known to be quite aggressive on TiN. A mild recipe which uses a gas mixture of 310 *sccm* of HF, 350 *sccm* of Ethanol (EtOH) and 1250 *sccm* of Nitrogen gas (N_2) at 125 *torr* pressure was used. The results obtained are shown below in figure 4.39.

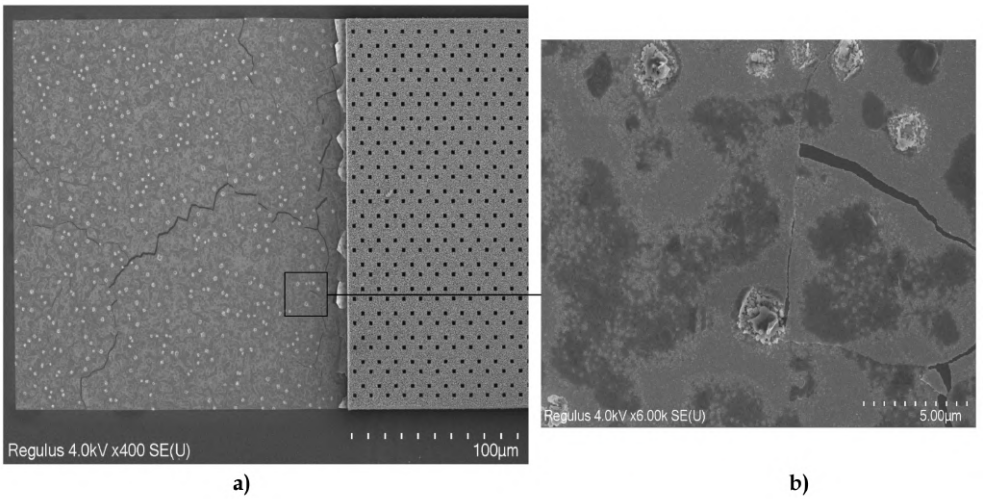


Figure 4.39: a) TiN pad after VHF
b) Cracks formed on the pad due to corrosion

The TiN pad still seemed to be severely damaged from the VHF. Cracks as seen above could lead to improper electrical contact. The release of the remaining structure, however, looked very promising as shown in figure 4.40.

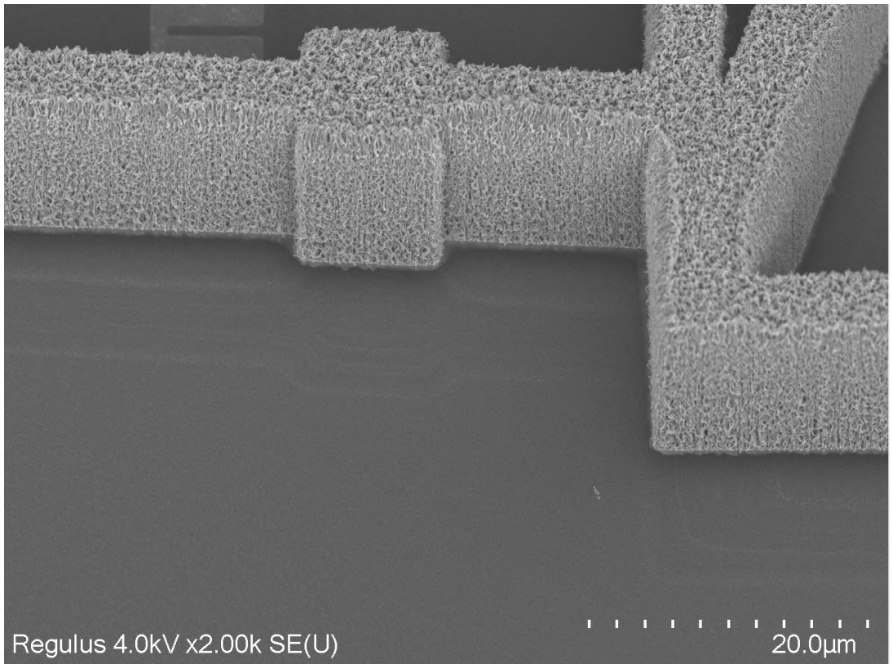


Figure 4.40: Actuator bridge free-standing after release

2 Sticking of the structure to the substrate due to the surface tension of the wet etchants.

A few more images from the release tests are attached in Appendix D. The VHF method for release seems to be much better than the BOE for our structures. The corrosion of the TiN is still a problem that has to be solved. One way of dealing with this would be to use an extra layer to protect the TiN pads before release.

4.2.2 Fabrication of the accelerometer

We have successfully tested out the critical steps in our process and have made a few changes to our process flow. This is depicted below in figure 4.41. The flowchart of the process is attached in Appendix E. In this section we will discuss the changes made in detail and the observations made while fabricating the CNT based accelerometer.

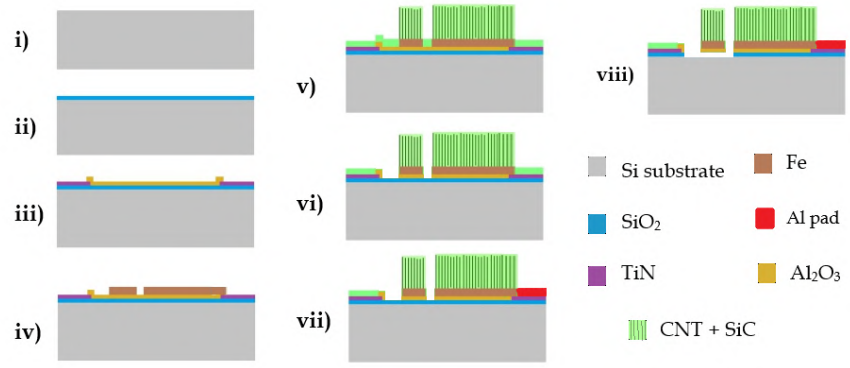


Figure 4.41: Final process flow
i, ii) Si substrate with SiO_2
iii, iv) Patterned TiN, Al_2O_3 and Fe
v) Filler material deposition
vi) Floor layer removal over oxide only
vii) Al pads for wire-bonding
viii) Release of the structure

Observations of critical process steps :

The CNT growth step encountered a few problems during processing. We have seen that the growth rate for the actuator samples was around $0.5\,\mu m/s$. Knowing this, a $30\,s$ growth was tested on a small sample. It was found that we had overshot our target height by $10-15\,\mu m$. This caused the spring and the fingers to bend as shown below in figure 4.42.

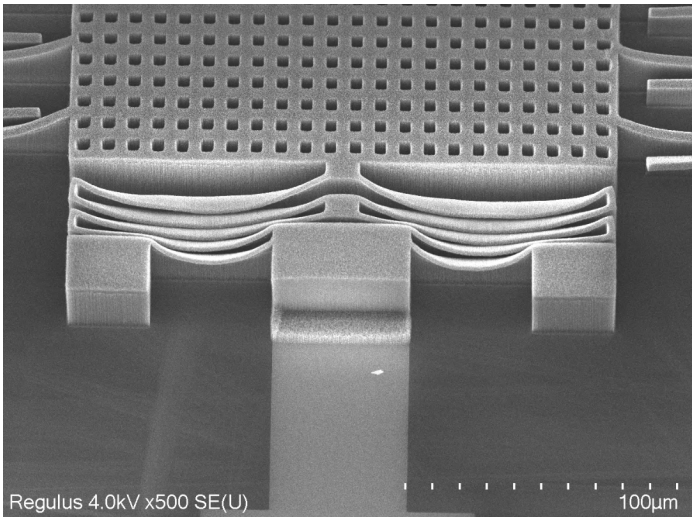
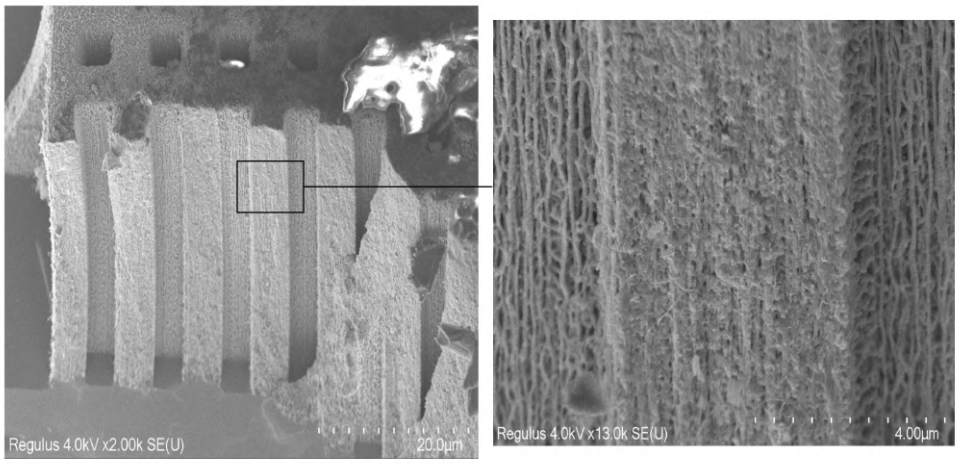


Figure 4.42: CNT growth time = $30\,s$
CNT height = $25\,\mu m$
Bending of the spring due to excess height

There are a few different reasons as to why this occurred, the main reason being the fact that the growth of nanotubes depends on the geometry of the structures [49]. Thus the growth times for the actuator sample could not be translated over for the accelerometer. The growth times were adjusted and nanotubes were grown with heights ranging from $8-12\,\mu m$ on a few accelerometer samples.

A test sample was first coated with around $40\,nm$ of SiC. Figure 4.43 shows a dissected sample coated with amorphous SiC. We can see that there are tiny voids in-between the nanotubes due to the nature of the deposition [7].



a) **b)**

Figure 4.43: a) Dissected sample of CNT accelerometer
b) Voids formed after deposition

These voids could pose a threat to the functioning of our device as it affects the mechanical stability. Thus, our main samples were coated with a sufficiently high amount of SiC to ensure that nothing breaks. Figure 4.44 shows an accelerometer after coating around 90 *nm* of carbide. We can see that there are almost no voids. A few more images are attached in Appendix D.

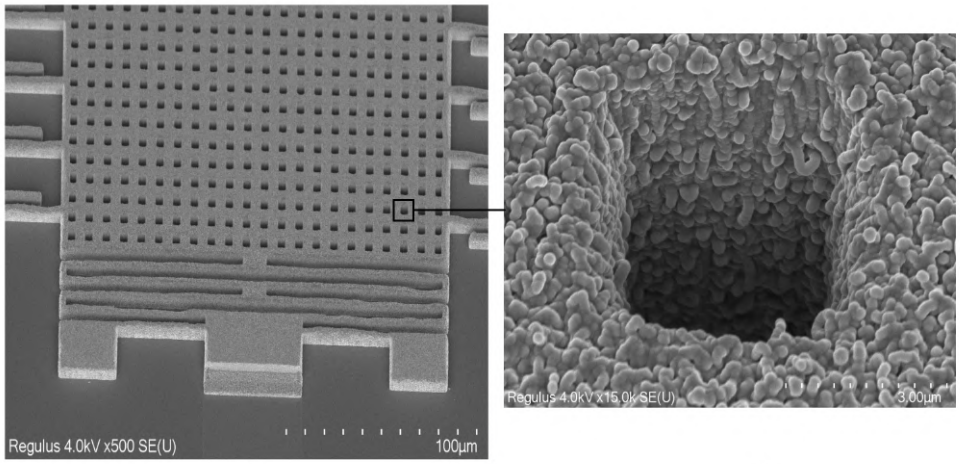


Figure 4.44: a) CNT based accelerometer coated with 90 *nm* a-SiC
b) Conformal coating with no voids

We now know that VHF release of the structure attacks the TiN quite significantly. A decision was made to protect the layer using an additional mask. Since the floor layer of SiC already exists at this point, we could pattern this above the TiN and etch away the remaining carbide over the oxide layer. In order to accomplish this, a new foil mask was designed as shown below in figure 4.45. This *protection* layer was intentionally made a few microns bigger than the underlying TiN to ensure that it completely blankets the layer, preventing any infiltration from the sides during release. The layer also has windows on the contact pad area to ensure electrical contact between the Al and the TiN layer.

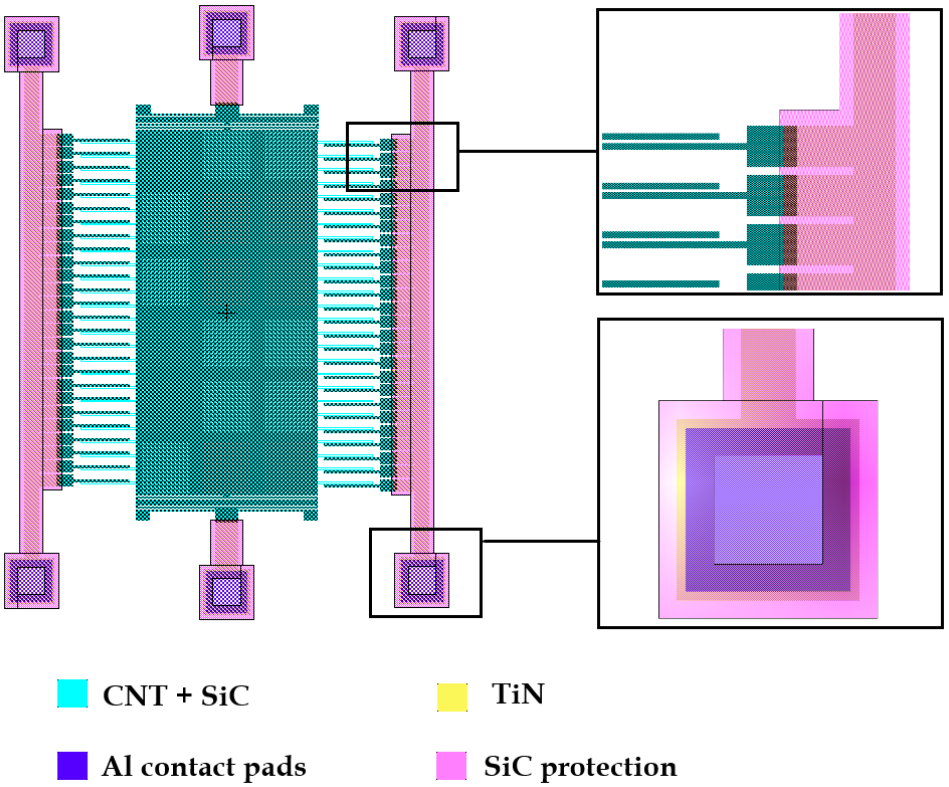


Figure 4.45: Top view of final mask after protection layer.

Since we have high aspect ratio structures on our wafer, the photoresist has to be spray coated. This is because spin coating would lead to uneven coating on the outer structures due to shielding from the inner ones. The spray coated samples of positive photoresist (*AZ9260*) were exposed with the new layer using the *SUSS Microtech MA/BA8 mask aligner* and developed using the *AZ-400K* developer. This patterned photoresist will now protect the TiN layer during floor layer etch. The results obtained after etching and stripping away the photoresist using acetone and Isopropyl alcohol (IPA) is shown below in figure 4.46.

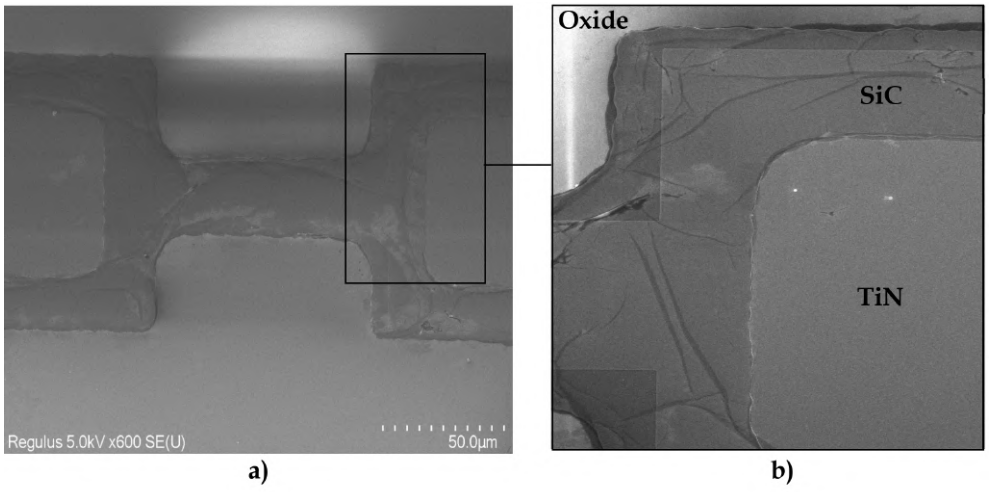


Figure 4.46: a) Contact pads after carbide protection
b) Close up view of SiC encapsulating the TiN pad

We now have our TiN layer protected and the structure ready for release. Since the TiN pad is not a very good wire-bondable material, another lithography step is needed to pattern an Al pad. The windows made on the SiC protection layer ensure proper contact between the TiN and the Al pad. First we sputter approximately $1\,\mu m$ of pure Al on our wafer. Positive photoresist (*AZ9260*) is spray coated on the wafer which is then exposed with the contact pad layer using the *ASML PAS 5500/80* wafer stepper and developed using the *AZ-400K* developer. The Al underneath is then etched using the *PES 77-19-04* at $35^{\circ}C$ and the resist is stripped away using acetone and IPA. The result obtained is attached below in figure 4.47.

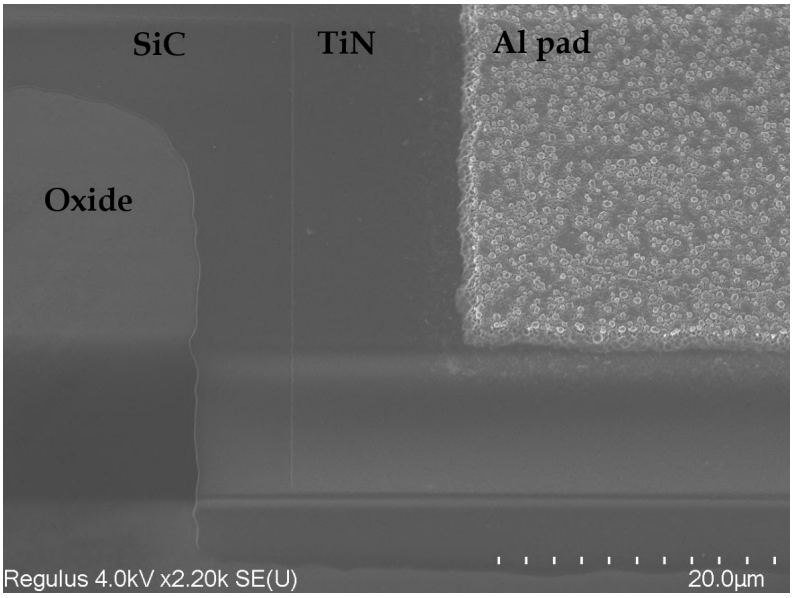


Figure 4.47: SiC protected TiN pad after patterning Aluminium

Finally, the structure was released using VHF using same mild recipe with gas mixture 310 *sccm* of HF, 350 *sccm* of EtOH and 1250 *sccm* of N_2 at 125 *torr* pressure. We can see from figure 4.48 that protecting the TiN layer is successful.

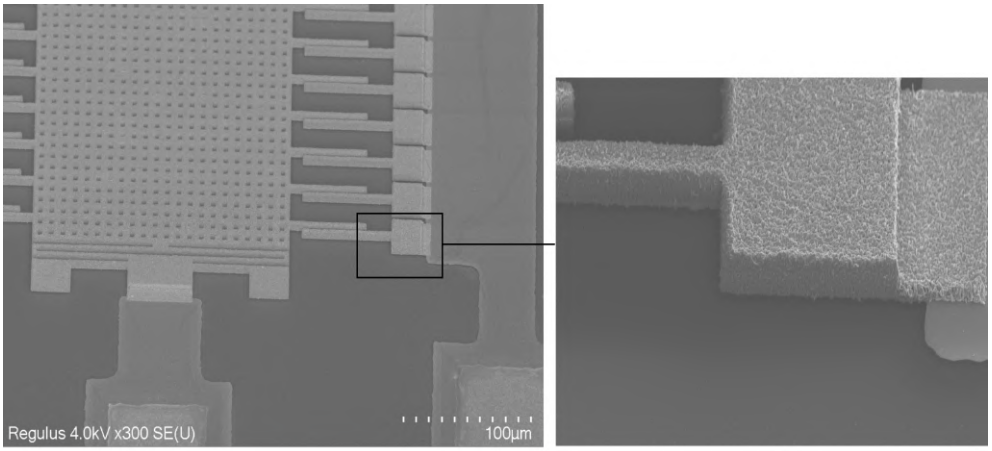


Figure 4.48: a) SiC protection after VHF release
b) Close up of the suspended electrode
CNT height $9\,\mu m$, Tilt 30°

The released structures now have to be diced and packaged. The dicing had to be done manually since using the dicing tool could dislodge our suspended structures.

The die is then packaged in a 40-pin Dual in-line package (DIP) as shown in the figure 4.49 below and wire-bonded. The device is now ready for testing.

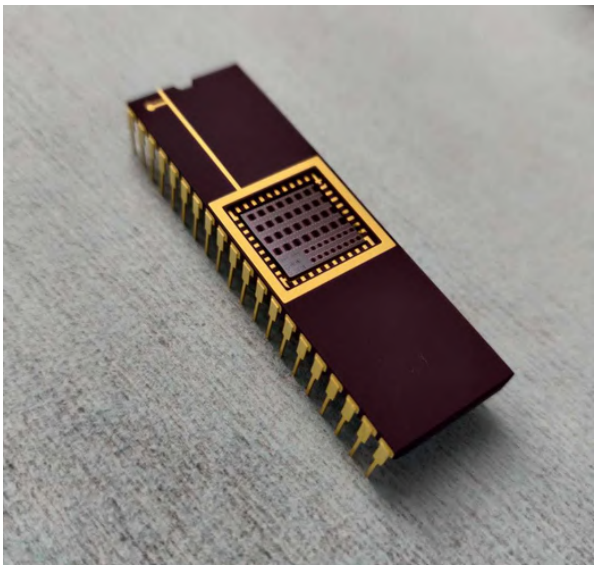


Figure 4.49: Final device packaged in a 40-pin DIP

4.3 CONCLUSION

In this chapter we have discussed the mask design and fabrication of our device. The mask design consisted of many electrical measurement and miscellaneous test structures. These help us determine various parameters of the nano-composite such as sheet resistance and resistivity. The following observations were made during the fabrication process :

- Having a thin TiN layer is crucial to ensure nanotube growth on the layer. A thicker layer would affect the ratio of Ti to N which could hinder the sustenance of the catalyst nano-particles.
- The amount of filler material deposited has to be quite low to ensure easy etch of the floor layer after. This also applies to the nanotube height since it can shield the floor layer underneath.
- Evaporation of Al_2O_3 show significantly better nanotube growth on the layer compared to sputtered Al_2O_3. This could be due to an uneven mixture of AlO_X being sputtered.
- Alternative methods for nanotube forest filling were tested using PECVD and ALD. It was found that PECVD cannot completely infiltrate the forest due to improper pressure and high rate of deposition. ALD is a relatively better option, but would require an extremely long deposition time which is quite impractical.
- The TiN layer must be protected by patterning the already existing floor layer. This will shield the layer during *Vapour HF* release later. Etching of the floor layer must be done with a very mild recipe to ensure that the nanotube height does not get depleted too much.
- Release of the structure by VHF is a better option compared to BOE since there is no issue of striction. The dicing has to be performed manually to prevent the suspended structures from dislodging.

5 DEVICE CHARACTERIZATION

In this chapter, we will study the performance of the device and characterize the electrical properties. We will first discuss the results obtained from the fabricated CNT - SiC thermal actuator in section 5.1. We will then extract the electrical parameters of the nanocomposite by measuring the TLM, VdP and ELM structures from our main sample. This is presented in section 5.2. This is followed by section 5.3 where the measurement setup for the accelerometer is discussed and the performance is tested. The conclusions and remarks are presented in section 5.4.

5.1 THERMAL ACTUATOR RESULTS

Using the work of Vadiraj A.M et al. [13], we successfully fabricated a CNT - SiC based thermal actuator. Although the design was used for process development, the final device fabricated was tested using the *Cascade Microtech* manual probe station. The TiN pads were damaged during VHF release but the bridge and the shuttle looked to be released correctly as shown below in figure 5.1. The device was probed by landing the probe needles directly on the nano-composite region of the pad.

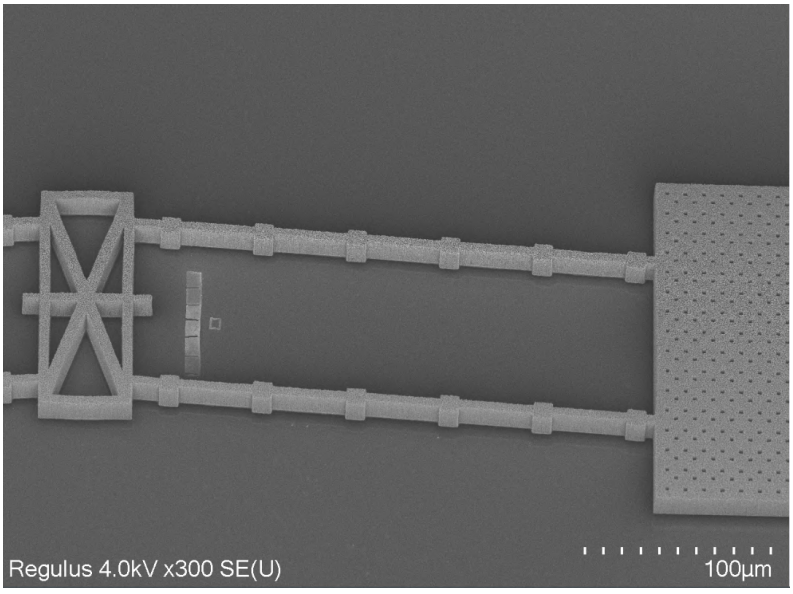


Figure 5.1: CNT - SiC thermal actuator
$6\,\mu m$ of oxide etched
Bridge and shuttle released

Due to the effect of Joule heating, applying a DC voltage across the actuator should cause the shuttle in the middle to deflect due to thermal expansion of the beams [50]. The test was first performed at room temperature, a pulsating DC voltage was applied across the actuator with an on time of $500\,ms$. The defection observed was approximately $6 \pm 1\,\mu m$ at $70\,V$ and $3.5\,mA$ current. This is depicted below in the figure 5.2.

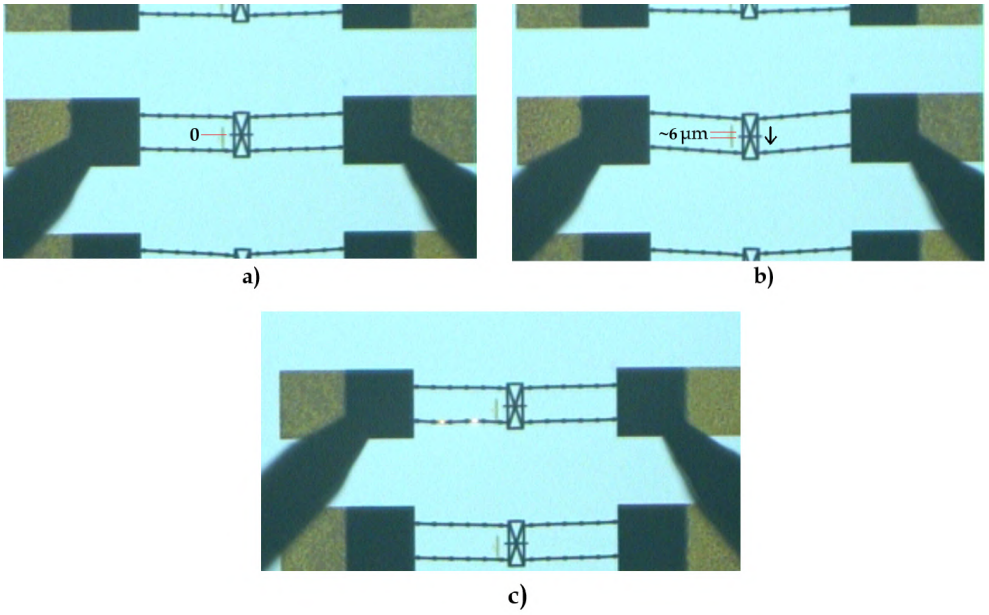


Figure 5.2: a) Initial position at $0\,V$
b) Final position at $70\,V$, $3.5\,mA$
c) Failure observed at $80\,V$, $4\,mA$

Using the deflection observed, we can calculate the average rise in temperature using the following equation [13] :

$$\mu = \frac{L\alpha\Delta T}{\omega} \tag{5.1}$$

$$\mu \approx \frac{\alpha P L^2}{3\kappa A\omega} \tag{5.2}$$

Where,
μ = Deflection = $6 \pm 1\,\mu m$ (experimental)
L = Length of the beam = $300\,\mu m$
α = Thermal expansion co-efficient of filler (a-SiC) = $3 * 10^{-6}\,K^{-1}$
ΔT = Average rise in temperature
ω = Pre-angle of the beams = $4^\circ = 0.069\,rad$
P = Power consumption of device $\approx 0.245W$
κ = Thermal conductivity of filler (a-SiC) = $130\,Wm^{-1}K^{-1}$ [51]
A = Cross-sectional area of beam = $1.5 * 10^{-10}m^2$

Since our device is quite small, the conduction through the beams is the primary mode of heat transfer [13]. Substituting the values in equation 5.1, we obtain an average rise in temperature $\Delta T = 460 \pm 76\,K$ for a deflection of $6\,\mu m$ observed during experimentation. This would mean that the final temperature of the beam during deflection is around $758 \pm 76\,K$ ($485 \pm 76^\circ C$).
Consider equation 5.2, the experimental deflection observed can be verified by substituting the values shown above. Doing so, we obtain a theoretical deflection $\mu_{theoretical} = 16.3\,\mu m$. The discrepancy in values could be due to non-uniform heating of the nanocomposite beams since the supporting structures created on the beams leads to a constantly changing cross-sectional area (A). Equation 5.2 also does not take the residual stress of the beam's material into account which can inhibit the maximum deflection.

A failure mode was also observed when the current was further increased to $4\,mA$ figure 5.2. We could observe hot spots forming on the bridge which led to its deformation and eventually its breakage. This could be due to imperfections in the CNT forest which leads to voids in the nanocomposite. An SEM image of the structure after breakage is shown in figure 5.3. We can still observe the hot spots on the nanocomposite beams. This charging observed during imaging could be due to secondary electrons being fired from the surface of the structure at a different rate. This would indicate that the composition of the beams has been altered which will require further investigation using energy dispersive X-ray spectroscopy (EDX). The close up image of the breakage show a few voids the joints that are uncoated by SiC, which could have been the weak link that led to failure.

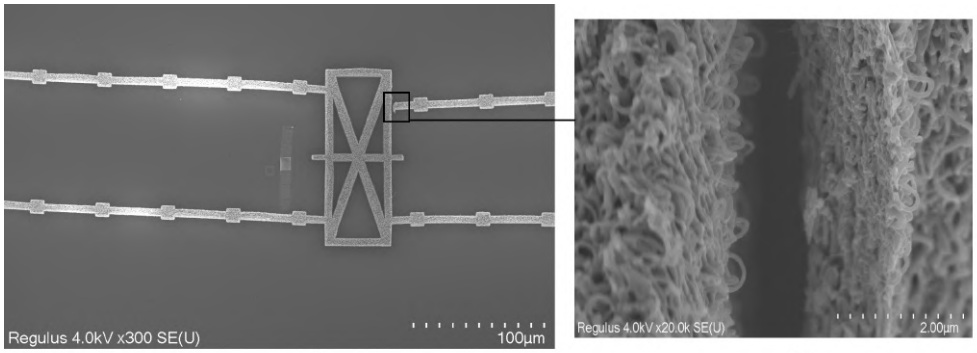


Figure 5.3: a) SEM image of the failure mode observed
b) Close up image of the broken beam

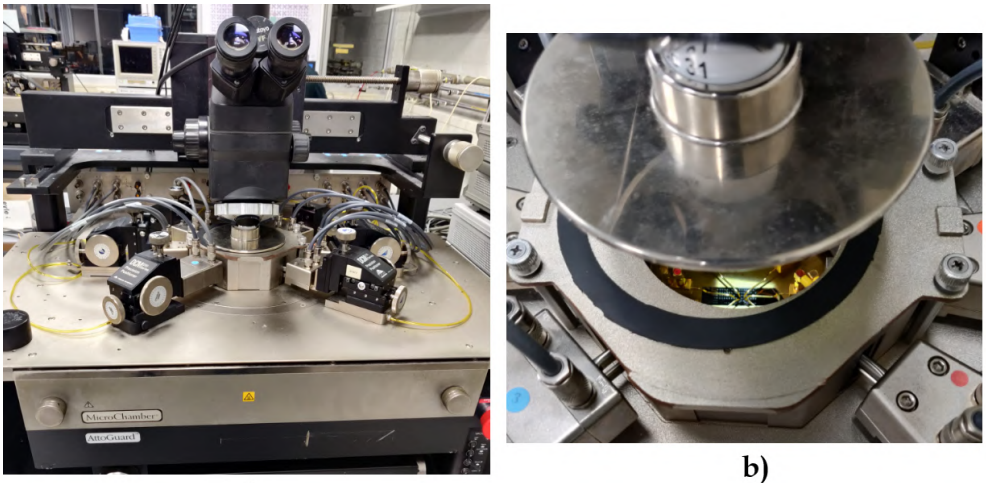
A temperature resilience test was also performed using the chuck heating function in the *Cascade* probe station. The results obtained are tabulated below. The device worked perfectly even at $200°C$ but the deflection observed was quite low. This could be due to the beams pre-deflecting during the heating process. Thus, there would not be enough slack in the beam to deflect further during experimentation.

Table 5.0 : Temperature testing of actuator

Test no.	Voltage, Current	Temperature ($°C$)	Deflection (μm)
1	70 V 3.5 mA	25	6
2	45 V 6 mA	100	1.5
3	40 V 6 mA	200	1

5.2 ELECTRICAL MEASUREMENTS

The electrical measurements on the main device were performed first after CNT growth step and again after the floor layer etching step. The measurement was performed using the *Cascade 33 Microtech* probe station as shown in figure 5.4. Using the *IC-CAP* software, a force current is swept from $-50\,\mu A$ to $+50\,\mu A$ while measuring the voltage across the pads. The results obtained are discussed below in the coming sections. More detailed data is attached in Appendix F.



a) b)

Figure 5.4: a) Cascade 33 Microtech manual probe station
b) Sample on the chuck with probe needles

5.2.1 VdP results

There are 3 variants of VdP structures with different widths used in this work. One main observation that was made during the VdP tests is that our structure does not meet the Van der Pauw criteria as discussed in section 4.1.2. When the thickness of our sample exceeds our selected widths ($5/10/20\,\mu m$), the resistance is not perfectly linear [52]. This can be observed in the following figure 5.5.

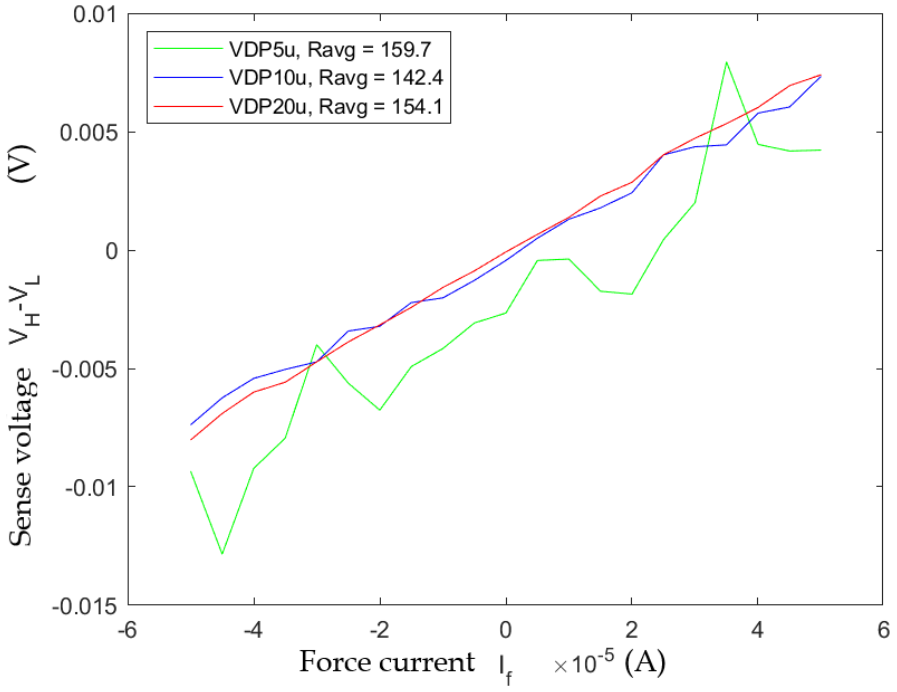


Figure 5.5: Sense voltage vs. force current
CNT height 10 μm
a-SiC thickness 90 nm

We can see that the average resistance measured on a VdP structure is independent of the width of the structure. However, only the 20 μm width structure shows a linear VI response. This is due to the fact that at that particular width, the VdP criteria is satisfied. A few more tests were performed, the results obtained are tabulated below in table 5.1.

Table 5.1 : VdP measurement results

Sample no.	CNT height (μm)	a-SiC thickness (nm)	R_{avg} (Ω)	$R_{\square}$ (Ω/sq)	Resistivity (ρ) ($\Omega.m$)
1	20	30	81.3	368.8	0.0073
2	50	-	27.9	126.4	0.0063
3	42	40	22.5	101.9	0.0042
4	10	-	195.7	886.9	0.0088
5	10	90	152	688.9	0.0068

The samples seem to show lesser resistivity after coating with SiC. This might be due to the increase in conductivity of the nanotubes during the LPCVD at 760°C in the furnace. The high temperature annealing leads to greater anisotropy in the nanotube forest which then increases its conductivity due to better tunneling [53]. These results can be compared with the other electrical structures for verification. In any case, it is clear that the CNTs dictate the electrical properties of the nanocomposite.

5.2.2 TLM results

The TLM measurements were performed on both left and right structures. The left TLM consisted of an Al_2O_3 layer inbetween the catalyst and the TiN. The right TLM structure had the catalyst directly on the TiN as shown previously in section 4.1.2. It was hypothesized that having the Al_2O_3 layer inbetween could show higher contact resistance.

The electrical measurements were performed using the *Cascade Microtech* probe station. A four point measurement was performed on both the structures for different lengths by sweeping a force current from $-50\,\mu A$ to $+50\,\mu A$ and measuring the voltage. The results obtained are shown below in figure 5.6.

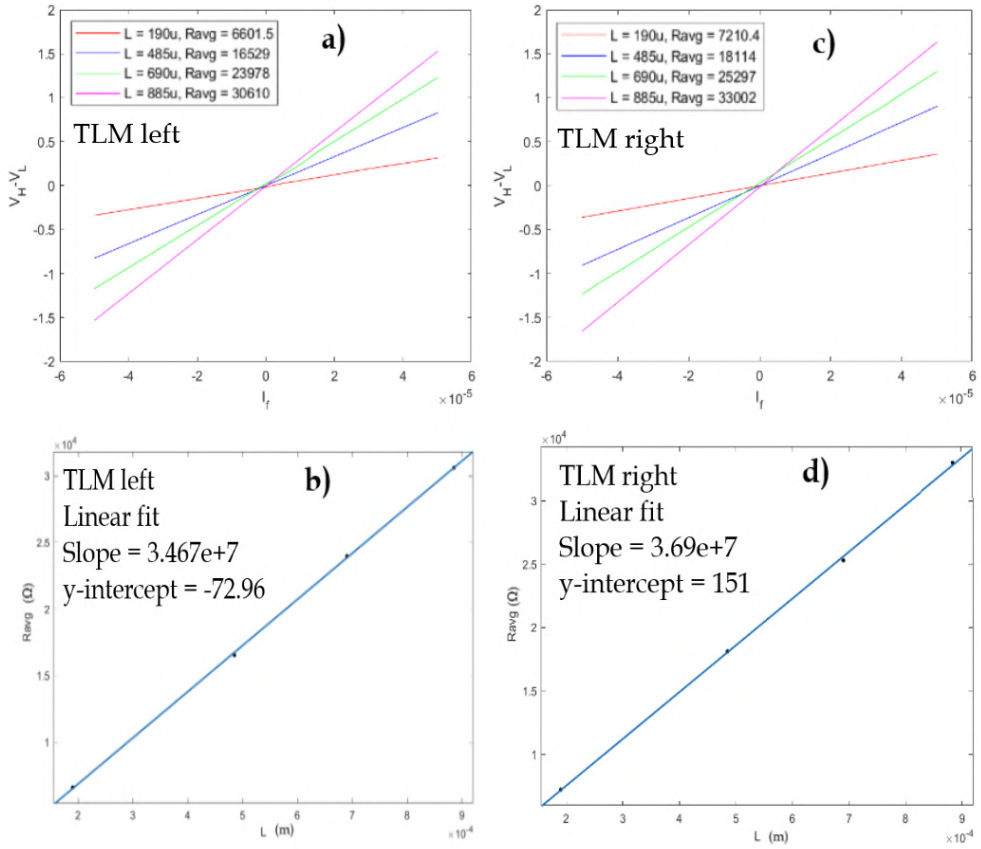


Figure 5.6: CNT height $10\,\mu m$, a-SiC $90\,nm$
a) TLM left VI plot
b) TLM left resistance vs length
c) TLM right VI plot
d) TLM right resistance vs length

It can be observed from plots (a) and (c) that the average resistance increases linearly with increase in length. This linearity can be verified by plotting the resistance obtained as a function of length. Using the slope and y-intercept from this plot, we can calculate the resistance per unit length and the contact resistance (R_C). This is tabulated below in table 5.2.

Table 5.2 : TLM left and right measurement results

Sample	CNT height (μm)	a-SiC thickness (nm)	TLM length (μm)	R_{avg} (Ω)	Resistance per unit length (Ω/m)	Contact resistance R_C (Ω)
TLM right	10	90	190 485 690 885	7210.4 18114 25297 33002	$3.69 * 10^7$	75.5
TLM left	10	90	190 485 690 885	6601.5 16529 23978 30610	$3.46 * 10^7$	-36.48

The resistance per unit length (slope) of both the TLM structures are approximately the same. Multiplying this value with the width of the structure ($20\,\mu m$) gives us the sheet resistance ($R_\square$). The sheet resistance calculated is as follows -

$$R_\square(TLM\ right) = slope * W = 3.69 * 10^7 * 20 * 10^{-6} = 738\ \Omega/sq \tag{5.3}$$

$$R_\square(TLM\ left) = slope * W = 3.46 * 10^7 * 20 * 10^{-6} = 692\ \Omega/sq \tag{5.4}$$

These values are comparable to the sheet resistance obtained from the VdP measurements. The contact resistance can be calculated using equation 4.3. An interesting observation was made, the contact resistance of the TLM left structure is a negative number. This could mean that the value is so low that the method used to calculate is not accurate enough to resolve it to the exact value. We can assume that the value is negligible compared to resistance per unit length.

Another observation made is that the right structure shows a higher R_C than the left. This goes against our initial hypothesis. This could mean that the Al_2O_3 layer inbetween does not play as significant as a role to R_C compared to the orientation of the CNTs. During fabrication it was observed that the CNTs grow differently on the left and right structures. On the left structure, it seems that the nanotubes grow along the edges on the overlap region and fall inside. Whereas, on the right structure the nanotubes just grow vertically upto a certain height and stop. Thus, the left structure has a few horizontal nanotubes at the top.

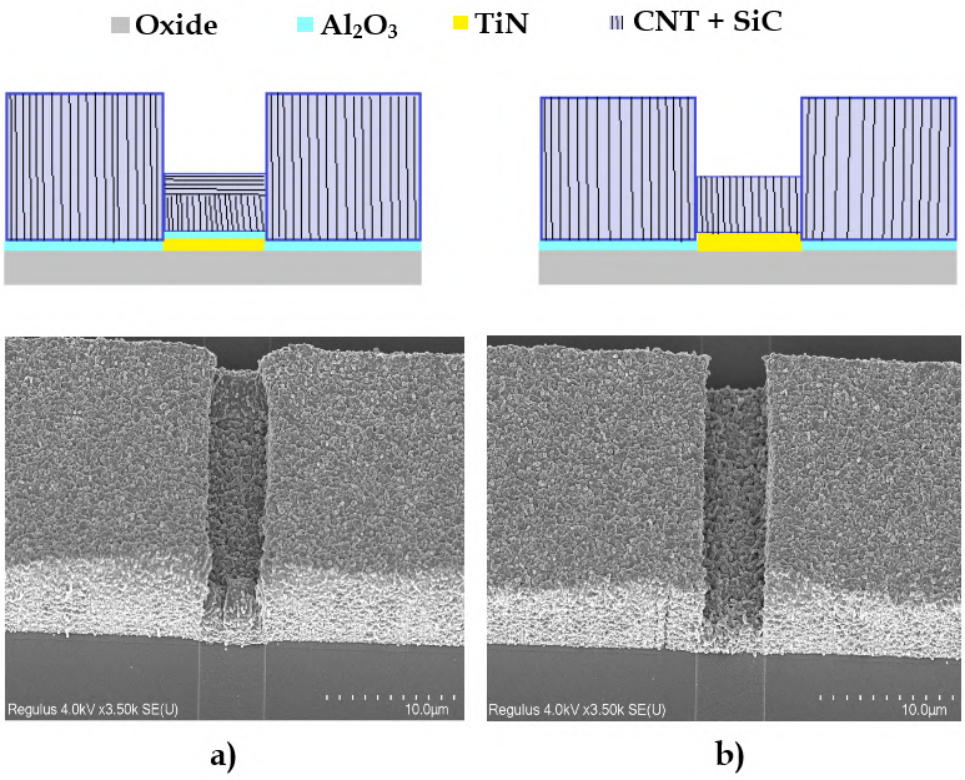


Figure 5.7: Cross section of TLM structures
a) TLM left CNT orientation and SEM image
b) TLM right CNT orientation and SEM image

It can be observed from figure 5.7 that both TLM structures have the same height of CNT forest above the TiN region. But the nanotubes in the left structure might be horizontally aligned on top due to bending. This could aid in better tunnelling of the electrons into the bulk of the nanocomposite and thus, leading to lower contact resistance. Another possibility is that the quality of CNTs grown over an Al_2O_3 layer is much better than the ones grown without. These high quality nanotubes could show better contact with the TiN layer.

5.2.3 ELM results

Similar to the VdP structures, we have 3 variants of ELM with different widths. The average resistance of the ELM structures are dependent on the dimensions according to the equation 4.1. A four probe measurement was performed as shown in figure 4.11 by sweeping a force current from $-50\,\mu A$ to $+50\,\mu A$ and measuring the voltage. The plot obtained is shown below in figure 5.8

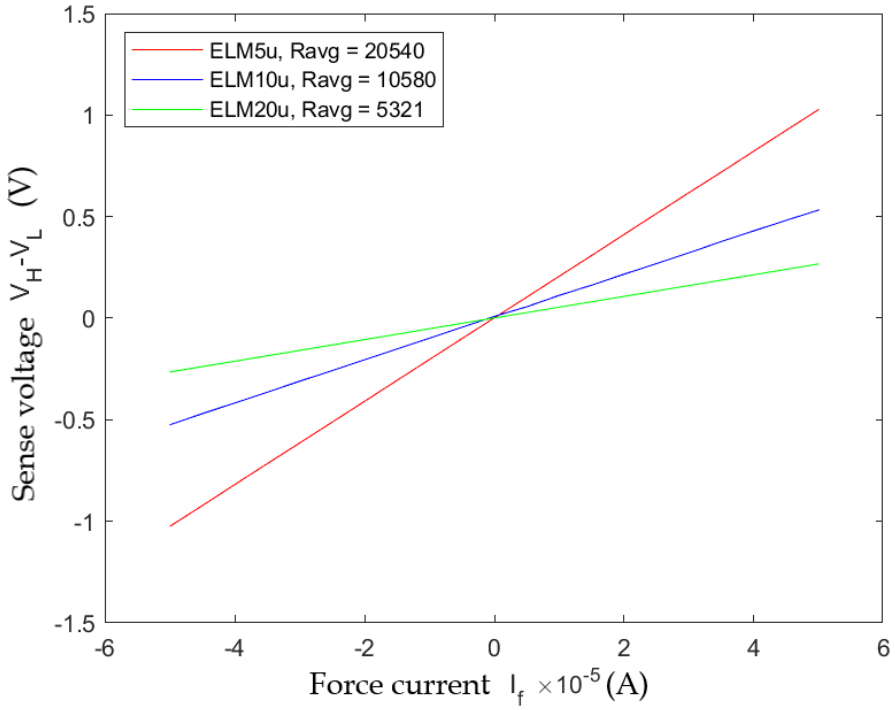


Figure 5.8: Sense voltage vs force current
CNT height $10\,\mu m$
a-SiC thickness $90\,nm$

Calculating the sheet resistance and resistivity, it was observed that the values do not quite match up with the results from the TLM and VdP structures. There currently is no definite reasoning as to why there is a difference in values. One explanation could be that the height of the nanotubes are not uniform throughout and the quality of the CNTs can vary between structures.

Table 5.3 : ELM measurement results

Sample no.	CNT height (μm)	a-SiC thickness (nm)	$R_\square$ (Ω/sq)	Resistivity (ρ) ($\Omega.m$)
1	20	30	189.08	0.0037
2	50	-	65.56	0.0032
3	42	40	72.66	0.003
4	10	-	598.77	0.0059
5	10	90	361.93	0.0036

The ELM structures were also used to calculate the Temperature co-efficient of resistance (TCR) of the nanocomposite. This was performed by using the chuck heating function on the *Cascade* probe station. The resistance (R_0) was measured at room temperature (21°C) followed by measurements at three different temperatures (100/150/200°C). The detailed results can be found in appendix F.3. The plot of resistance measured to temperature is depicted below in figure 5.9. The slope of this plot gives us the TCR.

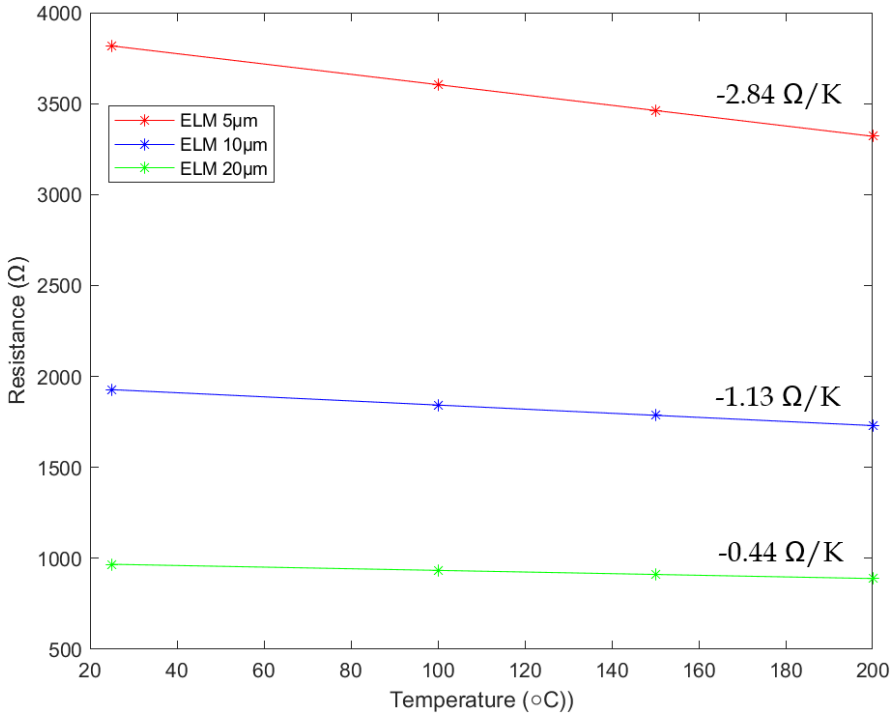


Figure 5.9: Plot of Resistance vs temperature for different ELM widths CNT height 42 μm, a-SiC 40 nm

We can see that the nanocomposite exhibits a negative TCR. As mentioned earlier, increasing temperature leads to better tunneling of the electrons through the nanotube forest [53]. Thus, increasing temperature leads to a decrease in resistance. The TCR is generally represented in parts per million per Kelvin. This can be calculated by dividing the obtained slope by the resistance at room temperature (R_0) as shown in table 5.4.

Table 5.4 : TCR measurement results

ELM width (μm)	R_0 (Ω)	TCR	
		Ω/K	ppm/K
5	3834	-2.84	-0.00074
10	1939	-1.13	-0.00058
20	973.6	-0.44	-0.00045

5.3 ACCELEROMETER RESULTS

The CNT - SiC capacitive accelerometer can now be tested for performance. One sample was chosen for the measurement of static capacitance to check if the fixed and movable fingers act as the parallel plates of a capacitor in section 5.3.1. Another sample was chosen before packaging to test its resilience to high temperatures. This is discussed in section 5.3.2. The theory for measurement of a capacitance change and the setup will be discussed in section 5.3.3.

5.3.1 Rest capacitance measurement

The rest capacitance as discussed in section 2.1.1 is the capacitance measured across the fixed and moving fingers when there is no acceleration applied. This can be calculated using equation 2.5. For our device, we have large structures with proof mass $800 * 400\,\mu m$ and small structures with proof mass $400 * 200\,\mu m$; where, $\epsilon = 8.85 * 10^{-12}\,F/m$, $N_f = 26$ *or* 13, $L_f = 105$ *or* $50\,\mu m$, $h = 10\,\mu m$, $d = 2$ *or* $3\,\mu m$. The capacitance-voltage (CV) measurements were performed using the *Cascade Microtech* probe station with the *Keysight 4284A LCR meter*. The results obtained are shown below in figure 5.10.

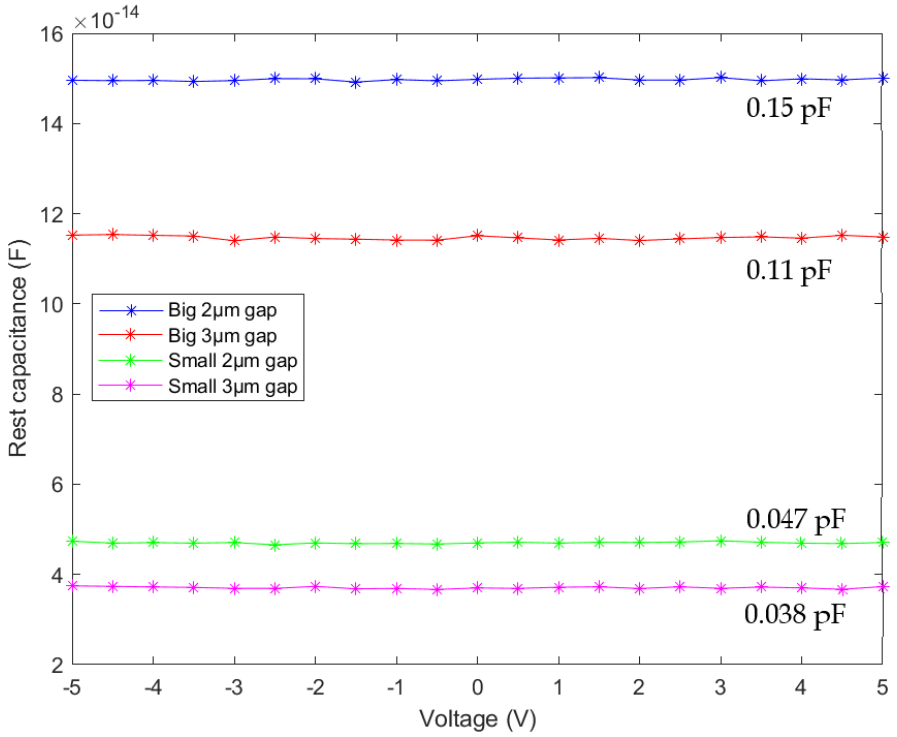


Figure 5.10: Plot of rest capacitance to voltage of different accelerometer variants

It was observed that for a finger gap of $2\,\mu m$, the rest capacitance varies quite a bit from device to device. There was also a difference in capacitance from the left and right side of the same accelerometer. This could be due to bending of the fingers during release. The slight discrepancy from the theoretical and practical capacitance values are due to the fact that the finger gap and height can vary depending of the alignment of the CNT forest. The bending of the forest can also cause a short if the fixed and moving fingers touch each other. This was observed during measurement when a few structures showed a negative capacitance[1].

1 Showing and inductive behaviour which means that the fingers are shorted.

Table 5.5 : CV measurement results for rest capacitance

Sample type	Finger gap (μm)	C_0 theoretical (pF)	C_0 experimental (pF)
Large structures	2	0.12	0.15 ± 0.05
	3	0.08	0.11
Small structures	2	0.028	0.04 ± 0.01
	3	0.019	0.03

5.3.2 Temperature testing

The high temperature resilience testing was performed using the *Nextron Microprobe station*. The sample was heated from room temperature to $700°C$ in steps of $100°C$ at $10\,min$ intervals. The detailed images are attached in appendix F.4.

The device did not breakdown even at $700°C$ but at temperatures above $600°C$, the Al pads did being to melt. In order to investigate further, SEM imaging was performed on the heated sample and compared to a reference sample. This is shown below in figure 5.11.

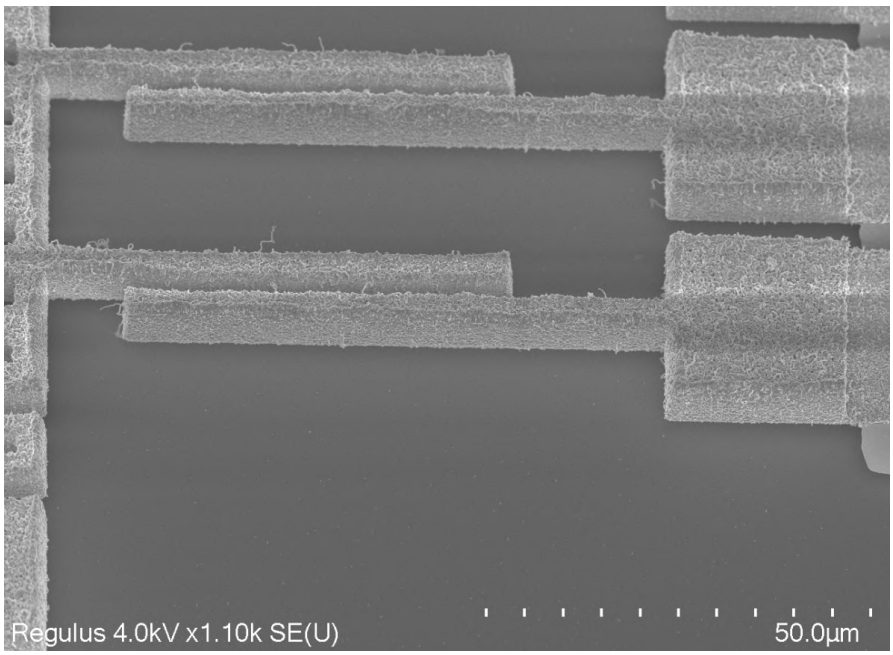


Figure 5.11: Final sample after $700°C$ heating
CNT height $10\,\mu m$, a-SiC $90\,nm$
Tilt $30°$

We can observe that the overall structure remains unaffected from the high temperature. Since the TiN layer is blanketed by SiC, the layer is protected. This is a testament to the superior propeties of SiC. However, we do observe a few coated CNTs sticking out of the structure. Since the device was heated to temperatures greater than 600°C (the growth temperature of CNTs), a few catalyst nano-particles might have been re-activated leading to a few extra nanometers of growth [54]. These stray nanotubes in-between the fingers could lead to a short and thus, failure of the device. This was verified by performing another CV measurement on the sample. The melted contact pads and the stray nanotubes possibly causing as short, made the measurement quite difficult and showed low negative capacitance on almost every structure.

5.3.3 Measurement plan

There are many different ways to test an accelerometer performance using various readout circuits. An ac-bridge with a voltage amplifier, switched capacitor circuit, transimpedance amplifier and many other methods have been tested on micro-g accelerometers previously [55]. Since we a focused on a proof of concept, a simple capacitance to voltage convertors (CVC) [14] technique can be used to test the performance of our device since it has good stability and low noise.

Figure 5.12 shows the readout circuit for the testing of our device. An AC signal from a signal generator is fed to a differential amplifier to obtain a differential signal. This differential signal has the same amplitude but opposite phase. The resistors R1 and R2 are used for common mode rejection. The output voltage of a half bridge can be represented by equation 5.5 [56]-

$$V_{out} = \frac{\Delta C}{2C_0} V_{in} \tag{5.5}$$

We can see that any acceleration leads to a change in capacitance (ΔC) which causes a linear change in output voltage (V_{out}). It is advised to use a sufficiently high frequency input voltage to filter out the noise better. The signal is amplified by a simple inverting amplifier and displayed using an oscilloscope.

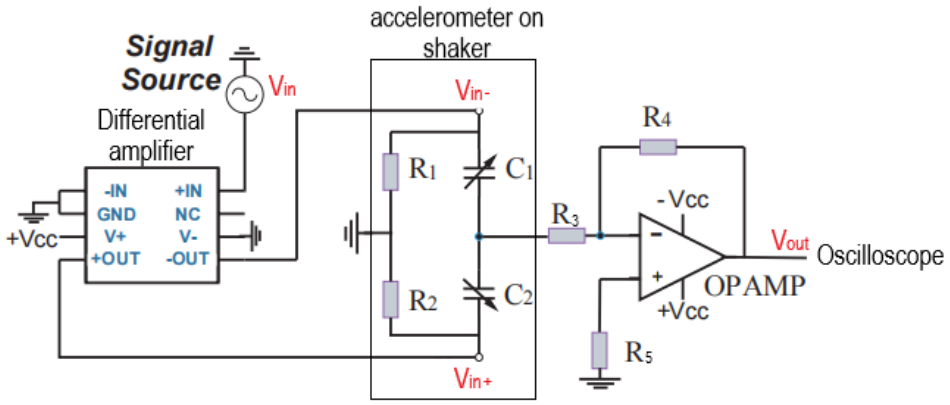


Figure 5.12: Differential CVC technique schematic [14]

The measurement will be carried out using the *LDS V406 permanent magnet shaker* from the *EI* lab. A special mount has been constructed to properly place the packaged device on the shaker as shown below in figure 5.13. The amplifier circuits can be soldered on a proto-PCB and connected to an oscilloscope for final readout. A $1\,V$, $1\,MHz$ AC signal will be sent through the differential amplifier to the left and right contact pads of the accelerometer. The output is drawn from the contact pad connected to the proof mass. This signal is then amplified and displayed. When the

shaker is turned on, the change in acceleration should show a linear change in the amplitude of the output voltage.

Figure 5.13: a) LDS V406 permanent magnet shaker [15]
b) Mount for the shaker

5.4 CONCLUSIONS

In this chapter the fabricated CNT - SiC actuator and accelerometer were tested to check its performance.

- The thermal actuator showed a maximum deflection of 5 μm at 70 V, 3.5 mA. A failure mode was also observed when the current was increased to 4 mA. Hot spots seem to form on the bridge which leads to deformation and breakage. Temperature testing was also performed on the actuator. The device worked even at 200°C but with lesser deflection, possibly due to less slack on the beams.
- Electrical measurements were performed on the nanocomposite to calculate its sheet resistance and resistivity. The nanocomposite showed very high conductivity due to the fact that its electrical properties are dictated by the CNT forest.
- CV measurements were performed to check the rest capacitance of the device. The values obtained match the theoretical values calculated. Although for the structures with 2 μm finger gap it was found that the rest capacitance varies quite a bit and can even short at times due to bending of the nanotubes.
- Temperature resilience tests were performed by heating the sample to 700°C. The Al pads melt at high temperatures while the remaining structure is unaffected due to the superior properties of the SiC filler. However, the stray nanotubes formed by reactivation can cause a short between the fingers.
- The measurement will be carried out using a simple CVC circuit. This will demonstrate that a change in acceleration will show a linear change in the output voltage.

6 CONCLUSION AND FUTURE WORK

In this section, we will first have a complete overview of the work in section 6.1. This is then followed by section 6.2 where we discuss the research objectives that were achieved. The recommended future work is then presented in section 6.3.

6.1 SUMMARY OF THE RESEARCH WORK

The research of harsh environment sensors has been crucial in recent times due to the apparent drawbacks of standard silicon technology. SiC has proved to be a viable replacement to silicon due to its superior properties. However, it is limited to just thin films due to high difficulty in etching.

The limitations of etching SiC can be overcome using CNTs as a 3D scaffold to make high aspect ratio structures. This work focused on fabricating and testing a CNT-SiC nanocomposite MEMS capacitive accelerometer with a comb drive. This would be the first sensor made using this novel technique. The accelerometer, in theory would have higher sensitivity due to larger surface area and potentially, resistance to harsh environments.

A simple MEMS accelerometer was modelled using *COMSOL Multiphysics*. The design focused on creating a device that can show the maximum displacement in order to make the measurement easier. A number of variants were designed to have a large enough data set. The mask was then designed using the *L-edit* tool.

In order to test the process, we first fabricated a CNT-SiC chevron type thermal actuator. The process was optimized based on the observations made during process development. The critical steps being, ensuring a thin TiN layer to allow CNT growth; keeping the filler deposition thickness and nanotube height reasonably low to ease the process of floor layer removal; protecting the TiN layer by the filler material before release of the structure by VHF. The actuator was successfully fabricated followed by the CNT - SiC capacitive accelerometer.

Electrical measurements were performed on the nanocomposite. Results show that the nanocomposite is highly conductive showing a resistivity in the range of $0.004 - 0.009\,\Omega m$. This proves that the electrical properties are dictated by the CNT forest. The mechanical properties of the nanocomposite seemed to be dominated by the SiC filler although, this is not certain since no mechanical stress tests were performed. The CV measurements were made using the *Keysight 4284A LCR meter* to measure the rest capacitance. The experimental values measured matched the calculated theoretical capacitances.

Temperature resilience tests were performed on the samples using the *Nextron microprobe-station*. The device seemed to handle high temperatures of upto $700°C$, but the Al pads did melt. The device was then packaged in a 40-pin DIP. A simple CVC circuit with a shaker and a mount will be used to measure the performance of the accelerometer.

6.2 RESEARCH OBJECTIVES ACHIEVED

In this work, we successfully fabricated and tested the CNT - SiC chevron type thermal actuator. This proves that high aspect ratio surface micromachining of SiC is possible by making use of CNTs as a 3D scaffold. This opens up possibilities of creating actuators that can withstand harsh environments.

We also showed that it is possible to create sensors using this technique. The CNT - SiC accelerometer has been successfully fabricated. The rest capacitance measured agrees with the theoretical calculations. This means that we are no longer constrained by the limitations of surface micromachining of SiC with high aspect ratio structures. More sensors could be designed to fully utilize the increase in aspect ratio while being operational in harsh environments.

The electrical properties of the nanocomposite show that the CNTs dictate the electrical parameters. Thus, making the nanocomposite highly conductive. The mechanical properties are also excellent since it depends on the properties of the filler (SiC) used. This makes the nanocomposite highly resilient to high temperatures.

6.3 RECOMMENDED FUTURE WORK

- The growth of CNTs appear to be affected by the type of layer beneath the catalyst. The growth on TiN and catalyst is different from the growth on TiN, Al_2O_3 and catalyst. This needs to be investigated further.
- This work used amorphous SiC as the filler material since it gives good conformality in the coating of the CNT forest. The forest infiltration of poly-SiC can be investigated to check its affect on the electrical properties of the nanocomposite.
- EDX measurements can be made on the hot spots of the actuator sample or after annealing the nanocomposite to very high temperatures to check the changes that might occur in its composition.
- Although the aspect ratio attained in this work is around 6, the maximum height can be made much higher by using clever supporting structures. More sensors (gas, pressure, etc.) can be fabricated that could benefit from the increase in aspect ratio. These sensors would naturally be resistant to harsh environments by making use of SiC as the filler material.
- Since the fabricated device is resistant to harsh environments, the packaging also needs to be just as resilient, else it would be the limiting factor.
- A *harsh environment smart sensor* could also be a possibility where the readout electronics could be fabricated on the same chip.

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A APPENDIX : SINGLE MEANDER VARIANTS

A.1 SIMULATION RESULTS

Attached below are all the simulation results obtained for the single meander variants using *COMSOL Multiphysics 5.4*.

A.1.1 Proof mass $800\mu mx400\mu m$ Spring width 2μm Finger gap 2μm

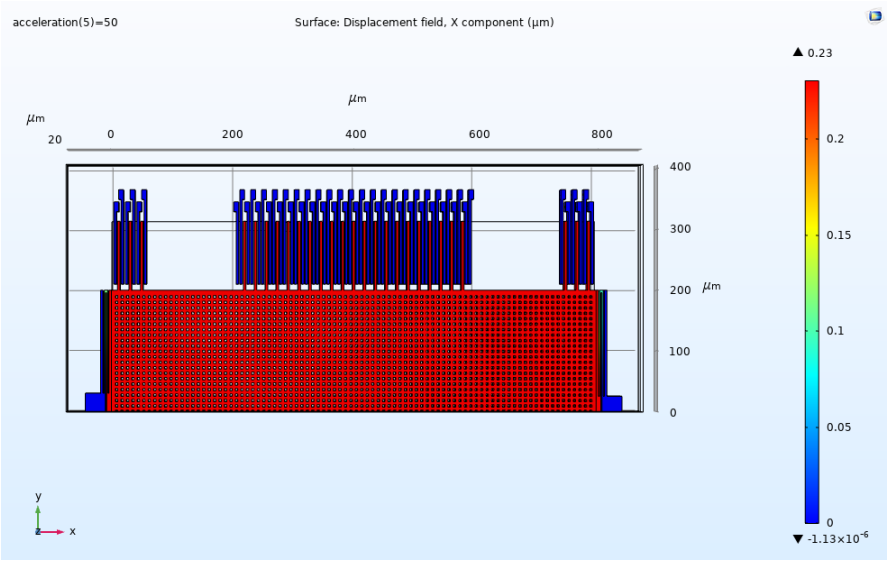


Figure A.1: Simulation result

A.1.2 Proof mass $800\mu mx400\mu m$ Spring width 2μm Finger gap 3μm

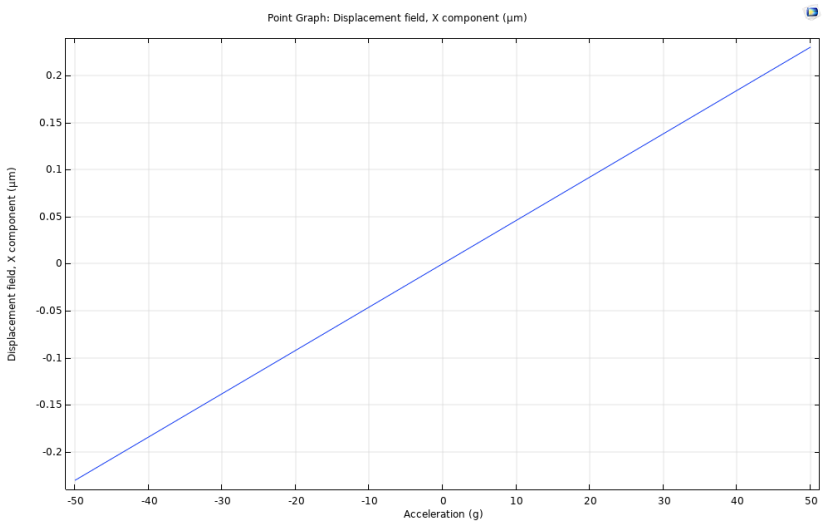


Figure A.2: Displacement vs. acceleration

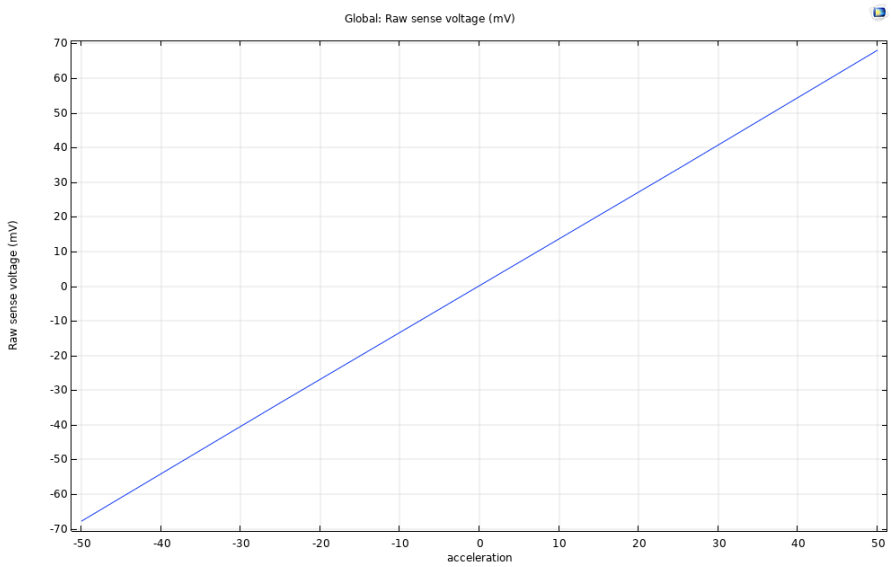


Figure A.3: Sense voltage vs. acceleration

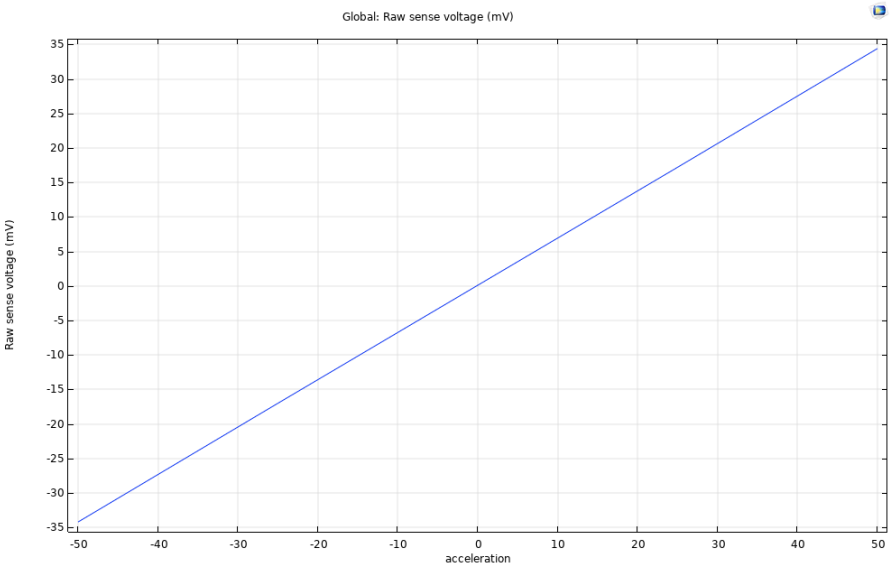


Figure A.4: Sense voltage vs. acceleration

A.1.3 Proof mass $800\mu mx400\mu m$ Spring width 3μm Finger gap 2μm

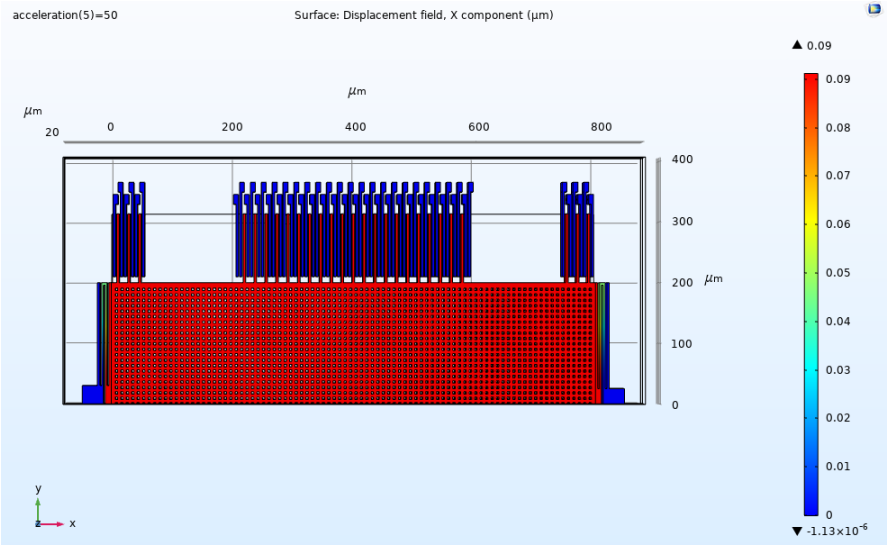


Figure A.5: Simulation result

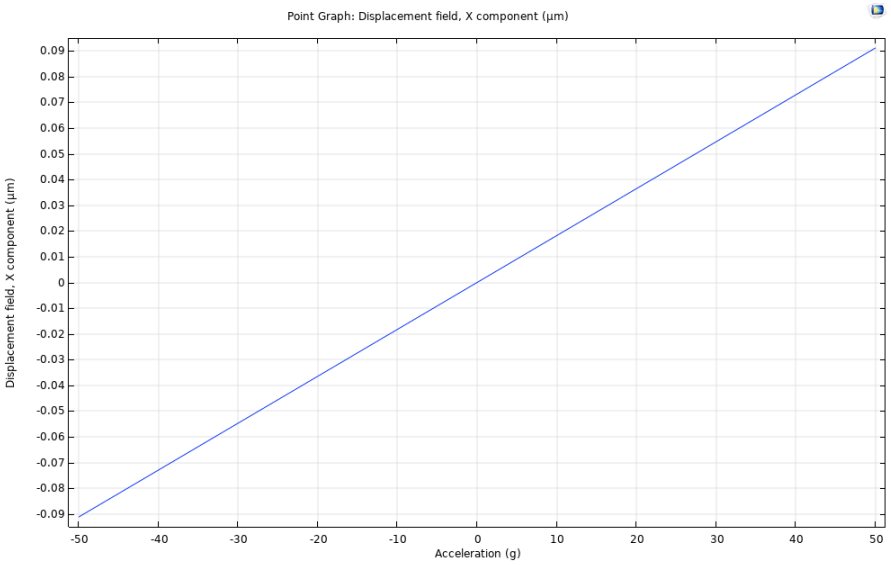


Figure A.6: Displacement vs. acceleration

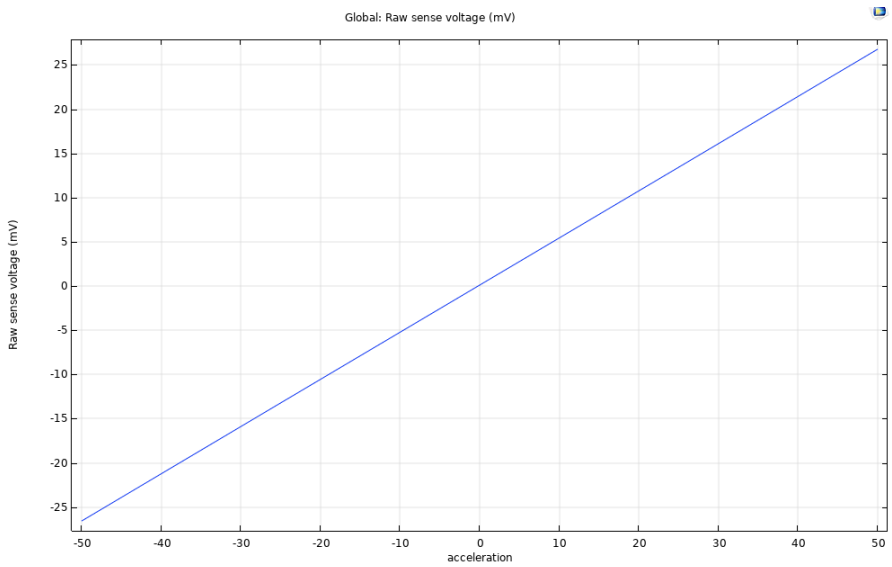


Figure A.7: Sense voltage vs. acceleration

A.1.4 Proof mass $800\mu m x 400\mu m$ Spring width 3μm Finger gap 3μm

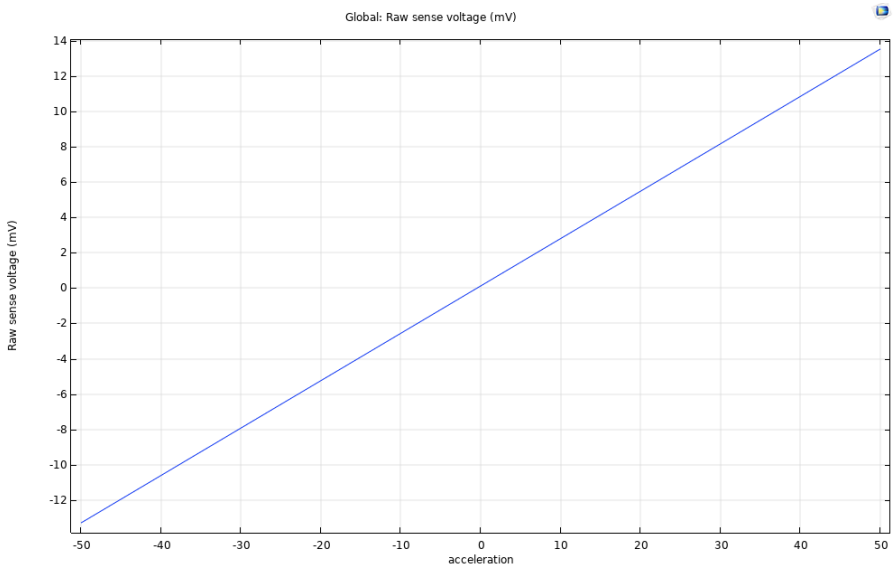


Figure A.8: Sense voltage vs. acceleration

A.1.5 Proof mass $400\mu mx200\mu m$
Spring width 3μm
Finger gap 2μm

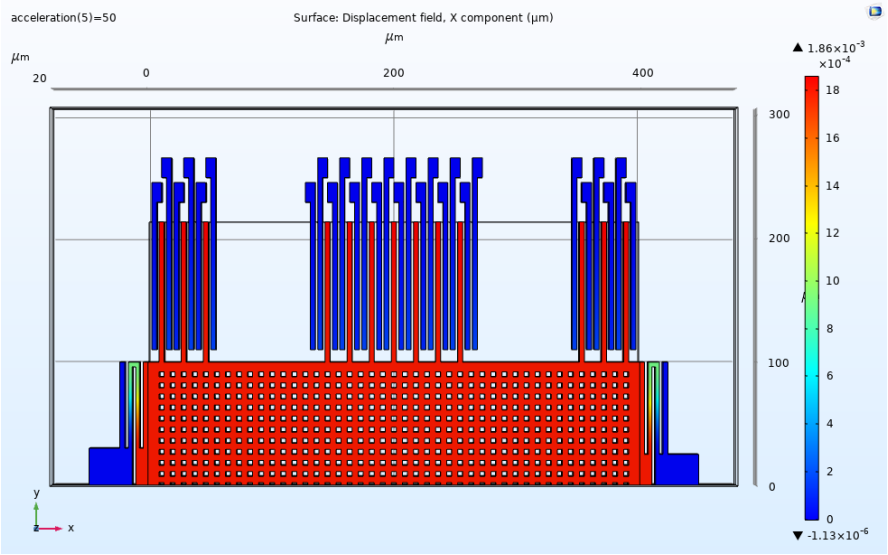


Figure A.9: Simulation result

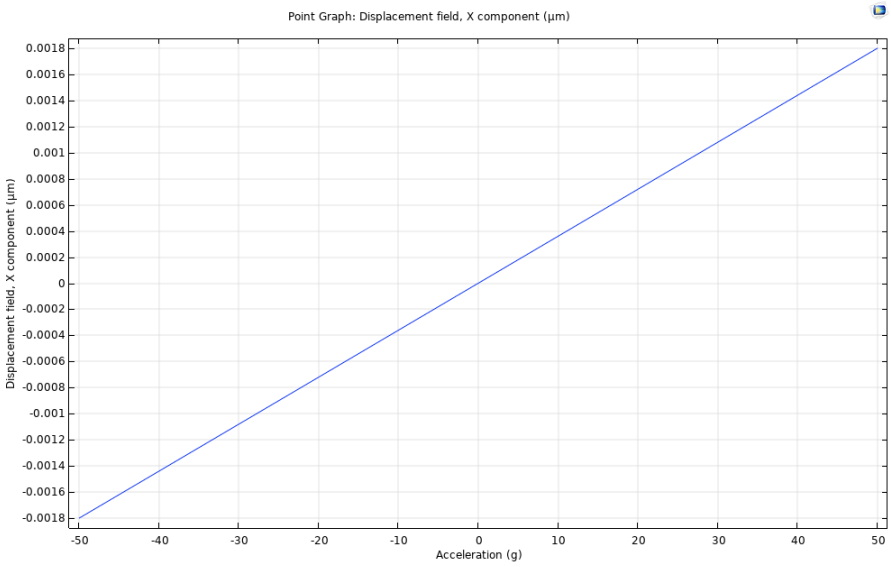


Figure A.10: Displacement vs. acceleration

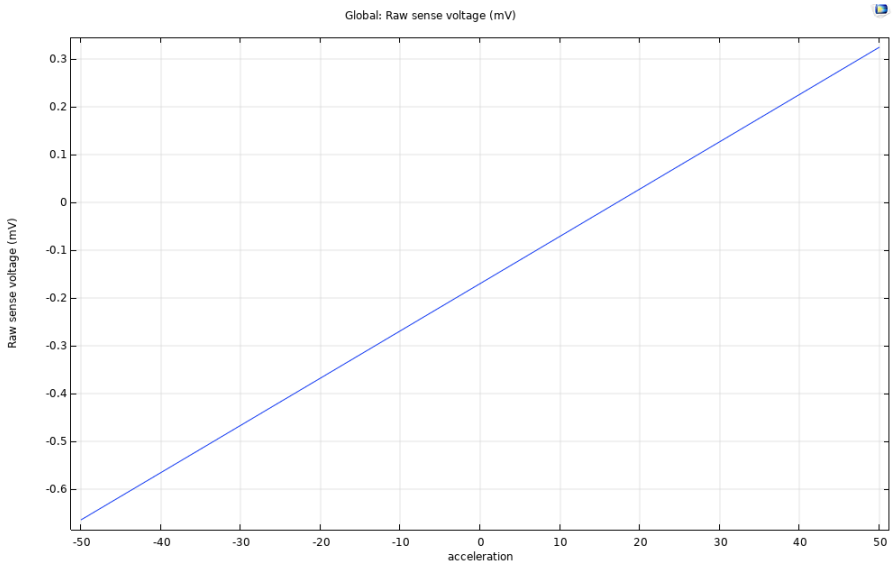


Figure A.11: Sense voltage vs. acceleration

A.1.6 Proof mass $400\mu m x 200\mu m$ Spring width 3μm Finger gap 3μm

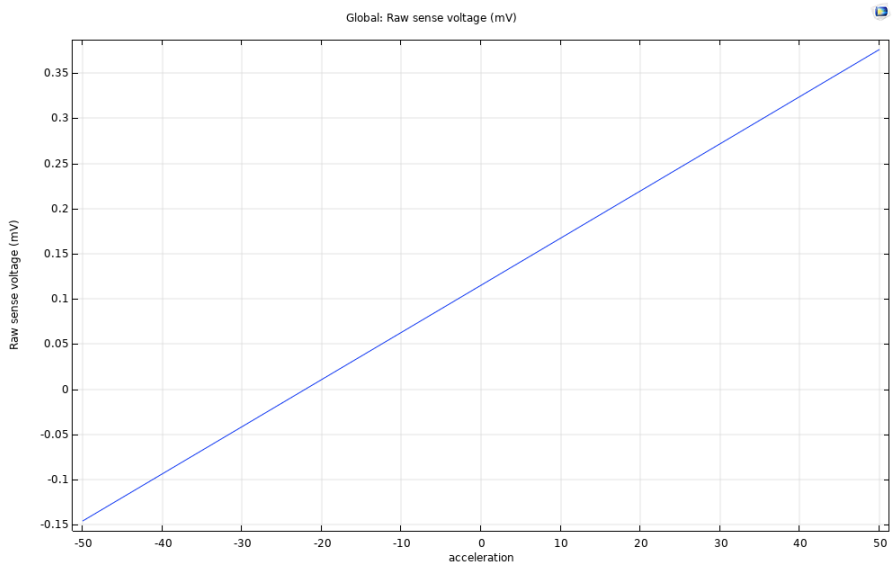


Figure A.12: Sense voltage vs. acceleration

B APPENDIX : DOUBLE MEANDER VARIANTS

B.1 SIMULATION RESULTS

Attached below are all the simulation results obtained for the double meander variants using *COMSOL Multiphysics 5.4*.

B.1.1 Proof mass $800\mu mx400\mu m$ Spring width 3μm Finger gap 2μm

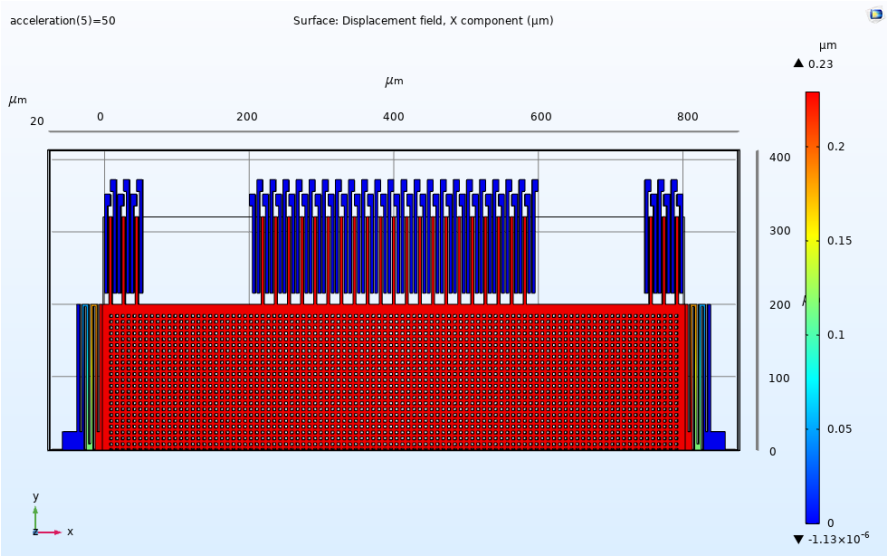


Figure B.1: Simulation result

B.1.2 Proof mass $800\mu mx400\mu m$ Spring width 3μm Finger gap 3μm

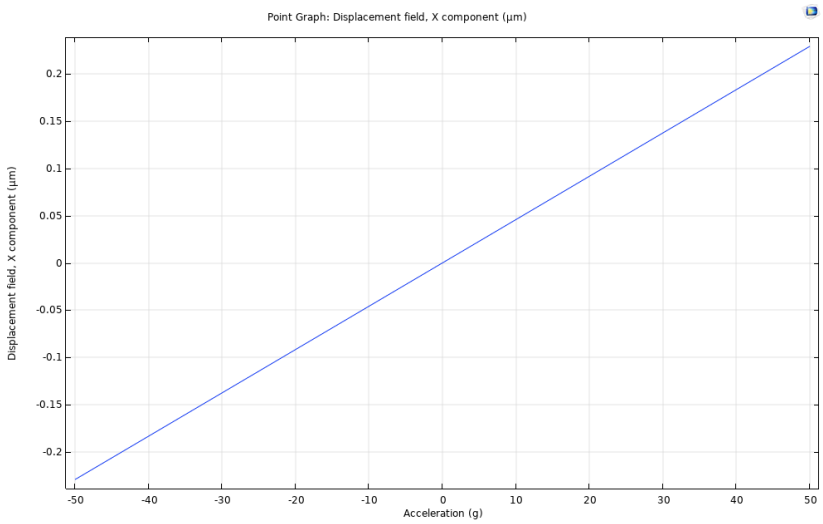


Figure B.2: Displacement vs. acceleration

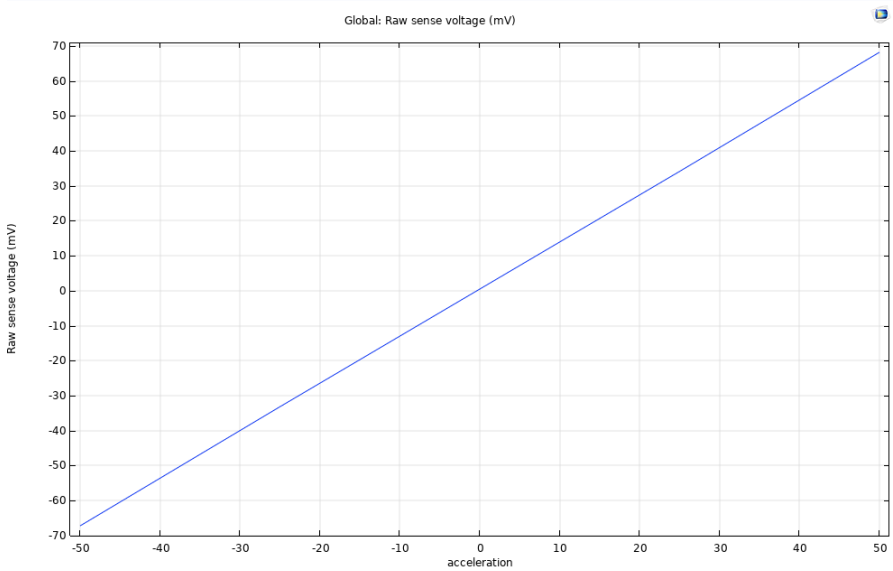


Figure B.3: Sense voltage vs. acceleration

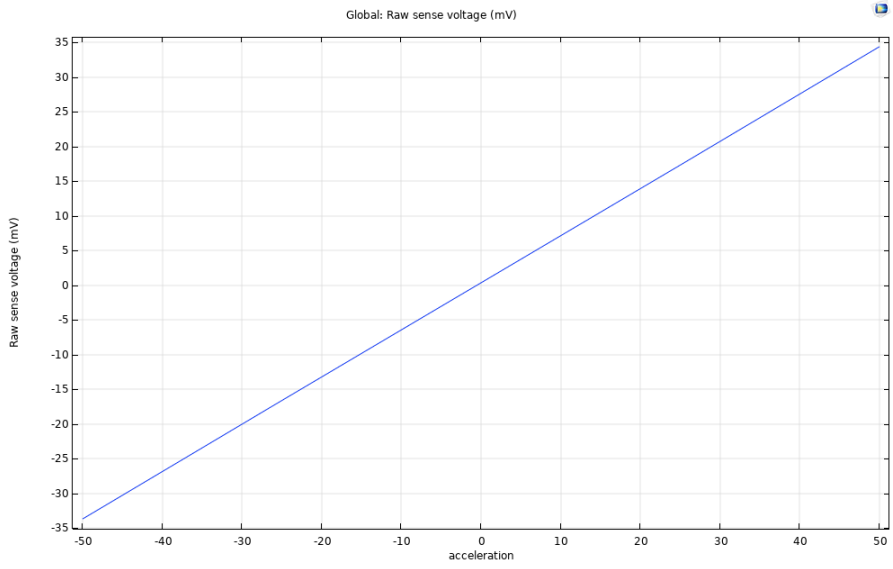


Figure B.4: Sense voltage vs. acceleration

B.1.3 Proof mass $800\mu m x 400\mu m$
Spring width 4μm
Finger gap 2μm

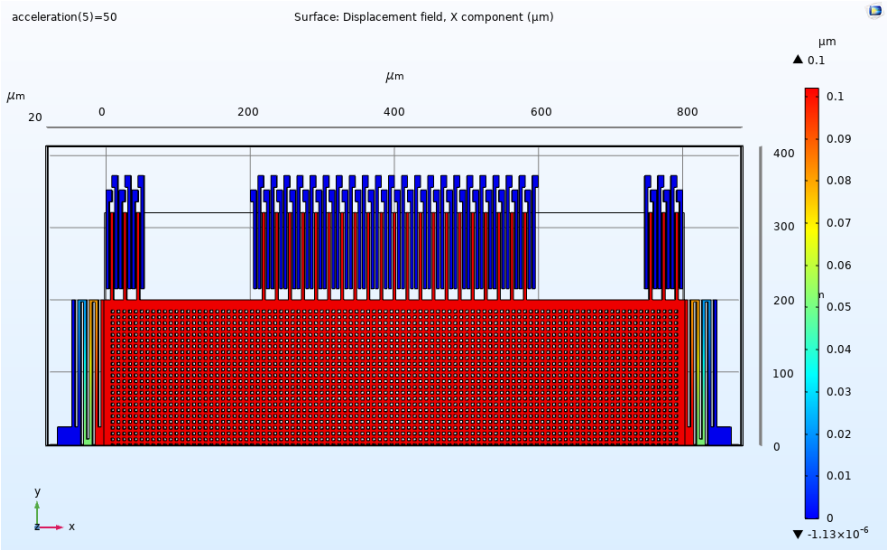


Figure B.5: Simulation result

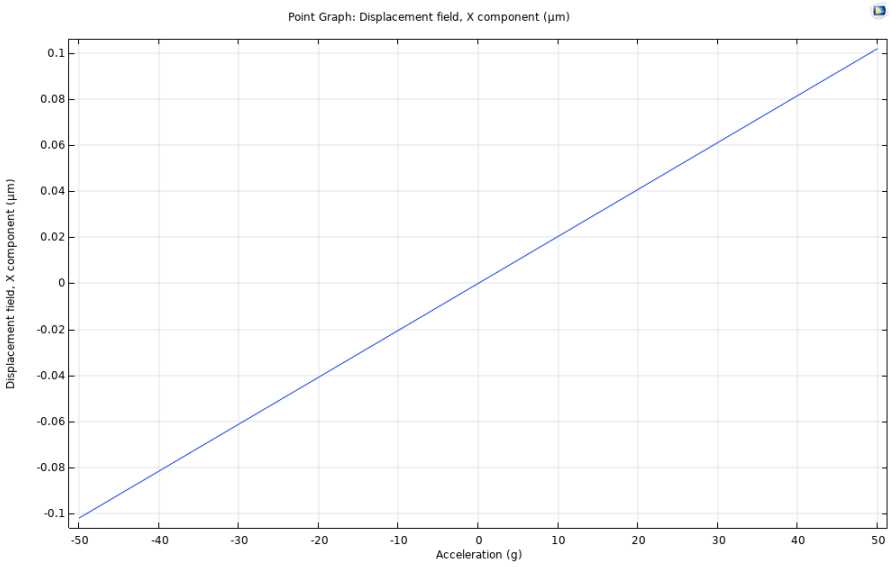


Figure B.6: Displacement vs. acceleration

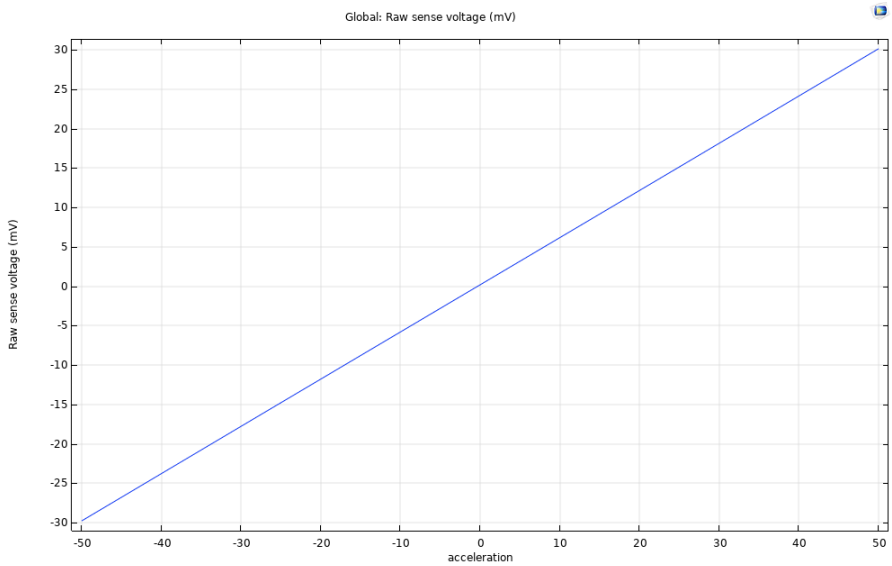


Figure B.7: Sense voltage vs. acceleration

B.1.4 Proof mass $800\mu mx400\mu m$ Spring width 4μm Finger gap 3μm

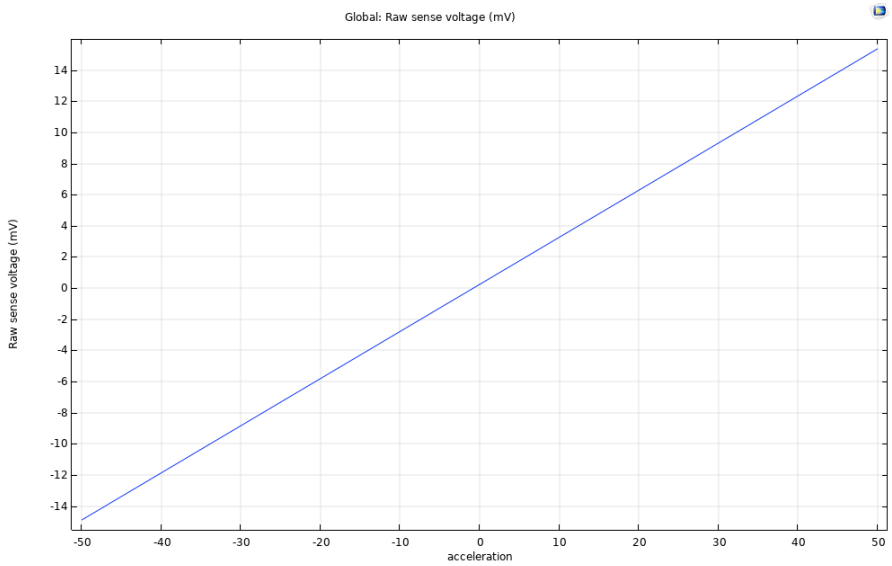


Figure B.8: Sense voltage vs. acceleration

B.1.5 Proof mass $400\mu m x 200\mu m$ Spring width 3μm Finger gap 2μm

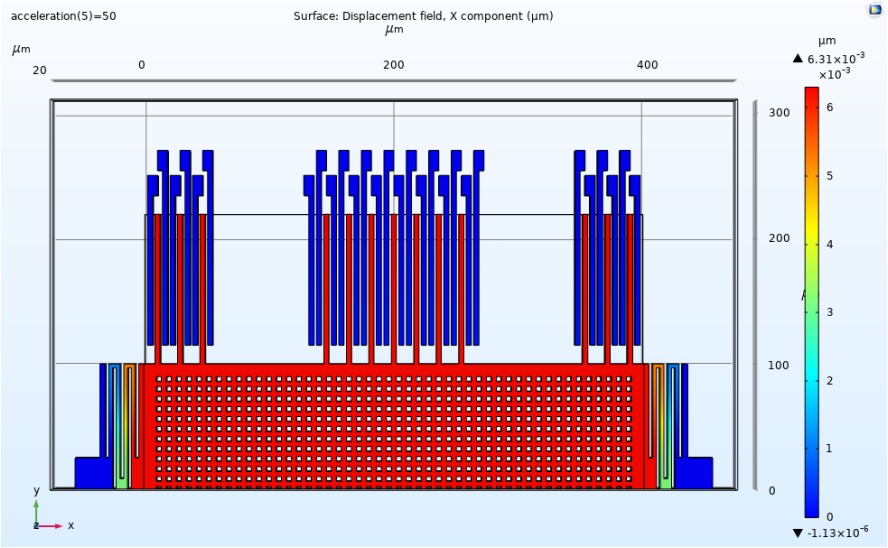


Figure B.9: Simulation result

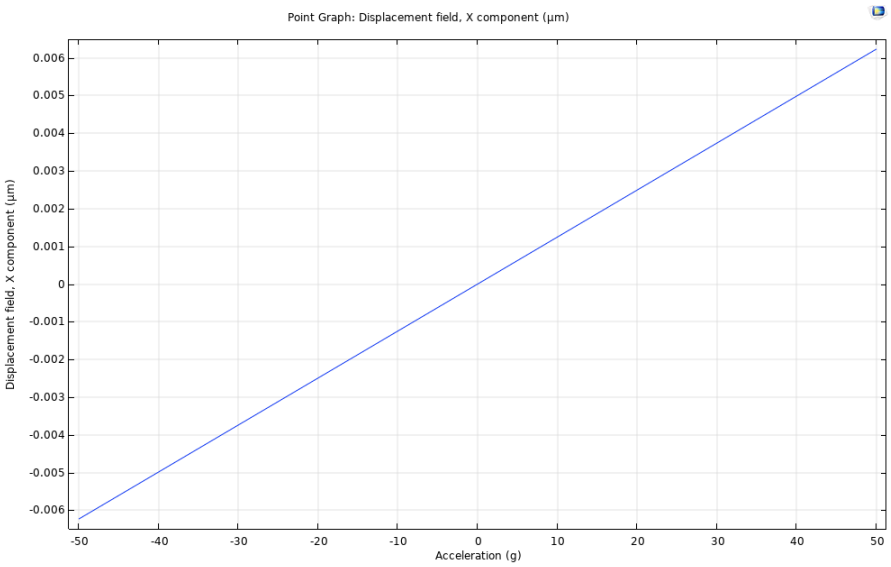


Figure B.10: Displacement vs. acceleration

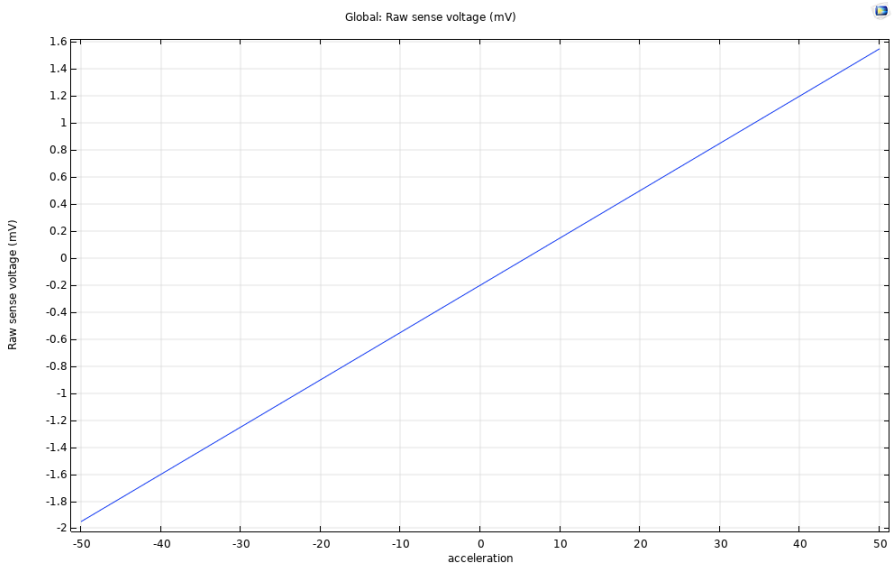


Figure B.11: Sense voltage vs. acceleration

B.1.6 Proof mass $400\mu mx200\mu m$ Spring width 3μm Finger gap 3μm

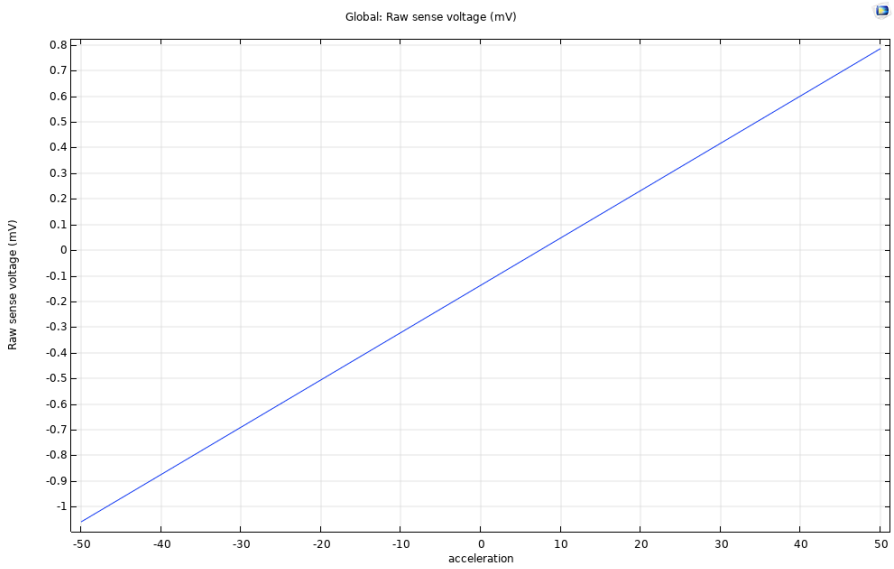


Figure B.12: Sense voltage vs. acceleration

C APPENDIX : CNT BASED THERMAL ACTUATOR

C.1 FLOWCHART

1. **COATING**
   Use the EVG 120 wafer track to coat the wafers with resist and follow the instructions specified for this equipment. The process consists of a treatment with HMDS (hexa methyl disilazane) vapor with nitrogen as a carrier gas, spin coating with Shipley SPR3012 positive photoresist and a soft bake at 95°C for 90 seconds. Always check the temperature of the hotplate and the relative humidity (48 ± 2 %) in the room first.

   Use coating "CO 3012 – 1.4 μm – no EBR" (resist thickness: 1.400 µm).

2. **ALIGNMENT AND EXPOSURE**
   Processing is performed on the ASM PAS 5500/80 automatic wafer stepper.

   Follow the operating instructions from the manual when using this machine.

   Use the correct litho job:
   Job: litho/ZEFWAM
   Layer ID: 1
   Mask ID: COMURK
   Exposure energy: 120 mJ/cm^2.

3. **DEVELOPING**
   Use the EVG 120 wafertrack to develop the wafers and follow the instructions specified for this equipment. The process consists of a post-exposure bake at 115°C for 90 seconds, followed by a development step using Shipley MF322 developer (single puddle process) and a hard bake at 100°C for 90 seconds. Always check the temperature of the hotplates first.

   Use development recipe "Dev – SP"

4. **INSPECTION**
   Visually inspect the wafers through a microscope:
   - No resist residues are allowed.
   - Check the linewidth of the structures.
   - Check the overlay of the exposed pattern if the mask was aligned to a previous pattern on the wafer.

5. **WAFER NUMBERING**
   Use the glass pen in the lithography room to mark the wafers with the BATCH and WAFER number. Write the numbers in the photoresist, just above the wafer flat. Always do this after exposure and development! It is NOT allowed to use a metal pen or a scriber (pen with a diamond tip) for this purpose.

6. **PLASMA ETCHING: Alignment markers (URK's) into Silicon**
   Use the Trikon Omega 201 plasma etcher. Follow the operating instructions from the manual when using this machine. It is not allowed to change the process conditions and times from the etch recipe!

   Use sequence URK_NPD (with a platen temperature of 20 °C) to etch 120 nm deep ASM URK's into the Si.

	Process conditions from chamber recipe URK_ETCH:					
Step	Gasses & flows	Pressure	Platen RF	ICP RF	Platen temp.	Etch time
1. breakthrough	CF_4/O_2 = 40/20 sccm	5 mTorr	60 W	500 W	20 °C	0'10"
2. bulk etch	Cl_2/HBr = 80/40 sccm	60 mTorr	20 W	500 W	20 °C	0'40"

7. **LAYER STRIPPING**
   Strip resist Use the Tepla Plasma 300 system to remove the photoresist in an oxygen plasma. Follow the instructions specified for the Tepla stripper, and use the quartz carrier. Use Program 1: 1000 watts power and automatic endpoint detection + 2 min. overetching.

8. **CLEANING: HNO3 99% and 69.5%**
   Clean - 10 minutes in fuming nitric acid at ambient temperature. This will dissolve organic materials. Use wet bench "HNO3 99% (Si)" and the carrier with the red dot.

   Rinse - Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ

   Clean - 10 minutes in concentrated nitric acid at 110°C. This will dissolve metal particles. Use wet bench "HNO3 69,5% 110C (Si)" and the carrier with the red dot.

   Rinse - Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ

   Dry Use the "Avenger Ultra-Pure 6" rinser/dryer with the standard program, and the white carrier with a red dot.

9. **WET OXIDATION: 3000 nm @ Class 100**
   Use furnace B1 to grow 30,000 Å of wet thermal oxide. Use recipe WETOXIDE with an oxidation time of 18hrs 3min 30sec at 1100°C. The oxide is used to isolate the structures from the substrate and to remove future possible backside contamination. Also a thick oxide helps in minimizing break-down. Verify thickness after.

10. **TiN METALLIZATION @ Class 100**
    Use the TRIKON SIGMA sputter coater for the deposition of TiN metal layer on the process wafers. Follow the operating instructions from the manual when using this machine. Reactively sputter 10 nm Ti for adhesion and a 50nm thick layer of TiN. Temperature = 350°C Visual inspection: the metal layer must look shiny.

    Use recipe Ti_10nm_TiN_50nm_350C
    Put dummy wafers between the process wafer with recipe Ti_in_between_350C to clean the target between depositions.

11. **COATING AND BAKING @ Class 100**
    Use the EVG-120 automatic wafertrack to coat the wafers with 1.4 µm resist. The process includes a treatment with HMDS (hexamethyldisilazane) vapor with nitrogen as a carrier gas, spin coating for 30 s with Shipley SPR 3012 and prebaking for 90 seconds at 95°C. Follow the instructions specified for this equipment, and always check the temperature of the hotplate first.

    Use the program: Co - 3012 – 1400nm_no_EBR (resist thickness: 1.400 µm at 48% RV).

12. **ALIGNMENT AND EXPOSURE @ Class 100**
    Processing performed on the ASM PAS 5500/80 automatic wafer stepper.

Follow the operating instructions from the manual when using this machine.

Use the correct litho job:
Job: 10mm_diesize/g10a-1
Mask ID: Metal 1
Exposure energy: 140 mJ/cm^2.

13. **DEVELOPMENT @ Class 100**
After exposure a post-exposure bake at 115°C for 90 seconds is performed on the EVG-120 wafer track, followed by a development step using Shipley MF322 developer (single puddle process), and a post bake at 100°C for 90 seconds. Follow the instructions specified for this equipment, and always check the temperature of the hotplates first.

Use program: Dev – SP

14. **INSPECTION: LINEWIDTH**
Visually inspect the wafers through a microscope, and check line-width.

15. **PLASMA ETCH TiN**
Use the Trikon Omega 201 plasma etcher. Follow the operating instructions from the manual when using this machine. The process conditions of the etch and passivation program may not be changed!

Use sequence TINTISVO and set the platen temperature to 25°C (check) to etch the TiN layer, set time: 25 seconds

16. **RESIST STRIPPING @ SAL**
Remove the resist in SAL using NMP @ 70°C (Si compatible bottle and glass-wear!). Don't perform a Tepla clean as this will damage the TiN!

17. **CLEANING PROCEDURE: HNO_3 100% metal**
Cleaning: 10 minutes in fuming nitric acid (Merck: HNO_3 100% selectipur) at ambient temperature. Use wet bench "HNO_3 (100%) metal" and the carrier with the yellow and red dots.
QDR: Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Drying: Use the Semitool "rinser/dryer" with the standard program, and the white carrier with a black dot.
NOTE: No 65% HNO_3 cleaning step!

18. **Al_2O_3 deposition @ Class 100**
Use the TRIKON SIGMA sputter coater for the deposition of Al_2O_3 metal layer on the process wafers. Follow the operating instructions from the manual when using this machine. Reactively sputter a 20nm thick layer of Al_2O_3. Temperature = 100°C Visual inspection: the metal layer must look shiny.

Recipe: Al_2O_3_20nm_100C

Check if the power supply pulse setting are correctly set for Al_2O_3

19. **COATING AND BAKING @ Class 100**
Use the EVG-120 automatic wafertrack to coat the wafers with 1.4 µm resist. The process includes a treatment with HMDS (hexamethyldisilazane) vapor with nitrogen as a carrier gas, spin coating for 30 s with Shipley SPR 3012 and prebaking for 90 seconds at 95°C. Follow the instructions specified for this equipment, and always check the temperature of the hotplate first.

Use program: Co - 3012 – 1400nm_no_EBR (resist thickness: 1.400 µm at 48% RV).

20. **ALIGNMENT AND EXPOSURE @ Class 100**
Processing performed on the ASM PAS 5500/80 automatic wafer stepper.

Follow the operating instructions from the manual when using this machine.

Use the correct litho job:
Job: 10mm_diesize/g10a-1
Mask ID: Metal 2
Exposure energy: 140 mJ/cm^2.

21. **DEVELOPMENT @ Class 100**
After exposure a post-exposure bake at 115°C for 90 seconds is performed on the EVG-120 wafer track, followed by a development step using Shipley MF322 developer (single puddle process), and a post bake at 100°C for 90 seconds. Follow the instructions specified for this equipment, and always check the temperature of the hotplates first.

Use program: Dev – SP

22. **INSPECTION: LINEWIDTH**
Visually inspect the wafers through a microscope, and check line-width.

23. **WET ETCH Al2O3**
Remove the Al2O3 layer using 0.55% HF for metals in SAL. Etch rate is 200nm/min, a 1 min dip is enough to be sure the layer is completely removed without too much overetch. Rinse till 5 $M\Omega$ and dry on manual dryer.

24. **RESIST STRIPPING**
Remove the resist in CR100 using the Acetone bath at 35°C, submerge wafers for at least 1 min and use transport boxes to transport the wafer to the cleaning line

25. **CLEANING PROCEDURE: HNO3 100% metal**
Cleaning: 10 minutes in fuming nitric acid (Merck: HNO3 100% selectipur) at ambient temperature. Use wet bench "HNO3 (100%) metal" and the carrier with the yellow and red dots.
QDR: Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Drying: Use the Semitool "rinser/dryer" with the standard program, and the white carrier with a black dot.
NOTE: No 65% HNO3 cleaning step!

26. **COATING AND BAKING @ Class 100**
Use the EVG-120 automatic wafertrack to coat the wafers with 1.5 µm resist. The process includes a treatment with HMDS (hexamethyldisilazane) vapor with nitrogen as a carrier gas, spin coating for 30 s with AZ Nlof2000 and prebaking for 90 seconds at 100°C. Follow the instructions specified for this equipment, and always check the temperature of the hotplate first. Use program: Co - Nlof2020 – 1500nm no EBR (resist thickness: 1.50 µm at 48% RV).

27. **ALIGNMENT AND EXPOSURE @ Class 100**
Processing performed on the ASM PAS 5500/80 automatic wafer stepper.

Follow the operating instructions from the manual when using this machine.

Use the correct litho job:
Job: 10mm_diesize/g10a-1
Mask ID: Metal 3
Exposure energy: 140 mJ/cm^2.

Also expose the edge using the open 10x10 mm reticle (box 262)
Job: g10a-edge(full), Layer id = 2, energy = 55 mJ/cm^2

28. **X-LINK BAKE @ Class 100**
Cross-link bake step on the EVG-120

Program: Dev – X-link only

29. **DEVELOPMENT @ Class 100**
    Development step on the EVG-120 using Shipley MF322 developer (double puddle process), and a hard bake at 100 °C for 90 seconds. Follow the instructions specified for this equipment, and always check the temperature of the hotplates first.

    Use program: Dev – DP 2 no PEB

30. **Fe CATALYST DEPOSITION @ Class 10000**
    Use the CHA Solution e-beam evaporator to deposit 2 nm Fe directly on the TiN and Al2O3 surface.
    After this step the wafer are considered contaminated. Use the red wafer box.

31. **Lift-off @ SAL**
    Perform lift-off procedure with NMP solvent in beaker on hotplate with stirrer at 70 °C and 250 rpm. Use dedicated beaker from Cu corner

32. **RINSE & DRY @ SAL**
    Rinse the wafers in DI and dry using manual dryer with special Cu chuck

33. **INSPECTION @ SAL**
    Visually inspect the wafers through a microscope, check if catalyst layer remained on surface. Put paper under wafer and throw away paper after use.

34. **CNT growth @ Class 10000**
    Use the AIXTRON BlackMagic Pro to grow CNTs using LPCVD at 600°C for Fe catalyst layers.

    Use the Cu-free chuck (ask Sten)

    Use recipe: lpcvd_600_vartime Recipe includes an activation step (3 min) in H2 environment at 500 °C, followed by CNT growth using 700/50 sccm H2/C2H2 at 80 mbar for XXX minutes at 600 °C.

    Expected CNT heights: xx μm on TiN, xx μm on Al2O3.

    The reason why we want growth on both surfaces is to address the problem of contacting and electrical isolation of the contact pads. A part of the TiN layer is in contact with the tubes for the purpose of applying potential difference/pumping current. Al2O3 layer electrically isolates the two contact pads from shorting.

35. **Chemical Vapor Deposition @ Class 10000**
    Use Tempress LPCVD F3 to deposit Silicon Carbide over the CNT forests. (only step to be PAC approved).

    Recipe: ... (a-SiC), target: 20 nm thickness Add a test wafer to measure the thickness

36. **Plasma etch of the floor layer - AMS110 @ Class 10000**
    Use the Adixen AMS110 to remove the floor layer Recipe: XXX (a-SiC), target: 20/50 nm thickness

37. **Release of the structures @ CR100**
    The structures are released by using the Vapour HF tool, the wafer can be manually cut into pieces to optimize the etching time.

D APPENDIX : IMPORTANT FIGURES

Attached here are all the images obtained in the work that led to important observations. The nanotubes were grown using *Aixtron Blackmagic* using the *lpcvd_vartime_600* recipe. The samples were observed using the *SEM Hitachi Regulus 8230*.
Note : The heights depicted in the figures (in microns) are before the tilt correction. Therefore, actual height = $\frac{measured\ height}{sin\,\theta}$, where, θ is the tilt angle.

D.1 CNT GROWTH SAMPLES (SPUTTERED Al_2O_3)

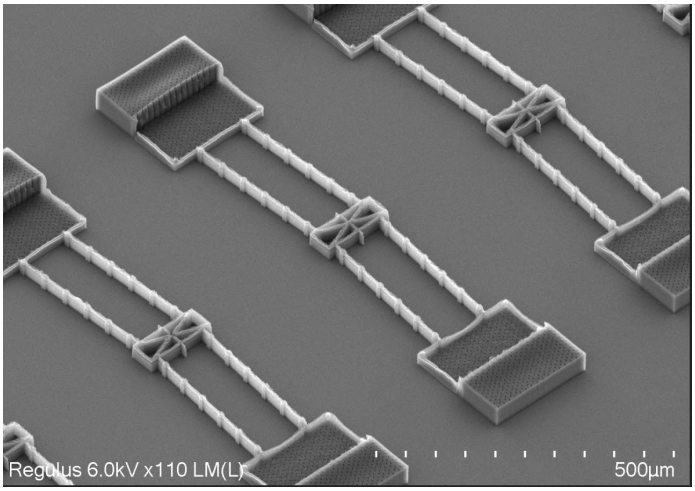


Figure D.1: Growth time = 5 min, Tilt = 45°
Measured height = 5.69 μm

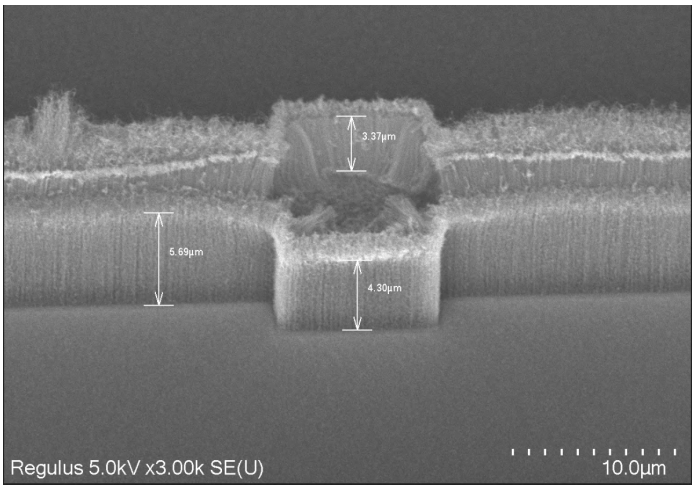


Figure D.2: Growth time = 5 min, Tilt = 45°

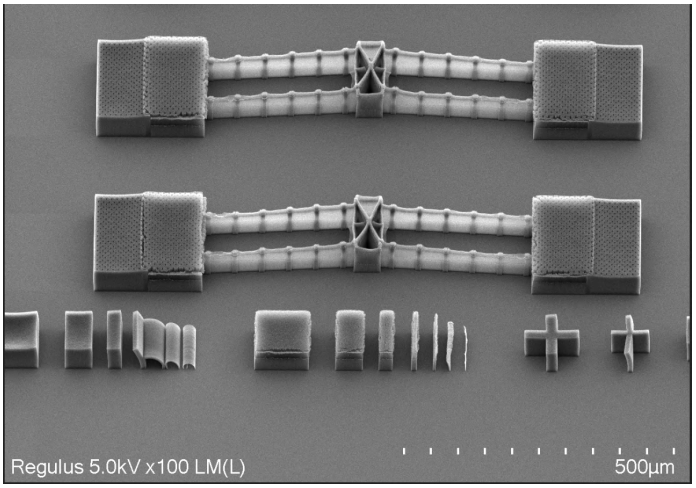


Figure D.3: Growth time = 7 min, Tilt = 45°
Measured height = 32.2 μm

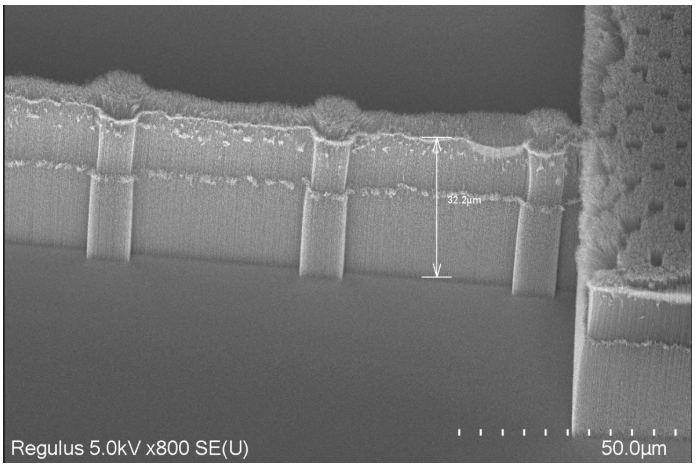


Figure D.4: Growth time = 7 min, Tilt = 45°

D.2 CNT GROWTH SAMPLES (EVAPORATED Al_2O_3)

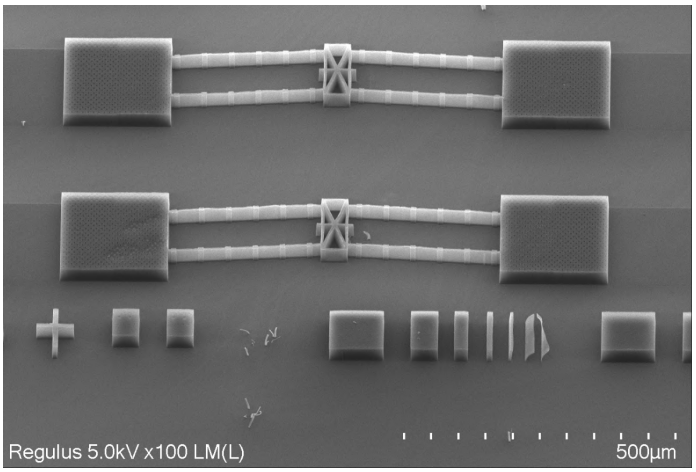


Figure D.5: Growth time = 1 min, Tilt = 45°
Measured height = 23.8 μm

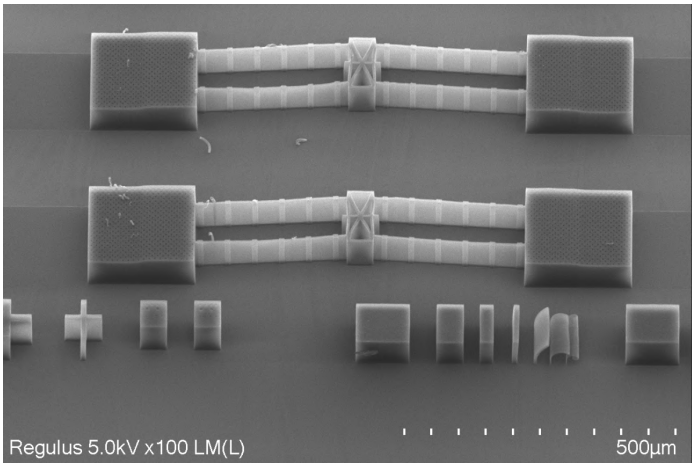


Figure D.6: Growth time = 2 min, Tilt = 45°
Measured height = 43.2 μm

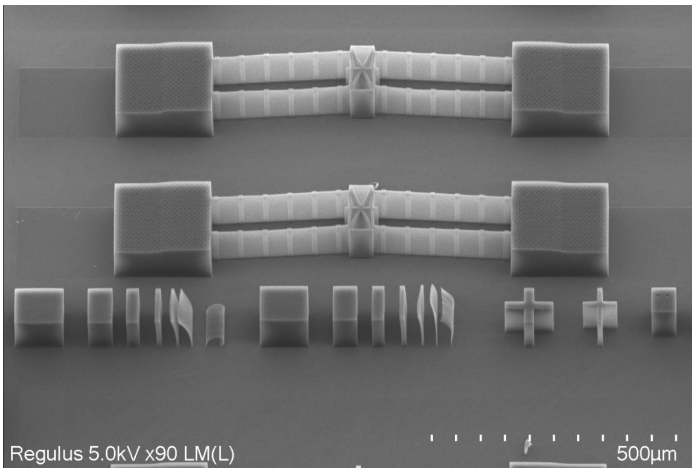


Figure D.7: Growth time = 3 min, Tilt = 45°
Measured height = 51.1 μm

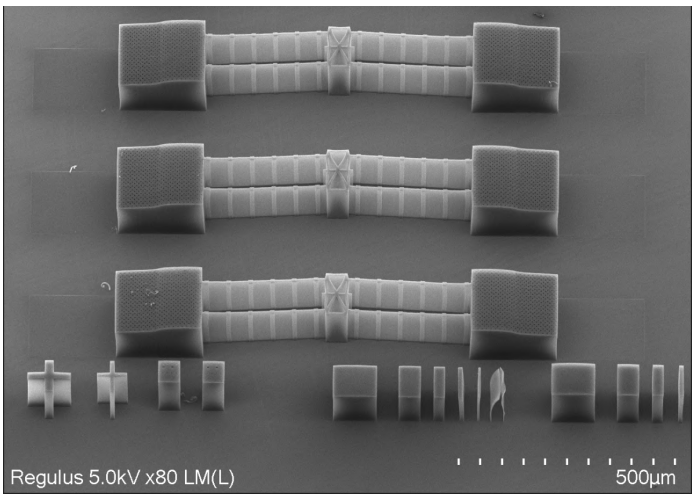


Figure D.8: Growth time = 5 min, Tilt = 45°
Measured height = 68.1 μm

D.3 PECVD SIC ON CNT

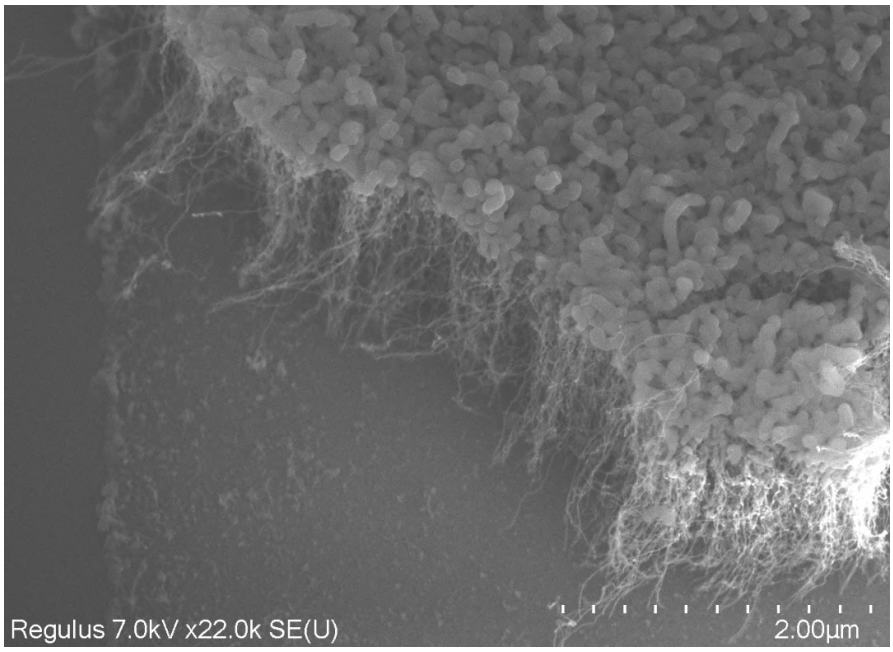


Figure D.9: 50 *nm* PECVD SiC on CNTs after dissection 1

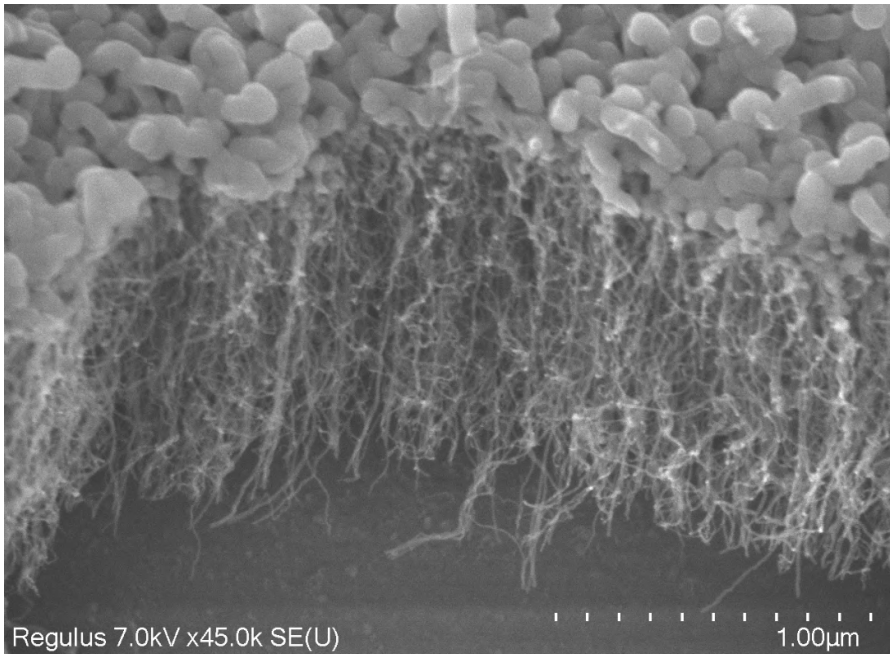


Figure D.10: 50 *nm* PECVD SiC on CNTs after dissection 2

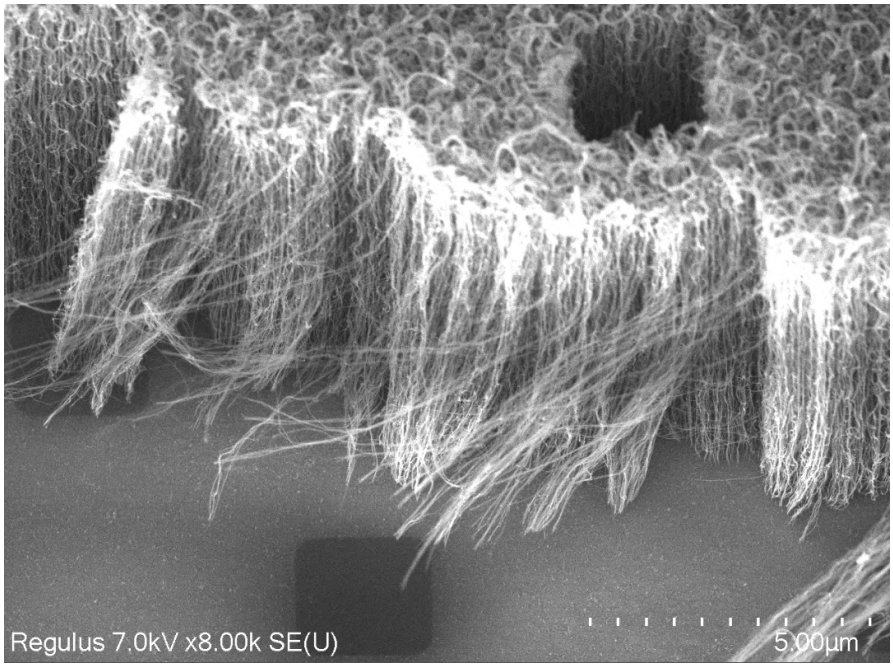
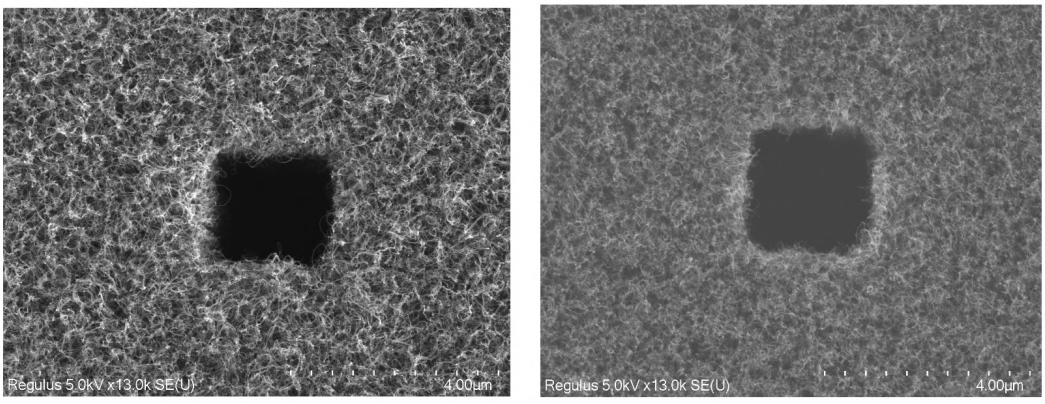


Figure D.11: 50 *nm* PECVD SiC on CNTs after dissection 3

D.4 ALD Al_2O_3 ON CNT



a) **b)**

Figure D.12: a) Top view of uncoated CNT forest
b) Top view of CNT forest coated with 20 *nm* ALD Al_2O_3

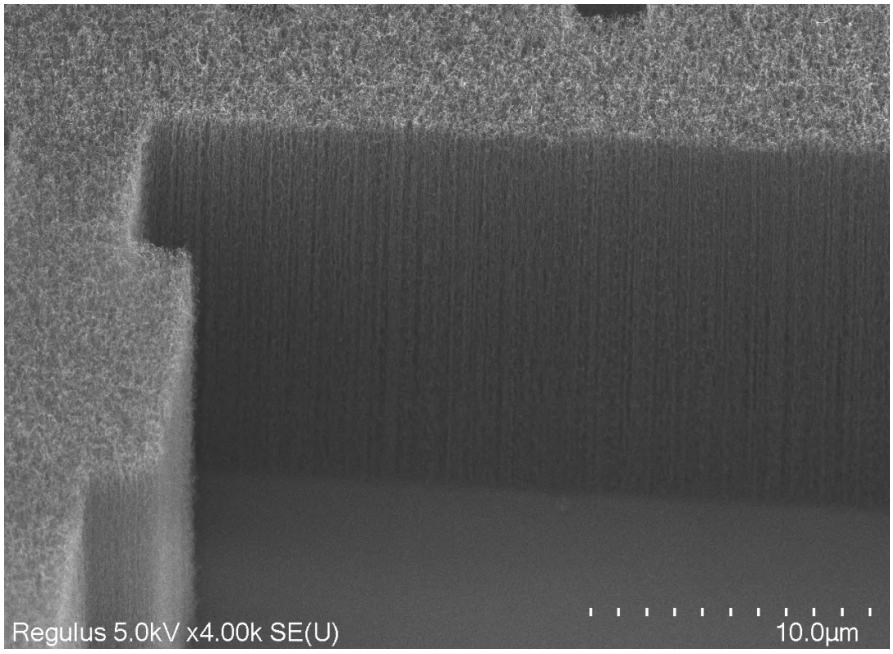


Figure D.13: 20 nm of ALD Al_2O_3
Tilt = 30°, CNT height = 34 μm

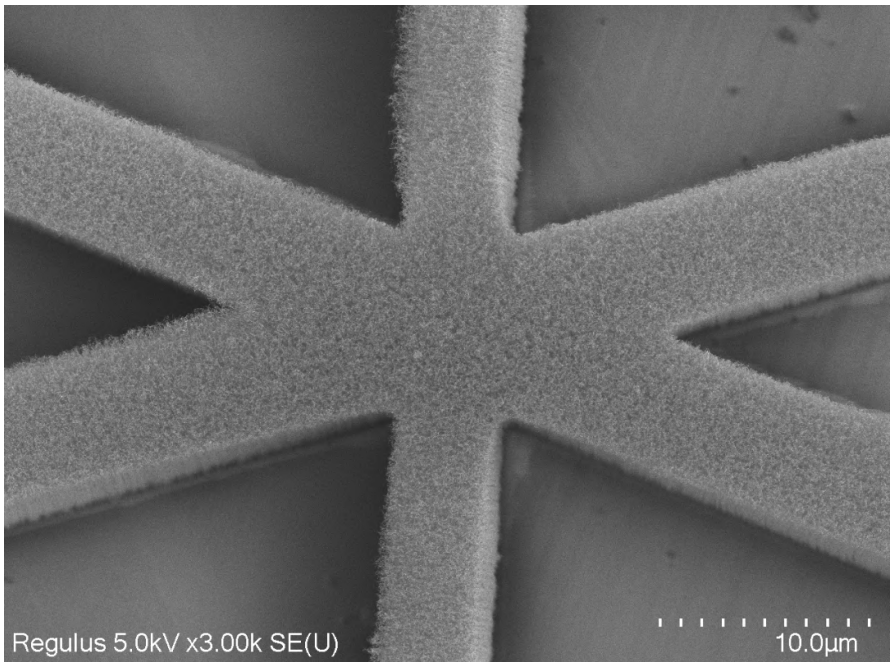


Figure D.14: Top view of the shuttle on the bridge coated with 20 nm ALD Al_2O_3

D.5 LPCVD SIC ON CNT

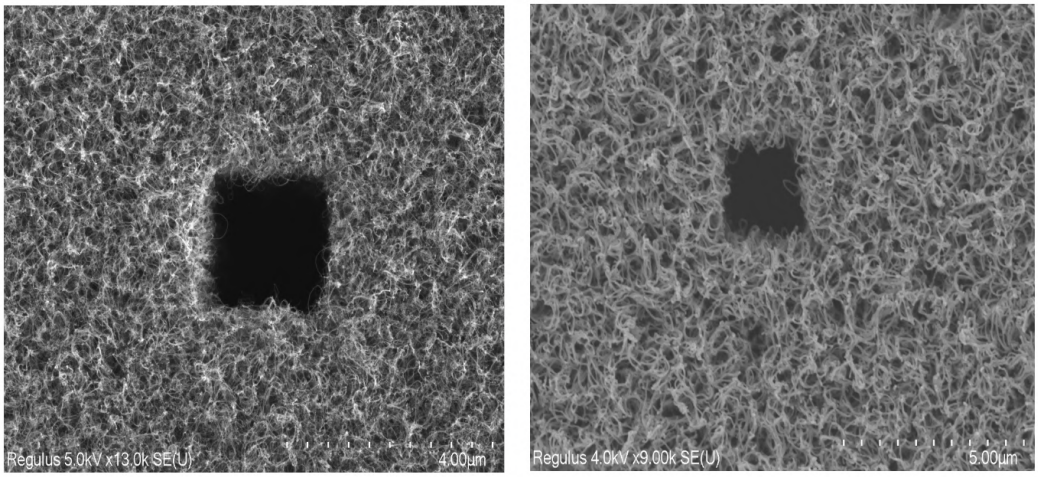


Figure D.15: a) Top view of uncoated CNT forest
b) Top view of CNT forest coated with 20.4 nm LPCVD SiC

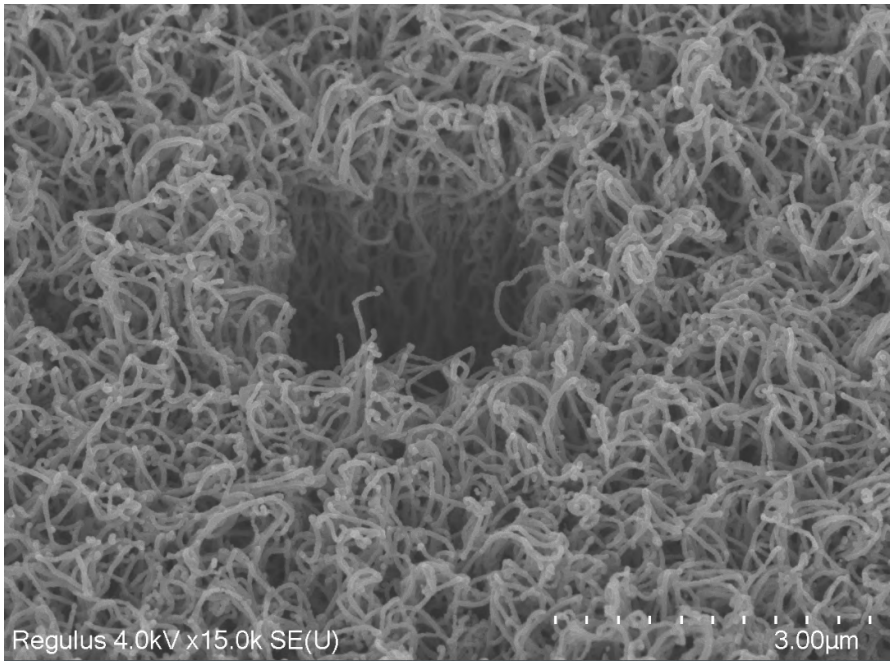


Figure D.16: LPCVD SiC coated vapour access holes, Tilt = 30°

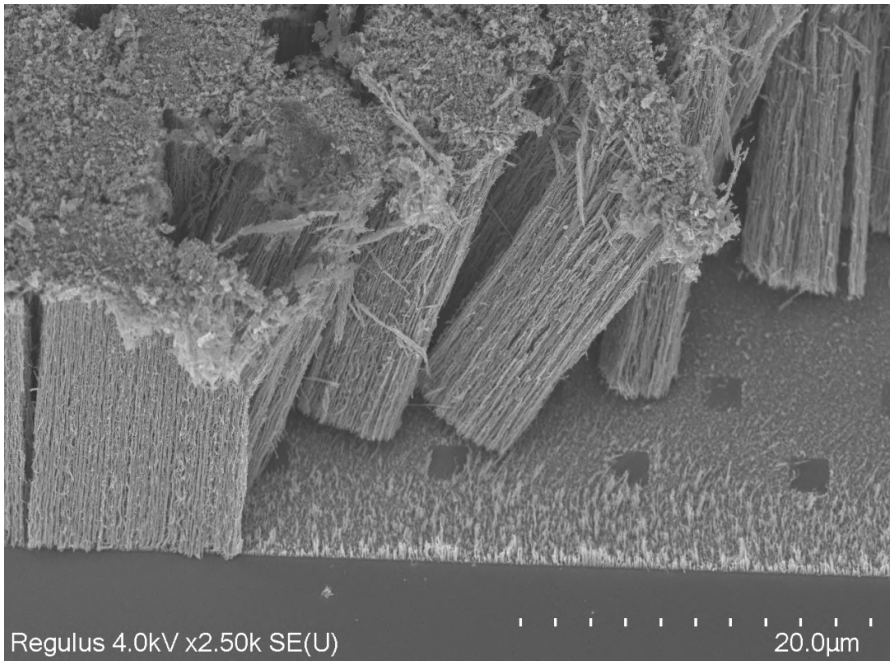


Figure D.17: Dissected structure of LPCVD SiC coated CNT forest

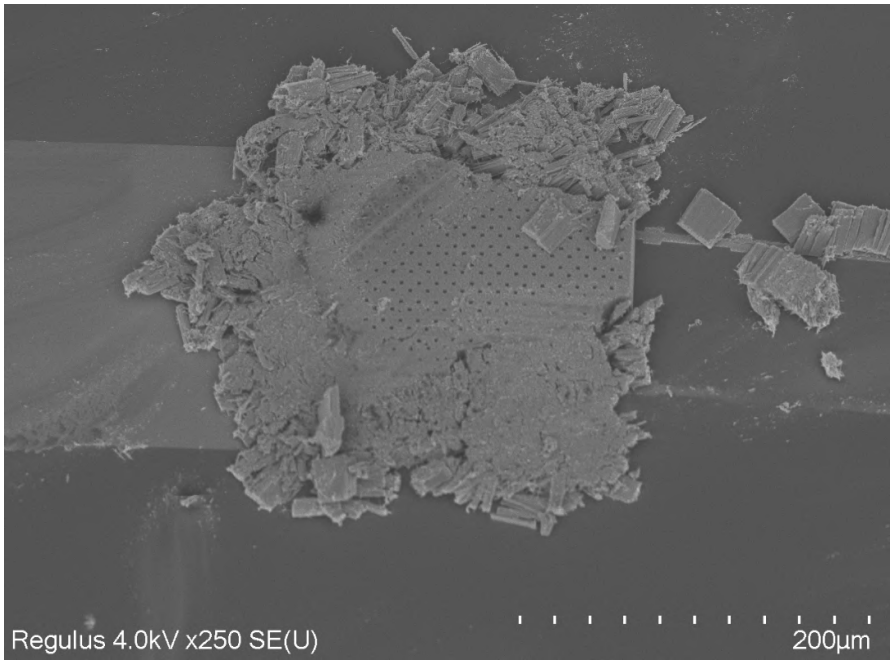


Figure D.18: Failure mode observed after excess force on the coated structure

D.6 AMS110 ETCH TESTS

In this section we have a few results obtained from etching the floor layer of the ALD Al_2O_3 samples of the thermal actuator. The recipe required optimization due to the damage being done to the CNTs. The SEM images obtained are attached below.

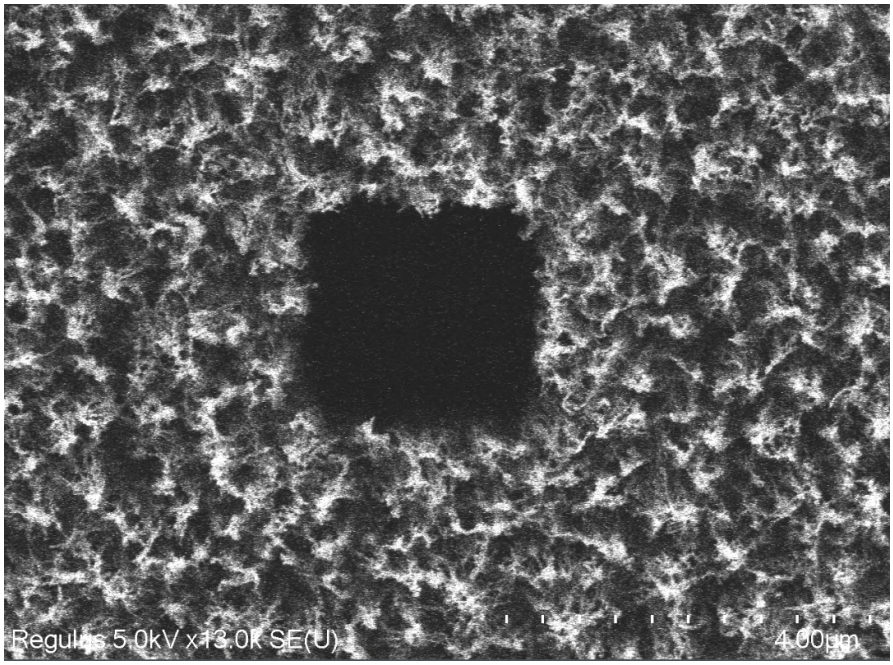


Figure D.19: Top view of ALD Al_2O_3 coated sample suffering from severe damage after RIE
Etch time = 1 *min*

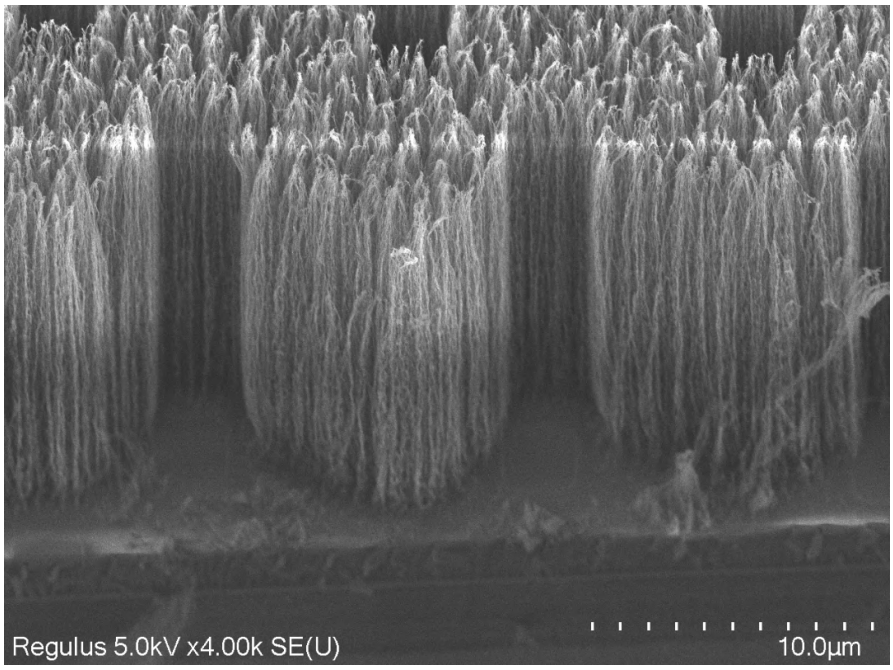


Figure D.20: Initial CNT height $\approx$ 34 μm
20 nm ALD Al_2O_3
AMS110 etch SF_6 ,O_2
Etch time = 1 *min*, Tilt = 30°

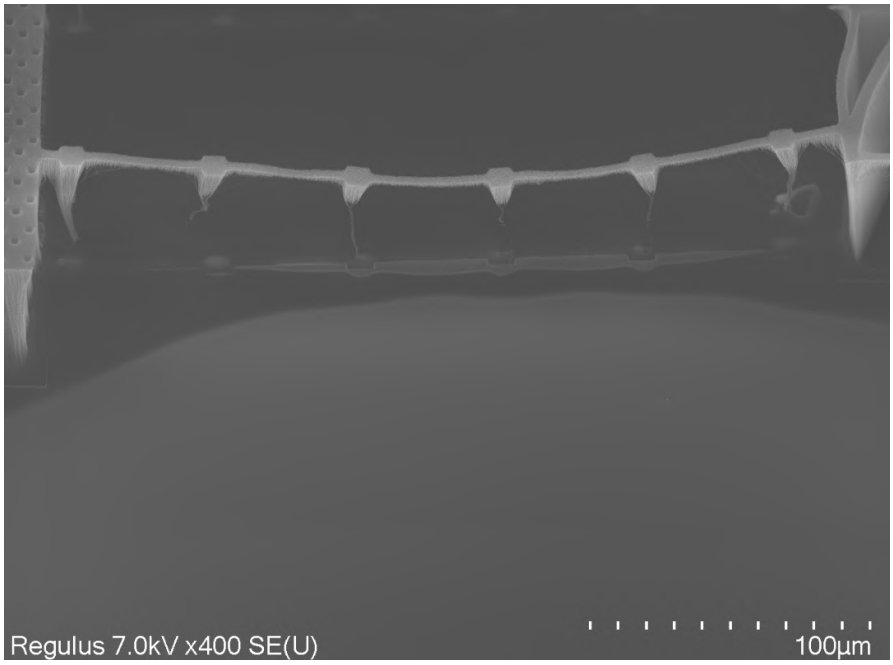


Figure D.21: CNT bridge completely etched away from excess RIE
20 nm ALD Al_2O_3
AMS110 etch SF_6 ,O_2
Etch time = 2 $mins$, Tilt = 30°

D.7 VAPOUR HF RELEASE TESTS

In this section we have a few results obtained from etching the oxide layer of the thermal actuator samples. Two recipes were tested -
Recipe 2 : 310 *sccm* of HF, 350 *sccm* of EtOH and 1250 *sccm* of N_2 at 125 *torr* pressure.
Recipe 3 : 525 *sccm* of HF, 400 *sccm* of EtOH and 1000 *sccm* of N_2 at 125 *torr* pressure

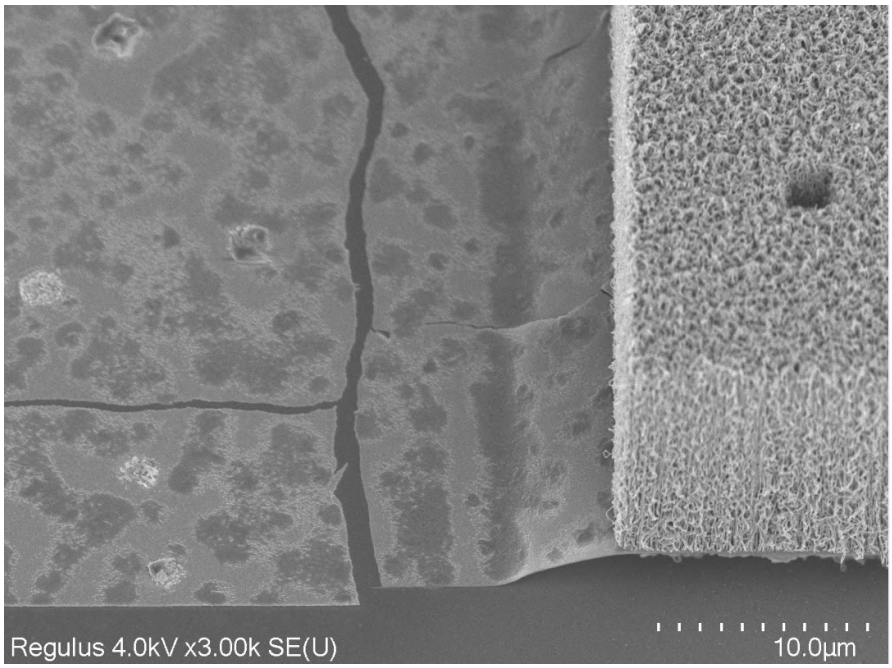


Figure D.22: Recipe 2
6 μm of oxide etched

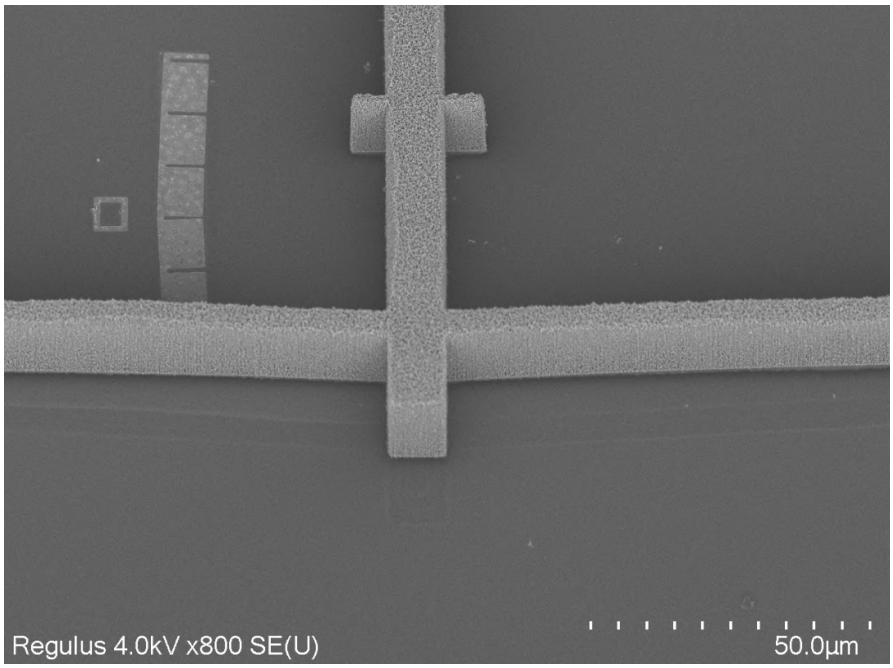


Figure D.23: Recipe 2
6 μm of oxide etched
Bridge released

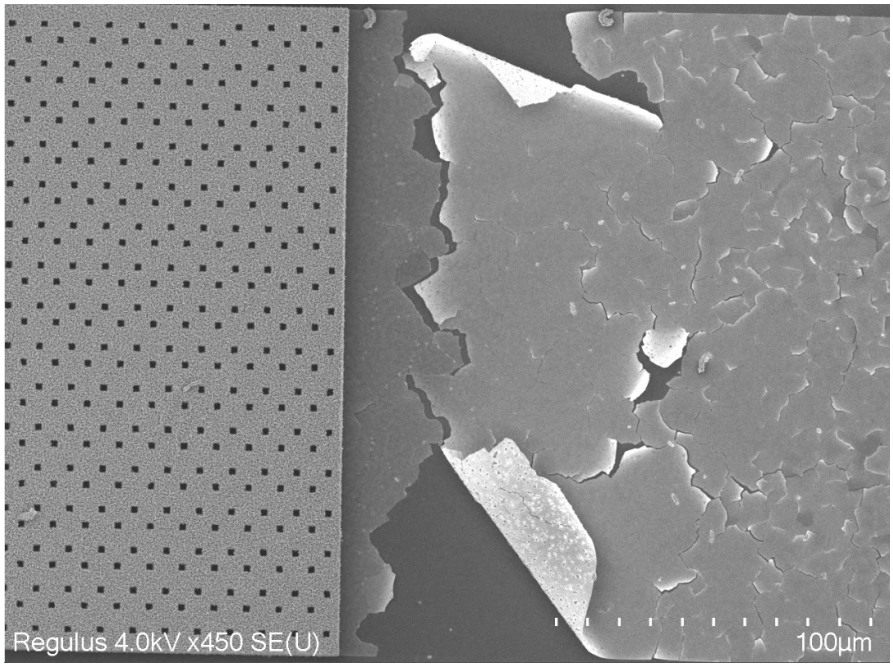


Figure D.24: Recipe 3
6 μm of oxide etched
TiN pad corroded

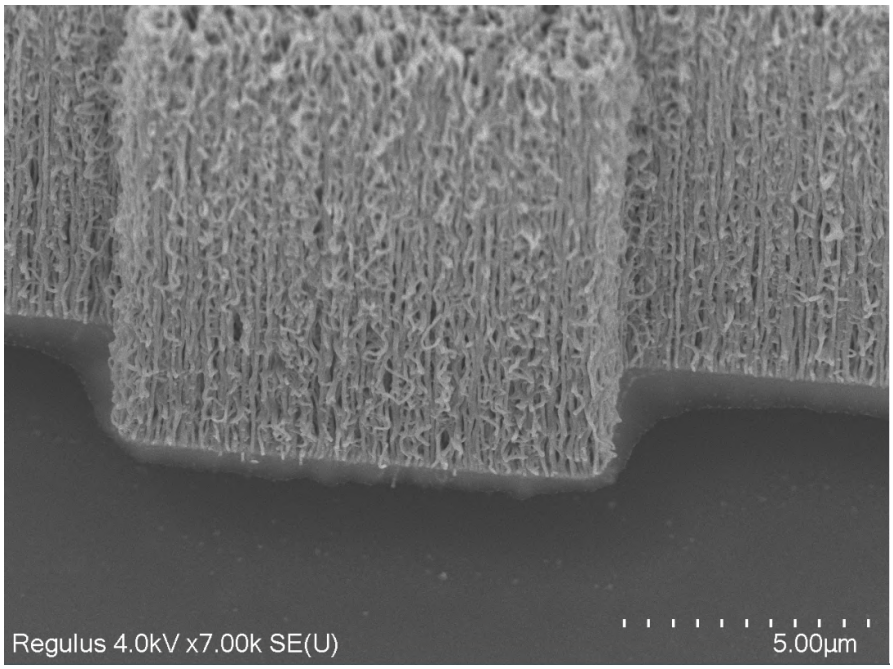


Figure D.25: Recipe 3
6 μm of oxide etched
SiC residues near base

D.8 SIC COATING OF CNT BASED ACCELEROMETER

In this section we have a few results obtained from LPCVD coating of SiC over the nanotubes.
Note :
TLM left has an overlap of Al_2O_3 over TiN.
TLM right has no overlap.

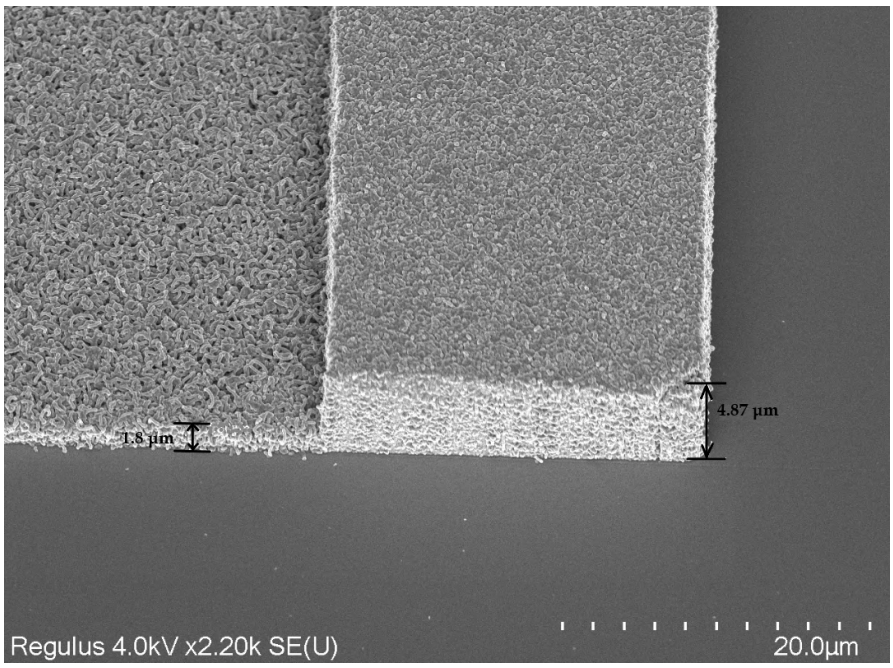


Figure D.26: Growth test structure
CNT growth time = 10 s
95 nm of a-SiC

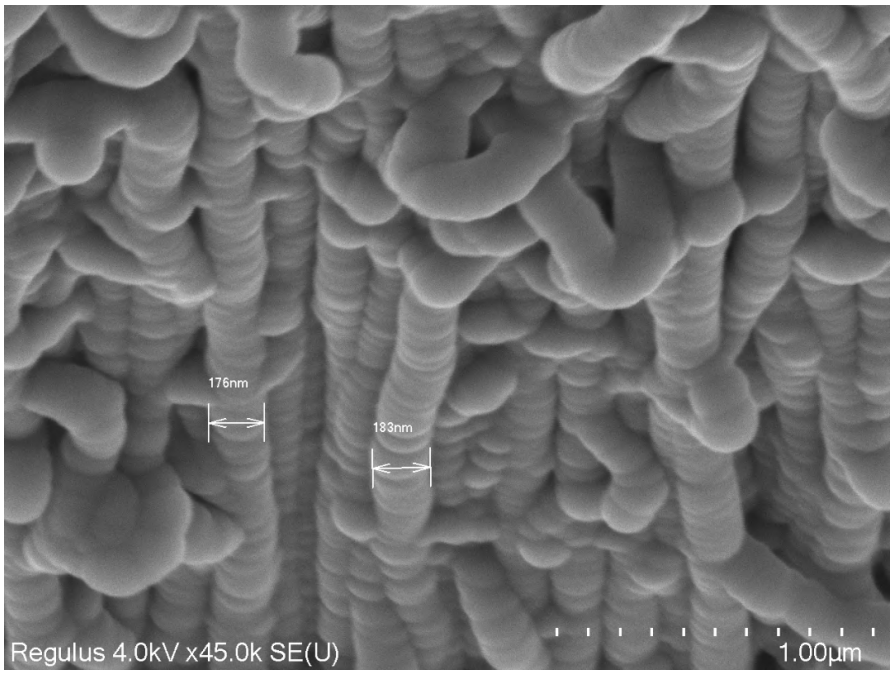


Figure D.27: Individual nanotubes coated with 90 nm a-SiC

E APPENDIX : CNT HAR ACCELEROMETER

E.1 FLOWCHART

1. **COATING**
   Use the EVG 120 wafer track to coat the wafers with resist and follow the instructions specified for this equipment. The process consists of a treatment with HMDS (hexa methyl disilazane) vapor with nitrogen as a carrier gas, spin coating with Shipley SPR3012 positive photoresist and a soft bake at 95°C for 90 seconds. Always check the temperature of the hotplate and the relative humidity (48 ± 2 %) in the room first.

   Use coating "CO 3012 – 1.4 μm – no EBR" (resist thickness: 1.400 µm).

2. **ALIGNMENT AND EXPOSURE**
   Processing is performed on the ASM PAS 5500/80 automatic wafer stepper.

   Follow the operating instructions from the manual when using this machine.

   Use the correct litho job:
   Job: litho/ZEFWAM
   Layer ID: 1
   Mask ID: COMURK
   Exposure energy: 120 mJ/cm^2.

3. **DEVELOPING**
   Use the EVG 120 wafertrack to develop the wafers and follow the instructions specified for this equipment. The process consists of a post-exposure bake at 115°C for 90 seconds, followed by a development step using Shipley MF322 developer (single puddle process) and a hard bake at 100°C for 90 seconds. Always check the temperature of the hotplates first.

   Use development recipe "Dev – SP"

4. **INSPECTION**
   Visually inspect the wafers through a microscope:
   - No resist residues are allowed.
   - Check the linewidth of the structures.
   - Check the overlay of the exposed pattern if the mask was aligned to a previous pattern on the wafer.

5. **WAFER NUMBERING**
   Use the glass pen in the lithography room to mark the wafers with the BATCH and WAFER number. Write the numbers in the photoresist, just above the wafer flat. Always do this after exposure and development! It is NOT allowed to use a metal pen or a scriber (pen with a diamond tip) for this purpose.

6. **PLASMA ETCHING: Alignment markers (URK's) into Silicon**
   Use the Trikon Omega 201 plasma etcher. Follow the operating instructions from the manual when using this machine. It is not allowed to change the process conditions and times from the etch recipe!

   Use sequence URK_NPD (with a platen temperature of 20 °C) to etch 120 nm deep ASM URK's into the Si.

	Process conditions from chamber recipe URK_ETCH:					
Step	Gasses & flows	Pressure	Platen RF	ICP RF	Platen temp.	Etch time
1. breakthrough	CF_4/O_2 = 40/20 sccm	5 mTorr	60 W	500 W	20 °C	0'10"
2. bulk etch	Cl_2/HBr = 80/40 sccm	60 mTorr	20 W	500 W	20 °C	0'40"

7. **LAYER STRIPPING**
   Strip resist Use the Tepla Plasma 300 system to remove the photoresist in an oxygen plasma. Follow the instructions specified for the Tepla stripper, and use the quartz carrier. Use Program 1: 1000 watts power and automatic endpoint detection + 2 min. overetching.

8. **CLEANING: HNO_3 99% and 69.5%**
   Clean - 10 minutes in fuming nitric acid at ambient temperature. This will dissolve organic materials. Use wet bench "HNO_3 99% (Si)" and the carrier with the red dot.

   Rinse - Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ

   Clean - 10 minutes in concentrated nitric acid at 110°C. This will dissolve metal particles. Use wet bench "HNO_3 69,5% 110C (Si)" and the carrier with the red dot.

   Rinse - Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ

   Dry Use the "Avenger Ultra-Pure 6" rinser/dryer with the standard program, and the white carrier with a red dot.

9. **WET OXIDATION: 3000 nm @ Class 100**
   Use furnace B1 to grow 30,000 Å of wet thermal oxide. Use recipe WETOXIDE with an oxidation time of 18hrs 3min 30sec at 1100°C. The oxide is used to isolate the structures from the substrate and to remove future possible backside contamination. Also a thick oxide helps in minimizing break-down. Verify thickness after.

10. **TiN METALLIZATION @ Class 100**
    Use the TRIKON SIGMA sputter coater for the deposition of TiN metal layer on the process wafers. Follow the operating instructions from the manual when using this machine. Reactively sputter 10 nm Ti for adhesion and a 50nm thick layer of TiN. Temperature = 350°C Visual inspection: the metal layer must look shiny.

    Start with a Trgtcln_Ti_350C on a dummy wafer
    Use recipe Ti_10nm_TiN_50nm_350C
    Put dummy wafers between the process wafer with recipe Ti_in_between_350C to clean the target between depositions.

11. **COATING AND BAKING @ Class 100**
    Use the EVG-120 automatic wafertrack to coat the wafers with 1.4 µm resist. The process includes a treatment with HMDS (hexamethyldisilazane) vapor with nitrogen as a carrier gas, spin coating for 30 s with Shipley SPR 3012 and prebaking for 90 seconds at 95°C. Follow the instructions specified for this equipment, and always check the temperature of the hotplate first.

    Use the program: Co - 3012 – 1400nm_no_EBR (resist thickness: 1.400 µm at 48% RV).

12. **ALIGNMENT AND EXPOSURE @ Class 100**
    Processing performed on the ASM PAS 5500/80 automatic wafer stepper.

    Follow the operating instructions from the manual when using this machine.

    Use the correct litho job:
    Job: 10mm_diesize/DIE10x10_4IMG
    Layer id: Image 1
    Mask ID: 2x2
    Exposure energy: 140 mJ/cm^2.

13. **DEVELOPMENT @ Class 100**
    After exposure a post-exposure bake at 115°C for 90 seconds is performed on the EVG-120 wafer track, followed by a development step using Shipley MF322 developer (single puddle process), and a post bake at 100°C for 90 seconds. Follow the instructions specified for this equipment, and always check the temperature of the hotplates first.

    Use program: Dev – SP

14. **INSPECTION: LINEWIDTH**
    Visually inspect the wafers through a microscope, and check line-width.

15. **PLASMA ETCH TiN**
    Use the Trikon Omega 201 plasma etcher. Follow the operating instructions from the manual when using this machine. The process conditions of the etch and passivation program may not be changed!

    Use sequence TINTISVO and set the platen temperature to 25°C (check) to etch the TiN layer, set time: 25 seconds

16. **RESIST STRIPPING @ SAL**
    Remove the resist in SAL using NMP @ 70°C (Si compatible bottle and glass-wear!). Don't perform a Tepla clean as this will damage the TiN!

    OPTION 1 : Al pads before CNT growth when low-T filling is used

17. **CLEANING PROCEDURE: HNO3 100% metal**
    Cleaning: 10 minutes in fuming nitric acid (Merck: HNO3 100% selectipur) at ambient temperature. Use wet bench "HNO3 (100%) metal" and the carrier with the yellow and red dots.
    QDR: Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
    Drying: Use the Semitool "rinser/dryer" with the standard program, and the white carrier with a black dot.
    NOTE: No 65% HNO3 cleaning step!

18. **Aluminium METALLIZATION @ Class 100**
    Use the TRIKON SIGMA sputter coat for the deposition of pure Al metal layer on the process wafers. Follow the operating instructions from the manual when using this machine. Reactively sputter 200nm Al. Temperature = XXX
    Visual inspection: the metal layer must look shiny.

    Use recipe XXX

    Perform a target clean is necessary.

19. **COATING AND BAKING @ Class 100**
    Use the EVG-120 automatic wafertrack to coat the wafers with 1.4 µm resist. The process includes a treatment with HMDS (hexamethyldisilazane) vapor with nitrogen as a carrier gas, spin coating for 30 s with Shipley SPR 3012 and prebaking for 90 seconds at 95°C. Follow the instructions specified for this equipment, and always check the temperature of the hotplate first.

Use program: Co - 3012 – 1400nm_no_EBR (resist thickness: 1.400 µm at 48% RV).

20. **ALIGNMENT AND EXPOSURE @ Class 100**
Processing performed on the ASM PAS 5500/80 automatic wafer stepper.

Follow the operating instructions from the manual when using this machine.

Use the correct litho job:
Job: 10mm_diesize/DIE10x10_4IMG
Layer id: Image 4
Mask ID: 2x2
Exposure energy: 140 mJ/cm^2.

21. **DEVELOPMENT @ Class 100**
After exposure a post-exposure bake at 115°C for 90 seconds is performed on the EVG-120 wafer track, followed by a development step using Shipley MF322 developer (single puddle process), and a post bake at 100°C for 90 seconds. Follow the instructions specified for this equipment, and always check the temperature of the hotplates first.

Use program: Dev – SP

22. **INSPECTION: LINEWIDTH**
Visually inspect the wafers through a microscope, and check line-width.

23. **WET ETCH Aluminium**
Remove the Al layer using Phosphoric acid Etching Solution (PES 77-19-04) for metals in CR100. Etch rate is XXX/min, a X min dip is enough to be sure the layer is completely removed without too much overetch. Rinse till 5 M*Omega* and dry on manual dryer.

First perform a Triton X-100 dip using the dedicated bat next to the Al etch bath. Etch till frontside is etched + 30 sec over etch
Note: etching should take place on the same day as the development, otherwise perform an additional bake in the Memert oven for 10 min

24. **RESIST STRIPPING**
Remove the resist in CR100 using the Acetone bath at 35°C, submerge wafers for at least 1 min and use transport boxes to transport the wafer to the cleaning line

25. **CLEANING PROCEDURE: HNO_3 100% metal**
Cleaning: 10 minutes in fuming nitric acid (Merck: HNO_3 100% selectipur) at ambient temperature. Use wet bench "HNO_3 (100%) metal" and the carrier with the yellow and red dots.
QDR: Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Drying: Use the Semitool "rinser/dryer" with the standard program, and the white carrier with a black dot.
NOTE: No 65% HNO_3 cleaning step!

26. **COATING AND BAKING @ Class 100**
Use the EVG-120 automatic wafertrack to coat the wafers with 1.5 µm resist. The process includes a treatment with HMDS (hexamethyldisilazane) vapor with nitrogen as a carrier gas, spin coating for 30 s with AZ Nlof2000 and prebaking for 90 seconds at 100°C. Follow the instructions specified for this equipment, and always check the temperature of the hotplate first. Use program: Co - Nlof2020 – 1500nm no EBR (resist thickness: 1.50 µm at 48% RV).

27. **ALIGNMENT AND EXPOSURE @ Class 100**
Processing performed on the ASM PAS 5500/80 automatic wafer stepper.

Follow the operating instructions from the manual when using this machine.

Use the correct litho job:
Job: 10mm_diesize/DIE10x10_4IMG
Layer id: Image 2
Mask ID: 2x2
Exposure energy: 55 mJ/cm^2.

28. **X-LINK BAKE @ Class 100**
Cross-link bake step on the EVG-120

Program: Dev – X-link only

29. **DEVELOPMENT @ Class 100**
Development step on the EVG-120 using Shipley MF322 developer (double puddle process), and a hard bake at 100 °C for 90 seconds. Follow the instructions specified for this equipment, and always check the temperature of the hotplates first.

Use program: Dev – DP 2 no PEB

30. **Al2O3 EVAPORATION @ Class 10000**
Use the CHA Solution e-beam evaporator to deposit 20nm Al2O3 directly on the TiN and Al surface. *The wafers are contaminated after this step. Use the appropriate wafer box.*

31. **Lift-off @ SAL**
Perform lift-off procedure with NMP solvent in beaker on hotplate with stirrer at 70 °C and 250 rpm. Use dedicated beaker from Cu corner

32. **RINSE & DRY @ SAL**
Rinse the wafers in DI and dry using manual dryer with special Cu chuck

33. **INSPECTION @ SAL**
Visually inspect the wafers through a microscope, check if layer remained on surface. Put paper under wafer and throw away paper after use.

34. **CLEANING PROCEDURE: HNO3 100% metal @ SAL**
Cleaning: 10 minutes in fuming nitric acid (Merck: HNO3 100% selectipur) at ambient temperature. Rinse: Rinse for 5 minutes Drying: Use the manual dryer in SAL with the Cu chuck

35. **Manual COATING AND BAKING @ PolymerLab**
Perform a manual 10 min HDMS using the Pt labelled wafer carrier

Use the Brewer science manual spinner to coat the wafers with 1.5 µm negative resist, AZ Nlof2020

Use program: XXX (resist thickness: 1.50 µm at 48% RV).

Perform a soft bake for 60 sec on 95 °C using the hotplate for contaminated wafers

36. **ALIGNMENT AND EXPOSURE @ Class 100**
Processing performed on the ASM PAS 5500/80 automatic wafer stepper. Use a special contaminated wafer carrier. Follow the operating instructions from the manual when using this machine.

Use the correct litho job:
Job: 10mm_diesize/DIE10x10_4IMG
Layer id: Image 3
Mask ID: 2x2
Exposure energy: 55 mJ/cm^2.

Also expose the edge using the open 10x10 mm reticle (box 262)
Job: g10a-edge(full), Layer id = 2, energy = 55 mJ/cm^2

37. **X-LINK BAKE @ PolymerLab**
    Perform a manual cross-link bake at 115 °C for 1:30 min on the contaminated hotplate

38. **DEVELOPMENT @ PolymerLab**
    Use the right fume hood in the polymer lab to develop your wafers using Shipley MF322 for 1:30 min. Rinse in DI for a few minutes and spin-dry using the manual spinner with the Cu chuck.

    Perform a manual hard bake at 100 °C for 2 min on the contaminated hotplate

39. **INSPECTION @ Class 100**
    Visually inspect the wafers through a microscope, check if layer remained on surface. Put paper under wafer and throw away paper after use.

40. **Fe CATALYST EVAPORATION @ Class 10000**
    Use the CHA Solution e-beam evaporator to deposit 2nm Fe directly on the TiN and Al surface.

41. **Lift-off @ SAL**
    Perform lift-off procedure with NMP solvent in beaker on hotplate with stirrer at 70 °C and 250 rpm. Use dedicated beaker from Cu corner

42. **RINSE & DRY @ SAL**
    Rinse the wafers in DI and dry using manual dryer with special Cu chuck

43. **INSPECTION @ SAL**
    Visually inspect the wafers through a microscope, check if catalyst layer remained on surface. Put paper under wafer and throw away paper after use.

44. **CNT growth @ Class 10000**
    Use the AIXTRON BlackMagic Pro to grow CNTs using LPCVD at 600°C for Fe catalyst layers.

    Use recipe: lpcvd_600_vartime / lpcvd_550_vartime (for Al pads)

    Recipe includes an activation step (3 min) in H2 environment at 500 °C, followed by CNT growth using 700/50 sccm H_2/C_2H_2 at 80 mbar for XX minutes at 600 °C.
    Target CNT height $\approx$ 15 microns

    The reason why we want growth on both surfaces is to address the problem of contacting and electrical isolation of the contact pads. A part of the TiN layer is in contact with the tubes for the purpose of applying potential difference/pumping current. Al_2O_3 layer electrically isolates the two contact pads from shorting.

45. **CNT coating using LPCVD @ Class 10000**
    Use Tempress LPCVD F3 to deposit Silicon Carbide over the CNT forests. (only step to be PAC approved). The wafer can be cut into pieces and placed on a carrier to ensure conformal coating.

    Recipe: 1st_SiC (a-SiC), target: 20-40 nm thickness

    OR

46. **CNT coating using ALD @ Kavli**
    Use the Oxford Instruments ALD at Kavli to deposit 50 nm of Al_2O_3

    Recipe: XXX (Al_2O_3), target: 50 nm thickness

Pattern floor layer to protect TiN

47. **Spray coating @ Class 100**
Use the EVG101 to spray coat positive resist on your wafer. Use the chuck for contaminated wafers.

48. **ALIGNMENT AND EXPOSURE @ Class 100**
Processing performed on the SUSS Microtec contact aligner.
Use a special contaminated wafer carrier.
Expose the SiC protection layer foil mask.
Exposure time : 50s

49. **DEVELOPMENT @ PolymerLab**
Use the right fume hood in the polymer lab to develop your wafers using AZ-400K for xx min. Rinse in DI for a few minutes and spin-dry using the manual spinner with the Cu chuck.

    Perform a manual hard bake at 100 °C for 2 min on the contaminated hotplate

50. **Plasma etch of the floor layer - AMS110 @ Class 10000 / Sentech F1 @ Kavli**
Use the Adixen AMS110 to remove the floor layer Recipe: XXX (a-SiC), target: 20/50 nm thickness

51. **Resist strip @ PolymerLab**
Use the right fume hood in the polymer lab to remove the PR using acetone and IPA.

52. **CLEANING PROCEDURE: HNO_3 100% metal @ SAL**
Cleaning: 10 minutes in fuming nitric acid (Merck: HNO_3 100% selectipur) at ambient temperature. Rinse: Rinse for 5 minutes Drying: Use the manual dryer in SAL with the Cu chuck

OPTION 2 : Au pads after LPCVD

53. **Spray coating @ Class 100**
Use the EVG101 to spray coat negative resist on your wafer. Use the chuck for contaminated wafers.

54. **ALIGNMENT AND EXPOSURE @ Class 100**
Processing performed on the ASM PAS 5500/80 automatic wafer stepper. Use a special contaminated wafer carrier. Follow the operating instructions from the manual when using this machine.

    Use the correct litho job:
    Job: 10mm_diesize/DIE10x10_4IMG
    Layer id: Image 4
    Mask ID: 2x2
    Exposure energy: 900 mJ/cm^2.

55. **DEVELOPMENT @ PolymerLab**
Use the right fume hood in the polymer lab to develop your wafers using AZ-400K for xx min. Rinse in DI for a few minutes and spin-dry using the manual spinner with the Cu chuck.

    Perform a manual hard bake at 100 °C for 2 min on the contaminated hotplate

56. **INSPECTION @ Class 100**
Visually inspect the wafers through a microscope, check if layer remained on surface. Put paper under wafer and throw away paper after use.

57. **Contact metal evaporation @ Class 10000**
Use the CHA Solution e-beam evaporator to deposit 10/100 nm of Cr/Au

58. **Lift-off @ SAL**
Perform lift-off procedure with NMP solvent in beaker on hotplate with stirrer at 70 °C and 250 rpm. Use dedicated beaker from Cu corner

59. **RINSE & DRY @ SAL**
Rinse the wafers in DI and dry using manual dryer with special Cu chuck

60. **INSPECTION @ SAL**
Visually inspect the wafers through a microscope, check if catalyst layer remained on surface. Put paper under wafer and throw away paper after use.

OPTION 3 : Al pads after LPCVD SiC

61. **Aluminium METALLIZATION @ Class 100**
Use the TRIKON SIGMA sputter coat for the deposition of pure Al metal layer on the process wafers. Follow the operating instructions from the manual when using this machine. Reactively sputter 1μm of Al. Temperature = 20/50°C Visual inspection: the metal layer must look shiny. Use the copper cassette and a contaminated wafer carrier.

Use recipe XXX

62. **Spray coating @ Class 100**
Use the EVG101 to spray coat positive resist on your wafer. Use the chuck for contaminated wafers.

63. **ALIGNMENT AND EXPOSURE @ Class 100**
Processing performed on the ASM PAS 5500/80 automatic wafer stepper. Use a special contaminated wafer carrier. Follow the operating instructions from the manual when using this machine.

Use the correct litho job:
Job: 10mm_diesize/DIE10x10_4IMG
Layer id: Image 4
Mask ID: 2x2
Exposure energy: 900 mJ/cm^2.

64. **DEVELOPMENT @ PolymerLab**
Use the right fume hood in the polymer lab to develop your wafers using AZ-400K for xx min. Rinse in DI for a few minutes and spin-dry using the manual spinner with the Cu chuck.

Perform a manual hard bake at 100 °C for 2 min on the contaminated hotplate

65. **INSPECTION @ Class 100**
Visually inspect the wafers through a microscope, check if layer remained on surface. Put paper under wafer and throw away paper after use.

66. **WET ETCH Aluminium @ SAL**
Remove the Al layer using Phosphoric acid Etching Solution (PES 77-19-04 @ 35°C) in SAL. Etch rate is XXX/min, a X min dip is enough to be sure the layer is completely removed without too much overetch. Rinse till 5 MOhm and dry on manual dryer.

First perform a Triton X-100 dip using the dedicated bath Etch till frontside is etched + 30 sec over etch Note: etching should take place on the same day as the development, otherwise perform an additional bake in the Memert oven for 10 min

67. **Resist strip @ PolymerLab**
Use the right fume hood in the polymer lab to remove the PR using acetone and IPA.

68. **CLEANING PROCEDURE: HNO_3 100% metal @ SAL**
    Cleaning: 10 minutes in fuming nitric acid (Merck: HNO_3 100% selectipur) at ambient temperature. Rinse: Rinse for 5 minutes Drying: Use the manual dryer in SAL with the Cu chuck

69. **INSPECTION @ SAL**
    Visually inspect the wafers through a microscope, check if catalyst layer remained on surface. Put paper under wafer and throw away paper after use.

70. **Release of the structures @ CR100**
    The structures are released by using the Vapour HF tool. Use a moderate recipe (Recipe 2) to etch approximately 4-5 microns of the oxide.
    OR
    BHF(1:7) can be used for CNT filled with LPCVD a-SiC.
    Use plastic beakers

F APPENDIX : MEASUREMENT RESULTS

F.1 VDP MEASUREMENTS

Here we see the detailed VdP tests performed on a variety of samples. The equations to calculate the electrical parameters are found in section 4.1.2. Tests are performed using *Cascade 33 microtech* probe station.
Force current $-50\,\mu A$ to $+50\,\mu A$.

Table 1 : VdP measurement results on various samples

Sample no.	CNT height (μm)	a-SiC thickness (nm)	VdP width (μm)	R_{avg} (Ω)	$R_{\square}$ (Ω/sq)	Resistivity (ρ) ($\Omega.m$)
1	20	30	5	78.25	350.12	0.007
			10	77.89	353.02	0.007
			20	87.99	398.8	0.0079
2	50	-	5	26.6	120.56	0.006
			10	27.6	125.5	0.0062
			20	29.59	134.11	0.0067
3	42	40	5	22.85	103.56	0.0043
			10	22.2	100.61	0.0042
			20	22.6	102.43	0.0043
4	10	-	5	193.7	877.9	0.0087
			10	192.9	874.29	0.0087
			20	200.5	908.7	0.009
5	10	90	5	159.7	723.8	0.0072
			10	142.4	645.4	0.0064
			20	154.1	698.4	0.0069

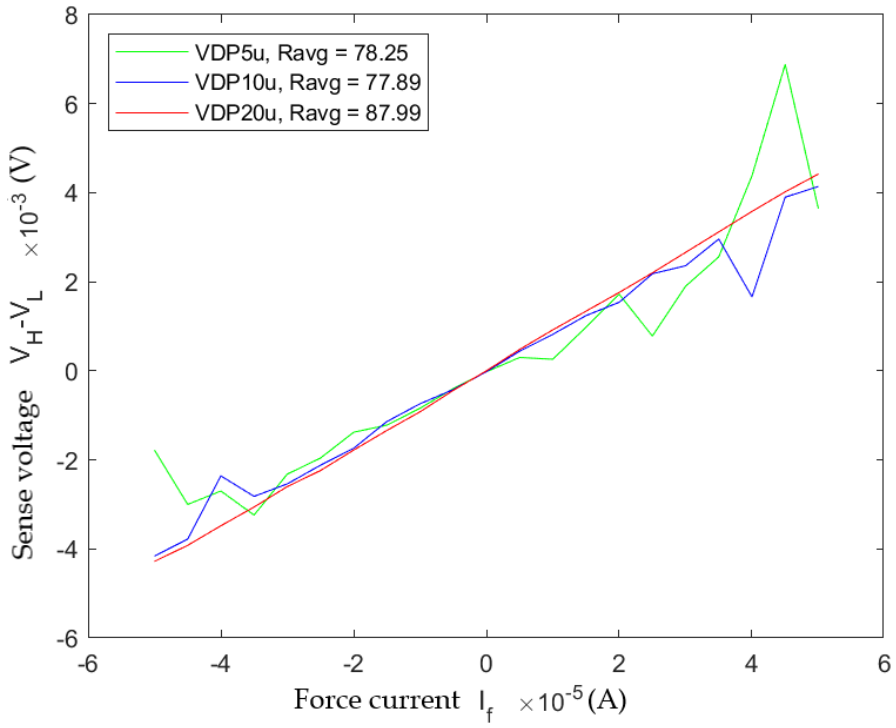


Figure F.1: Sense voltage vs force current
CNT height 20 μm
a-SiC thickness 30 nm

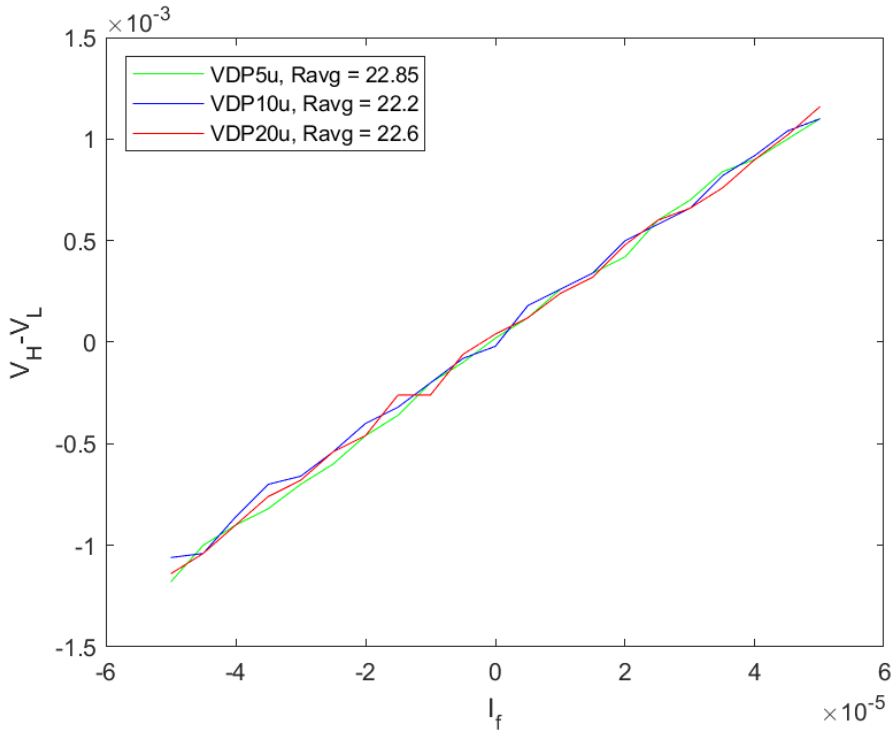


Figure F.2: Sense voltage vs. force current
CNT height 42 μm
a-SiC thickness 40 nm

F.2 TLM MEASUREMENTS

Here we see the detailed TLM tests performed on a variety of samples. The equations to calculate the electrical parameters are found in section 4.1.2. Tests are performed using *Cascade 33 microtech* probe station.
Force current $-50\,\mu A$ to $+50\,\mu A$.

Table 2 : TLM measurement results on various samples

Sample no.	CNT height (μm)	a-SiC thickness (nm)	TLM left length (μm)	R_{avg} (Ω)	Resistance per unit length (Ω/m)	Contact resistance (R_C) (Ω)
1	50	-	190 485 690 885	1483.8 3581.1 4489 6343.2	$6.98 * 10^6$	84.75
2	42	40	190 485 690 885	1511.5 3565.3 4594.2 6233.1	$6.28 * 10^6$	123.8
3	10	-	190 485 690 885	8707 21600 30380 39110	$4.36 * 10^7$	196.3
4	10	90	190 485 690 885	6601.5 16529 23978 30610	$3.46 * 10^7$	-36.3
5	16	90	190 485 690 885	5408.6 14036 20626 26319	$3.024 * 10^7$	-207.2

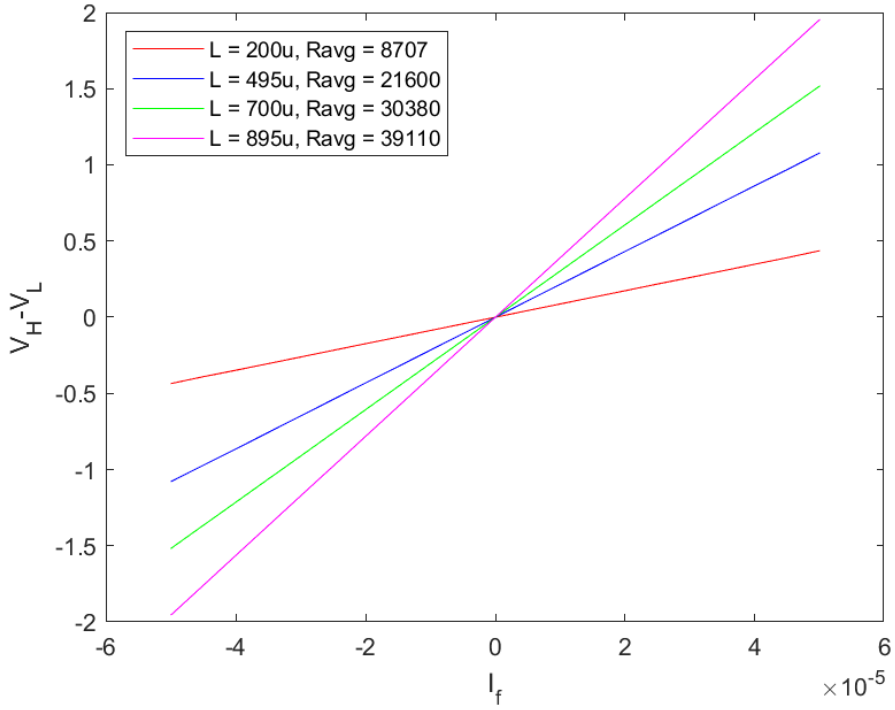


Figure F.3: TLM left
Sense voltage vs. force current
CNT height 10 μm
NO a-SiC

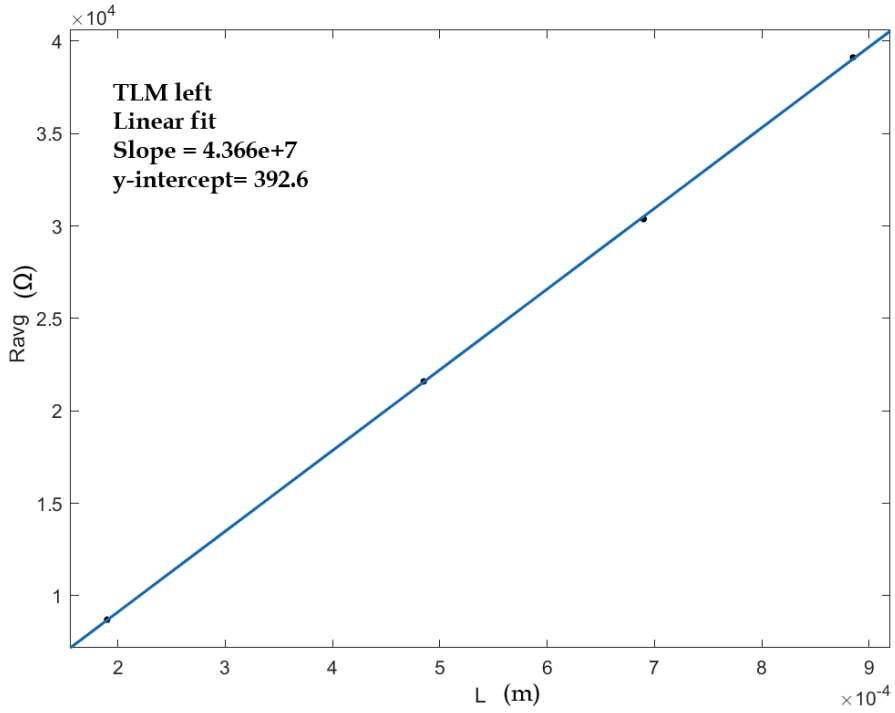


Figure F.4: TLM left
Resistance vs length
CNT height 10 μm
NO a-SiC

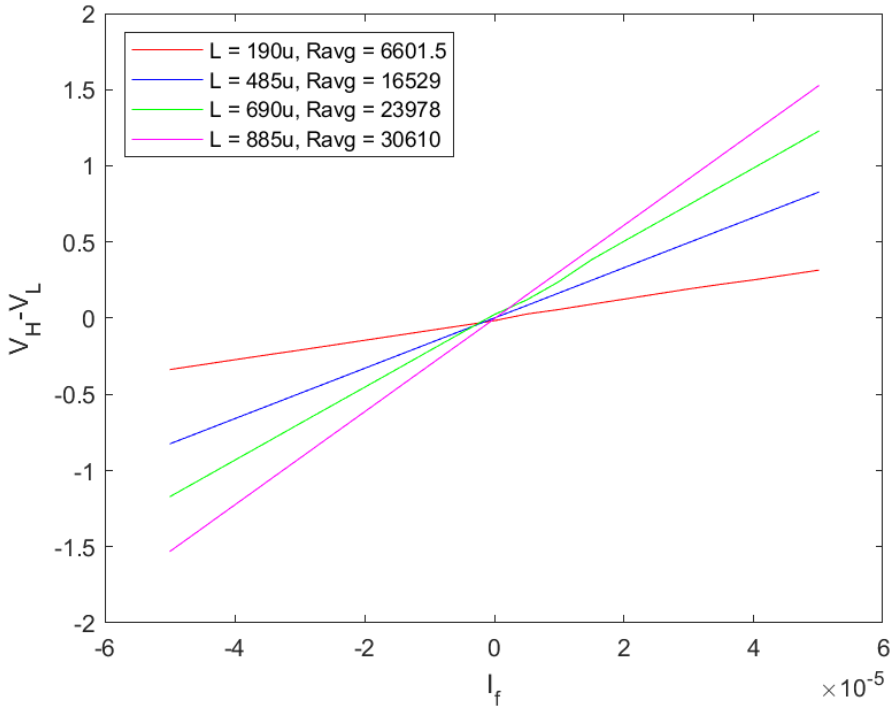


Figure F.5: TLM left
Sense voltage vs. force current
CNT height 10 μm
a-SiC thickness 90 nm

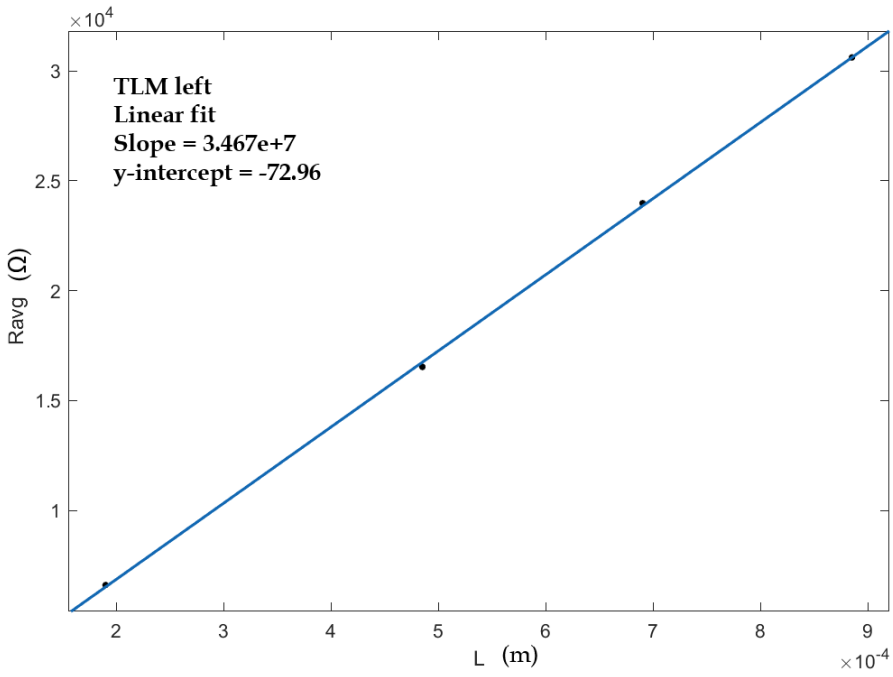


Figure F.6: TLM left
Resistance vs length
CNT height 10 μm
a-SiC thickness 90 nm

F.3 ELM MEASUREMENTS

Here we see the detailed ELM tests performed on a variety of samples. The equations to calculate the electrical parameters are found in section 4.1.2. Tests are performed using *Cascade 33 microtech* probe station.
Force current $-50\,\mu A$ to $+50\,\mu A$.

Table 3 : ELM measurement results on various samples

Sample no.	CNT height (μm)	a-SiC thickness (nm)	ELM width (μm)	R_{avg} (Ω)	$R_{\square}$ (Ω/sq)	Resistivity (ρ) ($\Omega.m$)
1	16	90	5	16140	278.27	0.0044
			10	8724	300.82	0.0048
			20	4760	328.27	0.0052
2	50	-	5	3684	63.5	0.0031
			10	1926	66.4	0.0033
			20	968.8	66.8	0.0033
3	42	40	5	4288	73.93	0.0031
			10	2031	70.34	0.0029
			20	1069	73.72	0.003
4	10	-	5	34810	600	0.006
			10	17420	600.68	0.006
			20	8637	595.65	0.0059
5	10	90	5	20540	354.1	0.0035
			10	10580	364.8	0.0036
			20	5321	366.9	0.0036

Table 4 : TCR measurements
CNT height 42 µm, a-SiC 40 nm

ELM width (μm)	Resistance (Ω)			
	$21°C$	$100°C$	$150°C$	$200°C$
5	3834	3581	3450	3339
10	1939	1826	1779	1742
20	973.6	923.5	909.6	894.5

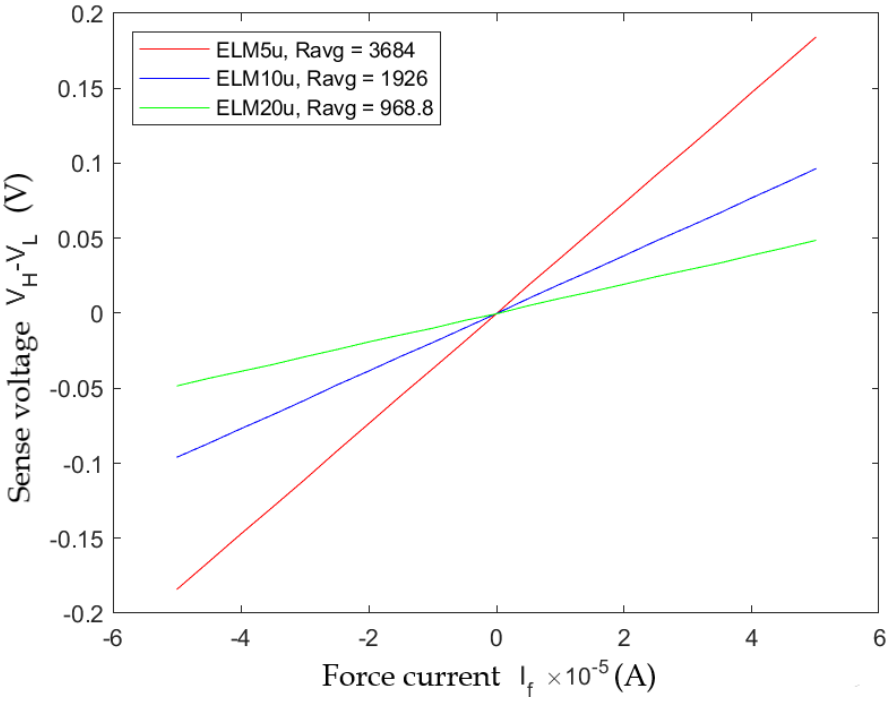


Figure F.7: ELM VI plot
CNT height 50 μm
NO a-SiC

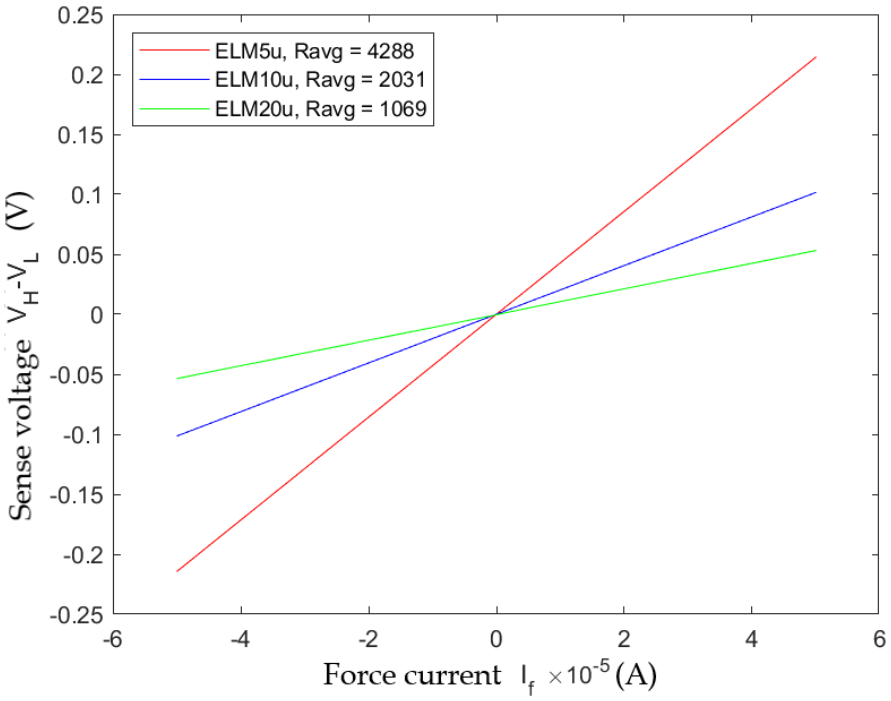


Figure F.8: ELM VI plot
CNT height 42 μm
a-SiC thickness 40 nm

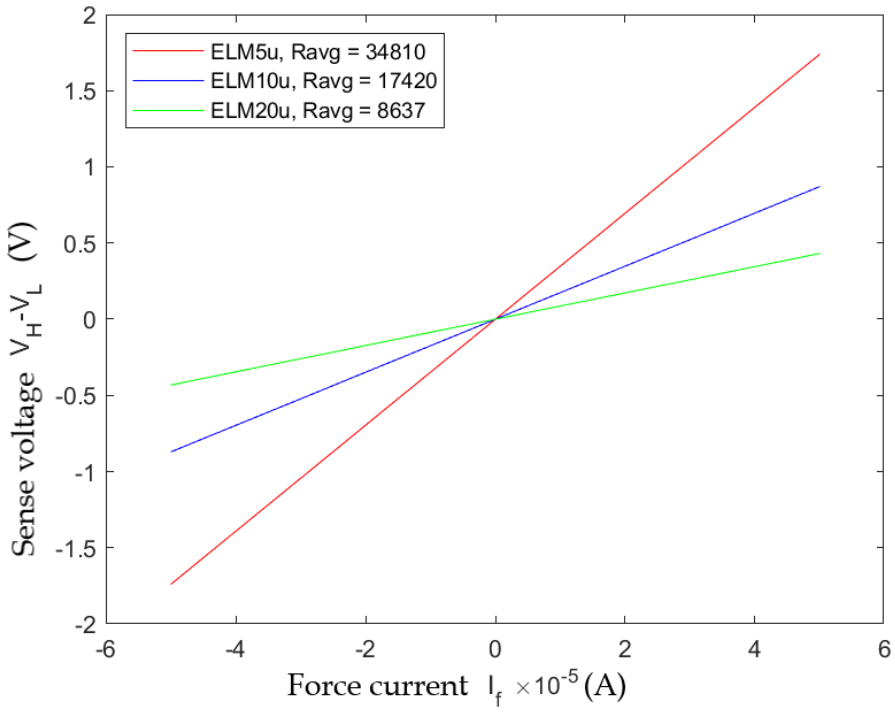


Figure F.9: ELM VI plot
CNT height 10 μm
NO a-SiC

F.4 TEMPERATURE RESILIENCE TEST

In this test, a sample was heated from room temperature to 700°*C* using the *Nextron microprobe station*. This was performed to check if the structure could breakdown at high temperature. The sample was heated in steps of 100°*C* in 10 *min* intervals. The results show that the accelerometer is able to withstand atleast 700°*C* without breakage. However, it can be observed from the images that above 600°*C* the Al pads being to melt.

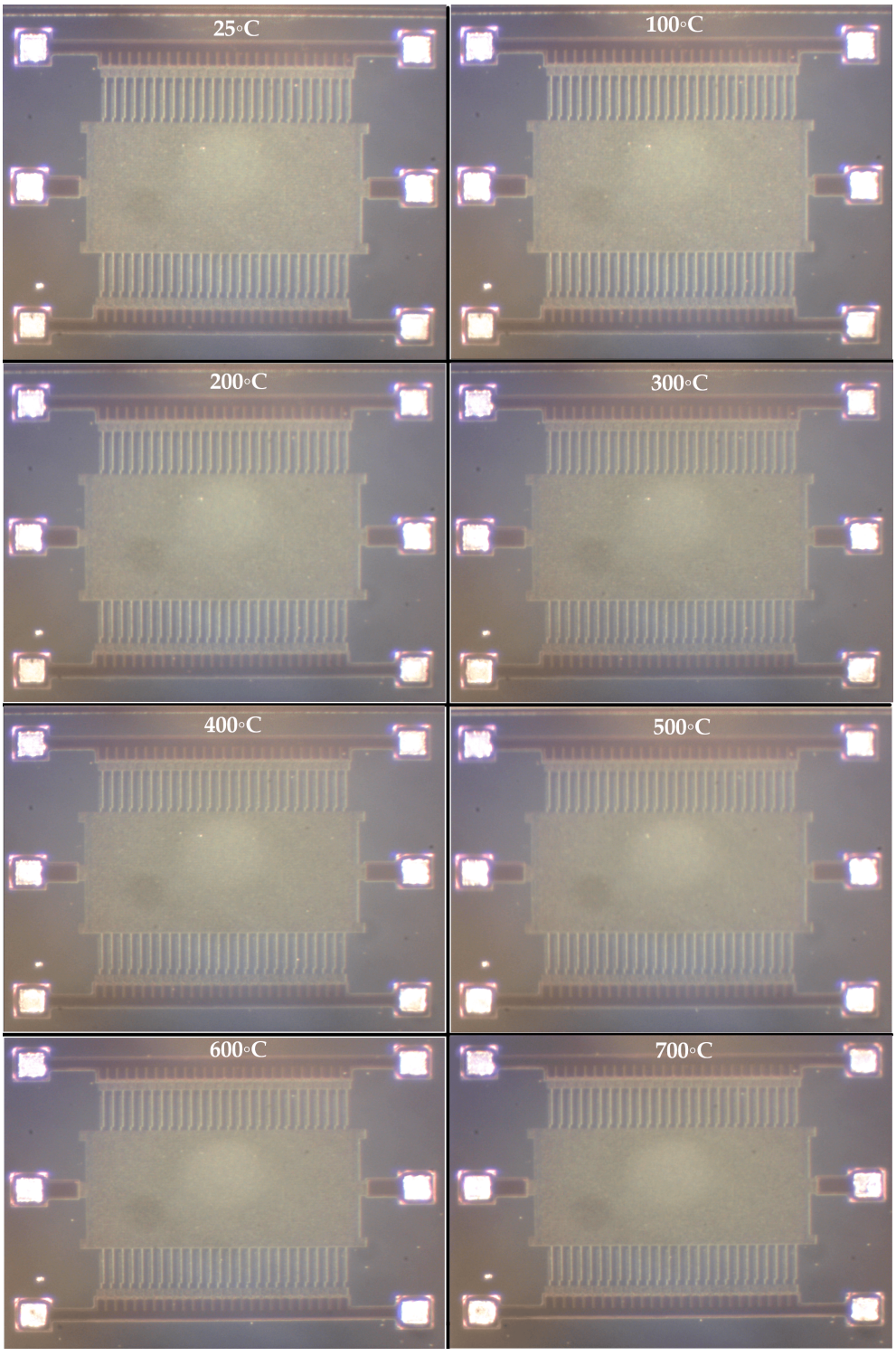


Figure F.10: Microprobe temperature resilience testing on a sample