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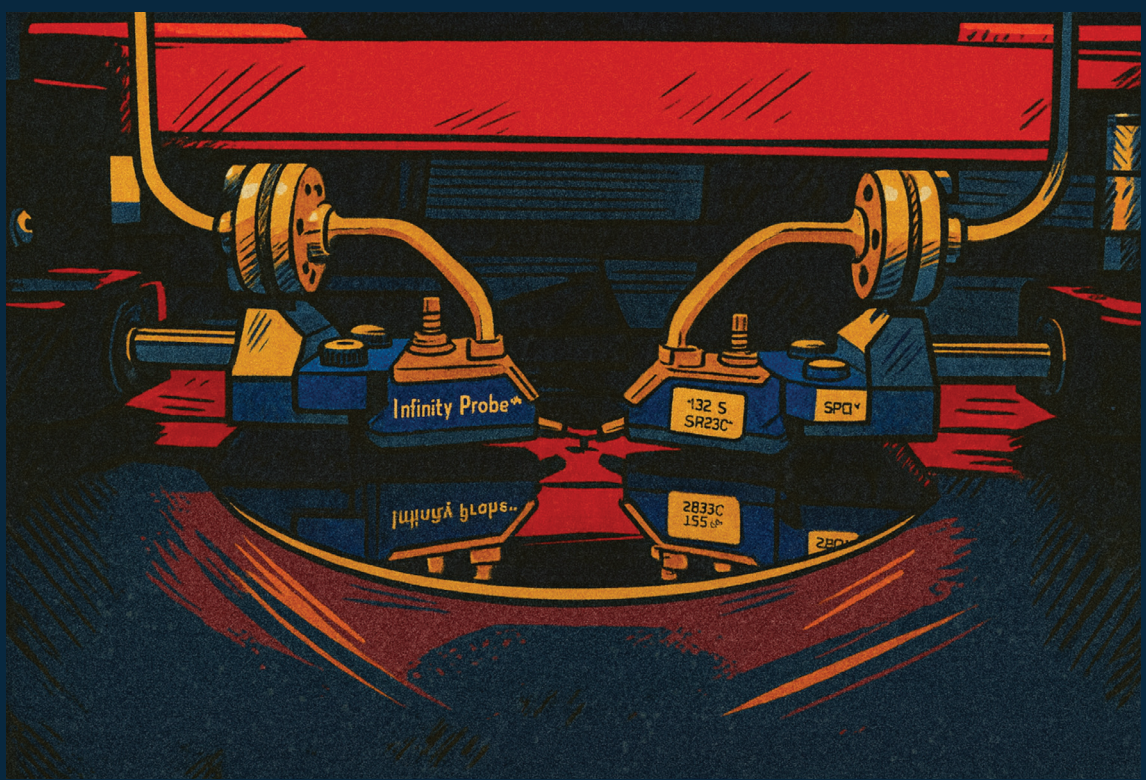

CARMINE DE MARTINO

Novel Calibration Approaches and Large Signal Measurement Techniques for Sub-THz Devices Characterization

NOVEL CALIBRATION APPROACHES AND LARGE SIGNAL MEASUREMENT TECHNIQUES FOR SUB-THZ DEVICES CHARACTERIZATION

Dissertation

for the purpose of obtaining the degree of doctor
at Delft University of Technology
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chair of the Board for Doctorates
to be defended publicly on
Monday 26 January 2026 at 12:30 o'clock

by

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Keywords: Broadband characterization, CMOS, device model, mm-wave, on-wafer calibration, load-pull, Large-Signal device characterization, 3D EM Simulation, de-embedding, VNA, small-signal sub-THz.

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Everybody is a genius. But if you judge a fish by its ability to climb a tree, it will live its whole life believing that it is stupid.

Albert Einstein

To my wife Annarita

To my father

To my family

CONTENTS

1

INTRODUCTION

1.1. TOWARDS SMART ENVIRONMENTS

Throughout history, technology has consistently supported humanity in accomplishing daily tasks, making them more efficient and less time-consuming. This capability of enabling tasks that were previously complex or even impossible, through technology, has driven human development. This interaction between humans and machines has existed since the Stone Age (see fig. 1.1) and has evolved into the computer age, where humans provide commands, and machines execute them.

However, since the dawn of the 21st century, this relationship has undergone a significant transformation. From a state of total human control over machines (as seen with industrial robots and standard cars), it has shifted towards autonomous machine control, exemplified by systems with decision-making capabilities, such as Artificial Intelligence (AI) and autonomous vehicles. At this point, the surrounding environment can no longer be considered inanimate or passive. Instead, it is now active, assisting and guiding humans autonomously. This phenomenon defines what we now refer to as smart environments. In fact, common definitions of smart environments are the following:

"A smart environment is an intelligent agent that perceives the state of the resident and the physical surroundings using sensors and acts on the environment using controllers in such a way that the specified performance measure is optimized. It is an automated management environment that is based on the continuous communication between sensors connected via the internet. " [2]

According to these definitions, for the environment to be considered "smart," it must possess the following capabilities:

- Sensing capabilities: to derive information from the surroundings.
- Communication capabilities: distribute the information to other machines or computational units.
- Data analysis and control capabilities: to apply data-driven decision-making processes.

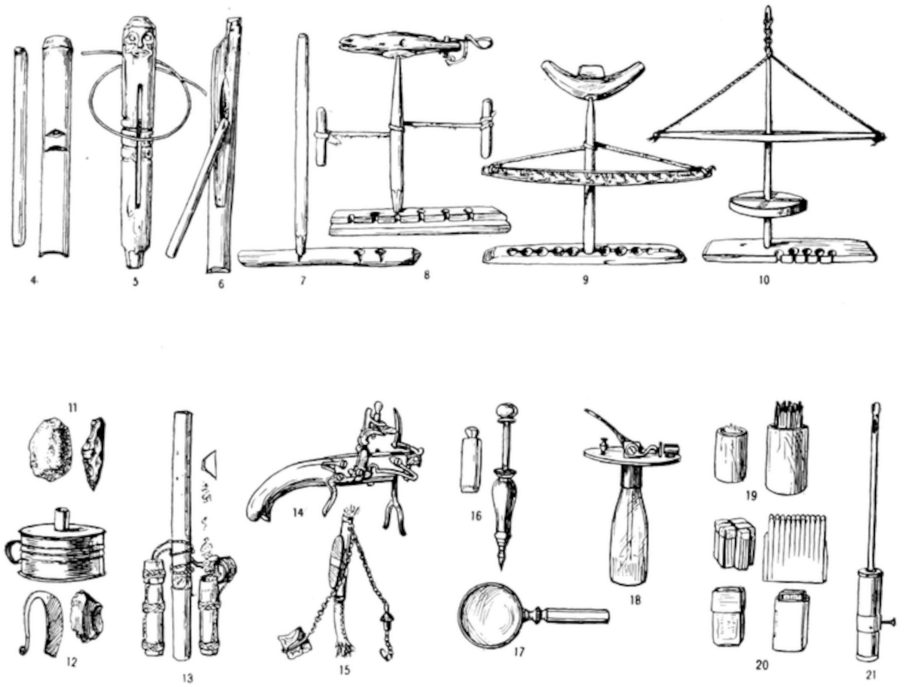


Figure 1.1.: History of fire-making tools: 4) Fire saw; 5) Fire thong; 6) Fire plow; 7) Fire drill 8) Fire drill; 9) Fire drill; 10) Fire drill; 11) Strike-a-light 12) Strike-a-light; 13) Strike-a-light; 14) Tinder pistol 15) Strike-a-light; 16) Fire syringe; 17) Lens; 18) Hydrogen lamp; 19) Match light box; 20) Match; 21) Electric gas light [1].

In order to fulfill the vision of smart environments, currently, the capabilities of the various machines to communicate with the processing hubs present in the environment are being perceived as a possible bottleneck due to the limited resources available in the frequency spectrum.

1.2. THE MM-WAVE AND TERAHERTZ SPECTRUM ADVANTAGES

To highlight thus bottleneck of wireless communication we need to recall the fundamental theorem expressing the capacity of a communication channel. The Shannon-Hartley theorem establishes the maximum amount of information that can be transmitted through a channel per unit of time as a function of its bandwidth (eq. (1.1)).

$$C = B\log\left(1+\frac{S}{N}\right) \tag{1.1}$$

Where:

- C is the channel's capacity,

- B is the bandwidth,
- S is the signal power,
- N is the noise power.

Equation (1.1) highlights the fact that one of the most advocated ways to increase the data rate is to expand the signal/channel's bandwidth. When reviewing the U.S. frequency allocation plan (fig. 1.2), it becomes evident that the available bandwidth to be allocated for future applications, below a few tens of GHz is limited, leaving little room for expansion. This limitation has driven increased interest in the mm-wave spectrum over recent years.

Moreover, in the future envisioned smart environments, both the sensing and communication capabilities are merging, and new technologies exploiting waveforms capable of communicating while sensing the environment are being developed [3]. In this regard, it is also useful to consider the advantages that the sub-THz spectrum offers for sensing applications. To do this in a simple and intuitive way, it is helpful to recall the relationship between signal bandwidth and resolution of an Frequency-Modulated Continuous Wave (FMCW) sensor capable to identify the distance of an object, i.e., the Radio Detection And Ranging (RADAR) sensor. The resolution of a RADAR is directly proportional to wavelength, as shown by eq. (1.2) [4].

$$\begin{cases} \Delta R = \dfrac{c}{2B} \propto \dfrac{\lambda}{2} \\ \Theta = \dfrac{\lambda}{D} \end{cases} \tag{1.2}$$

Where:

- ΔR is the radar resolution,
- c is the speed of light,
- B is the bandwidth,
- λ is the wavelength,
- Θ is the angular resolution,
- D is the aperture diameter.

This proportionality indicates that shorter wavelengths, such as those in the sub-THz range, offer better resolution, which explains the growing research and commercial interest in the sub-THz spectrum. While the advantages of the higher-frequency spectrum are evident, they come with significant challenges. Operating in frequencies above 100 GHz requires advanced hardware with highly accurate device models to support circuit design for the fundamental components of communication systems, such as amplifiers, antennas, and the entire up and down-converting chains. Furthermore, these system need to provide high spectral purity and energy efficiency. Consequently,today, much focus is being put in developing wide-band and high-efficiency Radio Frequency (RF)

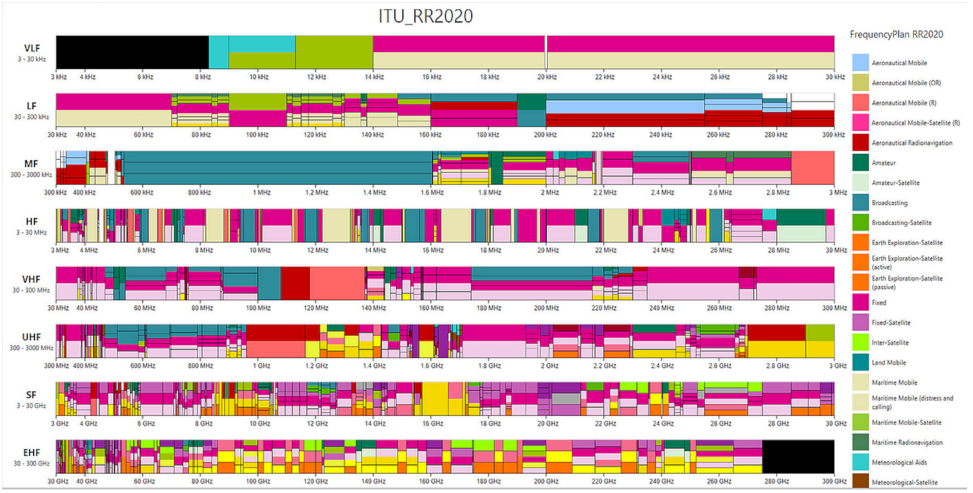


Figure 1.2.: International Telecommunication Union (ITU), Radio Regulations 2020.

transceivers. The two key silicon-based technologies, which can enable low-cost large-volume fabrication, i.e., Complementary Metal-Oxide-Semiconductor (CMOS) and Silicon-Germanium (SiGe) Heterojunction Bipolar Transistors (HBTs) have in the last decade improved their capabilities for realizing high-performance circuits at sub-THz. Nevertheless, understanding, characterizing and properly modeling the components and circuits in these technologies at application-relevant frequencies is a crucial step for enabling the (commercial) realization of smart environment scenarios.

1.3. THESIS OBJECTIVE

The work presented in this thesis aims move beyond the the boundaries of the state of the art by addressing the following research questions:

- How to combine broadband calibration approaches and de-embedding techniques to minimize the model to hardware error during validation measurements up to 325GHz. [Chapter 3]

- How to define a structured design flow with clear objective metrics to allow the evaluation of the calibration/de-embedding approach prior to silicon fabrication. [Chapter 3]

- How to quantify the sub-mm-wave specific hardware limitations and to enable new large-signal design/verification test-benches that overcome these limitations. [Chapter 5]

1.4. THESIS OUTLINE

The structure of this thesis is organized as follows:

- **Chapter 2** provides an introduction to the fundamentals of RF device characterization, focusing on the specific challenges that arise when transitioning to higher frequencies. This chapter discusses how measurements and characterizations are affected and details the limitations encountered when operating in these frequency ranges.
- **Chapter 3** presents a comprehensive procedure for designing an Metal 1 (M1) test fixture using an automated script-based approach. This approach converts a design that adheres to all required design rules into a format that is compatible with a Three-Dimensional (3D) Electromagnetic (EM) simulator. The chapter then outlines strategies to automatically import the structure under test and configure the 3D EM simulator to achieve accurate and consistent simulation results. Furthermore, it demonstrates the simulation results of the calibration standards and evaluates the accuracy of these results when applied to a calibration procedure. Finally, it discusses how the accuracy of the calibration propagates to the intrinsic parameters of active devices, presenting this propagation as error bounds.
- **Chapter 4** presents two enhancements that can be implemented when employing the M1 test fixture discussed in chapter 3. Specifically, it introduces a method to mitigate the effect of Electrostatic Discharge (ESD) antenna diodes, which must be integrated into the test fixture to prevent device damage during fabrication. Additionally, this chapter presents the development of a power calibration transfer device, enabling power calibration to be conducted directly on the wafer.
- **Chapter 5** details the design and implementation of a measurement setup capable of performing fundamental Continuous Wave (CW) active load-pull measurements in the mm-wave frequency range. After explaining the hardware and software strategies involved in building the system, the chapter presents measurement results obtained from various active devices tested with this setup.
- **Chapter 6** explores additional applications of the measurement setup described in chapter 5. It demonstrates how a modified version of the load-pull setup can be used to generate two phase-coherent sources for evaluating active feed-on-chip antennas. The second part of the chapter outlines a method for using the same setup to estimate device figures of merit, such as the Error Vector Magnitude (EVM), which cannot be measured directly at these frequencies.
- **Chapter 7** provides the concluding remarks of this thesis. It summarizes the main findings and offers recommendations for future research aimed at improving the methodologies and outcomes presented in this dissertation.

2

RF DEVICE CHARACTERIZATION AT MM-WAVES

2.1. INTRODUCTION

The characterization of active devices aims at capturing the component behavior under various conditions in order to extract and validate their model representation to support the development of current and future applications. For this reason, the characterization process needs to cover a broad spectrum, typically requiring multiple measurement setups to address different operating/bias regions and include the accurate extraction of a wide range of metrics which are used to describe the behavior of a Device Under Test (DUT). Four key response characteristics are particularly significant in evaluating semiconductor device behavior:

- *DC*: Characterizing the static behavior of a device under specific bias conditions.
- *Small-signal*: Assessing the device's response to a small perturbation around a DC operating point.
- *Noise*: Quantifying the device's contribution to the overall noise in the output signal.
- *Large-signal*: Describing the device's behavior under conditions where it no longer exhibits linear characteristics.

The data obtained from the characterization efforts described above can be used to evaluate semiconductor device performance by means of various Figure of Merits (FoMs), such as β_0, Noise Figure (NF), and $\mathrm{P_{1dB}}$, thereby enabling straightforward comparisons across different technologies or device implementations [5]. Additionally, the data supports the development of compact models, either by parameter extraction based on the collected data or more directly through the construction of database models using advanced techniques, such as (AI-based) data fitting. These models allow for the simulation of device performance when integrated into circuits. As discussed in the introduction to this dissertation, transitioning to the (sub)mm-wave frequency range offers considerable advantages for next-generation applications but also introduces substantial

challenges throughout the entire circuit/system development process in order to lead to a final prototype fulfilling the application requirements. This chapter will examine the field of RF active device characterization, highlighting the state-of-the-art techniques and identifying limitations specific to the mm-wave frequency range for the small-signal and large-signal characterization aspects.

2.2. RF ACTIVE DEVICE CHARACTERIZATION

Transistors are inherently nonlinear devices, but under certain conditions, they can be approximated as linear. These conditions determine whether the transistor operates in a small-signal or large-signal regime. From the perspective of RF characterization, these two operational regimes are characterized by distinct FoMs, necessitating different measurement techniques. In the small-signal regime, the behavior of the DUT remains unaffected by variations in signal magnitude allowing measurements to focus on signal ratios, and variations in loading conditions can be treated as linear allowing post-measurement data manipulation by linear operators. Conversely, in the large-signal regime, the signal magnitude significantly influences the DUT's response, necessitating the measurement of individual waves rather than their ratios. Moreover, the impact of loading conditions can no longer be evaluated through linear data manipulation after the measurement but it requires an effective tuning of these impedances during the characterization phase.

2.2.1. S-PARAMETER DEFINITION AND TEST BENCH

In high-frequency characterization, it is common practice to describe the input-to-output relationships of active devices using a two-port black-box matrix representation (fig. 2.1). The most suitable characterization method at RF frequencies employs the S-matrix (scattering matrix), as other parameter sets, such as Z-parameters and Y-parameters, necessitate open or short circuited-conditions at the measurement reference plane of the DUT. Achieving open and short conditions at RF frequencies presents significant challenges due to the inevitable parasitics, which often compel the use of RF stubs that are intrinsically frequency-dependent. Moreover, imposing an open or short circuited-conditions on the input or output of a transistor may induce oscillations. Another advantage of utilizing S-parameters is that they are based on traveling waves, which maintain a constant magnitude along a lossless transmission line [6], thereby allowing easy shifting of the reference plane by applying a phase delay or anticipation to the traveling wave. The black-box representation of the device is thus expressed as the incident and reflected (normalized) traveling waves (fig. 2.2). This is regarded as the de-facto standard representation of an N-port high-frequency device, as briefly described in eq. (2.1) for a 2 port network.

$$\left.\begin{aligned} b_1 &= S_{11}a_1 + S_{12}a_2 \\ b_2 &= S_{21}a_1 + S_{22}a_2 \end{aligned}\right\} \Longrightarrow \begin{aligned} S_{11} &= \left.\frac{b_1}{a_1}\right|_{a_2=0} & S_{12} &= \left.\frac{b_1}{a_2}\right|_{a_1=0} \\ S_{21} &= \left.\frac{b_2}{a_1}\right|_{a_2=0} & S_{22} &= \left.\frac{b_2}{a_2}\right|_{a_1=0} \end{aligned} \tag{2.1}$$

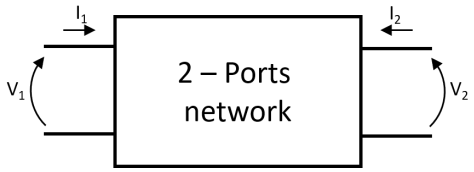


Figure 2.1.: Two-port network described using voltage and current representation.

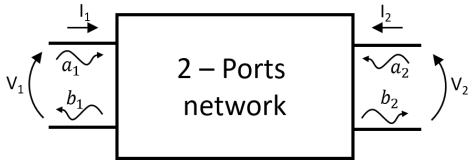


Figure 2.2.: Two-port network described using the traveling waves representation.

Where a_1 and a_2 are the incident waves while b_1 and b_2 represent the reflected waves at ports one and two, respectively. Considering a real port normalized impedance Z_n, these waves are defined as follows:

$$a_n = \left.\frac{V_n^+}{\sqrt{Z_n}}\right|_{n=1,2;Z_n real} \qquad b_n = \left.\frac{V_n^-}{\sqrt{Z_n}}\right|_{n=1,2;Z_n real} \tag{2.2}$$

The instrument employed to measure the S-parameters is the Vector Network Analyzer (VNA). The core of this instrument, irrespective of the specific implementation by different vendors, is based on a constant Intermediate Frequency (IF) heterodyne reflectometer, which is illustrated in fig. 2.3. This figure depicts the instrument's capability to provide a frequency-varying signal at either port one or port two and to separate the incident and scattered traveling waves at both ports. These four waves are down-converted to an appropriate frequency (IF) for digitization by the instrument. For a more comprehensive discussion on VNA architecture, the interested reader is referred to [6], with additional details provided on the measurement setups and techniques, which form the basis of this thesis work. For the purposes of this dissertation, it is necessary to discuss the higher-frequency version of the VNA together with its limitations. In fact, commercially available instruments typically offer measurements up to approximately 70 GHz, which corresponds to the upper-frequency range of the 1.85 mm connector. However, the majority of the studies referenced in this work will focus on the Software (SW) and Hardware (HW) limitation of the instrumentation when operating at frequencies above 70 GHz.

2.2.2. INCREMENT OF THE INSTRUMENTS' COMPLEXITY AT MM-WAVES

To extend the frequency measurement range of instruments (i.e., VNA) beyond the 1.85 mm coaxial limits, frequency extenders are employed (fig. 2.4a) (often also called simply extenders in this dissertation). These extenders utilize frequency multipliers and harmonically driven down-conversion chains (fig. 2.4b) to broaden the instrument frequency

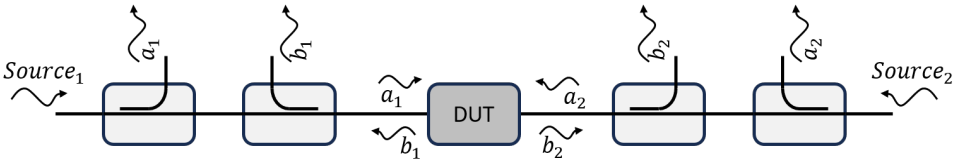
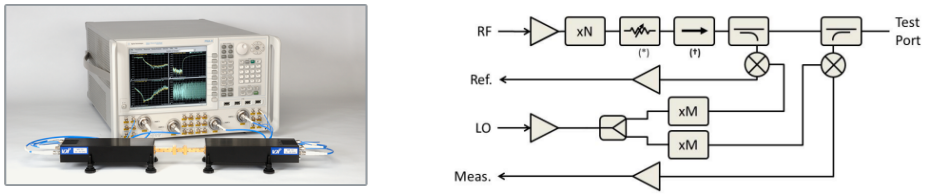


Figure 2.3.: Reflectometer for S-parameter measurements.

range up to 1.1 THz [7]. While the use of frequency extenders is essential for mm-wave measurements, it presents also a set of non-idealities compared to coaxial based (i.e., fundamental) setups. One first limitation relates to the output power level provided by the instrument. Conventional VNAs operating in the coaxial bands, integrate in their circuitry various Automatic Level Control (ALC) blocks (i.e., after every multiplication of the fundamental instrument Phase-Locked Loop (PLL)) allowing to properly regulate the output power versus frequency and thus optimize the Signal-to-Noise Ratio (SNR) of the measurement over a large frequency band. The simple architecture realized by using the frequency extenders shown in fig. 2.4b does not present an automatic power level control circuit after the non-linear multiplier operation. This impairs the ability to regulate and stabilize power levels (across frequencies), which are always equal to the maximum achievable value set by the multiplier saturated output power (e.g., in the order of 13 dBm for the WR6.5 version, i.e., 110 GHz-170 GHz [7]). The maximum power levels provided by the extenders are often too large for single device (small-signal) characterization. Employing these uncontrolled (from the user perspective) power levels poses a risk of driving the DUT into a (non-linear) large-signal operation, even during S-parameter measurements. [8]. Consequently, in small and large-signal characterization measurements, where the source power needs to be defined and swept, to characterize the various DUT metrics, controlling the power at the output of the mm-wave extender becomes essential. Some extenders attempt to obviate to the lack of power control by incorporating a variable (manual) attenuator before the coupler, see fig. 2.4b, allowing for a (user intensive) regulation of the power at the output of the extender. However, this approach introduces a large uncertainty in performing a power sweep since the mechanically attenuator at every power point relies on the low precision in the value setting which is only identified by knob scale. Moreover, the process becomes very operator intensive, making it slow and prone to errors. Finally, only using the relative value of the attenuation, i.e., provide by the scale setting and using the compressed power level as a reference, does not consider the impact of the frequency-dependent response of the attenuator and that of the extenders in the absolute power level. The interaction of these two latter factors results in a large fluctuation of the power across the band which can only be avoided if a single frequency approach is used, thus making the measurements troublesome and slower. Moreover, when small-signal measurements are targeted, and the simplistic approach of reducing the highest power level of the non-linear power vs. frequency trace is chosen (i.e., as the −45 dBm level at 230 GHz in fig. 2.5), will results in a significant reduction of the measurement Dynamic Range (DR), namely the 11 dB loss of dynamic range at 320 GHz shown in fig. 2.5. To obviate the several limitations of manually intensive power-controlled setups in [9] the electronic control of the mm-



(a) (b)

Figure 2.4.: a) Typical mm-wave VNA consisting of a VNA and frequency extenders; b) Internal schematic block of a typical frequency extender.

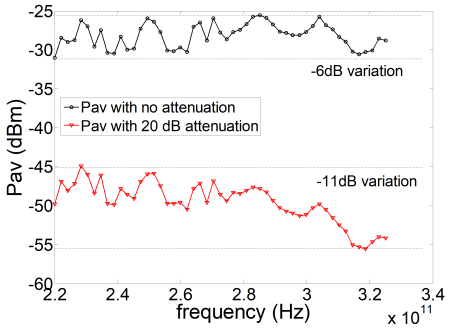


Figure 2.5.: Extenders output power variation across the frequency band with and without the use of the attenuator [9].

wave extension power through input power modulation was introduced. This approach involves a power calibration and comprehensive characterization of the extender, i.e., cascading reflection coefficient calibration with power calibrations, and enables accurate measurement and control of the output power through a full software solution. This approach successfully addresses the time, user interaction and DR optimization, by controlling the output power through modulating the input power of the extender (fig. 2.6), nevertheless, this approach necessitates careful consideration of the associated risks. A strategy to evaluate the purity of the signal supplied to the DUT when electronic power control is implemented has been presented in [10] and it is described in thesis work in Appendix A. It is reassuring that tested commercial frequency extenders (VDI extenders WR10 fig. 2.7a and WR6.5 fig. 2.7b) exhibit approximately 40 dB of dynamic range, with the total contribution of spurious signals being less than 1 dB, as shown in fig. 2.7a and WR6.5 fig. 2.7b, which is generally adequate for most large-signal characterization power sweeps. The frequency extenders upconverting operation with the amplitude and phase modulation of the input wave will be the base of the work presented in chapter 5 where also the extension of mm-wave test benches to realize non-50 Ohm characterization environment will be described.

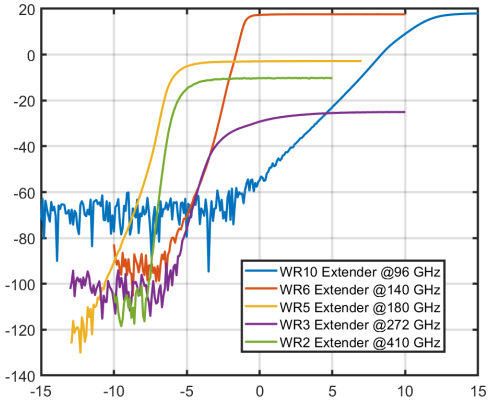
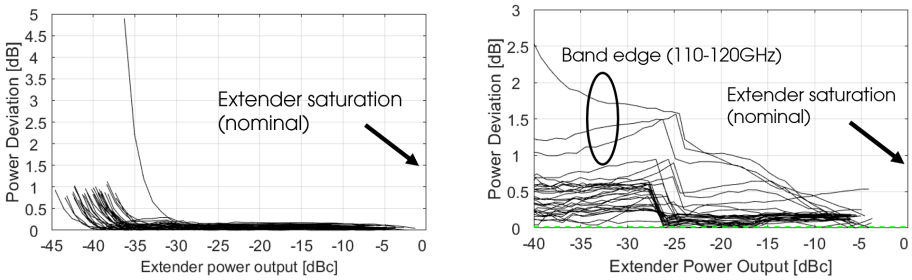


Figure 2.6.: Response input-output of the extenders in different bands.



(a) (b)

Figure 2.7.: Total spurious contribution measurements vs extender power output considering a Virginia Diode WR10 extenders (a) and a Virginia Diode WR6.5 extenders (b)[10].

2.3. MM-WAVE LIMITATIONS IN CALIBRATION AND DE-EMBEDDING

The scattering parameters briefly introduced in section 2.2.1 are referred to a specific locations in the measurement setup/DUT environment, these locations are also known to as the reference planes and are thereby set by the calibration procedure. Similarly to the procedure carried out in the lower RF frequency bands (i.e., below 40 GHz) mm-wave calibrations also make use of a set of known or partially-known artifacts denoted as standards, to extract the test-bench non-idealities such as amplitude losses and phase delays in the interconnection lines, the reflectometer, the down-converting chains and so on. The calibration procedure then enables to map the entire signal path up to the specified reference plane, in a simple input-output network formulation denoted as the error box, which can then be mathematically removed from the measurement. The calibration process relies on a set of artifacts known as "calibration standards," for which the expected measurement outcomes are precisely defined. By measuring these calibration

standards, it is possible to construct a system of linear equations where the parameters of the setup components are treated as the unknown variables to be determined. Depending on the chosen set of calibration standards, various calibration algorithms with differing levels of accuracy and informational requirements can be employed (e.g., Thru-Reflect-Line (TRL) [11], Short-Open-Load-Reciprocal (SOLR) [12], Line-Reflect-Match (LRM) [13], etc.) (see table 2.1). In the current RF telecom frequency range (i.e., below

	TRL		LRM/LRM+		SOLR	
	Port1	Port2	Port1	Port2	Port1	Port2
Transmission Standards						
THRU (Four Known S-parameters)	4 ET		4 ET		x	
LINE (Known: S_{11}, S_{22} and Unknown: S_{12}, S_{21})	2 ET		x		x	
RECIPROCAL (Known: S_{21}=S_{12}, known for ±90° Unknown: S_{11}, S_{22})	x		x		1 ET	
Number of Error Terms	**6**		**4**		**1**	
Reflection Standards						
OPEN (One known per port)	x	x	x	x	1 ET	1 ET
SHORT (One known per port)	x	x	x	x	1 ET	1 ET
LOAD (One known per port)	x	x	1 ET	1 ET	1 ET	1 ET
REFLECT (Known: S_{21}=S_{12}, known for ±90°, one known per two ports)	1 ET		1 ET		x	
Number of Error Terms	**1**		**3**		**6**	

Table 2.1.: Comparison of TRL, LRM, and SOLR calibration procedures [14] (It has been transcribed from the original without any modifications). All three methods provide the seven Error termss (ETs) required for S-parameter calibration. An "x" indicates that the corresponding standard is not used in the calibration procedure for that algorithm.

40 GHz) broadband calibration algorithms are often used to enable multi-octave calibrations. Those algorithms do require resistive terminations, i.e., loads, and are carried out on impedance standard substrates (fig. 2.8) which are provided by the various probe vendors. The general approach is then to transfer the calibration to the DUT measurement environment to obtain calibrated measurements. When attempting to apply this approach to mm-wave measurements for DUT embedded in a Si technology environment the limited field confinement (fig. 2.9) of wafer probes yield only limited accuracy as was shown in [16]. This transfer process can be improved by including a shunt reactive frequency dependent as was shown in [16], recovering the accuracy in the calibration transfer process. Nevertheless, the knowledge required by these broadband calibration

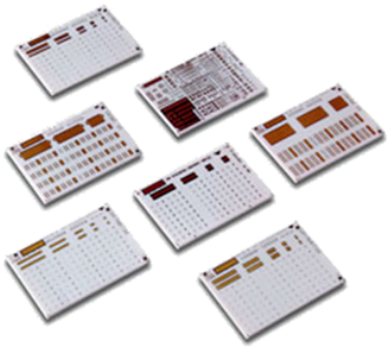


Figure 2.8.: Commercial calibration standard substrates [15]

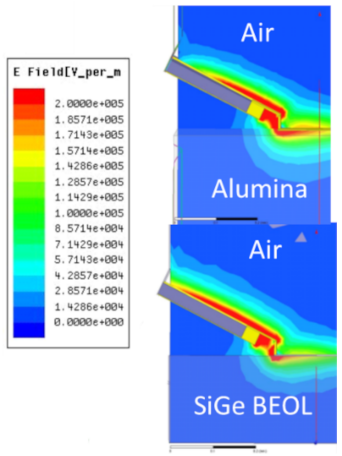


Figure 2.9.: Simulation of the electrical field distribution around the landing spot in the case of alumina and silicon-germanium substrate [16].

algorithms sets also the limitations for the achievable accuracy. Therefore, calibration algorithm, such as TRL and multiline-TRL [17], which do not require absolute knowledge of the standard artifacts), become the de-facto standards at mm-wave frequencies. The implementation of TRL-based algorithms (i.e., relying on transmission line propagation) requires mono-modal propagation operation of the lines. This necessitates a proportional scaling of the calibration standards to avoid the excitation of undesired radiating modes [18, 19]. However, the mechanical constraints in the construction of these calibration standards and the limited minimum size of the RF probe's contact tips (fig. 2.10), prevent the Coplanar Waveguide (CPW) lines from being scaled proportionally with frequency. The above mechanical limitations impose a shift in the calibration paradigm, in which the landing pads and the transmission line environment need to be decoupled by making the calibration plane offset concerning the probe tip plane and thus making the calibration standard technologies specific, as will be discussed in detail in chapter 3.

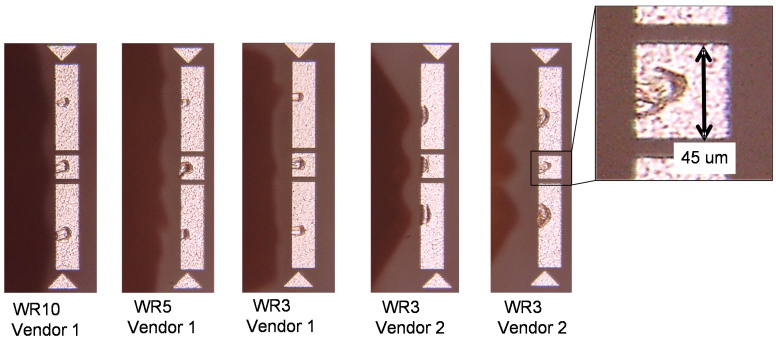


Figure 2.10.: Probe skating marks for different operation frequency bands and vendors.

2.3.1. DE-EMBEDDING APPROACH

When device model validation is targeted, the DUT is embedded in a test fixture, which interfaces the active device with the probe environment (i.e., Ground-Signal-Ground (GSG)) via the lines fabricated in the Back-End Of Line (BEOL). This fixture allows, once removed, the reporting of data at the intrinsic device reference plane. The complexity of the test fixture and the necessity for precise knowledge of the calibration standards, combined with the need to realize a clean mono-modal propagation environment, pose a significant challenge in defining or placing the calibration reference plane in close proximity to the DUT (fig. 2.11a). The simplest lumped-model-based de-embedding technique involves determining the values of lumped components in a predefined equivalent circuit model of the fixture section by using a set of dummies of the test fixture with idealized termination, such as open and short conditions (fig. 2.11b) [20]. The primary advantage of this method lies in its minimal requirements. In fact, the required terminations are easier to design and position correctly compared to matched loads or transmission line standards. The application of this latter method alongside the calibration in the microwave frequency band (below 40 GHz) has become a well-established and precise procedure to obtain accurate device-level results. However, as we move into the mm-wave regime, the reduction in wavelength has a profound impact on the de-embedding procedure, as briefly discussed in the next section.

MM-WAVE LIMITATION OF LUMPED-MODEL-BASED DE-EMBEDDING

To evaluate and validate the expected behavior of a design, prototypes and device models must be characterized within their targeted operational frequency range, which increasingly extends to millimeter-wave frequencies. At these frequencies, as previously anticipated, the open-short de-embedding technique presents notable limitations, primarily due to the trade-off between dimensional constraints, occupied area, and frequency validity. Specifically, the physical constraints imposed by the RF probes force the minimum size of the contact tips to a few tenths of microns (fig. 2.10). Consequently, this restriction determines the minimum feasible dimensions of the test fixture,

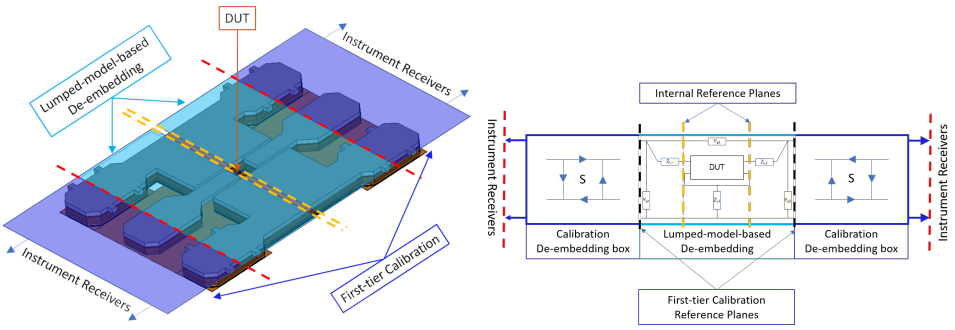


Figure 2.11.: Highlight different de-embedding blocks and the relative calibration plains: a) On a structure representation and b) schematic blocks representation.

which cannot be scaled proportionally to the wavelength. Therefore, with increasing frequency, the test fixture becomes more and more comparable to the wavelength, which leads to a distributed behavior that compromises the validity of the method based on a lumped model. This phenomenon has been shown in [21] where a simple test fixture, parametrized by the pad size (Wpad) (fig. 2.12), was simulated to assess, after applying a one-step open-short de-embedding approach (fig. 2.13a), the error in the extraction of a reference capacitance (fig. 2.13a) as a function of frequency and Wpad. The resulting error, expressed as a percentage, is depicted in fig. 2.13b where the 10% error threshold is also indicated. The data clearly indicate that as Wpad increases, the frequency at which the same 10% error occurs decreases. To enhance the frequency validity, the test fixture must be partitioned into multiple sub-fixtures, allowing individual segments to remain sufficiently small relative to the wavelength and thus be treated as lumped elements. Different solutions have been presented in the literature, differing in the number of subdivisions [22–24] (fig. 2.14). However, it is essential to note that increasing the number of sub-fixtures leads to significant area consumption, which is particularly undesirable in the context of costly fabrication technologies. Therefore, to extend the usability of the one-step open-short de-embedding to higher frequencies without compromising its accuracy, it is necessary to bring the primary calibration plane as close as possible to the DUT, reducing the size of the residual fixture. The work in [25] proposed the concept of shifting the primary calibration plane into the BEOL up to the first layer of metal, benefiting from a consistent calibration/measurement environment employing low-dispersion transmission line components. Nevertheless, the proposed paper, using TRL and/or multiline line TRL, fails to cover the band's low frequency part, often required to enable accurate comparison in the frequency ranges where current model parameters are being extracted. The work in [25] will be taken as reference in chapter 3 to realize M1 direct calibration/de-embedding approaches for broadband device model validation, presenting the design considerations and introducing a structured design/simulation and validation flow.

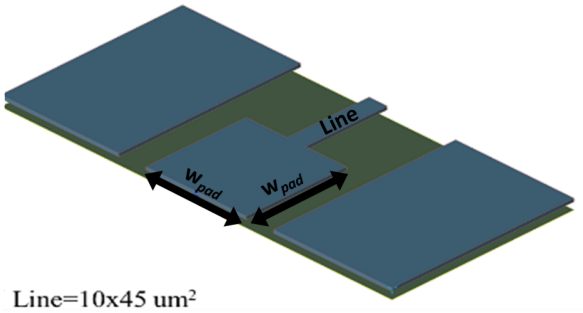
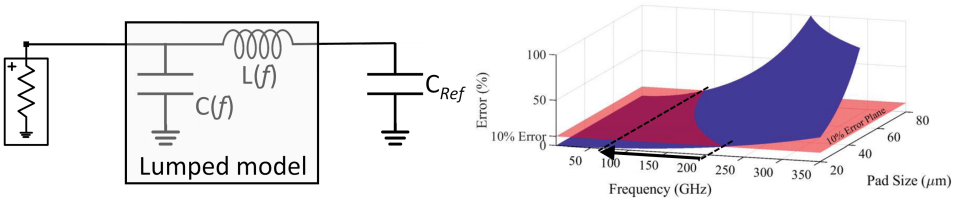
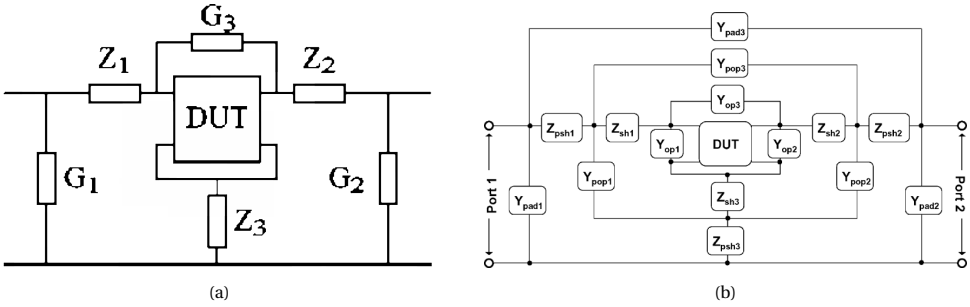


Figure 2.12.: Test fixture used in the simulation in [21]



(a) (b)

Figure 2.13.: a)Lumped representation of the text fixture included in the simulation test bench used in [21] to asses the error in the extraction of the reference capacitance b) Error in percentage resulting from the simulation as function of the frequency and the pad size.



(a) (b)

Figure 2.14.: a) Three-step de-embedding method [22] b) Five-step de-embedding method [24].

2.4. CONCLUSIONS

In this chapter, an overview of device characterization has been provided, beginning with an explanation of its significance in the device characterization/development cycle. Following this, the differences between the small-signal and large-signal regimes of an active device have been addressed, along with the definitions of S-parameters and the hardware utilized to measure them. After discussing the calibration concept, the limitations and complexity of measurements in the mm-wave range have been briefly

discussed, highlighting the opportunities for enhancing device characterization in frequencies exceeding the microwave spectrum. It is evident that the signal up-conversion in millimeter-wave measurement setups limits the extraction of large-signal parameters, necessitating new strategies to overcome these challenges (chapters 5 and 6). Additionally, the reduction in wavelength complicates the design and definition of test structures, making them more likely to introduce measurement and calibration error. Therefore, a structured design and verification procedure for test structures is essential to gain accuracy and allows fine-tuning new designs (based on expectations) before sending them to the foundry, which will be discussed in chapter 3.

3

TEST-FIXTURE DESIGN FLOW FOR PRE-SILICON CALIBRATION ACCURACY DETERMINATION

This chapter presents a structured design flow for RF device test fixtures, providing the capability to design and test up to mmw-wave on-wafer test-fixture and evaluate the forecasted uncertainty of device-level model parameters before silicon fabrication up to (sub)mm-wave bands. The presented design flow is developed and validated on advanced CMOS nodes, i.e., 22 nm *FD-SOI, and employs commercially available CAD tools, and can be applied on different silicon-based technology platforms. Two on-wafer calibration techniques, employing back-end-of-line first-tier calibration, are considered, namely the (broadband) Short-Open-Load-Reciprocal and the Thru-Reflect-Line. The design flow is developed to incorporate the technology fabrication requirements, i.e., design rule check (DRC) constraints, and their possible trade-offs (i.e., local versus global restrictions) in order to reach the desired accuracy level of the extracted parameters. A semi-automated procedure to move from DRC-compliant structures to ones that can be simulated in a 3D EM environment is introduced. Finally, after discussing the challenges and the solution in the 3D EM simulator settings, various device-level parameters and performance metrics are experimentally evaluated and compared to the foundry PDK model for the NMOS* 22 nm *FD-SOI 16 fingers up to* 325 GHz.

Parts of this chapter have been published in Test-Fixture Design Flow for Broadband Validation of CMOS Device Models up to (sub)mm-Waves (2025) [26].

3.1. INTRODUCTION

An increasing number of commercial applications, i.e., from beyond 5G communication [27–29] to the current and next generation of automotive radar systems [30, 31], are targeting the mm- and sub-mm-wave frequency ranges. This has generated a strong need from technology foundries to validate the accuracy of the models of their active devices (i.e., included in their process design kit) at the frequencies targeted by these applications. This need is reinforced by the fact that the experimental data, which are used to extract the model parameters, are often limited to frequencies (well) below 100 GHz. One of the reasons for the limited frequency range of the parameter extraction, even when considering technologies with f_T/f_{max} in excess of 300 GHz, lies in need to employ data referred to the intrinsic device plane (or at the first metal layer plane in some cases). This requirement implies that the systematic errors provided by the measurement test-bench (i.e., network analyzer up to the wafer probes), as well as the parasitic loading introduced by the fixture, interfacing the DUT with the probing environment, need to be removed. The first step, i.e., removal of the systematic errors provided by the test-bench is achieved by means of VNA calibration. Several papers [32–34] have reported how to achieve accurate VNA calibrations up to sub-mm-wave frequencies employing partially known calibration algorithms such as TRL or multi-line TRL [11, 17]. The combination of advanced calibration algorithms and the confinement of both calibration and measurement phases in the same dielectric environment has allowed to overcome the limitations of using off-wafer Impedance Standard Substrates (ISS) from commercial vendors [16, 18, 35, 36] when attempting device characterization above 67 GHz. Despite this wide range of publications, the de-facto standard approach in model extraction for foundries Process Design Kits (PDKs) [37] is to employ commercial, ISS-based, broadband, fixed distance (probe-to-probe) calibration algorithms, i.e., Short-Open-Load-Thru (SOLT)/SOLR [12] or LRM/Line-Reflect-Reflect-Match (LRRM) [38]. Among the various reasons for this choice, which provides a limited quality of calibration, is the complexity of designing and validating the accuracy of a custom-designed first-tier calibration kit. Moreover, after the VNA calibration, a second step is required to reach the intrinsic device plane, i.e., the removal of the device fixture parasitic elements, often termed by modeling engineers the *de-embedding step*. This step is realized by measuring a set of dummies of the test fixture (i.e., a version of the fixture excluding the DUT and employing an idealized termination) or part of it in order to realize a lumped model of the same, which can then be removed from the DUT measurements [20, 39], employing closed-form equation algorithms. Over the years, the complexity of the model of the test fixture has gradually increased, mainly to provide an increased model-to-hardware correlation in the higher frequency range. This has been achieved at the expense of an increased number of dummy elements [22–24]. Considering that the minimum dimension of the fixture is fixed by mechanical constraints, such as the landing pad area (fixed by the probe tip dimensions, which do not generally scale with frequency) and the input-to-output probe distance (limited by the probe-to-probe crosstalk effect [40]), the increased fixture model complexity is a direct result of the lumped approximation starting to fail when the electrical propagation delay over the considered structure approaches $\pi/2$. To enable a simple open-short de-embedding, without trading off model accuracy, [25, 41]

have proposed the concept of shifting the primary calibration plane in close proximity to the intrinsic device. The residual fixture parasitic can then be removed by employing a simple open-short de-embedding and still provide high model-to-hardware consistency to frequencies up and above 200 GHz, as was shown in [21]. Nevertheless, the proposed papers make use of TRL and/or multiline line TRL calibrations which fail to cover the low-frequency part of the band, which is strongly required in order to comply with the current model parameter extraction flow. The following sections present the design consideration and the simulation flow to realize broadband M1 direct calibration/de-embedding approaches for device model validation up to sub-mm-wave frequencies. Moreover, the approaches to incorporate, during the design phase, the stringent fabrication requirements (i.e., the design rule checking) of advanced CMOS nodes are discussed. Finally, in section 3.6 the measured data, up to 325 GHz, of key device level parameters validated versus the PDK device model for small signal operation are presented.

3.2. CMOS BROADBAND M1 TEST-FIXTURE

For decades, Chemical-Mechanical Polishing (CMP) of inter-level dielectrics [42] have been employed in CMOS technologies to improve global planarization and overall yield. Nevertheless, since CMP processes are sensitive to metal densities, metal-fill design rules and procedures have become an integral part of the layout process. The electrical impact of the metal-fill dummies has been recognized from the early years [43], at first, accounting mostly for the increased capacitance of those layers, and more recently, recognizing and modeling the complete electromagnetic behavior of layers containing the metal fills by employing equivalent an-isotropic dielectric layers [44]. Aside from the modeling challenges, the current inclusion of dummy fills in the design flow (i.e., via automatic fill algorithms) is prone to inconsistencies in the number of floating inclusions when an array of instances is placed on the reticulum (i.e., a grid of test fixtures for device model extraction and verification). To overcome the (potential) error arising from inconsistencies in fixtures that need to be removed based on a (fixed) model, the approach developed during this work is to employ a scripted hierarchical construction of basic unit shapes, which are parameterized by their fill factor.

3.2.1. BASIC ELEMENTS/UNITS AND BLOCKS

The lowest level in the hierarchy is realized by basic elements (see fig. 3.1), which can be drawn parametrized using a scripting language, i.e., Skill language [45] in the work carried out in this thesis. Subsequently, the basic elements can be combined into larger sections, thus realizing a basic unit. Various basic units, employing different sets of metals, are realized to provide the scripting tools with a large dataset to be employed in the structure design process, all complying with the density rules. It is important to note that given the parametric nature of the scripts, both local and global densities can be tuned and fulfilled at any point within the design flow. The basic units are then combined into blocks; see fig. 3.2.

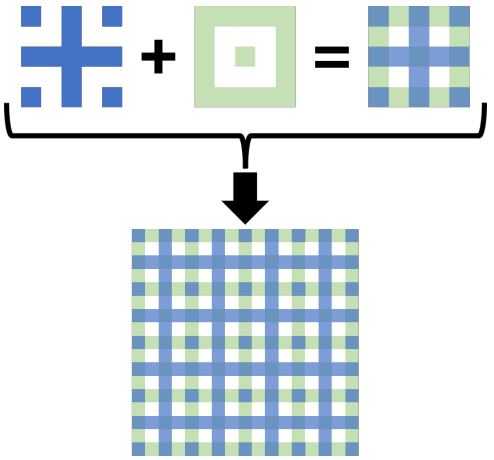
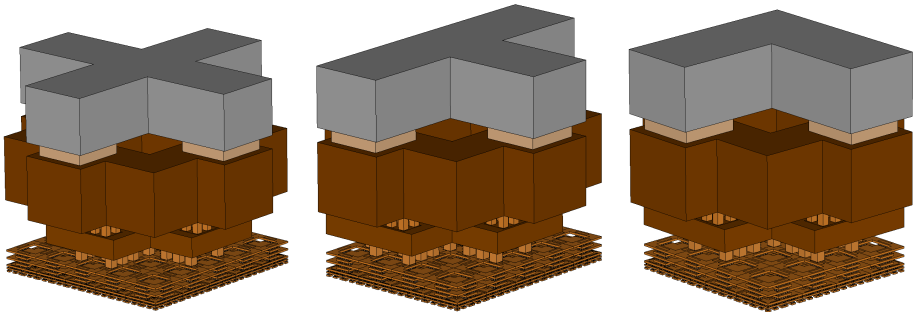


Figure 3.1.: Basic layout elements realized in the lowest level in the hierarchy using different metal layers.



(a) (b) (c)

Figure 3.2.: Vertical blocks created with different geometries to satisfy all the structure layout needs: a) internal block, b) side block, c) corner block.

3.2.2. FIXTURE SUB-SECTIONS

The various building blocks described before are then combined to create the various sub-sections of the device fixture, see fig. 3.3. In the proposed approach, the direct calibration/de-embedding fixture approach presented in [25] is employed. The fixture topology uses capacitively-Loaded Inverted Coplanar Waveguides (CL-ICPWs) and a M1 calibration reference plane. In the CMOS implementation addressed during this work, the fixture is realized with the basic element scripting approach as discussed, and each section is realized by an integer number of the DUT/Standard (STD) section dimension (1 unit, see fig. 3.3). The usage of the scripted "Lego" approach is done to simplify the entire die floor plan, providing a considerable time saving for the layout phase when aiming at a large number of devices to be modeled/characterized. The requirements and optimization steps of each of the test fixture sections are summarized below:

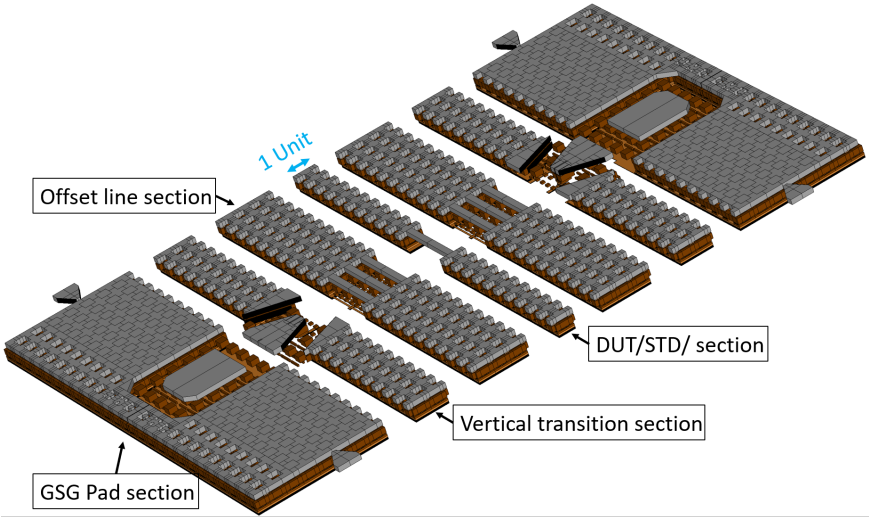


Figure 3.3.: Complete structure composed of the different test-fixture sections.

- *GSG Pad section*: the probe landing section of the fixture is designed to accommodate different pitches, given the broadband requirements of the modeling/validation measurements. The fixture implemented for this contribution supports probe pitches from 100 µm down to 50 µm.

- *Vertical transition section*: this section interfaces the pads with the CL-ICPW placed at M1. The inverse pyramidal shape, described in [25], is also employed here to minimize discontinuities and interface the larger top metal lines with the narrower M1 section. Given the field disturbances introduced by the transition (addressed in more detail in the section 3.2.3), ESD/Antenna protection diodes are also placed in this section. It is important to mention that, in ultra-scaled CMOS nodes, those protection diodes are strictly required even when dealing only with R&D test structures. When technology or available area limitations do not permit the full “transparency” of the diodes in the characterization window, an error split box procedure, as demonstrated in [46], should be applied. This technique is further detailed in section 4.2. The antenna diode stack employed for the fixture described in this section (CMOS 22FDX) provided “transparent” behavior up to 1 V.

- *Launch Line*: The launch line allows shifting the reference plane of the calibration "far enough" from the transition where the field is disturbed by evanescent high-order modes. Due to the high cost of the on-wafer area, there is a need to develop a procedure to quantitively define how "far enough" is required to achieve mono-mode propagation, this procedure is discussed in section 3.2.3.

- *Device Fixture*: The surroundings close to the device have been adapted for each different transistor instance, to fit their dimension (fig. 3.4). Furthermore, for each

device, an open ad short is added to allow the device fixture de-embedding.

3.2.3. LAUNCH LINE OPTIMIZATION

In order to identify the minimum required length for the launch line, a numerical approach has been developed based on extracting the 3D (i.e., volumetric) field over the line and defining a metric to identify the distance from the vertical transition where a mono-mode propagation is reached. Considering a launch line length of 60 µm on both sides (fig. 3.5a) the 3D field distribution is extracted in the boxed volume (yellow highlight) shown in fig. 3.5c. After, the transversal (to the direction of propagation) Two-Dimensional (2D) field is computed and mapped over a quantized XY grid fig. 3.5d. In order to create the mono-modal reference field (i.e., where no discontinuity is present), a separated simulation of the CL-ICPW line is performed, where the excitation port is now realized using a waveguide port in the FEM environment, i.e., CST Studio. The waveguide port excitation allows feeding of the traveling mode supported by the structure, thus removing the presence of discontinuities. Assuming the field along the propagation direction is periodic due to the geometry periodicity, each cross-section in fig. 3.5c is compared with the field on the 2D cross-section at the center of the CL-ICPW standalone (figs. 3.5b and 3.5e) at the same position in the period (fig. 3.5f). The root-mean-square-error between the field distribution of the propagation mode over the grid within the entire test fixture (i.e., including the vertical transition) and the mono-modal case (i.e., waveguide fed M1 CL-ICPW, excluding the vertical transition) is chosen as the numerical metric to identify the minimum offset line length. Observing the results shown in fig. 3.6, it is possible to see the error calculated at different positions along the line. The error decreases rapidly moving away from the transition (this is due to the quick decay versus length of the reactive, i.e., non-propagating fields). This region can then be identified as the single-mode quasi-TEM zone. The quick decay of the error and the (almost) independence from the frequency can be explained by the fact that non-propagating reactive fields (also known as evanescent) present a decay length that is not dependent on the frequency but only on the dimension of the field perturbation. This analysis provided, for the fixture implemented in the CMOS Silicon-on-Insulator (SOI) technology, a minimum length of 30 µm to reach a quasi-mono-modal behavior.

The method can be readily demonstrated using a well-known transmission line. For this purpose, a simulated example in a waveguide transmission line has been carried out fig. 3.7b. The waveguide considered is dimensionally designed for the WR6.5 frequency band, which spans from 110 GHz to 170 GHz, resulting in $a = 1.651\,\text{mm}$ and $b = a/2 = 0.8255\,\text{mm}$ (see, fig. 3.7a). The cutoff frequencies for the first three modes of this waveguide, calculated using eq. (3.1), are reported in table 3.1

$$f_c = \frac{c}{\sqrt{(\frac{m}{a})^2 + (\frac{n}{b})^2}} \tag{3.1}$$

Where c is the speed of light, a and b are the two waveguide dimensions, and m and n are the mode indices.

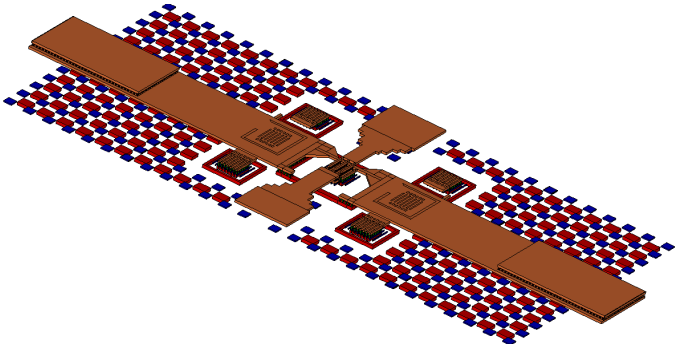


Figure 3.4.: Intrinsic Device Fixture.

Cutoff frequency for a WR6.5 waveguide

MODE	f_c [GHz]
TE_{10}	90.79 GHz
TE_{20}	181.58 GHz
TE_{01}	181.58 GHz

Table 3.1.: Cutoff frequencies of the first three propagation modes in a WR-6.5 band waveguide.

Subsequently, a 3D EM simulation of a 3 mm waveguide section has been performed at 140 GHz, employing a waveguide port excitation configured to excite the first three modes. From the simulation, the superposition of the three modal fields has been exported and provided to the algorithm to extract the attenuation behavior of the evanescent modes. The field distribution at the end of the structure has been used as the reference field for single-mode propagation.

The resulting attenuation trend has been compared with the theoretical one, which is characterized by the nominal exponential decay described by eq. (3.2). As shown in fig. 3.8, the method accurately predicts the attenuation behavior.

$$Attenuation \propto e^{-2\alpha z} \tag{3.2}$$

Where α is the real part of the propagation constant and z is the distance from the mode generation.

3.3. 3D-EM SIMULATION TEST BENCH

3.3.1. LAYOUT DESIGN

The evaluation of the "quality" of the designed calibration/de-embedding structures, i.e., fixture and relative standards, must include simplifying steps to convert the DRC-

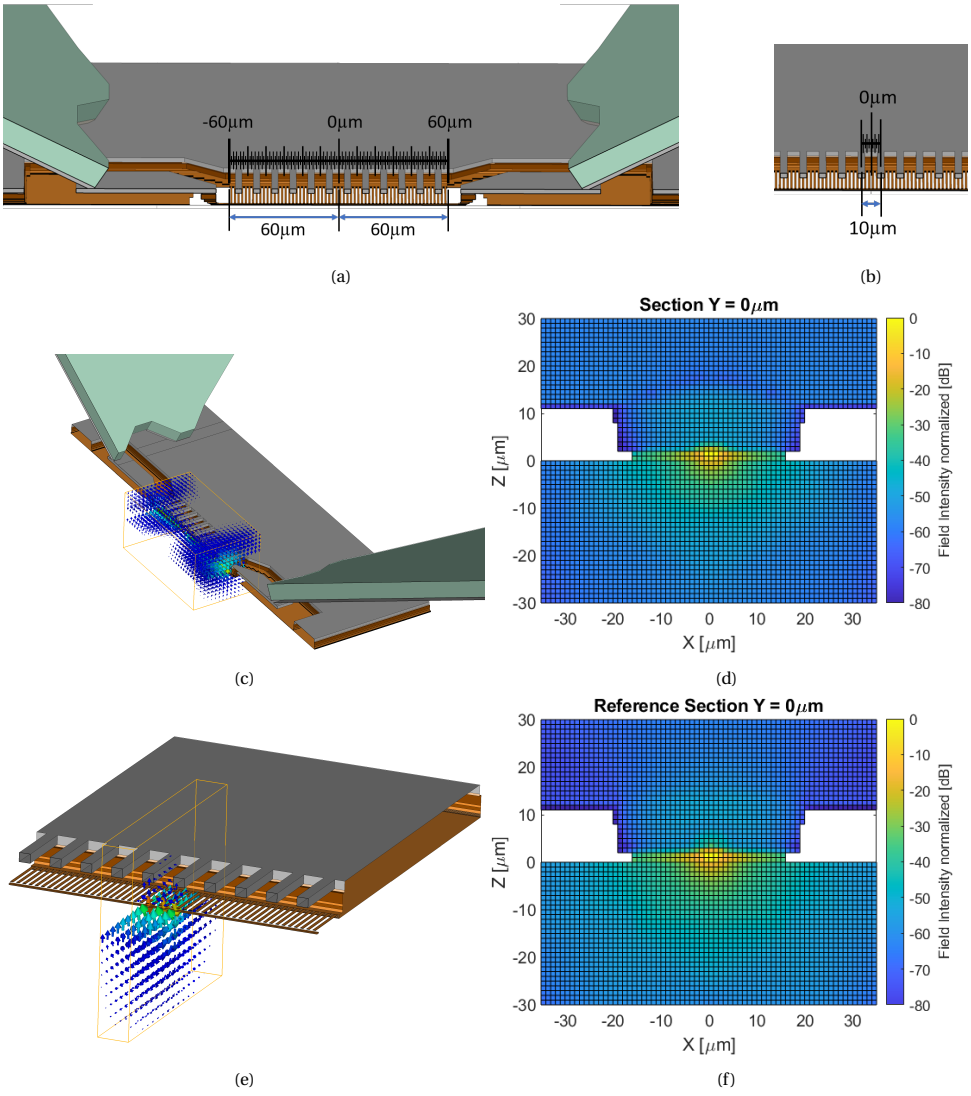


Figure 3.5.: Steps for the line length optimization analysis. a) discretization of the line for the 2D field distribution under test; b) discretization of the line for the 2D reference field distribution c) Volume of field under test acquired from the simulation for the analysis; d) 2D field under test distribution in a specific distance position (Y = 0 µm; i.e., Center of the structure); e) Volume of reference field acquired from the simulation for the analysis; f) 2D reference field distribution in a specific distance position (Y = 0 µm; i.e., Center of the structure);

compliant structure, discussed in the section 3.2, into one that can be efficiently simulated in modern 3D EM environments. As can be easily understood, structures including the dimensions and features shown in fig. 3.2, cannot be simulated even in the state-of-the-art high-performance servers. The main hurdle in importing and simulating such

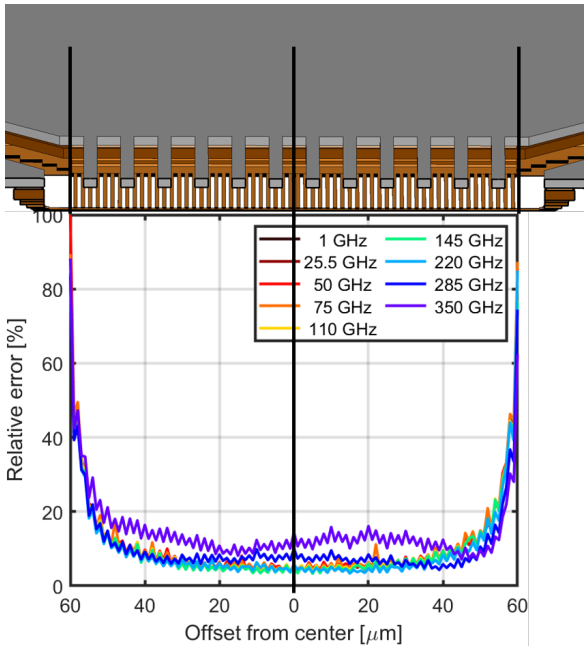
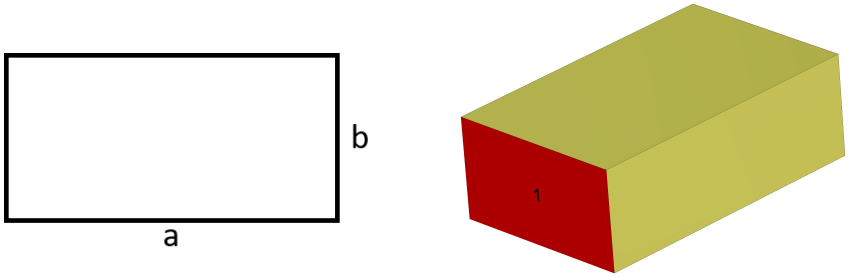


Figure 3.6.: Relative root square mean error across the line.



(a) (b)

Figure 3.7.: a) Waveguide transversal section, b) Simulated waveguide section.

Design Rule Checking (DRC)-compliant structures comes from the sizes of the vias and the dummy tiles fill which are required at every layer of modern CMOS nodes. At this point, it is important to recall that 3D EM simulators require, before solving Maxwell's equations, to discretize space into homogeneous volumetric cells, a process which is known as meshing. When the extremely small features imposed by the cheesing and filling rules of CMOS DRC-compliant structures are present, the meshing process would generate a space discretization that is too computationally onerous to be handled by current server technologies. The approach presented in this work introduces only a first-level conversion between the DRC-compliant structures and the ones to be 3D EM sim-

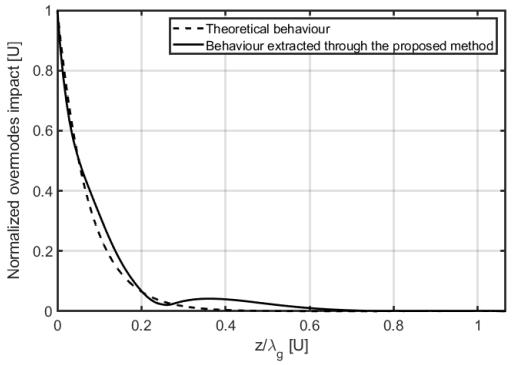


Figure 3.8.: Plot of the normalized evanescent mode effect as a function of the normalized distance from the discontinuity in a WR6.5 band waveguide.

ulated. This first-level approach includes only geometrical modification, while the electrical values of the conductive layers are left unchanged. The approach is briefly shown in fig. 3.9b, where the cheesing feature, which is embedded in the basic block (fig. 3.9a), is removed, as shown in fig. 3.9b. Moreover, the dummy tiles present in the dielectric layers are also simply removed and two approaches are considered:

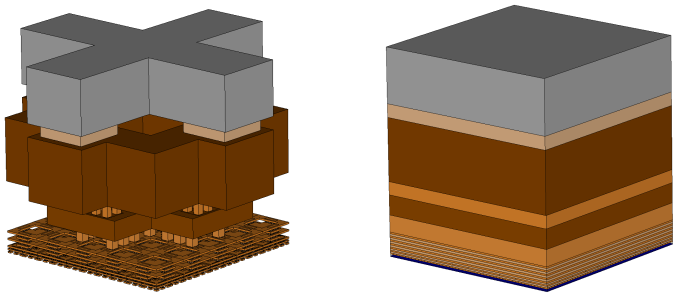
1. The electric parameters of the oxide layers are kept constant to the PDK default value.

2. The homogenized permittivity and permeability of the layer, including the floating structures, are computed using the approach shown in [47] and applied to the stratification of CMOS technology in [44]. This new ϵ/μ value, which is represented in a tensor form, given the non-isotropy of the equivalent layer can then be used in the EM reconstructed fixture.

Applying the simplification approach to the various sub-blocks of the structure results in changing the entire DRC-compliant structure shown in fig. 3.10a, into the EM solver-compatible one shown in fig. 3.10b.

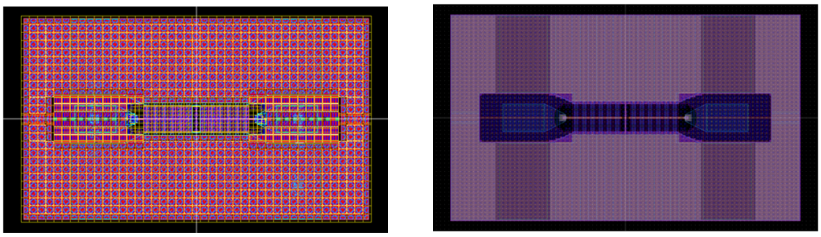
3.3.2. 3D EM SIMULATOR IMPORTING

The next step is to realize the conversion of the 2D Graphic Data System (GDS) file, which only contains the vector shapes of each layer in the structure but does not present any vertical information, into the 3D format supported by the drawing environment of the 3D EM Computer-Aided Design (CAD) tool to be employed, CST microwave studio in the work presented here. In addition to the conductor layers, which are the only ones present in the GDS file, also the substrate and the dielectric layers need to be added before considering any structure ready to be simulated (fig. 3.11c). This procedure, when performed manually, is very tedious and operator intensive, and for such reason is also



(a) (b)

Figure 3.9.: a) DRC-compliant basic vertical block; b) EM solver-compatible basic vertical block.



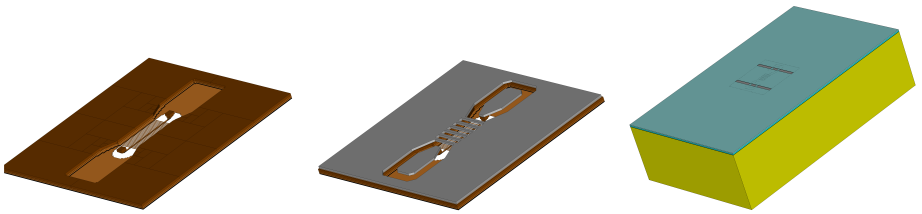
(a) (b)

Figure 3.10.: a) DRC-compliant structure; b)EM solver-compatible structure.

one of the main sources of errors (i.e., translation errors) between the simulated structures and the layout ones. The importing flow described below is detailed for the CST microwave studio platform but can be mapped to other 3D EM commercial tools such as Ansys HFSS. The detailed steps to carry out the automated import procedure are:

1. Read and import the GDS files defining for each layer its thickness, Z-absolute position and conductivity, as described in the PDK manual (fig. 3.11a).
2. Merge the macro elements still remaining from the previous merging to simplify the loading on the graphic processor (fig. 3.11b)
3. Add the dielectric layers in the stack using relative permittivity shown in the PDK manual (fig. 3.11c).

Finally the wafer probe tip is added to include a realistic discontinuity of the wave into the fixture environment. The probe tip model used in this work is derived from the Dominion [48] tip and is parametrized to realize a generic RF probe (fig. 3.12). The import procedure described above is fully coded in the scripting language supported by the CAD tool, in the case of CST this is a visual basic language. Some details of the script are shown in fig. 3.13, where fig. 3.13a represents the GDS import code, where the proper order in the vertical stack and the absolute z height is given to the various GDS layers fig. 3.13b, shows details of the merging code, and fig. 3.13c shows a part of the code where the parametrized wafer probes are inserted in the 3D structure.



(a) (b) (c)

Figure 3.11.: Importing steps. a) Raw importing structure having still same separate macro elements; b) Completed merge structure; c) Structure filled with the dielectric layer stack.

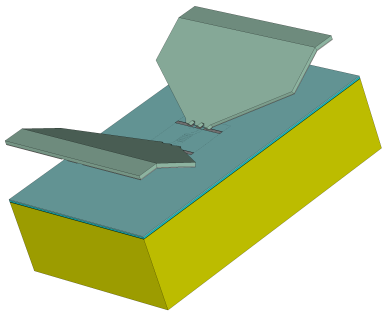


Figure 3.12.: Simulation structure with generic RF probes.

(a) (b) (c)

Figure 3.13.: Script code for the importing (a), the merging (b) and the probing (c).

3.3.3. SIMULATION SETTINGS

This section details the required settings, i.e., appropriate mesh distribution, material property settings and boundary conditions ensure accuracy simulations to achieve high model-to-hardware correlation in modern CMOS back-end-of-line stratifications.

EXCITATION

The excitation settings relate to the proper definition of the source that will be used to stimulate the structure under consideration. When a waveguide port is used as excitation, it generates a field distribution solving a two-dimensional eigenmode problem on its 2D section, thus assuming a homogeneous line without discontinuity [49]. The latter point leads to the conclusion that the waveguide port needs to "see" (i.e., be in direct contact with) the same geometry of the feeding line section. This is required to calculate and excite the right mode distribution to the various standards that will be simulated (i.e., line, open, short and match). Therefore, as shown in fig. 3.14, 50 µm of line in the Short-Open-Load (SOL) standards are included, ensuring that the waveguide port is in direct contact with the same 2D geometry of the feeding line (see offset line section in fig. 3.3). One of the critical points that sets the accuracy of the standard information, and thus the calibration accuracy, is the capability of generating a field distribution equal to the actual mode that propagates at the standard reference point, inside the test fixture. This capability changes depending on the different standards due to the high field discontinuity in proximity of the port presented by some of them (Short, Open, Load), which inserts disturbances in the field mode of the CL-ICPW not catchable by the waveguide port. Nevertheless, as will be discussed in the next paragraphs, the results representing the cumulative simulation error show, in the band of interest, an error comparable to the results extracted using transmission line based standards. Moreover, when different propagation modes are supported by the 2D geometry of the structure, the simulator chooses the one that has the highest propagation constant, which could be different from the one that is expected. One of the reasons for that could be because the actual potential distribution is unknown to the simulator. It is important to note that this problem doesn't have a defined/unique solution path and the user's experience plays an important role, there are some good starting points and valuable strategies to obtain a reliable simulation result. Typical rules of thumb for the waveguide port dimension in commonly used structures (i.e. coplanar waveguide, microstrip, etc.) are given in fig. 3.15 [49]. When the structure becomes more complicated, a good starting point is to vary the port dimensions, sometimes forcing an electrical shield on the edge to limit the supported propagation modes. Although modifying the port dimension can be helpful, one needs to constantly check the distribution of the propagation mode over the waveguide port and ensure it is all contained within the port without reaching the edge (i.e., using a level of −40 dBc at the port edge). This ensures that the entire energy is collected by the port. In this work, the multipin feature of CST has been used for the M1 structures with direct waveguide port excitation, to ensure the excitation of the right propagation mode. This feature defines the structure's potential signs (negative or positive) of some conductive blocks (fig. 3.16a). By doing so, it is possible to eliminate some of the allowed (by the port) propagation modes, providing a higher chance to excite the desired propagation mode (fig. 3.16b) whilst leaving more freedom in the port size (i.e., this enables larger frequency sweep with a single port size).

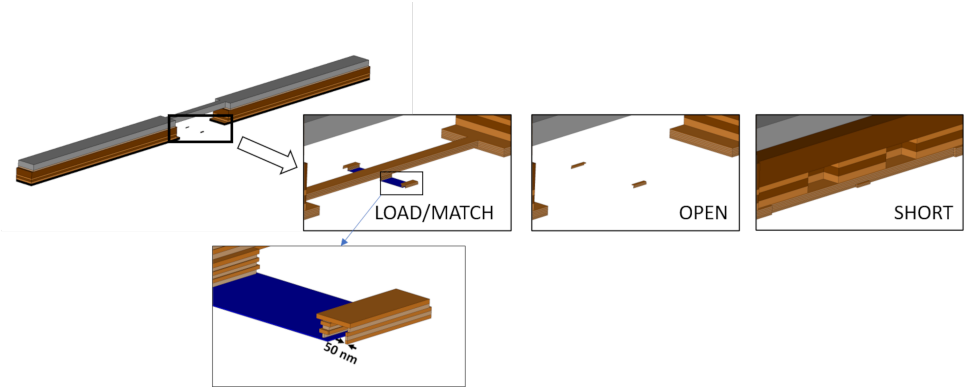


Figure 3.14.: Short, Open and Load/Match standards structures, highlighting the piece of line for the port mode calculation.

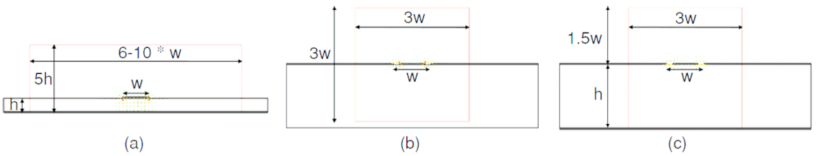


Figure 3.15.: Rules of thumb for waveguide port dimensions [49].

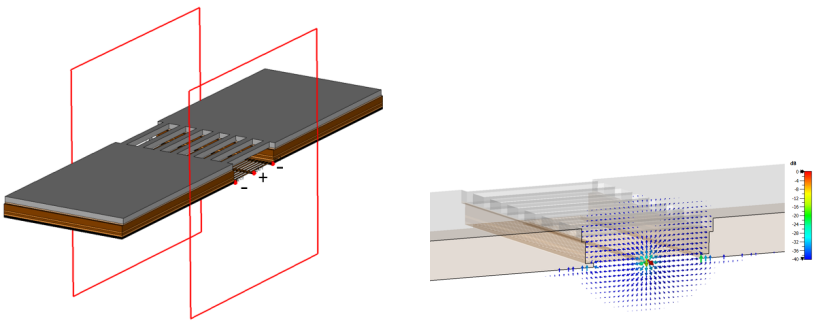


Figure 3.16.: a) Waveguide port placement using assigning potential signs; b) Port mode generated on the waveguide port.

MESHING

The finite element method solver engine, which is employed in the EM CAD tool, will discretize the 3D space in smaller regions, where Maxwell's equations are then solved. As already mentioned previously, this process of space discretization is called meshing. An adaptive mesh refinement feature of the simulator will iteratively increase the mesh

density to reach the desired accuracy for the S-parameters, set by the user. When the simulation domain presents extremely (spatially) fine features, it is important to set the starting mesh to a sufficient density level to identify the object-specific features properly; failing to do so will cause the simulator not to resolve some features of the structure, even when the mesh density increases, and potentially create numerical "inconsistencies" in the computed results. Moreover, a smart initial mesh setting can lead to a more efficient simulation in terms of time and resources. In this work, a specific (highly dense) local mesh setting with a maximum 2 µm step is set to the dielectric layers close to the stripes of the CL-ICPW. This allows for the mesh cells to be increased only in this area, where such (spatially) fine structures are placed. In addition, in this area, representing the capacitively load stripes of the inverted coplanar line, where an intense field with a high gradient is present, the high-density mesh allows high consistency among the various simulated structures without penalizing the (overall) simulation time. In addition, starting from the initial settings, the maximum number of the mesh refinement steps, in which the simulator increases the mesh cells while checking the difference on the S-parameters, is increased from 8 to 40 steps (The minimum is kept to 3) and the minimum accepted difference is decreased from 0.02 to 0.005. The latter settings allow for further increasing the accuracy and consistency among structures. Following, for the purpose of getting a sort of an idea about the advantages of using the settings presented in this work (case 2), the simulation is compared with one of the same structure where the default initial mesh settings are used (case 1). Figure 3.17a shows the time spent on every refinement step, which even if starts much higher in the case 2 lasts for much less time than the case 1. This leads to less time consumed during mesh refinement although the number of the mesh cells is higher (fig. 3.17b). Moreover, as said before, having control of the initial mesh promotes a high consistency across simulations and structures because the refinement mesh algorithm has more initial information to better concentrate and refine the mesh only where it is needed. In fact, considering a really high initial mesh density simulation (case 3) as a reference in terms of mesh covering accuracy, fig. 3.18 shows the deviation in percentage from this simulation (case 3) on the resulting S-parameters of the cases 1 and 2, and it is possible to see how the initial mesh settings can influence the consistency across simulations. In the table 3.2 are reported the numbers of cells in the tre cases.

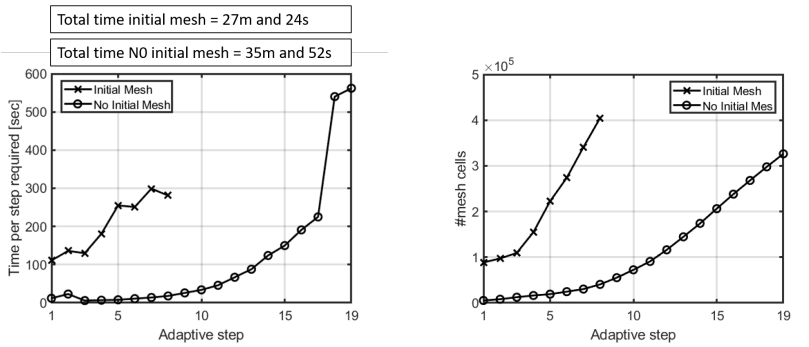
NUMBER OF MESH CELLS

No Initial settings (case 1)	Initial settings (case 2)	High Density(case 3)
326260	404590	1153964

Table 3.2.: Number of meshcells using in the mesh grid settings test

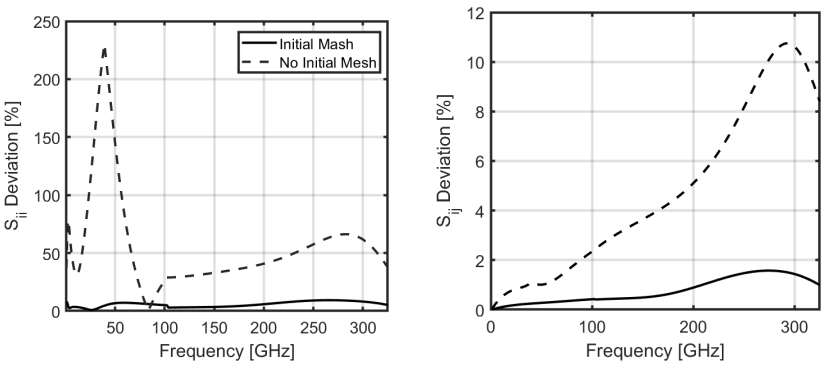
SOLVER SETTINGS

In this work, the adaptive feature of the frequency domain solver is used. This allows limiting the number of frequency points to be simulated while providing a fine cover-



(a) (b)

Figure 3.17.: a) Time spent per step of mesh refinement; b) Number of cells increment on the different refinement steps.



(a) (b)

Figure 3.18.: Deviation on the S-parameters in percentage from a high-density mesh simulation and two simulations, one with no initial mesh settings and the other one with a good compromise between accuracy and simulation time/resources. a) Deviation considering the reflection parameters; b) Deviation considering the transmission parameters;

age across the simulation band. All the extra frequency points are obtained using an interpolation procedure (implemented within the software tool). This feature reduces the simulation time but adds a new source of uncertainty due to the extrapolation of the S-parameters' behavior in between the calculated points. To limit this uncertainty, the simulator adds new points while checking the difference on the S-parameters and stops when the difference becomes smaller than a set threshold. In this work, the threshold has been reduced from 0.01 to 0.005. Due to the frequency specific characteristic of the solver, a fixed number of extra frequency points have been added to the minimum number to be computed by the solver. This allows to always obtain as faithful as possible low-frequency behavior of the port mode impedance, which would not be captured otherwise (fig. 3.19), leading to an error when renormalizing the S-parameters to 50 Ω. Specifically, 20 fixed points are added using a logarithmic spread across the simulation

frequency band. Moreover, adding these fixed frequency points increases the chances of identifying unexpected behavior across the frequency band which are sometimes not captured by the adaptive algorithm.

3.4. PRE-SILICON CALIBRATION EVALUATION ON DEVICE METRICS

Once the test fixture discussed in section 3.2 is simplified and imported into the EM simulation environment, the EM response of the various structures used in the intended calibration procedure can be numerically computed. This allows to acquire the nominal response of the various (standalone) standards (i.e., short, open, load), the response of the fixture, including wafer probes, as discussed in section 3.3, and all the various line lengths to properly realize the broadband calibration approach. Performing a broadband calibration using simulation data (considering the simulation with the RF probes as raw data in the calibration procedure) allows for validating the quality of the final product (i.e., test-fixture behavior and device-level calibrated metrics) on synthetic data.

3.4.1. M1 CALIBRATION KITS AND SIMULATION RESULTS

In this work, the two most used calibration algorithms in mm-wave ranges have been considered, i.e., the TRL and the SOLR. The quality metrics are calculated for the specific case of a calibration kit designed in a CMOS 22 nm technology in the frequency range from 1 GHz to 325 GHz. In the next paragraphs a more detailed description of the two calibration algorithms and the reasons why they are extensively used in mm-wave is given.

TRL CALIBRATION KIT IN CMOS 22NM

The TRL algorithm [11] is based on three measurements: the Thru, the Reflect and the Line. The Thru is realized as a zero-length line with a known ideal S-parameters matrix: $S_{11} = S_{22} = 0$ and $S_{12} = S_{21} = 1$. The Reflect has to provide a high-reflective termination (i.e., above 0.5) with $S_{11} = S_{22}$. This is often resolved by the knowledge of the type of Reflect, i.e., whether it is a short or an open. Since the S-parameters of a DUT, corrected using the error terms acquired by employing this calibration algorithm, will be referenced to the line's characteristic impedance, the knowledge of the characteristic impedance of the line is of key importance to allow renormalizing the data to a well-defined impedance i.e., 50 Ω. The overall knowledge requirements for the standards used by this algorithm are summarized in table 3.3. A common rule of thumb in the TRL algorithm is to ensure that the electrical length of the line is larger than 20°, in order to provide sufficient difference in the measured parameter from the thru (zero length line) response, and shorter than 160° to avoid the indetermination point which occurs at 180°. The minimum electrical length constraint limits the use of the TRL algorithm at low frequencies, especially in on-wafer measurements given the fact that it would result in extremely long

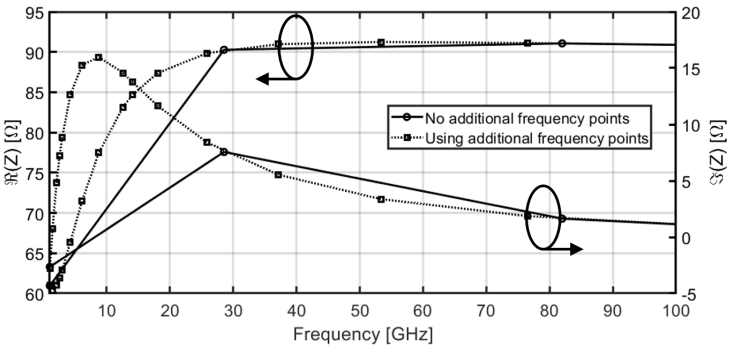


Figure 3.19.: Comparison between the waveguide port impedance using only the adaptive solving method of the simulator and adding extra frequency points in low-frequency.

TRL STANDARDS NEEDED INFORMATION	
Standards	Knowledge Requirements
THRU	$S_{11}, S_{21}, S_{21}, S_{22}$
LINE	$S_{11} = S_{22}, Z_0$
REFLECT	$S_{11} = S_{22}$

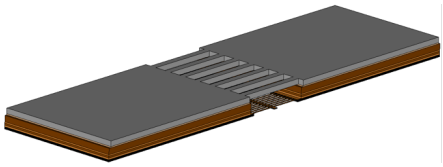
Table 3.3.: Required information about the standards using a TRL calibration.

(i.e., area-consuming) lines. The proposed calibration kit consists of 3 lines with different lengths (i.e. 70, 100, 150 µm) to cover the frequency band up to 325 GHz shown in fig. 3.20, in addition to the thru (which is realized as the bare fixture of fig. 3.3 where the DUT/STD section is omitted) and the short standard , shown in fig. 3.14. Figure 3.21 presents the characteristic impedance of the line from 1 to 325 GHz extracted from the simulated S-parameters [33] of the WR3 line using the approach reported in [50] and shown in eq. (3.3).

$$Z_0 = 50\sqrt{\frac{(1+S_{11})(1+S_{11}) - S_{12}S_{12}}{(1-S_{11})(1-S_{11}) - S_{12}S_{12}}} \tag{3.3}$$

SOLR CALIBRATION KIT IN CMOS 22NM

The SOLR algorithm [12] is a calibration procedure that requires the Short, the Open, the Load and the Reciprocal as standards (table 3.4). It requires exact knowledge of all standards through their S-parameters except for the Reciprocal, which has the only constraint of being a passive device, thus reciprocal. Figure 3.22 shows the S-parameters of the standards, obtained from EM simulations, in the frequency range from 1 to 325 GHz. The fact that it requires more information about the standard structures than the TRL, leads to a higher sensitivity to (potential) simulation errors. Despite this, the SOLR is still



$$\begin{cases} WR10\ Line\colon\ 150\ \mu m \\ WR5Line\colon\ 100\ \mu m \\ WR3Line\colon 70\ \mu m \end{cases}$$

Figure 3.20.: TRL line standards.

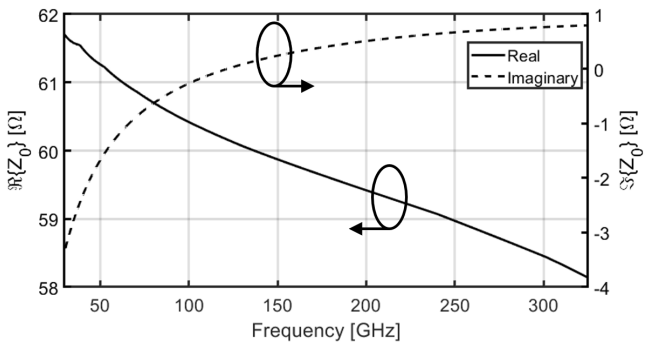


Figure 3.21.: Line characteristic impedance.

often used due to its broadband applicability without theoretical frequency limitation. The possibility of using it to an extremely low frequency without requiring a large (area consuming structure) is the reason why, in the scope of this thesis, it is used for the first calibration band i.e., up to 67 GHz. The SOLR calibration kit uses the same Thru and Reflect of the TRL as a Reciprocal device and Short, respectively. The Open, the Short and the Load are shown in fig. 3.14.

SOLR STANDARDS NEEDED INFORMATION	
Standards	Knowledge Requirements
SHORT	S_{11}, S_{22}
OPEN	S_{11}, S_{22}
LOAD	S_{11}, S_{22}
RECIPROCAL	$S_{11} = S_{22}, S_{12} = S_{21}$

Table 3.4.: Required information about the standards using a SOLR calibration.

CALIBRATION QUALITY METRIC

A metric to define the calibration quality must be selected to devise a design optimization flow that can be iteratively applied. Given the complex nature of the parameters commonly used in RF measurement labs (i.e., S-parameters) and the multiport nature

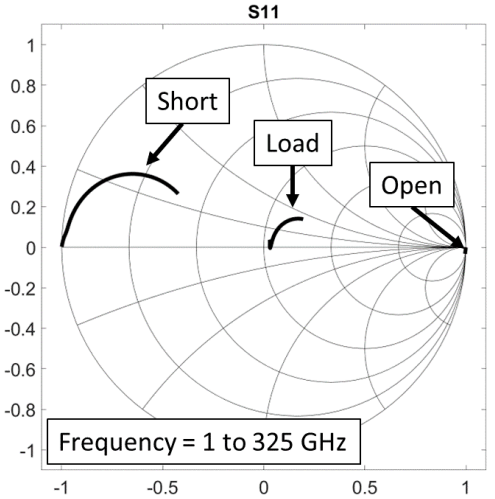


Figure 3.22.: S-paramenter response of the one-port calibration standards .

(i.e., two or more) of classical RF devices, the worst-case bound is adopted. This metric presents the worst-case of the error vector magnitude between the computed S-parameter and the reference response of the DUT used in the quality verification step. This metric, often defined as Worst-Case Error Bound (WCEB), is often employed in RF metrology papers and is defined as.

$$WCEB = max|S_{ij}^{Cal} - S_{ij}^{Ref}| \quad i,j = 1,2 \tag{3.4}$$

where S_{ij}^{Cal} represent any of the 2-port S-parameters obtained after the calibration process and S_{ij}^{Ref} the one of the reference structures. For carrying out more detailed information, a simple Error Bound (EB) for each parameter can be calculated, as shown in eq. (3.5).

$$EB = |S_{ij}^{Cal} - S_{ij}^{Ref}| \quad i,j = 1,2 \tag{3.5}$$

Using the value of the EBs, a worst-case error bound can also be extracted on the final intrinsic DUT's parameters using a Montecarlo analysis. This can be done by synthesizing the error on the DUT S-parameters and then calculating the intrinsic parameters or figure of merit (fig. 3.26). Since the S-parameters are correlated and the EBs are obtained considering a matched line, a simple addition on the single S-parameter independently would not be realistic. To maintain the correlation between the four S-parameters and considering the value of the device S-parameters and/or its possible mismatch, the error can be synthesized using fictitious calibration (e.g., SOLT calibration with ideal standards). A random error combination is added to the standards of simulated (i.e., based on combination of synthetic data) calibration, calculating the relative error terms. These error terms are then used to calibrate the reference line S-parameters and calculate the new relative EBs. At this point, only the combinations, and thus the error terms set, that satisfy the condition for which all the EBs are below the reference EBs are considered.

These error term sets are used to calibrate the device's S-parameters and calculate its relative parameters. Repeating this algorithm in a Montecarlo analysis a bound around the intrinsic device parameters can be created. For clarity, in fig. 3.24, the flow diagram of the algorithm used for extracting the bounds on the device's parameters starting from the knowledge of the EBs is shown.

CALIBRATION KIT VERIFICATION AND ACCURACY ASSESSMENT

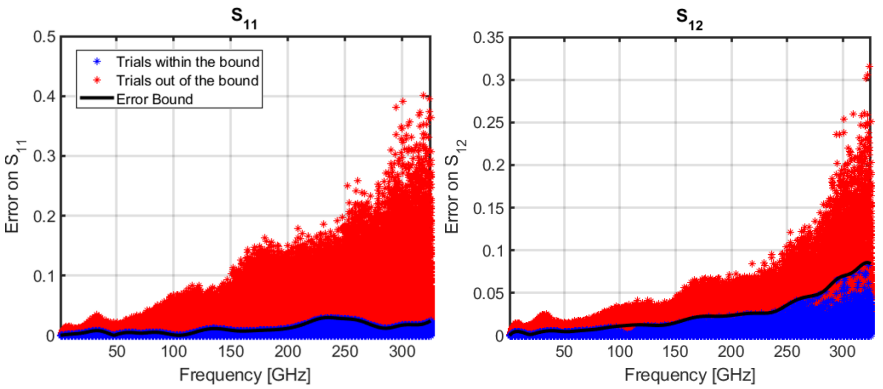
Finally, the TRL and the SOLR calibrations are performed using simulated data to assess the calibration accuracy set by the accuracy and consistency of the simulations. The probes added in the simulation, as shown in fig. 3.12, and the fixture described in the section 3.2.2 have been used to emulate the contribution of the measurement setup. All the required structures needed to complete the two calibrations have been simulated. After computing and applying the calibration, the two WCEB have been extracted using as DUT/Reference the WR3 line and are shown in fig. 3.25. As expected, the TRL calibration, compared to the SOLR, shows the minimum WCEB due to the reduced quantity of information needed and, thus, the chances of error passed to the algorithm. Given the equivalent model of a device, applying the procedure explained previously (see section 3.4.1) and considering the EBs calculate using the eq. (3.5), it possible to extrapolate the parameters' bounds, after using the subset of calibrations satisfying the condition shown in fig. 3.23. The final bound is asymmetrical, which means that it has been extracted by considering the upper and lower values separately with respect to the reference. In the specific case, it is calculated as the limit for which 99% of the values are closer to the reference (fig. 3.26a). In fig. 3.26a the result from the nominal TRL calibration, the complete set of the 1000 trials and the 2 bounds extracted are shown. The final bound for the Gate-Source Capacitance (Cgs), obtained using the calibration kit designed in this work, for the TRL and the SOLR calibration, is presented in fig. 3.26b. Using the same approach, the error bounds of the most common CMOS parameters are also calculated and shown in fig. 3.27. Apart from the discussion about the comparison of the two calibration algorithms, which is interesting in understanding the limitations of the single algorithm, the scope of this work is to show, in the pre-silicon design stage, the usability of the calibration kit and the fixture to obtain a high-quality calibration without erroneous behaviors which could not be achieved without the proposed design/validation flow. Analyzing the synthetic results predicted by the proposed flow, we can identify the expected accuracy during the experimental steps, as shown in fig. 3.26 providing less than ±300 aF at 300 GHz.

3.5. EXPERIMENTAL SETUP

3.5.1. MEASUREMENT SETUPS

The measurement session has been done in the band from 1 GHz to 325 GHz employing 5 different setups:

1. From 1 to 67 GHz;



(a) (b)

Figure 3.23.: EB points distribution among all the trials: a) Error bound on S11; b) Error bound on S12

2. WR10 waveguide band (i.e., From 67 to 110 GHz);
3. WR6.5 waveguide band (i.e., From 110 170 GHz);
4. WR5 waveguide band (i.e., From 140 to 220 GHz);
5. WR3 waveguide band (i.e., From 220 to 325 GHz);

All the setups employed the Keysight parameter analyzer E5270B as a power supply. A TU Delft-Van Swinden Laboratory (VSL) jointly developed probe station, see fig. 3.28, employing 4 piezo actuators (for x, y, z and tilt control) from Newport, per each manipulator, allowing a step resolution of ≈20 nm. The station allows for remotely controlled alignment and landing procedures, thus minimizing the vibration arising from operator contact with the probe station. The setup for the lowest band (setup 1) uses a Keysight N5227A 67 GHz PNA, while for the higher bands (setups 2 to 5), a VNA-X test bench was used. The VNA-X consists of a VNA with frequency extenders, which are based on a frequency multiplier for the up-conversion chain to bring the operation frequency to the desired measurement frequency band, and an RF mixer for the down-conversion chain [7]. The specific vendors for the various modules are OML Inc. for the WR10 and WR3 bands. and Virginia Diodes for the WR6 and WR5 bands. The RF probes used are Form Factor infinity probe 100 µm pitch for the lowest band, WR10, WR6 and WR5 band, and GGB 75 µm pitch for the WR3.

3.5.2. LAYOUT MAP

Figure 3.29 shows the layout map containing the different devices to be characterized together with the relative calibration kits and the de-embedding structures (i.e., open and short). In fig. 3.29, the structures that have been considered in this work are highlighted. The device under test is an N-channel Metal-Oxide-Semiconductor (NMOS) Fully Depleted Silicon-On-Insulator (FD-SOI) 22 µm with 16 fingers.

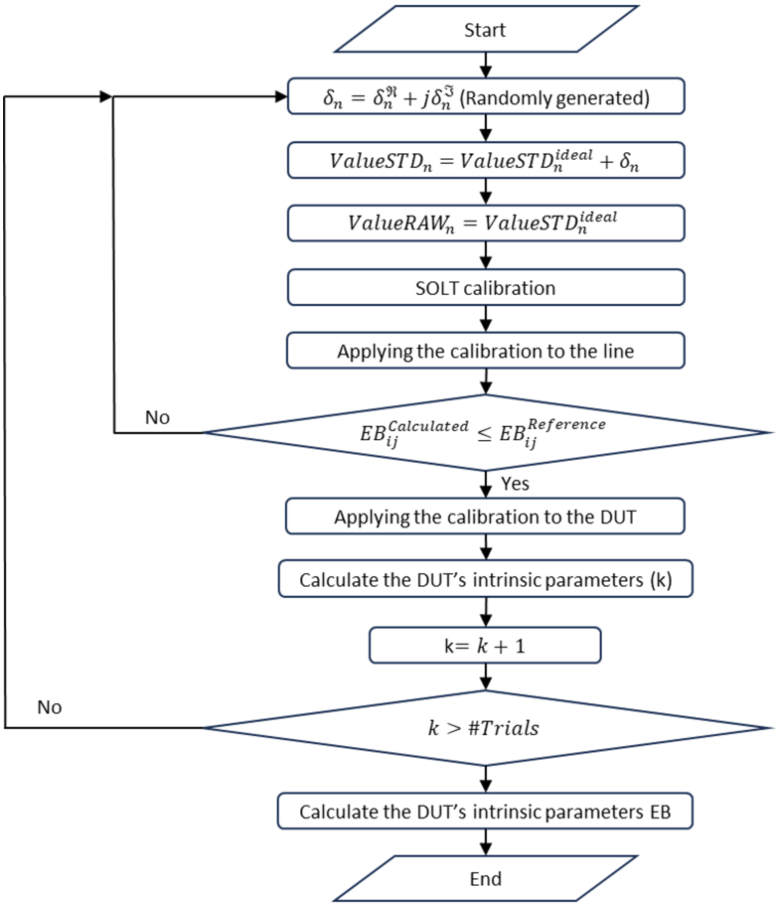


Figure 3.24.: Diagram flow of the algorithm for calculating the EB on the DUT's intrinsic parameters.

3.6. EXPERIMENTAL RESULTS

In order to evaluate the quality of the realized calibration, the WCEB metric discussed in section 3.4.1 is being computed for the various characterization bands and extracted for the TRL and the SOLR(<67 GHz) using a WR3 line as a reference DUT and it is shown in fig. 3.30. The WCEB extracted from the measurements, shown in fig. 3.30, is higher than the simulated one, which is an expected result, since has already been said that the WCEB contains only deviations coming from the simulation while the one from the measurement includes all the measurement imperfections. Finally, the measurements confirm what was predicted by the pre-silicon analysis done in this work. This calibration kit and fixture are able to provide an accurate device-level calibration without any further design iteration. In fact, the WCEB shown in fig. 3.30, shows an error confrontable with the state-of-the-art top metal calibrations [33].

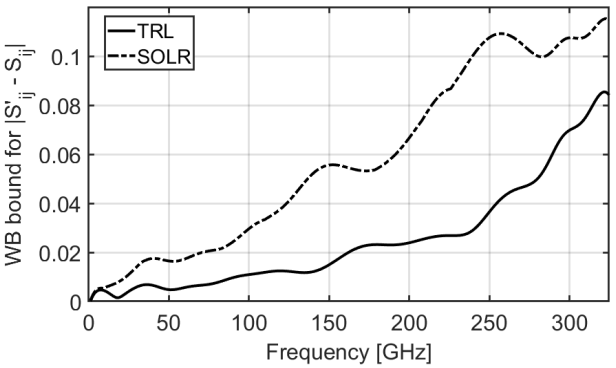


Figure 3.25.: WCEB for calibration kit verification.

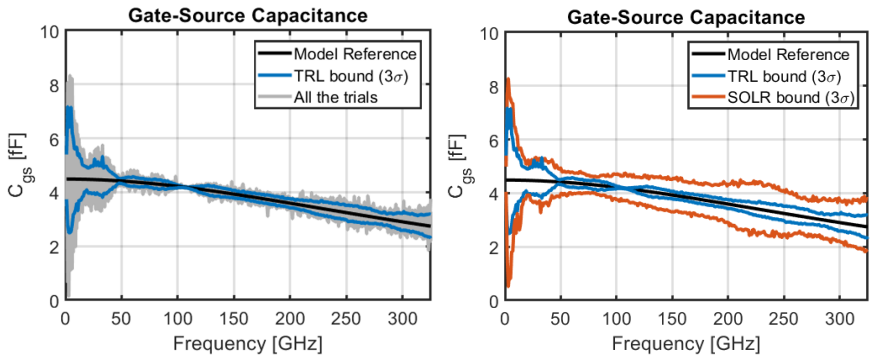


Figure 3.26.: a) The complete set of the 1000 trials (Blue) and the Cgs error bound extracted representing 99% of the values. b) The final Cgs error bound for the TRL and SOLR calibration together with the model reference.

3.6.1. DEVICE MEASUREMENT

Figure 3.31 shows the S-parameter measurement of GF NMOS FD-SOI 22 µm obtained using a SOLT/TRL M1 calibration. To increase the correlation between the measurement data and the PDK model, an extra open short de-embedding step after the M1 calibration plane is added, as discussed in [21], to remove the remaining intrinsic fixture (fig. 3.4). It is important to note that different frequency banded probes, different calibration kit artifacts (i.e., using structures from different dies) and thus different transistors have been used in the measurement campaign. As was mentioned in [51] this can lead to discontinuities at measurement band edges. Moreover, these discontinuities can be attributed to both calibration uncertainties as well as process variations. A very good agreement between the model and the measurement across the entire frequency band considered can be observe in fig. 3.31, which results in a good agreement of the parameters as well (see

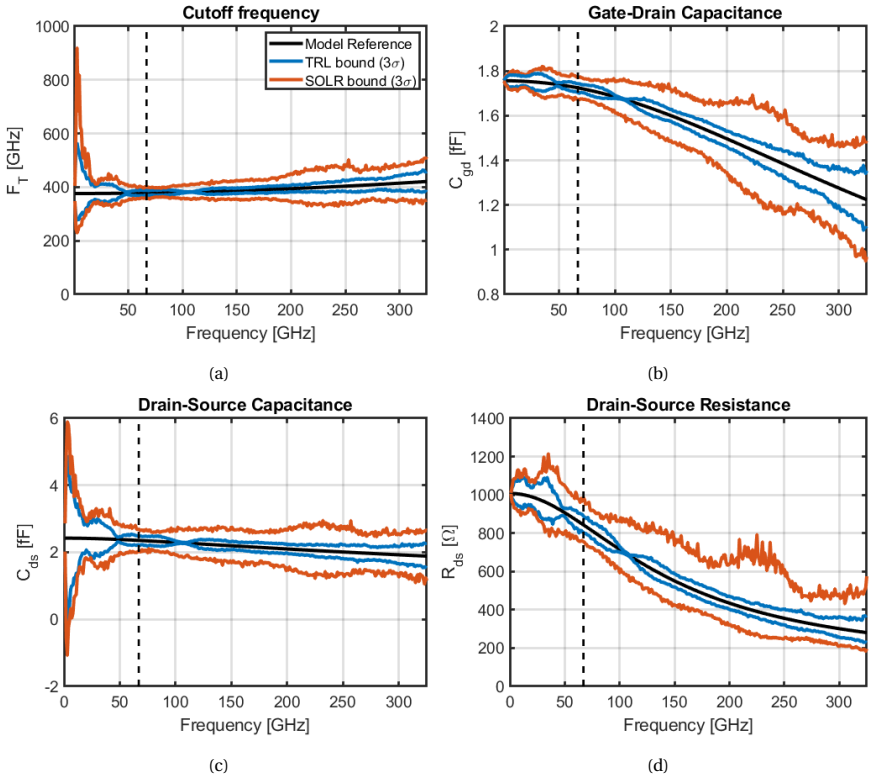


Figure 3.27.: EBs calculated using directly the parameters of the device's model. Black line - reference value; Blue line – TRL error bound; Red line – SOLR error bound. The vertical dashed line shows the frequency threshold between the SOLR and the TRL

fig. 3.32). The reader can observe some of the measured parameters go out of numerical uncertainty bounds because, as explained previously, those bounds estimate the lowest amount of uncertainty expected using the calibration kit discussed in this work. In fact, the measurement results contain not only the error due to the calibration kit accuracy but also a sum of different sources of errors coming from the instrument noise, probe positioning error, probe-to-probe, and substrate coupling [41, 52].

3.7. CONCLUSIONS

A procedure for a pre-silicon verification of an on-wafer calibration kit designed in a CMOS back-end of Line is presented. The work first presents a semi-automatic procedure to design the layout of the test fixture combining together basic elements, and then describes the flow for an easy and faithful importing in the 3D electromagnetic simulator (i.e., CST). The calibration kits for a Thru-Reflect-Line and Short-Open-Load-Reciprocal calibration have been simulated to evaluate their accuracy in terms of the worst-case

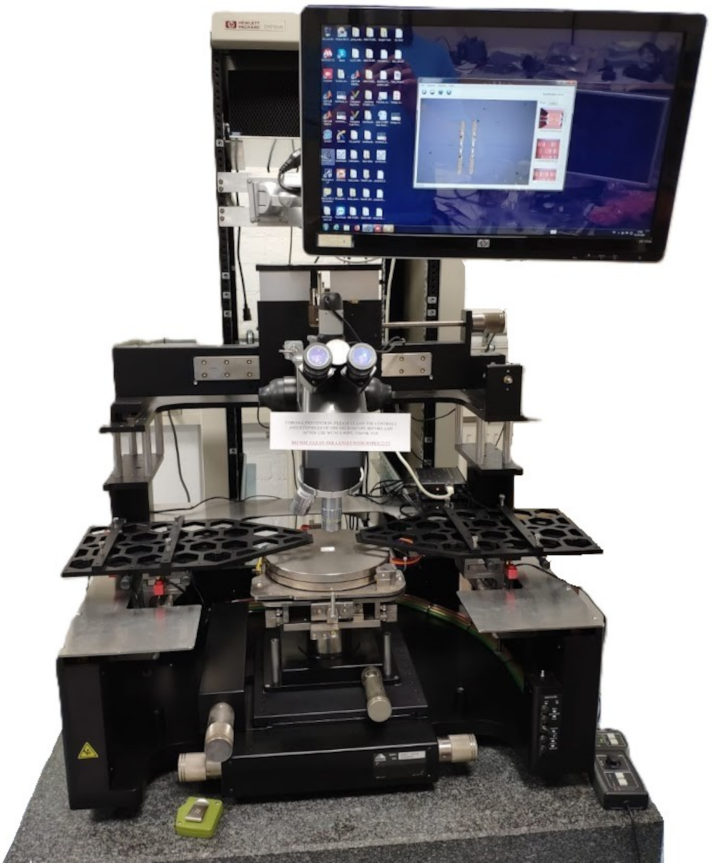


Figure 3.28.: In-house made semi-automatic probe station.

error bound. The WCEB shows a good calibration accuracy, reaching a maximum error of around 0.12 for the SOLR and 0.08 for the TRL. Calculating also the EBs on the four S-parameters allows the propagation of bound directly on the DUT's intrinsic parameters, using a Montecarlo analysis, which shows a very small error bound on six different device parameters (e.g., ±25 GHz on the FT and ±0.5 fF on the Cgs). Finally, the measurements in the frequency band from 1 to 325 GHz have been carried out, showing a very good agreement with the device model in the entire frequency band in terms of S-parameters and intrinsic device parameters.

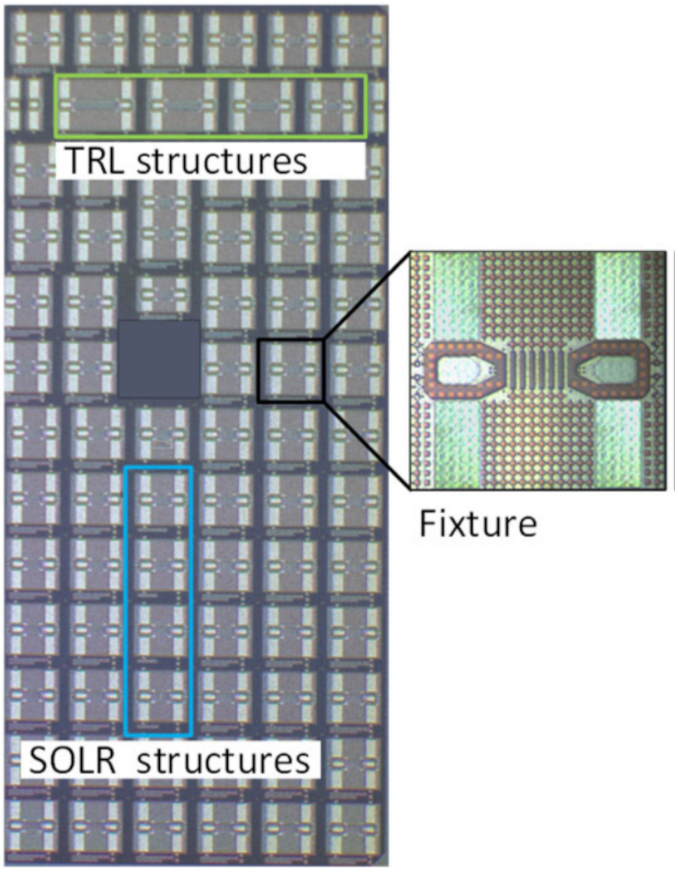


Figure 3.29.: Layout Map.

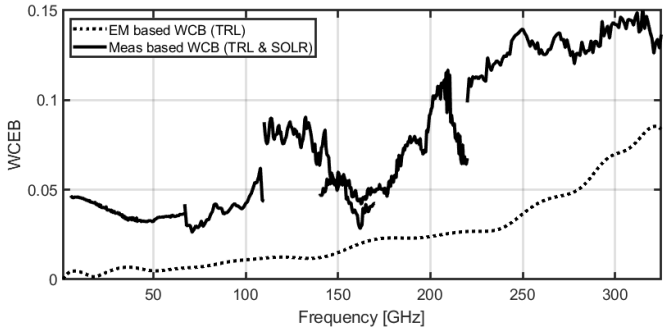


Figure 3.30.: WCEB extracted from measurement using a WR3 line as reference.

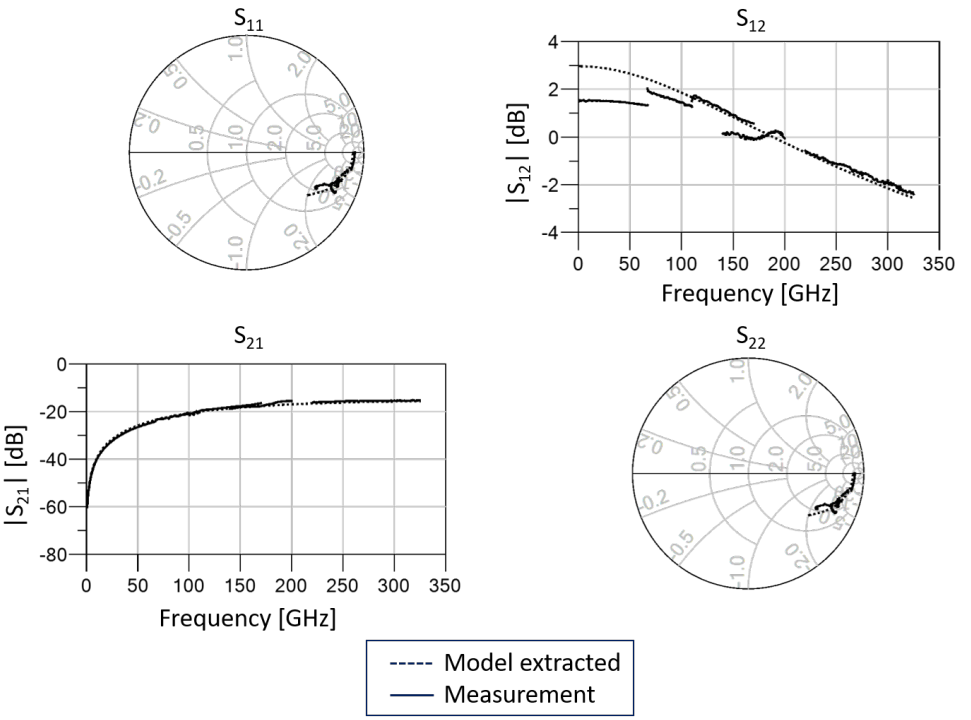
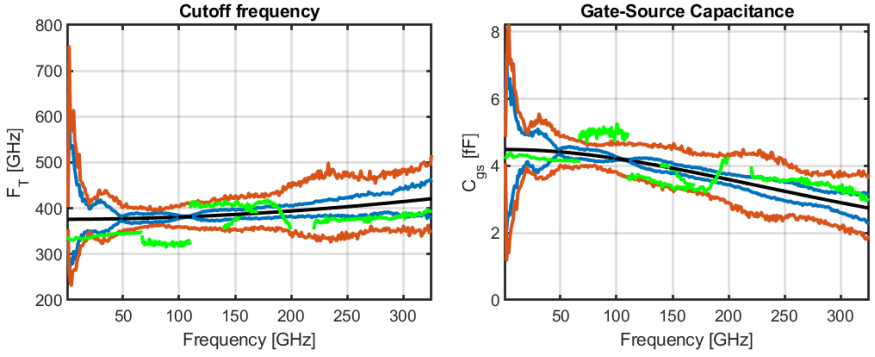
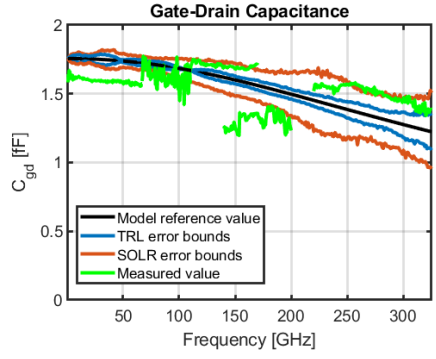


Figure 3.31.: S-parameter DUT.

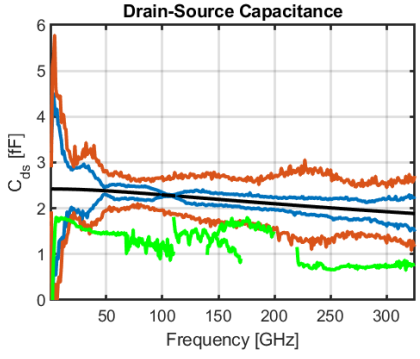


(a)

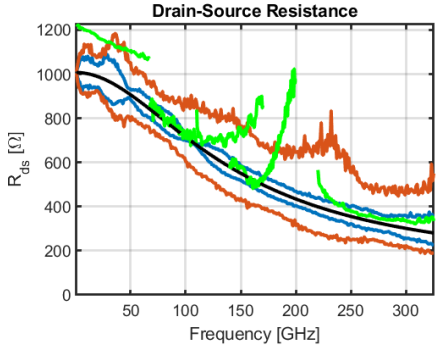
(b)



(c)



(d)



(e)

Figure 3.32.: Device Parameters and the relative individual bounds.

4

M1 Test fixture Enhancements: Small and Large Signal

This chapter addresses two enhancements that can be implemented when employing the M1 test fixture discussed in chapter 3. As was discussed, the M1 test fixture is designed to shift the first-tier calibration plane in close proximity to the DUT; this implies that the pad discontinuities and also protection circuitry are all embedded in the error terms of the calibration and potentially lead to small variation in the response across the bias ranges used in the DUT characterization. A structured calibration approach to incorporate these fluctuations in the primary calibration is then presented in this chapter, removing the residual error that might arise. A detailed mathematical analysis is presented, initially validated through circuit-level simulations utilizing exclusively S-parameter-defined error boxes and ideal lumped components. Subsequently, the analysis is verified using 3D electromagnetic simulations of the test fixtures. The circuit-level simulator confirms the mathematical analysis, while the 3D EM simulator validates the applicability in a more realistic setting. Finally, the proposed method is used in a real measurement where the test fixture, similar to the one presented in chapter 3, is implemented in a 28 nm *CMOS technology and characterized at frequencies between* 140 GHz *and* 200 GHz. *The measurement using the proposed method clearly shows reduced deviation from known reference compared to the non-split approach. Furthermore, the proposed M1 calibration approach, as shown in chapter 3, allows for close to intrinsic device response up to sub-mm-wave, which allows for the active device response in the large signal calibration process. In this chapter, we also present a* 28 nm *CMOS n-channel MOSFET employed as a power calibration transfer device, providing sufficient responsivity up to* 325 GHz. *The square-law conversion from mm-wave (RF power) to DC (voltage) through the CMOS device is employed to achieve a direct on-wafer power calibration. The use of the calibration transfer*

Parts of this chapter have been published in "A TRL Error-box Split Procedure to Compensate for the Bias Dependency Effects in Device Test-Fixtures (2019) [46]" and "Direct mm-Wave On-Wafer Power Calibration Employing CMOS as a Transfer Device (2018) [53]".

device allows for a (power) calibration procedure of a mm-wave measurement setup with zero extender movements, thereby minimizing errors associated with cable movements and reducing calibration time compared to the standard calorimeter-based procedure. The approach is experimentally benchmarked against the power meters procedure in the WR5 band (from 140 GHz *to* 220 GHz*), showing a maximum error propagated through the calibration equations, over the entire band and multiple devices, lower than* 1 dB.

4.1. INTRODUCTION

In the previous chapters, we reviewed how calibration is a procedure that generates a set of error terms to compensate for the effect of the measurement setup and highlighted the impact of calibration errors in device modeling extraction. The calibration process can incorporate numerous sources of error. Nevertheless, a fundamental assumption for an accurate and consistent calibration is that the electrical response of all components in the measurement setup remains constant throughout the calibration and measurement phases. This is true in most cases, aside from the inevitable drift due to the temperature fluctuation in the measurement environment. When a direct M1 calibration is employed, the ESD/Antenna [54] protection diodes are placed within the first tier calibration path, i.e., in the case considered in this work at the vertical transition section. It is important to mention that those protection diodes are strictly required in ultra-scaled CMOS nodes, even when dealing only with R&D test structures. These components can exhibit a bias-dependent behavior, which can induce a bias-dependent error in the calibration. To address this, this chapter presents a calibration procedure denoted as "split TRL" to incorporate the bias dependency of the test fixture in the first tier TRL. The proposed solution is obtained by combining two different error boxes, T_A (at port 1) and T_B (at port 2), which are calculated under different bias conditions. After introducing the mathematical base of the split and recombination of the TRL error boxes, the method's effectiveness is validated by employing a circuit-level simulation (Keysight ADS) where S-parameter-defined error boxes are used. This is followed by a 3D EM simulation (CST microwave studio) using a generic CPW transmission line for the test fixture. Finally, the approach is verified through measurements on devices fabricated in a 28 nm CMOS technology, characterized across the 140 GHz to 200 GHz frequency range, demonstrating its applicability in a realistic measurement environment.

4.2. A TRL ERROR-BOX SPLIT PROCEDURE TO COMPENSATE BIAS DEPENDENCY EFFECTS IN M1 TEST-FIXTURES

4.2.1. ESD DIODES AND THEIR EFFECTS ON THE MEASUREMENTS

To survive the fabrication process and the (machine or human) handling during assembly, integrated devices need to be protected by on-purpose designed structures (i.e., diodes). These structures can then route the electro-static discharge event, which occurs during the fabrication and handling processes, away from the device areas that would not withstand those sudden high-voltage events. For this reason, it is recommended that the ESD protection device be placed in proximity to the DUT. When employing a M1 text fixture, these protection devices can be incorporated after the vertical transition, as shown in figs. 4.1a and 4.1b. This contribution employs an nMOS fabricated in a 28 nm CMOS technology and embedded in the M1 TRL-compatible test fixture fig. 4.1b. The calibration/de-embedding procedure is based on an M1 level TRL following the method presented in [25] and discussed in chapter 3. The ESD protection circuitry considered in this work consists of a six-diode antiparallel configuration, with three diodes in series in

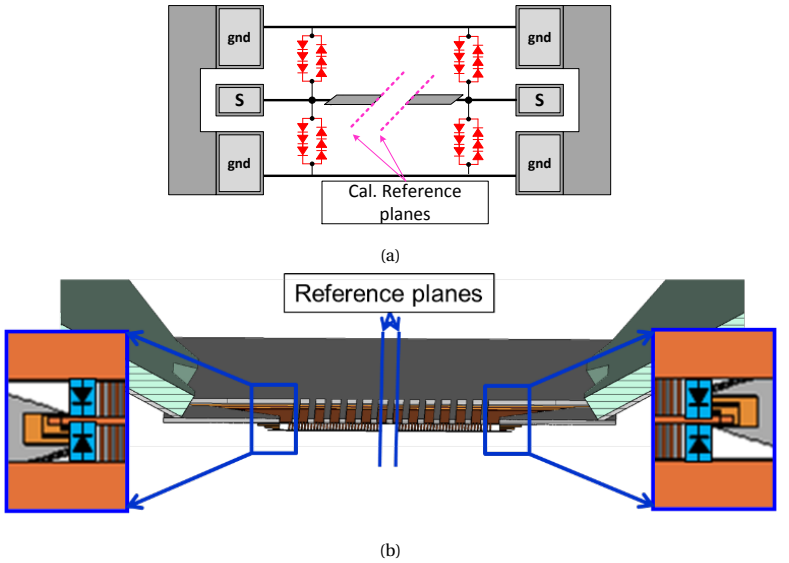
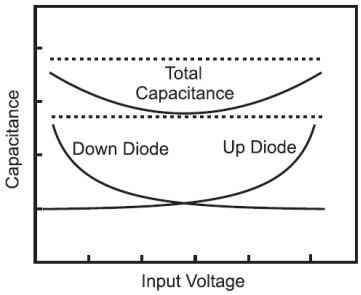


Figure 4.1.: a) Simplified representation of the fixture with embedded ESD protection devices (shown in red). b) The placement of the ESD diodes in the M1 Test fixture realized using 28 nm CMOS technology.

each branch, placed symmetrically on both sides of the (M1) line connecting the DUT. It is important to note that although the ESD protection diodes are designed to operate only in case of an electrostatic discharge event, their impedance (capacitance) is bias-dependent. This dependency comes partly from the junction capacitance variation of the diodes, as shown in fig. 4.2 [54] where the contribution of the two diode branches of fig. 4.1b are summed. The effect of the diode impedance variation can also be observed directly in the measurements. In see fig. 4.3a the S_{21} variation over the bias of a thru line embedded in the considered fixture is shown as function of the frequency. The line response, which would be constant without the presence of diodes, changes when the voltage on the fixture is modified. A variation of more than 0.1 dB (see fig. 4.3b), varying the voltage from 0 V to 2.5 V at 140 GHz, is observed.

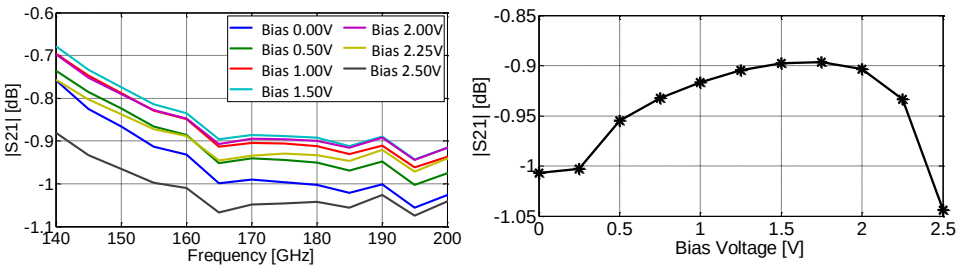
4.2.2. SPLIT TRL

The TRL calibration algorithm allows calculating the ETs in the form of T-matrixes, T_A and T_B (fig. 4.4), by measuring three standards: a thru connection, a symmetric reflect and a line [11]. When the ESD protection diodes are placed inside the fixtures, their perturbation and dependency on the applied voltage translate into bias-dependent error boxes. The dependence does not influence the measurements if the voltage is the same on the two ports. In this case it is indeed possible to perform the calibration directly at those voltage values (port 1 and port 2) using an “open” as reflect and applying the same (bias) conditions used during the calibration in the measurement phase. Typically, this condition (symmetric biasing of ports 1 and 2) cannot always be satisfied. For ex-



$$C_j(V) = \frac{C_o}{\left[1 - \frac{V}{V_o}\right]^{1/2}}$$

Figure 4.2.: Expected capacitance variation of the ESD protection diode due to the sum of the two branch C_j variation [54].



(a) (b)

Figure 4.3.: Measured S_{21} over a thru line embedded in the fixture at different bias levels. b) Variation of |S21| of the thru line embedded in the fixture changing the voltage at 180 GHz

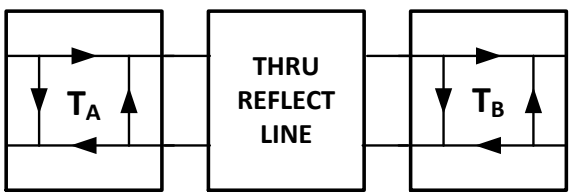


Figure 4.4.: Graphical representation of the 8-terms error model.

ample, when measuring an active device, it may be necessary to apply different voltages to the various terminals. In this case, a deviation from the original calibration is introduced, which can be mathematically modeled as an additional error box representing the perturbation component. The resulting discrepancy can be eliminated by combining the two error boxes obtained from calibrations performed at different bias points. This is true, provided that the perturbation is caused by a reciprocal network, as can be shown by the following mathematical analysis. Considering the conversion of the two T-parameter matrices of the error boxes into the S-parameters notation, employing the

well-known conversion formulas, yields to eqs. (4.1) and (4.2).

$$T_A = \frac{1}{S_{21}^A}\begin{bmatrix} -\Delta & S_{11}^A \\ -S_{22}^A & 1 \end{bmatrix} = K^A R_n^A \tag{4.1}$$

$$T_B = \frac{1}{S_{21}^B}\begin{bmatrix} -\Delta & S_{11}^B \\ -S_{22}^B & 1 \end{bmatrix} = K^B R_n^B \tag{4.2}$$

Where R_n^A and R_n^B are the two normalized T-matrixes and K^A and K^B are two coefficients that are considered equal to $1/S_{21}^A$ and $1/S_{21}^B$, respectively, in case the error boxes are reciprocal. The TRL algorithm provides the matrixes R_n^A and R_n^B and the product $K^A K^B$ [11]. As such, after some mathematical manipulation of eqs. (4.1) and (4.2) one can isolate K^A and K^B individually, resulting in eqs. (4.3) and (4.4) , respectively.

$$K^A = \frac{1}{\sqrt{S_{12}^A S_{21}^A}} \tag{4.3}$$

$$K^B = \frac{\sqrt{S_{12}^A S_{21}^A}}{S_{21}^A S_{21}^B} \tag{4.4}$$

Considering the calibration scenario with a perturbation added only on port1 (T_P) as given in fig. 4.5, where the transmission matrix T_P of the perturbation can be described in terms of its S-parameters as eq. (4.5).

$$T_P = \frac{1}{S_{21}^P}\begin{bmatrix} -\Delta & S_{11}^P \\ -S_{22}^P & 1 \end{bmatrix} \tag{4.5}$$

In this new scenario eqs. (4.3) and (4.4) can be written as eqs. (4.6) and (4.7).

$$K^A = \sqrt{\frac{(S_{22}^A S_{11}^P - 1)^2}{S_{12}^A S_{21}^A S_{12}^P S_{21}^P}} \tag{4.6}$$

$$K^B = \frac{(S_{22}^A S_{11}^P - 1)\sqrt{\frac{S_{12}^A S_{21}^A S_{12}^P S_{21}^P}{(S_{22}^A S_{11}^P - 1)^2}}}{S_{21}^A S_{21}^B S_{21}^P} \tag{4.7}$$

From eq. (4.7) it is possible to observe that if the component that represents the perturbation is reciprocal ($S_{12}^P = S_{21}^P$)K^B is equal to the one in the eq. (4.4), i.e., no perturbation. In order to finally conclude that T_B is equal in both of the two previous cases, it is still required to demonstrate that R_n^A and R_n^B are independent. However, given T_A(eq. (4.1)), T_B(eq. (4.2)), and T_P(eq. (4.5)), and using the TRL equations (eq. 40, 41 and 46 from [11]) the independence of the two renormalized matrixes from the perturbation immediately come out. Therefore, it is possible to conclude that when T_P is reciprocal the matrix T_B calculated with and without perturbation are the same and thus independent from what is present at port 1. This mathematical demonstration shows that performing two different calibrations at the respective device operating voltage values (fig. 4.6a) allows one to

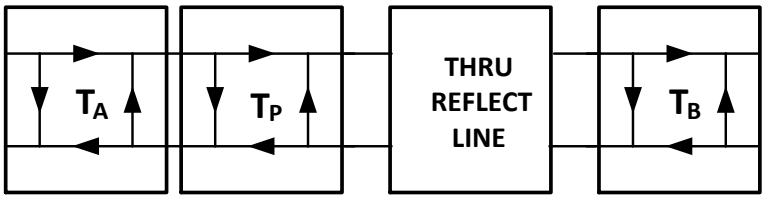
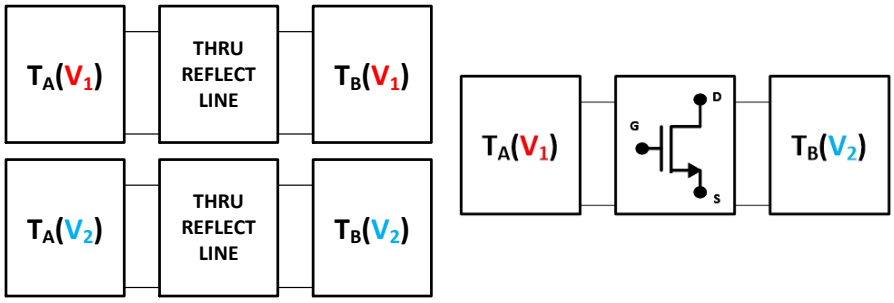


Figure 4.5.: Calibration scenario with perturbation box.



(a) (b)

Figure 4.6.: Calibration scenario at two different bias voltages (V_1 and V_2). b) Measurement scenario employing the split TRL. The error boxes coming from two different calibrations performed at different bias points are combining

combine their two error boxes, since the perturbation on one port does not impact the matrix at the opposite port. For this reason an accurate calibration can be obtained as shown in fig. 4.6b without introducing an error in the measurement. A set of simulations where performed to validate the proposed split TRL technique. First, an ADS simulation was carried out. This simulation consists of two sources and two error boxes with a set of S-parameters representing the measurement setup without any ESD protection diode effect. Two capacitances are then added to the schematic to include the ESD diode (bias-dependent) perturbation (fig. 4.7).

The verification consists of the 3 steps:

- A first TRL calibration is performed using the same value ($C_{p1} = C_{p2} = C_1$) of capacitance for both components. This would represent the two ESD protection diodes at the same voltage value (V_1).
- A second TRL calibration using the same value ($C_{p1} = C_{p2} = C_2$) of capacitance for both components is then carried out. This would represent the two ESD protection diodes at the same voltage value (V_2).
- The two calibrations are then combined to correct a simulation on the known S-parameters block where the first capacitance value is used for port 1 and the second one for port 2 ($C_{p1} = C_1$ and $C_{p2} = C_2$).

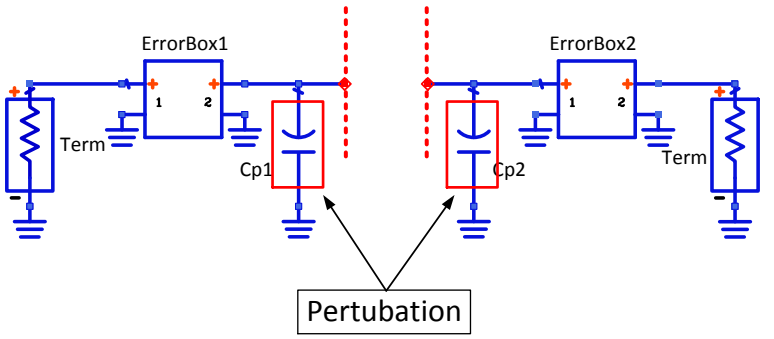
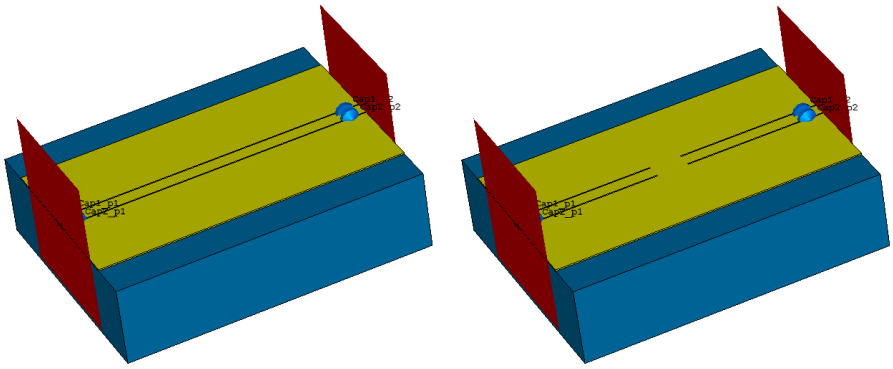


Figure 4.7.: ADS simulation using as a perturbation in the fixture two capacitances that would represent the bias-dependent ESD protection diode effect.

For this simulation, two different capacitance values were used: $C1$ =1 fF and $C2$ =5 fF. Those capacitance values are assumed to represent realistic values for the parasitic capacitance of the ESD or antenna protection diode in a fixture for the WR5 frequency band. The result of this simulation is that the proposed approach does not introduce any error, as expected. To validate the technique in a more realistic environment and to check if some parasitic effect can influence the results, 3D EM simulations are performed using CST microwave studio (fig. 4.8) in the frequency range from 75 GHz to 325 GHz. To simplify the structures a CPW in vacuum ($\epsilon_r = 1$) is considered to build the standards necessary for the TRL algorithm. The ESD protection diodes are included in the simulation by placing two lumped capacitors (through the usage of lumped ports), with the same value, symmetrically to the line for each port, as shown in fig. 4.8. To be consistent, the same procedure and the same capacitance values are used for the ADS analysis. The result, shown in fig. 4.9 as the maximum deviation of all the two-port S-parameters from the reference (Worst Case Error Bound), shows clearly that in case of a non-accounted (standard TRL) perturbation (i.e., ESD protection diode capacitance variation) an error arises in the fixture removal performed by the calibration. Moreover, it shows that, if a split TRL procedure is used, an error comparable to the one achievable using the TRL calibration in the mm-wave frequency range can be achieved.

4.2.3. EXPERIMENTAL RESULTS

In order to experimentally validate the proposed (split TRL) procedure, a reference measurement must first be defined. A direct TRL, i.e., with the desired bias value (V_1 at port 1 and V_2 at port 2) at the M1 calibration (M1 Cal) planes (see fig. 4.10) is not possible. This is due to the requirement to use a thru and line connection, which requires the same port voltages during the calibration. Moreover, note that using the zero-bias value of the open standard as a constant reference device is also not possible, since the substrate crosstalk varies with bias. For the above-mentioned reasons the Pads calibration (Pad Cal) planes were used to obtain the reference measurement to validate the procedure using as bias conditions $V_1 = 1.5\,\text{V}$ and $V_2 = 0\,\text{V}$. The following steps describe the



(a) (b)

Figure 4.8.: 3D design of the standard loads in CST: a) Thru/Line/Dut; b) Short.

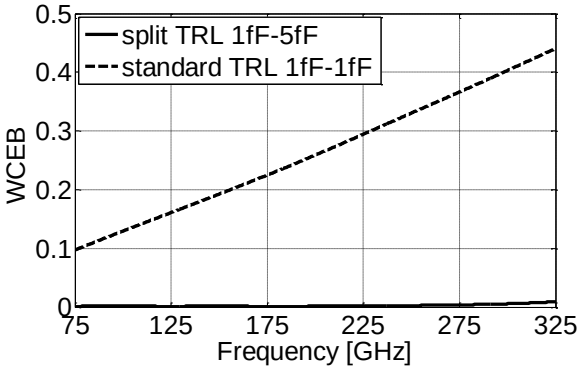


Figure 4.9.: WCEB obtained using a TRL split technique (solid line) and using a standard TRL calibration (dashed line).

experimental validation procedure:

1. Perform a Pad Cal at zero bias. Note that this calibration does not contain any ESD protection device and its accuracy is independent of the applied bias.

2. Perform two M1 Cal at $V_1 = V_2 = 1.5\,\mathrm{V}$ and $V_1 = V_2 = 0\,\mathrm{V}$.

3. Use the Pad Cal and M1 Cal to calculate the two T-matrixes ($\mathrm{Fix_A}$ and $\mathrm{Fix_B}$) for the condition $V_1 = V_2 = 1.5\,\mathrm{V}$ and $V_1 = V_2 = 0\,\mathrm{V}$ (fig. 4.10a)

4. Obtain the S-parameters of the open at the pads using the Pad Cal with $V_1 = 1.5\,\mathrm{V}$ and $V_2 = 0\,\mathrm{V}$ (fig. 4.10b), i.e., reference data.

5. Obtain the S-parameters of the open at M1 using the split TRL technique with the same voltage settings of step 4 (fig. 4.10c).

6. De-embed the fixtures by using the relative T-matrixes ($Fix_A(V_1)$ and $Fix_B(V_2)$), calculated in step 3, from the S-parameters obtained in step 5 to find the S-parameters of the open at the pads (fig. 4.10d).

7. Finally, calculate the S-parameters at the pads using the same procedure in step 6 but with the T-matrixes at 0 V (standard TRL).

Figure 4.11 shows the S_{11} and the S_{22} for the case computed from step 6 (split TRL) and step 7 (standard TRL) compared with the reference measurement at the pads computed from step 4. As shown in fig. 4.11, the S_{11} obtained using the split TRL approach is basically on top of the reference (step 1) showing only a small error because two different calibrations are employed. Instead, the S_{11} computed from the standard TRL performed at zero bias shows an evident deviation from the reference. Since the bias at port 2 doesn't change in both cases, the S_{22} doesn't show an error as expected.

4.3. DIRECT MM-WAVE ON-WAFER POWER CALIBRATION EMPLOYING CMOS AS A TRANSFER DEVICE

Continuing in the direction of complementing the on-wafer device characterization, moving from small-signal to large signal excitation, one key step is required, i.e., knowledge of the absolute power at the input and output of the device. The classical procedure [9] uses a power meter operating in the mm-wave range (i.e., Vdi PM5 [55]) to provide the absolute power reference value, requiring first a calibration and measurements at the waveguide port of the frequency extenders. Although this approach is accurate, from the procedure standpoint, the calibration process is hampered by module movements, which reduce the method's precision, particularly when targeting final on-wafer measurements, and require extensive handling and mounting efforts from the operator. To overcome these limitations, the second part of this chapter proposes the use of square-law detectors integrated into the M1 device fixture, capable of operating up to the sub-THz region, as a Power Calibration Transfer Device (pCTD). This approach aims to address the current challenges in broadband on-wafer power measurements due to the lack of an on-wafer broadband power meter and thus to increase the direct usability of vector power calibration methods while reducing the calibration/handling efforts and movement-related errors.

4.3.1. STANDARD MM-WAVE SETUP CALIBRATION

When targeting power leveled or large signal on-wafer measurements using a mm-wave extender VNA based as shown in [9], a large effort is devoted to the calibration procedure. The on-wafer setup, i.e., probe station and manipulators, makes the required movements for the waveguide level TRL calibration a very cumbersome process, requiring large cable movements thus hampering the accuracy of the final calibration. The entire procedure can be divided into the following steps, as also shown in fig. 4.12:

- Standard two-port calibration at the waveguide ports of the extender (i.e., TRL).

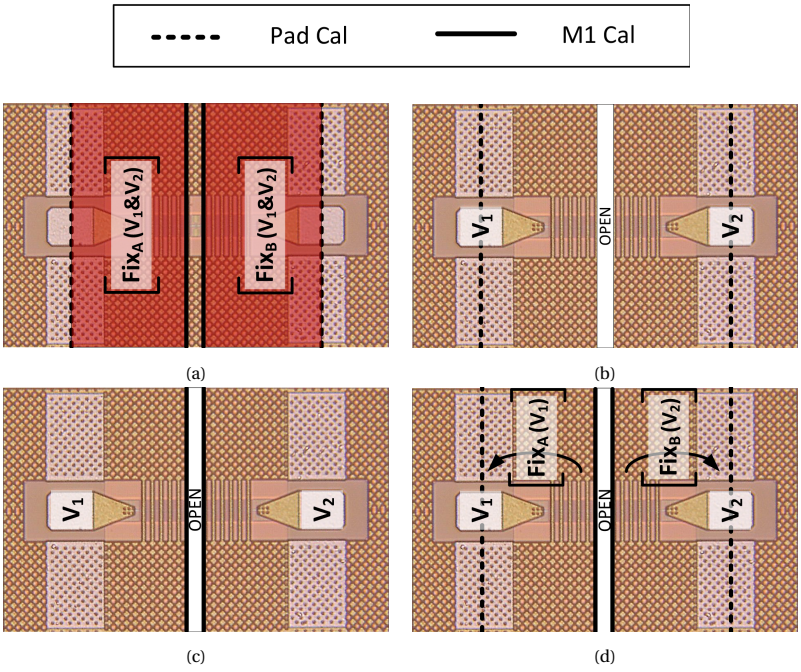


Figure 4.10.: Measurement verification steps. a) M1 Cal and Pad Cal are used to calculate the fixtures at two different bias voltages. b) Pad Cal is used to get the reference. c) M1 Cal is used to obtain the measurements of an open at different bias voltages directly to M1; d) The fixtures are de-embedded from the measurements at M1.

- Waveguide flange power calibration, (employing instrument power meter, i.e., Vdi calorimeter).
- Generating a look-up table to allow high-speed power level control.
- Performing the on-wafer second-tier calibration.

The mechanical movements on the VNA extenders to complete step A (fig. 4.12) (i.e., zero length thru connection) and then to allow for step B (i.e., insertion of the waveguide connectorized power meter head) can extend to more than 10 cm. To qualitatively indicate the impact on the output phase of the module, the phase error due to cable flexion at ~20 GHz from [56] can be used where they consider just 5 mm movement. Considering, as an example, the WR5 frequency band and accounting for the frequency multiplication introduced by the extender modules (x12), the overall phase error can be computed to be as high as 1.71 degrees, thus hampering the final calibration accuracy. The usage of a calibration transfer device, which can be directly connected at the probe tips, providing absolute power information, would reduce the entire procedure to only step C of fig. 4.12. This would allow to easily and quickly carry out both vector and power calibration, directly at the probe tips, given that the calibration transfer devices provide sufficient stability and consistency to the characterized one.

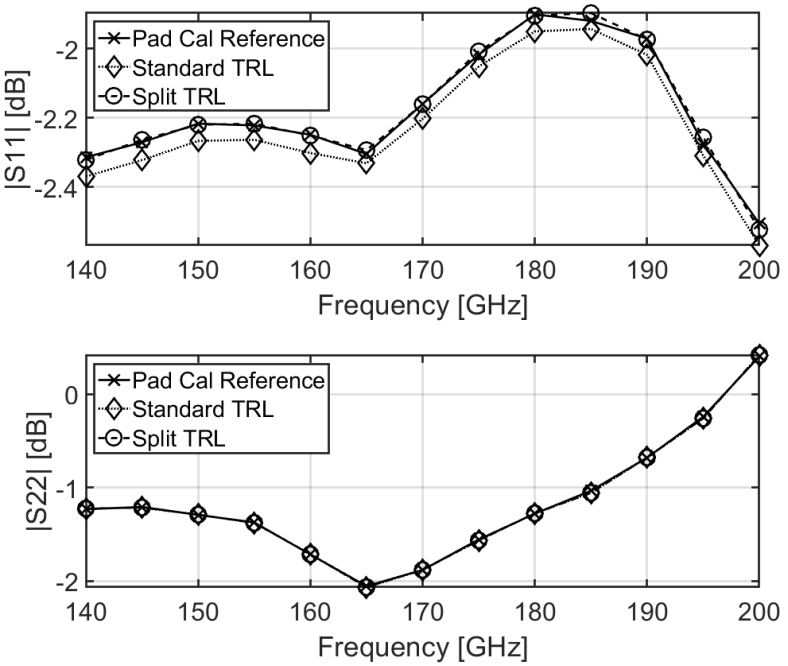


Figure 4.11.: Reflection parameters at the pads obtained using the TRL split and the standard 0-bias calibration compared with the reference measurement at the pads.

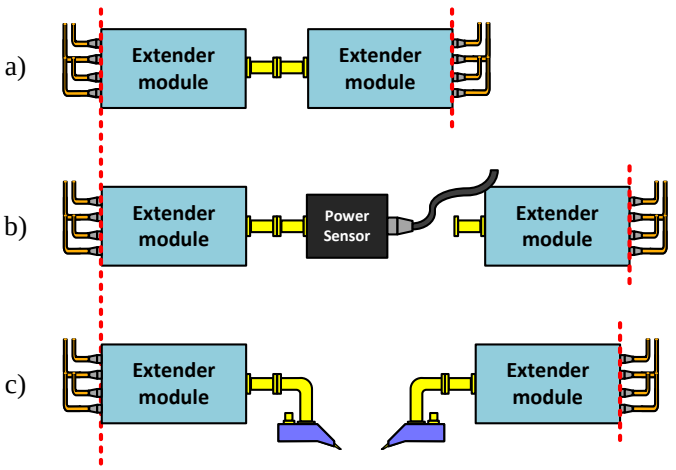


Figure 4.12.: Calibration steps that cause more movements: a) standard two-port calibration (TRL), b) power calibration, c) on-wafer two-port calibration.

4.3.2. POWER CALIBRATION TRANSFER DEVICE

The maturity of both CMOS and Bipolar CMOS (BiCMOS) state-of-the-art mm-wave technology nodes allows leveraging on large volume production capabilities and their electrical model-ready availability to provide an economical expendable on-wafer calibration transfer device. However, the proposed devices are disposable devices that can only be used a limited number of times, due to the pads wearing out, as the SOLT/TRL calibration structures. For this reason, it is important to analyze the possible performance (i.e., response) variation within the various fabricated devices, with respect to the reference (i.e., characterized) one. Device process variations are usually categorized into global and local variations [57], where the global variations relate to device parameters, such as oxide thickness or dopant concentrations, that change equally for all transistors between wafer-to-wafer and/or lot-to-lot. These variations can be captured by parametric model corners and their impact can be reduced by monitoring a few device parameters to extract which sub-model (i.e., fast/slow corner) to apply. In contrast, local variations, often called mismatch or random variations, can affect each transistor within the same lot separately. These local variations tend to increase with the CMOS technology scaling, and can only be mitigated in a given process line by optimizing the device layout following the simple formulas of eq. (4.8)

$$\sigma_{\Delta Vt} = \frac{A_{\Delta Vt}}{\sqrt{WL}} \quad \text{and} \quad \sigma_{\Delta k/k} = \frac{A_{\Delta k/k}}{\sqrt{WL}} \tag{4.8}$$

Where $\sigma_{\Delta Vt}$ and $\sigma_{\Delta k/k}$ represent the standard deviation of threshold voltage and the current factor, respectively. While $A_{\Delta Vt}$ and $A_{\Delta k/k}$ represent matching parameters characterizing the specific manufacturing line. The device used in this work is a 28 nm NMOS device with a minimum gate length and six fingers with a 720 nm width. This relatively small feature size and the absence of special layout techniques to mitigate local variation effects provide a close to the worst-case scenario in terms of stability of the device response across samples. The simplified schematic of the power calibration transfer device is given in fig. 4.13. The pCTD consists of a square-law detector capable of directly down-converting the mm-wave input signal into a linearly proportional DC output voltage. In this contribution, the detector is implemented using a common-source nMOS device with an off-chip 1 kΩ load resistor (R_{load}) connected at the drain side. Square-law operation is obtained by biasing the NMOS at the edge of the subthreshold region where the device has the highest current while still exhibiting strong non-linear (i.e., quadratic) behavior, required for the frequency translation. The resulting DC output voltage is generated by the even terms of the device's Taylor expansion of the transfer characteristic around the chosen bias point. The squaring terms generate a linearly proportional DC-term for any sinusoidal signal swing at the pCTD input [58]. The relation between the input power and the output voltage, referred to as the responsivity, is obtained using the following relation:

$$R_A = \frac{V_{out}^{OFF} - V_{out}^{ON}}{P_{in} R_{load}} \tag{4.9}$$

where R_{load} is the resistive value of the load resistor, V_{out}^{ON} and V_{out}^{OFF} are the voltages at the output of the detector when the input power is respectively ON and OFF. Finally,

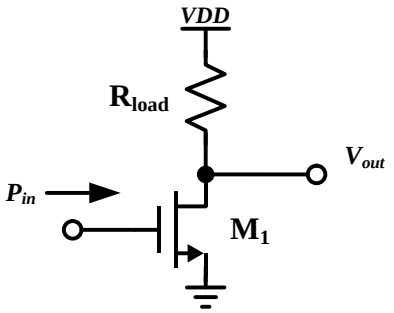


Figure 4.13.: Calibration transfer device, realized as a nMOS square law detector, with the resistive load condition to maximize the component responsivity.

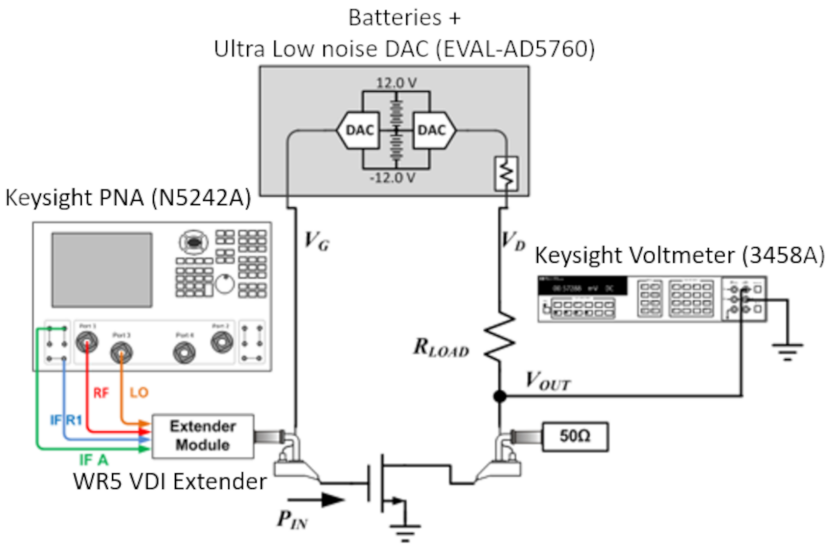


Figure 4.14.: Measurement setup.

P_{in} is the power entering the detector. The device responsivity is often assumed to be constant (for a given bias level) versus power but, as can be seen from fig. 4.15 this approximation is too coarse. In order to achieve an accurate power calibration, the P_{in} to Responsivity characteristic must be extracted, at every frequency of interest, for the entire power range covering the expected extender module calibration power (i.e., dependent on the frequency band and the extender module capabilities). For this reason, after identifying the optimal bias level to achieve the highest responsivity ($V_{drain} = 0.9V$ and $V_{gate} = 0.35V$), a complete characterization of the pCTD was carried out over power and frequency using the setup shown in fig. 4.14. The setup is calibrated using the VDI PM5 dry calorimeter and the vector power calibration procedure is performed as described in [9]. Note, that for the pCTD only a one port setup is required, allowing to reduce the

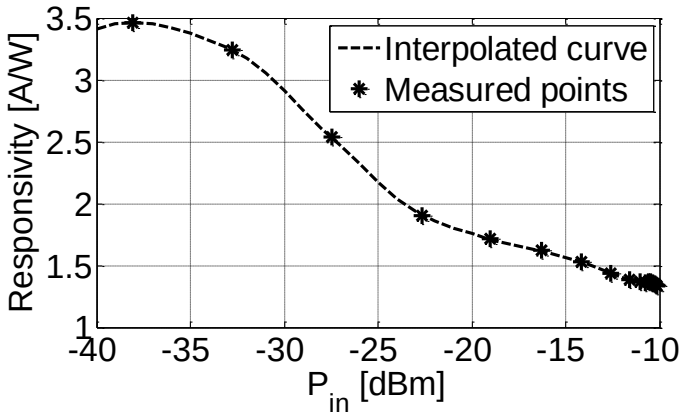


Figure 4.15.: Measured device responsivity versus power at 180 GHz.

waveguide TRL calibration to a simpler Short-offset Short-Load (SSL), thus requiring no extender movements. The difference in the square-law detector output voltage is then measured while sequentially applying and removing the input mm-wave signal. This last step is applied to reduce the effect of global variation (i.e., threshold voltage fluctuations, without the need of using parametric look-up table characterization). Figure 4.16 shows the variation of ΔV (V_{out}^{ON} - V_{out}^{OFF}) with the input power of the pCTD and the frequency at the optimal chosen bias point. This look-up table allows to map the output DC voltage to the input power to the detector, thus effectively transforming the square law detector into a calibration transfer device, i.e., from the PM5 to the VNA receivers. Finally, to present the first indications that the current state-of-the-art commercial technologies provide sufficient high frequency performance to be employed as multi-band mm-wave pCTD, the responsivity, see fig. 4.17, at the optimal bias level, was extracted for the WR10, WR5 and WR3 bands, thus covering the frequency range from 75 GHz to 325 GHz.

4.3.3. DEVICE-TO-DEVICE VARIATIONS

As mentioned in section 2.3, when "consumable" devices are used in the calibration process the stability of their response in comparison to the reference one (i.e., characterized/modeled) is to be considered an intrinsic uncertainty of the approach, and for this reason, needs to be quantified. In this work, we present a first-level analysis of these variations, by measuring the input power computed using different device samples (i.e., three nMOS from different dies). The ΔV response characteristic (see fig. 4.16) is computed on one single device (i.e., reference sample), and the simple model, which does not incorporate any parametric variation, is used to compute the input power from three pCTD samples. The error, see fig. 4.18, among the samples and versus frequency is established by comparing the power extracted from the different measurements to the one computed from the PM5 calibration (i.e., assumed as the reference value). While this analysis does not have any statistical significance, it provides some first-level indi-

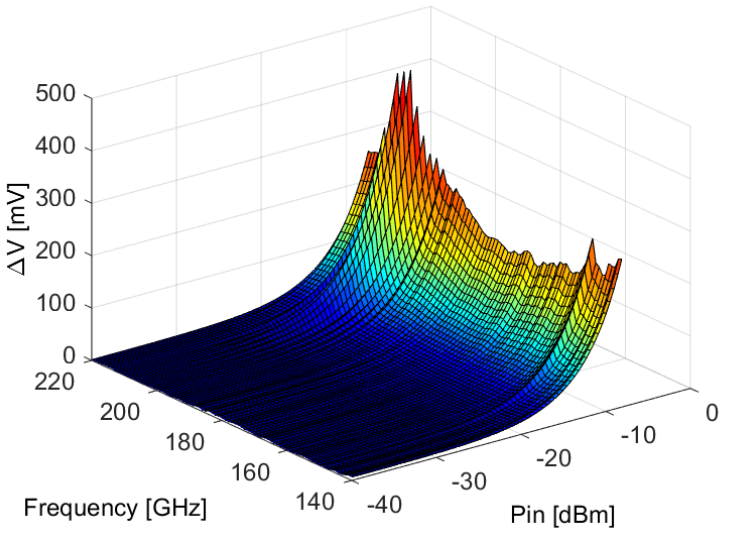


Figure 4.16.: Characterization of the pCTD versus input power over the entire WR5 frequency band.

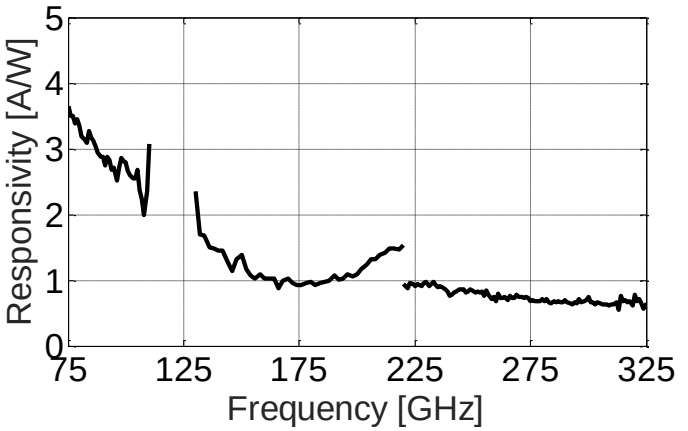


Figure 4.17.: Responsivity versus frequency for the 28 nm common source NMOS device, at the optimal bias point.

cation of the stability of the process, giving the indication that when employing parametric models and optimized device layouts an error below 0.25 dB (i.e., comparable to the accuracy of mm-wave power meters) can be targeted.

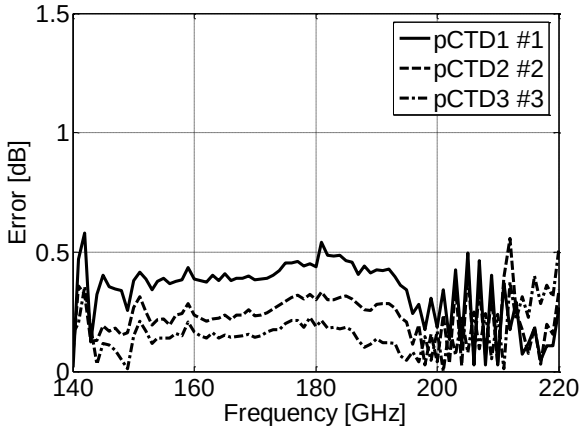


Figure 4.18.: Error between the measurements computed with the PM5 and those computed with different pCTD samples

4.3.4. EXPERIMENTAL RESULTS

To quantify the final error on the power calibration, the variation of the Pin computed by the different pCTD samples needs to be propagated through the power calibration equations [6]. In this comparison the raw data of one single power leveled measurement (at different power levels from −55 dBm to −15 dBm with 10 dB step) are corrected using the error terms derived by the power calibration obtained from the different pCTD samples and the PM5 (reference trace), see fig. 4.19. In the insert of fig. 4.19 it can be seen that the final error of the power calibration using the pCTD over three samples is confined to be less than 1 dB over the entire band, indicating this approach as a viable direction for the realization of power controlled mm-wave VNA-based setups.

4.4. CONCLUSIONS

This chapter presented improvements in performing on-wafer small and large signal calibration when employing the M1 test fixture presented in the previous chapter. The first part presents a strategy to remove the error that the ESD protection diode can cause during device characterization. This error is due to the dependency of the ESD protection diode parameters on the different bias voltages applied to the fixtures when a direct M1 calibration is used. The strategy consists of combining the error-terms boxes calculated performing a TRL algorithm at different voltages in one set of the error-terms. After a mathematical demonstration, the technique is validated with a circuit-level simulation that shows no errors, followed by a 3D EM simulation that shows an error comparable with the one achievable using the TRL calibration in the mm-wave frequency range. Finally, measurements on a passive structure (i.e. Open) are presented to experimentally validate the proposed method. The split TRL technique enables to employ direct calibration/de-embedding techniques also in the characterization of extremely low par-

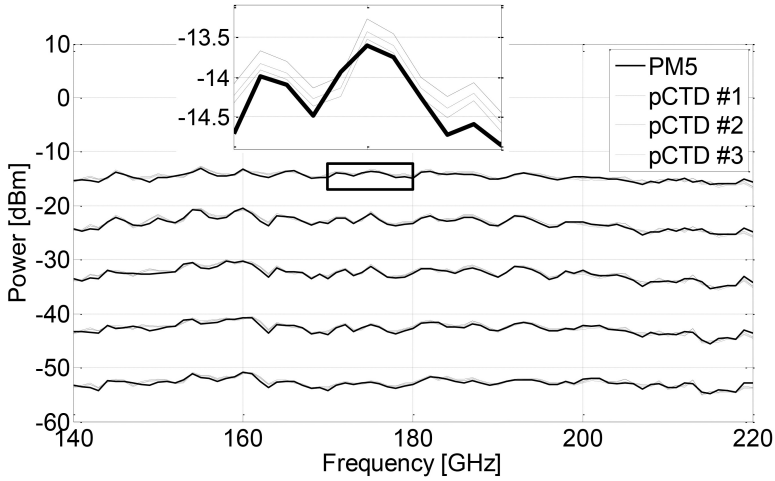


Figure 4.19.: Comparison between the measurement performed with the standard calibration and the measurements performed using four different pCTD.

asitic devices, as state-of-the-art CMOS and future nano-devices. The second part presented a calibration procedure capable of achieving direct on-wafer power calibration in mm-wave bands (i.e., up to 325 GHz). The approach is based on the usage of high-performance Mosfets, which provide sufficient responsivity up to 325 GHz. The technique with the proposed pCTD was benchmarked with approaches employing power meter. The results presented for the WR5 frequency band highlight the possibility of performing a direct on-wafer power calibration achieving a maximum error, after propagation through the calibration equations of 1 dB.

5

Hardware and Software solutions for Frequency Scalable (sub)mm-wave Active Load-Pull

This chapter presents a comprehensive analysis of the hardware and software solutions required for frequency scalable active load-pull test benches operating in the (sub)mm-wave frequency bands. First, the constraints arising from the harmonic (non-linear) operation of mm-wave extender modules are discussed and analysed. Next, hardware solutions for signal generation and control, together with their specific software algorithms to realize a frequency scalable load-pull, are presented. The key performances of the measurement setup are analysed for different frequency bands up to 500 GHz, *i.e., waveguide bands from WR10 up to WR2.2. Finally, load-pull measurements on a HBT device at* 75 GHz, *and a two stage differential PA at* 135 GHz *are presented to show the capability of the proposed test-bench to characterize and optimize mm-wave components for their non-linear behaviour.*

Parts of this chapter have been published in Hardware and Software Solutions for Active Frequency Scalable (Sub)mm-Wave Load–Pull (2020) [59].

5.1. INTRODUCTION

Load-pull has been the corner-stone measurement technique for the characterization and design of devices operating in non-linear regime for many years. Over time, increased functionalities to the load-pull test benches have been introduced: from active tuning [60] to high power capabilities [61], from harmonic impedance control [62], [63], [64] to the usage of realistic modulated signals (i.e., CDMA IS-95) [65] and the capability to achieve ultra-wideband and high-speed characterization [66]. When approaching mm-wave frequencies, both the test benches [56], [67] as well as the role of load-pull need to be redefined to accommodate the constraints of the bands. First of all, from the hardware perspective, the frequency ranges of system level interconnections (typically rectangular waveguides above 65 GHz) and wafer probe components are limited to less than one octave. This bandwidth strongly limits, if not completely removes, the capability of achieving harmonic control in mm-wave test benches. Moreover, the scarce commercial availability of medium/high power amplifiers and pre-matching tuners (especially above 110 GHz) implies that extreme $|\Gamma_L|$ cannot be reached for medium/high power transistor cells. To illustrate this, in fig. 5.1, the formula of [68] is used to plot the power required to emulate a given $|\Gamma_L|$. It is shown that, for devices capable of providing more than -10 dBm), the conventional frequency extenders are not able to reach $|\Gamma_L|$ unitary. This boundary results considering ~10 dBm max output power limitation from the extender (i.e.,the nominal value in datasheet for modules operating in the WR5/WR3 bands). To avoid the high costs and development times connected to full-custom hardware implementations of mm-wave load-pull setups [56], [67], test benches to complement existing mm-wave instrumentation are required. When doing so, it is important to mention that the source and load injection paths will have to employ multiplication stages to reach the DUT operation frequency. This yields a non-linear transfer function between the control plane and the DUT one, requiring changes in the calibration and measurement algorithms. From a designer perspective, the shift in frequency to mm-wave allows limited use of the classical information gathered by load-pull test benches. For example, at frequencies up to X-band, designers are used to employ load pull contours to synthesize the passive network on a laminate technology to realize high power amplifiers incorporating packaged active devices [69]. When shifting to mm-wave frequencies, matching networks are integrated on the same Integrated Circuit (IC) of the active device due to the reduced wavelength. Moreover, passive structures, interconnections and even device contacts and vias need to be accounted for and optimized for a specific design. This implementation path forces the design process to rely more and more on electromagnetic solvers for the optimization of the layout, thus limiting the usage of a generic transistor load-pull contours. The abovementioned considerations shift the focus of mm-wave load-pull to device model validation (i.e., fundamental load while the passive harmonic impedance are fixed and known), as well as the tuning/optimization of complete circuits (i.e., Power Amplifier (PA)). For the latter, even when only limited injection power is available, sufficient $|\Gamma|$ mismatch can be achieved to tune and successfully re-design complete PAs. To better support mm-wave characterization for modelling and circuit tuning, load-pull test benches can be co-integrated with VNA based large-signal platforms [8]. In this contribution we introduce a frequency scal-

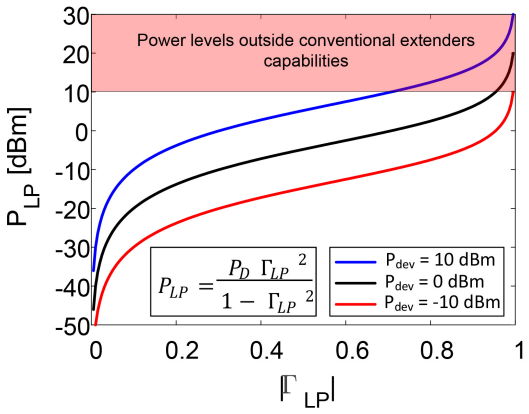


Figure 5.1.: Power required from the output source to emulate a defined $|\Gamma_L|$, for different device output power (i.e., related to the power cell size, and indicating what is a power range achievable by commercial extender modules (i.e., indicative number for WR5/WR10 waveguide bands).

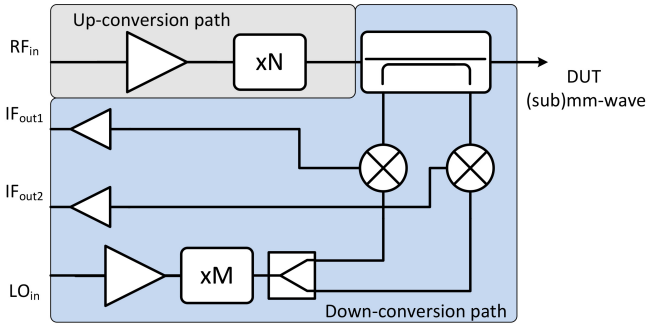


Figure 5.2.: Simplified block scheme of mm-wave extenders.

able active load-pull solution realized as an add-on module to the commercially available hardware of mm-wave VNAs. After reviewing the available hardware solutions to realize the active loads, the calibration and algorithms to account for the non-linear behavior of mm-wave extender modules are introduced. Finally, the experimental results of the proposed test bench for different mm-wave non-linear devices are presented.

5.2. HARDWARE SOLUTION FOR LOAD CONTROL

VNAs operating at frequencies above 67 GHz make use of mm-wave extenders, a hardware element composed (see fig. 5.2) of a:

- Up-conversion path, providing the high frequency signal to the DUT by using a xN multiplier (set by the output frequency of the extender) that requires a lower frequency input, typically provided directly by the VNA.

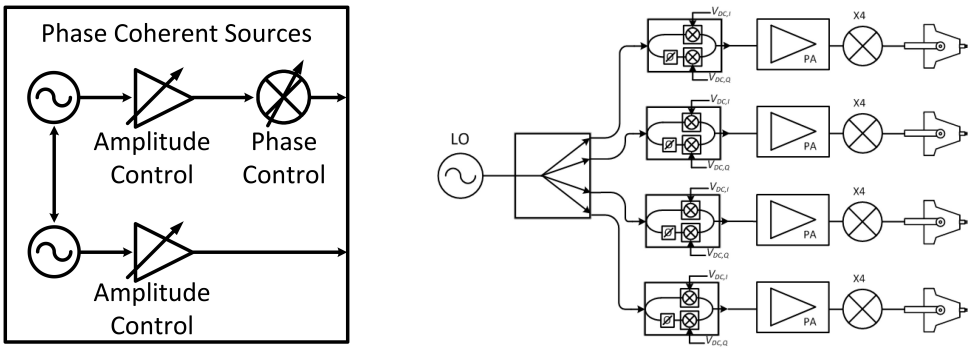
- Down-conversion path, composed of a bi-directional coupler to sample the incident and scattered wave and a set of down-converting mixers (sub-harmonic or harmonically fed) to provide the IF signals for the analog to digital converter of the VNA.

Considering the mm-wave extenders architectures, and to maximize the frequency scalability of the load-pull test bench, the amplitude and phase control of the injected signal needs to be performed at the low-frequency input (RF_{in}, see fig. 5.2) of the mm-wave extender. This will effectively result in the amplitude and phase control of the frequency up-converted signal delivered to the DUT. However, it is important to note that the up-conversion process is realized by a strongly nonlinear relation which is frequency and power dependent, denoted in the rest of this chapter as $H(f, Pin)$. To achieve an accurate control of the injected wave at the DUT frequencies, and thus of the load reflection coefficient, a very precise and stable amplitude and phase control of the signal in input to the mm-wave extenders needs to be realized. To analyze the possible configurations, we compare two hardware implementations, namely:

- Employing phase-coherent sources, as shown in fig. 5.3a [72], [70], [73].

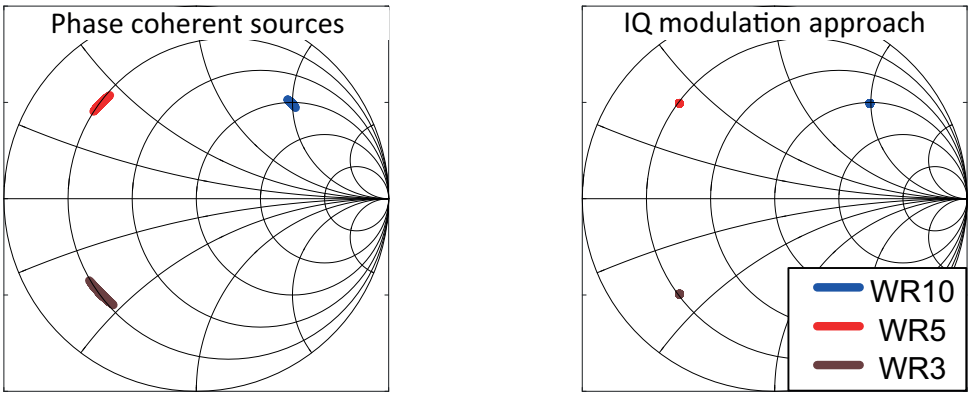
- Employing power splitting of a single synthesizer output and IQ vector modulation to realize the relative amplitude and phase control, as shown in fig. 5.3b [71].

To compare the performances of the two solutions, when attempting to generate amplitude and phase-controlled waves after frequency up-conversion (i.e., using multiplier chains), the stability of the injected signal presented in [74] is considered. Note that the analysis of [74] was performed at 3 GHz, and is considered here as a reference number for the RF_{in} wave (see fig. 5.2) which varies in the frequency range $10-20$ GHz. The injected wave magnitude stability for both implementations is set to a 3σ value of 10^{-4} while the phase stability is set to a $3\sigma = 0.3^{\circ}$ and $3\sigma = 0.003^{\circ}$ for the implementation fig. 5.3a and fig. 5.3b, respectively. The magnitude dependency of $H(f, Pin)$ versus input frequency and power level is extracted from the experimental data presented in [9] for the WR10, WR5 and WR3 waveguide bands. A constant multiplication factor (N), set by the mm-wave extenders output frequency band, is considered for the phase response of $H(f, Pin)$. The noise expansion on the mm-wave injected signal, resulting from the non-linear nature of $H(f, Pin)$, is mapped on the load reflection coefficient in fig. 5.4. As can be seen in fig. 5.4a, the phase-coherent sources solution results in a large uncertainty in the phase control of the reflection coefficient, mostly when considering the higher frequency waveguide bands (i.e., WR3), i.e., $3\sigma \sim 5.4^{\circ}$ (i.e., approximated to the first decimal and directly computed from the iteration data generated in the higher frequency band). The high stability of the IQ modulation approach results in a more accurate phase control of the reflection coefficient when compared with the multiple source solution (figs. 5.4a and 5.4b) over the various considered waveguide bands, with a worst-case $3\sigma = 0.05^{\circ}$ degrees for the WR3 band.



(a) (b)

Figure 5.3.: a) Phase coherent sources architecture in VNA adapted from [70]; b) generation of multiple phase coherent mm-wave signals setup, adapted from [71]



(a) (b)

Figure 5.4.: Comparison between the Γ_L stability offered by a multiple source solution [70] and single source with IQ modulation [71].

5.3. FREQUENCY SCALABLE LOAD-PULL ARCHITECTURE

In order to realize a frequency scalable load-pull architecture capable of providing high performance in terms of Γ_L stability and control, the single source solution with IQ vector modulation for the injected waves was chosen. The proposed system architecture is shown in fig. 5.5. The system is based on high-performance VNAs and standard mm-wave extender modules to provide large dynamic range acquisition of the input and output waves (incident and scattered). A high precision (i.e. resolution of 83 nV) and low noise (i.e. voltage noise of 6.3 nV) digital-to-analog converter provides the DC signals to a broadband RF IQ modulation unit driven by a single synthesizer source. The increasing multiplication order (N, see fig. 5.2) of commercially available mm-wave extender modules for the higher waveguide bands allows the usage of a unique broadband (pas-

sive, diode-based) IQ modulation unit (operating in the 10 – 20 GHz frequency range), realizing a true system scalability. realizing a truly scalable system.

5.4. EXTENDER NON-LINEAR RESPONSE CALIBRATION

In [8] and [74], it was shown that, by stepping the internal source of the VNA, the non-linear amplitude response of the mm-wave extenders could be employed to provide accurate power control and realize software-controlled power sweeps at the mm-wave ports. When considering the system architecture described in fig. 5.5, the single source configuration requires the power control at the input of the mm-wave extenders to be provided by the IQ modulators. The transfer function that links the voltage provided at the IQ ports to the mm-wave power available to the DUT will depend on the specific extender and modulator model. Nevertheless, as shown in fig. 5.6, accurate power control of more than 70 dB can be achieved for the various waveguide bands and mm-wave extender manufacturers by employing high-resolution digital-to-analog converters. To accurately predict the IQ modulator voltage settings to realize a user-defined reflection coefficient at the calibration reference planes, also the non-linear phase response of $H(f, Pin)$ needs to be known. Additional information needs to be extracted during the calibration process on the thru standard to acquire this phase response. This is achieved in two steps: first, the link between the IQ modulator settings and the raw waves is obtained using eq. (5.1).

$$\angle\frac{a_2^{RAW}}{a_1^{RAW}} = \left(\angle IQ_{p1} + \Delta_{ph} + \angle IQ_{p2}\right) * N \tag{5.1}$$

Where $\angle IQ_{p1}$ and $\angle IQ_{p2}$ are the phase shift settings of the IQ modulators at port 1 and port 2, respectively. While Δ_{ph} is the phase delay introduced by the connections/HW setup and N is the frequency multiplication factor (shown in fig. 5.2). Then, using the expression of eq. (5.2), during the thru connection measurement, the phase relation between the incident wave at port 1 (a_1) and port 2 (a_2) can be computed at the calibration reference planes through the error terms.

$$\Gamma_{IN} = \frac{b_1}{a_1} = \frac{a_2}{a_1}\bigg|_{DUT=thru} \tag{5.2}$$

With this extra step, the IQ settings, required to generate at every frequency a given (complex) a_2^{inject}, can be accurately predicted.

5.5. ALGORITHM FOR MM-WAVE LOAD-PULL

The architecture in fig. 5.5 shows a open loop active load-pull implementation based on a digitally controlled IQ modulator. The open loop configuration requires an iterative convergence algorithm to account for the non-linear behavior of the DUT at every change of power level and/or load condition. In this contribution, a Newton–Raphson method is employed to reach the desired reflection coefficient (Γ_L^{obj}). Differently from

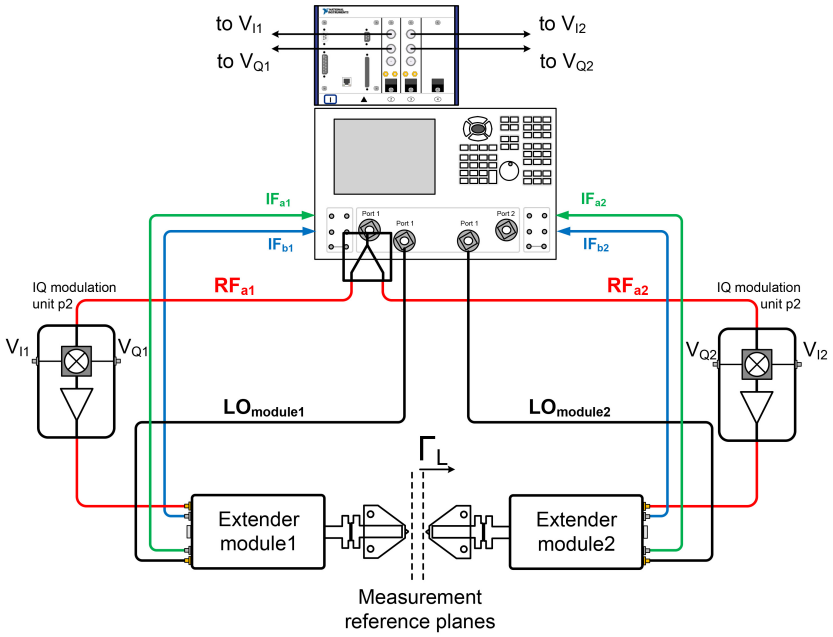


Figure 5.5.: Proposed frequency scalable (sub)mm-wave load-pull architecture, employing IQ modulation.

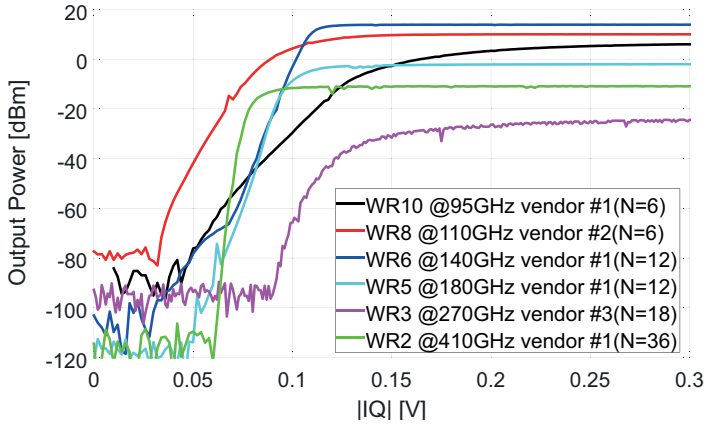


Figure 5.6.: Mm-wave output power available from the extender versus the absolute value of the IQ voltage (extracted at a specific frequency points from the related waveguide full band characterization), measured after the leveling procedure introduced in [8] for different waveguide bands and extenders manufacturer.

[66] and [56], the control of the injected wave to synthesize Γ_L^{obj} is realized at a frequency (N times) lower than that of the DUT. The frequency (up)scaling of the wave to the DUT frequency range is achieved via the non-linear (harmonic) signal multiplication of the

mm-wave extenders $H(f, Pin)$, adding a new level of complexity to the convergence algorithm. Figure 5.7a shows the measured relation between the (user set) loading condition and the I-Q voltage search plane for a non-frequency multiplied active tuner (i.e., 10 GHz with $N = 1$), as is the case in [64] and [65], performed on a thru connection. In this case, the transfer function $\Gamma_L^{obj}(I,Q)$ has non-zero derivates in the entire I-Q search plane, thus creating the base for a robust and fast Newton-Raphson search. For a frequency-multiplied active tuner (i.e., 180 GHz with $N = 12$), the same kind of characteristic becomes much more complex (see, fig. 5.7b), with a number of local-minima equal to the multiplication factor N and large flat regions. At this stage, it is important to recall that the Newton-Raphson algorithm calculates the tangent line of the function and its intercept with the x-axes, representing a first approximation of the solution. The procedure is then iterated (eq. (5.3)) until the error ($\left|\Gamma_L - \Gamma_L^{obj}\right|$) reaches a value below a user defined level, i.e., convergence criterion.

$$X_{n+1} = X_n + \frac{f(X_n)}{f'(X_n)} \tag{5.3}$$

5

Being Newton-Raphson a derivate-based convergence algorithm, it can reach a high convergence speed, but it is also strongly limited by flat regions in the function domain, where the solution would be undefined, as it is the case of the characteristic shown in fig. 5.7b. When plotting the 2D cross-section of fig. 5.7b for a fixed Q value (fig. 5.8) one can even better observe the severe challenges posed to the derivate-based convergence algorithm in mm-wave frequency scalable test benches. The usable function domain (i.e., parts with no flat regions), which is strictly correlated to the transfer function of the extender (fig. 5.6), is limited to a small range of Q (or I), close to 107 mV in the case considered (fig. 5.8). Based on the above, only employing high precision digital to analog converters together with knowledge of the complex $H(f, Pin)$ as discussed in the previous section allows achieving a fine resolution of the controlled reflection coefficient and an accurate first prediction of the IQ values. The latter is needed to be within the usable part of the mm-wave extender non-linear transfer characteristic. To quantify the improvements when using the prediction enabled by the knowledge of the complex $H(f, Pin)$, we compare the number of iterations required to converge to a set of Γ_L^{obj} (with convergence error $|err| < 0.02$) with and without this prediction. The algorithm is tested over 2065 points homogeneously distributed over the entire Smith chart to provide a statistical meaningful comparison between the two procedures. The test uses the Γ_L versus I-Q response, shown in fig. 5.7b, measured on a WR5 extender module. The complex $H(f, Pin)$ is computed following the calibration procedure described in Section IV. The no prediction case employs, as a start value, I and Q equal to zero. fig. 5.9 summarizes the results of the comparison describing on the x-axis the number of iterations to reach a required reflection coefficient and on the y-axis the number of occurrences (over the 2065) where those iterations took place. From fig. 5.9 it is possible to observe that using no prediction the average value (μ) in terms of number of iteration is 32.82 and the standard deviation (σ) is 28.84. Using the prediction, based on the complex $H(f, Pin)$ knowledge, μ is reduced to 2.45 and σ to 0.54. Moreover, all the points converged with a maximum of 4 iterations. Another advantage associated to the usage of an accurate first guess prediction is the reduction of the vector distance between Γ_L^{obj}

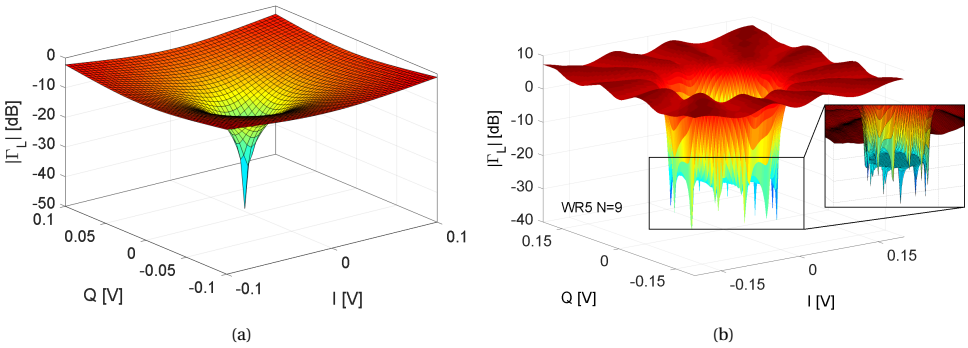


Figure 5.7.: Magnitude of $|\Gamma_L|$ versus IQ bias settings for: a) injected wave control at the fundamental (DUT) frequency as in [66] and [56] (setting $P_{port1} = -30$ dBm); b) injected wave control at the sub-harmonic frequency (N times lower than DUT frequency) as implemented by the architecture of fig. 5.5 (setting $P_{port1} = -40$ dBm).

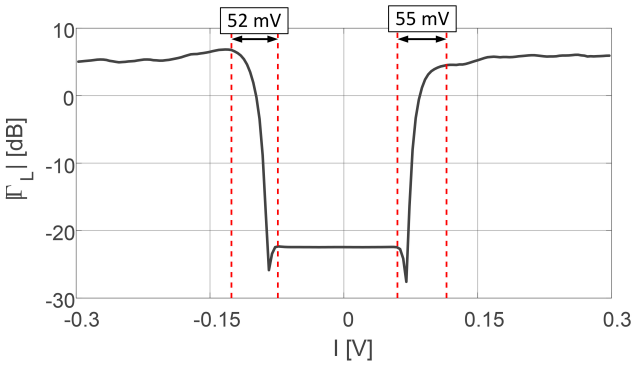


Figure 5.8.: Cross section of fig. 5.7b for a fixed Q value.

and the actual guess (Γ_L) during the convergence. This reduction of the distance of an applied Γ_L from the targeted one, during the iteration process, allows avoiding load conditions that could trigger DUT's instabilities/oscillations. Figure 5.10 shows how the load trajectory and distance to the wanted reflection coefficient can be minimized when the injected wave prediction (based on the $H(f, Pin)$) is used (fig. 5.10a), compared to the case when the initial guess is set to I and Q values equal to zero (fig. 5.10b).

5.6. SYSTEM PERFORMANCE

To validate the frequency scalability of the architecture presented in fig. 5.5, the short term stability of the reflection coefficient was evaluated across the different waveguide bands. Four Γ_Ls have been selected in the four quadrants of the Smith chart with a magnitude of approx. 0.8 (varying from 0.75 to 0.85 for different bands) to be acquired for 100

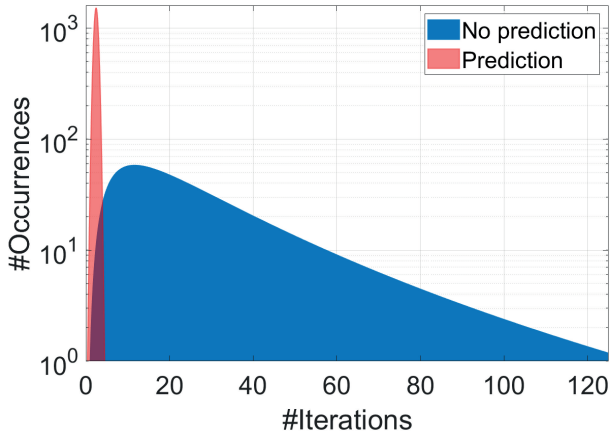


Figure 5.9.: Number of convergence occurrence for a set of 2065 homogeneously distributed Γ_L conditions, versus the number of iterations required to reach convergence, achieved using initial prediction (Red), as well as without prediction (Blue) applied to the Newton-Raphson based algorithm.

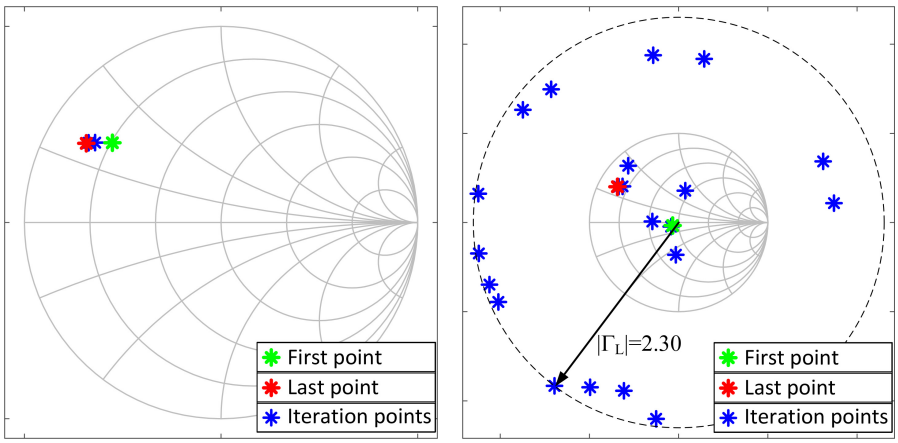


Figure 5.10.: Γ_L (intermediate) values during the convergence using: a) the algorithm with prediction and b) without the prediction.

consecutive times during a period of approximately 100 sec. In an iterative open loop architecture, the short term stability defines the accuracy with which the algorithm can effectively converge in a reasonable timeframe, long term stability is not crucial since these fluctuations are compensated by the iteration process. In fig. 5.11a the various measurements for the different waveguide bands are plotted normalized to the user set value. The 3σ circles indicate the convergence accuracy that can be expected for a given waveguide band. As anticipated, from the analysis of section 5.2, the decrease of short term accuracy is primarily dependent to the multiplication factor of the mm-wave ex-

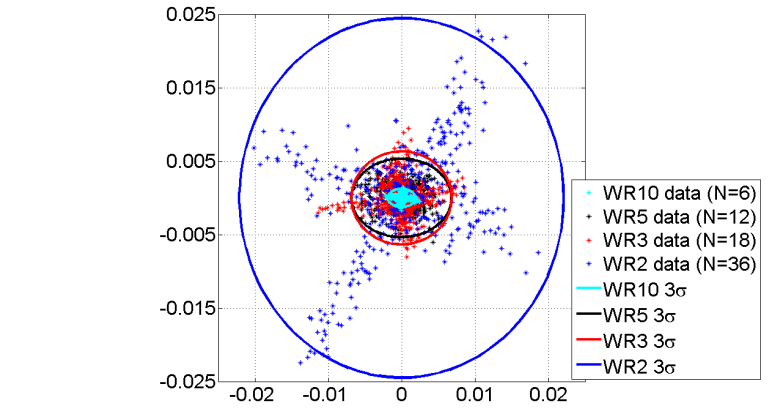
tenders (with higher frequency extenders showing larger spread) and secondly to their specific non-linear characteristic. The results in fig. 5.11a demonstrate that the proposed hardware setup is able to set as a convergence criteria for the iteration process an $|err| < 0.01$ for bands up to WR3 and $|err| < 0.025$ for the WR2.2 band. In fig. 5.11c the operating gain measurement on a thru at 180 GHz is presented. It is measured on the Γ_L points depict in fig. 5.11b at different power values (i.e., -40 to −5 dBm) to show the calibration accuracy [75] of the measurement setup. The operating gain remains within ±0.4 dB for a $|\Gamma_L|$ within 0.9. Note that the calibration accuracy is presented just for the sake of completeness since it is not the core of this work. In fact, the calibration path of the measurement setup is equal to a commercial mm-wave VNA where the calibration procedures and their accuracy are well defined.

5.7. EXPERIMENTAL RESULTS

The frequency scalable system architecture (see fig. 5.5) was employed in the WR10 and WR6 frequency band to validate the proposed usage of mm-wave fundamental load-pull, i.e., non-linear device data collection for model optimization, and complete PA tuning for optimization. The large signal performance of IHP microelectronics SG13G2 130 nm HBTs is tested at 75 GHz (i.e., WR10), see fig. 5.12. The large signal compression and PAE response of the device incorporate valuable information to validate and tune the the active device model and its parameters in the mm-wave range for high performance applications. The single propagation mode nature of the mm-wave extenders and the waveguide probe employed in the testing do not allow for harmonic load pull. Nevertheless, the harmonic impedance (static) provided by the probe can be measured and reported to better correlate active device models to their measurement data. Figure 5.13a shows the optimization of a two-stage amplifier [76] at 135 GHz for its $P1_{dB}$ obtained by tuning the output loading condition. The optimization allows a close to 2 dB improvement for $P1_{dB}$. The results of these experimental optimization can be used by the designer to develop a modified layout scheme or output pad configuration in a re-design of the circuit to maximize the achievable performance at a specific frequency of operation.

5.8. CONCLUSIONS

In this work, a frequency-scalable load-pull architecture based on commercially available mm-wave extender modules and high-performance VNAs capable of reaching frequencies up to 500 GHz is presented. The choice of the HW solution to realize the wave amplitude and phase control was benchmarked versus available solutions, demonstrating a superior control accuracy. The improved calibration to account for the non-linear complex response ($H(f, Pin)$) of the mm-wave extender modules was described, and the improvements during the iteration process in both convergence speed and distance to target where analyzes in details. The performance of the load-pull test bench in terms of short time fluctuation of the presented reflection coefficients were experimentally characterized, demonstrating that the proposed hardware is able to set as a convergence criterion an $|err| < 0.01$ for bands up to WR3 and $|err| < 0.025$ for the WR2.2 band. Fi-



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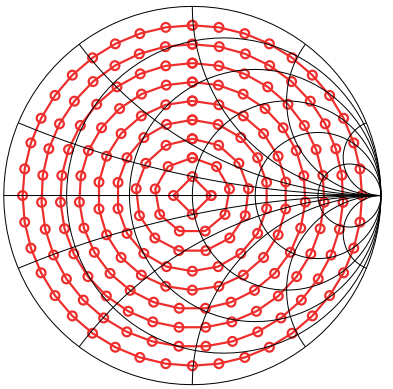

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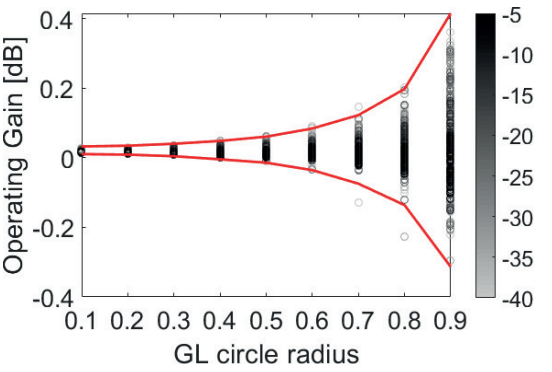
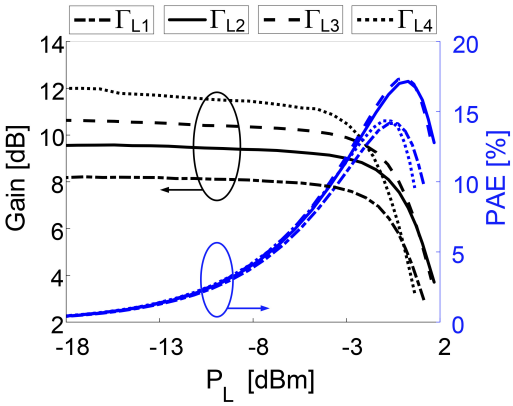


(c)

Figure 5.11.: a) Normalized distribution of 100 repeated measurements performed on 4 Γ_L points equally distributed on the smith chart for different mm-wave extenders (different xN). b) Γ_L points measured on the circles at different absolute values to get the gain test and generate fig. 5.11c. c) Operating gain versus the Γ_L absolute values for the points shown in fig. 5.11b. It is measured on a thru connection at 180 GHz at various power levels (i.e., from -40 dBm to -5 dBm, right intensity scale). The red lines represent the 3σ (i.e., 99 %) confidence bounds.

nally, experimental data from a high performance SiGe transistor and PA were presented to show the capability of this test bench to provide valuable data for model validation and IC optimization.



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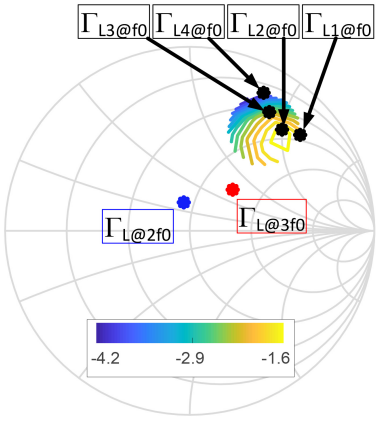
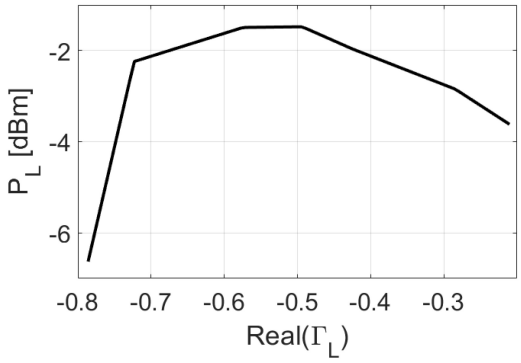


(b)

Figure 5.12.: Load-pull measurement results on IHP microelectronics SG13G2 130 nm HBTs at 75 GHz. a) Gain and Power Added Efficiency (PAE) sampled in 4 Γ_L points distributed from the lowest to the highest gain value point. b) Contour plot showing the P_L constant circle and the 2 harmonic passive impedances ($\Gamma_{L@2f0} = -0.032 + j0.155$; $\Gamma_{L@3f0} = 0.233 + j0.224$). Moreover the 4 Γ_L points position are highlighted ($\Gamma_{L@1f0} = 0.597 + j0.512$; $\Gamma_{L@2f0} = 0.495 + j0.550$; $\Gamma_{L@3f0} = 0.435 + j0.636$; $\Gamma_{L@4f0} = 0.409 + j0.744$).



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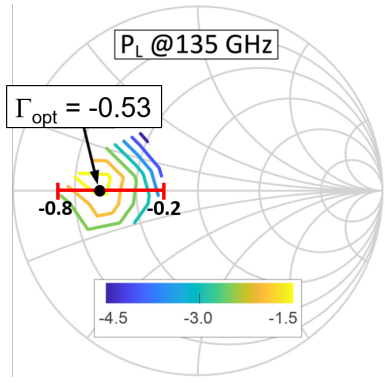


(b)

Figure 5.13.: Load-pull measurement results on PA reported in [76] at 135 GHz. a) Output power over the red (Γ_L) indicated trajectory (shown in fig. 5.13b) to show a P_L increment of around 2 dB concerning $\Gamma_L = 0$; b) Contour plot showing the constant P_L circles around the optimum point.

6

APPLICATION EXAMPLES

In this chapter, two examples detailing the usage of this dissertation's key technologies in other application fields are presented, such as:

- *Over the Air characterization*
- *MM-Wave signal analysis (EVM)*

Parts of this chapter have been published in "A near-field setup with independent amplitude and phase control of the stimuli for phased antenna testing" (2017) and "Vector gain based EVM estimation at mm-wave frequencies" (2020) [77, 78].

6.1. OVER-THE-AIR CHARACTERIZATION OF MM-WAVE ANTENNAS

Sub-THz applications, such as imaging [79], radar [80] and high-rate communication, [81] are starting to embed the antenna element in the RF integrated circuit to minimize the losses and complexity of the wafer to interpose transition [82]. From a characterization point of view, the use of on-chip antennas poses strong challenges in adapting existing microwave measurement techniques [83], which are typically based on coaxial cables, to the mm-wave and sub-THz frequency ranges, where waveguides and on-wafer transmission lines are commonly used. Although some antenna parameters (e.g., directivity, beam width, radiation pattern) can still be easily measured by exposing the Antenna Under Test (AUT) to a probe antenna [84, 85], which can be moved over a scanning area. Other parameters (e.g. gain, efficiency) are more challenging to measure. These latter parameters require precise knowledge of the absolute power levels at both the feeding and receiving ports. Accurate absolute power measurements in mm-wave, using a power meter, present challenges at arbitrary reference planes due to errors that are difficult to correct in a scalar-based setup. Furthermore, considering the limited availability of fast and high-dynamic range power sensors on the market, conventional scalar-based antenna measurement techniques are not only time-consuming but also constrained by a limited dynamic range. For this reason, recent years have seen efforts to develop vector-calibrated power measurement techniques [9]. Despite these advances, ongoing research aimed at enhancing integrated antenna performance has led to increasing complexity in antenna designs, consequently demanding more sophisticated measurement setups. In this chapter, an adapted version of the setup presented in chapter 5 is used to characterize a Combining Active-Fed On-Chip Antenna (CAFOA) presented in [86].

6.1.1. INTEGRATED POWER SOURCE COMBINED WITH A COMPACT DIELECTRIC RESONATOR ANTENNA

The device discussed in the first part of this chapter was designed by A. Visweswaran from IMEC and published in [86]. To help the reader better understand the CAFOA and provide some background, parts from [86] are included in this paragraph.

DESCRIPTION OF THE DEVICE UNDER TEST

The DUT considered is a high-power, high-efficiency D-band radiating unit integrated in 0.13 µm BiCMOS (f_T/f_{MAX} 250/370 GHz) that operates over 132-147 GHz and delivers 27 dBm of Effective Isotropic Radiated Power (EIRP) at 13.8% Power Added Efficiency (PAE). The prototype (fig. 6.1a) features 4-way spatial power combining via hybrid on-chip antennas, wherein each signal path comprises a 5-stage PA drive. The transformer-coupled PA is based on regenerative reactive feedback techniques for common-emitter and cascode amplifiers outlined in [87], aimed at maximizing gain at the expense of reducing the margins on unconditional stability.

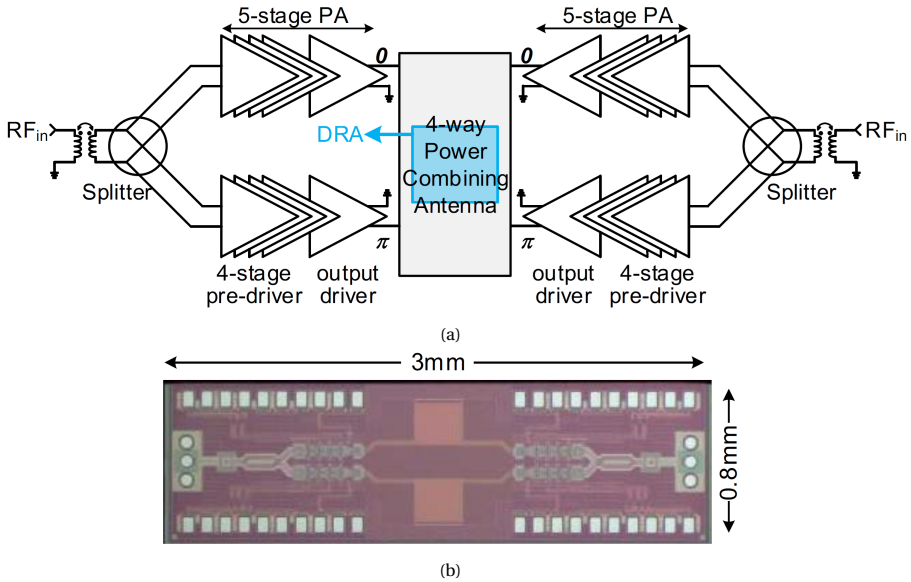


Figure 6.1.: a) Block diagram of the integrated 4-way spatial power-combining source; b) Chip micrograph

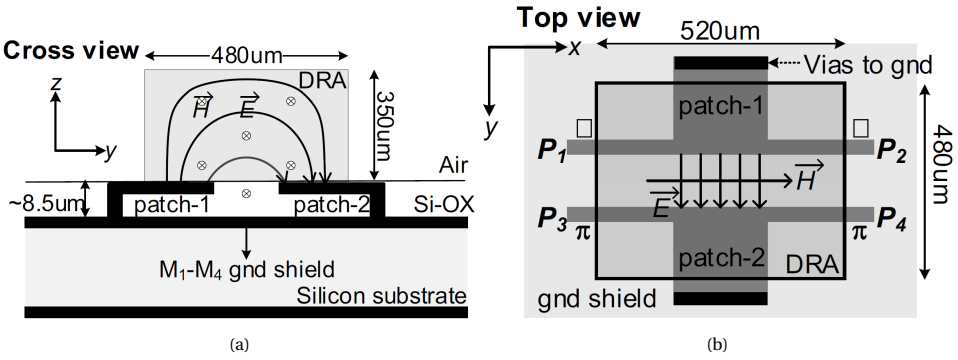


Figure 6.2.: Cross-section (a) and top view (b) of the hybrid antenna.

THE HYBRID ANTENNA

The hybrid antenna comprises shorted patches (Zin 50 Ω) onchip that proximity-couple to an external rectangular dielectric resonator antenna (DRA) glued on the chip surface (fig. 6.2a). In contrast to a parasitic off-chip patch [88], a DRA increases the efficiency to 80% ($\Delta f/f_c$ = 16%). The approach benefits from low losses in the compact DRA, while shielding the silicon substrate with M1-M4 eliminates substrate modes and undesired backside radiation. The resonant antenna (~ $\lambda_0/4$) should not be confused with large off-chip lenses used for beam collimation. The DRA, 3D-printed in Alumina, is 520x480x350 µm^3 in size ($r = 9.5, tanD = 0.01$). Efficient excitation of the TE_{11} mode in

the DRA is realized by mirroring the two patches w.r.t the x-axis and driving them with opposite phases (fig. 6.2b). Each shorted patch has two single-ended, 50 Ω feed lines. The antenna thus combines the power of four input lines when driven with the excitations shown in fig. 6.2b. The simulated 7 dBi gain, impedance match and radiation efficiency of the 4-port antenna are shown in fig. 6.3. The impedance match is the same at all four ports by virtue of symmetry. The pattern shows a 3 dB beamwidth of 70 and 32° in the E and H planes, respectively. Simulations include bondwires and probes, and their impact is minimized via optimized pad distribution.

POWER AMPLIFIER LARGE MEASUREMENT

Large-signal measurements of the PA are shown in fig. 6.4. The PA has a broad saturated b/w of 113-152 GHz, with a peak P_{sat} of 18 dBm observed at 136 GHz. As indicated in fig. 6.4a, the power is corrected for transmission loss of the output balun (for comparison with the integrated source) using a dedicated test structures. The PA response to input power levels at 140 GHz are shown in fig. 6.4b. Note: these also include corrections for output balun losses. The maximum P_{sat} of 17.8 dBm correspond with the results of fig. 6.4a. The peak gain is ~31 dB and a P_{sat} of 17.7 dBm is observed at 13.8% PAE.

6.1.2. MEASUREMENT SETUP

The measurement setup is based on the one presented in chapter 5. Specifically, this setup employs a four-ports Keysight VNA (Model N5227A) along with WR6.5 (110 GHz to 170 GHz) VDI frequency extender modules [7], which are mounted on a CNC machine to enable the probe antenna to move across the scanning area (fig. 6.5). The reader interested to learn more about planar near field antenna measurements is invited to read [89]. Since phase control is required to achieve the necessary relative phase relations between the two ports, the setup presented in chapter 5 can be employed with minor differences, as shown in fig. 6.6. To collect the energy radiated by the antenna, instead of using the power meter, a mixer (RX mixer in fig. 6.6) has been employed, which down-converts the signal received by the probe antenna and feeds it to an extra receiver of the VNA for its measurement. The reason for this choice, as already mentioned in the previous chapters, is that the power meter is based on a calorimeter sensor at these frequencies, which presents limitations in terms of dynamic range and measurement speed. Moreover, since the VNA used has only two sources, that are used for the RF and LO signals of the frequency extenders, a receiver RX mixer has been chosen with the same multiplication factor for its LO port, matching that of the frequency extenders (i.e., x12). This allows the use of a common LO signal across all down-conversion chains (fig. 6.6). The original setup in chapter 5 was designed to converge to a defined loading condition presented by port 2 to the DUT, with the software coded to identify the needed a_2 that achieves a prespecified a_2/b_2 ratio (i.e., Γ_L). In contrast, the aim of the current measurement setup is to measure the radiated field of the AUT when a user-defined ratio (in both amplitude and phase) is applied between the two signals provided at two feeding ports. Accordingly, the software has been modified to converge to the user-defined complex ratio a_2/a_1.

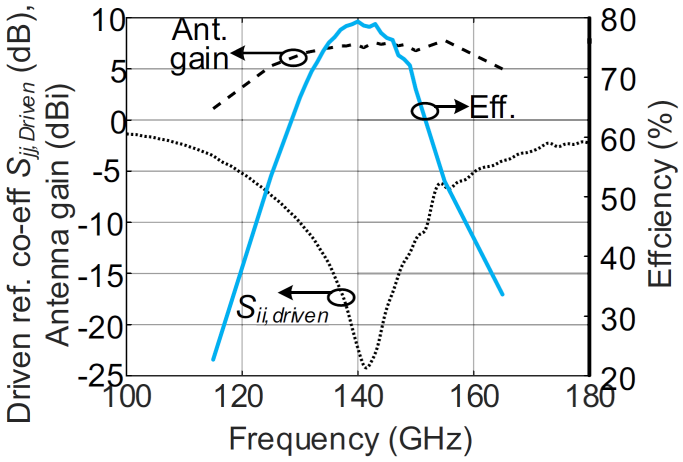
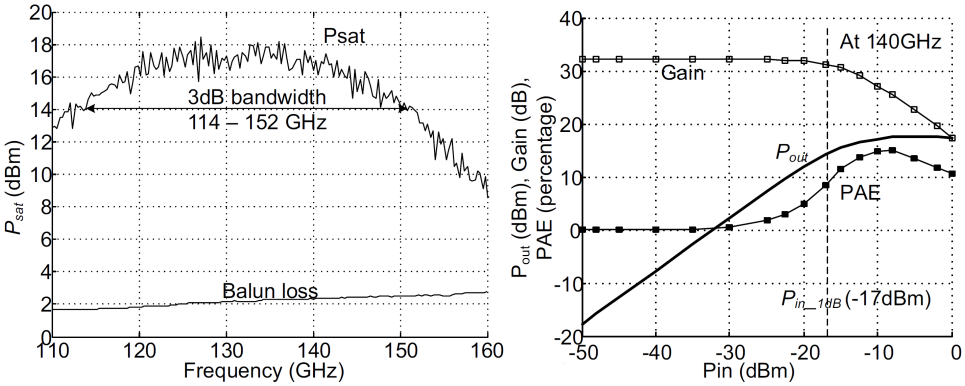


Figure 6.3.: Combining active fed on-chip antenna.



(a) (b)

Figure 6.4.: a) PA large-signal measurement P_{sat} vs. frequency; b) PAE, P_{sat} and Gain vs. P_{in} at 140 GHz.

6.1.3. SETUP CALIBRATION

The calibration procedure follows the same steps as those presented in chapter 5 except for an additional step required to account for the parasitic losses in the received path (RX mixer). This additional step involves a scalar power calibration, in which a scalar factor is determined to relate the power input at the VNA receiver for each frequency point across the entire frequency range. This calibration is conducted following the initial power calibration at the waveguide ports of the extenders, which is thus used to obtain a reference power source for the RX mixer during its calibration (fig. 6.7).

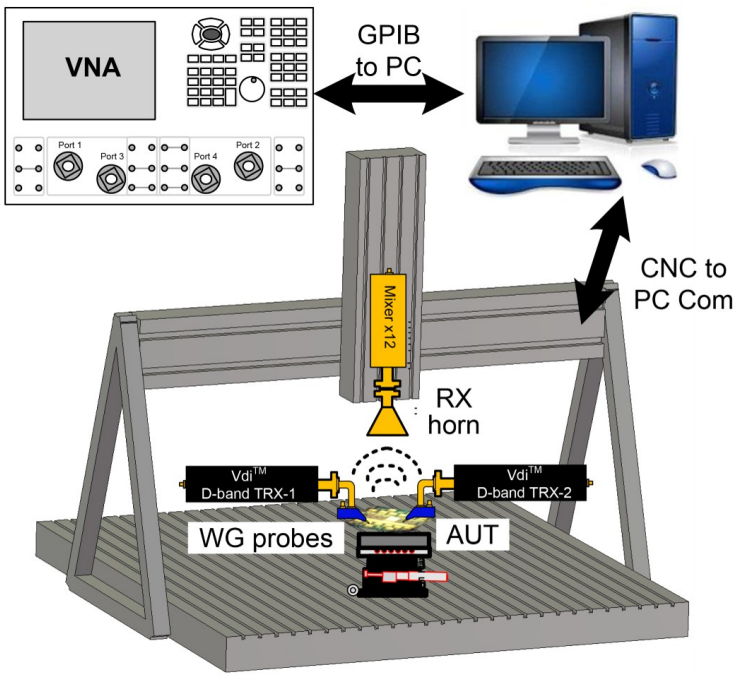


Figure 6.5.: Setup configuration.

6.1.4. MEASUREMENT PROCEDURE

Figure 6.8a illustrates the measurement setup, while fig. 6.8b shows the IC, mounted and bondwired, where the dielectric superstrate has been mounted on the antenna. After the calibration and the modification of the target signal ratio, for the convergence algorithm, from $\Gamma_L = a_2/b_2$ to the ratio a_2/a_1, the measurement setup enables convergence to any user-defined complex ratio between the two feed signals at the two ports. The measurement procedure consists of two main phases, in the first phase, the desired input power at port 1 is set. In the second phase, the algorithm converges to the preset ratio $a_2/a_1 = K$, thereby determining the input power of port 2 ($|a_2|^2$) and the relative phase between the two signals. In this process, a_1 is considered as a reference wave, with its absolute phase set to 0.

6.1.5. MEASUREMENT RESULTS

In order to assess the capability of the setup to provide accurate results first a measurement in-phase (Performed by setting a relative phase between port 1 and port 2 equal to 0 at the calibration reference plane) versus power input of the far-field at 140 GHz has been performed. Then, the EIRP is estimated from far-field power measurements (at

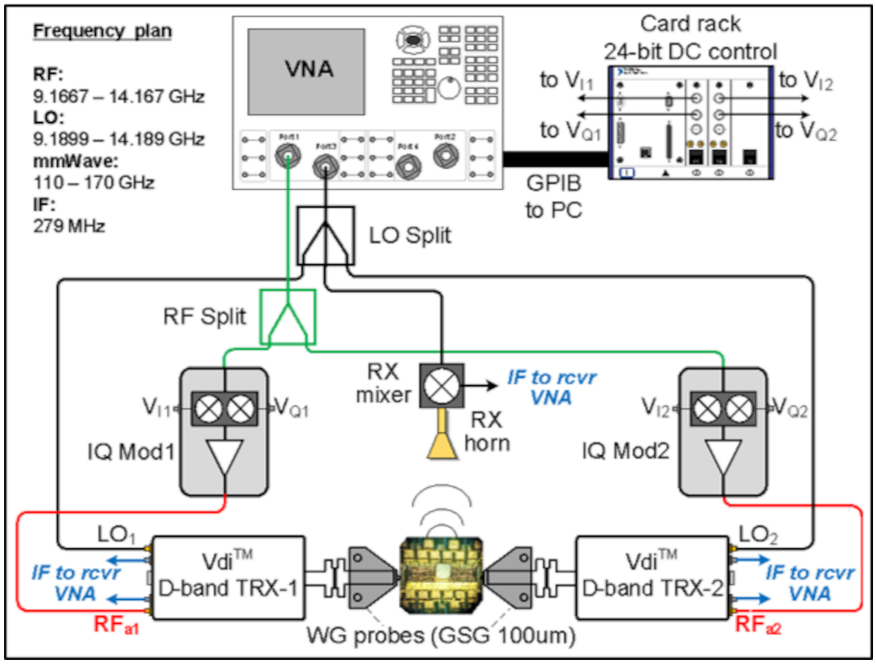


Figure 6.6.: Block schematic of the setup.

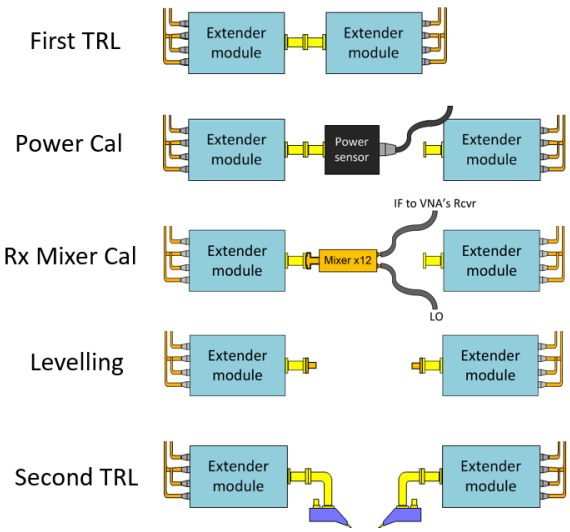
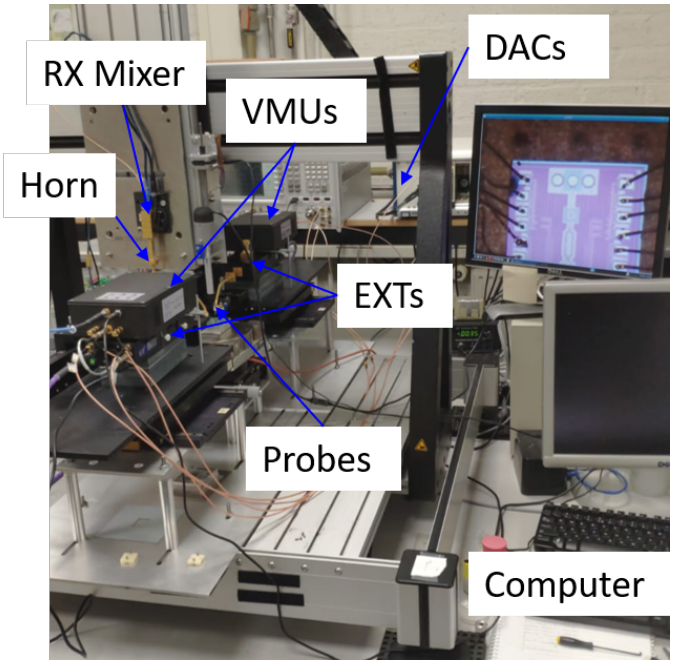
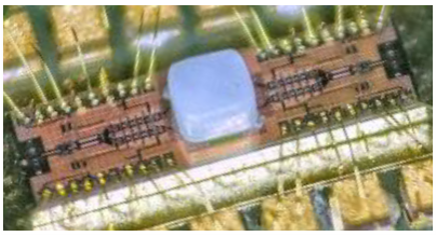


Figure 6.7.: Measurement setup calibration procedure steps.

25 cm) using the Friis' formulation for free-space pathloss. Figure 6.9 shows the comparison of the EIRP with the Pout of the standalone PA showed previously in fig. 6.4b. The



(a)



(b)

Figure 6.8.: a) Measurement setup; b) Micrograph of the assembled IC.

6.8dB difference in gain is the sum of the insertion loss of the output Wilkinson combiner of the standalone PA and the antenna gain. The measured standalone Wilkinson loss (performed in advance) is ~1 dB while the simulated antenna gain is 7 dBi fig. 6.3. The estimated antenna-gain of 5.8 dBi is in close agreement with this simulation. Once the setup has been tested, five repeated measurements in-phase of the EIRP for each frequency point are performed. The result is depicted in fig. 6.10a along with the corresponding fitting curves which shows a 3 dB bandwidth of 132-147 GHz. In fig. 6.10b the EIRP at 140 GHz is shown as a function of the relative phase variation from 0 to 70°. As was expected from the simulations, this plot shows a decrease in the power delivered by the antenna as the relative phase angle between the two sources increases, demonstrating the measurement setup's ability to control the relative phase.

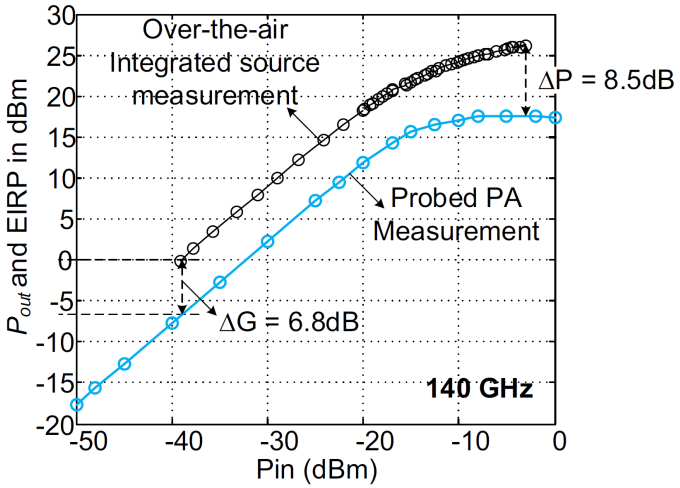
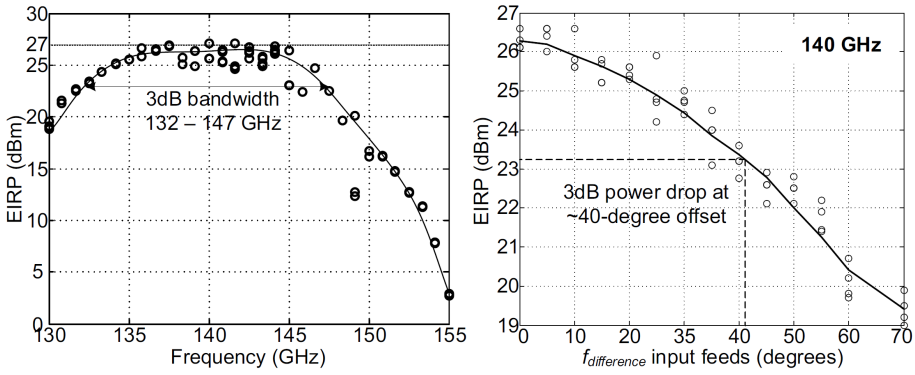


Figure 6.9.: Pout vs. Pin of the integrated source and standalone PA.



(a) (b)

Figure 6.10.: a) EIRP Vs Frequency ensuring 0 degrees as phase relation between port 1 and port 2; b) EIRP Vs relative phase variation at 140 GHz.

6.1.6. CONCLUSIONS

In this section, it has been shown that the setup presented in chapter 5 can be easily reconfigure to perform over-the-air measurements of complex on-chip antennas. The setup is first described in detail in terms of hardware, followed by an explanation of the calibration steps. Finally, measurements of a CAFOA, which requires two coherent sources, are presented. The results include the EIRP versus frequency, spanning from 130 to 155 GHz, and EIRP as a function of the relative phase variation between the two input sources from 0 to 70 degrees. These results highlight the ability of the measurement setup to control the relative phase between the two ports in the millimeter-wave range.

6.2. VECTOR GAIN-BASED EVM ESTIMATION AT MM-WAVE FREQUENCIES

As discussed in chapter 2, the use of frequency extenders based on multipliers in an mm-wave measurement setup results in a highly nonlinear up-conversion chain, which limits the large-signal device characterization to a single-tone excitation. To clarify this statement, in fig. 6.11, the simulation results of a generic x12 multiplier response are reported when the feeding signal consists of two spectral tones with a Δf of ~0.166 GHz that after the multiplication results in the dense frequency spectrum of fig. 6.11b and not the wanted two-tone spectrum with 2 GHz tone spacing. This restrict the large-signal characterization using frequency extenders to single-tone signal, which leads to a lack of comprehensive figures-of-merit concerning the linearity of the DUT. Specifically, this approach confines the analysis to Amplitude Modulation (AM)-AM and AM-Phase Modulation (PM) responses, which, although fundamental parameters of the device, do not provide all the necessary information for optimizing complex state-of-the-art designs. Therefore, there is a clear need for an alternative method to obtain linearity information for nonlinear devices in the mm-wave range. In order to make accurate predictions of the device linearity, there is a need to extract this FOM on millimeter-wave characterization test benches. A linearity FoM proposed in [90] based on the AM-AM distortion in single-tone measurement was shown to closely correlate with the linearity performance of a GaN HEMT measured under two-tone as well as modulated excitation at 31.5 GHz. In this work, a similar approach is proposed to predict the device linearity performance, including both the AM-AM and AM-PM distortion mechanisms. Moreover, the proposed approach also includes the frequency dependency of the device's non-linear transfer function across the operating bandwidth, which plays an important role in the large modulation bandwidths of mm-wave systems. The method proposed is based on a power-sweep, single-tone vector gain measurement of the transistor. These characterization routines are employed to set up a complex, power-dependent, transfer function in the frequency domain. By measuring the load-dependent vector gain over the (signal) operation band at several power levels, an estimation can be made of the EVM response of the device under modulated signals, provided that the memory effect can be kept low. Finally, the proposed vector gain-based EVM estimation method is first benchmarked for its prediction capability versus load pull measurements under modulated signals in the 5 GHz bands on a 22 nm CMOS FD-SOI. Next, vector gain measurements under CW load pull conditions at 165 GHz are used to predict the EVM performance of the device for a QAM16 stimulus signal in this band.

6.2.1. EVM ESTIMATION CONCEPT

The vector gain of a two-port device can be measured from the ratio of the down-converted waves b_2/a_1 in a large signal characterization test bench as was shown in [91]. Following this definition, the vector gain represents a complex transfer function describing the magnitude and phase response from the input to the output of the device. The nonlinear nature of this transfer function imposes dependency on the bias, frequency, drive

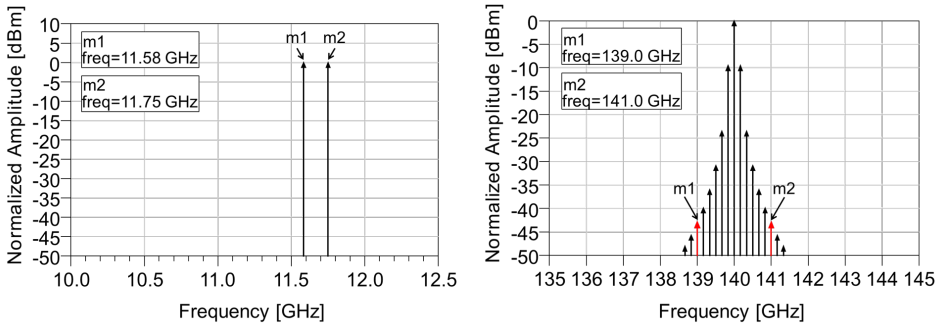


Figure 6.11.: a) Two-tone input signal in a generic x12 multiplier b) and the related simulated dense frequency spectral response of the output signal

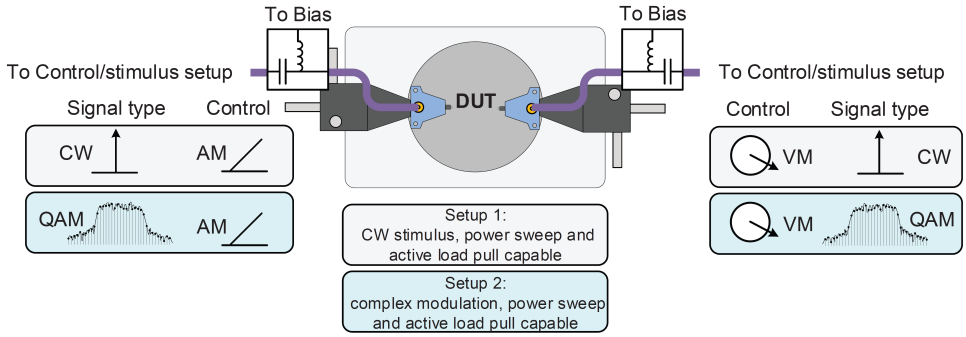


Figure 6.12.: Overview of the measurement setups used.

level, as well as loading condition. This input-to-output behavior can be described by the complex function in eq. (6.1), for every bias and load condition. Here, both the amplitude and phase responses are frequency and power-dependent. This transfer function is acquired by measuring the vector gain at various power levels, frequency points, and for several load conditions (i.e., during load-pull).

$$H(\omega, P_{in}) = A(\omega, P_{in}) * e^{\phi(\omega, P_{in})} \tag{6.1}$$

Where $A(\omega, P_{in})$ describes the power-dependent magnitude transfer and $\phi(\omega, P_{in})$ the power-dependent phase transfer versus frequency. While the non-linear device response is acquired under continuous wave excitation at different frequencies, the input-to-output behavior for modulated signals is computed (numerically) for a multi-tone signal, with a frequency grid compliant to a user-selectable standard definition. For this reason, a relation between the CW power level and the bin-related power level in the modulated signal case needs to be defined. The proposed method relates the constant power (CW case) to the average bin power (modulated case) mapping. Each spectral bin component is then compared to the bin average power (i.e., P_{avg}/Bandwidth) and the relative

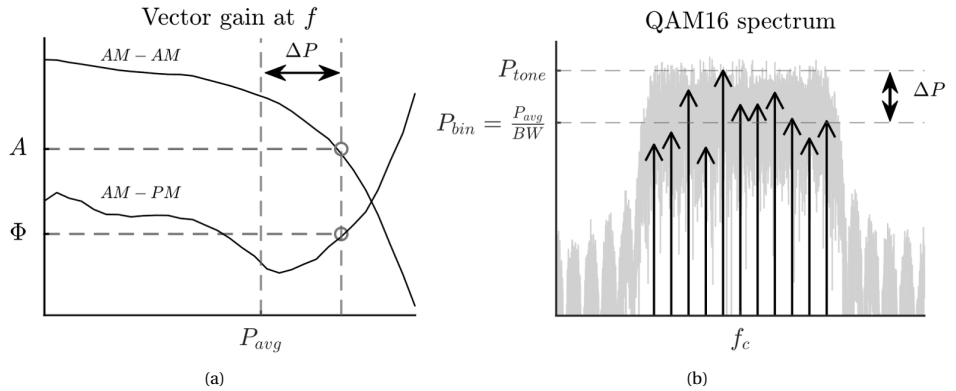


Figure 6.13.: a) Device's vector gain with an example of the distortion values in terms of amplitude and phase; b) Input signal spectrum of a defined modulation type showing the average power.

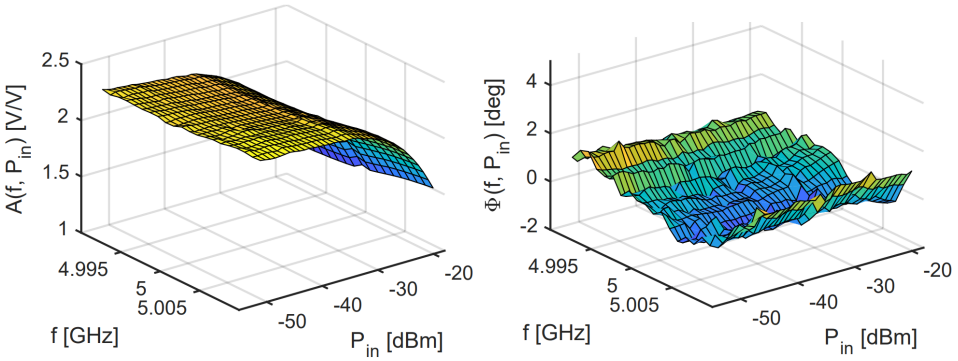
power offset in the vector gain transfer function fig. 6.13a is used to apply the effective distortion (AM-AM and AM-PM) to that frequency bin, see fig. 6.13b. After obtaining the distorted spectrum at the output of the DUT, in the frequency domain, the resulting signal is transformed back to the time domain. The EVM can then be calculated from eq. (6.2).

$$EVM_{rms} = \sqrt{\frac{\sum_n |y_n - x_n|^2}{\sum_n |x_n|^2}} = \sqrt{\frac{P_{error}}{P_{signal}}} \tag{6.2}$$

6.2.2. EVM ESTIMATION BENCHMARKING

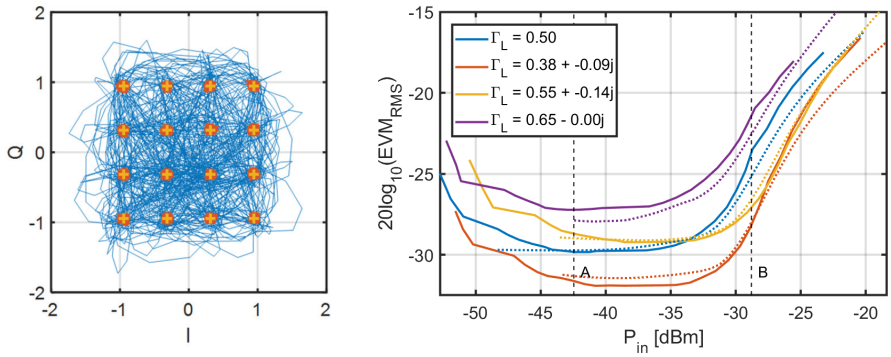
SETUP DESCRIPTION

Two different test benches are employed to validate the proposed vector gain-based EVM estimation of fig. 6.12. Setup 1 is the one presented in chapter 5 that allows the extraction of the CW vector gain versus power at different frequencies, under varying loading conditions. Setup 2 is the Maury Microwave MT-2000 Series Mixed-Signal Active Load Pull system [92] that allows to provide a complex modulated signal to the device under varying loading conditions and acquires the true EVM response of the device. The validation is done at 5 GHz for a QAM16 modulated signal over a 20 MHz band. The vector gain was measured over 21 tones (1 MHz spacing) in the operating band, at 31 source power levels from -30 to 0 dBm (1 dB spacing), and for six different loading conditions around the maximum 1 dB compression point. Figure 6.14 shows the AM-AM gain compression characteristic and the AM-PM phase variation across the frequency band and input power for one of the six loading conditions.



(a) (b)

Figure 6.14.: Magnitude (a) and phase (b) of vector gain measured against frequency centered at 5 GHz and output power at the load for $\Gamma_L = 0.5$



(a) (b)

Figure 6.15.: a) Constellation points estimated using the vector gain at 5 GHz for a QAM16 waveform (P_{in} = −37.85 dBm, Γ_L= 0.5) using 1000 random symbols. b) Correlation between estimated and measured EVM for a QAM16 signal at four loading conditions at 5 GHz. Solid lines are true modulated wave EVM measurements, dashed lines are estimations of the EVM using the vector gain.

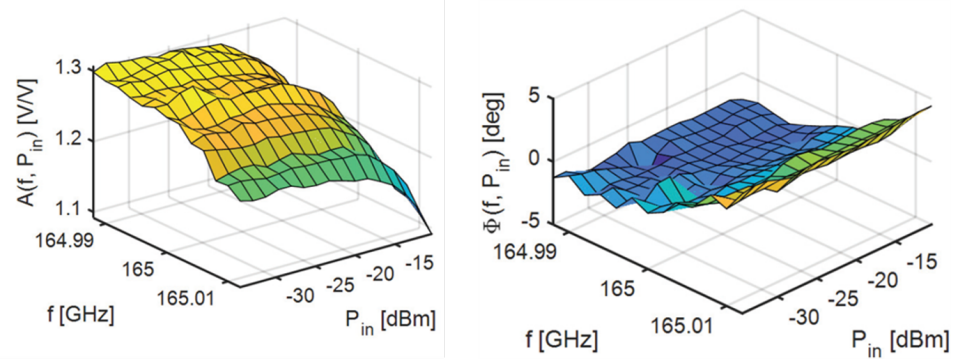
EVM COMPARISON

Figure 6.15b shows the estimated EVM using the vector gain proposed approach versus the directly measured EVM using setup 2 at 5 GHz for a QAM16 signal for four of the six measured loading conditions. However, it is important to note that the absolute value can partially depend on renormalization choices made at the firmware level by the equipment providing true EVM, which are difficult to replicate in the processing of the CW measured data. Therefore, the results are more relevant for evaluating the agreement between the proposed approach and the directly measured EVM values across loading conditions, rather than for assessing absolute accuracy. The prediction of the constellation points for the loading condition $\Gamma_L = 0.5$ at an input power of −37.85 dBm

is shown in fig. 6.15a. This approach, by its nature, accounts only for first-order distortions. Consequently, the estimation remains largely consistent with the measured EVM in the weakly nonlinear region. Beyond point B, the estimated EVM deviates downward from the measured values due to the limited capture of higher-order nonlinearities. Across the whole characterized range, the vector gain EVM estimation can predict which of the loading conditions would achieve the lowest EVM. This shows that the approach is useful in providing a first-order estimation of the best loading condition for EVM, directly from measurements without the need for a model/circuit simulation framework.

6.2.3. OPTIMAL LOADING CONDITION ESTIMATION AT 165 GHZ

To demonstrate the use of the EVM estimation approach, the vector gain of the CMOS devices is measured in a 20 MHz band centered at 165 GHz using the setup presented in chapter 5. The vector gain is measured using single-tone CW load-pull measurements and is used to estimate the EVM for a QAM16 signal. The vector gain is measured at 11 tones (2 MHz spacing) across the operating band, at 16 source power levels from -37.1 to −7.1 dBm (2 dB spacing) and at six loading conditions. Figure 6.16 shows the AM-AM gain compression characteristic and the AM-PM phase variation across the frequency band and input power for one of the six loading conditions at 165 GHz. The EVM for a QAM16 modulated signal is estimated for each of the loading conditions and the result is shown in fig. 6.17 where it is possible to see that, for the specific case, the optimal loading condition for the lowest EVM is Γ_L = 0.15 + j0.20. With the proposed approach of using the vector gain to estimate EVM performance it is possible to evaluate bias conditions, frequencies, drive levels and loading conditions during a large signal CW measurement in the upper millimeter-wave regime without requiring a complex modulated wave setup or the need of a circuit simulator.



(a) (b)

Figure 6.16.: a) Magnitude (a) and phase (b) of vector gain measured against frequency centered at 165 GHz and output power at the load for Γ_L = 0.60 + j0.35.

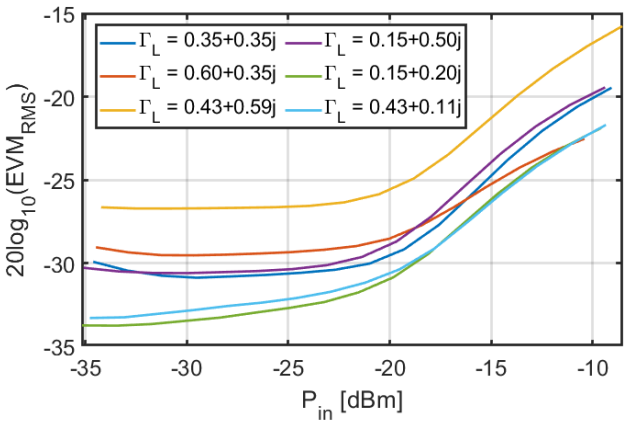


Figure 6.17.: Vector gain-based EVM estimation at 165 GHz for a QAM16.

6.2.4. CONCLUSIONS

In this section, a method is presented for the evaluation of linearity performance under modulated signals of devices operating far into the millimeter-wave regime. The method uses the power-dependent vector gain that is extracted during a continuous wave large signal (load pull) measurement of the device under test to directly estimate the EVM performance of the device. The behavioral model was benchmarked at 5 GHz with modulated wave measurements on a 22 nm FD-SOI device transistor. The vector gain approach shows a good correlation with measured EVM versus power and applied loading conditions for a QAM16 waveform. However, the absolute accuracy in predicting the EVM is limited. As a demonstration, the method is used to estimate EVM performance at 165 GHz where other non-linear characterization methods, such as a two-tone test or modulated signal measurements, are difficult to perform. The EVM estimation could, therefore, be used for the prediction of optimal bias conditions, frequencies, drive levels and loading conditions during a large signal CW measurement in the upper millimeter-wave regime.

7

CONCLUSIONS AND FUTURE WORK

The work presented in this dissertation is focused on addressing a scientific knowledge gap in the design, validation and characterization of sub-THz device models using calibration techniques able to shift the primary calibration plane in close proximity to the intrinsic device in advanced process technologies. Moreover, it introduced and quantified the accuracy levels of (sub)mm-wave large signal test-benches.

7.1. OUTCOME OF THE THESIS

7.1.1. CALIBRATION

The first part of this dissertation is dedicated to providing guidelines for designing, validating and testing M1 calibration kits. The procedure presented starts with an accurate, user-error-free automatic structure build using small units and then combining them like "Lego blocks" to assemble the full, design-rule-compliant structure. This approach allows for high consistency and allows to simplify the structures to make them compatible with 3D EM importing and simulation. A combination of two calibration algorithms was used to cover the frequency range from 1 to 325 GHz, i.e., Short-Open-Load-Reciprocal until 67 GHz and Thru-Reflect-Line above. FD-SOI 22 nm CMOS technology was employed to develop the calibration standards, for which the 3D-EM responses were extracted. Subsequently, a detailed analysis is provided regarding port placement, mesh grid settings, and simulation parameters. Thanks to the 3D simulation environment capability, a method was presented to define the length of the launch line for achieving a quasi mono-modal propagation mode at the reference plane, thereby saving valuable on-wafer area. Finally, all structures were simulated and utilized to perform a full calibration, assessing the expected accuracy using the designed calibration kit. Next, this calibration kit was employed to characterize NMOS with 16 fingers from 1 to 325 GHz. In terms of accuracy, a maximum worst-case error bound of 0.08 across the entire frequency band was obtained. This worst-case error bound was then propagated through the calibration equations to provide an uncertainty bound around the classical DUT technology metrics. This calibration is used to measure the device, with its intrinsic parameters and compared to the model, demonstrating good agreement with the pre-

viously calculated error bounds.

7.1.2. LARGE SIGNAL MEASUREMENT

The second part presented the hardware and software solutions to enable load-pull measurements up to (sub)millimeter-wave frequencies using off-the-shelf equipment. The hardware solution allows for fine control of the phase and amplitude of the feeding signals at ports 1 and 2. This is achieved by employing a high-resolution and low-noise Digital-to-Analog Converter (DAC). Using this DAC, it is possible to achieve a signal control resolution of approximately 6.3 µV, ensuring high repeatability in gamma control. On the software side, an easy, fast, and accurate calibration is provided (i.e., S-parameter and vector power calibration). The phase calibration allows for predicting the first solution for the convergence algorithm, which, given the highly nonlinear response of the setup, ensures that the iteration point remains close to the target point, avoiding offering dangerous reflection coefficients before convergence is achieved. By using the prediction, it was possible to reduce the average number of iterations from 33 to 2.5 per load point, with the maximum gamma absolute distance reduced from 2.64 to 0.13. The overall system was tested on a "thru" connection, achieving a gamma load of 0.9 and sweeping the power from -40 to −5 dBm at 180 GHz. The results show that the power-gain error of the “thru” remained below 0.4 dB. Finally, a 130 µm HBT in SG13G2 technology at 75 GHz and a power amplifier at 135 GHz were measured, demonstrating the capabilities of the novel measurement setup presented. To conclude, it is worth highlighting the frequency scalability of the system. By utilizing the commercial extenders, the system can scale up or down in frequency simply by changing the frequency extenders, making it easy to adapt across the entire millimeter and sub-THz frequency spectrum.

7.2. FUTURE WORK

While this dissertation provides a comprehensive solution to improve mm-wave device characterization, several aspects could still be enhanced.

7.2.1. CALIBRATION

MATERIAL PROPRIETIES SPECIFICATION

Chapter 3 discusses how simulations can be used in design of the test fixture, and the importance of including all structural and material properties to mimic the real electrical response of the structure under simulation. While many factors were considered in this work, all material properties were assumed to be uniform in three directions and equal to nominal values. However, in reality, metal layers are rarely used as compact pieces, particularly in advanced technology nodes, and often exhibit a spatial density based on the technology’s density rules. This could lead to discrepancies between the simulation and real-world performance, which could be addressed by adjusting the material properties according to physical density. Moreover, in certain metal layers (e.g., those used for

vias), there is no electrical continuity in specific directions, which could also affect the simulation. This could be accounted for in the simulator by considering the material's non-homogeneous electrical response.

CALIBRATION STANDARDS RESPONSE SIMULATION

This dissertation also demonstrated in chapter 3 that different calibration algorithms exhibit different worst-case error bounds. One reason for this variation is the amount of information required on the calibration standards to execute the algorithm. Additionally, as explained in chapter 3, a high discontinuity near the waveguide port during simulation can reduce the accuracy of the results. To enable constant probe distance calibration algorithms, such as SOLR, at (sub)mm-wave frequencies, it could be worthwhile to investigate the potential use of accuracy transfer through calibration algorithms, as presented in [93]. This approach could, in fact, make it possible to obtain the calibration standard responses with the same accuracy provided by a TRL algorithm, whether in simulations or measurements.

7.2.2. LARGE SIGNAL MEASUREMENT

TWO-TONE CHARACTERIZATION

As discussed in chapter 2, the mm-wave setup presents many challenges that limit the implementation of standard measurement techniques used at lower frequencies. While some of these limitations have already been addressed in this work, others remain still an open question. One such limitation is the two-tone measurement, which provides information about the linearity of the DUT. Currently, this type of measurement is not possible due to the high non-linearity of the up-conversion chain in frequency extenders. It would be of interest to investigate the use of frequency extenders with two inputs (and thus two up-conversion chains) [94], which would enable the measurement setup presented in chapter 5 to perform two-tone large-signal measurements.

POWER CALIBRATION TRANSFER DEVICE

Chapter 4 presented a power calibration transfer device to enable on-wafer power measurement. Although it has already been shown that this approach can yield good results, it is still subject to technological variations that could effect consistency. Therefore, it would be beneficial to also explore if it is possible to develop new methods predicting the variations in RF behavior of the device by measuring its variation in DC characteristics and correlating them with the RF response.

A

Spectral Purity Evaluation of VNA Frequency Extenders to Enable Electronic Software-Based Power Control

Parts of this appendix have been published in "Spectral Purity Evaluation of VNA Frequency Extenders to Enable Electronic Software-Based Power Control" (2023) and "VNA-Based in-Band Spectral Purity Assessment for MM-Wave Frequency Extenders" (2025) [10, 95].

A

A.1. SPECTRAL PURITY IN A FREQUENCY EXTENDERS

The limitations of coaxial-based environments at frequencies above 67 GHz (i.e., losses, stability) have led to the widespread adoption of waveguide-based measurement setups. These setups rely on external frequency extenders, which utilize frequency multiplier-based up-conversion chains and mixer-based down-conversion chains to first convert the signal to mm-wave frequencies and subsequently transform it back into a coaxial-compatible environment. The use of frequency multipliers, which operate in a saturated regime and exhibit highly nonlinear behavior, along with the absence of ALC for the output signal, presents challenges in controlling the output power. One method for power control, proposed in [9], achieves this by adjusting the relative input power of the extender. However, deviating from the nominal specifications of the multiplier can compromise its expected performance. In particular, one specification that may be affected by this is the spectral quality of the output signal. The degradation of spectral purity can impact the DUT measurements during a large-signal characterization .

A.1.1. CONSEQUENCE OF SPECTRAL PURITY DEGRADATION

During large-signal measurements, the DUT is pushed into an operation region where it exhibits nonlinear behavior, and different metrics can be acquired. In this region, when a single-tone measurement setup is used (such as a VNA-based system [9]), the presence of a multitone signal (i.e., large spurious presence) at the DUT's input can lead to errors in the interpretation of the results. A primary effect is the incorrect measurement of input power. In fact, the narrow-band nature of the measurement setup limits to the measurement of only the fundamental tone, neglecting the energy coming from all the harmonics which are still contributing to the drive level of the DUT. As a result, this extra input power contributes to pushing the DUT into earlier compression, leading to errors in the extracted FoMs, e.g., $\mathrm{Pin}_{1\mathrm{dB}}$, $\mathrm{Pout}_{1\mathrm{dB}}$, $\mathrm{Pout}_{3\mathrm{dB}}$. A secondary effect is the contribution of intermodulation distortion, which will impact the FoMs of the DUT but are ignored by the measurement setup. A simple circuit-based simulation carried out using the Advanced Design System (ADS) from Keysight Technologies can give an indication of the impact of a pure source spectral purity in a device large signal measurement. The simulation consists of a multi-tone source, an isolator, and a generic amplifier model (fig. A.1). To ensure a generalized analysis, a Monte Carlo simulation is used with varying harmonic amplitudes over 200 trials. The considered harmonics include f_{-1}, f_0, f_2, and f_3 (considering f_0 as the fundamental tone) with harmonic variations ranging from a minimum of −100 dBc to a maximum of −15 dBc. This variation results in a maximum harmonic contribution of 4 dB to the input power. The results, presented in fig. A.2, illustrate the variation in power gain. By analyzing the figure, one can assess the potential measurement errors that may arise from an imprecise source and a narrowband measurement setup. In this example, an uncertainty of ∼1 dB in the $\mathrm{Pin}_{1\mathrm{dB}}$ measurement is observed. Therefore, it is necessary to quantify this degradation before employing the mm-wave frequency extenders in a large signal measurement.

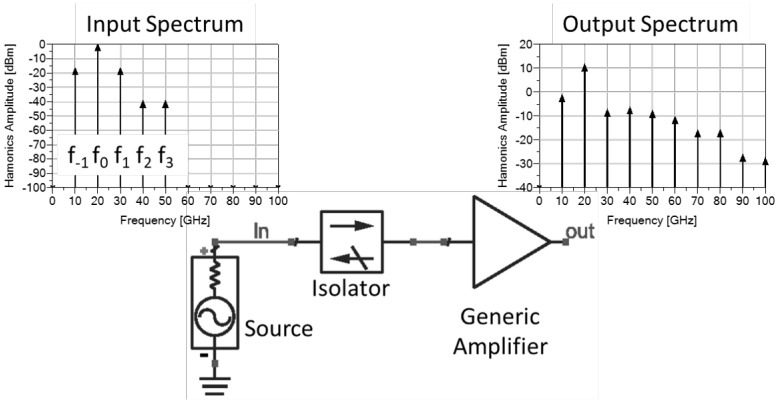


Figure A.1.: ADS simulation setup where only one trial of the Montecarlo analysis is shown in terms of input and output spectra.

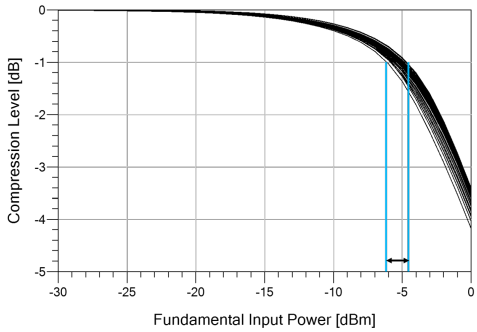


Figure A.2.: Normalized power gain at different harmonic combinations.

A.2. SPECTRAL PURITY ASSESSMENT

There are two methods to evaluate the spectral purity of a mm-wave frequency extender:

- Power meter based
- VNA-based

A.2.1. POWER METER BASED

A calorimeter-based power meter, as the PM5, by its nature, is a true averaging detector which means that the power value measured represents the integrated power spectral density of the input signal over its large bandwidth from 0.075 to 3 THz. Instead, using the narrow band mixer-based receiver of the VNA vector power calibrated, the power measured can be considered spectral power. This means that when considering a signal with a non-continuous spectrum content, as is the case of the signal out of an exten-

der where only harmonic related tones (and few, low power, non-harmonically related tones) are present, the VNA is capable of isolating only the tone of interest. Thus, by performing two simultaneous measurements of the extenders' output power using the two previously mentioned methods (fig. A.3), and then subtracting the obtained values, the spectral purity of the extenders' source can be evaluated. Since the aim is to assess the harmonic contribution to the output signal when the output power is adjusted by varying the multiplier's input power, the same procedure can be repeated for multiple input power levels within the extender's dynamic range

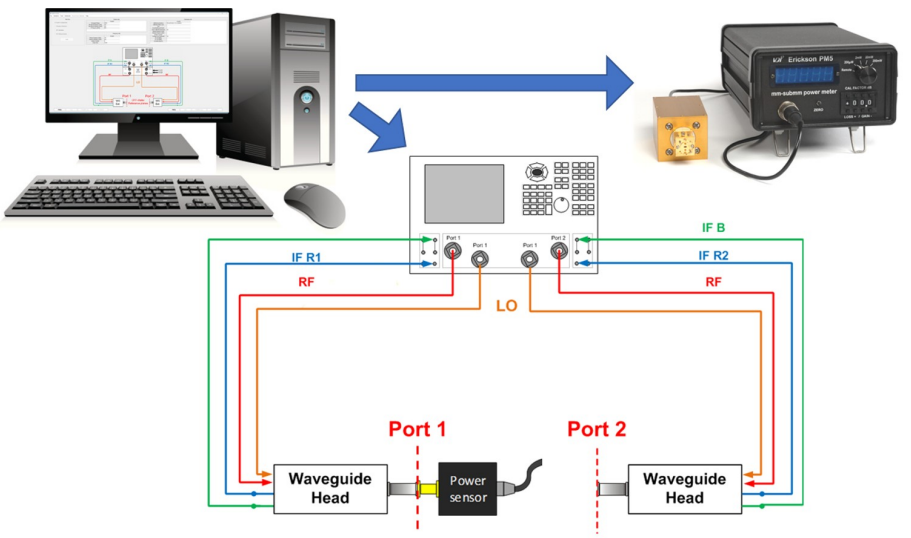
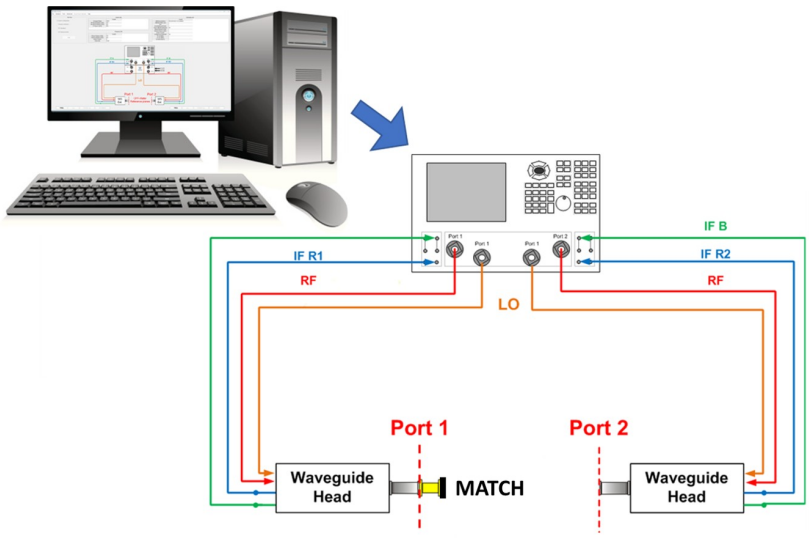


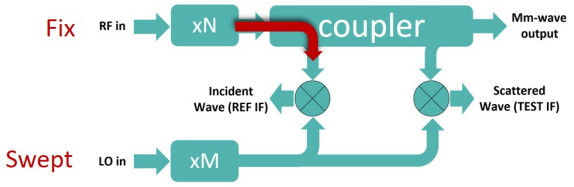
Figure A.3.: Power meter-based measurement setup

A.2.2. VNA-BASED

As previously mentioned, the narrowband, mixer-based receiver of the VNA, vector power calibrated, is capable of measuring the power of a single spectral tone. This feature can be exploited to measure the power of each in-band harmonic tone individually, and then sum them to obtain a reliable approximation of the extender's spectral purity. To perform this measurement, the VNA, which, under standard operation, only considers the fundamental tone and is calibrated at the frequency points selected by the user during system setup, must also be calibrated at the specific harmonic frequency points. Additionally, the calibration and measurement at these harmonic frequencies are enabled by keeping the input frequency (RFin in fig. A.4a) constant, while sweeping the receiving frequency across all harmonic positions. This is accomplished by varying the Local Oscillator (LO) frequency (LOin in fig. A.4a) of the extender's down-conversion chain to target the relevant harmonic frequency points.



(a)



(b)

Figure A.4.: a) VNA-based measurement setup; b) VNA-based method procedure

A.3. METHODS CONSIDERATIONS

The power meter–based method allows for the measurement of the extender's spectral spurious energy within the power meter's bandwidth (i.e., 75 GHz to 3 THz). While effective, this approach has several limitations: it is extremely slow due to the thermal characteristics of the sensor, which, at the lowest scale, requires up to 30 seconds to stabilize; it has a limited dynamic range of approximately 50 dB; it necessitates range setting adjustments during the measurement, each of which introduces additional settling time; and it exhibits uncertainty variations across different measurement ranges. In contrast, the VNA-based method relies solely on the capabilities of the VNA. It is considerably faster, offers a wider dynamic range, and delivers higher accuracy. The only drawback is that the result is an approximation of the actual value, since it is limited to the waveguide band under consideration. However, this can still be regarded as a reliable approximation, as shown in fig. A.5.

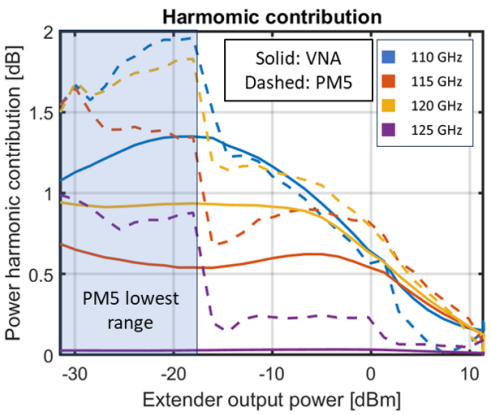


Figure A.5.: Comparison of the unwanted harmonics contribution on the extender output signal measured with the PM5 (dashed line) and with the VNA (Solid Line)

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SUMMARY

Modern commercial applications increasingly rely on advanced communication and sensing capabilities to make autonomous, real-time decisions. This trend continually pushes the demand for higher data communication rates and finer sensing resolution. Meeting these requirements using the currently allocated microwave spectrum has become challenging due to limited available bandwidth and the physical constraints associated with longer wavelengths. Consequently, both research and, more recently, commercial applications have been shifting toward higher-frequency spectrum ranges, where wider bandwidths and shorter wavelengths can be exploited. To support this transition, numerous studies have been published in recent years, documenting significant progress in the electronic device development cycle. Nevertheless, despite these advances, several areas still require improvement. This thesis addresses some of the persistent limitations in the measurement and characterization of electronic devices (both before and after fabrication) where the community continues to rely on low-frequency methods, techniques, or data extrapolated from lower frequencies and applied at higher frequencies. **Chapter 2** begins by reviewing the fundamentals of RF measurements, outlining the distinctions between large-signal and small-signal device behavior, the motivation for using S-parameters in device characterization, and the instruments employed to measure them. In fact, commercial vector network analyzers are typically limited to approximately 70 GHz, necessitating the use of frequency multipliers to access higher-frequency bands. The strong nonlinearities introduced by the up-conversion chain, coupled with the limited bandwidth of waveguide transmission lines, impose significant constraints on standard measurement and characterization approaches.

In RF characterization, the active device is interfaced with the probing environment through embedding in a test fixture. At microwave frequencies (below 40 GHz), open–short de-embedding combined with conventional calibration procedures has become a well-established and highly accurate method for retrieving device-level performance. However, at mm-wave frequencies, the substantial reduction in wavelength profoundly impacts the de-embedding process. For this reason, a direct device-level calibration becomes necessary to incorporate the test fixture's contribution into the broadband calibration error box. **Chapter 3** presents a structured design, simulation, and validation flow for developing a metal-1 test fixture and calibration kit using an automated script-based methodology. The chapter outlines key design considerations for calibration standards and discusses the minimum feasible test fixture size required to achieve an appropriate balance between a clean monomodal field distribution at the calibration reference plane and acceptable area occupancy.

When employing device-level calibration, it is also essential to consider the influence of electrostatic discharge protection diodes, which must be integrated into the test fixture to prevent device damage during fabrication. Although these diodes are intended

to activate only during an electrostatic discharge event, their impedance, particularly their capacitance, varies with applied bias. As a result, the fixture behavior during actual measurements may differ from the behavior observed during calibration, when no voltage is applied. **Chapter 4** introduces a method to mitigate this issue by separating and subsequently combining the port error boxes obtained under the corresponding voltages used during calibration. In addition, when power measurements are required, a power calibration becomes necessary, typically involving a power meter. Since commercial power meters are designed for coaxial and waveguide environments, power calibration for on-wafer measurements requires multiple calibration steps at different planes along with several hardware movements. This reduces the achievable precision and demands extensive handling by the operator. **Chapter 4** also presents the development of a power-calibration transfer device that enables direct on-wafer power calibration using high-performance MOSFETs as transfer elements.

One of the primary RF measurement techniques used to extract information on the nonlinear behavior of active devices is the load-pull method, which evaluates device performance and key parameters under varying load conditions. **Chapter 5** discusses the constraints and challenges associated with load-pull measurements in mmw-wave and introduces a method for performing continuous-wave fundamental load-pull using a commercial standard mm-wave measurement setup.

Finally, **Chapter 6** illustrates how the measurement setups and techniques developed in this dissertation can be applied to characterize complex devices or extract additional information that is otherwise difficult to obtain due to hardware limitations. In the first part, the setup introduced in chapter 5 is used to generate two coherent phase sources for the characterization of a combining active-fed on-chip antenna. The second part presents a method for estimating linearity parameters (specifically the error vector magnitude) using data measured across frequency, power, and bias, based on the calibration method described in chapter 3 together with the measurement setup developed in chapter 5.

LIST OF FIGURES

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Acronyms

2D Two-Dimensional. 24, 125

3D Three-Dimensional. 5, 125

AI Artificial Intelligence. 1, 125

ALC Automatic Level Control. 10, 125

AM Amplitude Modulation. 90, 125

AUT Antenna Under Test. 82, 125

BEOL Back-End Of Line. 15, 125

BiCMOS Bipolar CMOS. 61, 125

CAD Computer-Aided Design. 28, 125

CAFOA Combining Active-Fed On-Chip Antenna. 82, 125

Cgs Gate-Source Capacitance. 39, 125

CL-ICPW capacitively-Loaded Inverted Coplanar Waveguide. 22, 125

CMOS Complementary Metal-Oxide-Semiconductor. 4, 125

CMP Chemical-Mechanical Polishing. 21, 125

CPW Coplanar Waveguide. 14, 125

CW Continuous Wave. 5, 125

DAC Digital-to-Analog Converter. 98, 125

DR Dynamic Range. 10, 125

DRA dielectric resonator antenna. 83, 125

DRC Design Rule Checking. 26, 125

DUT Device Under Test. 7, 125

EB Error Bound. 38, 125

EIRP Effective Isotropic Radiated Power. 82, 125

EM Electromagnetic. 5, 125

ESD Electrostatic Discharge. 5, 125

ET Error terms. 13, 125

EVM Error Vector Magnitude. 5, 125

FD-SOI Fully Depleted Silicon-On-Insulator. 40, 125

FMCW Frequency-Modulated Continuous Wave. 3, 125

FoM Figure of Merit. 7, 125

GaN Gallium Nitride. 125

GDS Graphic Data System. 28, 125

GSG Ground-Signal-Ground. 15, 125

HBT Heterojunction Bipolar Transistor. 4, 125

HEMT High Electron Mobility Transistor. 125

HW Hardware. 9, 125

IC Integrated Circuit. 68, 125

IF Intermediate Frequency. 9, 125

ISS Impedance Standard Substrates. 20, 125

ITU International Telecommunication Union. 4, 119, 125

LRM Line-Reflect-Match. 13, 125

LRRM Line-Reflect-Reflect-Match. 20, 125

M1 Metal 1. 5, 125

NF Noise Figure. 7, 125

NMOS N-channel Metal-Oxide-Semiconductor. 40, 125

PA Power Amplifier. 68, 125

PAE Power Added Efficiency. 82, 125

pCTD Power Calibration Transfer Device. 58, 125

PDK Process Design Kit. 20, 125

PLL Phase-Locked Loop. 10, 125

PM Phase Modulation. 90, 125

RADAR Radio Detection And Ranging. 3, 125

RF Radio Frequency. 3, 125

SiGe Silicon-Germanium. 4, 125

SNR Signal-to-Noise Ratio. 10, 125

SOI Silicon-on-Insulator. 24, 125

SOL Short-Open-Load. 31, 125

SOLR Short-Open-Load-Reciprocal. 13, 125

SOLT Short-Open-Load-Thru. 20, 125

SSL Short-offset Short-Load. 62, 125

STD Standard. 22, 125

SW Software. 9, 125

TRL Thru-Reflect-Line. 13, 125

VNA Vector Network Analyzer. 9, 125

VSL Van Swinden Laboratory. 40, 125

WCEB Worst-Case Error Bound. 38, 125

GLOSSARY

β_0 DC current gain. 7, 125

FT Cut-Off Frequency. 44, 125

P_{1dB} Maximum input or output power an amplifier can handle before its performance becomes significantly non-linear. 7, 125

WR10 Waveguide frequency band from 75 to 110 GHz. 11, 125

WR2.2 Waveguide frequency band from 330 to 500 GHz. 125

WR3 Waveguide frequency band from 220 to 325 GHz. 39, 125

WR5 Waveguide frequency band from 140 to 220 GHz. 40, 125

WR6.5 Waveguide frequency band from 110 to 170 GHz. 10, 125

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2. Z. Gao, **C. De Martino**, M. Pelk, S. Lehmann, and M. Spirito. "Characterization Approaches to Reduce Process Variation Dependencies for on-Wafer Power Calibration Transfer Devices in BiCMOS Technologies". In: *2025 IEEE/MTT-S International Microwave Symposium - IMS 2025*. 2025, pp. 907–910. DOI: 10.1109/IMS40360.2025.11103834

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Propositions

accompanying the dissertation

Novel Calibration Approaches and Large Signal Measurement Techniques for Sub-THz Devices Characterization

by

Carmine DE MARTINO

1. High frequency modelling strategies have been focused on minimizing the error of sub-optimal solutions rather than optimizing the approach in the first place (this thesis, Chapter 3).
2. Interchanging error boxes between two different TRL calibrations is possible only if the element difference can be modelled as a reciprocal device. (This thesis, Chapter 4).
3. The phase prediction of the up-converted injected wave is the key aspect that has enabled a fast and robust sub-THz load-pull system (This thesis, Chapter 5).
4. Fundamental source pull in large signal measurements is commercially attractive, but does not provide any extra measurement information.
5. The scientific community has neglected the limited spectral quality and its impact on the measured metrics of multiplier-based RF sources used in single-tone characterization.
6. Prof. Dr. Earl McCune once said:" Only measurement contains 100% of the truth". The statement is correct, but it requires 100% of trust in your measurements.
7. Maintaining a reasonable level of worries is key to psychological well-being and a happy life.
8. No expectations translate into no let-downs. When we let go of the big plans, we start enjoying also the small moments in life, for example, reaching our destination using the Dutch railway system (personal experience).
9. The key difference between working in a startup and in a larger company lies in the way you consider your role, fundamental in the first case and simply useful in the second.

These propositions are regarded as opposable and defendable, and have been approved as such by the promoters Prof. dr. L.C.N. De Vreede and Dr. M. Spirito.

About the Author

Carmine De Martino was born in Battipaglia, Salerno, Italy, in 1988. He is currently a Senior R&D Engineer at Maury Microwave, Eindhoven, The Netherlands, where he develops advanced millimeter-wave measurement solutions. He received first his B.Sc in from the University of Salerno, Salerno, Italy, in 2012 and then the M.Sc. degree in Electrical Engineering from the University of Naples Federico II, Naples, Italy, in 2015. His master's thesis project, carried out at Delft University of Technology, focused on smart-antenna measurement techniques.

In 2015, he joined the Electronic Research Laboratory at Delft University of Technology as a Researcher, and in 2016 he began his Ph.D. studies. From 2020 to 2024, he served as a Senior Application Engineer at Vertigo Technologies, where he contributed to high-frequency measurement solutions and advanced instrumentation.

His research interests span several areas of high-frequency and millimeter-wave engineering, including the development of novel calibration and measurement paradigms up to the sub-THz range, small- and large-signal device characterization, 3-D electromagnetic simulation of passive components, and antenna characterization in the millimeter-wave and sub-THz domains.

Mr. De Martino received the Best Student Paper Award for his contribution to the 93rd ARFTG Microwave Measurement Conference in 2019 with the article entitle: "A TRL Error-box Split Procedure to Compensate for the Bias Dependency Effects in Device Test-Fixtures".

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NOVEL CALIBRATION APPROACHES AND LARGE SIGNAL MEASUREMENT TECHNIQUES FOR SUB-THZ DEVICES CHARACTERIZATION

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