Load-Modulation-Based IMD3 Cancellation for Millimeter-Wave Class-B CMOS Power Amplifiers Achieving EVM < 1.2%

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Load-Modulation-Based IMD3 Cancellation for Millimeter-Wave Class-B CMOS Power Amplifiers Achieving EVM < 1.2%

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***Abstract*— This letter presents a novel load-modulation-based 3rd-order intermodulation distortion (IMD3) cancellation technique for class-B CMOS power amplifiers (PAs). In a class-B PA, the IMD3 generated by the 3rd-order transconductance (g_{m3}) and the gain compression have opposite signs, and thus, they can cancel each other at specific bias and loading conditions. The proposed Doherty topology allows adjusting the gain compression by modulating the effective loading, facilitating IMD3 cancellation over the entire load modulation region. The proposed approach is verified using a 28 GHz 40 nm CMOS series-Doherty PA (DPA) topology. The experimental result demonstrates 10/17 dB IMD3 improvement compared to class-B/DPA operation. Without using any digital pre-distortion, the measured EVM of the proposed technique for a 50 MHz 64-QAM OFDM signal with 8.9 dBm average output power is −38.7 dB (1.2%), which is 5.7/11 dB better than a standard class-B/DPA operation.**

***Index Terms*— 5G New Radio (NR), Doherty, intermodulation distortion, load modulation, millimeter-wave, power amplifiers (PAs).**

I. Introduction

MILLIMETER-WAVE (mm-wave) 5G communication systems have been rapidly developing to address the market demand for high data throughput and user capacity. Their transmitters (TXs) typically employ spectrally efficient complex modulation schemes with high peak-to-average power ratios (PAPRs). However, this requires the operation of the power amplifiers (PAs) in power back-off (PBO) to fulfill the stringent linearity requirements like the adjacent channel leakage ratios (ACLRs) and error vector magnitudes (EVMs). The key design trade-off is the PA linearity and efficiency close to compression.

Since the PAs typically operate at relatively high-power levels, their actual 3rd-order intermodulation distortion (IMD3) mechanism must be investigated under these conditions rather than in low-power operation [1]. Four dominant IMD3 contributors are present in a CMOS PA: 1) the 3rd-order transconductance (g_{m3}); 2) the gain compression due to drain voltage clipping; 3) the voltage-dependent nonlinear parasitic capacitors (e.g., gate–source C_{gs}, gate–drain C_{gd}, and gate-bulk C_{gb}); and 4) the 2nd-order mixing products. Enhanced 2nd-harmonic termination [2], [3], pMOS varactor-based amplitude-to-phase (AM-PM) compensation [4], [5], hybrid nMOS/pMOS PA structures [6]–[8], and transformer-based AM-PM correction [9] are proposed to improve the mm-wave PAs' linearity, deteriorated by the 2nd-order mixing products and nonlinear capacitors. Moreover, adaptive biasing, multi-gate transistor, and antiphase [10]–[18] techniques are proposed for IMD3 cancellation. However, their cancellation regions are narrow and occur at low power levels, making them less suitable for PAs operating closer to compression.

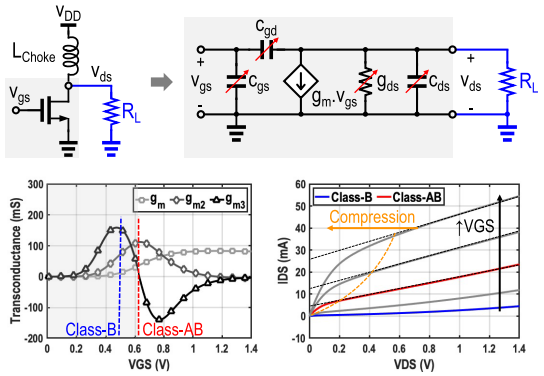

Fig. 1. Equivalent model of a common-source PA. The simulated g_m, g_{m2}, and g_{m3} of a 40 nm nMOS transistor versus gate bias voltage and drain–source current versus drain–source voltage are given.

In this letter, a new load-modulation concept is presented for IMD3 cancellation in energy-efficient class-B/deep class-AB operation. In a class-B PA, the IMD3 generated by g_{m3} and gain compression have opposite signs, and thus, they can cancel each other at a specific point. This condition provides a sweet spot near the PA's peak power level. The proposed load-modulated PA topology allows dynamic adjustment of the gain compression point by modulating the load seen by the drain nodes. Consequently, this mechanism can suppress the IMD3 generated by g_{m3} over a large PBO range.

II. Load-Modulation-Based IMD3 Cancellation

A. Load-Modulation-Based IMD3 Cancellation Principles

Fig. 1 depicts an equivalent model of a common-source PA. A 40 nm nMOS transistor's transconductance (g_m) and its 1st and 2nd derivatives (g_{m2} and g_{m3}) are given versus gate bias voltage (VGS). For a highly efficient class-B PA, the bias point is chosen close to the turn-on point where g_m starts to increase, and the g_{m3} reaches its maximum value with a positive sign

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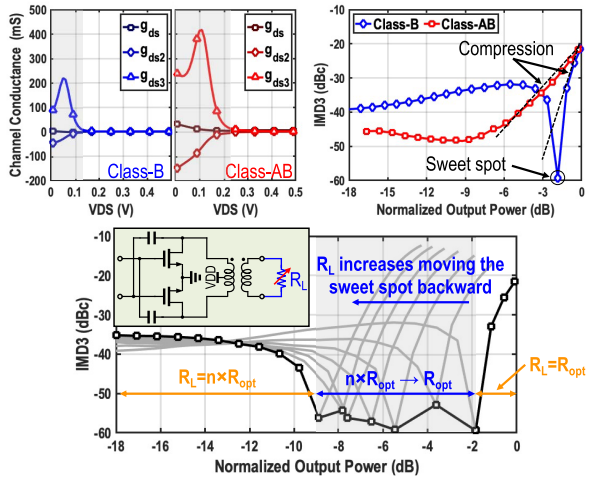

Fig. 2. g_{ds}, g_{ds2}, and g_{ds3} versus VDS and the two-tone simulation results of class-B and class-AB PAs (top). The two-tone simulations for various R_L exhibiting IMD3 sweet spot at lower output power levels (bottom).

because of the PA's gain expansion. On the other hand, in a pure class-AB operation, the quiescent bias point at low-power operation provides low IMD3 while g_{m2} is at its maximum, entailing 2nd-order mixing products, giving rise to higher IMD3. Furthermore, the drain–source currents are presented versus drain–source voltage (VDS) for various gate bias points. The transistor enters the linear region by decreasing VDS, resulting in gain compression and, thus, entailing an IMD3 component with a negative sign.

To gain more insight, the 1st-, 2nd-, and 3rd-order channel conductance (g_{ds}, g_{ds2}, and g_{ds3}) versus VDS for the class-B and class-AB are depicted in Fig. 2 (top-left). It shows that the class-AB operation introduces high IMD3 at higher power levels due to its higher bias voltage. In contrast, the class-B operation offers lower IMD3 at higher power levels as it is biased close to its turn-on region. Moreover, since the class-B has positive g_{m3} at lower power levels and negative g_{ds3} at higher power levels due to gain compression, moving from lower to higher power levels, an IMD3 sweet spot is expected, as shown in Fig. 2 (top-right). Nevertheless, this sweet spot is observed only at a single output power level yielding a sharp notch.

To take practical advantage of this IMD3 sweet spot, the cancellation should happen over a larger dynamic range. Since the gain compression depends on the output voltage swing, the sweet spot is shifted to lower output power levels by increasing the load resistor (R_L). Fig. 2 (bottom) demonstrates two-tone IMD3 simulations for various R_L. Accordingly, if R_L is modulated dynamically to maintain the output gain compression point at a region where the IMD3 component caused by g_{ds3} cancels its counterpart generated by g_{m3}, IMD3 suppression can be achieved for a wide output power range.

B. Proposed Load-Modulated Linear PA (LLPA)

Fig. 3 (top) depicts parallel- and series-Doherty PA (DPA) structures that use load modulation techniques to enhance their PBO efficiency. In a DPA structure, the auxiliary PA (i_a) modulates the main PA's load (Z_m) to keep its drain voltage (v_m) at the maximum swing, maintaining the maximum drain efficiency (see Fig. 3, middle). Employing the same topology, the proposed LLPA features a new load modulation scheme to provide linearity enhancement. In this context, the load

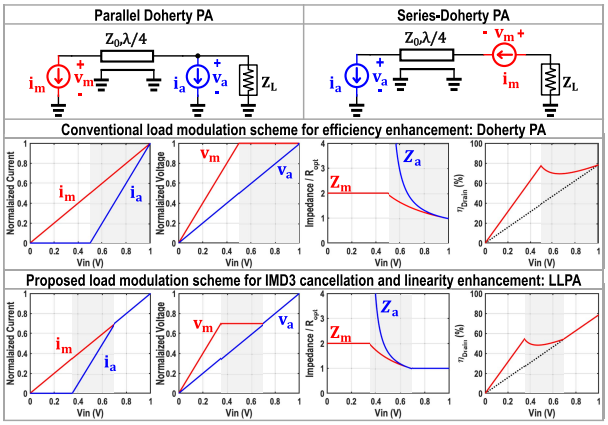

Fig. 3. Parallel and series DPAs' simplified structures (top), the load modulation scheme of conventional DPA (middle), and the proposed load modulation scheme for IMD3 cancellation (bottom).

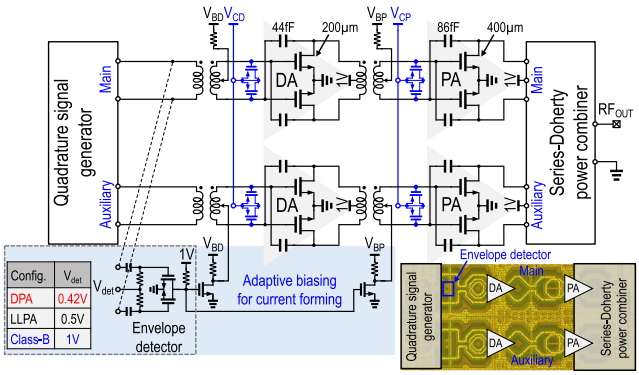

Fig. 4. Schematic and die photo of the employed 28 GHz series-DPA to realize the proposed LLPA.

modulation starts sooner than a conventional DPA to keep v_m at its optimum level where the sweet spot occurs, achieving IMD3 cancellation (see Fig. 3, bottom). Consequently, the main PA works in three loading conditions: 1) the low-power region where $R_L = 2 \times R_{\text{opt}}$; 2) the load modulation region while R_L is modulated from $2 \times R_{\text{opt}}$ to R_{opt}; and 3) the high-power region where $R_L = R_{\text{opt}}$. Note that the drain efficiency at PBO is degraded in this new arrangement compared to the conventional DPA to benefit the linearity. It is worth mentioning that in an ideal DPA structure, the output power and linearity are determined by the main PA, whereas the auxiliary PA only regulates the main PA's drain voltage.

III. Implementation and Experimental Results

As proof of concept, the proposed IMD3 cancellation load modulation technique is verified using a 28 GHz 40 nm CMOS series-DPA prototype [19].

A. Circuit Implementation

The prototype contains two identical series-DPAs that are combined through a quadrature hybrid coupler, achieving more than 20 dBm peak power to meet the 5G application requirements [19]. Fig. 4 shows the employed series-DPA topology, which can be reconfigured exploiting its (dynamic) biasing conditions to realize the proposed LLPA. Each main/auxiliary branch comprises a neutralized driver amplifier (DA), a transformer as inter-stage matching, and a neutralized

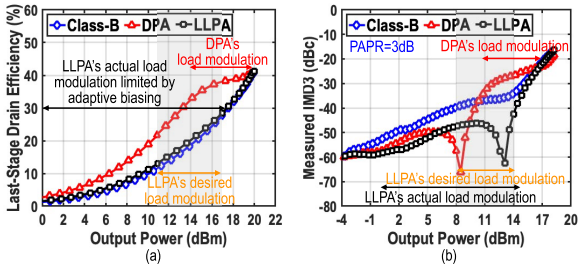

Fig. 5. (a) CW and (b) two-tone IMD3 measurement results versus output power.

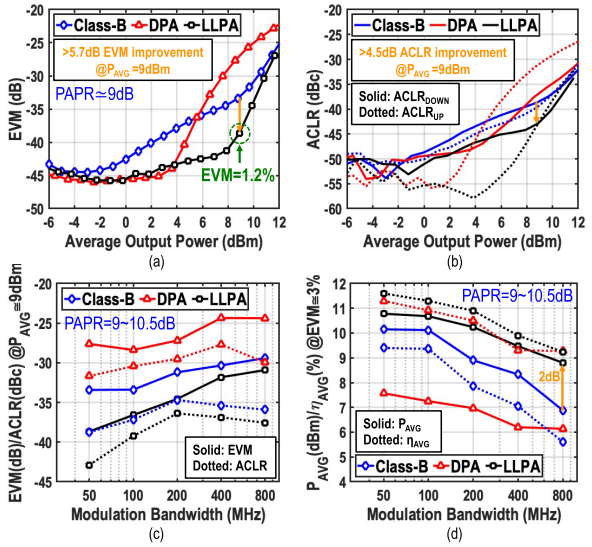

Fig. 6. Measured (a) EVM and (b) $\text{ACLR}_{\text{DOWN}}$ (solid)/ACLR_{UP} (dotted) of a 50 MHz 64-QAM OFDM versus PAVG. (c) Measured EVM (solid) and ACLR (dotted) of the 64-QAM OFDM signals at 9 dBm P_{AVG}. (d) P_{AVG} (solid) and η_{AVG} (dotted) when EVM = 3% for 64-QAM OFDM signals.

common-source push-pull PA. The PAs are connected to a series-Doherty power combiner (a detailed combiner design method is discussed in [20]). Adaptive biasing circuits modulate the biases of the auxiliary branch to perform load modulation. Using the detection bias voltage of the envelope detector (V_{det}), the load modulation can be configured to operate in three modes: 1) a conventional efficiency enhancement for a DPA; 2) the proposed IMD3 cancellation (LLPA); and 3) two standard class-B PAs whose loads are always equal to R_{opt} and simply power-combined through the Doherty passive network. Moreover, two pMOS varactors at the input of the DA and PA improve the AM-PM profile, which was mainly set by nonlinear nMOS gate capacitors [4].

B. Experimental Results

The performance of the proposed technique is measured at 28 GHz carrier frequency. The measured last-stage drain-efficiency of the LLPA ($V_{\text{det}} = 0.5$ V) is compared to the class-B PA ($V_{\text{det}} = 1$ V) and DPA ($V_{\text{det}} = 0.42$ V) operating conditions in Fig. 5(a). Note that all bias and supply voltages (except V_{det}) are kept the same for these three configurations. In this prototype, the control of the envelope detector and adaptive biasing speed is somewhat limited. Therefore, the load modulation starts at a lower power level yielding some drain efficiency degradation at deep PBO. However, the LLPA

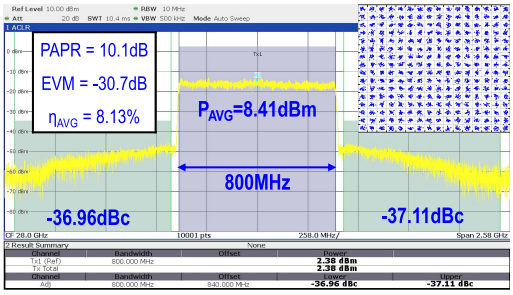

Fig. 7. Measured spectrum and constellation of an 800 MHz 256-QAM OFDM signal.

TABLE I
EXAMPLE OF A TABLE

	This work		Park IMS 2016 [2]	Vigilante RFIC 2017 [4]	Li IMS 2021 [6]	Ali ISSCC 2018 [9]	Choi LMWC 2020 [10]
Linearization Technique	Load-modulation-based IMD3 cancellation		2nd harmonic termination	Varactor-based AM-PM compensation	NMOS/PMOS power combining	Transformer based AM-PM correction	Three-stage antiphase
Technology	40nm CMOS		28nm CMOS	28nm CMOS	45nm SOI	65nm CMOS	65nm CMOS
Supply (V)	1		2.2	0.9	1.1	1.1	1
Freq. (GHz)	28		28	43	55	28	25
P_{SAT} (dBm)	20.1		19.8	16.6	16.3	15.6	17.3
η_{PEAK} (%)	40.6		43.3 (PAE)	24.2 (PAE)	35.4 (PAE)	41 (PAE)	32 (PAE)
Modulation scheme	64-QAM OFDM	256-QAM OFDM	64-QAM WLAN	64-QAM (at 34GHz)	64-QAM CP-OFDM	64-QAM	64-QAM WLAN
Modulation bandwidth (MHz)	50	800	80	675	800	340	20
PAPR (dB)	8.9	10.1	10.8	8.3	9.8	NR	10.55
EVM_{RMS} (dB)	-38.7 (1.2%)	-30.7 (2.92%)	-27.5	-25	-23.2	-26.4	-25
ACLR (dBc)	-42.9	-36.96	NR	-30.2	-26.4	-30	NR
P_{AVG} (dBm)	8.9	8.41	10.97	8.9	8	9.8	10.2
η_{AVG} (%)	9.46	8.13	17.3 (PAE)	4.4 (PAE)	8.1 (PAE)	18.2 (PAE)	6.8 (PAE)

exhibits >10 dB IMD3 improvement over its class-B operation in a two-tone test scenario [see Fig. 5(b)].

The measured EVM and ACLR of a 50 MHz 64-QAM OFDM signal versus average output power (P_{AVG}) for three PA operating conditions are depicted in Fig. 6(a) and (b) without using any digital pre-distortion. The proposed LLPA achieves −38.7 dB EVM at 8.9 dBm P_{AVG}, which is 5.7/11 dB lower than its class-B/DPA counterparts. Likewise, the measured ACLR is 4.5 and 11 dB lower than the class-B and DPA, respectively. Fig. 6(c) shows the EVM and ACLR for various modulation bandwidths when $P_{\text{AVG}} = 9$ dBm. Furthermore, the measured P_{AVG} and average drain efficiency (η_{AVG}) are demonstrated for various modulation bandwidths when EVM = 3% [see Fig. 6(d)]. Note that EVM = 3% is required for supporting a 256-QAM OFDM signal. The measurement shows that the proposed LLPA achieves the highest P_{AVG} and η_{AVG} for a specified EVM. Namely, for the 800 MHz modulated signal, LLPA offers 2 dB higher P_{AVG} compared to the class-B configuration. Moreover, the measured spectrum and constellation of an 800 MHz 256-QAM OFDM signal with 8.41 dBm P_{AVG} is exhibited in Fig. 7, offering −30.7 dB EVM and −37 dBc ACLR. The performance of our LLPA is summarized in Table I and compared to the prior art.

IV. CONCLUSION

This letter presents a load-modulation-based IMD3 cancellation technique for class-B CMOS PAs. The experimental result demonstrates >10 dB IMD3 improvement compared to a class-B PA. The measured EVM/ACLR of the proposed approach for a 50 MHz 64-QAM OFDM signal with 8.9 dBm average power are −38.7 dB/−42.9 dBc, respectively, which are 5.7/4.5 dB better than the class-B configuration.

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