

A novel 4H-SiC multiple stepped SGT MOSFET with improved high frequency figure of merit

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PAPER

A novel 4H-SiC multiple stepped SGT MOSFET with improved high frequency figure of merit

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21 November 2023Jingping Zhang¹ , Houcai Luo¹, Huan Wu¹, Zeping Wang¹, Bofeng Zheng¹, Guoqi Zhang² and Xianping Chen^{1,3}¹ Key Laboratory of Optoelectronic Technology & Systems, Chongqing University, Chongqing, People's Republic of China² Delft Institute of Microsystems and Nanoelectronics, Delft University of Technology, Delft 2628 CD, The Netherlands³ Key Laboratory of Power Transmission Equipment & System Security and New Technology, Chongqing University, Chongqing, People's Republic of ChinaE-mail: xianpingchen@cqu.edu.cn

Keywords: 4H-SiC MOSFET, SG, Cgd, Qgd, HF-FOM, switching loss

Abstract

A novel 4H-SiC Multiple Stepped SGT MOSFET (MSGT-MOSFET) is presented and investigated utilizing TCAD simulations in this paper. We have quantitatively studied the characteristics of the device through simulation modeling and physical model calculations, and comparatively analyzed the performance and application prospects of this novel device. The gate-to-drain capacitance (C_{gd}) and gate-to-drain charge (Q_{gd}) of the MSGT-MOSFET are significantly reduced in comparison with the double trench MOSFET (DT-MOSFET) and the conventional SGT MOSFET (CSGT-MOSFET), due to the reduction of the overlapping area of the split gate (SG) structure and drift region. Therefore, the obtained high frequency figure of merit (HF-FOM) defined as $[R_{on} \times C_{gd}]$ reduced by 23.9% compared with DT-MOSFET and CSGT-MOSFET. And the HF-FOM $[R_{on} \times Q_{gd}]$ for the MSGT-MOSFET significantly decreased by 71% and 50%, respectively, compared to that of the DT-MOSFET and CSGT-MOSFET. Furthermore, the switching loss is also simulated and calculated. And the total switching loss of the proposed MSGT-MOSFET realizes 42.9% and 21.7% reduction in comparison with the DT-MOSFET and CSGT-MOSFET. The overall enhanced performances suggest that the MSGT-MOSFET is an excellent choice for high frequency power electronic applications.

1. Introduction

4H-SiC MOSFETs are an attractive power semiconductor device in electronic systems for its high power rating, fast switching speed, and low drive power consumption [1–5]. Compared to SiC planar MOSFETs, SiC trench MOSFETs are more popular in the industry for their better tradeoff between on-resistance and breakdown voltage [6–9]. The most advanced 4H-SiC trench MOSFETs in the industry today are Infineon's asymmetric trench MOSFETs and Rohm's double trench MOSFETs [10–12]. Double trench MOSFETs (DT-MOSFET) are more favored because of their greater design flexibility and lack of process limitations for high-energy ion implantation [13–16]. Therefore, 4H-SiC DT-MOSFETs are one of the best power switching devices due to their extremely low on-resistance (R_{on}), high breakdown voltage (BV) and fast switching speed, etc [17, 18].

In order to reduce the power dissipation in high frequency and high power applications, the C_{gd} of the MOSFET must be minimized because the power dissipation originates from their charging and discharging during each switching cycle [19–21]. Based on this, Split Gate Trench (SGT) MOSFETs are becoming key components for various high efficiency medium to high voltage power applications due to their relatively low switching losses [22–24]. The SG structure serves as a vertical field plate which optimizes the electric field distribution of the drift region under the instruction of RESURF theory [25]. The grounded SG electrode isolates the control gate from the drift region and the drain electrode, which results in a drastic decrease in the C_{gd} [26–28]. Hence, the Q_{gd} is reduced and better switching performance is assured. Conventional SGT MOSFETs (CSGT-MOSFET) can reduce C_{gd} and Q_{gd} to some extent [29, 30]. But in fact, it is far from bringing the

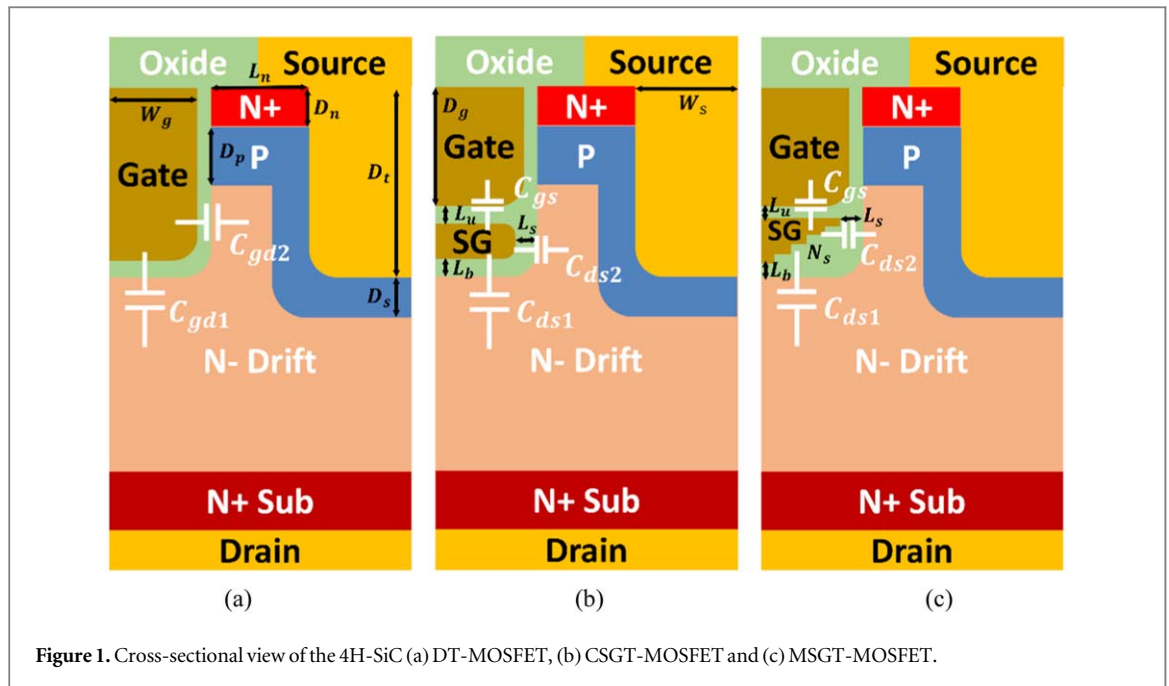


Figure 1. Cross-sectional view of the 4H-SiC (a) DT-MOSFET, (b) CSGT-MOSFET and (c) MSGT-MOSFET.

advantages of SG to full play. Besides, it makes an unsatisfactory compromise between static performance and switching losses.

This paper proposes a novel 4H-SiC Multiple Stepped SGT MOSFET (MSGT-MOSFET). In the MSGT-MOSFET, the SG structure is designed into a multi-step shape, which can achieve ultralow C_{gd} and Q_{gd} . And it achieves low values for the high frequency figure of merit, defined as $[R_{on} \times C_{gd}]$ and $[R_{on} \times Q_{gd}]$. The SG structure was optimized by Sentaurus TCAD simulation, and the number of steps was also optimized. Moreover, the switching loss of the DT-MOSFET, CSGT-MOSFET and MSGT-MOSFET is discussed in this paper.

2. Device structure and mechanism

Figure 1 shows the cross-sectional cell view of the 4H-SiC DT-MOSFET, CSGT-MOSFET and MSGT-MOSFET. In the three SiC MOSFETs under study, a grounded P-shield region is employed to protect the gate oxide from the high electric field. The gate and source double trench technology could reduce the trench mesa without much reliance on special processes and enhance its performance. The three SiC MOSFETs under study are rated for 1.2 kV and have the same cell pitch for a fair comparison. The cell's detailed parameters are listed in table 1. For the CSGT-MOSFET, the L_u , L_s and L_b are the distance from the SG to the gate, the side wall of the oxide trench and the oxide bottom of the trench, respectively. And the initial value of all three is set to 0.05 μm . As for the MSGT-MOSFET, the N_s is the number of steps in the SG structure. The width and height of each step are consistent, which can be calculated by the L_u , L_s , L_b and N_s .

Figure 1 also illustrates the C_{gd} distribution of the three SiC MOSFETs. In figure 1(a), the C_{gd} of DT-MOSFET can be demonstrated as $C_{gd} = C_{gd1} + C_{gd2}$. For the CSGT-MOSFET in figure 1(b), the SG acts as a shielding region between the gate and drain, and the C_{gd} is $C_{gd} = (C_{gs}^{-1} + (C_{ds1} + C_{ds2})^{-1})^{-1}$ [3, 31]. As for the MSGT-MOSFET in figure 1(c), the composition of C_{gd} is the same as that of CSGT-MOSFET. But the only difference is that C_{ds1} and C_{ds2} change dynamically with the number of steps in the SG structure.

In this paper, Sentaurus TCAD tools are used to perform the device simulations and the compact model simulations. Standard SiC physical models are used in the simulation, including Fermi statistics, Shockley-Read-Hall and Auger recombination, Okuto and GradQuasiFermi avalanche, incomplete dopant ionization, anisotropic material properties, and nonlocal tunneling [16, 32]. The bandgap models are OldSlotboom and NoFermi. Mobility models with doping dependence, high field saturation, and Enormal (IALMob) are also taken into consideration. The fixed charge concentration along the SiC/SiO₂ interface is $1 \times 10^{11} \text{ cm}^{-2}$ [33]. Other parameters of the material and models are adapted according to calibrated work in [16, 32, 34]. Besides, we also calibrated with the [4] as shown in figure 2. From this figure, the IV curves calibrated according to the structural simulation of [4] perfectly fit the data in the literature. It can also be found that the current of our proposed CSGT-MOSFET at $V_g = 10 \text{ V}$ is much higher than that of [4]. It should be noted that although the

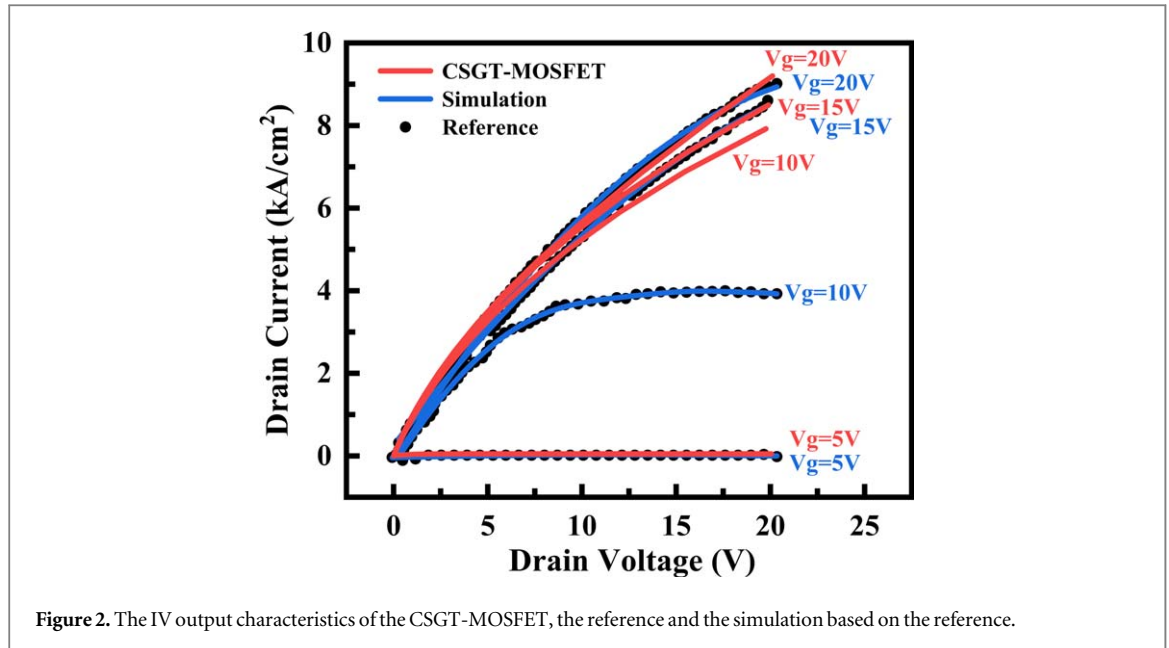


Figure 2. The IV output characteristics of the CSGT-MOSFET, the reference and the simulation based on the reference.

Table 1. Simulation parameters of 4H-SiC MOSFET structure.

Symbol	Structure parameter	Value	Unit
N_s	Substrate doping concentration	1.0×10^{19}	cm^{-3}
T_d	Drift thickness	10.0	μm
N_d	Drift doping concentration	8.0×10^{15}	cm^{-3}
W_g	Gate trench half width	0.5	μm
W_s	Source trench half width	0.3	μm
D_t	Trench depth	1.5	μm
D_g	Gate depth	1.0	μm
N_n	N+ doping concentration	1.0×10^{19}	cm^{-3}
L_n	N+ length	0.6	μm
D_n	N+ depth	0.3	μm
N_p	P-well doping concentration	1.0×10^{17}	cm^{-3}
D_p	P-well depth	0.5	μm
D_s	P-shield depth	0.3	μm
T_o	Gate oxide thickness	0.05	μm
W_c	Cell pitch half width	1.4	μm

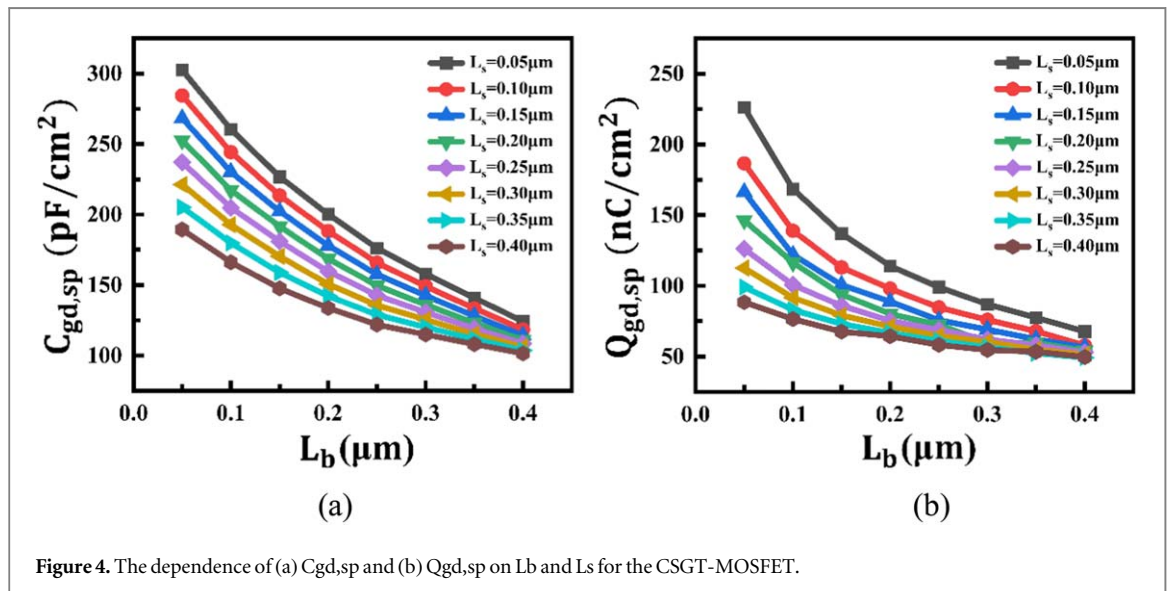
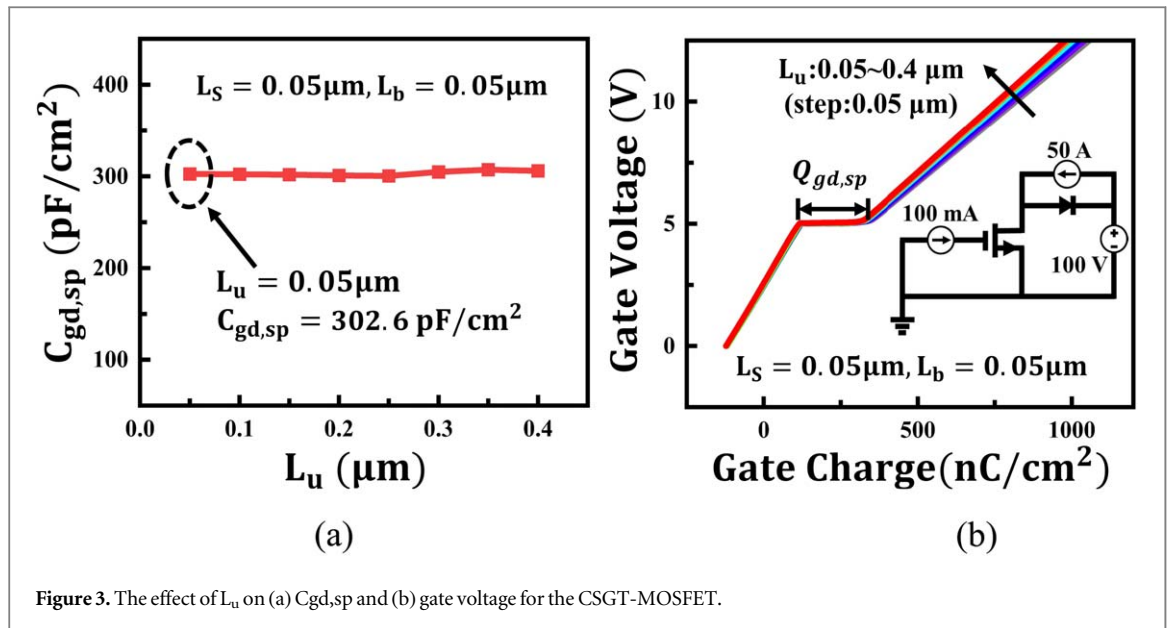
calibration procedure was carried out, the simulation results are not fully representative of the actual results due to the influence of simulation accuracy and model bias. Therefore, it could be taken as a more general case study.

3. Simulation results and discussion

In order to optimize the HF-FOM [$R_{\text{on}} \times C_{\text{gd}}$] and [$R_{\text{on}} \times Q_{\text{gd}}$] of the proposed MSGT-MOSFET, it is necessary to first optimize L_u , L_s and L_b of the SG structure in the CSGT-MOSFET, and then bring the optimal values of the three into the SG of the MSGT-MOSFET. Finally, the step number N_s of SG is optimized to obtain the device with the best performance.

Figure 3 shows the influence of L_u on C_{gd} and Q_{gd} . And the C_{gd} is extracting at $V_{\text{ds}} = 800 \text{ V}$, $V_{\text{gs}} = 0 \text{ V}$ and $f = 1 \text{ Mhz}$. As L_u increases from $0.05 \mu\text{m}$ to $0.4 \mu\text{m}$, C_{gd} and Q_{gd} remain basically unchanged, which indicates that L_u has little effect on the high frequency performance of the device. This is also verified in [3, 31, 35], since L_u mainly affects the gate-to-source capacitance and has little effect on the gate-to-drain capacitance, and thus has little effect on Q_{gd} . To increase the comparability of the CSGT-MOSFET and the DT-MOSFET, as well as improve the flexibility of the L_b optimization, L_u was set to $0.05 \mu\text{m}$ for subsequent optimization.

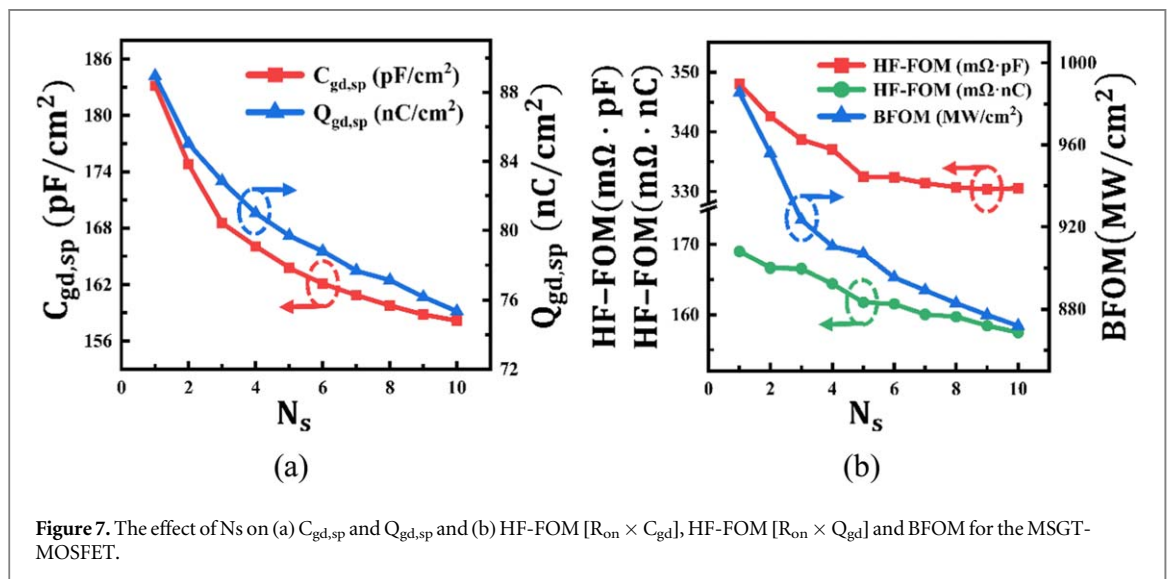
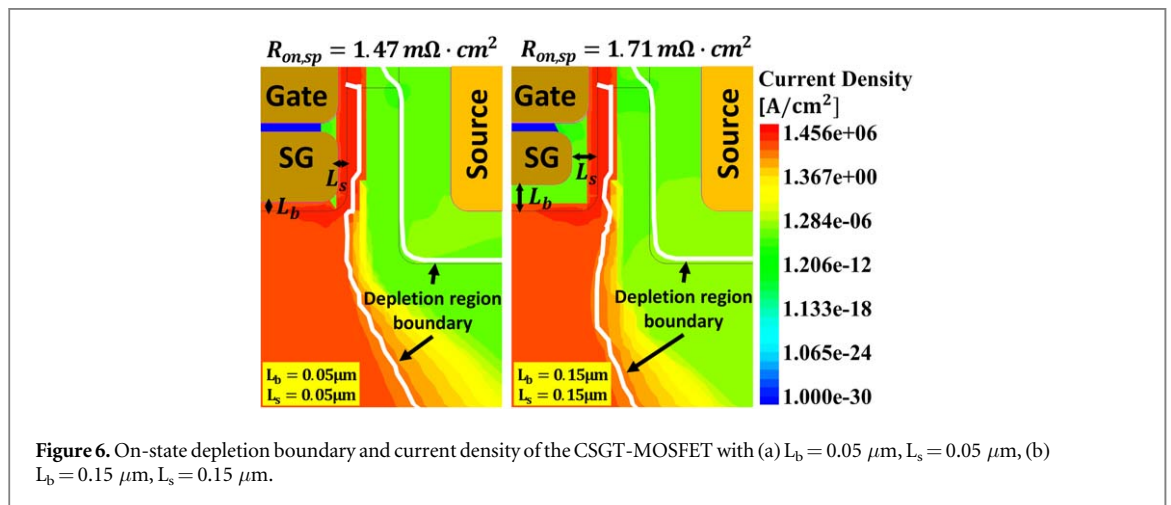
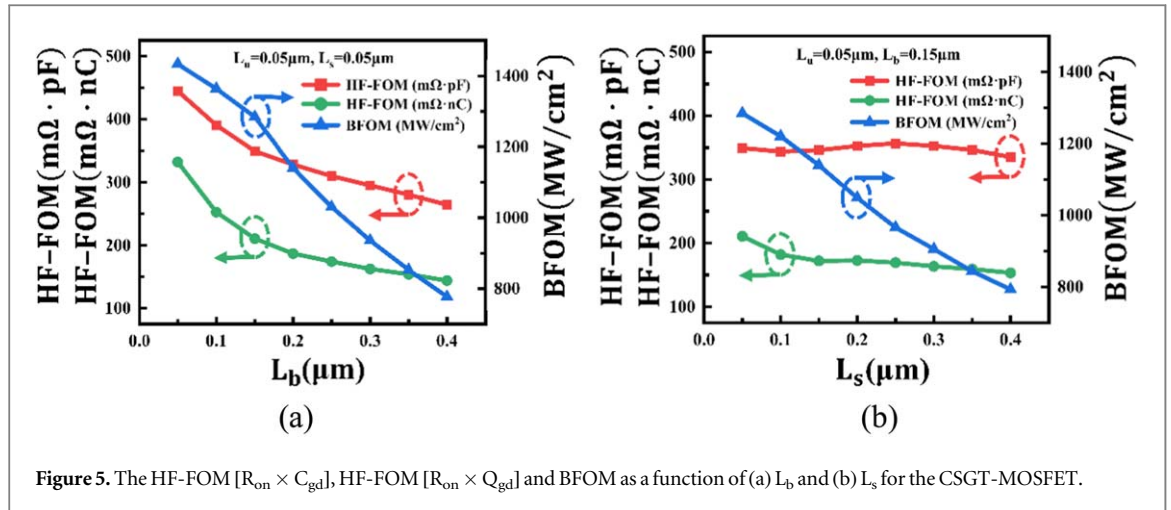
Figure 4(a) shows the dependences of C_{gd} on L_b and L_s for the CSGT-MOSFET. The C_{gd} slowly decreases with the increase in L_b and L_s , the reason is that the thickness of the oxide layer increases, and both the flat plate capacitance C_{ds1} and C_{ds2} decrease, resulting in a reduction of the total gate-to-drain capacitance. The decrease



of C_{gd} in figure 4(a) is consistent with the literature [3, 23]. Due to the decrease in C_{gd} , the device's turn-on speed increases; thus, its Miller platform will become shorter, eventually leading to the reduction of Q_{gd} . And this is the reason why Q_{gd} also decreases with the increase of L_b and L_s in figure 4(b).

Figure 5 shows the relationship between HF-FOM [$R_{on} \times C_{gd}$], HF-FOM [$R_{on} \times Q_{gd}$] and Baliga's figure of merit (BFOM [$BV^2/R_{on,sp}$]) [36, 37] at different L_b and L_s , respectively. In figure 5(a), when L_s is set to $0.05 \mu m$, both the HF-FOM and BFOM decrease as L_b increases. And when L_b is $0.15 \mu m$, there is only a slight decrease in HF-FOM with the increase of L_s , and the overall change is not significant; however, BFOM will continue to decrease with increasing L_s , as shown in figure 5(b). Therefore, in order to determine the optimal parameters of the SG structure, the HF-FOM and BFOM of the device need a compromise. Because with the increase of L_b and L_s , the oxide layer at the bottom and side of the SG structure becomes thicker, which will strengthen the depletion region and narrow the current path, leading to an increase in R_{on} . This is confirmed by the current distribution of the device in the on-state in figure 6. When $L_b = 0.15 \mu m$ and $L_s = 0.15 \mu m$ in figure 6(b), the on-resistance of the CSGT-MOSFET is 16.3% (from $1.47 m\Omega \cdot cm^2$ to $1.71 m\Omega \cdot cm^2$) larger than the initial value ($L_b = 0.05 \mu m$ and $L_s = 0.05 \mu m$). By fully considering the high frequency characteristics and low frequency characteristics of the CSGT-MOSFET, the BFOM is still maintained at a high level while ensuring a low value of HF-FOM. Finally, the specific parameters of the SG structure were determined with $L_u = 0.05 \mu m$, $L_b = 0.15 \mu m$ and $L_s = 0.15 \mu m$.

The thickness of the oxide layer on the top, bottom and side walls of the SG structure of the proposed MSGT-MOSFET is determined, and the remaining SG structure is constructed in a multiple stepped shape. For a



determined number of steps N_s , the height and width of the steps are divided equally. Increase N_s from 1 to 10 and observe its effect on C_{gd} and Q_{gd} , as shown in figure 7. An increase in N_s will lead to a decrease in C_{ds1} and C_{ds2} , which in turn decreases C_{gd} and Q_{gd} . From the two slowly falling curves in figure 7(a), we can deduce that when N_s is infinite, the multiple stepped SG structure becomes triangular, and the capacitance and gate charge of the device could reach the minimum limit value at this time. However, etching a perfect triangle in a one-

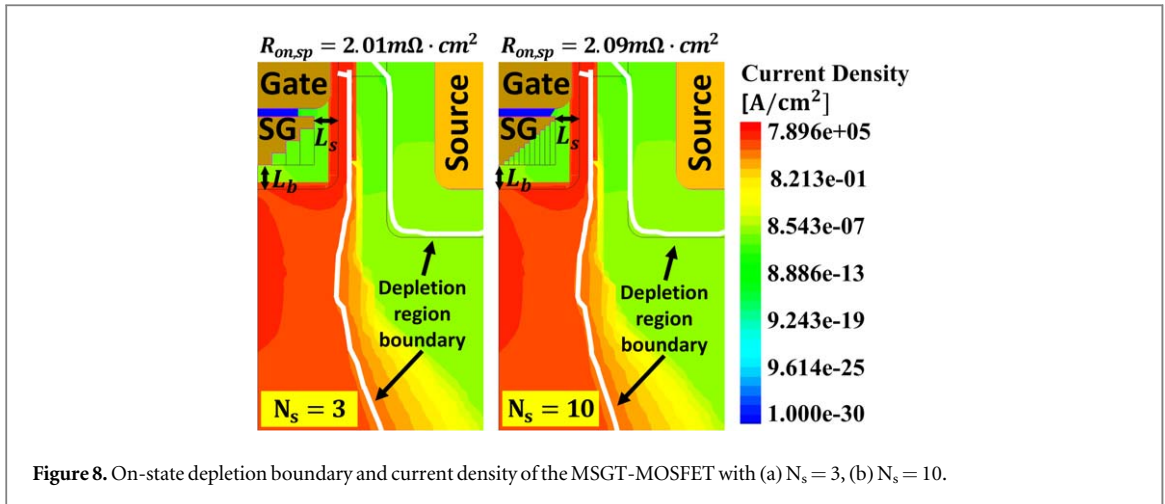


Figure 8. On-state depletion boundary and current density of the MSGT-MOSFET with (a) $N_s = 3$, (b) $N_s = 10$.

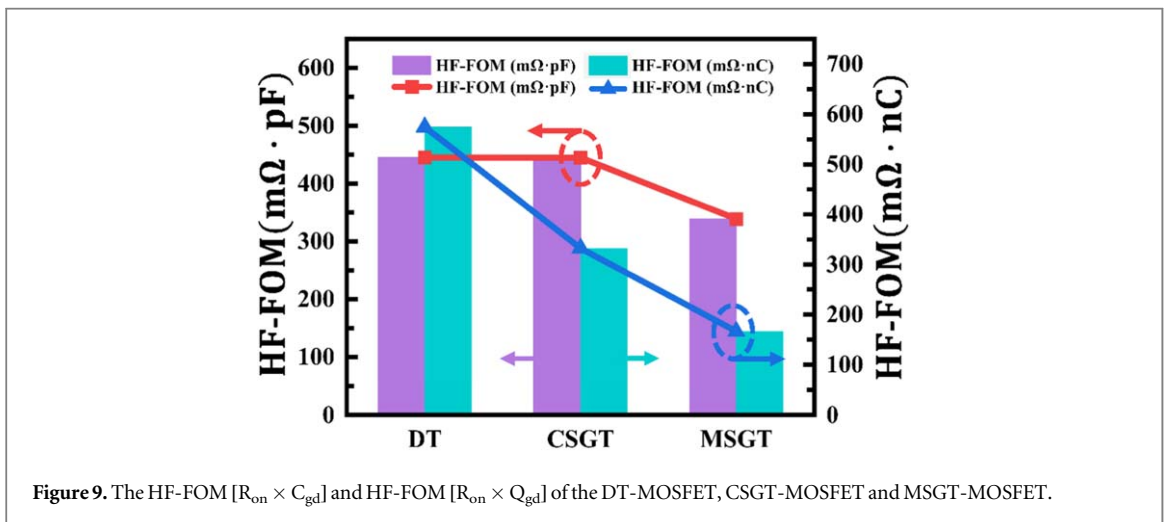


Figure 9. The HF-FOM $[R_{on} \times C_{gd}]$ and HF-FOM $[R_{on} \times Q_{gd}]$ of the DT-MOSFET, CSGT-MOSFET and MSGT-MOSFET.

micron-wide trench is a great challenge for the current manufacturing process. By calculation, the curves of HF-FOM and BFOM of the MSGT-MOSFET with N_s are shown in figure 7(b). Unlike the slight decrease in figure 5(b), the magnitude of the HF-FOM decrease with N_s is larger because both the C_{gd} and Q_{gd} decrease significantly, while the increase in on-state resistance R_{on} is slight. It can also be found from this figure that the decline of both HF-FOM and BFOM becomes slower when N_s is greater than 3, from which it can also be inferred that $N_s = 3$ is a better result. From figure 8, it can be found that the current paths of $N_s = 3$ and $N_s = 10$ are basically the same, and the R_{on} of $N_s = 10$ is only increased by 4% (from $2.01 \text{ m}\Omega \cdot \text{cm}^2$ to $2.09 \text{ m}\Omega \cdot \text{cm}^2$).

To obtain the optimal device performance, a compromise between the high and low frequency characteristics of the MSGT-MOSFET is needed again. On the other hand, as the number of steps of the device increases with N_s , the width and height of each step of the device become narrower, which requires higher precision in the fabrication process. Besides, the formation of each step requires at least one polysilicon etch-back and one oxide layer etch-back. Therefore, the more steps there are, the more complex the manufacturing process will be, and its cost will increase dramatically. After comprehensive consideration, $N_s = 3$ is the optimal result, where the HF-FOM of the MSGT-MOSFET is lower and the BFOM is higher, while the manufacturing process is less complicated and the cost is relatively low. Once N_s is determined, since the height and width of each step are equal, the specific structure of the multiple stepped split gate structure can be obtained by a simple calculation. And the MSGT-MOSFET studied in subsequent simulations are all 3-step SGT-MOSFET.

Figure 9 shows the comparison of the HF-FOM $[R_{on} \times C_{gd}]$ and $[R_{on} \times Q_{gd}]$ for the DT-MOSFET, CSGT-MOSFET and MSGT-MOSFET. The proposed MSGT-MOSFET has the best high frequency characteristics among the three devices. And the HF-FOM $[R_{on} \times C_{gd}]$ for the MSGT-MOSFET is 23.9% (from $445.29 \text{ m}\Omega \cdot \text{pF}$ and $444.82 \text{ m}\Omega \cdot \text{pF}$ to $338.73 \text{ m}\Omega \cdot \text{pF}$) lower than that of both the DT-MOSFET and CSGT-MOSFET. The calculated HF-FOM $[R_{on} \times Q_{gd}]$ of the MSGT-MOSFET is 71% (from $574.68 \text{ m}\Omega \cdot \text{nC}$ to $166.55 \text{ m}\Omega \cdot \text{nC}$) and 50% (from $332.35 \text{ m}\Omega \cdot \text{nC}$ to $166.55 \text{ m}\Omega \cdot \text{nC}$) lower than that of the DT-MOSFET and CSGT-MOSFET, respectively.

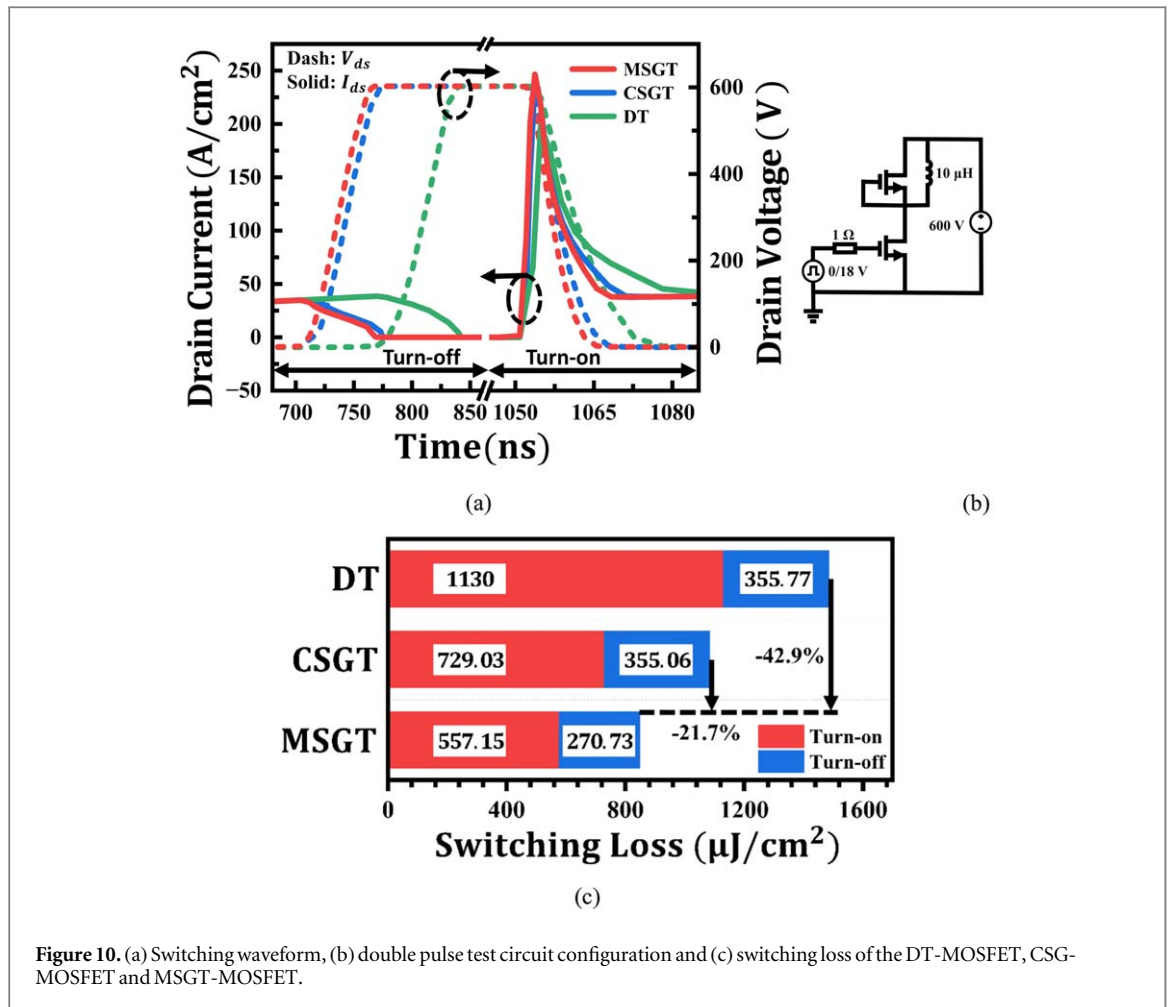
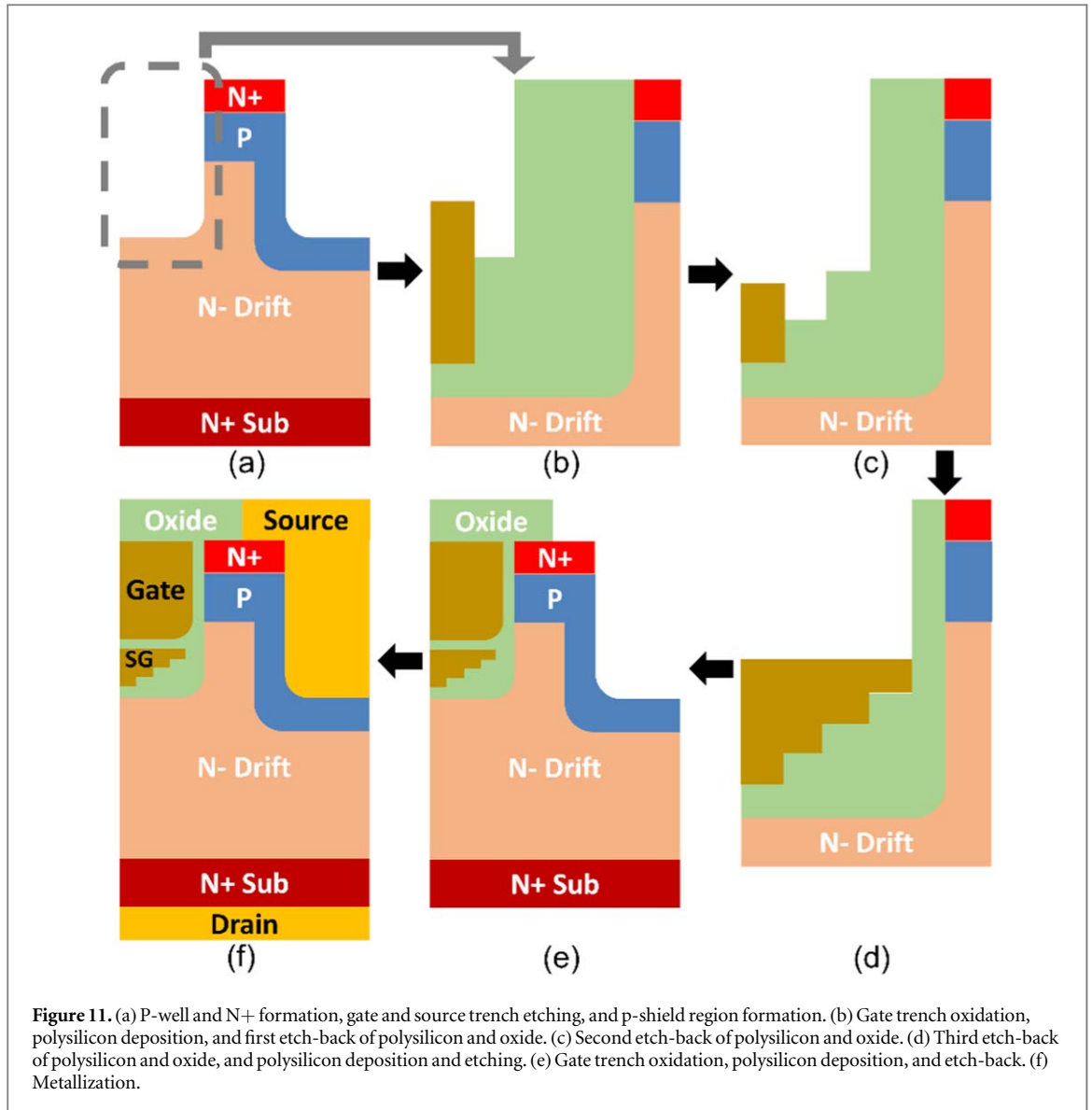


Figure 10. (a) Switching waveform, (b) double pulse test circuit configuration and (c) switching loss of the DT-MOSFET, CSGT-MOSFET and MSGT-MOSFET.

The switching waveforms of the three 4H-SiC MOSFETs are further simulated, as shown in figure 10(a). There is a current spike when the device is turned on due to the reverse recovery current. Both the turn-on time and turn-off time of the MSGT-MOSFET are shorter than the DT-MOSFET and CSGT-MOSFET. And the switching loss of the proposed MSGT-MOSFET is greatly reduced due to the smaller C_{gd} and Q_{gd} . As shown in figure 10(c), the MSGT-MOSFET realizes a 42.9% (from $1485.77 \mu J/cm^2$ to $847.88 \mu J/cm^2$) and 21.7% (from $1084.09 \mu J/cm^2$ to $847.88 \mu J/cm^2$) reduction in the switching loss compared with the DT-MOSFET and CSGT-MOSFET, indicating the great superiority to enhance the system frequency in power-conversion applications. Table 2 summarizes the key parameters of the DT-MOSFET, CSGT-MOSFET and MSGT-MOSFET for a clear presentation.

Considering the feasibility of the proposed MSGT-MOSFET, one available fabrication process is given in figure 11. First, the P-well and N+ can be formed by implantation before trench etching, while the P-shield implantation under the source trench and the sidewall is carried out after source trench etching [see figure 11(a)]. Then, the fabrication of the split gate structure was started, which is the most challenging step of the manufacturing process. The oxide layer and polysilicon are deposited in the gate trench, and then the first etch-back of the polysilicon and the first etch-back of the oxide layer are carried out successively to form the first step [see figure 11(b)]. Repeat the previous step for the second etch-back of the polysilicon and the second etch-back of the oxide layer to form the second step [see figure 11(c)]. Repeat the previous step again for the third etch-back of the polysilicon and oxide layer, and then polysilicon deposition and etch-back to form a 3-step split gate structure [see figure 11(d)]. After the split gate structure is fabricated, the remaining step is compatible with that of the double trench MOSFET. Gate oxidation, polysilicon deposition, and polysilicon etch-back are performed [see figure 11(e)]. Finally, the substrate is thinned and metallized to form the gate, source and drain [see figure 11(f)].

**Table 2.** Performance comparison.

Parameter	DT	CSGT	MSGT	Unit
V_{th}	4.86	4.86	4.88	V
$R_{on,sp}$	1.47	1.47	2.01	$m\Omega \cdot cm^2$
BV	1403.68	1401.38	1392.37	V
$C_{gd,sp}$	302.92	302.6	168.52	$pF \cdot cm^{-2}$
$Q_{gd,sp}$	390.94	226.09	82.86	$nC \cdot cm^{-2}$
$BFOM$	1340.35	1335.96	964.52	$MW \cdot cm^{-2}$
$HF-FOM [R_{on} \times C_{gd}]$	445.29	444.82	338.73	$m\Omega \cdot pF$
$HF-FOM [R_{on} \times Q_{gd}]$	574.68	332.35	166.55	$m\Omega \cdot nC$
E_{on}	1130	729.03	557.15	$\mu J \cdot cm^{-2}$
E_{off}	355.77	355.06	270.73	$\mu J \cdot cm^{-2}$
E_{tot}	1485.77	1084.09	847.88	$\mu J \cdot cm^{-2}$

4. Conclusion

A novel 4H-SiC multiple stepped SGT MOSFET is proposed in this paper. The thickness of the oxide layer at the top, bottom and side of the SG structure and the number of steps were optimized using Sentaurus TCAD

simulation. And the optimal structural parameters were finally obtained: $L_u = 0.05 \mu\text{m}$, $L_b = 0.15 \mu\text{m}$, $L_s = 0.15 \mu\text{m}$ and $N_s = 3$. The proposed MSGT-MOSFET has reduced HF-FOM [$R_{\text{on}} \times C_{\text{gd}}$] by 23.9%, and HF-FOM [$R_{\text{on}} \times Q_{\text{gd}}$] by 71% and 50% compared with that of the DT-MOSFET and CSGT-MOSFET, respectively due to the significantly decreased C_{gd} and Q_{gd} . Furthermore, the total switching losses including turn-on and turn-off processes are reduced by 42.9% and 21.7% compared with the DT-MOSFET and CSGT-MOSFET, which makes the dMSGT-MOSFET an excellent choice for high frequency and high power applications, such as on-board charger (OBC), power converters, inverters, etc.

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Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

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References

- [1] Kobayashi K, Nishiguchi T, Katoh S, Kawano T and Kawaguchi Y 2015 100 V class multiple stepped oxide field plate trench MOSFET (MSO-FP-MOSFET) aimed to ultimate structure realization *2015 IEEE 27th Int. Symp. on Power Semiconductor Devices & IC's (ISPSD) 2015 IEEE 27th Int. Symp. on Power Semiconductor Devices & IC's (ISPSD) (Hong Kong, China: IEEE)* 141–4
- [2] Jang S-L and Liu S-S 1998 An analytical surrounding gate MOSFET model *Solid-State Electronics* **42** 721–6
- [3] Luo X, Liao T, Wei J, Fang J, Yang F and Zhang B 2019 A novel 4H-SiC trench MOSFET with double shielding structures and ultralow gate-drain charge *J. Semicond.* **40** 052803
- [4] Tian K, Hallen A, Qi J, Ma S, Fei X, Zhang A and Liu W 2019 An Improved 4H-SiC Trench-Gate MOSFET With Low ON-Resistance and Switching Loss *IEEE Trans. Electron Devices* **66** 2307–13
- [5] Li P, Ma R, Shen J, Jing L, Guo J, Lin Z, Hu S, Shi C and Tang F 2022 A novel SiC MOSFET with a fully depleted p-base MOS-channel diode for enhanced third quadrant performance *IEEE Trans. Electron Devices* **69** 4438–43
- [6] Chiang T K 2005 A scaling theory for fully-depleted, surrounding-gate MOSFET's: including effective conducting path effect *Microelectron. Eng.* **77** 175–83
- [7] Lu H, Yu B and Taur Y 2008 A unified charge model for symmetric double-gate and surrounding-gate MOSFETs *Solid-State Electronics* **52** 67–72
- [8] Hu J-W, Jiang J-Y, Chen W-C, Huang C-F, Wu T-L, Lee K-Y and Tsui B-Y 2021 1100 V, 22.9 mΩcm² 4H-SiC RESURF lateral double-implanted MOSFET with trench isolation *IEEE Trans. Electron Devices* **68** 5009–13
- [9] Chaturvedi M, Dimitrijević S, Haasmann D, Moghadam H A, Pande P and Jadli U 2022 comparison of commercial planar and trench SiC MOSFETs by electrical characterization of performance-degrading near-interface traps *IEEE Trans. Electron Devices* **69** 6225–30
- [10] Su L, Wang C, Yang W and An J 2022 Study on failure mechanism caused by voltage leap of SGT-MOSFET during UIS testing *Microelectron. Reliab.* **139** 114822
- [11] Gonzalez J O, Wu R, Jahdi S and Alatise O 2020 Performance and reliability review of 650 V and 900 V silicon and SiC devices: MOSFETs, cascode JFETs and IGBTs *IEEE Trans. Ind. Electron.* **67** 7375–85
- [12] Fu H, Wei J, Wei Z, Liu S, Ni L, Yang Z and Sun W 2021 Quasisaturation effect and optimization for 4H-SiC Trench MOSFET With P+ shielding region *IEEE Trans. Electron Devices* **68** 4550–6
- [13] Zhou X, Pang H, Jia Y, Hu D, Wu Y, Tang Y, Xia T, Gong H and Zhao Y 2020 SiC double-trench MOSFETs with embedded MOS-channel diode *IEEE Trans. Electron Devices* **67** 582–7
- [14] Wei J, Liu S, Yang L, Tang L, Lou R, Li T, Fang J, Li S, Zhang C and Sun W 2019 Investigations on the degradations of double-trench SiC power MOSFETs under repetitive avalanche stress *IEEE Trans. Electron Devices* **66** 546–52
- [15] Wei J, Liu S, Tong J, Zhang X, Sun W and Huang A Q 2020 Understanding short-circuit failure mechanism of double-trench SiC power MOSFETs *IEEE Trans. Electron Devices* **67** 5593–9
- [16] Peng D and Feng Q 2022 A 4H-SiC double trench MOSFET with split gate and integrated MPS diode *Microelectron. J.* **128** 105553
- [17] Ghosh P, Haldar S, Gupta R S and Gupta M 2012 An analytical drain current model for dual material engineered cylindrical/surrounded gate MOSFET *Microelectron. J.* **43** 17–24
- [18] Verma J H K, Pratap Y, Haldar S, Gupta R S and Gupta M 2015 Capacitance modeling of gate material engineered cylindrical/surrounded gate MOSFETs for sensor applications *Superlattices Microstruct.* **88** 271–80
- [19] Deng S, Hossain Z and Taniguchi T 2017 Detailed study on dynamic characteristics of a high-performance SGT-MOSFET with under-the-trench floating P-pillar *IEEE Trans. Electron Devices* **64** 735–40
- [20] Han K, Baliga B J and Sung W 2017 Split-Gate 1.2-kV 4H-SiC MOSFET: Analysis and Experimental Validation *IEEE Electron Device Lett.* **38** 1437–40
- [21] Shen Z, Zhang F, Yan G, Wen Z, Zhao W, Wang L, Liu X, Sun G and Zeng Y 2020 High-frequency switching properties and low oxide electric field and energy loss in a reverse-channel 4H-SiC UMOSFET *IEEE Trans. Electron Devices* **67** 4046–53

- [22] Tian Y, Yang Z, Xu Z, Liu S, Sun W, Shi L, Zhu Y, Ye P and Zhou J 2018 Novel failure mechanism and improvement for split-gate trench MOSFET with large current under unclamped inductive switch stress *Superlattices Microstruct.* **116** 151–63
- [23] Wang Z, Qiao M, Li Z and Zhang B 2021 Mechanisms and characteristics of a low-loss split gate trench MOSFET with shield layer *Microelectron. J.* **118** 105310
- [24] Luo X, Huang J, Song X, Jiang Q, Wei J, Fang J and Yang F 2022 Novel SiC SBD-wall-integrated trench MOSFET with a semi-superjunction and split trench gate *Sci. China Inf. Sci.* **65** 169404
- [25] Appels J A and Vaes H M J 1979 High voltage thin layer devices (RESURF devices) 1979 *Int. Electron Devices Meeting 1979 Int. Electron Devices Meeting (IRE)* 238–41
- [26] Kaur H, Kabra S, Bindra S, Haldar S and Gupta R S 2007 Impact of graded channel (GC) design in fully depleted cylindrical/surrounding gate MOSFET (FD CGT/SGT) for improved short channel immunity and hot carrier reliability *Solid-State Electronics* **51** 398–404
- [27] Wu L, Liu Q, Deng G, Liu M, Song X, Zhang B, Qiu T and Wang J 2022 Improving dynamic performance for split-gate trench power MOSFETs using variable vertical doping profile *Micro and Nanostructures* **172** 207446
- [28] Wu W, Yin L, Zhu S, Tang P, Yang G, Liu S and Sun W 2022 Comprehensive investigation on electrical properties of split-gate trench power MOSFETs under mechanical strains *IEEE Trans. Electron Devices* **69** 1191–5
- [29] Kranti A, Haldar S and Gupta R S 2001 An accurate 2D analytical model for short channel thin[®]Im fully depleted cylindrical/surrounding gate (CGT/SGT) MOSFET *Microelectron. J.* **32** 305–13
- [30] Li P, Guo J, Lin Z, Hu S, Shi C and Tang F 2021 A novel approach to inactivate the body p-i-n diode of SiC MOSFET by using the normally-OFF JFET *IEEE Trans. Electron Devices* **68** 1784–90
- [31] Williams R K, Darwish M N, Blanchard R A, Siemieniec R, Rutter P and Kawaguchi Y 2017 The trench power MOSFET: Part I—history, technology, and prospects *IEEE Trans. Electron Devices* **64** 674–91
- [32] Guo J, Li P, Jiang J, Zeng W, Wang R, Wu H, Gan P, Lin Z, Hu S and Tang F 2023 A new 4H-SiC trench MOSFET with improved reverse conduction, breakdown, and switching characteristics *IEEE Trans. Electron Devices* **70** 172–7
- [33] Han Z et al 2021 A novel 4H-SiC trench MOSFET integrated with mesa-sidewall SBD *IEEE Trans. Electron Devices* **68** 192–6
- [34] Kang J, Liu Q, Luo H, Cao H, Zhang Z-H and Xin Z 2023 Investigation of off-state stress induced degradation of SiC MOSFETs under short-circuit condition *IEEE Trans. Ind. Electron.* **70** 5224–34
- [35] Fang D, Yang G, Qiao M, Xiao K, Yang X, Bian Z and Zhang B 2022 Split-gate trench metal-oxide-semiconductor field effect transistor with an inverted L-shaped source region *Microelectron. J.* **130** 105616
- [36] Shen Z et al 2018 Simulation of a short-channel 4H-SiC UMOSFET with buried p epilayer for low oxide electric field and switching loss 2018 *1st Workshop on Wide Bandgap Power Devices and Applications in Asia (WiPDA Asia) 2018 1st Workshop on Wide Bandgap Power Devices and Applications in Asia (WiPDA Asia) (Xi'an, China: IEEE)* 118–22
- [37] Kim D, Yun N, Jang S Y, Morgan A J and Sung W 2021 An inclusive structural analysis on the design of 1.2kV 4H-SiC planar MOSFETs *IEEE J. Electron Devices Soc.* **9** 804–12