# A Piezoelectric Energy-Harvesting Sensor Interface IC With High-Efficient Power Management and Readout Circuitry for Structural Health Monitoring

Dehong Wang, *Graduate Student Member, IEEE*, Mengyu Li, *Graduate Student Member, IEEE*, Siyao Cao, Yulu Zhang, Jiankao Pan, Kai Huang, *Member, IEEE*, Sijun Du, *Senior Member, IEEE*, Zhichao Tan, *Senior Member, IEEE*, Menglian Zhao, *Member, IEEE*, and Shuang Song, *Member, IEEE*

***Abstract*—A vibration piezoelectric energy-harvesting (PEH) sensor interface IC including high-efficiency power management and readout circuit for structural health monitoring is presented in this paper. The PEH interface consists of a parallel synchronized switched harvesting on inductor (SSHI) rectifier, and a novel duty cycle based maximum power point tracking (MPPT) circuit implemented with comparators and a switched capacitor. The comparators in both the SSHI and MPPT controllers are dynamically biased to provide fast response with low power. The switched capacitor based MPPT can tune the output voltage to suit the input effectively with a simple circuit structure. Moreover, the vibration frequency can be monitored to wake up the readout circuit when a certain threshold (20 Hz) is surpassed, indicating a possible catastrophic event. The readout circuit includes a low-power amplifier with dynamic bias, providing a programmable gain of 4/8/32/128 for the following 12-bit SAR ADC. The proposed system is implemented in a 55 nm standard CMOS technology. Experimental results show that a peak MPPT efficiency of 98.7% and up to 711% output power enhancement are achieved at 133 Hz resonance frequency. Moreover, the event driven wake-up of the readout circuit is successfully demonstrated. With a 11.3-bit ENOB achieved in the SAR ADC, the vibration frequency, temperature, and strain can be extracted from the proposed interface IC.**

***Index Terms*—Piezoelectric energy harvesting, SSHI rectifier, duty cycle based MPPT, high efficiency, dynamic bias, low power.**

## I. Introduction

BUILDINGSCAN accumulate damage because they are exposed to changing environmental conditions, e.g., seismic events, foundation settlement, heating, material aging and vibrations caused by urban activities, during the operational lifetime [1], [2], [3]. Compared with natural hazard-related vibration sources like seismic events, those more common in daily life mainly originate from urban activities, such as transportation [4], engineering construction [5], and industrial production [6]. These activities can generate vibrations with a frequency of around 20-200 Hz [4], [5], [6], which have impacts on buildings, ranging from structural safety hazards to accelerated material deterioration. As per [7], [8], and [9], such vibrations need to be monitored to evaluate the building structural health. Owing to the rapid development of the wireless sensor networks, monitoring structural health of buildings by recording vibration frequency, strain and temperature [10], [11] has been proven to be a useful approach to guarantee an adequate level of safety. Compared with labor-intensive regular maintenance, monitoring with wireless sensors provides a low-cost alternative with real-time operational capabilities. Therefore, sensors for structural monitoring of buildings attracted attention from both industry and academia [12], [13], [14]. In order to keep the sensor system economical, operations, e. g., changing the battery, other than installation should be minimized. Therefore, consuming low power and preferably harvesting energy from the environment is of significant importance for such sensor systems [15], [16], [17].

As shown in Fig. 1, a typical sensor node for structural health monitoring consists of a set of power management circuit, a sensor readout amplifier and ADC, together with a data interface and a RF link [18], [19], [20]. A customized ASIC including the power management and sensor readout can adapt to different sensing and energy harvesting modalities, providing a small form factor, while the RF link can be implemented by standard off-the-shelf components. In order to enhance the power efficiency to extend the battery lifetime, two techniques are usually implemented. First, energy harvesting from vibrations by a piezoelectric component can be useful, especially for sensor nodes deployed on bridges where vibrations are widely present. Second, an event-driven operation can minimize the RF power by only sending data sparsely and when an abnormality is detected.

Quantitatively, a piezoelectric vibration sensor, a resistive strain sensor, and a temperature sensor together with the readout usually consumes several $\mu$A to several 10s of $\mu$A [21]; the data interface and digital controller including threshold gating function consumes similar level of current; the radio

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Dehong Wang, Mengyu Li, Siyao Cao, Yulu Zhang, Kai Huang, Zhichao Tan, Menglian Zhao, and Shuang Song are with the Institute of VLSI Design, Zhejiang University, Hangzhou 310027, China (e-mail: shuangsonghz@zju.edu.cn).

Jiankao Pan is with Zhejiang Transsemi Microelectronics Company Ltd., Jiaxing 312099, China (e-mail: jiankao.pan@transsemi.com).

Sijun Du is with the Department of Microelectronics, Delft University of Technology, 2628 CD Delft, The Netherlands (e-mail: sijun.du@tudelft.nl).

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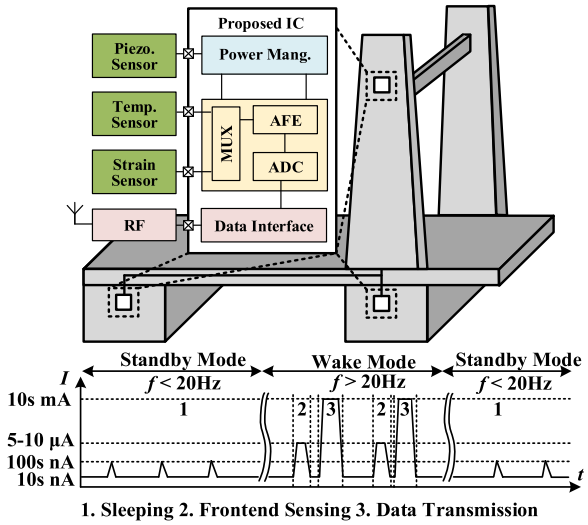



Fig. 1. (a) System schematic of a typical IoT sensor for structural monitoring of buildings. (b) Power consumption diagram of the proposed sensor interface.

link can consume a peak power of several 10s of mA, which may be active only once daily, making the energy negligible. From energy harvesting point of view, a medium size (10 cm X 2 cm) piezoelectric sheet working at a moderate vibration frequency of buildings (≈ 20 Hz) can provide a sustainable power of around 20 $\mu$W, which makes it possible to power the sensors together with its readout [22], [23], [24].

Indeed, existing piezoelectric based energy harvesting technique is helpful for sensor nodes in structural monitoring. These nodes are typically connected to a parallel synchronized switched harvesting on inductor (P-SSHI) rectifier, which shows a higher power efficiency and a lower operating voltage, compared to the synchronous electric charge extraction (SECE), whose extraction efficiency is independent of the variation of the loads [25]. One of the major challenges is to maintain a high efficiency with changing environments, varying harvestable energy levels, and load conditions [25]. Various maximal power point (MPP) techniques have been developed, and conventional techniques are based on either fractional open circuit voltage (FOCV) [26], [27], [28], [29] or perturb and observe (P&O) [30], [31], [32], [33]. The FOCV periodically disconnects the circuit from the harvester, resulting in a waste of energy. Moreover, the relationship between the open circuit voltage ($V_{OC}$) and the efficiency can change during operation, while timely adjustments are challenging. Besides, the P&O algorithm can continuously adjust the rectified output power without requiring prior knowledge of the system parameters, but at the cost of implementing a complex and power-hungry control scheme.

In [34], Yue et al. proposed a duty-cycle-based (DCB) MPPT technique that monitor the rectifier turn-off ($T_{OFF}$) duty cycle and adjusts the rectified voltage ($V_{REC}$) accordingly. The DCB algorithm operates continuous and automatic without requiring prior knowledge of the system parameters. However, its implementation requires a DC-DC converter, introducing additional power consumption and area overhead.

Meanwhile, the ultra-low power sensor nodes have already been developed. The work in [35] presents a resistive and capacitive sensor interface built-in around a successive approximation register (SAR) ADC. Based on this sensor structure, [36] improves energy efficiency further by exploiting automated optimization based on pre-experiment obtained behavior and power models and [37] increase the measurement range with a system-level ratio metric technique. However, the overall effective SNR achieved by these readout frontends is still limited to around 45 dB, primarily due to the absence of an amplifier between the sensor and the ADC for power minimization.

This paper proposed an event-driven sensor node IC powered by a vibrational piezoelectric harvester, designed for structural health monitoring applications to measure strain, temperature, and vibration. This chip includes an AC-DC rectifier with a power efficient compact DCB MPPT circuit using switched capacitor, achieving a peak MPPT efficiency of 98%. Thanks to the dynamic biased schemes used in the SSHI and MPPT controllers, the proposed system achieves a peak overall efficiency of 85.4%. This rectifier also works as a vibrational sensor to provide frequency information as the event-driven threshold. Moreover, two LDOs are integrated to power both the sensors and on-chip circuitry.

Additionally, a set of sensor interface circuitry supporting time-multiplexed strain and temperature sensor readout is designed. This frontend exploits a dynamic biasing low power amplifier and a 12-bit SAR ADC, consuming a quiescent current ($I_Q$) of only 4.6 $\mu$A when enabled continuously. Owing to the implementation of the dynamic biased scheme, the input range of the amplifier is increased 20X larger with the same $I_Q$. Moreover, in order to reduce the power consumption of the sensor interface circuit, the proposed IC operates in an event-driven way, i.e., the readout frontend is activated only when the vibration frequency is over 20 Hz, indicating structure abnormalities. This self-sustained sensor IC is suitable for long term monitoring applications.

The rest of the paper is organized as follows: Section II presents the system architecture of the sensor IC, including the energy harvester (EH) with power management circuitry together with MPPT and the sensor interface circuitry. Section III describes implementation of key circuit blocks, i.e., the SSHI rectifier, MPPT controller for energy harvesting and the dynamic biased low power amplifier, and SAR ADC for readout. Experimental results of the energy harvester, the sensor interface circuitry and the system are given in section IV and conclusions are drawn in Section V.

## II. Proposed Sensor Architecture

Fig. 2 shows the system architecture of the proposed sensor IC including the energy harvester and the sensor interface circuits. The EH and power management circuit are described in subsection A, while the power efficiency is analyzed in subsection B; the sensor interface and event-driven way of operation are described in subsections C and D, respectively.

### A. Energy Harvesting System Architecture

The energy harvesting system is shown in Fig. 3 (a), which consists of an SSHI rectifier followed by an active

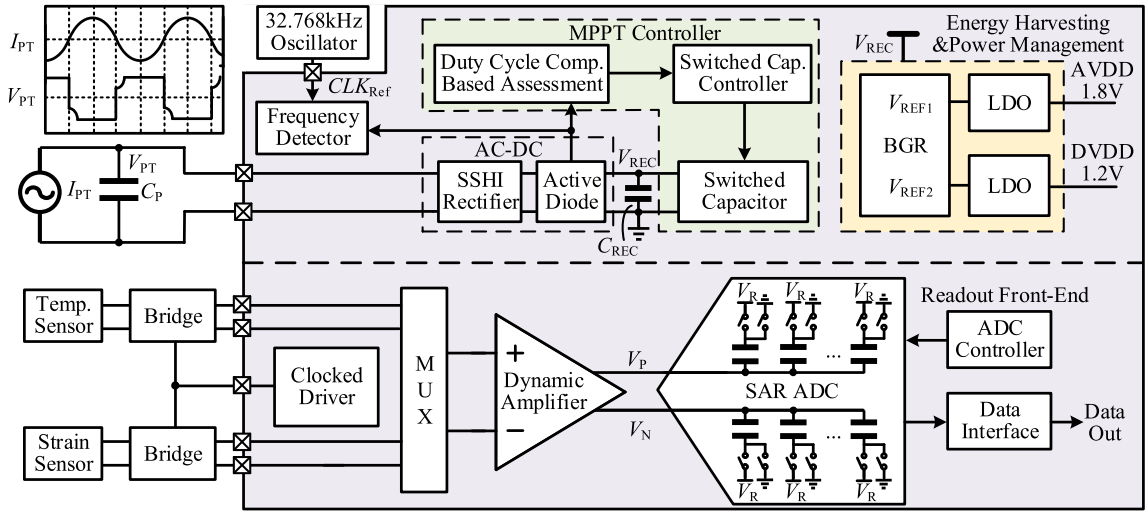



Fig. 2. System architecture of the proposed piezoelectric energy-harvesting sensor IC with high-efficient power management and readout circuitry.

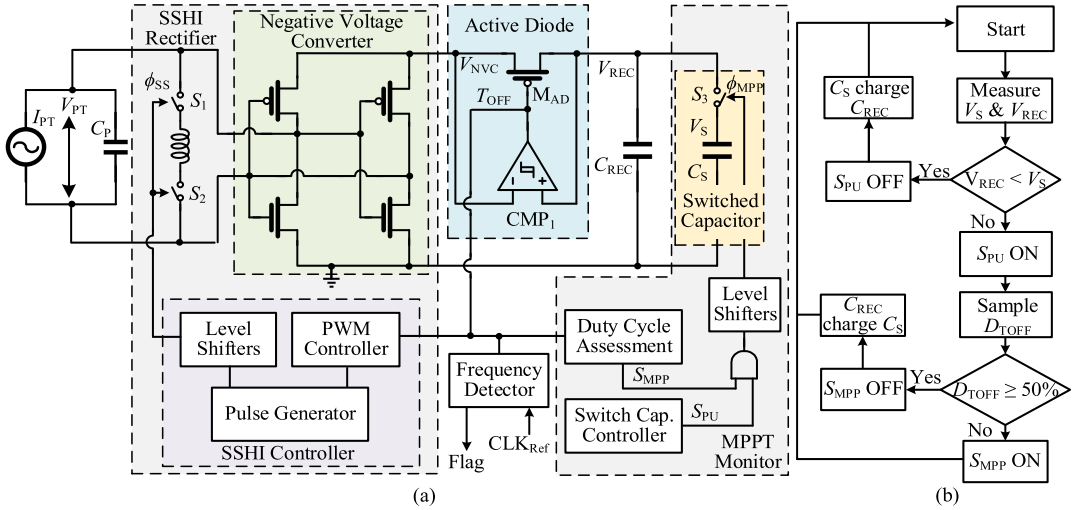



Fig. 3. (a) System architecture of an SSHI rectifier with DCB MPPT technique. (b) Working flow of the DCB MPPT logic.

diode, an MPPT circuit including a duty cycle detector and a switched capacitor for the MPPT implementation. Meanwhile, a frequency detector using an on-board crystal oscillator as the frequency reference is implemented to monitor the vibration frequency ($f_P$).

The SSHI rectifier contains a negative voltage converter (NVC) for negative-to-positive voltage conversion, an SSHI controller, two integrated power MOSFETs, and an off-chip inductor. As shown in Fig. 3 (a), the SSHI controller contains a PWM controller, a pulse generator, and level shifters. The chargers in the parasitic capacitor ($C_P$) passes through the rectifier in first. Then the energy is stored in the $C_{REC}$, making the voltage on the $C_{REC}$ increase, until both $C_P$ and $C_{REC}$ are fully charged. In order to minimize the reverse current flowing from the $C_{REC}$ to $C_P$, an active diode ($M_{AD}$) is implemented. It also provides the crossing time information for the MPPT controller, enabling duty cycle evaluation. This information is also used by the frequency detector to activate the readout circuitry.

A comparator $CMP_1$ is used to generate the turn off ($T_{OFF}$) signal to turn off the $M_{AD}$. When the $V_{REC}$ is higher than the $V_{NVC}$, the $M_{AD}$ is turned off. Meanwhile, the flipping moment ($T_{OFF}$) is given to the PWM controller to enable the inductor via $\Phi_{SS}$ signal and starts the resonance. Thus, the piezoelectric transducer voltage ($V_{PT}$) is flipped power efficiently. To achieve maximum flipping efficiency ($\eta_F$), the $\Phi_{SS}$ signal is determined by the optimum conduction time ($t_{SSHI}$) expressed in (1), where $L$ is the inductance of the inductor and $C_P$ is the parasitic capacitance of the piezoelectric transducer (PT).

$$t_{SSHI} = \pi \sqrt{LC_P} \tag{1}$$

It is worth noting that as shown in Fig. 4 (a), the flipping moment is essential for the efficiency of the rectifier. The light-grey areas in Fig. 4 (b) indicate the power loss due to the non-ideal flipping moment. Therefore, the $CMP_1$ should be made high-speed, while its always-on power consumption needs to be minimized. In order to achieve high speed with low power, a dynamically biased high-speed low-power comparator is introduced in Section III-A.

### B. Duty Cycle Based MPPT and Power Efficiency Analysis

As shown in Fig. 2, an AC-DC SSHI rectifier is usually followed by an MPPT circuit and output regulators [38]. The

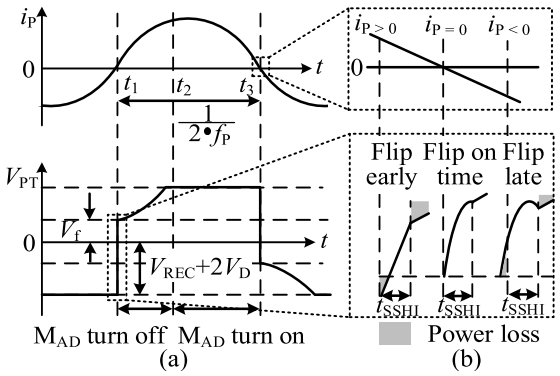



Fig. 4. Transducer current and simplified voltage waveforms.

overall end-to-end power conversion efficiency (PCE) $\eta_{E2E}$ of the EH interface can be expressed as (2), where $\eta_{REC}$, $\eta_{MPP}$, $\eta_{CONT}$, and $\eta_{REGU}$ are the efficiency of AC-DC rectifier, MPPT, control logic, and voltage regulator, respectively.

$$\eta_{E2E} = \eta_{REC}\eta_{MPP}\eta_{CONT}\eta_{REGU} \tag{2}$$

A PT can be modeled as a sinusoidal current source $i_P(t) = I_P \cdot \sin(2\pi f_P t)$ in parallel with an internal capacitor $C_P$, where $I_P$ is the amplitude and $f_P$ is the excitation frequency. Fig. 4 shows the $I_P$ and corresponding voltage waveform during operation. To simplify the calculation, the $\eta_F$ can be expressed as $V_f/(V_{REC}+2V_D)$, where $V_f$ is the flip voltage and $V_D$ is the forward voltage drop of an NVC. Then the PCE of an AC-DC ($\eta_{REC}$) can be derived as (3) [39].

$$\eta_{REC} = \frac{V_{REC}}{V_{REC} + 2V_D} \tag{3}$$

The efficiency of the MPPT circuit ($\eta_{MPP}$) achieves its maximum when the $V_{REC}$ equals to the $V_{MPP}$ [40], where $V_{MPP}$ is the optimal voltage of $V_{REC}$. It can be defined as $V_{OC}/(1\text{-}\eta_F)$ [40], where the $V_{OC}$ is the zero-to-peak open circuit voltage given by (4). The extracted power in a half-period is given by (5), where $Q_{waste} = V_{REC}\ (1\text{-}\eta_F)$ [41]. Making the derivative of (5) with $V_{REC}$ 0, the maximum power and corresponding $\eta_{MPP}$ can be derived by (6) and (7) [41].

$$V_{OC} = \frac{I_P}{2\pi f_P C_P} \tag{4}$$

$$P_{SSHI} = 2 f_P C_P V_{REC}\,[2V_{OC} - Q_{waste}] \tag{5}$$

$$P_{MPP} = \frac{2 C_P f_P V_{OC}^2}{1 - \eta_F} \tag{6}$$

$$\eta_{MPP} = \frac{P_{SSHI}}{P_{MPP}} = \frac{V_{REC}\left[2\frac{I_P}{2\pi f_P C_P} - Q_{waste}\right](1-\eta_F)}{\left(\frac{I_P}{2\pi f_P C_P}\right)^2} \tag{7}$$

Meanwhile, $Q_{waste}$ can also be expressed as $I_P$ (1-$\cos(\pi D_{TOFF})$) /$2\pi f_P C_P$, derived in [42], where the $D_{TOFF}$ is the off cycle of half vibration period. Then the $\eta_{MPP}$ can be rewritten as (8). Observably, the $\eta_{MPP}$ can theoretically achieve 100% when the $D_{TOFF}$ is 50%. In order to keep the $D_{TOFF}$ at around 50%, [42] uses a buck-boost DC-DC converter as the load of the rectifier to adaptively adjust the output current, and thus control the output voltage.

$$\eta_{MPP}(D_{TOFF}) = 1 - \cos^2(\pi D_{TOFF}) \tag{8}$$

However, this can lead to a high output voltage, requiring a BCD technology with a high voltage tolerance. In addition, the control logic for the converter can become complicated and power consuming. To improve its efficiency, the losses in a DC-DC converter is analyzed.

This efficiency $\eta_{DCDC}$ can be expressed by ($P_{IN}$-$P_{CL}$-$P_{SL}$-$P_{CON}$)/$P_{IN}$, where $P_{CL}$ in (9) and $P_{SL}$ in (10) are the conduction loss and the switching loss, respectively [43]. The $I_{ind}$, $R_{HS}$, $R_{LS}$, $t_{HS}$, $t_{LS}$, $C_{HS}$, $C_{LS}$, $\alpha$, $\beta$, $f_{SW}$, and $k$ are the inductor current, resistance of high-side switch and low side switch, on-time of the high-side switch and low-side switch, the capacitance of the high-side and low side switch, power consuming factor of the gate driver, the switching frequency, and the voltage conversion gain. In addition, the $P_{CON}$ stands for the power consumption of the controller circuity.

$$P_{CL} = \frac{1}{3} I_{ind}^2 (R_{HS} t_{HS} + R_{LS} t_{LS}) \tag{9}$$

$$P_{SL} = (\alpha C_{HS} + \beta C_{LS}) k^2 V_{IN}^2 f_{Sw} \tag{10}$$

It is worth noting that for an MPP tracking application for the targeted PTs, the current from $C_{REC}$ to $C_S$ is usually very small (10s-100s of $\mu$A). In this case, the $P_{SL}$ and $P_{CON}$ dominate. Especially the controller and clock generation circuits of the DC-DC converter can consume already tens of $\mu$A, which is at similar level of its load, need minimization. Additionally, to provide a proper voltage for the readout circuity, linear regulators i.e. LDOs are also required [38].

This paper proposed a switched capacitor (SC) based DC-DC conversion scheme for MPP tracking. As shown in the Fig. 3 (a), the aforementioned $T_{OFF}$ is measured by the duty cycle assessment module. When it is higher than 50%, the signal $S_{MPP}$ is generated to enable charging the $C_S$ by $C_{REC}$. While the $T_{OFF}$ falls below 50% again the $C_S$ is disconnected. During operation, the load draws current from $C_S$, making its voltage low than $V_S$. In this case, the MPP controller switches on $S_3$ to provide additional charge from the $C_S$. The SC circuit works in an event-driven style, which is discussed in details in Section III-B.

Its power efficiency $\eta_{SC}$ is ($P_{IN}$-$P_{CL}$-$P_{SL}$-$P_{CON}$)/$P_{IN}$, and conduction loss ($P_{CL}$) is given in (11), where the $Z_{SSL}$ and $Z_{FSL}$ are output impedance with slow switching limited and fast switching limited, respectively [44], [45].

$$P_{CL} = I_{out}^2 \left(Z_{SSL}^2 + Z_{FSL}^2\right)^{0.5} \tag{11}$$

Similar to the analysis for the DC-DC, $P_{CL}$ is very low thanks to the low energy level and the step-by-step operation of the capacitor array, which is also discussed in Section III-B. The switching loss ($P_{SL}$) is made negligible by exploiting the proposed event-driven operation. Moreover, the control circuits are digital except for low power voltage comparators within the switched capacitor controller, which are discussed in Section III-B. The quiescent current is made lower than 1 $\mu$A, making the $P_{CON}$ much lower than the one in the DC-DC converter-based solution.

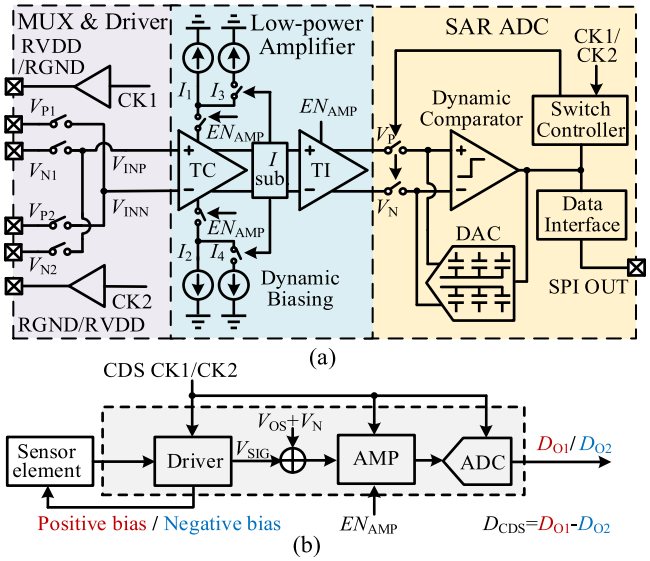



Fig. 5. (a) System architecture of the amplifier and SAR ADC (b) Operation with CDS.

### C. Frequency Detection Based Event Driven Operation

In order to minimize the power consumption, the proposed sensor interface is only turned on with event driven strategy on system level. Moreover, on the circuit level, it also exploits an event driven style dynamic biasing scheme.

A digital frequency detector is applied to wake up the sensor interface by comparing the $f_{TOFF}$ with the $f_{REF}$. If the building structure vibrates at a very low frequency ($f_{TOFF} < f_{REF}$), the sensor interface is kept off, with 10 nA level leakage current. Once the building structure vibrates at a higher frequency ($f_{TOFF} \geq f_{REF}$), an active Flag will wake up the sensor interface to detect the vibrating amplitude by measuring the strain of the PT by a Wilson-bridge resistive sensor [46]. The detailed implementation will be explained in Section III-C.

### D. Sensor Interface System Architecture

The typical sensor interface circuit connects the Wilson-bridge to the SAR ADC directly, consuming low power. However, the signal amplitude only occupies a small portion of the ADC dynamic range, limiting the effective resolution. On the other hand, solutions with a continuous-time frontend amplifier before the ADC may consume high power. Therefore, a dynamic architecture is implemented as shown in Fig. 5. The system includes a mux switch, a sensor driver, a low power amplifier, and an asynchronized SAR ADC.

The mux is used to select the input signals between the temperature sensor and the strain sensor, while the driver provides the bias voltage for Wheatstone bridges dynamically to save power. It can work in a two-phase mode, with positive and negative bias in each phase, providing a correlated double sampling (CDS) operation. The low-power amplifier consumes only 4.6 $\mu$A quiescent current if enabled continuously, and it can adapt to the input amplitude, exploiting a dynamic bias scheme. As shown in Fig. 5, the current $I_1$ and $I_2$ low quiescent biases used to maintain the operation of the amplifier, whereas the $I_3$ and $I_4$ can adapt to input signal by a current subtraction ($I$-sub block in Fig. 5) based amplitude detector.

The 12-bit asynchronous SAR ADC works at the sampling frequency ($f_S$) and consumes only dynamic power, which is followed by a serial data interface. Moreover, dynamic power-saving technique is also applied to the amplifier within the sensor interface system, providing enhanced resolution with minimum power. More details of implementation are given in section III-D.

## III. Circuit Implementation

The implementation of the self-startup SSHI rectifier, the MPPT controller, the system wake-up frequency detector and the dynamic biased sensor interface are presented in the section with transistor level details.

### A. SSHI Rectifier

As shown in Fig. 6 (a), there are two blocks in the proposed circuit around the rectifier: a dynamically biased low power comparator based active diode and an SSHI controller including a pulse generator and a level shifter.

*1) Low Power Comparator With Dynamic Bias:* The SSHI rectifier shown in Fig. 6 (a) is kept always on to provide the rectified voltage, with the comparator consuming the main quiescent current to provide the $T_{OFF}$ signal. Meanwhile, the delay of this comparator should be minimized to prevent the reversed current and thus guarantee the efficiency of the power stage. In order to have a fast comparator with minimum power, a dynamic biasing scheme is proposed to enhance the performance of the topology, as shown in Fig. 6 (b), which typically used in zero current sensing applications [41], [47].

The comparator consists of a 10 nA DC bias, a preamplifier, a dynamic biasing, and an output buffer. To prevent gate oxide breakdown due to abrupt change of voltage polarities, the sources of the $M_{P1}$ and $M_{P2}$ devices are used as inputs of the preamplifier within the proposed comparator. This amplifier is biased by a small DC current (10 nA) through the current mirror $M_{N1}$, $M_{N2}$, and $M_{N3}$ (1:1:1) to maintain operation. When the $V_{NVC}$ is much smaller than $V_{REC}$, the $V_{O1}$ is high and the $M_{P5}$ is switched off, keeping the amplifier in low-power mode. The dynamic biasing current enhancement is only enabled when the voltage $V_{NVC}$ and $V_{REC}$ are getting similar to each other, during operation of the rectifier.

When the $V_{NVC}$ increases, the $V_{O1}$ decreases, and moving towards the threshold of the $M_{P5}$. Meanwhile, an enhancement current mirror $M_{P4}$ and $M_{P3}$ (1:2) starts to increase the bias current the pre-amplifier. As the result, more current (60 nA) will flow into $M_{N2}$, $M_{N3}$, which makes the $V_{O1}$ drops sharply, enhancing the speed of the comparator. When the $V_{NVC}$ exceeds the $V_{REC}$, the current of $M_{P2}$ decreases due to the reduction of the $V_{SG,MP2}$. Meanwhile, the gate of transistor $M_{P5}$ goes towards $V_{GND}$, reducing the enhancing current to save power.

Similarly, when the $V_{NVC}$ crosses the $V_{REC}$ from the high to low, the $M_{P2}$ starts to turn on again, and the $V_{O1}$ begins to increase, enabling the enhancement when the two input voltages are similar. Fig. 6 (c) illustrates the relationship between the inputs and the bias current.

Compared to the topology in [48], the proposed topology is less vulnerable to PVT variations, because the on/off threshold

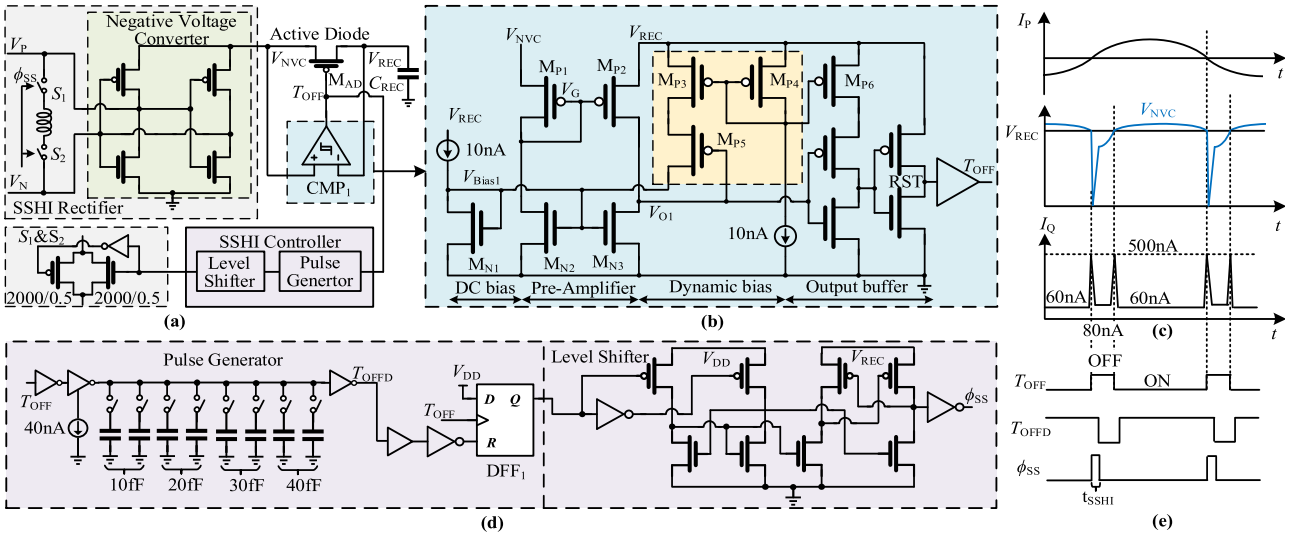



Fig. 6. Circuit diagram of the proposed SSHI rectifier and the low power comparator. (a) Scheme of the SSHI rectifier. (b) The circuit of the dynamic biased low power comparator. (c) Timing diagram and the power consumption of the comparator. (d) Scheme of the pulse generator and level shifter. (e) Timing diagram of the SSHI controller.

of $M_{P5}$ is based on a fixed bias current. Compared with the one-side enhanced topology for level-crossing ADCs [49], [50], the proposed topology features dynamic enhancement of speed on both positive and negative cross of the differential signal, suiting the application well. As the result, the simulated average quiescent current of the low power comparator is around 60 nA. While the peak current can be as high as 500 nA to provide sufficient speed. Comparing with a static biased (60 nA) comparator with the same topology, the latency time is shortened from 10 $\mu$s to 1 $\mu$s and the gain is two times larger.

*2) Synchronized Switched Harvesting on Inductor Controller:* The $T_{OFF}$ signal generated by the previous low power comparator is sent to the SSHI controller which contains a pulse generator and a level shifter, shown in fig. 6 (d). The pulse generator consists of a current biased inverter, a capacitor array, and relevant logic cells. In order to operate with different piezoelectric transducer and valid the MPPT operation with different $\eta_F$ of the SSHI rectifier, the delay time can be tuned by selecting capacitors.

The charges in the capacitor array are drained by the inverter with fixed-biasing current (40 nA). Once the voltage of the capacitor is approaching the threshold of the followed inverter, a delayed $T_{OFF}$ ($T_{OFFD}$) with $t_{SSHI}$ delayed is generated. The $T_{OFFD}$ will reset the $DFF_1$ resulting a low $\phi_{SS}$, switching on the $S_1/S_2$ for synchronization of the current and voltage. Meanwhile, this $T_{OFFD}$ is also monitored by the MPPT controller. The timing diagram of this controller is shown in fig. 6 (e).

### B. The Duty Cycle Based MPPT Controller

In order to boost the power efficiency, a DCB based MPPT technique is exploited. Fig. 7 (a) illustrates the circuit implementation of the duty cycle assessment circuit on the left and the switched capacitor controller on the right. The duty cycle of $D_{TOFF}$ is compared with 50% in time domain by using a 5 nA current source to charge either $C_H$ or $C_L$. Thus, the corresponding voltages $V_H$ and $V_L$ are compared by a high-speed low power comparator $CMP_2$, which generates a $S_{MPP}$ signal indicating the result of the evaluation. Meanwhile the $S_{MPP}$ is also used to generate the $RST_L$ signal to clear $C_L$, finishing the comparison. This signal is also fed to the switched capacitor controller.

Similar to the $CMP_1$ discussed in the previous section, the $CMP_2$ exploits also a dynamic biasing scheme to enhance the performance. As shown in Fig. 7 (b), the concept of $CMP_2$ is similar to the $CMP_1$, while the gates of the $M_{P1}$ and $M_{P2}$ devices are used as inputs of the preamplifier. This comparator is biased by a 10 nA current and can be enhanced by a 30 nA current source according to the input signal amplitude. The ratio of $M_{P3}/M_{P4}$ and $M_{N3}/M_{N4}$ is designed to be 1:2, 1:8, respectively. It is worth noting that the $CMP_2$ features a level-crossing ADC style operating [49], [50], namely, the $C_L$ capacitor is reset once the $V_L$ exceeds the $V_H$. Fig. 7 (d) shows the timing diagram and simulated power consumption.

The detailed DCB MPPT timing diagram is shown in Fig. 7 (e). During the start-up period, both the $V_{REC}$ and $V_S$ are low, the $C_{REC}$ capacitor obtains energy from the PT with a much higher $V_{NVC}$. Thus, the active diode is switched on, controlled by the $T_{OFFD}$ signal with a duty cycle much lower than 50%. In this case, through the D-flip-flops flowing the $CMP_1$, the capacitor array at the output is disconnected from the $C_{REC}$. Along with the increase of $V_{REC}$, the $D_{TOFFD}$ gradually exceed 50%. Then, the $S_{MPP}$ is turned on to enable the charge transfer from the $C_{RES}$ to $C_S$ in the next vibration period. Correspondingly, the $V_{REC}$ will slightly decrease and the $D_{TOFFD}$ will fall below 50% and the $S_{MPP}$ is turned off again, keeping the rectifier always at the maximum power efficiency. When there is too much energy from the PT, making the $C_S$ capacitor also fully charged, the $\phi_{MPP}$ will be kept on to short $C_S$ and $C_{REC}$.

Fig. 7 (c) shows the implementation of the comparator in the switched capacitor controller. An ultra-low power comparator $CMP_3$ with source input, to work reliably with changing input

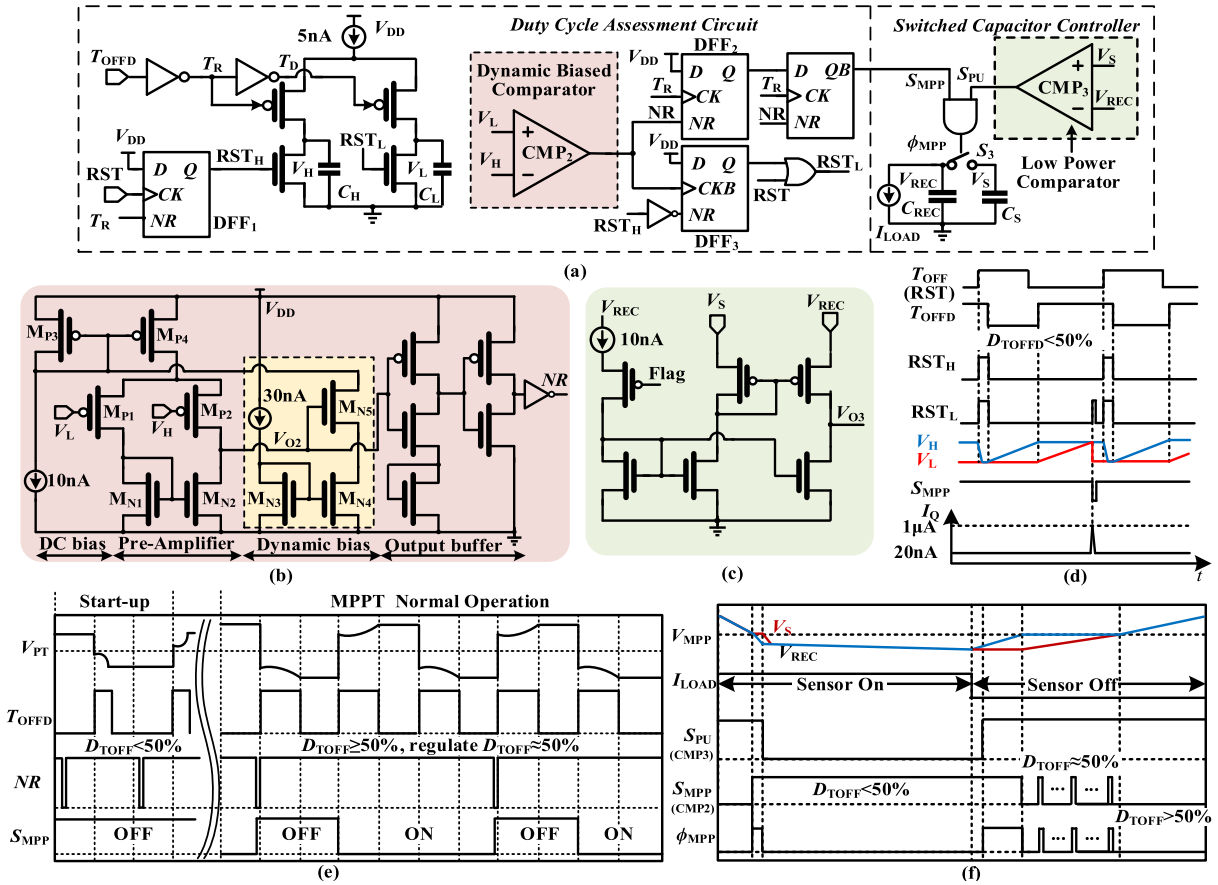



Fig. 7. (a) Circuit diagram of the proposed duty cycle assessment block and switched capacitor. (b) Scheme of the dynamic biased comparator. (c) Scheme of the ultra-low power comparator. (d) Timing diagram and power consumption of the $CMP_2$. (e) Timing diagram of the duty cycle assessment block. (f) Timing diagram of the switched capacitor controller.

polarity, is used to compare the voltages on the $C_S$ and $C_{REC}$, namely $V_S$ and $V_{REC}$, during the sensor readout enabling phase. Fig. 7 (f) shows the detailed timing diagram of the switched capacitor controller. The red line indicates the voltage $V_S$ and the blue line indicates the voltage $V_{REC}$. Assuming a scenario when $C$s is fully charged and 1the readout circuit is on, a high $I_{LOAD}$ making $V_{REC}$ gradually to drop below $V_{MPP}$ ($D_{TOFFD}$ < 50%). The $V_{MPP}$ is considered to be the optimum voltage at the rectifier output, which is a function of $\eta_F$ for an SSHI rectifier [32], [42]. Meanwhile, the switch $S_3$ is turned off by the duty cycle assessment block, disconnecting $C_{REC}$ with $C_S$. In order to exploit the energy stored in the $C_S$, the $CMP_3$ can short the $C_S$ and $C_{REC}$ again when the $V_{REC}$ is lower than $V_S$. When the readout circuit is off, the switch $S_3$ will be controlled by the duty cycle assessment block according to the $D_{TOFF}$ again as described previously.

If there is too much energy harvested from the PT, making the $C_S$ capacitor fully charged, the $\phi_{MPP}$ will be kept on to short $C_S$ and $C_{REC}$. In this case, the MPPT will stop and lead to a lower $\eta_{MPPT}$. It is worth noting that comparing with the $C_{REC}$, a much larger $C_S$ can extend the MPPT working period. However, such a large $C_S$ makes the $V_{REC}$ drops sharply. In the proposed design the $C_{REC}$ is equal to the $C_S$ for simplicity. To perfectly solve this issue, one of the effective solutions is to charge a capacitor array sequentially, which will increase the complexity of the control circuit.

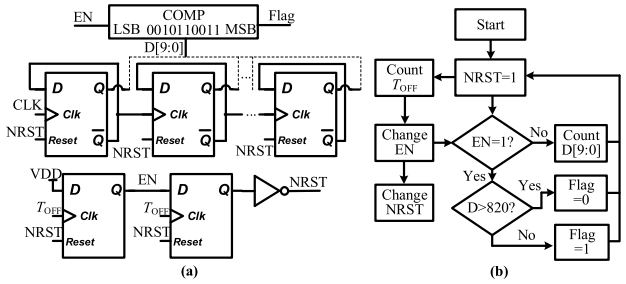



Fig. 8. (a) Implementation of the frequency detector; (b) the operation flowchart of the frequency detector.

## C. Frequency Detector

Fig. 8(a) shows the circuit implementation of the frequency detector. It consists of a 2-bits shift register, a 9-bits counter, and a digital comparator. The 2-bit shift register sense the $T_{OFF}$ as a clock and enable the 9-bits counter via signal EN. The clock of the counter is provided by an off-chip crystal oscillator with a working frequency at 32.768 kHz. It is worth noting that the vibration frequency is half of the frequency of $T_{OFF}$ ($f_{TOFF}$). Once the EN is off, the counter will stop counting and send its result to the digital comparator, which compares the result with a constant number 820, corresponding to a frequency of 40 Hz. Fig. 8 (b) shows the operation flowchart of the frequency detector. As the result, the $f_P$ exceeds the $f_C$, generating a Flag signal to indicate an abnormal event.

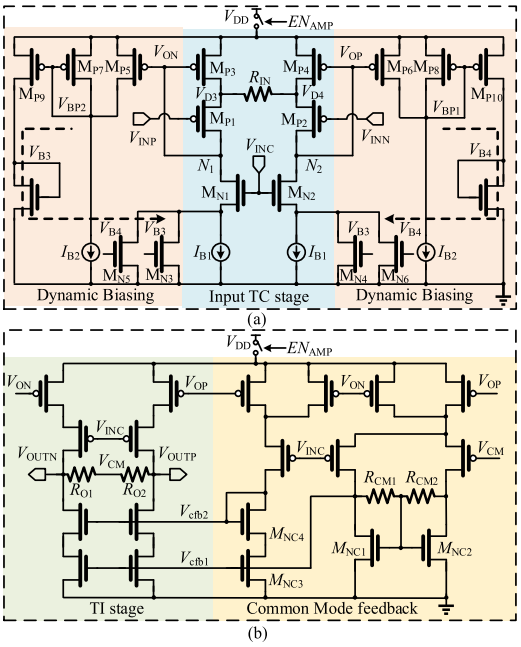


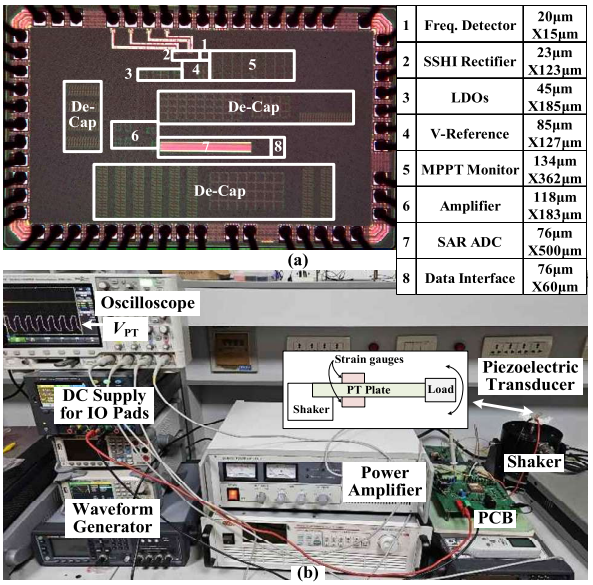

Fig. 9. Circuit diagram of (a) the transconductance stage and the dynamic bias and (b) the transimpedance stage and the common mode feedback.

### D. Low Power Amplifier and SAR ADC

Wheatstone bridge style sensors are usually used to measure strain and thus vibration amplitude resistively. Because of the small signal amplitude from the bridge, the effective resolution can be limited if the sensor is directly connected to the ADC. Therefore, a dynamically biased amplifier is implemented in this design, to increase the effective range of the ADC with minimum power penalty. Fig. 9 shows the proposed amplifier, including an input stage with dynamic bias (a) and an output stage with common feedback (b). It is worth noting that to achieve high accuracy with minimal consumption current, a resistive feedback amplifier is applied in the design.

The input stage employs a current feedback topology () [51], [52], where the $M_{P1}$ and $M_{P2}$ are the differential input transistors. The small signal input voltage is converted to a current through transistor $M_{P3}$ and $M_{P4}$, controlled by the voltage of high impedance node $N_1$ and $N_2$. There is a well-known trade-off between the supported input range ($V_{IN,MAX}$) and the input noise at the same current consumption, namely, a large resistor offers a large $V_{IN,MAX}$ but generates more noise [52], [53]. In this design, a small $R_{IN}$ (12k) and a low quiescent current (2 $\mu$A) is used in the input stage, supporting a $V_{IN,MAX}$ of around 20m$V_{PP}$.

The dynamic bias scheme can enhance the $V_{IN,MAX}$ without increasing the quiescent current. When the signal amplitude is small, the current in $M_{P3,4}$ ($M_{P5,6}$) are balanced, turning off $M_{P7}$ and $M_{P8}$. When the signal amplitude is large, the current either in $M_{P3}$ or $M_{P4}$ can decrease. Once either $I_{P3}$ or $I_{P4}$ is lower than a current threshold defined by the current in $I_{B2}$, $M_{P7}/M_{P8}$ is turned on, enabling the dynamic enhancement. The enhancing current is provided to the main branch through the arrows shown in Fig. 9 (a). As the result, a $V_{IN,MAX}$ of 400 mV can be generated with the same $I_Q$, showing an increase of 20X.




| | | |
|---|---|---|
| 1 | Freq. Detector | 20µm X15µm |
| 2 | SSHI Rectifier | 23µm X123µm |
| 3 | LDOs | 45µm X185µm |
| 4 | V-Reference | 85µm X127µm |
| 5 | MPPT Monitor | 134µm X362µm |
| 6 | Amplifier | 118µm X183µm |
| 7 | SAR ADC | 76µm X500µm |
| 8 | Data Interface | 76µm X60µm |

Fig. 10. (a) die micrograph of the fabricated sensor interface IC and (b) measurement setup.

The output stage basically mirrors the current in $M_{P3,4}$ with a current ratio of 2:1 to save power, generating a voltage gain of $R_O/2R_{IN}$. The common mode feedback (CMFB) consists of a differential input branch and a bias generating branch, both of which are biased by a scaled current of $M_{P3,4}$ to suit the dynamic bias scheme of the input stage. The gate bias voltage $V_{INC}$ is fixed at $V_{DD}/2$ and it is also used as the common mode reference voltage. The CMFB amplifier has transistor $M_{NC1}$, $M_{NC2}$ and resistor $R_{CM1,2}$ as the load, providing a suitable gain. The feedback voltage $V_{cfb1}$ together with voltage $V_{cfb2}$ from the bias generating branch stabilized the common mode voltage of the output stage accurately, during the operation of the dynamic bias scheme of the input stage.

In case of CDS operation at 100 Hz as shown in the top of Fig. 5 (b) with dynamic turning on/off by the $EN_{AMP}$, the quiescent power can be reduced to 0.6 $\mu$W.

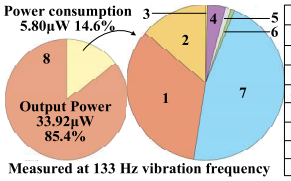
A 12bit asynchronized SAR ADC is implemented following the amplifier, with customized fringe capacitor-based array to digitize the signal. It samples usually at a speed of 100-10 kHz and only consumes dynamic power, which is less than 1 $\mu$W. The sensor interface circuit consumes a total quiescent power of 0.94 $\mu$W with 100 Hz CDS operation and it provides programmable gain of 4/8/32/128 with constant quiescent current, enhancing the overall effective SNR of the frontend system.

## IV. Implementation Results

The proposed sensor interface IC including the EH and the readout circuits is implemented in a standard 55 nm CMOS process. As shown in Fig. 10, it occupies an active area of 0.135 mm$^2$, where the MPPT controller with 5 nA current reference and 100 pF capacitance is relatively large. The chip is characterized with suitable measurements.

### A. Measurement of the Energy Harvester

A commercial PT S129-H5FR-1803YB (PPA-1021) is used in the measurement, with a parasitic capacitor of 22 nF and




| $i$ | Module | $I_i$ | $P_i$ | $P_i/P_{Total}$ |
|---|---|---|---|---|
| 1 | LDO1V8 | 590nA | 1.96μW | 33.80% |
| 2 | LDO1V2 | 450nA | 0.80μW | 13.80% |
| 3 | SSHI Controller | 11nA | 19nW | 0.33% |
| 4 | Switch Driver | 65nA | 0.21μW | 3.62% |
| 5 | Switched Capacitor | 37nA | 67nW | 1.16% |
| 6 | MPPT Controller | 24nA | 43nW | 0.74% |
| 7 | Voltage Reference | 820nA | 2.7μW | 46.55% |
| 8 | Output Loads | 10.3μA | 33.92μW | 85.4% |

Fig. 11. Power breakdown of the proposed AC-DC interface.

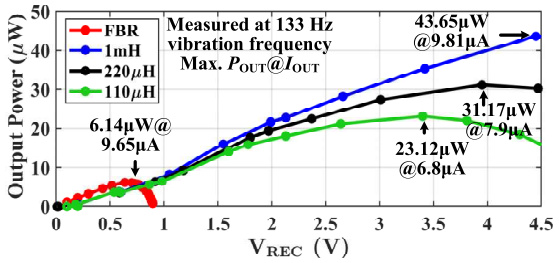



Fig. 12. Output power of NVC vs SSHI with different off-chip inductors.

a resonant frequency of 133 Hz. A set of PPA-9001 clamp kit is used to mount the PT with metal loads to increase the peak-to-peak displacement of the PT, as also been done in the measurement of other works [23], [54]. A shaker (SA-JZ010) is driven by 33600A waveform generator and SA-PA020 power amplifier is used for excitation. Three off-chip inductors with 110 $\mu$H, 220 $\mu$H, and 1 mH, are used to validate the performance of SSHI controller. Two 10 $\mu$F capacitors are used to store the extracted power and realize the MPPT technique. An off-chip oscillator ESC-327KE with 32.768 kHz is used as the reference frequency for the frequency detector, which consumed only 2 $\mu$A, provided by the on-board power supply.

Fig. 11 illustrates the measured power consumption and breakdown of the proposed energy harvesting system including a 1 mH inductor, at $f_P$ = 133 Hz, $V_{OC}$ = 1.5 V. Meanwhile, consumption currents of each module are listed in the right table. The system delivers 39.72 $\mu$W output power with a 10.3$\mu$A load current, while 5.80 $\mu$W is consumed in the control circuits, LDO, reference etc., achieving an overall power efficiency of 85.4%. Thanks to the proposed dynamic bias technique, the power consumption of the comparator in the MPPT and SSHI are 43 nW and 19 nW, respectively. In other works [19], [24], the comparator can consume a much higher power in order to provide sufficient bandwidth.

The measured rectifier output powers at 1.5 V $V_{OC}$ with different inductors are shown in Fig. 12. The load currents with corresponding output power are listed in the figure. The maximum output power measured with an on chip NVC is 6.14 $\mu$W, while it is 23.12 $\mu$W (3.77X), 31.17 $\mu$W (5.08X), and 43.65 $\mu$W (7.11X) with 110 $\mu$H, 220 $\mu$H, and 1 mH inductors, respectively.

Fig. 13 (a) shows the measured waveform of $V_{PT}$, $V_{REC}$, and $V_S$ during start-up, by a DSOX2004 oscilloscope. The system starts from a cold state with a vibration excitation level equivalent to 1.5 V $V_{OC}$. Initially, the $V_{REC}$ increases steadily when $D_{TOFF}$ < 50%, accumulating charge in the output capacitor without connecting the switched capacitor $C_S$. Once the $V_{REC}$ reaches the $V_{MPP}$, the $D_{TOFF}$ becomes 50% and tends to increase further. At this moment, the switched

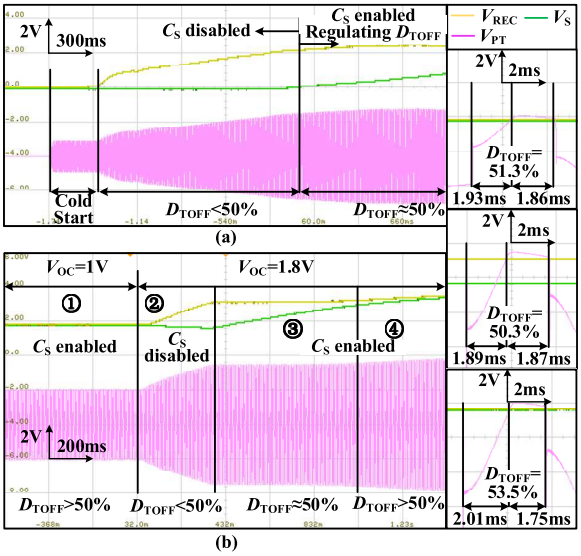



Fig. 13. (a) Measured start-up of the piezoelectric system. (b) Measured waveform of $V_{PT}$, $V_{REC}$ and $V_S$ during the MPPT transient time with 1 and 1.8V $V_{OC}$ input. (1) Steady-state at 1V $V_{OC}$. (2) SC-DCB MPPT evaluates $D_{TOFF}$ making the $V_{REC}$ = $V_{MPP}$. (3) The $C_S$ is fully charged, MPPT stops.

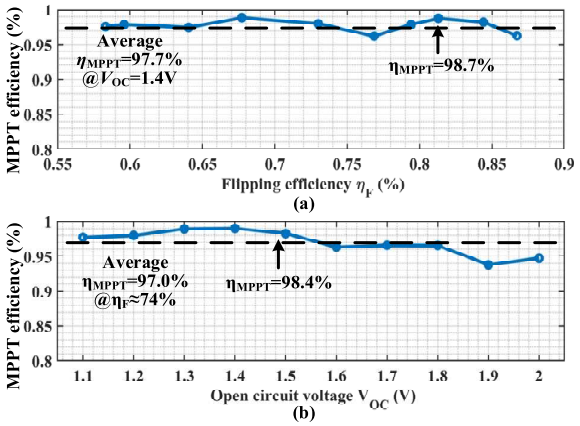



Fig. 14. MPPT efficiency versus (a) $\eta_F$ and (b) $V_{OC}$.

capacitor $C_S$ is enabled by the MPPT controller to regulate $V_{REC}$, making it back to $V_{MPP}$ ($D_{TOFF}$ at 50%). This effect is shown by the green curve ($V_S$) in Fig. 13(a), which starts to increase ($C_S$ enabled) rises after $D_{TOFF}$ reaches 50%.

Fig. 13 (b) shows the measured waveform during the MPPT transient time with input changing from 1.0 V to 1.8 V $V_{OC}$. At the first steady state, the $C_S$ is fully charged making $V_S$ = $V_{REC}$ and it keeps connected when the $D_{TOFF}$ exceeds 50% as shown in the (1) section. Once the vibration excitation level increases to 1.8 V $V_{OC}$, the $D_{TOFF}$ falls below 50% by the SSHI scheme, and the MPPT controller disconnects the $C_S$, resulting the $V_{REC}$ increases to track the higher $V_{MPP}$, as shown in the (2) section. When the $D_{TOFF}$ reaches 50%, the $C_S$ is enabled again to maintain the $V_{REC}$ at the new $V_{MPP}$, while keeping the $D_{TOFF}$ at around 50%, as shown in the (3) section. Once the $C_S$ is fully charged again, the $D_{TOFF}$ exceeds 50%, as shown in the (4) section, where the $D_{TOFF}$ = 53.5% at final steady state, limited by the power loss.

Fig. 14 shows the overall efficiency of the system with MPPT at different flipping efficiency ($\eta_F$) and open circuit voltage ($V_{OC}$), by adjusting the off-chip inductor and the

TABLE I
PERFORMANCE COMPARISON WITH PRIOR WORKS

| | **This Work** | JSSC 2020 [26] | JSSC 2024 [28] | JSSCL 2022 [31] | ISSCC 2020 [33] | JSSC 2023 [42] | JSSC 2025 [39] |
|---|---|---|---|---|---|---|---|
| Technology (nm) | **55** | 180 | 180 | 180 | 600 | 180 | 180 |
| Active Area ($mm^2$) | **0.071** | 0.2 | 0.7 | 0.258 | N/R | 0.8 | 0.91 |
| Rectifier scheme | **SSHI** | SPFCR | SBFRR | SSHC | SECE | SSHI | BMRR |
| PZT | **PPA-1021** | PPA-1021 | PPA-1021[A] | PPA-1021 | PPA-1011 | PPA-1014 | PPA-1021 PPA-1011 |
| $C_P$ (nF) | **22** | 22 | 88[A] | 18 | 24 | 42 | 23/116 |
| Frequency (Hz) | **133** | 200 | 100 | 200 | 56 | 230 | 133/120 |
| $V_{OC}$ (V) | **1.1 - 2** | 2 | N/R | 0.2 - 1.5 | 0.64 - 2.33 | 1.2 - 2 | 0.4 - 2 |
| MPPT Technique | **SC-DCB** | FOCV | FOCV | P&O | P&O | DCB | DCB |
| Peak MPPT Efficiency | **98.7%** | 72% | 83% | 95% | 94% | 98% | 99.9% |
| Power Consumption | **129 nW[B]** | N/R | 2.1 μW | N/R | <1 μW[C] | 306 nW[D] | 43.3 nW[D] |
| Flipping efficiency $\eta_F$ | **82%** | 84% | 80% | 87% | N/R | 82% | 87.5% |
| FoM ($P_{IC}/P_{NVC}$) | **711%** | 590%~930% | 278%~488% | 570% | 328% | 738% | 930% |

[A] Four PTs are used. [B] Including SSHI controller, duty cycle assessment block and switched capacitor controller. [C] Including power sensing, P&O and SSECE controller. [D] Including MPPT block only. N/R: Not reported.

vibration excitation level. Fig. 14 (a) shows the averaged $\eta_{MPPT}$, defined in (9), is 97.7% within the range of flipping efficiency from 58% to 87% at 1.4 V $V_{OC}$, proving its theoretical achievable value (100%) analysed in Section II-B. A peak efficiency of 98.7% is achieved at a $\eta_F$ of 82%. In the Fig. 14 (b), when the $V_{OC}$ of the PT device varies from 1.1 V to 2 V, with a $\eta_F$ of around 74%, the measured averaged $\eta_{MPPT}$ is 97.0%. It also achieves the peak $\eta_{MPPT}$ is 98.4%. The results show that a high MPPT efficiency can be achieved over different $\eta_F$ and $V_{OC}$. This independency on $\eta_F$ and $V_{OC}$ is also reported in [39] and [42], with DCB MPPT.

Table I summarizes the performance of the proposed energy harvesting interface and compares it with the state-of-the-art designs. Thanks to the use of the DCB MPPT technique, the proposed interface circuit achieves a 98.7% peak $\eta_{MPPT}$, which is in line with other works with continuous MPPT technique. Measured results shows a power extraction enhancement FoM of 711%, which is in line with other works. The peak $\eta_{MPPT}$ of the proposed interface circuit is much higher than FOCV based designs [26], [28]. Meanwhile the controller of the proposed interface consume only 129 nW, including two comparators and controllers, which is the lowest compared to other works except [39] (43.3 nW) with a digital controller. It is worth noting that, the MPPT block in [39] requires an on-chip oscillator which consumes 67.5 nW, which is not included. Moreover, the power consumption of the $V_{OUT}$ regulation block is also not included.

### *B. Measurement of the Sensor Interface and System*

Fig. 15 shows the measured waveform of the $V_{PT}$ and the Flag signal during wakeup operation, with a 4-gram loads added to the PT [23]. The vibration frequency varies from 15 Hz to 25 Hz. Initially, the flag is low when the vibration frequency stays below 20 Hz. When the frequency becomes higher than the threshold value, it takes about 60ms for the frequency detector to wake up the frontend interface.

Fig. 16 shows the measured input noise spectrum, of the amplifier with a gain of X8. An input-referred noise floor

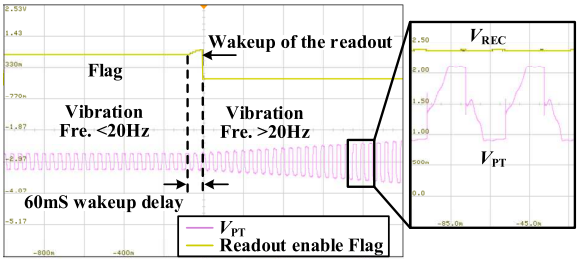



Fig. 15. Measured waveform of $V_{PT}$ and Flag during wakeup operation.

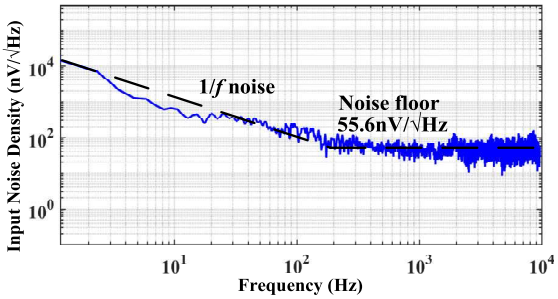



Fig. 16. Input noise density of the ultra-low power amplifier.

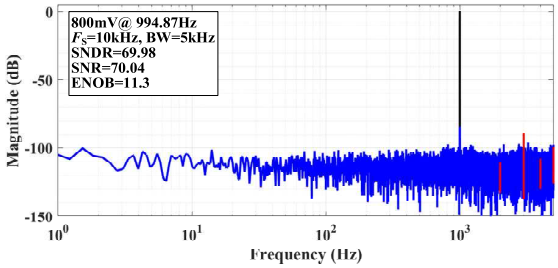



Fig. 17. Measured spectrum of the ultra-low power amplifier and ADC with input sinusoidal wave frequency of 994.87Hz.

of 55.6 nV/√HZ and a 1/$f$ corner frequency of 110Hz can be derived, resulting in a $V_{RMS}$ of 5.5 $\mu$V in-band (1 to 10 kHz). Fig. 17 shows the measured FFT of the SAR ADC with an input signal of 800m$V_{PP}$.@994.87Hz. An SNDR of 69.98dB in 5 kHz bandwidth is obtained, providing an ENOB of 11.3 bit.

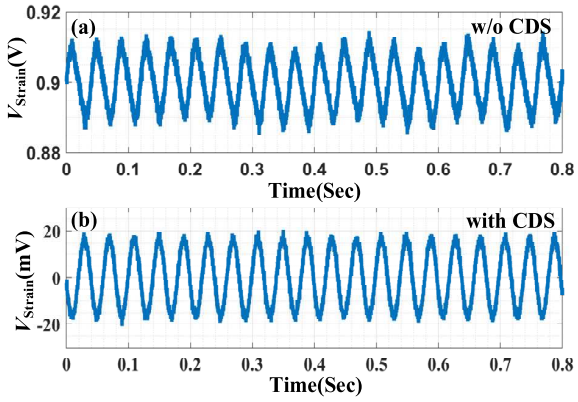



Fig. 18. Measured Strain curve w/o and with CDS.

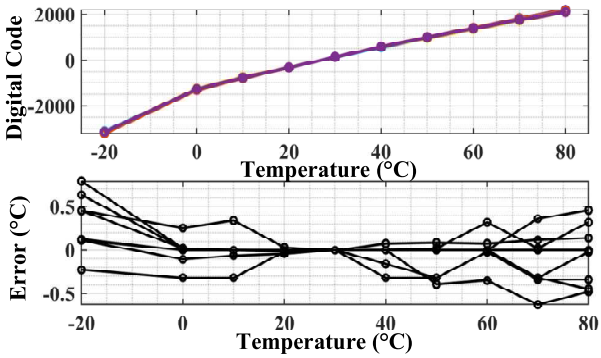



Fig. 19. (a) Measured temperature curve with CDS. (b) Temperature inaccuracy for 10 samples, measured at 100 S/s.

Fig. 18 shows the measured strain curve with/without correlated double sampling (CDS). Two BF-1000 strain gauges are attached on both sides of the vibrating transducer plate, together with two 1 kΩ resistors to setup a Wheatstone bridge. The PT amounts 6-grams mess as load to increase the excited energy and the strain. The excitation frequency is 25 Hz with acceleration amplitude around 1$g$. In order to save power, the $f_S$ of the SAR ADC is reduced to 100 Hz. The small waveform from the strain gauge is amplified 128X and sensed by the SAR ADC. The power line interference coupled to the signal Fig. 18 (a) an be removed by the CDS effectively in Fig. 18 (b). The averaged peak voltage of Fig. 18 (b) is 18.93 mV, indicating that the strain $\varepsilon$ is around 40$\mu$ [15], [35].

Fig. 19 shows the measured temperature output codes acquired from ten IC samples in a temperature chamber from -20 to 80 °C. Two PT-1000 sensors are placed in the Wheatstone bridge. A 100 Hz correlated double sampling frequency is chosen to balance the performance and the efficiency. As proven in [26], 1-point calibration is sufficient for double sided measurements. In this case, the CDS based ADC is 1-point calibrated by reading out at room temperature. This results in an inaccuracy of -0.6/0.8 °C.

Fig. 20 shows the power breakdown of the proposed sensor interface. The sensor interface consumes 9.05 $\mu$W in total when it is enabled continuously with 10 kHz sampling frequency and the amplitude is configurated as 4X. The averaged power consumption of the proposed amplifier is 8.28 $\mu$W. Meanwhile the SAR ADC consumes an averaged power of 0.77 $\mu$W. Thanks to the event-driven like CDS operation with

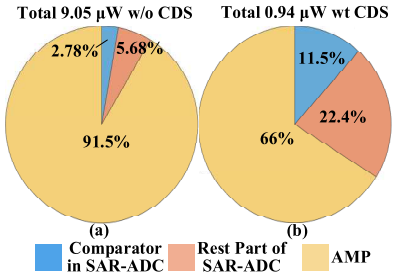



Fig. 20. Power breakdown of the proposed sensor interface: (a) continuous operation with $f_S$ = 10 kHz; (b) CDS operation with $f_S$ = 100 Hz.

TABLE II
PERFORMANCE COMPARISON WITH PRIOR WORKS

| | **This Work** | JSSCL'18 [35] | TCASI'20 [55] | TCASI'21 [56] | JSSC'24 [57] |
|---|---|---|---|---|---|
| ADC | **SAR** | SAR | ΣΔ | FDC | NS SAR |
| Area (mm$^2$) | **0.064** | 0.06 | 0.003 | 0.07 | 0.057 |
| T range (°C) | **-20-80** | 0-100 | -10-110 | 0-80 | -50-110 |
| Power | **0.94µW** | 49.6nW | 111.8µW | 0.196µW | 61.2µW |
| Resolution (mK) | 55 | 68 | 65 | 100 | 92 |
| Inaccuracy | **-0.6/0.8** | -1.1/1.5 | +-0.45 | +0.44/-0.4 | +1/-1 |
| Calibration | **1-point** | 1-point | 2-points | 2-points | 1-point |
| Conversion Time | **100µs** | 1ms | 4.1ms | 59ms | 80µs |
| Energy/Conv (nJ) | **9.39** | 0.496 | 460 | 11.56 | 9.39 |

100 Hz CDS frequency, the power consumption of the amplifier can be reduced to 0.6 $\mu$W with the same configuration. With 100 $\mu$s conversion time, the power consumption of the SAR ADC is 0.34 $\mu$W.

Table II summarizes the key performance of the proposed sensor interface compared with others. This work achieves good accuracy with one-point calibration. The conversion time is shorter than the others thanks to the asynchronized SAR operation. With the implementation of the amplifier, the effective resolution of the frontend is 55 mK. Meanwhile, the dynamic bias of the amplifier reduces the average power of the readout to < 1 $\mu$W, at 4X amplifier gain and 100 Hz $f_S$. Moreover, this ADC $f_S$ can be adjusted from 100 Hz to 10 kHz.

## V. CONCLUSION

In this paper, a vibration piezoelectric energy-harvesting sensor interface IC with high-efficient power management and readout circuit is proposed for structural health monitoring. The SC-DCB MPPT scheme is implemented together with an SSHI rectifier. This scheme can adjust the switched capacitor array to regulate the duty cycle by a simple and power efficiency controller. The chip is implemented in a 55 nm CMOS technology and validated by suitable experiments. Compared to an NVC, the energy harvesting interface achieves a 711% power extraction enhancement at the 133 Hz vibration frequency. By exploiting the DCB MPPT scheme, the efficiency can be kept above 95% with a flipping efficiency and open circuit voltage range from 58% to 87% and 1.1 V to 2 V at 133 Hz, respectively. Meanwhile, the vibration frequency based event driven wake-up of the readout circuit is demonstrated. Within the readout circuit, the amplifier consumes an average quiescent current of 4.6 $\mu$A with a $f_S$

of 10 kHz, while supporting CDS operation. The SAR ADC achieves 11.3 ENOB in a 5 kHz bandwidth with 0.77 $\mu$W power. The temperature, strain and vibration frequency can be extracted from the proposed interface IC at a minimal 20Hz vibration frequency, with only 0.94 $\mu$W total power, which makes the propose IC suitable for structural health monitoring.

## REFERENCES


[1] H. F. Lima et al., "Structural health monitoring of the church of santa casa da MisericÓrdia of Aveiro using FBG sensors," *IEEE Sensors J.*, vol. 8, no. 7, pp. 1236–1242, Jul. 2008, doi: 10.1109/JSEN.2008.926177.

[2] Z. S. Chen, Y. M. Yang, and Z. Hu, "A technical framework and roadmap of embedded diagnostics (Don't short) and prognostics for complex mechanical systems in prognostics and health management systems," *IEEE Trans. Rel.*, vol. 61, no. 2, pp. 314–322, Jun. 2012, doi: 10.1109/TR.2012.2196171.

[3] P. Dobrzycki, C. Kongar-Syuryun, and A. Khairutdinov, "Vibration reduction techniques for rapid impulse compaction (RIC)," *J. Phys., Conf. Ser.*, vol. 1425, no. 1, Dec. 2019, Art. no. 012202, doi: 10.1088/1742-6596/1425/1/012202.

[4] L. Zhu, J. Meng, L. Chen, and X. Hu, "Experimental investigation and in-situ testing of traffic-induced vibrations on the adjacent ruins of an ancient cultural sites," *Appl. Sci.*, vol. 13, no. 24, p. 13347, Dec. 2023, doi: 10.3390/app132413347.

[5] S. Chrisopoulos and J. Vogelsang, "A finite element benchmark study based on experimental modeling of vibratory pile driving in saturated sand," *Soil Dyn. Earthq. Eng.*, vol. 122, pp. 248–260, Jul. 2019, doi: 10.1016/j.soildyn.2019.01.001.

[6] R. Zhou, S. Zhou, and X. Zha, "Vibration and wave propagation in high-rise industrial buildings," *Buildings*, vol. 14, no. 8, p. 2340, Jul. 2024, doi: 10.3390/buildings14082340.

[7] *Vibrations in Buildings-Part 3: Effects on Structures*, document DIN 4150-3:2016-12, German Institute for Standard, Berlin, Germany, 2016.

[8] *Circulaire Du 23/07/86 Relative Aux Vibrations Mécaniques émises Dans L'environnement Par Les Installations Classées Pour La Protection De L'environnement — AIDA*. Accessed: Sep. 4, 2025. [Online]. Available: https://aida.ineris.fr/reglementation/circulaire-230786-relative-vibrations-mecaniques-emises-lenvironnement-installations

[9] *Code of Practice for Noise and Vibration Control on Construction and Open Sites-Part 2: Vibration. BSI*, document BS 5228-2:2009, London, U.K., 2009.

[10] M. Baca, "Structural vibration analysis with reference to different standards," *Buildings*, vol. 15, no. 11, p. 1951, Jun. 2025, doi: 10.3390/buildings15111951.

[11] P. A. Laplante, M. Kassab, N. L. Laplante, and J. M. Voas, "Building caring healthcare systems in the Internet of Things," *IEEE Syst. J.*, vol. 12, no. 3, pp. 3030–3037, Sep. 2018, doi: 10.1109/JSYST.2017.2662602.

[12] H. S. Park, K. Park, Y. Kim, and S. W. Choi, "Deformation monitoring of a building structure using a motion capture system," *IEEE/ASME Trans. Mechatronics*, vol. 20, no. 5, pp. 2276–2284, Oct. 2015, doi: 10.1109/TMECH.2014.2374219.

[13] K. Javed, R. Gouriveau, N. Zerhouni, and P. Nectoux, "Enabling health monitoring approach based on vibration data for accurate prognostics," *IEEE Trans. Ind. Electron.*, vol. 62, no. 1, pp. 647–656, Jan. 2015, doi: 10.1109/TIE.2014.2327917.

[14] W. Flores-Fuentes, M. Rivas-Lopez, O. Sergiyenko, J. C. Rodríguez-Quiñonez, D. Hernández-Balbuena, and J. Rivera-Castillo, "Energy center detection in light scanning sensors for structural health monitoring accuracy enhancement," *IEEE Sensors J.*, vol. 14, no. 7, pp. 2355–2361, Jul. 2014, doi: 10.1109/JSEN.2014.2310224.

[15] S. A. A. Jabir and N. K. Gupta, "Thick-film ceramic strain sensors for structural health monitoring," *IEEE Trans. Instrum. Meas.*, vol. 60, no. 11, pp. 3669–3676, Nov. 2011, doi: 10.1109/TIM.2011.2138310.

[16] D. Praslicka et al., "Possibilities of measuring stress and health monitoring in materials using contact-less sensor based on magnetic microwires," *IEEE Trans. Magn.*, vol. 49, no. 1, pp. 128–131, Jan. 2013, doi: 10.1109/TMAG.2012.2219854.

[17] R. Blakey, I. Nakouti, O. Korostynska, A. Mason, and A. Al-Shamma'a, "Real-time monitoring of Pseudomonas Aeruginosa concentration using a novel electromagnetic sensors microfluidic cell structure," *IEEE Trans. Biomed. Eng.*, vol. 60, no. 12, pp. 3291–3297, Dec. 2013, doi: 10.1109/TBME.2013.2268277.

[18] M. W. Häckell, R. Rolfes, M. B. Kane, and J. P. Lynch, "Three-tier modular structural health monitoring framework using environmental and operational condition clustering for data normalization: Validation on an operational wind turbine system," *Proc. IEEE*, vol. 104, no. 8, pp. 1632–1646, Aug. 2016, doi: 10.1109/JPROC.2016.2566602.

[19] H. Wang, L. Dong, W. Wei, W.-S. Zhao, K. Xu, and G. Wang, "The WSN monitoring system for large outdoor advertising boards based on ZigBee and MEMS sensor," *IEEE Sensors J.*, vol. 18, no. 3, pp. 1314–1323, Feb. 2018, doi: 10.1109/JSEN.2017.2770324.

[20] F. Zonzini, M. Zauli, M. Mangia, N. Testoni, and L. De Marchi, "Model-assisted compressed sensing for vibration-based structural health monitoring," *IEEE Trans. Ind. Informat.*, vol. 17, no. 11, pp. 7338–7347, Nov. 2021, doi: 10.1109/TII.2021.3050146.

[21] S. Song et al., "Low-power on-chip energy harvesting: From interface circuits perspective," *IEEE Open J. Circuits Syst.*, vol. 5, pp. 267–290, 2024, doi: 10.1109/OJCAS.2024.3423484.

[22] D. A. Sanchez, J. Leicht, F. Hagedorn, E. Jodka, E. Fazel, and Y. Manoli, "A parallel-SSHI rectifier for piezoelectric energy harvesting of periodic and shock excitations," *IEEE J. Solid-State Circuits*, vol. 51, no. 12, pp. 2867–2879, Dec. 2016, doi: 10.1109/JSSC.2016.2615008.

[23] A. Morel et al., "A shock-optimized SECE integrated circuit," *IEEE J. Solid-State Circuits*, vol. 53, no. 12, pp. 3420–3433, Dec. 2018, doi: 10.1109/JSSC.2018.2868299.

[24] J. Kan, C. He, Y. Lin, S. Lin, Z. Cao, and Z. Zhang, "Low-frequency piezoelectric energy harvesting from coupled longitudinal–transverse vibration of two magnetic coupling-based orthogonal beams," *IEEE Sensors J.*, vol. 24, no. 9, pp. 13892–13902, May 2024, doi: 10.1109/JSEN.2024.3373021.

[25] L. Costanzo, A. Lo Schiavo, and M. Vitelli, "Analytical study of piezoelectric harvesters with SECE and SSHI under variable excitation," *IEEE Trans. Ind. Appl.*, vol. 58, no. 2, pp. 2280–2290, Mar. 2022, doi: 10.1109/TIA.2022.3142664.

[26] Z. Chen, M.-K. Law, P.-I. Mak, X. Zeng, and R. P. Martins, "Piezoelectric energy-harvesting interface using split-phase flipping-capacitor rectifier with capacitor reuse for input power adaptation," *IEEE J. Solid-State Circuits*, vol. 55, no. 8, pp. 2106–2117, Aug. 2020, doi: 10.1109/JSSC.2020.2989873.

[27] B. Çiftci, S. Chamanian, A. Koyuncuoglu, A. Muhtaroglu, and H. Külah, "A low-profile autonomous interface circuit for piezoelectric micro-power generators," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 68, no. 4, pp. 1458–1471, Apr. 2021, doi: 10.1109/TCSI.2021.3053503.

[28] Z. Li et al., "Piezoelectric energy harvesting interface using self-bias-flip rectifier and switched-PEH DC–DC for MPPT," *IEEE J. Solid-State Circuits*, vol. 59, no. 7, pp. 2248–2259, Jul. 2024, doi: 10.1109/JSSC.2023.3341865.

[29] L. Mamouri, T. Mesbahi, and V. Frick, "MPPT technique with improved FOCV control applied to a full active rectifier for low-voltage piezoelectric energy harvesting," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 71, no. 2, pp. 532–536, Feb. 2024, doi: 10.1109/TCSII.2023.3308956.

[30] A. Devaraj, M. Megahed, Y. Liu, A. Ramachandran, and T. Anand, "A switched capacitor multiple input single output energy harvester (Solar + Piezo) achieving 74.6% efficiency with simultaneous MPPT," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 12, pp. 4876–4887, Dec. 2019, doi: 10.1109/TCSI.2019.2934985.

[31] S. Chamanian and P. P. Mercier, "MIPSIMO: A multi-input piezo-adaptive single-inductor multi-output energy harvester achieving using a shared inductor with an integrated analog computer achieving 95% MPPT efficiency," *IEEE Solid-State Circuits Lett.*, vol. 5, pp. 222–225, 2022, doi: 10.1109/LSSC.2022.3203978.

[32] S. Li, A. Roy, and B. H. Calhoun, "A piezoelectric energy-harvesting system with parallel-SSHI rectifier and integrated maximum-power-point tracking," *IEEE Solid-State Circuits Lett.*, vol. 2, no. 12, pp. 301–304, Dec. 2019, doi: 10.1109/LSSC.2019.2951394.

[33] A. Morel et al., "32.2 Self-tunable phase-shifted SECE piezoelectric energy-harvesting IC with a 30nW MPPT achieving 446% energy-bandwidth improvement and 94% efficiency," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2020, pp. 488–490, doi: 10.1109/ISSCC19947.2020.9062972.

[34] X. Yue, S. Javvaji, Z. Tang, K. A. A. Makinwa, and S. Du, "30.3 A bias-flip rectifier with a duty-cycle-based MPPT algorithm for piezoelectric energy harvesting with 98% peak MPPT efficiency and 738% energy-extraction enhancement," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2023, pp. 442–444, doi: 10.1109/ISSCC42615.2023.10067284.

[35] H. Xin, M. Andraud, P. Baltus, E. Cantatore, and P. Harpe, "A 174 pW–488.3 nW 1 S/s–100 kS/s all-dynamic resistive temperature sensor with speed/resolution/resistance adaptability," *IEEE Solid-State Circuits Lett.*, vol. 1, no. 3, pp. 70–73, Mar. 2018, doi: 10.1109/LSSC.2018.2827883.

[36] J. De Roose, H. Xin, A. Hallawa, G. Ascheid, P. J. A. Harpe, and M. Verhelst, "Flexible, self-adaptive sense-and-compress SoC for sub-microWatt always-on sensory recording," *IEEE Solid-State Circuits Lett.*, vol. 3, pp. 362–365, 2020, doi: 10.1109/LSSC.2020.3018382.

[37] H. Xin, P. Baltus, E. Cantatore, and P. Harpe, "A 0.32 nW–1.07 $\mu$W all-dynamic versatile resistive sensor interface with system-level ratiometric measurement," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 69, no. 2, pp. 506–517, Feb. 2022, doi: 10.1109/TCSI.2021.3119541.

[38] S. Roy, A. N. M. W. Azad, S. Baidya, and F. Khan, "A comprehensive review on rectifiers, linear regulators, and switched-mode power processing techniques for biomedical sensors and implants utilizing in-body energy harvesting and external power delivery," *IEEE Trans. Power Electron.*, vol. 36, no. 11, pp. 12721–12745, Nov. 2021, doi: 10.1109/TPEL.2021.3075245.

[39] X. Yue and S. Du, "A single-stage bias-flip regulating rectifier with fully digital duty-cycle-based MPPT for piezoelectric energy harvesting," *IEEE J. Solid-State Circuits*, vol. 60, no. 3, pp. 850–860, Mar. 2025, doi: 10.1109/JSSC.2024.3495232.

[40] S. Du, Y. Jia, C. Zhao, G. A. J. Amaratunga, and A. A. Seshia, "A passive design scheme to increase the rectified power of piezoelectric energy harvesters," *IEEE Trans. Ind. Electron.*, vol. 65, no. 9, pp. 7095–7105, Sep. 2018, doi: 10.1109/TIE.2018.2798567.

[41] L. Wu, X.-D. Do, S.-G. Lee, and D. S. Ha, "A self-powered and optimal SSHI circuit integrated with an active rectifier for piezoelectric energy harvesting," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 3, pp. 537–549, Mar. 2017, doi: 10.1109/TCSI.2016.2608999.

[42] X. Yue, S. Javvaji, Z. Tang, K. A. A. Makinwa, and S. Du, "A bias-flip rectifier with duty-cycle-based MPPT for piezoelectric energy harvesting," *IEEE J. Solid-State Circuits*, vol. 59, no. 6, pp. 1–11, Jun. 2024, doi: 10.1109/JSSC.2023.3313733.

[43] Q. Kuai, H.-Y. Leung, Q. Wan, and P. K. T. Mok, "A high-efficiency dual-polarity thermoelectric energy-harvesting interface circuit with cold startup and fast-searching ZCD," *IEEE J. Solid-State Circuits*, vol. 57, no. 6, pp. 1899–1912, Jun. 2022, doi: 10.1109/JSSC.2021.3128625.

[44] J. De Vos, D. Flandre, and D. Bol, "A sizing methodology for on-chip switched-capacitor DC/DC converters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 5, pp. 1597–1606, May 2014, doi: 10.1109/TCSI.2013.2285692.

[45] S. Song et al., "A low-voltage chopper-stabilized amplifier for fetal ECG monitoring with a 1.41 power efficiency factor," *IEEE Trans. Biomed. Circuits Syst.*, vol. 9, no. 2, pp. 237–247, Apr. 2015, doi: 10.1109/TBCAS.2015.2417124.

[46] J. Yao, Y.-Y.-M. Hew, A. Mears, and H. Huang, "Strain gauge-enable wireless vibration sensor remotely powered by light," *IEEE Sensors J.*, vol. 15, no. 9, pp. 5185–5192, Sep. 2015, doi: 10.1109/JSEN.2015.2437843.

[47] M. Zhao et al., "An ultra-low quiescent current tri-mode DC–DC buck converter with 92.1% peak efficiency for IoT applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 69, no. 1, pp. 428–439, Jan. 2022, doi: 10.1109/TCSI.2021.3090911.

[48] S. van der Ven et al., "A 6.1fJ/conv-step 0.0017 mm$^2$ level crossing ADC for compressive neural sensing with event-driven ramp generation and sparse DAC switching scheme," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Nov. 2024, pp. 1–3, doi: 10.1109/A-SSCC60305.2024.10848955.

[49] M. Timmermans, K. van Oosterhout, M. Fattori, P. Harpe, Y.-H. Liu, and E. Cantatore, "A 1.8–65 fJ/Conv.-step 64-dB SNDR continuous-time level crossing ADC exploiting dynamic self-biasing comparators," *IEEE J. Solid-State Circuits*, vol. 59, no. 4, pp. 1194–1203, Apr. 2024, doi: 10.1109/JSSC.2024.3352735.

[50] M. Li et al., "A 62.2dB SNDR event-driven level-crossing ADC with SAR-assisted delay compensation loop for time-sparse biomedical signal acquisition," *IEEE Trans. Biomed. Circuits Syst.*, vol. 19, no. 2, pp. 344–356, Apr. 2025, doi: 10.1109/TBCAS.2024.3423366.

[51] N. Van Helleputte et al., "A 345 $\mu$W multi-sensor biomedical SoC with bio-impedance, 3-channel ECG, motion artifact reduction, and integrated DSP," *IEEE J. Solid-State Circuits*, vol. 50, no. 1, pp. 230–244, Jan. 2015, doi: 10.1109/JSSC.2014.2359962.

[52] R. van Wegberg et al., "A 5-channel unipolar fetal-ECG readout IC for patch-based fetal monitoring," *IEEE Solid-State Circuits Lett.*, vol. 2, no. 9, pp. 71–74, Sep. 2019, doi: 10.1109/LSSC.2019.2931608.

[53] S. Song et al., "A noise reconfigurable current-reuse resistive feedback amplifier with signal-dependent power consumption for fetal ECG monitoring," *IEEE Sensors J.*, vol. 16, no. 23, pp. 8304–8313, Dec. 2016, doi: 10.1109/JSEN.2016.2589281.

[54] M. Edla, Y. Y. Lim, D. Mikio, and R. V. Padilla, "A single-stage rectifierless boost converter circuit for piezoelectric energy harvesting systems," *IEEE Trans. Energy Convers.*, vol. 37, no. 1, pp. 505–514, Mar. 2022, doi: 10.1109/TEC.2021.3103879.

[55] O. Bass and J. Shor, "A miniaturized 0.003 mm$^2$ PNP-based thermal sensor for dense CPU thermal monitoring," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 67, no. 9, pp. 2984–2992, Sep. 2020.

[56] J. Li, Y. Lin, N. Ning, and Q. Yu, "A + 0.44°C/-0.4°C inaccuracy temperature sensor with multi-threshold MOSFET-based sensing element and CMOS thyristor-based VCO," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 68, no. 3, pp. 1102–1113, Mar. 2021, doi: http://dx.doi.org/10.1109/TCSI.2020.3042825

[57] A. Aprile, M. Folz, D. Gardino, P. Malcovati, and E. Bonizzoni, "An area-efficient smart temperature sensor based on a fully current processing error-feedback noise-shaping SAR ADC in 180-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 59, no. 3, pp. 716–727, Mar. 2024, doi: http://dx.doi.org/10.1109/JSSC.2023.3342937

**Dehong Wang** (Graduate Student Member, IEEE) was born in Qingdao, China, in 1990. He received the B.S. degree in automation from Qingdao University of Science and Technology, Qingdao, and the dual M.S. degrees in electronic engineering and in artificial intelligent from the Katholieke Universiteit Leuven, Belgium, in 2017 and 2018, respectively. He is currently pursuing the Ph.D. degree in electronic and information engineering with Zhejiang University, Hangzhou, China. From 2016 to 2017, he was a Digital IC Design Intern with imec, Leuven. From 2018 to 2021, he was a Software Engineer with Honeywell, Shanghai, China. His research interests include analog and mixed-signal IC design, power management circuits, and digital circuit design methodology.

**Mengyu Li** (Graduate Student Member, IEEE) received the B.S. degree in microelectronic engineering from Xidian University, Xi'an, China, in 2019, and the Ph.D. degree in electronic science and technology from Zhejiang University, Hangzhou, China, in 2025. From 2018 to 2019, she was a Power Management IC Design Intern with Infineon Technology, Beijing, China. From 2023 to 2024, she was a Visiting Scholar with KU Leuven; and an IC Design Intern on neural interfaces with imec, Leuven, Belgium. In 2025, she moved to Eindhoven, The Netherlands and worked as a Researcher in biomedical integrated circuits and systems with imec, Eindhoven. Her research interests include analog and mixed signal IC design, low-power power management circuits, low-power ADCs, and recording and stimulation circuits for biomedical applications.

**Siyao Cao** was born in Xuchang, China, in 1993. She received the B.S. degree from the University of Electronic Science and Technology of China in 2014, and the M.S. degree in electronic engineering from the Katholieke Universiteit Leuven, Leuven, Belgium, in 2017. She is currently pursuing the Ph.D. degree in electronic and information engineering with Zhejiang University, Hangzhou, China. From 2016 to 2017, she was an IC Design and Application Intern with Connected Health Solutions, imec, Belgium. From 2017 to 2023, she was an Electronics Engineer with Lenovo, Beijing, China. Her research interests include analog and mixed signal IC design, power management circuits for the IoT, and bio-medical applications.

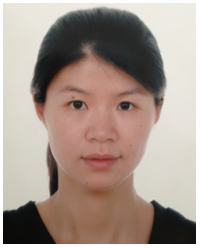
**Yulu Zhang** was born in Lishui, Zhejiang, China, in 2001. She received the B.S. degree in electronics engineering from Zhejiang University, Hangzhou, Zhejiang, in 2024, where she is currently pursuing the M.Sc. degree in integrated circuit engineering. Her research interests include analog and mixed signal IC design, interface circuits, and ADCs for the IoT and biomedical applications.

**Jiankao Pan** was born in 1988. He received the bachelor's degree in mechanical engineering. He is currently pursuing the Postgraduate degree with Shanghai Jiao Tong University. He is the Founder and one of the top managers of Zhejiang Transsemi Microelectronics Company Ltd. Before founding Transsemi, he was the Director of the Automotive-Grade Chip Laboratory, Zhejiang Provincial Innovation Center for Green and Intelligent Automotive and Components. He has extensive experience in full lifecycle of chip development, including product definition, design, and development. His research interests include electronics systems and ICs for automotive applications, MCUs, and low power design.

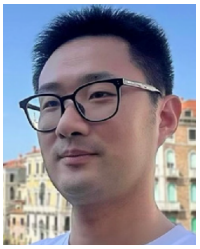
**Kai Huang** (Member, IEEE) received the B.S.E.E. degree from Nanchang University, Nanchang, China, in 2002, and the Ph.D. degree in engineering circuit and system from Zhejiang University (ZJU), Hangzhou, China, in 2008. In 2006, he was a short-term Visitor with the TIMA Laboratory, Grenoble, France. From 2009 to 2011, he was a Post-Doctoral Research Assistant with the Institute of VLSI Design, ZJU. In 2010, he was a Collaborative Expert with the VERIMAG Laboratory, Grenoble. From 2012 to 2020, he was an Associate Professor with the College of Information Science and Electronic Engineering, ZJU, where he is currently a Full Professor and the Director of the Institute of VLSI Design. He is also the Director of the ZJU-Apex Joint Laboratory. His current research interests include embedded processors and SoC design methodology.

**Sijun Du** (Senior Member, IEEE) received the B.Eng. degree (Hons.) in electrical engineering from the University Pierre and Marie Curie (UPMC), Paris, France, in 2011, the M.Sc. degree (Hons.) in electrical and electronic engineering from Imperial College London, London, U.K., in 2012, and the Ph.D. degree in electrical engineering from the University of Cambridge, Cambridge, U.K., in January 2018. He was with the Laboratoire d'Informatique de Paris 6 (LIP6), University Pierre and Marie Curie, and then an IC Engineer in Shanghai, China, from 2012 to 2014. He was a Summer Engineer Intern with Qualcomm Technology Inc., San Diego, CA, USA, in 2016. He was a Post-Doctoral Researcher with the Department of Electrical Engineering and Computer Sciences (EECS), University of California at Berkeley, Berkeley, CA, USA, from 2018 to 2020. In 2020, he joined the Department of Microelectronics, Delft University of Technology (TU Delft), Delft, The Netherlands, as an Assistant Professor. His current research is focused on energy-efficient integrated circuits and systems, including power management integrated circuits (PMIC), energy harvesting, wireless power transfer, and dc/dc converters.

**Zhichao Tan** (Senior Member, IEEE) received the B.Eng. degree from Xi'an Jiaotong University, Xi'an, China, in 2004, the M.Eng. degree from Peking University, Beijing, China, in 2008, and the Ph.D. degree from Delft University of Technology, Delft, The Netherlands, in 2013. From 2013 to 2019, he was a Staff IC Design Engineer with Analog Devices Inc., Wilmington, MA, USA, working on low-power, high-precision analog/mixed-signal circuit design. He joined Zhejiang University, Hangzhou, China, as a Faculty Member, in 2019. His research interests include energy-efficient sensor interfaces, precision analog circuits, and ultra-low-power analog-to-digital converters (ADCs). This has resulted in over 100 technical journal and conference papers. He holds five U.S. patents. He is a TPC Member of IEEE Custom Integrated Circuits Conference and IEEE Asian Solid-State Circuits Conference. He has served as an Associate Editor for IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, IEEE SENSORS JOURNAL, and IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS.



**Menglian Zhao** (Member, IEEE) received the M.S. degree in microelectronics and solid-state circuits and the Ph.D. degree in circuits and systems from Zhejiang University, Hangzhou, China, in 2001 and 2004, respectively. She joined the College of Electrical Engineering, Zhejiang University, in 2004. From 2005 to 2006, she was a Research Assistant with the Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Hong Kong. She is currently an Associate Professor with the College of Information Science and Electronic Engineering, Zhejiang University. Her current research interests include CMOS analog and mixed-signal integrated circuit design, low-power techniques for integrated circuits, and SoC.



**Shuang Song** (Member, IEEE) received the P.D.Eng. and Ph.D. degrees in mixed-signal IC design from Eindhoven University of Technology, Eindhoven, The Netherlands, in 2010 and 2015, respectively. From 2009 to 2010, he was an Analog IC Design Trainee with NXP Semiconductors, Eindhoven, The Netherlands. From 2015 to 2020, he was with imec, Leuven, Belgium, as a Researcher in biomedical integrated circuits. In 2020, he joined the School of Micro-Nano Electronics, Zhejiang University, Hangzhou, China, as a Faculty Member. He has (co-) authored over 50 papers in journals and conference proceedings, while holding several U.S. and EU patents. His research interests include analog and mixed signal integrated circuits, physiological signal processing, interface circuits for biomedical/IoT applications, and power management and battery management circuits and systems. He received the Distinguished-Technical-Paper Award from ISSCC 2019.