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A Sub-1 V 90 dB-SNDR Power/BW Scalable DTDSM Using Low-Voltage Cascoded Floating Inverter Amplifiers in 130 nm CMOS

Xinjie Wu, *Graduate Student Member, IEEE*, Yuyan Liu, *Graduate Student Member, IEEE*, Zhangming Zhu, Xiaopeng Yu, *Member, IEEE*, Nick Nianxiong Tan, *Senior Member, IEEE*, and Zhong Tang, *Member, IEEE*

***Abstract*— This paper presents a sub-1V delta-sigma modulator (DSM) with power and bandwidth (BW) scalability for IoT applications. It is built around a fully dynamic and low-voltage floating inverter amplifier (LVFIA). To extend the power and BW scalability of the LVFIA, its relatively supply-independent bias current is auto-controlled by DSM's sampling frequency f_s. Dynamic techniques such as auto-zeroing and chopping are applied to achieve low noise. Fabricated in a 130nm CMOS, the proposed sub-1V DSM shows a near-consistent SNDR (~90dB) and linearly scalable power and BW (2.5nW/Hz) over a ×30 scaling range of f_s. It achieves Walden FoM and Schreier FoM of 51.3fJ/conv-step and 175.7dB, respectively.**

***Index Terms*— Delta-sigma modulator (DSM), low-voltage FIA (LVFIA), low supply voltage, power/BW scalable, high-resolution.**

I. Introduction

The analog-to-digital converter (ADC) is an indispensable building block in IoT systems. It converts analog signals into digital codes for subsequent digital domain processing. In recent years, the evolution of IoT has driven the need for ADCs with high resolution and high energy efficiency. An effective way to reduce power consumption is to cut down the supply voltage. Lower supply is well-suited for battery-powered applications to extend service lifespan, or energy harvesting applications which typically have output voltages within a few hundred mV [1], [2], [3], [4]. Powered by batteries or energy harvesters, various sensors and biomedical devices need high-resolution ADCs with low/medium bandwidth (BW) typically ranging from DC to several kHz. The ADCs are expected to respond rapidly when processing high-speed signals while consuming ultra-low power for DC signal processing. Therefore, their power and BW are expected to be scalable for flexibility [5], [6]. However, it is challenging to achieve high precision and power/BW scalability simultaneously at low supply voltages.

Successive approximation register (SAR) ADCs feature fully dynamic and low supply operations [3], [7], [8]. The high proportion of digital circuits enables them to scale power simply by changing their sampling frequency f_s. However, they suffer from the mismatch in the capacitive digital-to-analog converter (CDAC) when achieving high resolution (>12bits). Although analog/digital calibration [9], [10], [11], noise shaping [12], [13], [14] and mismatch error shaping [15], [16] can be employed, these methods come at the expense of area and power.

Discrete-time delta-sigma modulators (DTDSMs) are widely used in high-resolution and low/medium BW IoT applications. However, their loop filters are usually based on the static operational transconductance amplifiers (OTAs), limiting their power and BW scalability. Fully dynamic DTDSMs based on floating inverter amplifiers (FIAs) have power/BW scalability [5], [6], [17], [18], [19]. However, the conventional FIAs typically require an over-1V supply [5], [6], [17], [19], [20], [21] to ensure fast settling, which limits their applications in low-supply sensors and devices.

To overcome this limitation, this paper proposes a sub-1V low-voltage FIA (LVFIA). It can operate at a lower supply and can adaptively change its power when f_s is varied. Based on it, a power/BW scalable DTDSM is designed which can operate at a 0.8V supply voltage. Dynamic techniques such as auto-zeroing (AZ) and chopping are applied to achieve low noise. Fabricated in a 130nm CMOS, the proposed sub-1V DSM demonstrates a near-consistent SNDR (~90dB) and linearly scalable power and BW (2.5nW/Hz) over a ×30 scaling range of f_s. It achieves Walden FoM and Schreier FoM of 51.3fJ/conv-step and 175.7dB, respectively.

The rest of this paper is organized as follows. Section II reviews previous dynamic amplifiers. Section III presents the proposed LVFIA and its operation principle in detail. The LVFIA-based DTDSM implementation is elaborated in Section IV, followed by measurement results in Section V. Section VI concludes this paper.

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Xinjie Wu and Xiaopeng Yu are with the School of Integrated Circuits, Zhejiang University, Hangzhou 310063, China.

Yuyan Liu is with the Department of Microelectronics, Faculty of Electrical Engineering, Mathematics and Computer Science (EEMCS), Delft University of Technology, 2628 CD Delft, The Netherlands.

Zhangming Zhu is with the School of Microelectronics, Xidian University, Xi'an 710126, China.

Nick Nianxiong Tan and Zhong Tang are with Vango Technologies, Inc., Hangzhou 310051, China (e-mail: tangz@zju.edu.cn).

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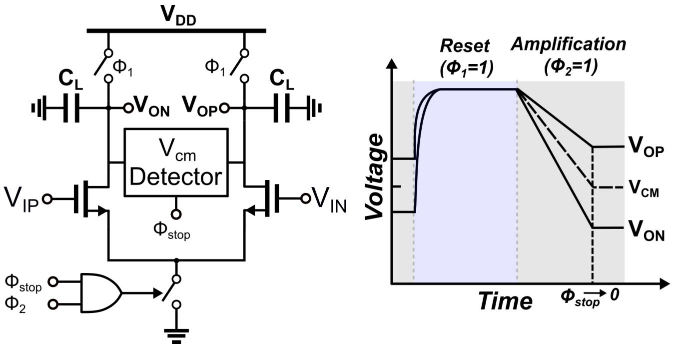


Fig. 1. The conventional dynamic amplifier with common-mode detector [22].

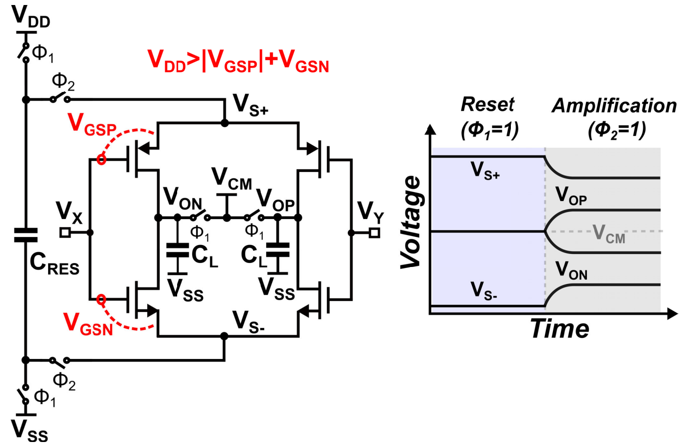


Fig. 2. The floating inverter amplifier [20].

II. Review of Prior-Art Dynamic Amplifiers

As an essential block of the DSM, the OTA must be fully dynamic to enable a power/BW scalable DSM. This section will review the existing dynamic OTAs.

A. The Conventional Dynamic Amplifier

The conventional dynamic amplifier (DA) [22], as shown in Fig. 1, consists of an input differential pair and two load capacitors C_L. C_L are pre-charged in ϕ_1, then discharge in ϕ_2 through the input differential pair, resulting in a change in the output common-mode voltage. When the common-mode voltage reaches the target value V_{CM}, the common-mode detector will be triggered to pull down the ϕ_{stop}. Then the current path from the source of the diff-pair to ground will be cut off and the amplification will be stopped. Therefore, the conventional DA based on the common-mode detector has fully dynamic characteristics when the sampling frequency is altered. However, its gain is moderate and varies greatly with temperature and supply voltages [22], [23]. As a result, the conventional DA is not suitable for loop filter designs in DSMs.

B. The Floating Inverter Amplifier

The FIA is another type of dynamic amplifier and also enables fully dynamic operation [20]. As shown in Fig. 2, there are two operation phases: during ϕ_1 (reset phase), a reservoir capacitor C_{RES} is pre-charged to the supply voltage; during ϕ_2 (amplification phase), a pair of inverters are powered by C_{RES} and differential charges are transferred to the load capacitors C_L. As the C_{RES} discharges, the current flowing through the inverters gradually decreases. Benefiting from the current-reuse structure, the FIA can achieve high energy efficiency. Moreover, the dynamic operation makes the FIA compatible with switch-capacitor circuitry. In addition, the FIA provides excellent common-mode rejection even without any common-mode feedback (CMFB) circuitry [20]. However, the bias current of this amplifier is heavily supply-dependent [5] and the voltage on pre-charged C_{RES} is constrained by:

$$V_{DD} > |V_{GSP}| + V_{GSN}. \tag{1}$$

where V_{GSP} and V_{GSN} are the gate-to-source voltages of the amplification transistors. To ensure adequate transconductance, we usually set the initial V_{GS} higher than the threshold voltage V_{TH}. Therefore, the supply voltage of the FIA is usually greater than 1V in mature CMOS processes. Although the FIA can also work at sub-1V supply by operating in sub-threshold region from the beginning of ϕ_2, it will slow down the fast initial settling [13], [24], leading to a lower bandwidth.

C. The Swing-Enhanced Floating Inverter Amplifier

Recently, the swing-enhanced FIA (SEFIA) was proposed as shown in Fig. 3 [5]. The SEFIA utilizes two reservoir capacitors C_{RES1} and C_{RES2}, operating in a ping-pong fashion. During ϕ_1, capacitors C_I function as floating current sources and the amplifier is auto-zeroed, powered by C_{RES2}. Thanks to the auto-zero capacitors C_C, the bias voltages of the PMOS and NMOS are separately defined thus the output swing can be increased [5]. During ϕ_2, C_{RES1} discharges to enable the amplification. As a result, the SEFIA achieves a wider output swing by the voltage across C_I at the end of the AZ phase, which equals $V_{BP} - V_{BN}$. Meanwhile, the fully dynamic and CMFB-free operation of the FIA is also preserved. However, the voltages across the diode-connected transistors (in ϕ_1) and C_I increase the requirement for the supply voltage to

$$V_{DD} > |V_{GSP}| + V_{GSN} + V_{CI} \tag{2}$$

where V_{CI} is the voltage across C_I. As a result, the SEFIA is not suitable for sub-1V operations. Furthermore, the use of two C_{RES} and C_I increases the die area.

Consequently, neither the conventional FIA nor the SEFIA is appropriate for sub-1V operations, especially in mature processes, where V_{TH} is high.

III. The Proposed Low-Voltage Floating Inverter Amplifier

To reduce the supply overhead, a low-voltage FIA is proposed in this section. Subsequently, its power efficiency, output swing, and BW scalability are discussed.

A. The Proposed LVFIA

The topology of the proposed LVFIA is shown in Fig. 4. The sub-1V operation can be realized using only one reservoir capacitor C_{RES}, several auto-zero capacitors C_C (much

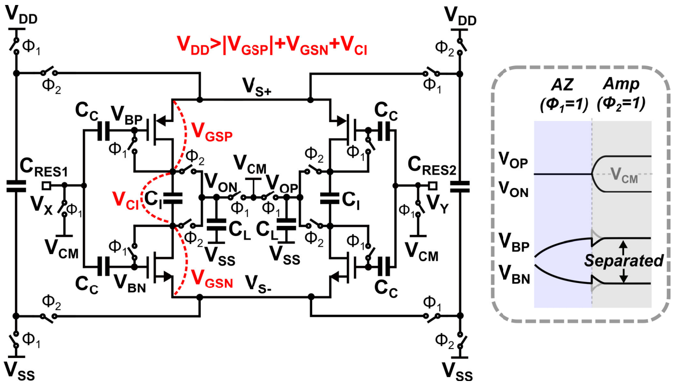


Fig. 3. The swing-enhanced floating inverter amplifier [5].

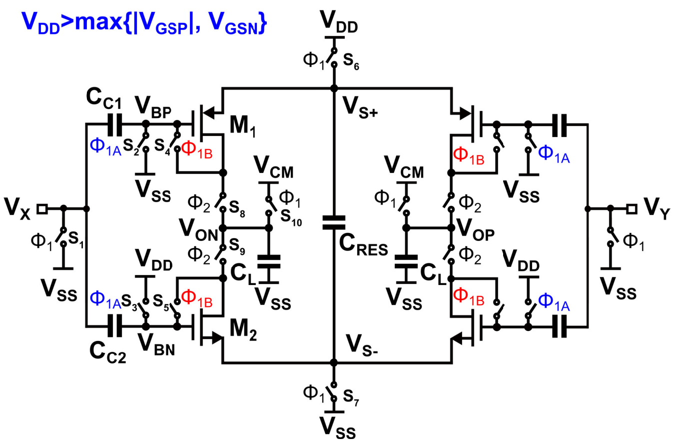


Fig. 4. The proposed low-voltage floating inverter amplifier (LVFIA).

smaller than C_{RES}) and a few switches. Fig. 5 illustrates its three operation phases and time-domain behaviors of the key nodes. Initially, during the reset phase (ϕ_{1A}), switches $S_{1,2,3,6,7,10}$ are closed and $C_{C1,2}$ and C_{RES} are pre-charged to V_{SS} or V_{DD} (Fig. 5(a)). The parasitic capacitors of the relevant nodes are reset simultaneously to avoid the impact on the amplification gain due to the residual signal-dependent charge. Additionally, the output voltages V_{OP} and V_{ON} are both reset to the common-mode voltage V_{CM}.

Subsequently, it enters the discharging and auto-zero phase (ϕ_{1B}) (Fig. 5(b)). During this phase, switches $S_{2,3}$ are opened while $S_{4,5}$ are closed, causing $C_{C1,2}$ to discharge through the diode-connected transistors M_1 and M_2, respectively. At the end of ϕ_{1B}, the gate potentials of $M_{1,2}$ (V_{BP} and V_{BN}) together with the offset and flicker noise are all stored on $C_{C1,2}$. The V_{GS} of $M_{1,2}$ will exhibit a logarithmic function of time and they are independent of the initial pre-charged potential of the capacitor C_C after a short initial period [25], [26], [27]. As a result, the sampled V_{GS} of M_1 and M_2 exhibit minimal variation with supply voltage changes, defining the bias current of the amplifier in a relatively supply-independent manner.

Then during the amplification phase (ϕ_2), switches $S_{1,4,5,6,7,10}$ are turned off, while $S_{8,9}$ are turned on (Fig. 5(c)). The input signal is AC coupled to $M_{1,2}$ through capacitors $C_{C1,2}$. Powered by C_{RES}, the input signal is amplified. The current mismatch of M_1 and M_2 at the end of ϕ_{1B} can be automatically corrected without a CMFB circuit similar to the conventional FIAs [20]. With the discharge of C_{RES}, the LVFIA will be turned off automatically, and the output voltage remains constant afterwards until the next clock cycle.

B. Power Efficiency

Because the auto-zero phase is used to establish the bias voltages, it only needs to be run once at the first clock cycle, theoretically. However, the leakage current causes the bias voltages to drift, so the auto-zero operation should be done at frequency f_{AZ} ($f_{AZ} = f_s/16$ in this work) to refresh the bias voltages. In addition, C_C (2pF) is much smaller than C_{RES} (21pF), thus the auto-zero phase of the LVFIA incurs negligible additional power consumption (5.7% of total power at $f_{AZ} = f_s/16$).

Consequently, the total power consumption of the LVFIA is still determined by the amplification phase. In this phase, the LVFIA is powered by capacitor C_{RES}, leading to a fully dynamic power consumption.

C. Supply Voltage Requirement and the Output Swing

For the proposed LVFIA, the supply voltage is limited by the discharging and auto-zero phase (ϕ_{1B}). In this phase, the V_{BP} and V_{BN} are established separately on two independent paths which are disconnected by switches $S_{8,9}$. Thus, the supply voltage only needs to be higher than the larger one of $|V_{GSP}|$ and V_{GSN}:

$$V_{DD} > max\{|V_{GSP}|, V_{GSN}\}. \tag{3}$$

Compared to the conventional FIA and the SEFIA, the proposed LVFIA reduces the supply voltage requirements by half or even more.

From [5], we know that the output swing of the SEFIA is increased by the separated bias voltages V_{BP} (for PMOS) and V_{BN} (for NMOS) which are generated by the voltage across C_I at the end of AZ phase. For the LVFIA, the bias voltages of PMOS and NMOS are also separately generated in the AZ phase. Therefore, like the SEFIA, the LVFIA can also achieve output swing enhancement. Fig. 6 shows the simulated output swing (corresponding to the −3dB point from peak gain) and the V_{BP}/V_{BN} as functions of the supply voltage V_{DD} at the best case (SS, −40°C) and the worst case (FF, 85°C). The results show that V_{BP} increases with V_{DD} to ensure that the V_{GS} of PMOS remains unchanged. At the same time, as $V_{BP} - V_{BN}$ increases, the output swing also increases with V_{DD}.

Compared to the SEFIA, the LVFIA needs only one reservoir capacitor and the AZ phase can be run at a lower frequency instead of f_s in [5], achieving higher area and power efficiency.

D. BW Scalability

Due to the fully dynamic operation of the LVFIA, there is no static current consumption. It allows its power consumption to scale linearly with sampling frequency f_s, which is commonly

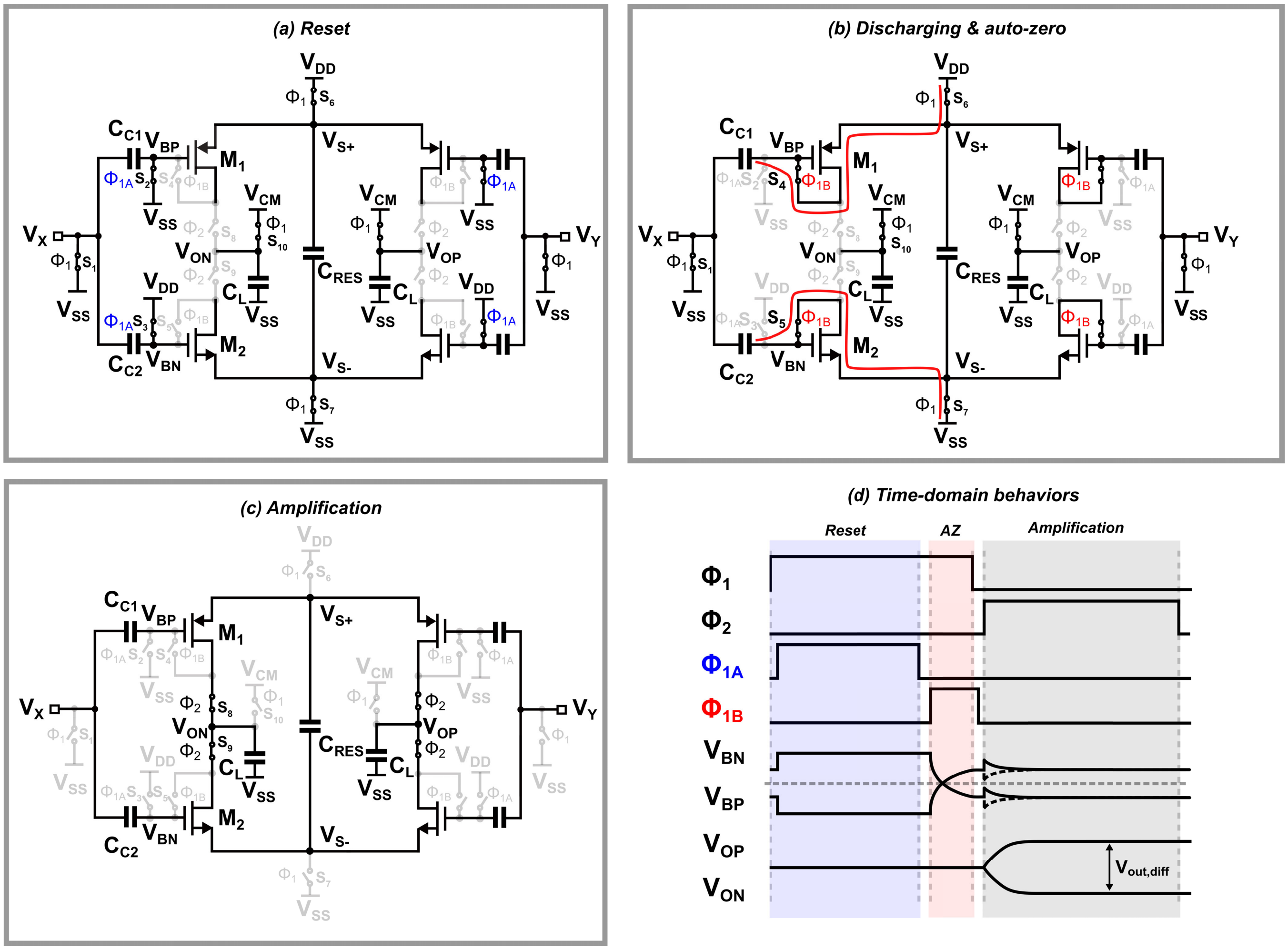


Fig. 5. (a)-(c) Operating phases of the proposed LVFIA; (d) Timing diagram and key-node waveforms of the proposed LVFIA.

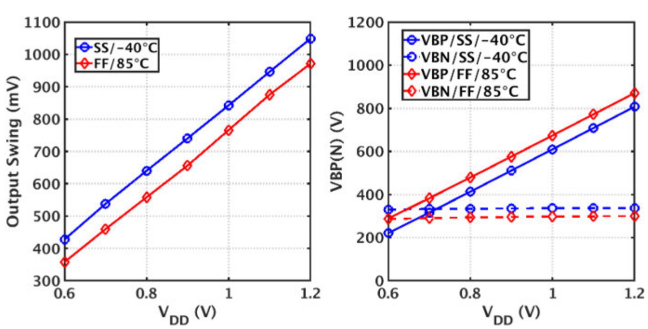


Fig. 6. The simulated output swing variation and the V_{BP}/V_{BN} variation with V_{DD} at the best case (SS, $-40°$C) and the worst case (FF, 85°C).

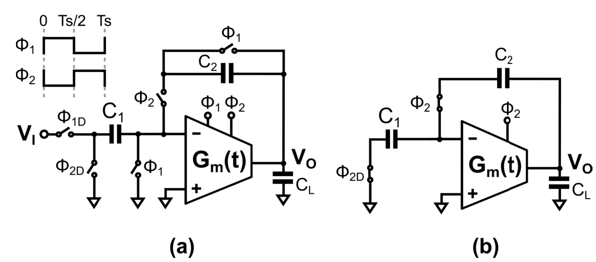


Fig. 7. (a) The single-ended SC amplifier based on the dynamic amplifier; (b) The equivalent circuit in the amplification phase.

known as power/BW scalability [5], [28]. However, due to the finite BW, the amplifier cannot settle well when f_s exceeds a certain range. To analyze the bandwidth scalability of the LVFIA, we use the SC amplifier shown in Fig. 7 for illustration (single-ended for simplification). The $G_m(t)$ represents the time-varying transconductance of the dynamic amplifier.

Because the $G_m(t)$ is time-varying, we define the $G_{m,avg}$ as the average transconductance of the amplifier in the amplification phase:

$$G_{m,avg} = \frac{2}{T_S}\int_0^{T_S/2} G_m(t)dt. \quad (4)$$

Then the average bandwidth of the amplification phase is:

$$BW_{avg} = \beta\frac{G_{m,avg}}{C_{L,tot}} \quad (5)$$

where $\beta = C_2/(C_1+C_2)$ and $C_{L,tot} = C_L + C_1C_2/(C_1+C_2)$. The output voltage V_O at the end of ϕ_2 [17] is:

$$V_O(T_S) = V_I(\frac{T_S}{2})\frac{C_1}{C_2} + V_I(\frac{T_S}{2})(1+\frac{C_1}{C_2})exp(-BW_{avg}\cdot\frac{T_S}{2}) \quad (6)$$

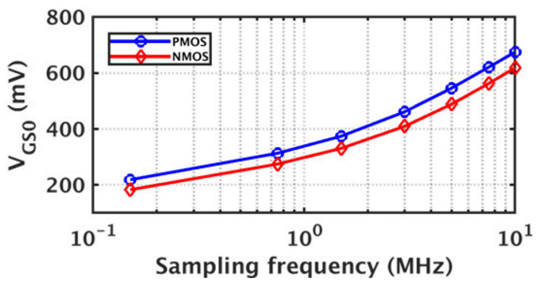


Fig. 8. The simulated bias voltages V_{GS0} of $M_{1/2}$ vs. sampling frequency f_s.

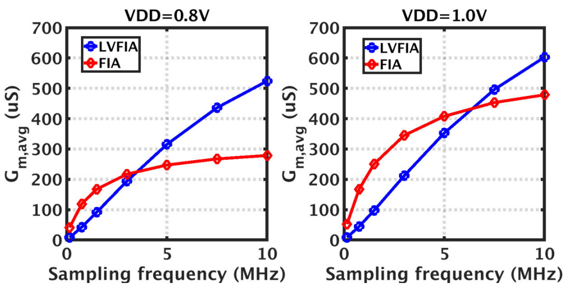


Fig. 9. The simulated average transconductances $G_{m,avg}$ of the LVFIA and the FIA vs. sampling frequency at different supplies.

Thus, the settling error caused by the finite bandwidth depends on the coefficient E_C:

$$E_C = exp(-BW_{avg} \cdot \frac{T_S}{2}) = exp(-\frac{\beta}{2C_{L,tot}} \cdot \frac{G_{m,avg}}{f_s}). \quad (7)$$

To ensure a negligible settling error as f_s changes, the $G_{m,avg}$ should scale linearly to track the variable f_s.

From [17] and the appendix, we know that the $G_{m,avg}$ of the FIA/LVFIA is related to the bias voltage V_{GS0} of $M_{1,2}$ at the beginning of the amplification phase. For the FIA, the bias voltage V_{GS0} is a constant at different f_s. For the proposed LVFIA, implemented by on-chip frequency dividers, the bias-defining phase ϕ_{1B} is in a fixed proportion (1/16) to the sampling clock $\phi_1(\phi_2)$, thus the generated bias voltages V_{GS0} of $M_{1,2}$ scale with the f_s as shown in Fig. 8.

Using the SC amplifier shown in Fig. 7, the $G_{m,avg}$ variations of the FIA and the LVFIA (with the same C_{RES} and transistor size) as functions of the sampling frequency have been simulated and are shown in Fig. 9. It can be seen that the scaled V_{GS0} helps the $G_{m,avg}$ of the LVFIA scale linearly with f_s. For higher f_s, the average bandwidth of the LVFIA will increase to expand the maximum value of f_s; for lower f_s, the average bandwidth of the LVFIA will decrease linearly with f_s to reduce the power consumption. At the same time, benefiting from the relatively supply-independent V_{GS0} generated in the AZ phase, the bandwidth scalable range of the LVFIA is less affected by supply voltage variation than that of the FIA.

IV. Sub-1v Power/Bw Scalable Dtdsm

To demonstrate the performance of the proposed LVFIA, it is used to build a sub-1V power/BW scalable DTDSM for IoT applications.

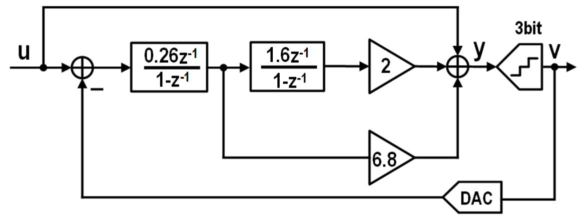


Fig. 10. The block diagram of the proposed delta-sigma modulator.

A. Architecture

The block diagram and the circuit diagram of the proposed DSM are shown in Fig. 10 and Fig. 11, respectively. To achieve a high resolution (~90dB), the DTDSM employs a 2^{nd}-order 3-bit architecture with an OSR of 128 and a sampling capacitor C_S of 0.8pF ($C_S = 0.8C_{DAC}$), which ensures that thermal noise is the dominant noise source. The cascade of integrators with feedforward (CIFF) structure and multi-bit quantization [29] are used to reduce the signal swing of the integrators (within ±70mV for the 1^{st} integrator and ±100mV for the 2^{nd} integrator), thus facilitating sub-1V operation. The 3-bit quantizer is implemented by an asynchronous SAR ADC. Top-plate sampling is adopted to simplify the DAC network. The SAR ADC also functions as a passive adder [29] for the feedforward paths, as shown in Fig. 11, avoiding the overhead of the active adder circuitry. Dynamic element matching (DEM) is adopted to mitigate nonlinearity in the CDACs of the DSM.

B. Integrator Based on Cascoded LVFIA

For this architecture, Fig. 12 shows the variation of SQNR with the amplifier's gain using the system modeling in SIMULINK. It can be seen that a 50dB gain is a safer choice for a 105dB SQNR. In circuit implementation, a cascoded version of LVFIA (Fig. 13(a)) can be used to ensure a DC gain of >50dB over PVTs. The C_{RES} is 21pF and the $C_{C1,2}$ are 2pF. Fig. 13(b) shows the simulated output swing of the cascoded LVFIA over PVTs (TT/FF/SS/FS/SF, 0.72V/0.80V/0.88V, −40°C/25°C/85°C). The results show an output swing of >150mV and the DC gain of >50dB (minimum at SS, 0.72V, −40°C) can be achieved. The cascode transistors $M_{3,4}$ also serve as the switches $S_{8,9}$ in Fig. 5 by switching their gate voltages. During ϕ_1, they are turned off by connecting their gates either to V_{DD} or V_{SS}. During ϕ_2, they are connected to the bias voltages $V_{1,2}$, respectively. The $V_{1,2}$ are dynamically generated by discharging small pre-charged capacitors $C_{1,2}$ (200fF) through the diode-connected transistors $M_{5,6}$ to maintain the robustness over supply variation while consuming negligible power. During ϕ_1, the load capacitors C_L are reset to V_{CM} which will be maintained during ϕ_2 without CMFB circuitry. To ensure both low leakage and low switch-on resistance with a sub-1V supply, the switches $S_{4,5,11,12}$ are implemented by thick gate oxide NMOS transistors driven by clock boosters [30].

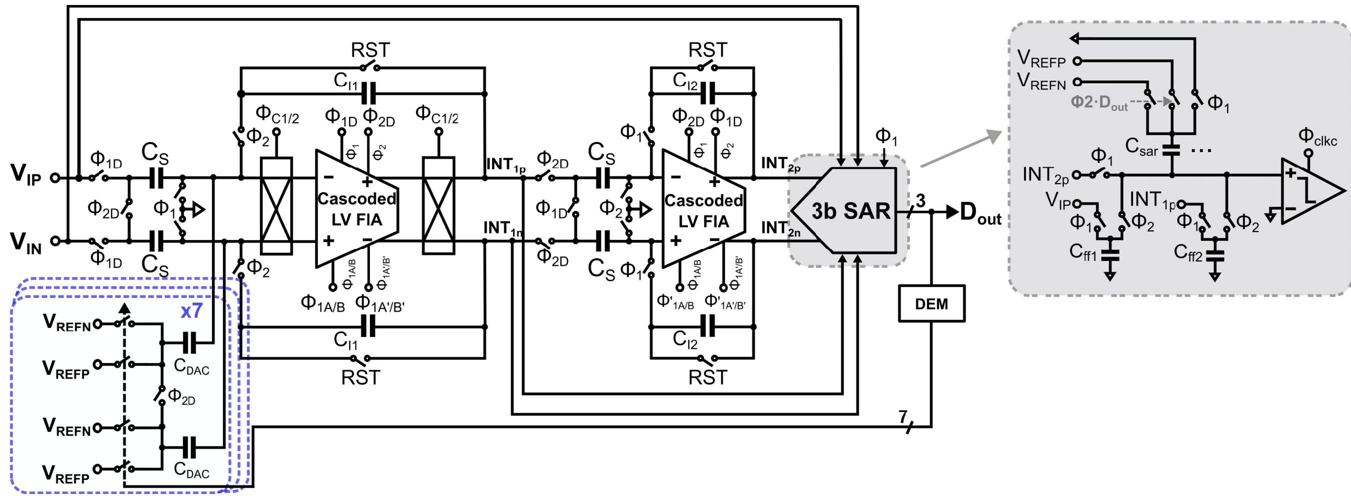


Fig. 11. The circuit diagram of the proposed delta-sigma modulator.

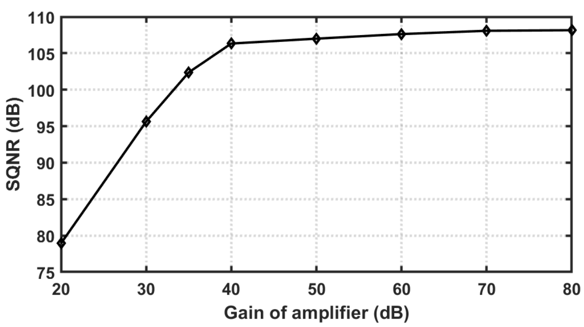
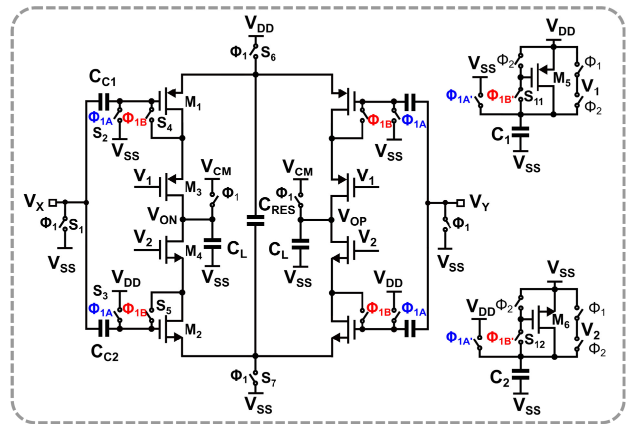
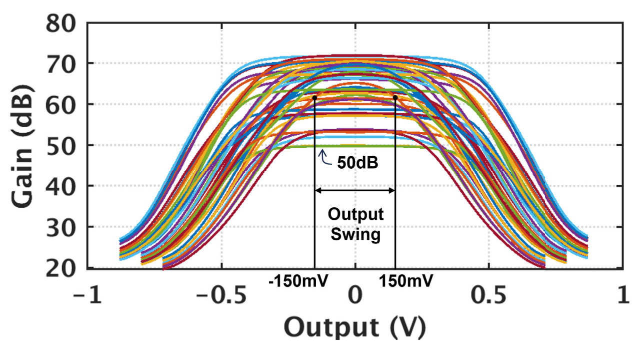


Fig. 12. SQNR vs. gain of amplifier (based on the system modeling in SIMULINK).



(a)



(b)

Fig. 13. (a) The proposed cascoded LVFIA; (b) The simulated output swing of the cascoded LVFIA over PVTs (TT/FF/SS/FS/SF, 0.72V/0.80V/0.88V, −40°C/25°C/85°C).

C. Timing

The timing diagram of the proposed DSM is illustrated in Fig. 14. The $\phi_{1,2}$ are sampling clocks, and $\phi_{1A,1B}$ are reset/AZ clocks for input transistors, while $\phi_{1A',1B'}$ are for cascode transistors of the amplifier. As mentioned before, the auto-zero frequency (f_{AZ}) of $\phi_{1A,1B}$ is restricted by the leakage current. Trading off between accuracy and power consumption, f_{AZ} is chosen to be $f_s/16$ to periodically refresh the bias voltages of input transistors $M_{1,2}$. Since the cascode transistors $M_{3,4}$ also function as switches ($S_{8,9}$), the frequency of $\phi_{1A',1B'}$ is set to f_s to avoid long-time charge sharing between $C_{1,2}$ and the gate parasitic capacitors of $M_{3,4}$. To further reduce the thermal noise aliasing caused by auto-zero in the LVFIA, the chopper stabilization technique [31] is used and the frequency of $\phi_{C1,C2}$ is set to $f_s/2$.

V. Measurement Results

A prototype of the LVFIA-based DTDSM is fabricated in a 130nm process and occupies an active area of $0.26mm^2$ (Fig. 15). During the measurement, the reference voltage is generated off-chip, and the input signal is provided by the high-quality audio signal source APx555. The $sinc^2$ decimation filter is implemented off-chip for flexibility.

Fig. 16 shows an output spectrum when the ADC operates at 1.5MHz f_s with a 0.8V supply. Measured with a −0.82dBFS (0.91Vpeak) 1kHz sinusoidal input and an OSR of 128, it achieves a SNDR of 89.8 dB within a 5.9kHz BW. Fig. 17 depicts the SN(D)R as a function of input amplitude, showing a DR of 91.6dB.

Thanks to the proposed fully dynamic LVFIA, the DSM exhibits a 2.5nW/Hz linear power/BW scalability from 2.0μW to 50.1μW over a 165kHz-5MHz f_s at a 0.8V supply

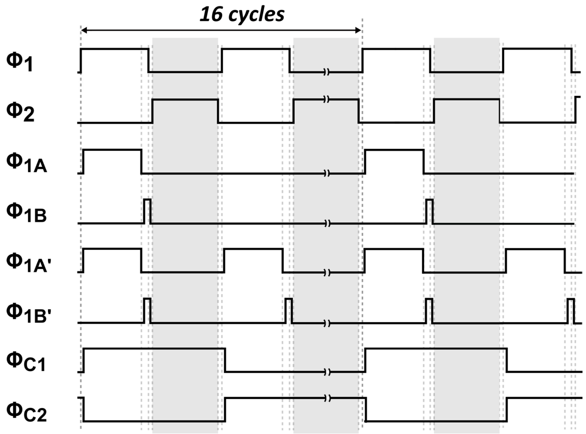


Fig. 14. Timing diagram of the proposed delta-sigma modulator.

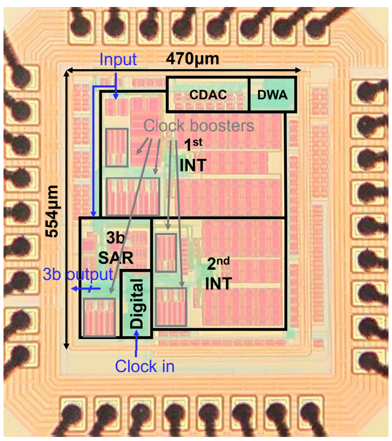


Fig. 15. Die micrograph.

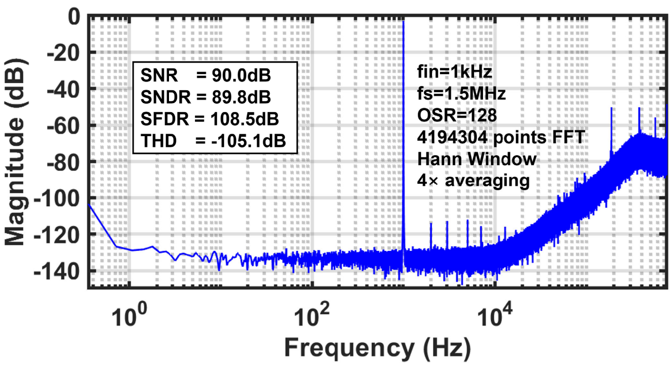


Fig. 16. Measured spectrum at 1.5MHz f_s.

(Fig. 18(a)). Noticing that 59% of the power is dissipated by digital logic in 130nm CMOS. Fig. 18(b) shows that the DSM achieves a consistent SNDR of >86.5dB over a ×30 scaling range of f_s with a 0.8V supply. The scaling range is limited by the amplifier's settling speed and leakage at high and low frequencies, respectively. The Schreier FoM variation with f_s is also shown in Fig. 18(b) demonstrating a stable FoMs of >171dB over the scaling range of f_s.

Fig. 19 shows the SN(D)R variation with input signal frequency when f_s is 1.5MHz. To demonstrate the robustness, the DTDSM was measured with supply varying from 0.7V to

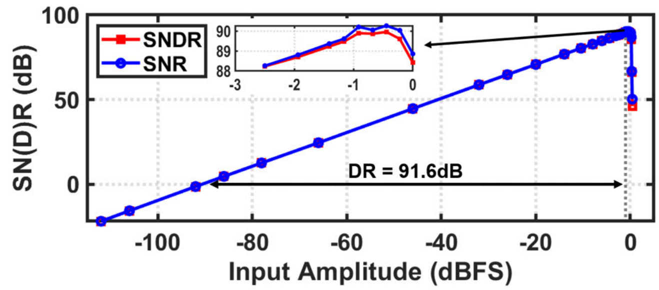


Fig. 17. Measured SNDR/SNR vs. input amplitude.

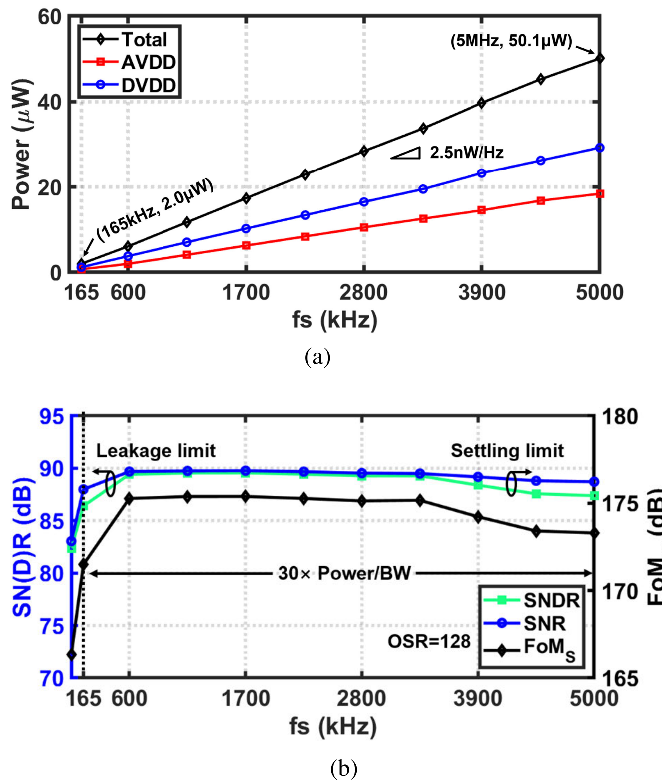


Fig. 18. (a) Measured power consumption vs. f_s when f_{in} = 50Hz. (b) Measured SNDR/SNR/FoMs vs. f_s when f_{in} = 50Hz.

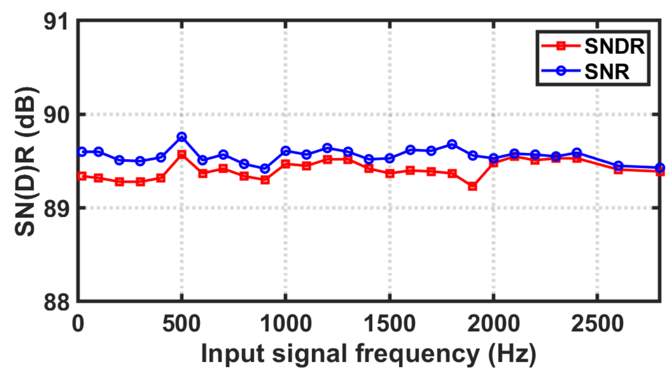


Fig. 19. Measured SNDR/SNR vs. f_{in} when f_s = 1.5MHz.

1.2V and a fixed input amplitude. The SN(D)R variation is within 0.2(0.3) dB over the supply range of 0.75V to 1.2V, as shown in Fig. 20. The measured SN(D)R versus temperature

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	This work	JSSC'22 [5]	JSSC'22 [17]	TCASII'22 [18]	TCASII'23 [6]	TCASII'23 [19]
Technology (nm)	**130**	180	180	65	55	65
Area (mm²)	**0.26**	0.75	0.8	0.04	0.5	0.048
Architecture	**DTDSM**	DTDSM	DTDSM	DTDSM	Zoom ADC	DTDSM
Amplifier	**Cascoded LVFIA**	SEFIA	Cascoded FIA	2-stage cascoded FIA	SEFIA with CLS	CLS-assisted FIA with SNC
Power/BW Scalable	**30×** (0.64kHz-19.5kHz) (2.0μW-50.1μW)	4× (0.4kHz-1.6kHz) (2.2μW-7.0μW)	2× (24kHz-48kHz) (~340μW-680μW)	2.5× (7.8kHz-19.5kHz) (~20.5μW-43.5μW)	1250× (10Hz-12.5kHz) (453nW-122μW)	2.5× (7.8kHz-19.5kHz) (~36μW-79μW)
Supply (V)	**0.8**	1.5	1.8	1.0	1.2	1.2
OSR	**128**	125	64	256	125	256
DR (dB)	**91.6***	94.1	98	91.7	97.3	92.0
SNDR (dB)	**89.8***	89.3	96.2	88.5	96.3	94.8
FoM_{SNDR}[1] (dB)	**175.7***	172.3	174.7	175.0	176.1	178.7
FoM_W[2] (fJ/conv-step)	**51.3***	104.8	134.2	51.2	98.0	45.2

* $Measured\ at\ f_s = 1.5MHz\ (BW = 5.9kHz,\ power = 15.3\mu W)$ [1] $FoM_{SNDR} = SNDR + 10 \cdot log_{10}(\frac{BW}{power})$ [2] $FoM_W = \frac{power}{2^{ENOB} \cdot 2 \cdot BW}$

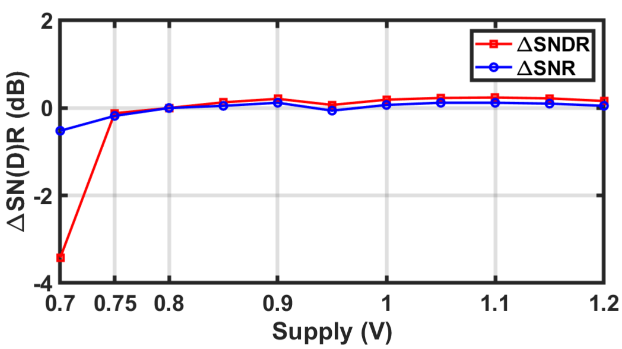


Fig. 20. Measured Δ SNDR/SNR vs. supply voltage when $f_s = 1.5$MHz.

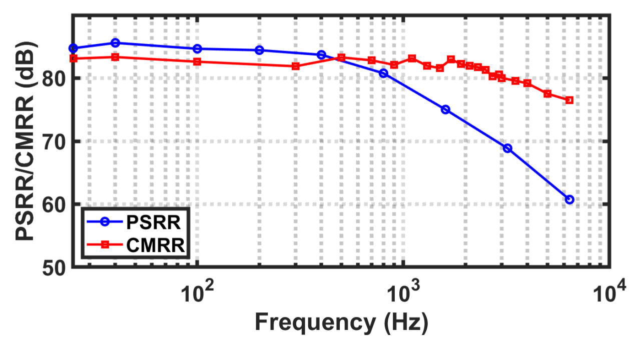


Fig. 22. Measured PSRR/CMRR vs. frequency.

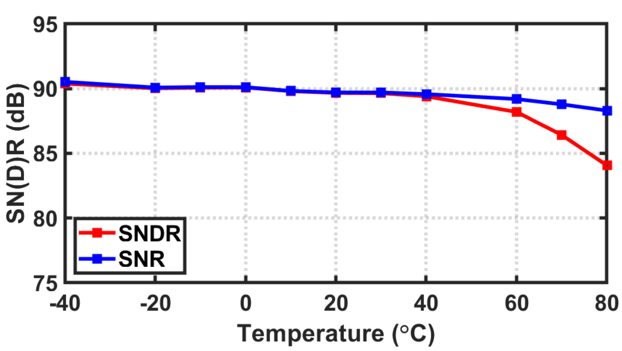


Fig. 21. Measured SNDR/SNR vs. temperature when $f_s = 1.5$MHz.

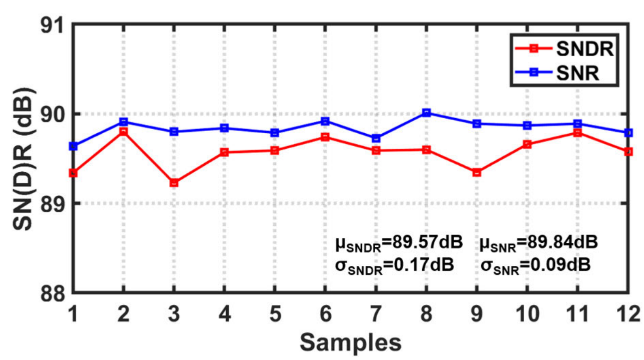


Fig. 23. Measured SNDR/SNR of different chips when $f_s = 1.5$MHz.

result is shown in Fig. 21. Due to increased leakage, the performance slightly degrades at higher temperatures.

Fig. 22 shows the measured power-supply rejection ratio (PSRR) for a 100-mV sine-wave signal superimposed on 0.9V DC supply voltage, as well as the measured common-mode rejection ratio (CMRR). The PSRR reaches 85.6dB at 40Hz and stays above 80dB over an 800Hz BW without external decoupling capacitors. The CMRR reaches 83.3dB at 40Hz and remains above 80dB over a 3000Hz BW. 12 chips from one batch were measured under a 0.8V supply and a 1.5MHz f_s. The averaged SN(D)R is 89.84 (89.57) dB, while the standard deviation is 0.09 (0.17) dB (Fig. 23).

Table I summarizes the performance of this work and compares it to state-of-the-art high-resolution (~90dB) power/BW scalable DSMs with a similar BW. This work is the only sub-1V power/BW scalable DSM in the table thanks to the proposed LVFIA. Compared to the DTDSM with cascoded

FIA in [17] and SEFIA in [5], this work reduces the supply voltage by >1.8 and increases the bandwidth scaling range by >7.5 even with a lower supply. Despite the lower maximum input signal amplitude due to the reduced supply voltage of 0.8V, the proposed DTDSM achieves a competitive FoM_w of 51.3fJ/conv-step and a FoM_{SNDR} of 175.7dB, making it suitable for low-voltage and low-power applications.

VI. Conclusion

In this paper, a fully dynamic LVFIA is proposed, which can operate at a sub-1V supply. Its bias current is defined in a relatively supply-independent manner and is auto-controlled by operating frequency to extend the power/BW scalability. Based on the LVFIA, a sub-1V DSM is proposed which achieves fully dynamic operation and high resolution, resulting a ~90 dB SNDR over a 30× power/BW scalable range.

Appendix
Detailed Analysis of the Average Transconductance of the LVFIA

To obtain the average transconductance $G_{m,avg}$ of LVFIA, we need to get the expression of the instantaneous transconductance $G_m(t)$. Assuming the input signal is zero for simplification, Fig. 24 shows the single-ended equivalent circuit during the amplification phase of the LVFIA. This also holds for the FIA when the $V_{BP} = V_{BN} = V_{CM}$. We can split the capacitor C_{RES} into two series-connected capacitors to obtain a midpoint V_S with constant voltage [17]. Additionally, we assume that the transconductances of the PMOS and NMOS satisfy:

$$G_{mp}(t) = G_{mn}(t) = G_{m,half}(t) = \frac{G_m(t)}{2}. \tag{8}$$

The discharge equation of capacitors is given by:

$$I(t) = -2C_{RES}\frac{dV_{S+}(t)}{dt}. \tag{9}$$

According to the different operation regions of LVFIA at higher f_s and lower f_s, we consider the following two cases:

a. The MOSFET operates in the saturation region in the most of amplification time:

The square law of current in the saturation region is:

$$I(t) = \frac{1}{2}\mu C_{OX}\frac{W}{L}(V_{S+}(t) - V_{BP} - |V_{THP}|)^2 \tag{10}$$

where μ is the carrier mobility and C_{OX} is the gate oxide capacitance per unit area. By combining equations (9) and (10), along with the initial condition $V_{S+}(0) = V_{DD}$, we obtain

$$V_{S+}(t) = V_{BP} + |V_{THP}| + \frac{1}{(\frac{\mu C_{OX}\frac{W}{L}}{4C_{RES}})t + 1/(V_{DD} - V_{BP} - |V_{THP}|)}. \tag{11}$$

Then, the instantaneous transconductance in the saturation region is

$$G_{m,half,s}(t) = \frac{1}{\frac{t}{4C_{RES}} + \frac{1}{G_{m,half,s}(0)}} \tag{12}$$

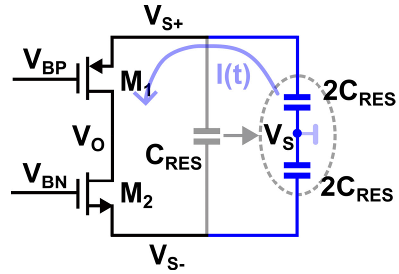


Fig. 24. The single-ended equivalent circuit of the LVFIA during the amplification phase.

where $G_{m,half,s}(0)$ is the transconductance at the beginning of the amplification phase:

$$G_{m,half,s}(0) = \mu C_{OX}\frac{W}{L}(V_{DD} - V_{BP} - |V_{THP}|). \tag{13}$$

And the average transconductance will be

$$G_{m,avg,s} = 16C_{RES}f_s \cdot ln(1 + \frac{G_{m,s}(0)}{16C_{RES}f_s}). \tag{14}$$

b. The MOSFET operates in the subthreshold region during the amplification phase:

The current equation in the subthreshold region is given by:

$$I(t) = \mu C_{OX}\frac{W}{L}(n-1)V_T^2 exp(\frac{(V_{S+}(t) - V_{BP} - |V_{THP}|}{nV_T}) \tag{15}$$

where n is the slope factor in weak inversion and V_T is the thermal voltage kT/q. Combining equations (9) and (15), we obtain the instantaneous transconductance in the subthreshold region:

$$G_{m,half,w}(t) = \frac{1}{\frac{t}{2C_{RES}} + \frac{1}{G_{m,half,w}(0)}} \tag{16}$$

where $G_{m,half,w}(0)$ is the transconductance at the beginning of the amplification:

$$G_{m,half,w}(0) = \frac{\mu C_{OX}\frac{W}{L}(n-1)V_T^2 exp(\frac{(V_{DD} - V_{BP} - |V_{THP}|)}{nV_T})}{nV_T}. \tag{17}$$

And the average transconductance will be

$$G_{m,avg,w} = 8C_{RES}f_s \cdot ln(1 + \frac{G_{m,w}(0)}{8C_{RES}f_s}). \tag{18}$$

Therefore, for both cases, the average transconductance $G_{m,avg}$ of the LVFIA is

$$G_{m,avg} = aC_{RES}f_s \cdot ln(1 + \frac{G_m(0)}{aC_{RES}f_s}) \tag{19}$$

where a is 16 for the saturation region and 8 for the subthreshold region.

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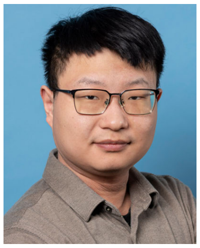
Xinjie Wu (Graduate Student Member, IEEE) received the B.E. degree in electronic science and technology from Zhejiang University, Hangzhou, China, in 2021, where she is currently pursuing the Ph.D. degree with the College of Integrated Circuits. Her current research interests include low-power analog and mixed-signal circuits design.



Yuyan Liu (Graduate Student Member, IEEE) received the B.E. and Ph.D. degrees from Zhejiang University, Hangzhou, China, in 2018 and 2023, respectively. In August 2023, he joined Delft University of Technology, Delft, The Netherlands, as a Post-Doctoral Researcher with the Faculty of Electrical Engineering, Mathematics and Computer Science (EEMCS). His research interests include low-power data converters and mixed-signal circuits and systems.

Zhangming Zhu received the M.S. and Ph.D. degrees in microelectronics from Xidian University, Xi'an, China, in 2001 and 2004, respectively. He is currently a Professor with the School of Microelectronics, Xidian University. His research interests include CMOS data converters, analog-front end, low power mixed-signal, and RF integrated circuits.

Xiaopeng Yu (Member, IEEE) received the B.Eng. degree in optical engineering from Zhejiang University, Hangzhou, China, in 1998, and the Ph.D. degree from the School of Electrical and Electronic Engineering, Nanyang Technological University (NTU), Singapore, in 2006.

From 2000 to 2002, he was an Engineer with MOTOROLA's Global Telecom Solutions Sector, Hangzhou, and a Research Staff Member with NTU, from 2005 to 2006. Since 2006, he has been with the Institute of VLSI Design, Zhejiang University, where he holds the position of a Qiushi Distinguished Professor. He further expanded his academic horizons as a Visiting Scholar with Eindhoven University of Technology (TU/e), Eindhoven, The Netherlands, from 2008 to 2010, and a Marie Curie Fellow with the Mixed Signal Microelectronics Group, TU/e, a role co-hosted with Philips Research, Eindhoven. His research interests include the design and development of analog, mixed-signal, and radio frequency integrated circuits.

Nick Nianxiong Tan (Senior Member, IEEE) received the B.Eng. and M.Eng. degrees from Tsinghua University, Beijing, China, in 1988 and 1991, respectively, and the Ph.D. degree from Linköping University, Linköping, Sweden, in 1994.

He is currently a Full Professor with Zhejiang University, Hangzhou, China, and the Chairperson of Vango Technologies, Inc., Hangzhou, a fabless semiconductor company for the Internet of Energy. Prior to starting up Vango Technologies, Inc., he was the Founder and the CEO of AnaLutions, Inc., Laguna Niguel, CA, USA, a chip design service company. He also was a Design Director at GlobeSpan (a Bell lab spinoff), Red Bank, NJ, USA, and with the Ericsson's Research and Development Center, Stockholm, Sweden. He taught mixed-signal chip design and supervised Ph.D. students at Linköping University. He is an Accomplished Chip Designer and a Researcher with an interest in mixed-signal chip design and agile design methodologies. He holds 32 U.S. patents and numerous Chinese patents. In addition, he has written three books and book chapters and published over 100 articles.

Zhong Tang (Member, IEEE) received the B.S. and Ph.D. degrees in electrical engineering from Zhejiang University, Hangzhou, China, in 2015 and 2020, respectively.

From 2019 to 2020, he was a Visiting Ph.D. Student with the EEIC Group, Eindhoven University of Technology, Eindhoven, The Netherlands. From 2020 to 2023, he was a Post-Doctoral Researcher with the Electronic Instrumentation Laboratory, Delft University of Technology, Delft, The Netherlands. He is currently an Analog IC Designer with Vango Technologies Inc., Hangzhou. His research interests include precision analog and mixed-signal integrated circuits. This has led to over 40 technical articles, including 8 from the IEEE International Solid-State Circuits Conference (ISSCC) and seven from the IEEE JOURNAL OF SOLID-STATE CIRCUITS (JSSC).

Dr. Tang was a recipient of the Outstanding Doctoral Thesis Award of the Chinese Institute of Electronics in 2022.