Interface Properties of Group-III-Element Deposited-Layers Integrated in High-Sensitivity Si Photodiodes

Lin QI

齐麟

Interface Properties of Group-III-Element Deposited-Layers Integrated in High-Sensitivity Si Photodiodes

Proefschrift

ter verkrijging van de graad van doctor
aan de Technische Universiteit Delft,
op gezag van de Rector Magnificus prof.ir. K.C.A.M. Luyben;
voorzitter van het College voor Promoties,
in het openbaar te verdedigen op
maandag 18 januari 2016 om 15:00 uur

door

Lin QI

Elektrotechnisch ingenieur, Technische Universiteit Delft
geboren te Changchun, China

This dissertation has been approved by the
promotor: Prof.dr. L.K. Nanver

Composition of the doctoral committee:

Rector Magnificus	chairman
Prof.dr. L.K. Nanver	Delft University of Technology

Independent members:

Prof.dr. E. Charbon	Delft University of Technology
Prof.dr. H. Radamson	KTH Royal Institute of Technology
Prof.dr. J. Schmitz	University of Twente
Prof.dr. J.N. Burghartz	University of Stuttgart
Prof.dr. T. Suligoj	University of Zagreb
Dr. G.N.A. van Veen	FEI Company
Prof.dr. L.C.N. de Vreede	Delft University of Technology, reserve member

Lin Qi,
Interface Properties of Group-III-Element Deposited-Layers Integrated in High-Sensitivity Si Photodiodes,
Ph.D. Thesis, Delft University of Technology,
with summary in Dutch

This research was funded by the Huygens Scholarship Programme, Ministry of Education, Culture and Science, The Netherlands.

ISBN 978-94-6203-978-0

Printed by CPI, Wöhrmann Print Service, Zutphen, The Netherlands

To my family

Content

Chapter 1
Introduction

In the developments of the semiconductor industry over the last decade, many efforts have been devoted to the themes “More-than-Moore” and “Beyond-Moore” in a search for alternative logic building blocks and new materials to enhance Si CMOS (Complementary Metal-Oxide Semiconductor) IC (Integrated Circuit) technology [1]. Nevertheless, in the foreseeable future purely Si CMOS will no doubt remain the dominant technology defining the mainstream semiconductor industry. Therefore, it is a standing truth that it is worthwhile investing in making new devices CMOS compatible. The work presented in this thesis continues research on the recently developed PureB photodiodes in an effort to increase their applicability and also compatibility with CMOS. These photodiodes have become important for the detection of low-penetration-depth photons and particles in Si, such as photons in the ultraviolet range and low-energy electrons. Both these applications have already been commercialized and interest from other application areas is continually increasing from both inside and outside the field of semiconductors. In this thesis the focus is on the basic ultrashallow junction that is formed by depositing PureB [2] on Si and how it can be incorporated in CMOS-compatible (photo)diodes either as a front-end or back-end module. The work includes design, fabrication, characterization and modeling of new devices as well as specially developed test structures.

To detect low-penetration-depth beams in Si, the photo-sensitive region of the detector should be as close to the irradiated surface as possible. In principle, Schottky diodes can form the shallowest photodiodes since the light-sensitive depletion region extends right up to the metal-contacting of the silicon surface. However, Schottky diodes are often an unattractive solution since the reverse leakage current and surface recombination can be high. As an alternative, diffused junctions can offer much lower dark currents but combining this with an ultrashallow junction depth has proven to be challenging. The most common technique used to form n^+/p^+ ultrashallow junctions and contacts in the

semiconductor device fabrication industry is high-dose, low-energy As^+/B^+ (and/or BF_2^+) ion implantation in combination with a high-temperature, short-time rapid thermal annealing (RTA) process. However, transient enhanced diffusion (TED) induced by the defects caused by implantation damage can seriously affect the doping profile and the performance of the devices. The defects can act as generation-recombination centers, particularly if those situated within the depletion region are not annealed out, and this will increase junction leakage current [3]. Other doping methods, for example during Si epitaxy, have also been investigated but the combination of ultrashallow junction depth with low dark current and robustness during irradiation has not been successfully demonstrated for low-penetration-depth beams. In fact, recent publications reviewing the properties and status of photodiode detectors for the 1 nm to 400 nm wavelength range, have concluded that PureB photodiodes offer the only technology that combines high-sensitivity with high-robustness over the whole spectral range [4, 5].

The Si p^+-n ultrashallow junctions that can be fabricated with PureB technology have excellent properties both electrically and optically. This technology was developed in the Silicon Device Integration Group over the last 10 years. The term PureB refers to the pure boron layer that is the central element in the technology. In short, this layer is deposited by chemical vapor deposition (CVD) on a clean Si surface. Nanometer-thin pure boron layers can be reliably formed at temperatures from 400 °C to 700 °C and at atmospheric or reduced pressure. Subsequent *in-situ* drive-in and higher-temperature thermal annealing are also possible but even without driving the boron dopants into the Si it is possible use PureB as p^+-regions to fabricate near-ideal, high-quality, extremely ultrashallow p^+-n junction photodiodes for which the saturation current can be tuned from high Schottky-like levels to low deep-junction-like levels [6]. Besides forming a p^+-region at the silicon interface, the PureB layer deposited on the Si surface can also be used as a robust front-entrance window with a minimum of beam attenuation. All of these properties allow the shallow-penetration photons/particles to reach the sensitive region of the diode and generate a high response to the signal.

PureB photodiodes are a particularly attractive solution for the detection of low-penetration-depth beams in Si such as vacuum-UV (VUV) light and low-energy electrons with energies smaller than 1 keV. The penetration depths in Si are only a few nanometers so high sensitivity demands that the photosensitive

region extends close to the Si surface which is the case for PureB devices. Besides high-sensitivity, the PureB diodes also offer low noise levels and high stability. The sensitivity can be increased to single-photon/-electron counting capability by designing single-photon avalanche diodes (SPADs). The diode then operates well beyond the breakdown voltage and even a single photon or electron can initiate an avalanche current. This thesis includes the development of the first PureB Si SPADs. Up until this work, the focus was on mm-large photodiodes, the contacting of which is not suitable for the micrometer-sized photodiodes needed for SPAD operation. To preserve low noise combined with high fill-factor for such small photodiodes, alternative post-PureB processing steps were investigated and implemented.

With the goal of enabling a PureB process module that could be added to fully-processed wafers from a CMOS foundry, this thesis work also included a more detailed study of the properties of PureB deposition at low temperatures down to 400 °C. It was experimentally verified that 400 °C PureB could be deposited after metallization and still form diodes with a sensitivity equal to that of the 700 °C devices. This is quite surprising considering that the 400 °C deposition is not able to dope the bulk Si. To get a better understanding of the PureB-to-Si interface properties that might explain this behavior special test structures were developed to study the current flows through the PureB region. Beside different diode configurations, bipolar structures and sheet resistance test structures to monitor the lateral conductance along the interface were also designed and fabricated.

In the following sections of this introductory chapter, first an overview of semiconductor photodetectors based on *p-n* junction photodiodes is provided with focus on the fundamental operation principles, characteristics and specific qualities of different photodiode technologies. Second, the fundamental limits of detection for low-penetration-depth particles in Si, such as photons and low-energy electrons, when using Si photodiodes are discussed. Lastly, an overview is given of the status of PureB technology research in relationship to the properties that enable the fabrication of *p-n* junction photodiodes with outstanding performance.

1.1 Si *p-n* Junction Photodetectors

Silicon *p-n* junctions are one of the most elementary building blocks in semiconductor electronic devices such as diodes, transistors and light-emitting diodes (LEDs). To form a *p-n* junction, a counter doping is created in the Si. For example, a *p*-type doping can be created on an *n*-type Si layer by dopant diffusion, ion implantation/annealing or by epitaxy.

A *p-n* diode is formed by contacting a *p-n* junction as schematically shown in Fig. 1.1 along with the corresponding circuit symbol and typical *I-V* characteristics. When there is no bias applied to the *p-n* diode, the band diagram is as shown in Fig. 1.2(a). The *p*- and *n*-regions are joined together so that electrons and holes can cross the junction to establish a thermal equilibrium status with a depletion region (space charge region) providing band bending. The built-in electric field over the depletion region will form a barrier to hold back the majority holes and electrons inside *p*- and *n*-regions, respectively. When under forward bias as in Fig. 1.2 (b), the applied forward bias will lower of the barrier height and make the depletion region narrower so that holes in the *p*-region can be injected across the depletion region into the *n*-region, diffuse into the *n*-region and finally recombine with electrons there, and vice versa for electrons in the *n*-region. As long as forward bias is applied, this injection and diffusion process will continue, producing a diffusion current. When the *p-n* diode is under reverse bias as in Fig. 1.2(c), the barrier height is increased and the depletion region gets wider. The high electric field drives holes and electrons into the *p*- and *n*-regions, respectively. Holes and electrons generated inside the depletion region due to generation-recombination centers will also be swept away to the *p*- and *n*-regions, causing a generation current. When the applied reverse bias is high enough, the barrier width becomes so thin that the holes and electrons can be injected through the depletion region, which is a tunneling effect. If the reverse bias voltage keeps increasing further, at some point, the device will break down and the reverse current will increase rapidly. The generation process cannot only be induced by generation-recombination centers, but also by a trigger from outside such as an incident photon or electron. This induces extra current, i.e., photodetection is achieved with the *p-n* diode, normally with the device under zero or reverse bias. A more detailed discussion of the carrier transport processes in a diode under reverse biasing will be given in Chapter 5 in connection with Fig. 5.4.

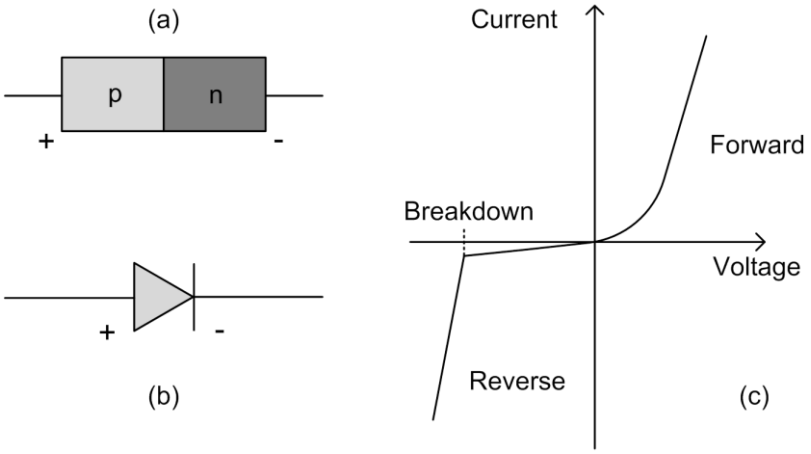


Fig. 1.1. (a) Schematic cross section of a *p*-*n* diode, (b) corresponding circuit symbol and (c) *I*-*V* characteristics.

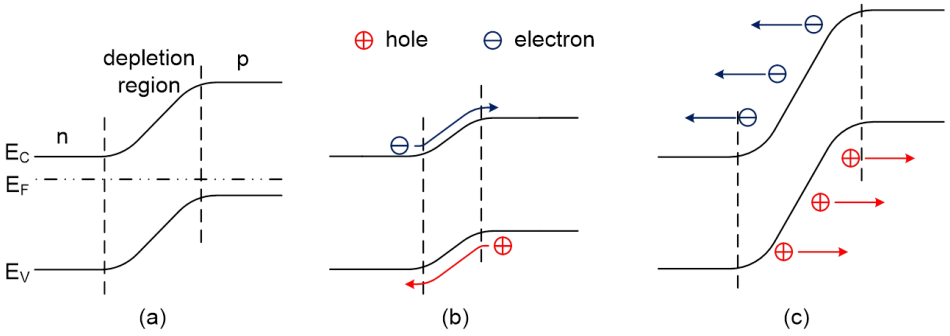


Fig. 1.2. Band diagram of a *p*-*n* junction under (a) zero bias, (b) forward bias and (c) reverse bias. Carrier flows are indicated.

1.1.1 *p(i)n* photodiodes

A photodiode responds to light by generating current. The junctions can be used with either a *p*–*n* or *p*-*i*-*n* structure. When a photon with sufficient energy strikes the diode, it generates an electron-hole pair as illustrated in Fig. 1.3. The electron and hole will be swept into the *n*- and *p*-regions by the electric field in the depletion region thus creating a generation current. This mechanism is also known as the inner photoelectric effect. If the generation rate G_L of electron-hole pairs is constant, the light-induced current density J_L can be defined as:

$$J_L = eG_L W \tag{1.1}$$

where e is the elementary charge and W is the width of depletion region. The generation rate G_L as a function of x, the distance into the material from the surface, can be expressed as [7]:

$$G_L(x) = \Phi_0 \alpha \exp(-\alpha x) \tag{1.2}$$

where Φ_0 is the incident photon flux at the surface, α is the absorption coefficient.

When a photon strikes the diode, if an electron-hole pair is generated inside the depletion region or within about one diffusion length from the edge of depletion region, it can contribute to the light-induced current. With a *p-i-n* photodiode as shown in Fig. 1.4, an intrinsic region is formed between the *p*- and *n*-regions. When the device is under reverse or even zero bias, the intrinsic region can be fully depleted which means that the depletion region can be made much wider. In this way the detection probability is increased and a higher light-induced current density J_L results.

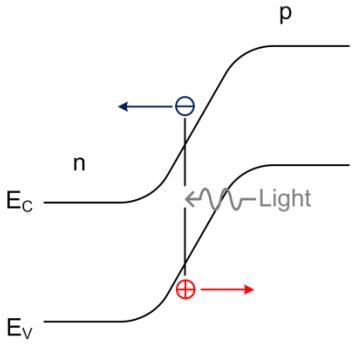


Fig. 1.3. Illustration of electron-hole pair generation induced by an incident photon.

Fig. 1.4. Schematic cross section of a *p-i-n* photodiode.

1.1.2 Avalanche photodiodes

A photodiode is normally under zero bias or small reverse bias, but if higher sensitivity is needed, it can be further reverse biased to increase the electric field. When the localized electric field is large enough, about 10^5 V/cm [8], the

generated electrons and/or holes acquire sufficient energy to ionize other atoms and generate new electron-hole pairs. These newly generated electrons and/or holes can continue this process as shown in Fig. 1.5, and thus the impact-ionization process becomes an avalanche-multiplication process. The photodiode then works as an avalanche photodiode (APD), a highly-sensitive photodiode that has been widely used in many applications such as in Laser Detection and Ranging (LADAR) systems and range finding, free-space optical communication, optical time domain reflectometry and confocal microscopy.

The avalanche photodiode has a current gain introduced by the avalanche multiplication factor *M*, which has been empirically defined as [9]:

$$M = \frac{1}{1-\left(\frac{V_R}{V_{BD}}\right)^m} \tag{1.3}$$

where V_R is the reverse applied voltage, V_{BD} is the breakdown voltage and *m* is a constant depending on the material and temperature. In general, the higher the reverse bias, the higher the multiplication factor. Typical values of the multiplication factor are at least 100 for Si avalanche photodiodes [10].

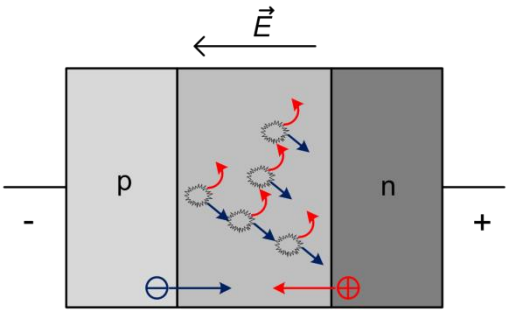


Fig. 1.5. Impact ionization process in a reverse biased *p-n* junction.

1.1.3 Single-photon avalanche diodes

If very high gain (10^5 to 10^6) and sensitivity is needed, some avalanche photodiodes can be reverse biased even further, beyond the breakdown voltage, without introducing an avalanche-multiplication process. In this working region, the device is so sensitive that an avalanche breakdown can be triggered by the electron-hole pairs generated by just one single photon. Therefore this kind of

avalanche photodiode is also called a single-photon avalanche diode (SPAD). Since the working mechanism is similar to that of a Geiger-Muller counter [11], the SPAD operation mode is also called Geiger-mode, and a SPAD is also known as a Geiger-mode APD or G-APD.

In Fig. 1.6 the basic circuit is shown for operating the SPAD in Geiger-mode with passive quenching and passive recharge via a ballast resistor R_Q. The device is biased above breakdown (V_{BD}) by a voltage known as the excess bias (V_{EB}) so that the operating voltage is $|V_{OP}| = |V_{BD}| + V_{EB}$. With the resulting high electrical field, an avalanche event can be triggered by an incoming photon or an internal mechanism.

When the operation voltage is above the breakdown voltage, as shown in Fig. 1.7, the electric field is very high, the device is very sensitive and ready to response to any trigger from the outside or inside. When a light signal comes, the incident photons will trigger an avalanche breakdown. To stop the avalanche a passive quenching circuit can be used where the high avalanche current is passed through R_Q, creating a voltage drop over the resistor that brings the voltage across the diode below breakdown. This stops the avalanching and the diode biasing is restored to the initial values, and a new incoming photon can be detected. This cycle takes an average time known as the dead time. The avalanche pulses are sensed using a comparator with an appropriate threshold voltage V_{th}, thus converting the Geiger pulses into digital signals for photon counting. An oscilloscope image of the Geiger pulse is shown in Fig. 1.8 when the output is connected to an oscilloscope.

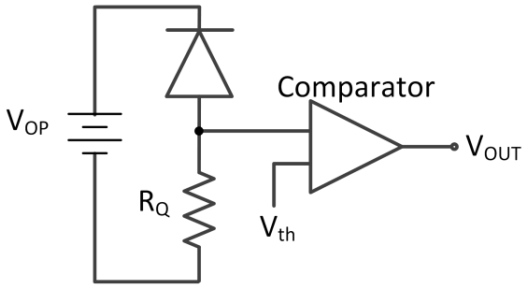


Fig. 1.6. Electronic circuit schematic of a SPAD with passive quenching and passive recharge.

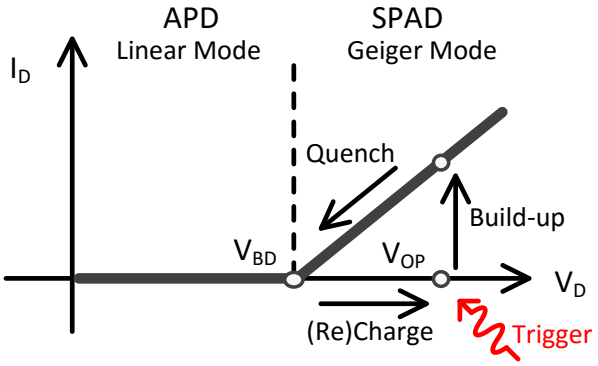


Fig. 1.7. Reverse *I-V* characteristics of APD operation and SPAD operation with a working cycle in Geiger-mode.

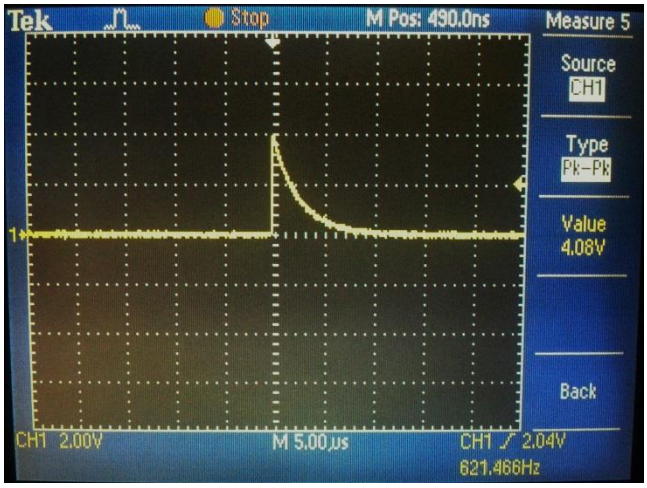


Fig. 1.8. An oscilloscope image of a Geiger pulse.

When a photodiode works below the breakdown voltage, the total current through the photodiode is the sum of the dark current (current that is generated in the absence of light) and the photocurrent, so the dark current must be minimized to maximize the sensitivity of the device [12]. When the device is biased above the breakdown voltage and works in Geiger-mode, the counts induced by internal mechanisms in the absence of light must be suppressed as much as possible and they should not surpass the counts induced by the incident signal. To achieve a good situation in this respect it is desirable to have photodiodes with as few as possible defects. In this thesis, the design and

fabrication of near-ideal, defect-free PureB photodiodes and very low-noise-level single-photon avalanche diodes will be studied and discussed.

1.2 Detection of Low-Penetration-Depth Irradiation Beams in Si

To detect a signal radiated on a Si surface, the radiation should, for the first, have sufficient energy to be absorbed in Si and generate an electron-hole pair. Otherwise, if the energy is too low, the radiation will see Si as transparent and go through it. Secondly, the radiation has to arrive within about one diffusion length away from the edge of the depletion region, from where the generated electrons or holes outside the depletion region can be swept to the depletion region and collected by the cathode or anode. Last but not least, the response to the radiation should be large enough to be distinguished from noise sources.

To detect irradiation in Si for which the penetration depth is only a few nanometers to tens of nanometers, the depleted region of the junction that detects the radiation should be located close to the Si surface, for the first, to maximize the collectable electron-hole pairs that are induced by the incident radiation. Secondly, a junction close to the surface can significantly increase the percentage of electron-hole pairs generated in the depletion region, which will benefit to the response time since the carriers can be collected more quickly. Moreover, the high electric field that extends from the metallurgical junction can separate the electron-hole pairs generated in this diffused area more efficiently. In this thesis, work has been performed to enhance the capabilities of Si-based photodiode detectors for detection of photons in the ultraviolet wavelength range and low-energy electrons with energy below 1 keV, the penetration depth (attenuation length) of which is only a few nanometers in Si.

1.2.1 UV light detection

In recent years, there has been a significant interest in the development and fabrication of highly-sensitive robust ultraviolet (UV) detectors in the wavelength range of 10 ~ 400 nm, especially in the vacuum UV (VUV) wavelength range from 10 to 200 nm. This has been mainly driven by the development of advanced lithography systems that employ these UV detectors to sense and monitor position and beam intensity. Nowadays, high-volume

lithography systems are using 193 nm ArF beams to reach the 10-nm CMOS technology node with immersion wafer-scanner technology, and in the future, systems using extreme UV light (EUV, 13.5 nm in wavelength) are under development to be introduced in mass production from the 7-nm technology node. Besides advanced lithography systems, UV light is also being used in many other fields such as disinfection, DNA sequencing, drug discovery, and medical imaging of cells [13].

UV light generally has a lower penetration-depth in Si than visible light (390 to 700 nm in wavelength) as shown in Fig. 1.9. For the deep UV (DUV) light around the 100 ~ 300 nm wavelength range, the penetration in Si is only a few nanometers. It goes down to an attenuation length of ~ 5 nm for the important lithography wavelength of 193 nm and a minimum of ~ 3 nm is reached at wavelengths around 280 nm. To detect this low-penetration-depth light in Si, the photosensitive region has to be really close to the surface to enable an efficient collection of generated electron-hole pairs.

For many applications in the UV range, the detectors have to work in a harsh environment where the radiation-sensitive area is exposed to high photon flux doses. They should also withstand the *in-situ* cleaning steps used to prevent the degradation caused by the surface and bulk contamination. Therefore, besides a junction close to the surface, a Si *p-n* detector is also required to have high ruggedness and long-term stability [14]. All in all, a robust Si device with shallow junctions, high responsivity and uniformity, low noise and excellent reliability is highly desirable.

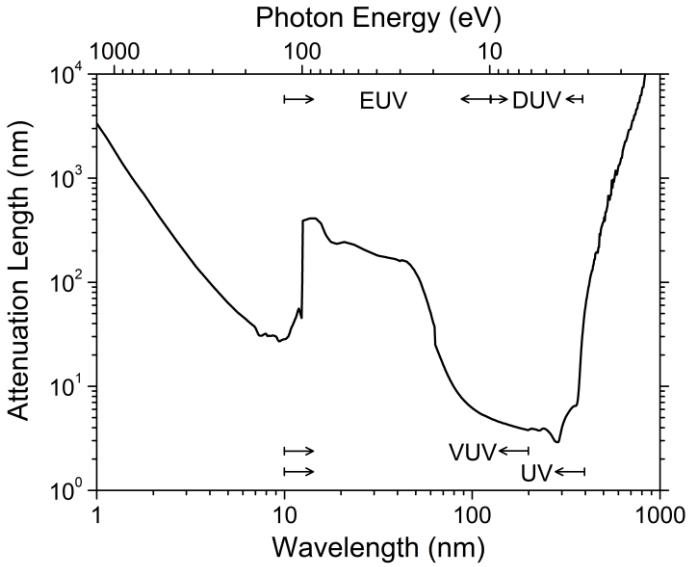


Fig. 1.9. Attenuation length in Si as a function of wavelength. The data is taken from [15, 16]

1.2.2 Low-energy electrons detection

Low-energy particle detection has been used in many fields such as electron microscopy, space plasma physics, etc. [17, 18, 19, 20, 21]. Especially the detection of low-energy electrons in electron microscopy has received much attention in recent years, initially due to the requirements of the semiconductor industry that demanded atomic-scale imaging of nm-sized structures. When electrons with sufficient energy impinge upon a solid surface, a series of phenomena occur that may lead to emission of different types of particles as show in Fig. 1.10: elastically and inelastically backscattered electrons (BSE), excitons, phonons, plasmon excitations, photoelectrons, Auger recombination of holes left by photoelectrons, fluorescence recombination and the so-called secondary electrons. Many of these phenomena carry information on the topographical and compositional properties of the impinged matter. The detection of backscattered electrons induced by elastic interaction as exploited in Scanning Electron Microscopy (SEM) systems is one of the main topics of this thesis.

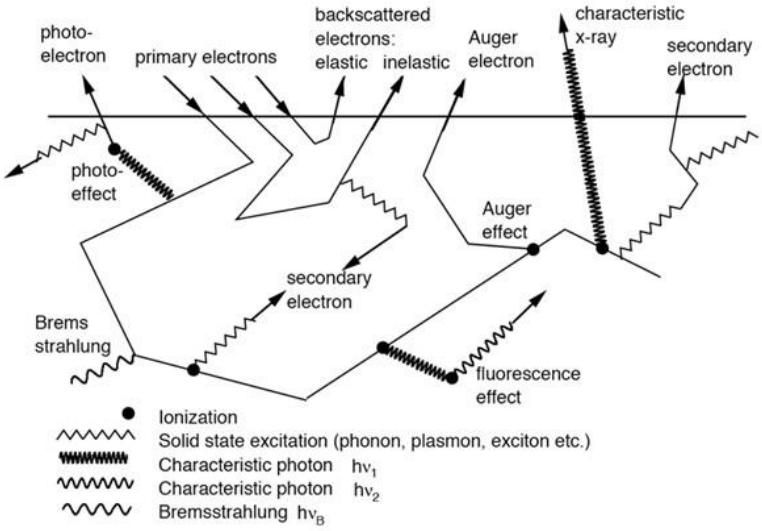


Fig. 1.10. Possible interactions of electrons in matter [22].

Beam energy is a differentiating parameter in SEM imaging. Information on the properties of the bulk of a specimen can be revealed by irradiation with high electron energies while with energies below 1 keV that give nm shallow penetration-depths in solid materials, information is gathered from the surface of the specimen. In many fields, nano-technological trends demand imaging of feature sizes in the nm range, which makes Low-Voltage Scanning Electron Microscopy (LVSEM) a preferred tool for nanometer-scale inspection. It can provide atomic-scale resolution of the specimen surface due to the short interaction range of electrons in matter, and suppresses charging effects that for higher voltages obscure the imaging of non-conducting materials such as those often used in semiconductor device fabrication [23].

The detection of low-energy electrons with Si photodiodes is challenging. The penetration depth of electrons goes from a few tens of nm around 1 keV down to around one nm at 100 eV as shown in Fig. 1.11. Therefore, the photosensitive region must extend almost right up to the Si surface and it cannot be covered by any extra layers that are much thicker than a nm since any extra thickness will result in energy loss of the incident electrons. PureB photodiodes that can fulfill these requirements will be shown and discussed in this thesis.

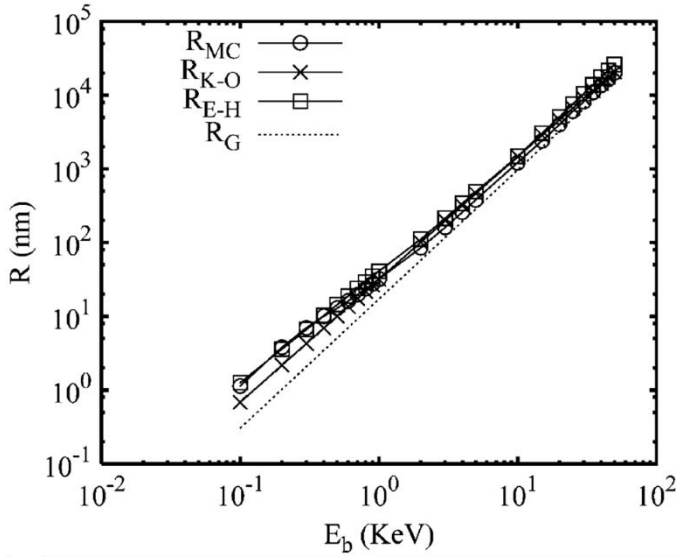


Fig. 1.11. Electron range in silicon. R_{MC} is from Monte Carlo simulations, R_{K-O} is from the Kanaya and Okayama range, R_{E-H} is from the Everhart-Hoff universal curve calculation, and R_G is from the extrapolated Gruen range [24].

1.3 Outline of the thesis

This thesis focuses on the detection of shallow-penetrating beams in Si with photodiodes based on PureB technology. The work is devoted to achieving high-quality, low-noise-level CMOS-compatible Si photodiodes. With this purpose, several characterization techniques were developed to investigate the properties of the fabricated devices. The basic structure of this thesis is as follows:

In Chapter 2, the basic process flows for fabricating PureB photodiodes and vertical *pnp* transistors with PureB emitters are introduced. The main methods used to influence the dark current, series resistance, and capacitance of the diodes are reviewed and illustrated by examples of some of the mm-large detectors developed in earlier PureB projects. These were all made with 700 ℃ PureB deposition while in the present project focus was also placed on 400 ℃ deposition. The electrical behavior of the two is compared in this chapter in the low-voltage regime where all the early photodiodes were operated. In contrast, for APDs and SPADs operation takes place in the vicinity of breakdown. To

optimize the performance of these devices, the electrical characterization of the existing 700 ℃ photodiodes was extended to the high-voltage, reverse-bias range including breakdown behavior.

In Chapter 3, two test structures are introduced to give a tool for quickly evaluating whether an effective counter-doping of the surface has been achieved. They are straightforward both with respect to the required processing and the applied measurement technique. Only the diode itself and a contact to the substrate needs to be processed and the electrical measurements are limited to simple *I-V* characterization of a lateral bipolar structure that gives information on the individual electron and hole current flows. The method is particularly handy for fast-turnaround-time experiments during the development of ultrashallow junctions or ohmic contacts. In the following chapters it is used to gain information on diodes fabricated with low-temperature deposition of B and Ga.

In Chapter 4, another property of the PureB layer, the conductance along the PureB-on-Si interface, is studied by designing and fabricating sheet resistance (R_{SH}) structures for measuring the as-deposited layers. The design and measurement considerations are treated in detail and with the purpose of achieving a quick turnaround tool for in-line monitoring, a simple layout with 2 masks was implemented. The accuracy and reliability of simple Van der Pauw structures was validated by also designing and measuring sets of ring-shaped structures. Moreover, a physical model is proposed to explain why the 400 ℃ PureB junctions behave like conventional p^+-n junctions and the effect of various post-processing steps is studied and found to readily influence the R_{SH} of the low-temperature depositions.

In Chapter 5, the capabilities of PureB photodiodes are shown to be enhanced by the design and fabrication of PureB SPADs. The fabrication considerations for realizing high-quality, low-noise-level PureB SPADs are discussed in detail and the processing performed directly above the PureB layer is evaluated for two techniques for contacting the p^+-anode. A process for fabricating PureB SPADs with near-ideal electrical characteristics was achieved.

In Chapter 6, the fabricated PureB SPADs are characterized, the devices display low-noise levels and good optical response was measured for ultraviolet light down to 270 nm in wavelength. The PureB SPADs are also characterized

for exposure to low-energy electrons down to 200 eV that have a penetration depth of less than 5 nm in Si.

In Chapter 7, a new PureB-based technology, pure-gallium-boron (PureGaB) technology, is proposed and studied. Photodiodes with PureGaB anodes are fabricated and characterized. They show good electrical characteristics and high response to the ultraviolet and low-energy electrons which is very similar to the behavior of PureB photodiodes.

Finally Chapter 8 summarizes the main conclusions of the work in this thesis and provides recommendations for the future work.

Chapter 2

Photodiodes made in PureB Technology

In this chapter we take a closer look at the fundamentals of PureB technology and how it is integrated in photodiode detectors. A considerable amount of past work has been devoted to this subject and this is reviewed in Section 2.1 on PureB deposition and Section 2.2 on device design and fabrication. In both sections, emphasis is placed on the details that are important for the results achieved in this thesis work. Besides the light-entrance windows made with PureB, four elements play an important role for the functioning of the specific detector application: leakage current, series resistance, capacitance, and isolation between photodiodes. Each of these aspects will be treated in relationship to the photodiode fabrication process. In the last sub-section 2.2.5, examples are given of detectors that were fabricated in the past, particularly with the aim of illustrating the process flexibility. Throughout the whole section comments are made on the possible integration of the process and detectors in CMOS.

Section 2.3 is devoted to investigations made in the context of this thesis project to further the understanding of the electrical properties of PureB diodes. One focus of the research was the development and understanding of diodes formed by PureB depositions at 400 ℃. The initial experiments are presented in sub-section 2.3.1 to underline the properties that needed to be understood, i.e., why equally low saturation-currents and low series-resistance were regularly found for both 400 ℃ and 700 ℃ photodiodes.

A second focus of the thesis is the development of VUV-sensitive SPADs in PureB technology. With this in mind, in sub-section 2.3.2, the basic knowledge of the electrical properties of PureB diodes was extended to features related to the breakdown voltage. Since the breakdown voltage is very often determined by the depletion of the Si/SiO_2 region at the perimeter of the anode, different methods of designing this perimeter and the window for PureB

deposition were studied, including the implementation of guard rings, as discussed in sub-section 2.3.2.

2.1 PureB Deposition

The pure boron layers are deposited on silicon by exposing the Si surface to diborane B_2H_6 gas at temperatures from 400 ℃ to 700 ℃ and at either atmospheric or reduced pressure in commercial chemical-vapor deposition (CVD) equipment for Si/SiGe epitaxy, the ASM Epsilon single wafer epi reactor. Quite a number of reactions occur between the carrier gas H_2, the precursor gas diborane and the Si, the deposition mechanisms are illustrated in Fig. 2.1. The resulting chemical reaction is:

$$B_2H_6(g) \rightarrow 2B(s) + 3H_2(g) \tag{2.1}$$

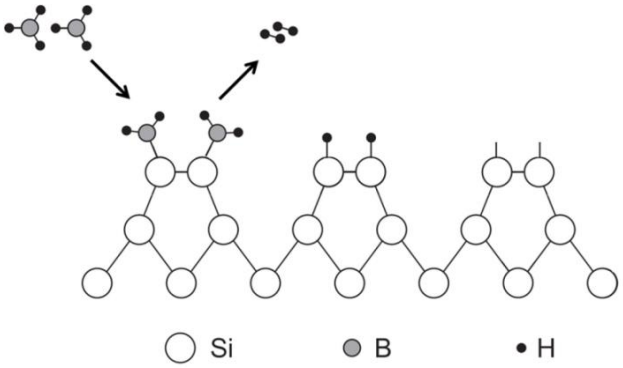


Fig. 2.1. Doping reaction model for Si surface exposure to B_2H_6 dopant gas (after [4, 25]).

To form an ultrashallow junction, a few nanometer of amorphous boron (α-B) is deposited. An example of such a layer formed by 10-min deposition at 700 ℃ and atmospheric pressure is shown in the high-resolution transmission electron microscopy (HRTEM) image of Fig. 2.2, where the segregation of B atoms in an amorphous layer is visible. At the interface with the Si, a mixing of the Si and B in a region about 1 nm thick is also discerned [26]. At 700 ℃, bulk doping of the Si will also occur up to the solid solubility of 2×10^{19} cm^{-3} [27].

Diodes fabricated with PureB technology showed remarkably similar electrical properties for all depositions from 400 ℃ to 700 ℃. While some bulk doping of the Si occurs at 700 ℃, as the temperature is reduced to 400 ℃ this is

no longer possible. Nevertheless, extremely shallow junctions can be formed that behave as p^+-n junctions and despite the junction depth of a few nanometer they can have a saturation current as low as that of conventional deep junctions. One of the goals of this thesis was to understand the properties of the boron-to-Si interface that make this possible. Among other things, the test structures described in Chapter 4 were developed to determine the sheet resistance along this interface.

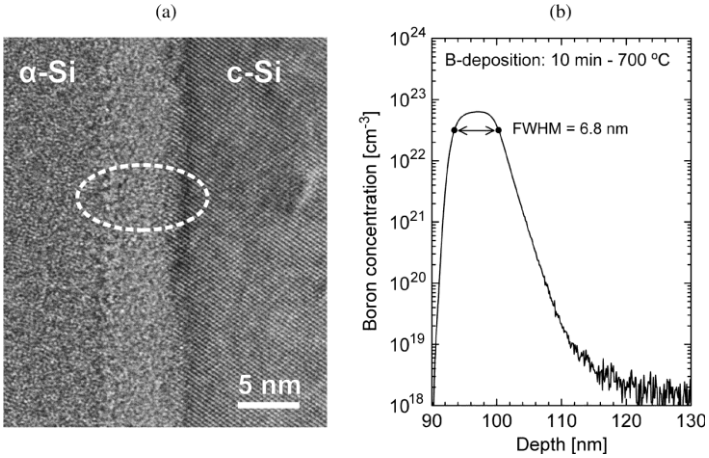


Fig. 2.2. (a) HRTEM image and (b) SIMS profile (O_2^+ primary ion beam at 1 keV) of an as-deposited B-layer formed on (100) Si surfaces at 700 ℃ after a 10-min B_2H_6 exposure [3]. A layer of PVD α-Si has been deposited at room temperature prior to the analytical characterization.

The PureB layer itself has very high resistivity, in the kΩ-cm range [28]. In applications where the Si device is contacted vertically through the PureB layer, excess series resistance can be avoided by limiting the layer thickness to below 3 nm which is the tunneling limit. The accuracy with which the layer can be deposited allows such a thickness to be reliably reproduced across the wafer and from wafer to wafer. In large-area photodiode applications the lateral sheet resistance can give a significant contribution to the series resistance. Therefore, there was interest in reducing the resistivity of the PureB. Previous experiments have led to the suggestion that an impurity doping of the PureB layer could be the origin of large variations in the resistivity. Some of the experiments described in Chapter 7 with Ga deposition were originally meant to investigate whether an alloy with a metal like Ga could serve to bring the resistivity down to values in the tens of Ω-cm range.

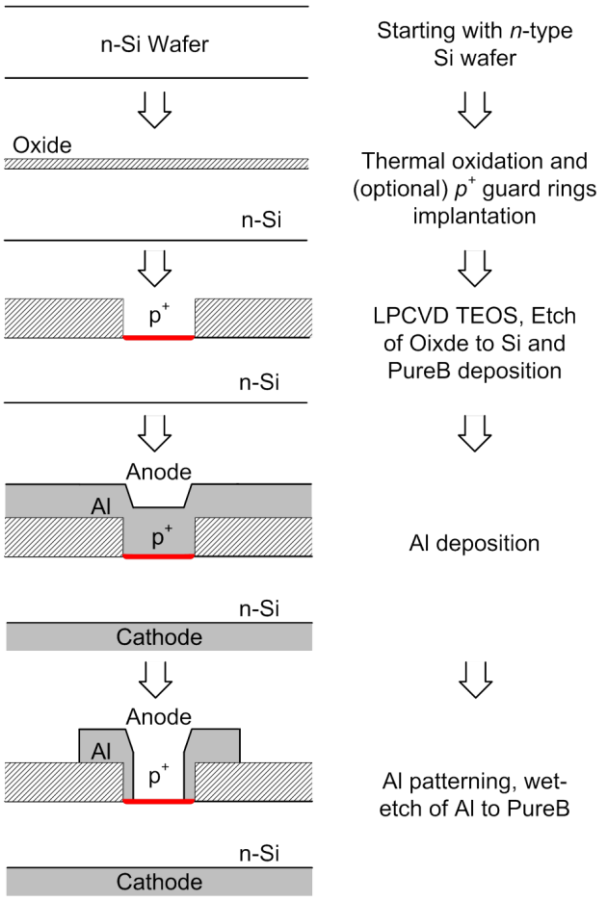


Fig. 2.3. Schematic process flow for fabrication of PureB diodes.

The basic process flow used to fabricate all the PureB diodes investigated in this thesis is shown in Fig. 2.3. The starting wafer is *n*-type Czochralski (100) 1-10 Ω·cm Si substrates. In some cases a thick, 10 µm or more, n^--Si epitaxial layer is grown on the *n*-type starting wafer to lower the diode capacitance [29]. A thermal oxide is grown, either 30-nm or 300-nm thick, through which heavily-doped p^+ guard rings are optionally implanted and annealed in argon gas at 950 ℃ for 20 min. The wafers with 30-nm oxide are then covered with 300-nm LPCVD TEOS oxide. The anode window is opened in the oxide and treated with a 0.55% HF-dip to remove native oxide after which Marangoni-drying is performed to provide a clean and oxide-free Si surface. This is essential for a defect-free PureB deposition [30]. Deposition is performed at temperatures from 400 ℃ - 700 ℃. *In-situ* drive-in/annealing is also possible

right after the deposition process in the same reactor without breaking the vacuum.

For contacting the anode, a 675-nm pure Al is sputtered at 350 ℃ and the back of the wafer is also sputtered with Al to form the cathode contact. After anode interconnect patterning, the entrance windows to the photosensitive areas are opened first by plasma etching the Al back to 100 – 200 nm. This thin Al layer is then removed by wet etching in HF 0.55% for 3 to 5 min, selectively to the PureB layer. Lastly, a 400 ℃ alloy step in forming gas is performed to passivate the Si/SiO_2 interface at the perimeter of the diodes, thus reducing perimeter leakage.

To further investigate the properties of PureB diodes, conventional vertical *pnp* bipolar transistors were fabricated with PureB diodes as emitters as shown in Fig. 2.4. To simplify the fabrication process, the *p*-type Si substrate is used as the collector, the base region is formed by an *n*-type implantation (P^+, 1.5×10^{12} cm^{-2} at 180 keV and 1×10^{12} cm^{-2} at 60 keV) to a level of 1×10^{17} cm^{-3} and contacted through n^+ implantation plugs (P^+, 5×10^{15} cm^{-2} at 60 keV). The emitter is formed by a PureB deposition. With this structure, the hole and electron currents can be measured separately, for example, by measuring the Gummel plot, i.e., the base current I_B and collector current I_C as a function of base-emitter voltage V_{BE}. In principle, the Gummel number of a doping region governs the injection of minority carriers into that region from an adjacent region of opposite doping [26]. The Gummel number is proportional to the total doping of the region. In the simple case of uniform doping and no bandgap variations this is expressed by

$$G_p \propto N_A \cdot W_p \tag{2.2}$$

and

$$G_n \propto N_D \cdot W_n \tag{2.3}$$

where G_p and G_n are the Gummel numbers for *p*- and *n*- regions, N_A and W_p are the impurity concentration and junction width of the *p*-region, and N_D and W_n are the impurity concentration and junction width of the *n*-region. The hole injection (e.g. from *p*-emitter to *n*-base) current density J_p and electron injection (e.g. from *n*-base to *p*-emitter) current density J_n can be expressed as [31, 32]:

$$J_p \approx -\frac{qn_{io}^2}{G_n}\left\{\exp\left(qV/kT\right)-1\right\} \tag{2.4}$$

and

$$J_n \approx -\frac{qn_{io}^2}{G_p}\left\{\exp\left(qV/kT\right)-1\right\} \tag{2.5}$$

where q is the electronic charge, n_{i0} is the intrinsic carrier concentration, V is the applied voltage, k is Boltzmann's constant and T is the temperature. From equations 2.4 and 2.5 we can see that the higher the Gummel number is, the lower the injection current will be. For a *pnp* bipolar transistor as shown in Fig. 2.4, $I_C \propto J_p$ and $I_B \propto J_n$, thus the collector current I_C gives information on the injection of holes into the base from the emitter and the base current I_B on how efficient the emitter is in suppressing the injection of electrons.

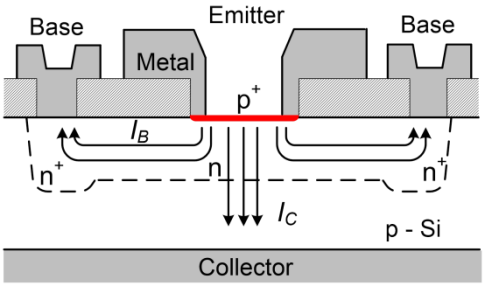


Fig. 2.4. Schematic cross-sections showing how the vertical *pnp* bipolar transistors were fabricated.

2.2 Photodiode Design and Fabrication

2.2.1 Series resistance

For high speed detection applications, it is important to achieve a low series-resistance and low capacitance of the individual devices. The pure boron layer itself has very high resistivity, therefore, the sheet resistance depends on the conductivity created at the interface with the Si. For a 700 ℃ deposition of a 2-nm-thick PureB layer the sheet resistance is determined by the doping of the bulk Si at this temperature. This gives a sheet resistance of about 10 kΩ/sq [26]. This is so high that the series resistance of large area photodiodes can become a limitation. There are several ways to lower the sheet resistance. With an *in-situ* annealing process at higher temperatures, the sheet resistance can be lowered due to the higher solid solubility giving a more effective *p*-doping of the bulk Si.

For instance, the sheet resistance of the 700 ℃ as deposited PureB photodiode can be lowered from about 10 kΩ/sq to about 2 kΩ/sq with an additional 800 ℃ 10 min anneal and to 250 Ω/sq with 900 ℃ 20 min [30]. From Fig. 2.5 it can also be seen that the depth of the junction will increase with increasing anneal temperature, reaching almost 200 nm for a 20 min annealing process at 900 ℃. Nevertheless, also in this case a high responsivity can be obtained for shallow-penetration irradiation if the gradient of the doping profile results in a high electric field across the whole *p*-region that can separate any generated electron-hole pairs just like in the depletion region.

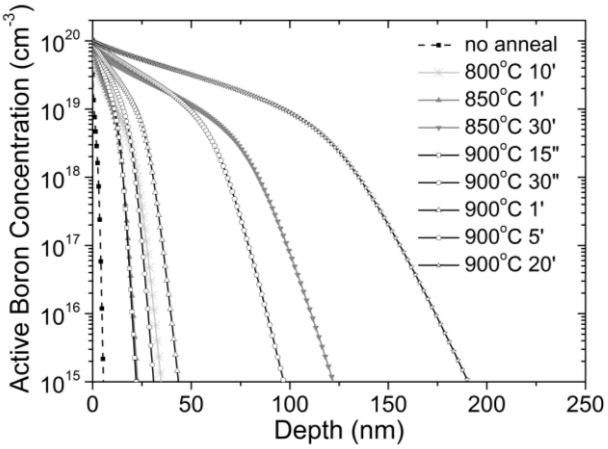


Fig. 2.5. Simulated doping profiles for different anneal conditions. The dopant activation model is based on solid-solubility [30].

In some situations, high temperature annealing is incompatible with the thermal budget of the total process flow. In that case, the sheet resistance can also be lowered by depositing a more conductive layer on top of the PureB. An *in-situ* option that was used in the fabrication of varactor diodes [33], is the deposition of doped Si directly after the PureB deposition. The Si is then amorphous but with a boron doping of 2×10^{19} cm^{-3} as obtained at 700 ℃, the series resistance can be significantly lowered when the α-Si layer can be grown thick enough.

For some photodiode applications, any layer on the photosensitive surface will lower the responsivity. An alternative way of lowering the series resistance over the anode surface is to create a metal grid. Such a grid can be etched in the aluminum layer that is deposited to contact the PureB surface as illustrated in

Fig. 2.6. Examples of detectors using this type of grid will be presented in Section 2.2.5.

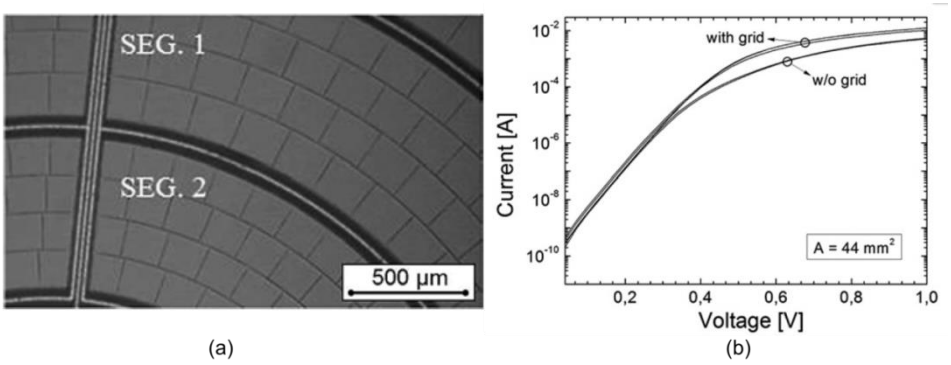


Fig. 2.6. (a) Example of patterning of an Al conductive grid and (b) forward *I-V* characteristics of a PureB photodiode with and without a conductive grid on the photosensitive surface [34].

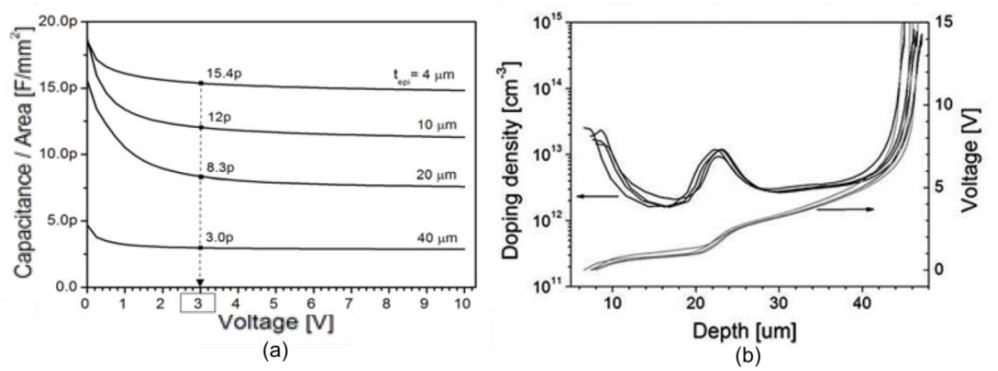


Fig. 2.7. (a) Capacitance-voltage measurements of PureB photodiodes for various epitaxial layer thicknesses. The dashed line marks the operating reverse voltage of 3 V and the Capacitance/Area values at each epi-layer thicknesses are also indicated. (b) *C-V* doping profiles of a 40 µm-thick n^{--} epitaxial layer showing the doping density and the corresponding voltages [35].

2.2.2 Capacitance

To achieve a low capacitance value of the device while not significantly sacrificing series resistance or dark current, the width of the photosensitive depletion layer can be increased by growing a very low-doped epi layer on low-ohmic substrates to create a *p-i-n* like structure [34]. In the PureB photodiode

case, the low-doped region should be lightly *n*-doped for diode isolation purposes. During operation, the low-doped epi layer, which represents a high resistance, should be fully depleted so that the series resistance is determined by the low-ohmic substrate. In previously developed detectors a capacitance of 3 pF/mm^2 was required [34]. As shown in Fig. 2.7, this was achieved by growing a 40-µm-thick epi layer with a doping level in the range of 10^{12} to 10^{13} cm^{-3}. The epi layer was grown *in-situ* with two 20-µm steps.

2.2.3 Guard rings and diode isolation

Due to the curvature at the perimeter of a p^+n junction diode the electric field over the depletion layer is generally higher than in the laterally uniform region away from the perimeter. For this reason, to prevent the premature edge breakdown, a guard ring is often integrated along the perimeter. To reduce the curvature, this region is therefore usually deeper and less abrupt than the original p^+-region. For a shallow planar junction on the Si surface, an implanted guard ring is normally used that overlaps the active region of the device. In most the devices fabricated as part of this thesis work, a p^+-guard ring around the PureB perimeter is formed with boron implantation at 100 keV, with a dose of 5×10^{15} cm^{-2}. In Fig. 2.8, the *I-V* characteristics of large diodes with and without a guard ring are displayed showing a shift in the forward current towards much lower levels when the guard ring was applied. A large number of devices were made - both before and during this thesis work, and with varying deposition temperatures from 400 ℃ to 700 ℃ - that consistently showed this shift. Hence it was concluded that it must be due to an inherent property of the PureB junction perimeter. The origins of this effect will be discussed further in Section 4.2.1 in connection with the study of the PureB anode-region sheet resistance. The lower saturation current with guard ring also means that the ideal reverse current is lower, which is beneficial for lowering the dark current to give the photodiode a higher dynamic range.

To achieve an effective curvature of the guard ring region, the width must usually be around a micrometer or more. For micrometer-sized devices, implementing such a wide guard ring would consume too much space thus severely decreasing the fill-factor, especially for arrays comprising many small devices. Thus as described in Chapter 5, a different type of guard ring was implemented, i.e., a virtual guard ring was integrated in the small devices by increasing the electrical field in the central part of the device.

When p^+n photodiodes are processed on low-ohmic *n*-type wafers, two adjacent photodiodes are automatically electrically isolated from each other if the *n*-region between them remains undepleted. This can be achieved with only a few micrometers distance between the diodes. When a thick low-doped epi-layer is introduced on the surface, the lateral extension of the depletion layer can mean that tens of micrometers separation is necessary for isolation. Moreover, inversion of the Si/SiO_2 interface can create a conductive channel connection the two diodes. Therefore, an *n*-type channel stop implantation was implemented when low-doped epi-layers were used.

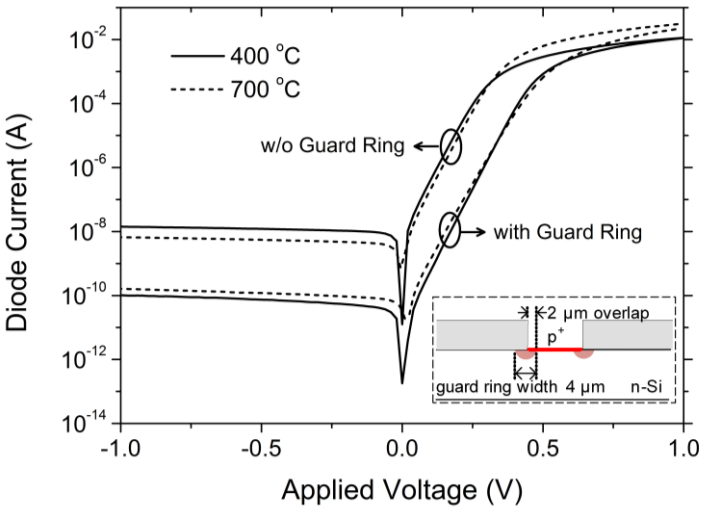


Fig. 2.8. *I-V* characteristics of 400 ℃ and 700 ℃ deposited PureB diodes with and without guard ring, the device area is 1×1 cm^2. The width of the guard ring is 4 µm, with a 2 µm overlap with the p^+-region.

2.2.4 Integration flexibility

For integration with CMOS processes, the 700 ℃ PureB depositions are compatible with front-end processing [36]. Particularly for detector integration, the fabrication temperature, material and processing equipment are common in front-end CMOS processing. The PureB layer itself has excellent properties: it can be integrated as a robust and almost non-absorbing light-entrance window. The layer is conductive, does not oxidize, and does not charge during irradiation [5]. Moreover, it is chemically resistant in many situations and it can be used to form a barrier against silicidation/spiking of metals like Al [37]. Various

functional layers for protection, antireflection, filtering or absorption can be coated on top of the PureB layer, such as physical-vapor deposited (PVD) Zr and AlN, plasma-enhanced CVD SiO_2 and SiN, and *in-situ* growth of B-doped polysilicon. When measures are taken to retain a complete PureB coverage, the robustness of the PureB layer will not be compromised and a lower-than-ideal but still high responsivity can be maintained with thermal processing steps with minute long exposure to temperatures up to 900 ℃ [30]. These properties enhance the flexibility with which the 700 ℃ layer could be integrated for specific detector applications. Examples of this are given in the following sub-section.

2.2.5 Examples of PureB photodiode applications

PureB technology has seen a rapid development and it has already reached a level of maturity where photodiode detectors with outstanding performance have been fabricated and commercialized. It has been possible to integrate detectors that have surpassed the performance of other existing technologies on points such as internal/external quantum efficiency, dark current, and responsivity degradation [6, 38, 39]. In particular focus has been placed on the application to EUV/VUV photodiodes for advanced lithography systems and to low-energy electron detectors for SEM systems [38].

A *VUV/EUV photodiodes*

Due to the importance of DUV and EUV lithography for both the present and future development of the semiconductor industry, extensive work [40] was performed on VUV optical characterization of PureB photodiodes. Specifically, 193 nm is the wavelength in use for DUV and 13.5 nm for EUV lithography. With PureB photodiodes with 2 – 3 nm thick boron layers as light-entrance windows, near-theoretical responsivity is obtained at these wavelengths as can be seen from the measurement examples that are given in Fig. 2.9 for the spectral ranges 2 - 18 nm and 35 – 310 nm. An overview of all the work performed on VUV characterization is given in [30] in which the electrical and optical measurements were re-evaluated in order to further analyze the special features of the PureB layer. The conclusions were:

- The PureB photodiodes made without any high-temperature treatments after the pure boron deposition, show near-theoretical responsivity in the EUV/VUV spectral ranges, independent of the deposition

temperature. This is demonstrated for 400 ℃ and 700 ℃ depositions, and the optical stability is also found to be high for both these cases.

- A similarly high stability is also obtained for devices exposed to up to 900 ℃ thermal drive-in of the boron to 100-nm junction depths if a complete coverage of PureB is maintained on the surface. The responsitivity for such deep junctions is lower than for as-deposited PureB junctions but still very high. If the PureB layer is removed or seriously corrupted by the drive-in a much lower responsivity is measured than would be expected from the results of devices where the layer is kept intact.

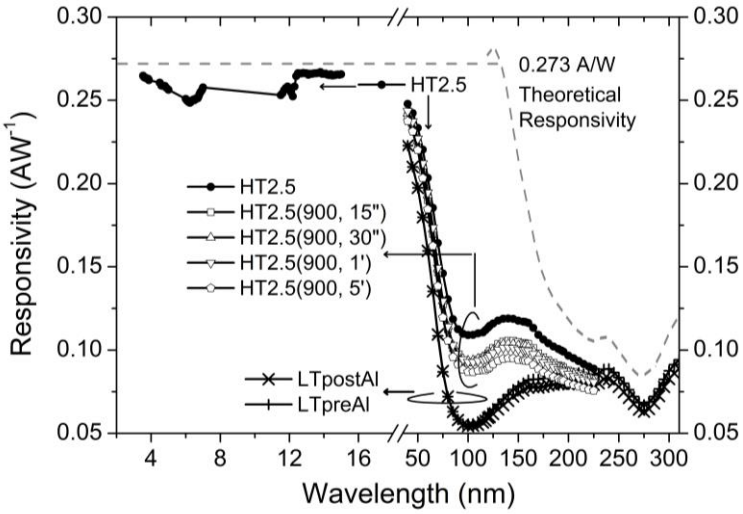


Fig. 2.9. A compilation of VUV responsivity measurements performed on PureB photodiodes that was previously presented in [30, 39]. The graph here displays a selection of the measurements that were particularly important for deciding the experiments to be carried out within the present thesis work: the HT (High Temperature) and LT (Low Temperature) devices have a PureB layer deposited at 700 ℃ and 400 ℃, respectively; the HT2.5(T,t) series devices have an approximately 2.5-nm-thick PureB layer as light-entrance window that is partly deposited after an anneal at temperature T(℃) for a time t; the LTpreAl and LTpostAl indicating the 20 min, 400 ℃ PureB deposition is performed either before (pre) Al deposition or after (post) Al deposition.

- due to the diffused doping gradient from the PureB layer and the effective p^+ layer at the PureB/Si interface, an electric field to separate the photo-generated charge carriers is created and it is particularly high

at the surface where recombination of electrons will otherwise degrade the performance.

- This tolerance to thermal processing gives PureB a high compatibility with CMOS and wide general applicability.
- The experimental evidence distilled in this paper added support to the earlier proposal that the special electrical PureB diode characteristics are related to the chemical properties of the interface of the pure boron on the Si and not the bulk boron properties [41]. However, to arrive at a truly well-founded explanation of the behavior it was clear that more dedicated experimental and theoretical studies were needed. The test structures presented in Chapter 4 were specifically designed for this purpose.

B Low-energy electron detectors

Several PureB detectors were developed and fabricated for use in advanced scanning electron microscopy (SEM) systems to enhance performance by detecting electrons with energies below 1 keV and record-high electron-signal-gain was achieved with 2 – 3 nm thick boron layer for electron energies as low as 200 eV, Many of the elements discussed in Section 2.2 as being important for the design of a detector have found realizations in these electron detectors. A cross section is shown in Fig. 2.10 where the following elements are indicated:

- low capacitance is achieved by epitaxially growing very lightly-doped, tens-of-micrometers thick n-layers on low-ohmic substrates,
- compact segmented anode layouts are achieved with lateral junction isolation of the segments by introducing an *n*-channel stop to eliminate conductive inversion channels and limit the lateral expansion of the depletion layer,
- low photodiode-series-resistance combined with a large sensitive front-window area is achieved by patterning a fine aluminum grid directly on the boron surface. With a width of the grid of 2 μm, it only covered less than 2% of the sensitive region. The series resistance dropped more than 10 times as shown in Fig. 2.6b, from 280 Ω for a device without metal grid, to 20 Ω with metal grid.
- through-wafer apertures etched close to the anode regions for detectors designed to monitor back-scattered electrons (BSE) in SEM systems such as shown in Fig. 2.11.

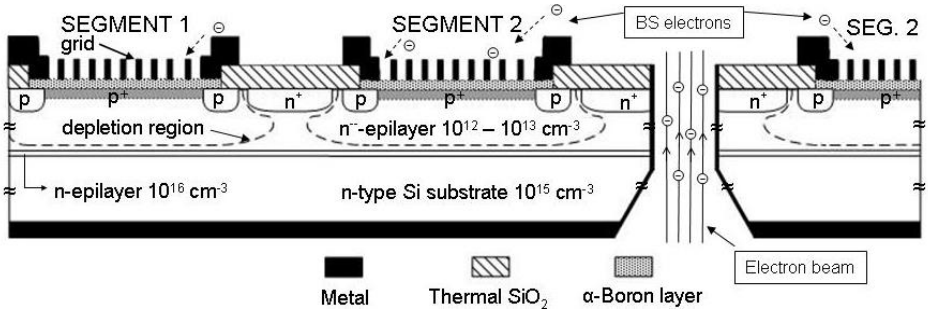


Fig. 2.10. Schematic cross-section of two neighboring segments of a B-layer detector with a through-wafer hole as aperture for the electron beam. The depletion of the typically 40 µm deep n^- epitaxial layer is indicated. Segments are isolated by the n^+-channel-stop and the undepleted n^{--}layer [35].

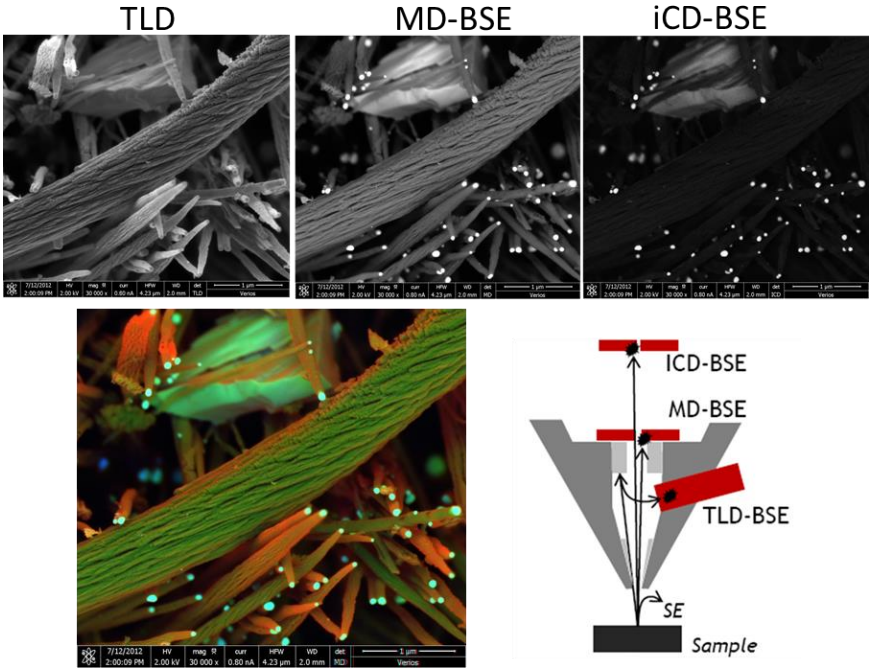


Fig. 2.11. Example of an enhanced-imaging image of catalyst particles on top of nano-tubes by combining and coloring the 3 images shown above from the back-scattered-electron (BSE) detectors (iCD, MD and TLD) in the optical column of a SEM system. Two of the detectors, the iCD (in column detector) and the MD (mirror detector), are made with PureB photodiodes [42].

In Fig. 2.11 an example is given of the enhanced imaging capabilities of an extreme-high-resolution scanning-electron microscope (XHR SEM) using PureB detectors. Two PureB detectors are employed as back-scattered electron detectors (BSEs) placed at two different positions in the column and the information taken at low-electron energies is combined to reveal more details of the sample. The low series-resistance and capacitance values of the detectors combine to give low transit-times and thus high scanning speeds.

2.3 Electrical Behavior of PureB Diodes

2.3.1 Low-temperature deposited PureB diodes

While research was continued on the high-temperature (HT) PureB layer deposited at 700 ℃, in this thesis work effort was also put into developing PureB layer deposition at low temperatures (LT) down to 400 ℃. PureB diodes were fabricated with PureB layer deposition at both high and low temperature on *n*-type Czochralski (100) 1-10 Ω•cm Si wafers as illustrated in Fig. 2.3. For the diodes with micrometer-sized dimensions, no guard rings were implemented and the light-entrance windows were not opened. The Current-Voltage (*I-V*) characteristics were measured for PureB diodes with a 20-min 400 ℃ PureB deposition as shown in Fig. 2.12, where a comparison is made to the characteristics of a 6-min 700 ℃ deposited PureB diode. As seen from the graph, the large 1×1 cm^2 400 ℃ diode is very similar to the 700 ℃ diode. Both exhibit very good *I-V* characteristics: the ideality factors are close to 1 and the dark currents are very low. However, for the LT deposition the 40×1 μm^2 PureB diode has a current level under the same forward bias that is more than 3 decades higher than the HT diode. This behavior can be attributed to the Al on top of the diodes. Unlike the 700 ℃ deposited PureB layer, the 400 ℃ layer has higher surface roughness as shown in Fig. 2.13. It is very likely that this is associated with a higher density of pin-holes. When the Al is removed from the light-entrance windows, the Al-to-boron interface has not been exposed to any significant temperature steps and there is no noticeable reaction between the two. In contrast, when the Al is left on the PureB surface and subjected to the 400 ℃ alloying step, it becomes difficult to remove with HF, i.e., a reaction/intermixing with the boron has occurred. Also the total plasma-etching process of the Al interconnect pattern can expose the small diodes to temperature steps that can be up to 300 ℃. This can explain the increased

current levels in the *I-V* characteristics because any Al that reaches the Si through pin-holes may form a Schottky junction with the *n*-Si substrate. These have many decades higher saturation current and even a small percentage of Al-Si area can give a few decades increase in current.

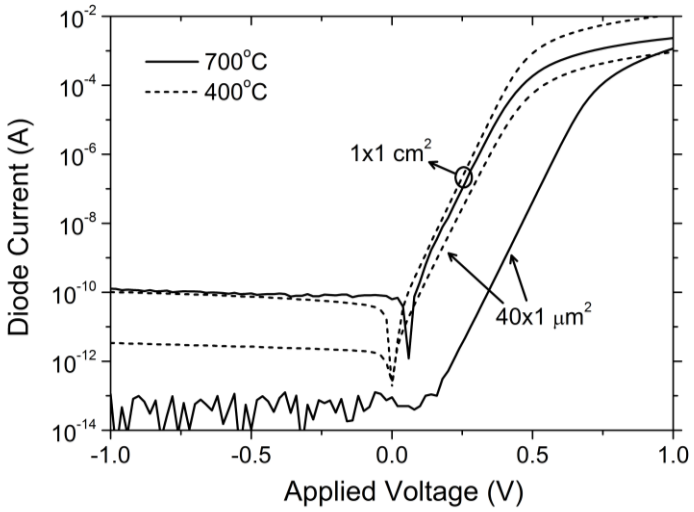


Fig. 2.12. *I-V* characteristics of PureB diodes with different dimensions.

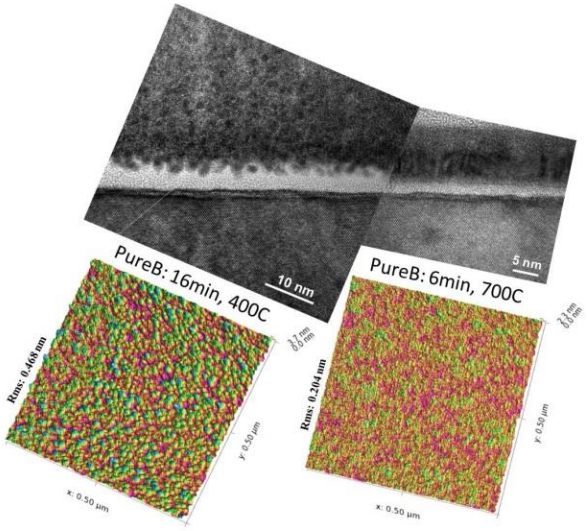


Fig. 2.13. HRTEM images of PureB layers grown at 400 ℃ (left) and 700 ℃ (right). [39]

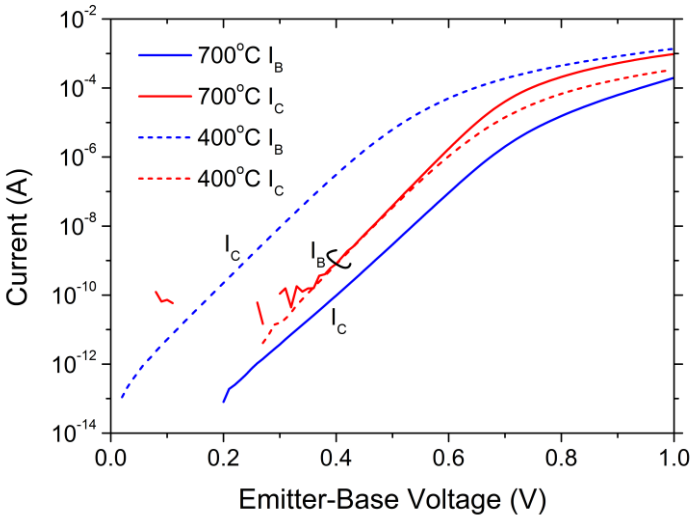


Fig. 2.14. Gummel plot of PureB vertical *pnp* bipolar transistors. The emitter area is 40×1 μm^2.

To further investigate the properties of PureB diodes, conventional vertical *pnp* bipolar transistors were fabricated with PureB diodes as emitters as illustrated in Fig. 2.4. The emitter is formed with the PureB diode deposited at 400 ℃ for 20 min or 700 ℃ for 6 min. As discussed in Section 2.1, with this structure the hole and electron currents can be measured separately. From the Gummel plot as shown in Fig. 2.14, the collector currents caused by the injection of holes into the base region is of the same level for both the HT and LT devices. This suggests that the 400 ℃ deposited PureB layer forms a device that behaves like a *p*-*n* junction diode in being able to inject minority carrier holes into the *n*-type Si substrate. For the same reason discussed in connection with the diode characteristics (Fig. 2.12), the I_B is much higher in the 400 ℃ diode.

2.3.2 PureB diodes with biasing in the vicinity of breakdown

As discussed in section 2.2.3, the breakdown of a diode is determined by the electric field over the depletion region, the width of which is determined by the doping profiles of the *p*- and *n*-regions. The ideal breakdown voltage can be lowered if defects are present to generate electrons or holes that can arrive in the depletion region. From the electrical and optical analysis of PureB diode behavior it has been concluded that the PureB junction itself is damage free.

The perimeter regions of diodes are therefore expected to be the main source of such defects. To investigate this, diodes were measured that were fabricated with the four different methods of processing the PureB anode windows shown in Fig. 2.15 and filled with a PureB layer deposited at 700 °C. The windows to the silicon were etched through the oxide either entirely wet (Fig. 2.15a), by plasma etching with soft- or wet-landing (Fig. 2.15b), or by plasma etching about 1 μm into the Si (Fig. 2.15c). On some wafers the PureB-filled window was covered by 100 nm oxide and after this contact windows to the PureB, a few micrometer from the anode perimeter (Fig. 2.15d), were etched in 0.55% HF. On some of the substrates a lightly-doped epitaxial Si layer was grown on the more heavily-doped substrate. For large PureB photodiodes previous studies were devoted to the design of guard rings to optimize the trade-off between capacitance and leakage current for operation at low reverse-voltages [43]. Although it adds to the capacitance, minimizing the depletion along the surface can be important because, as has been shown previously, the depleted region at the oxide interface is the source of both leakage and degradation during exposure to radiation [5]. An overview of the diodes fabricated for this study is given in Table 2.1.

In Fig. 2.16 the *I-V* characteristics of 3 large diodes, Dg(intr,pl), D(intr,wet) and D(oxide), are compared. The electrical *I-V* diode characteristics were measured at room temperature. The current compliance was set at 10 μA for the breakdown measurement. All three have high breakdown, which for the Dg(intr,pl) is lowest due to the small distance between the *n*- and *p*-guard. Moreover, the forward characteristics show that the saturation current for the D(intr,wet) device is almost two decades higher than for the two other device types. This difference is reproducible over the wafer and from run to run. As already commented in Section 2.2.3 in connection with Fig. 2.8, such a shift to lower currents is seen consistently when adding a guard ring to PureB diodes. The origin of the shift will be discussed in Section 4.2.1.

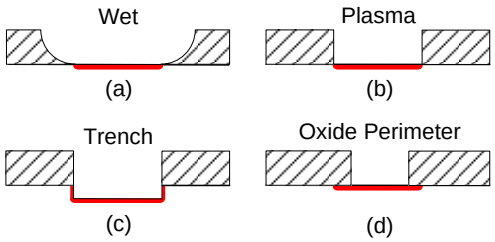


Fig. 2.15. Schematic of 4 different methods of etching and filling the PureB anode windows.

Table 2.1. List of the measured PureB diodes indicating the different process variations

Device	Epi	Geometry	Guard ring	Anode window etch
Dg(intr,pl)	10 µm intrinsic	diameter = 3.6 mm	p^+	plasma
D(intr,wet)	10 µm intrinsic		no	wet
D(oxide)	no		no	wet + oxide perimeter
D(pl+wet)	no	300×315 µm^2	no	plasma + wet
D(trench)	no		no	trench

In Fig. 2.17 *I-V* characteristics are compared for the devices D(pl+wet) and D(trench). For the latter the breakdown voltage is decreased, presumably because the trench in which the PureB is deposited has corners where the electric field will be higher than for the flat structure. Nevertheless, the breakdown is high and reproducible over the wafer and from wafer to wafer.

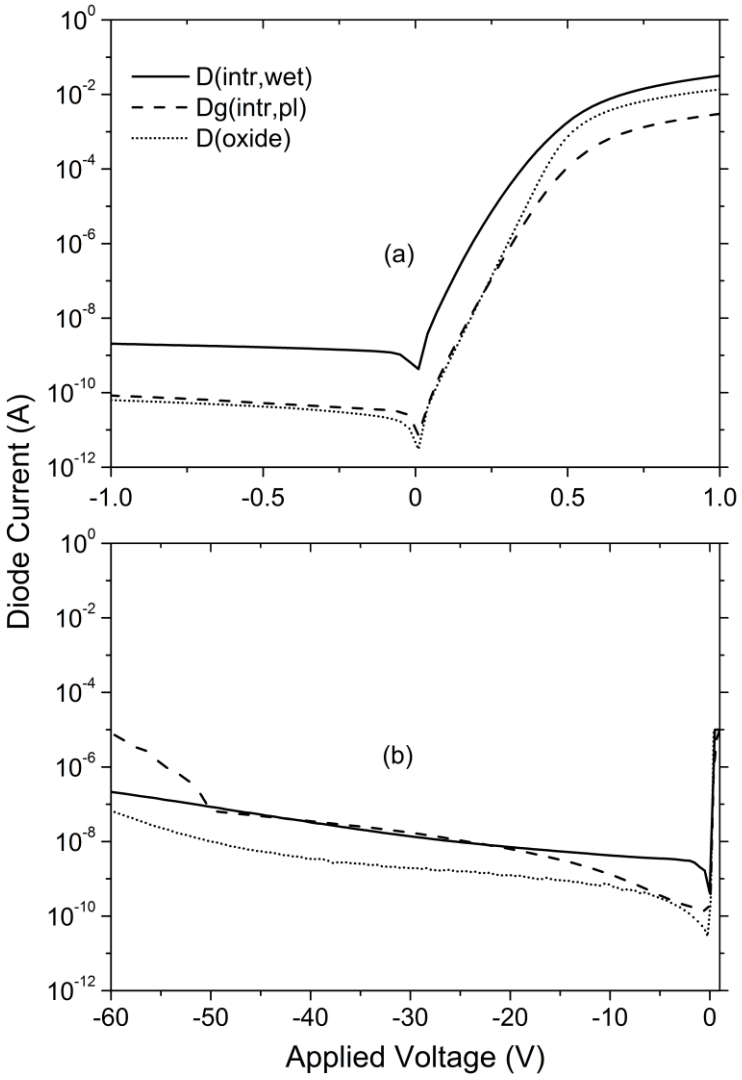


Fig. 2.16. *I-V* characteristics of 3 large diodes fabricated in different ways, (a) in the forward and small reverse-bias regime and (b) in the large reverse-bias regime. The diameter of the diodes is 3.6 mm.

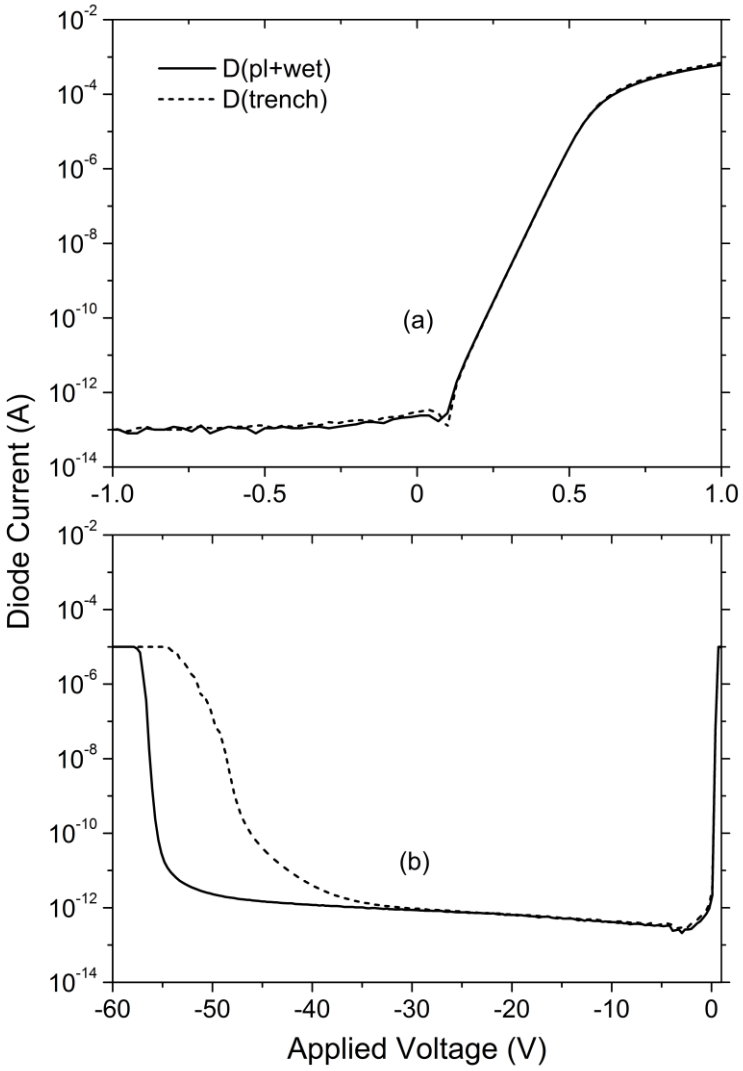


Fig. 2.17. *I-V* characteristics of diodes where the anode window is opened in two different ways, (a) in the forward and small reverse-bias regime and (b) in the large reverse-bias regime. The diodes have an area of 300×315 μm^2.

2.4 Conclusions

The work reviewed in this chapter underlines that the 700 ℃ PureB photodiodes have proven their worth as integrated detectors for a wide spectral range. The initial attempts to make similar diodes with 400 ℃ depositions show that also this deposition has great potential for the fabrication of photodiodes with similarly good performance. In addition, there is the extra advantage that this deposition could be performed after metallization of other devices on the wafer.

The reverse current behavior was investigated for a large number of 700 ºC PureB diodes with different anode window geometries and different configurations of guard rings. In all cases the leakage current is low right up until breakdown and the breakdown behavior is well-defined and reproducible over the wafer. This shows that although the PureB anode forms a p^+-doping of the Si that is only about 2 nm deep, the leakage currents and breakdown voltage are determined by the doping of *n*-Si and/or the depletion of the oxide interface at the diode perimeter. Even in the cases without guard rings or with trench-etched anode windows, the PureB perimeter coverage is complete and allows high breakdown voltages.

Chapter 3

Lateral Bipolar Structures for Evaluating the Effectiveness of Surface Doping Techniques

3.1 Introduction

As basic semiconductor building blocks, Schottky diodes and ultrashallow junctions are playing a very important role in the development of advanced devices for future CMOS and bipolar transistors generations [45, 46]. With the advanced doping techniques being explored today for the fabrication of ultrashallow junctions, it can often be difficult to discern whether or not an actual counter-doping of the Si surface has been achieved. More specifically, it is not always obvious whether the resulting junction, for example in the case of a *p*-Si substrate to be *n*-doped, forms a metal/*n*-Si/*p*-Si (*m*-*n*-*p*) junction or a metal/*p*-Si (*m*-*p*) Schottky diode. In fact, a change in the surface conditions can have the same effect on the Schottky barrier height (SBH) as a bit of counter-doping. The latter will effectively appear as an increase of the Schottky barrier height (SBH) giving a corresponding decrease of the diode current [47].

Commonly used doping-profile characterization techniques can give some valid information about the surface doping but most of them are destructive and require special equipment or measurement structures [48]. Moreover, they are particularly time consuming when ultrashallow junctions are to be accurately profiled. In contrast, the test structures presented in this chapter are designed to give a tool for quickly evaluating whether an effective counter-doping of the surface has been achieved. They are straightforward both with respect to the required processing and the applied measurement technique. Only the diode itself and a contact to the substrate need to be processed and the electrical measurements are limited to simple *I*-*V* characterization of a lateral-transistor structure that gives information on the individual electron and hole current

---

Part of this chapter have been published in *IEEE Trans. Manufact. Technol.*, **25**, 581 (2011) [44]

flows. By studying the behavior of electrons and holes, especially that of the minority carriers, the effectiveness of the surface doping can be evaluated. The method is particularly handy for fast-turnaround-time experiments during the development of ultrashallow junctions or ohmic contacts. This is illustrated here by the measurement of a series of diodes produced by depositing arsenic dopants in contact windows to *p*-type silicon and then activating these dopants by excimer laser annealing. Depending on the laser energy, the silicon surface will be heated or melted, allowing the *n*-type dopants to be driven-in to different depths and activation levels for junction depths below 20 nm. The interpretation of the results is supported by device simulations.

The work presented in this chapter makes use of n^+-*p* ultrashallow junctions produced by laser annealing to verify the applicability of the test structures. This set of experimental devices was particularly suited for this purpose because a gradual transition from Schottky-type junctions to n^+-*p* junctions could be realized as a function of the applied laser-anneal energy. Nevertheless, for this thesis work, the main goal was to create test structures for evaluating the behavior of PureB diodes, particularly the ones produced at low temperatures where no doping of the Si can be expected. In the last sections, electrical behavior of PureB diodes with various deposition temperatures are investigated with these test structures, the general behavior is also valid for p^+-*n* diodes.

In this chapter, the aim is to develop methods that are easy to fabricate and use during the process development and can even be combined with the integration of the diode itself. With these methods, the electrical characteristics of junctions with behavior from Schottky-like to a hybrid of Schottky and *p*-*n* junction to *p*-*n* junction-like can be investigated. Specifically, the electrical characteristic of low-temperature deposited PureB diodes are studied here and compared to high-temperature deposited PureB diodes.

3.2 Theoretical Considerations

A number of device simulations in Sentaurus were performed to illustrate the current flows in the different situations that can occur in ultrashallow and Schottky junctions. Examples are given in Fig. 3.1 of the main three types of diode behavior:

(a) an *m*-*p* Schottky diode, the metal-semiconductor contact is defined as a Schottky contact to simulate the thermionic emission of majority carrier

holes from the semiconductor into the metal, which is the process that dominates the diode current. As illustrated by the schematic band diagram in Fig. 3.2, the application of a forward bias V_a will lower the barrier for holes that are injected from the Si into the metal. At the same time, a very small current of electrons is injected from the metal into the semiconductor.

(b) a fully-depleted *m-n-p* diode : an ultrashallow heavily-doped *n*-type region is created at the surface of the *p*-type substrate, as indicated in the band diagram shown in Fig. 3.3a, and the contact to this region is a Schottky contact. Under reverse and small forward bias, the *n*-region is fully depleted by the metal-semiconductor depletion region and the diode displays the electrical characteristics of a *p*-Schottky. The current is dominated by hole injection into the metal but the effective *SBH* is so high that the total current is much lower than the pure Schottky case of Fig. 3.2. With a large reverse bias, V_d in Fig. 3.3a, the effective *SBH* is lowered due to image-force lowering, and the reverse current is increased. At a high enough forward-bias voltage, V_a in Fig. 3.3b, the *n*-region can become non-depleted. The *n*-region is heavily doped, thus an ohmic contact is formed. The presence of the *n*-region effectively reduces the hole current to the point where the device behaves as an *n-p* diode and when the whole *n*-region becomes non-depleted the hole current starts to increase again as shown in Fig. 3.1b and the current of the diode is a diffusion current. An analytical formulation of this type of transition from Schottky-like to *p-n* junction-like behavior is given in [49].

(c) an ohmic-contacted *m-n-p* diode as shown in Fig. 3.4, the diode current is dominated by the injection of minority carrier electrons from the n^+ region into the substrate (*p*-region) and the electron current is much higher than in cases (a) and (b). For shallow junctions the metal forms a sink for the minority carrier hole injection and the very low hole-current increases for junctions that are less than about 20 nm deep. This is shown in Fig. 3.1c for different junction depths. The electron current is in all cases of the same level as the one shown in Fig. 3.1b and the hole current starts to dominate the total current for the shallower junctions.

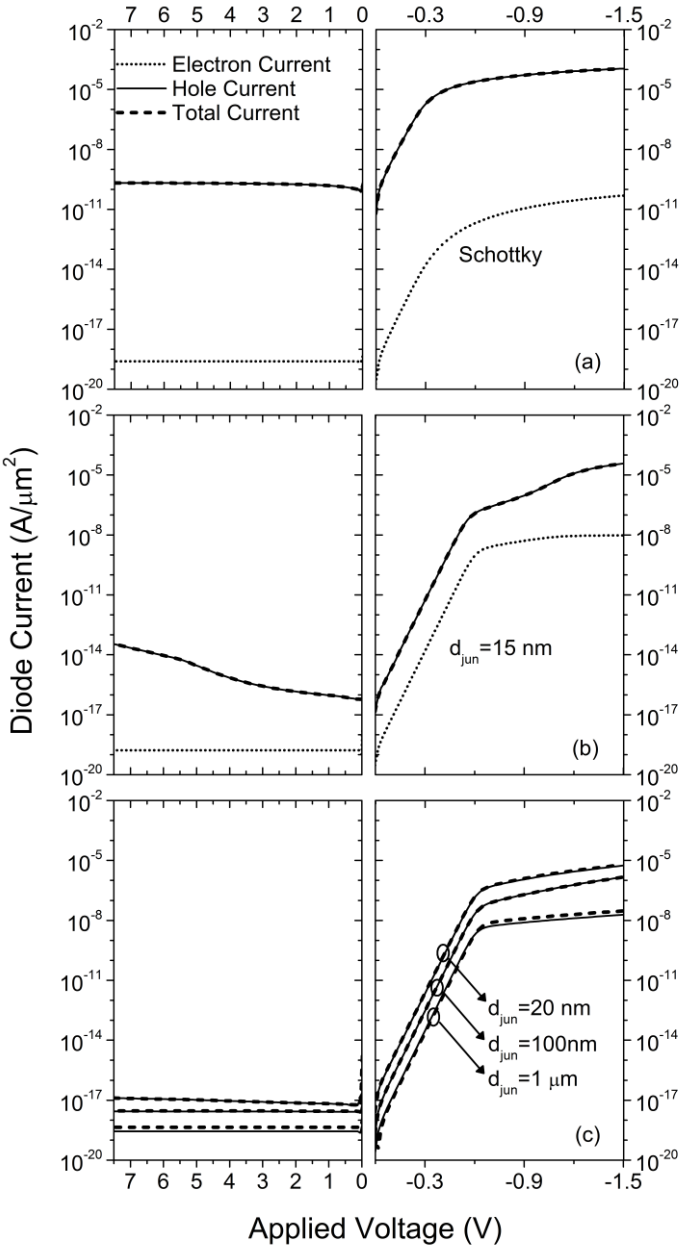


Fig. 3.1. Simulated output characteristics of (a) an *m-p* Schottky diode, (b) a fully-depleted *m-n-p* with d_{jun}=15 nm with N_D=5×10^{18} cm^{-3}, and (c) an non-depleted *m-n-p* diode, all with N_D=5×10^{18} cm^{-3}. In all cases the substrate doping is N_A=1×10^{17} cm^{-3} and the contact is Schottky contact with a *SBH*=0.55 V over *p*-Si.

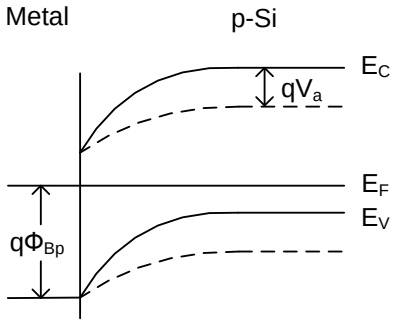


Fig. 3.2. The band diagram of an *m-p* Schottky diode at zero bias (solid line) and forward bias V_a (dashed line).

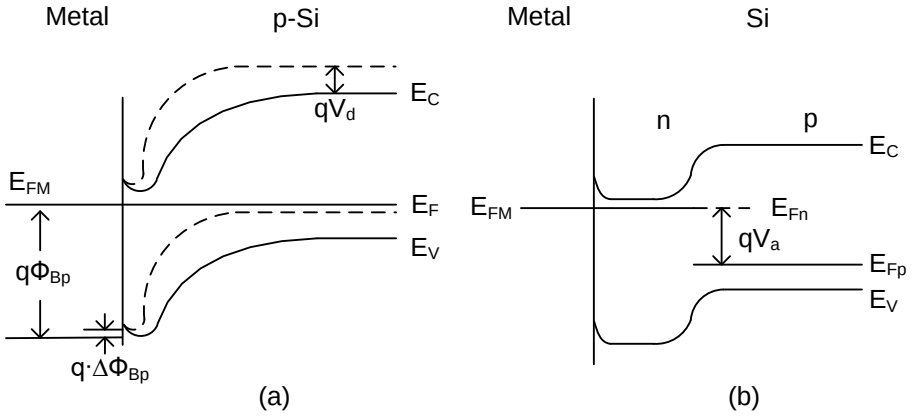


Fig. 3.3. The band diagram of a fully-depleted *m-n-p* diode at (a) zero bias (solid line) and reverse bias V_d (dashed line) and (b) forward bias V_a .

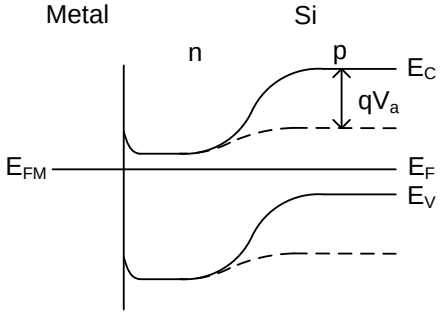


Fig. 3.4. The band diagram of an omhic-contacted *m-n-p* diode at zero bias (solid line) and forward bias V_a (dashed line).

3.3 Test Structures and Experimental Material

The basic test structures are designed as finger structures with 3 parallel contact windows as shown in Fig. 3.5a. The central window is referred to as the emitter with width W_E and length L_E, the outer windows are the collectors with width W_C, and the substrate is the base with a width at the surface of W_B. The contact windows are all processed with the same deposition, laser annealing and metallization steps. All *I-V* measurements are performed at 27°C (300 K) with an Agilent 4156C parameter analyzer.

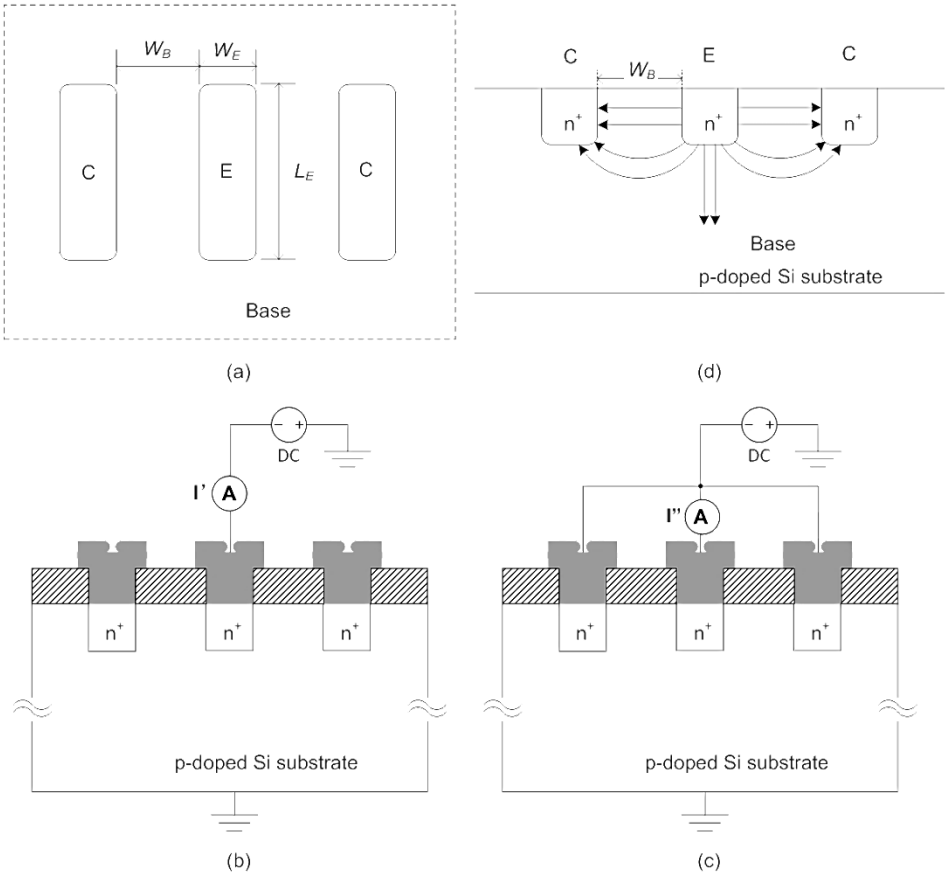


Fig. 3.5. (a) Schematic top view of the contact windows of the test structure consisting of 3 parallel diodes. Configurations for measuring the current through the middle diode with (b) biasing of the middle diode only and (c) all 3 diodes in parallel. (d) Schematic of the lateral transistor and the current paths of the injected electrons.

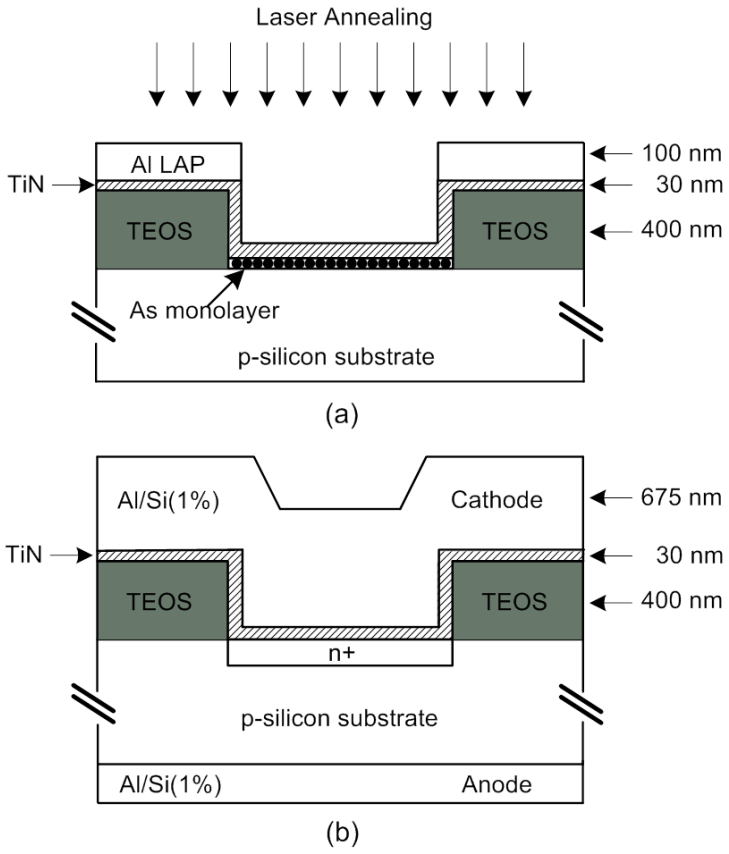


Fig. 3.6. Schematic of (a) deposition and laser annealing, and (b) metallization of the contact windows.

A series of diodes were fabricated on *p*-type Si substrates with a bulk doping of ~ 10^{15} cm^{-3} and a surface doping of the top 300 nm of ~ 10^{17} cm^{-3}. An oxide isolation layer was deposited and contact windows were etched to the Si. A mono-layer of arsenic was deposited in the windows by chemical-vapor deposition in a commercial epitaxial reactor. Then a 30-nm-thick TiN layer was deposited by sputtering and this layer encapsulates the arsenic layer during excimer laser annealing. Before laser annealing the TiN is covered with a 100-nm-thick layer of Al LAP (Laser Annealing Protection) sputtered at 50 ℃ and then removed from the contact windows by wet etching in diluted HF(0.55%). The laser annealing is then performed as illustrated in Fig. 3.6a at energy densities from 600 mJ/cm^2 to 1200 mJ/cm^2, applied in columns across the wafer. At a certain amount of laser annealing energy, a very shallow surface layer of Si

is melted and the As is absorbed in the melt, thus doping the Si when it recrystallizes. All the Al LAP is removed before metallization, exposing the whole TiN layer. Since this layer does not oxide, a dip etch before metallization is not necessary. In this way the oxide coverage of the perimeter of the n^+-region is kept intact. as shown in Fig. 3.6b, a metallization layer of 675 nm Al/Si(1%) is then sputtered at 50 ℃ and patterned. The back of the wafer is also metallized to make contact to the *p*-substrate. An alloy step at 400 °C in forming gas completes the processing.

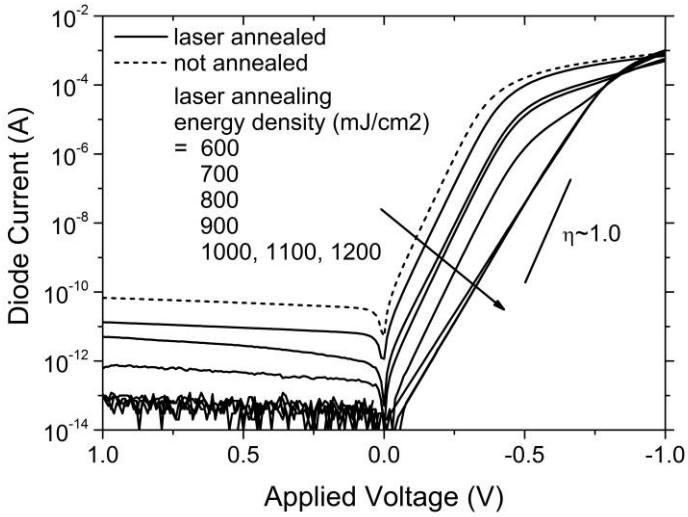


Fig. 3.7. Measured *I-V* characteristics of laser-annealed diodes. The diode area is 20×1 μm^2.

3.4 Characterization Results

3.4.1 Single-diode characteristics

The *I-V* characteristics of a single 20×1 μm^2 diode are shown in Fig. 3.7 for seven different laser-anneal energy densities. The current levels go from the high-current Schottky situation that exists when the contact is not laser annealed, to lower and lower currents as the laser energy increases. The current saturates at an anneal energy of around 1000 mJ/cm^2 for which it is known that a heavily-doped *n*-region is created with a doping $N_D > 1\times10^{19}$ cm^{-3} and an estimated doping depth $d < 20$ nm.

In the one-dimensional diode case, the injection of the minority carriers into the substrate is only governed by the Gummel number [50], i.e., the total impurity dose per surface area, of the substrate. When the area of the diode is finite, minority carriers can also be injected into the peripheral region, and this extra current will have an increased relative importance as the diode size is scaled down. In general, the measured diode current I_D can be modeled as

$$I_D = J_A \cdot A + J_P \cdot P + I_{CORNER} \tag{3.1}$$

where J_A and J_P are the area and perimeter current density, respectively, I_{CORNER} is the current related to the corners, and A and P are the area and perimeter of the contact, respectively. To evaluate the importance of the perimeter current, first J_A is extracted as described in [51] for a set of well-separated single diodes with the dimensions 1×1, 2×2, 4×4, 6×6 and 10×10 μm^2. When it is assumed that the perimeter current of the Schottky diode is zero, i.e., I_D is totally dominated by majority carrier injection from the substrate, the mismatch between the on-wafer and on-mask dimensions is found to be 0.1 μm. By applying this mismatch to the *p-n* diode situation a value for the J_P in this case can be found. Current levels extracted in the ideal forward-biased region are given in Table 3.1. For a 20×1-μm^2-large diode annealed at 1200 mJ/cm^2, the perimeter current is more than 80% of the total diode current. This is in accordance with the fact that the two-dimensional spreading of the minority current [52] is especially large if the half-width $W_E/2$ of the diode is a factor 10 smaller than the diffusion length of the minority carriers in the substrate.

Table 3.1. Extracted forward-bias perimeter and area current densities for 20×1 μm^2 diodes fabricated with or without laser annealing

Laser energy (mJ/cm^2)	V_{EB} (V)	J_A (A/μm^2)	J_P (A/μm)	I_P/I_D
0	0.15	1.45×10^{-9}	0	0
1200	0.5	2.95×10^{-10}	6.12×10^{-10}	82.6%

3.4.2 Parallel-diode characteristics

The degree to which electron spreading into the substrate is determining the current through the diodes of the test structures can be evaluated by comparing the current through either individually connected or parallel connected diodes as indicated in Fig. 3.5b and Fig. 3.5c. The forward current through the middle diode is measured in situation (a) where only the diode itself is biased (*I'*) as in Fig. 3.5b and in situation (b) where all diodes are biased in parallel (*I''*) as in

Fig. 3.5c. If the diodes are Schottky junctions, the current in the two situations will be the same because the dominating current, majority hole current injection from the substrate into the metal, only depends on the area of the diode. There is a small amount of reverse injection of the minority electron-current but it is too small to have any impact. In contrast, if the diodes are non-depleted *m-n-p* diodes, the spreading of the electrons injected into the substrate from the middle diode will be limited by any electron injection from the two neighboring diodes. This presumption has been verified by device simulations as shown in Fig. 3.8, for which the diodes have been forward biased at three different voltages in both situations (a) and (b). Comparing the electron and hole currents in the two situations, a significant decrease in electron current, the minority carrier current injected into the substrate, is observed when the two neighboring diodes are biased in parallel, while the hole current remains practically constant. Thus the current will decrease when the neighboring diodes are connected. The difference will be larger the closer together the diodes are placed to each other and the lighter the doping of the substrate is, i.e., the longer the diffusion length L_n of the minority carrier electrons. This limiting of the current is illustrated by the simulation shown in Fig. 3.9. As the diodes are moved closer and closer together the perimeter current through the middle diode will disappear and the situation becomes one-dimensional with the electron injection being governed by the Gummel number of the *p*-substrate. This gives a lower limit for the current through this diode.

The difference in diode current through the middle diode can be given as the relative current discrepancy $\Delta I/I'$, with $\Delta I = I' - I''$. This value is listed in Table 3.2 for all the different laser annealing energy densities at a forward biasing of 0.1 V, 0.3 V and 0.5 V. The discrepancy is only calculated if the diode current is in the exponential region, i.e., not attenuated by the series resistance. It can be seen that for laser energy densities from 0 to 900 mJ/cm^2, the relative discrepancy is only around 1%, indicating that there is no electron spreading current, and hole injection from the substrate is dominating the current. This is not immediately evident from the *I-V* diode characteristics of Fig. 3.7 where it is seen that the total current drops significantly with increasing laser energy. However, closer inspection of the 900 mJ/cm^2 curve shows that at a forward bias of about 0.7 V the current suddenly drops to *n-p* type values. This indicates that this diode is *n*-doped but fully-depleted and at this point the depletion is reduced enough to reveal active *n*-doping.

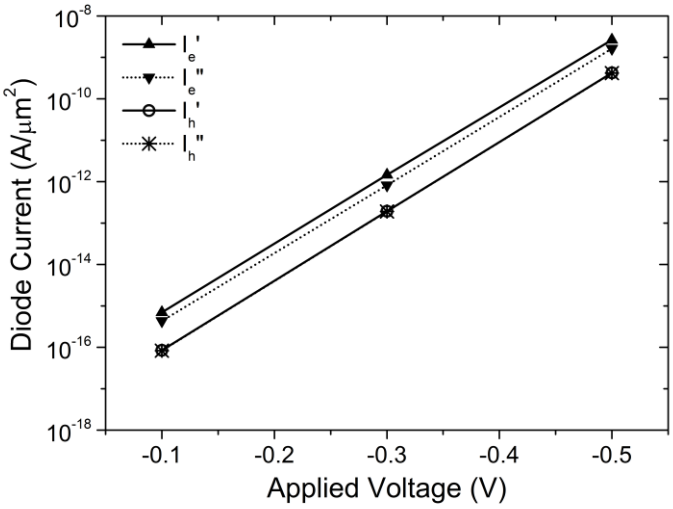


Fig. 3.8. Simulated electron and hole currents of which *I'* and *I''* are composed when the forward biasing is 0.1 V, 0.3 V and 0.5 V. All the diodes have d_{jun}=20 nm, N_D=1×10^{19} cm^{-3} and the substrate doping is N_A=1×10^{15} cm^{-3}.

For diodes annealed from 1000 to 1200 mJ/cm^2, the relative discrepancy is around 100%, which means that electron injection is dominating and these are non-depleted *m-n-p* junctions. In this way, this measurement method gives a very clear answer to the question of whether or not there is a significant *n*-doping of the surface. However, in many other practical cases the differences in current leading to the determined discrepancy are small compared to the diode leakage current. This may limit the usefulness of this measurement method and, alternatively, the method described in the next section could be applied.

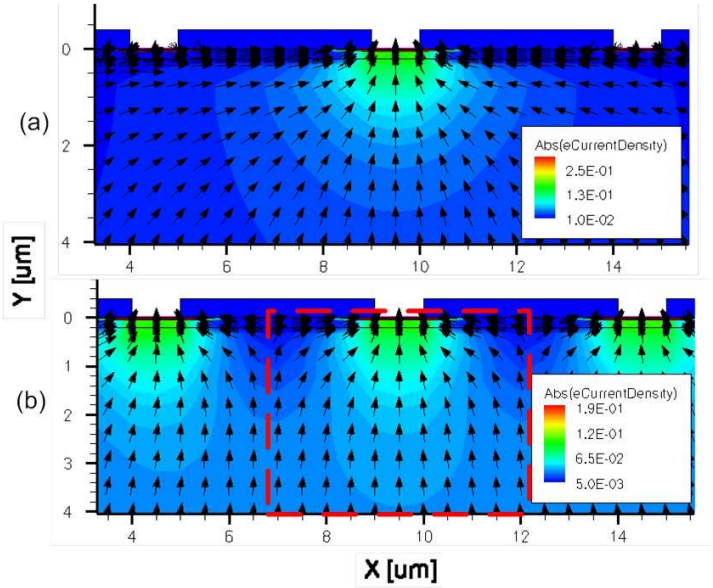


Fig. 3.9. Simulation of the electron current through 3 *n-p* diodes when (a) only the middle diode and (b) all 3 diodes are forward biased at 0.5 V.

Table 3.2. Current discrepancy in the parallel diode configuration for diodes annealed with different laser energies

Laser energy [mJ/cm^2]	Forward biasing		
	0.1 V	0.3 V	0.5 V
0	2.2%	--	--
600	0.2%	0.4%	--
700	1.8%	0.6%	--
800	0.3%	0.4%	--
900	3.1%	1.2%	--
1000	**96.7%**	**89.2%**	**76.5%**
1100	**92.5%**	**86.3%**	**78.1%**
1200	**95.7%**	**90.1%**	**80.0%**

3.4.3 Lateral-transistor characteristics

To achieve a measurement that is less sensitive to diode leakage, it can be profitable to bias the 3 diodes as the emitter or collectors. In this configuration, most of the injected minority carriers will flow parallel to the surface since the collector is functioning as a sink for the electrons; hence the name “lateral transistor”. The collector current can be described by [53]

$$I_c = J_{nE} \cdot A_{el} \cdot L_n / W_B \tag{3.2}$$

where J_{nE} is the electron current density of the emitter and A_{el} is the lateral area of emitter.

In Fig. 3.10, the Gummel plots are shown for the forward-biased transistors in the two extreme cases: (a) high laser-anneal energy giving non-depleted *m-n-p* diodes and (b) no laser anneal giving *m-p* Schottky diodes. In the latter case the base current is as high as expected from the diode *I-V* characteristics and the collector current is very low but measurable.

Device simulations are performed to investigate the origin of the collector current I_C. The Schottky barrier height to *p*-Si is set at 0.61 V as extracted from the *I-V* characteristics of the diode without laser annealing. The forward emitter voltage is swept from 0 to 1 V. The base contact is in all cases biased at 0 V, so the emitter-base voltage V_{EB} is just the applied emitter voltage. The collector contacts are biased at 0 V. From the simulation result for the collector current shown in Fig. 3.11, it is concluded that both electrons and holes contribute to the collector current. They increase with increasing V_{EB} and for small V_{EB} the hole current is larger than the electron current. As V_{EB} increases the hole current reaches an upper limit which corresponds to the reverse-bias current of the collector diode itself. The electron current keeps increasing and becomes the main current at a forward bias of 1.0 V.

For the Schottky diodes, minority carriers are always injected along with the thermionic emission of the majority carriers [54]. For a *p*-Schottky diode, the barrier height Φ_{Bp0} for majority carrier holes is independent of the biasing voltage. When the Schottky diode is forward biased at V_a, the barrier Φ_{Bn0} that prevents electrons in the metal from being injected into the semiconductor is lowered by a value of $q \cdot V_a$ as shown in Fig. 3.12, where q is the elementary charge. At the same time the electric field in the space-charge region is reduced and more electrons from metal side can then be injected into semiconductor to become excess minority carriers.

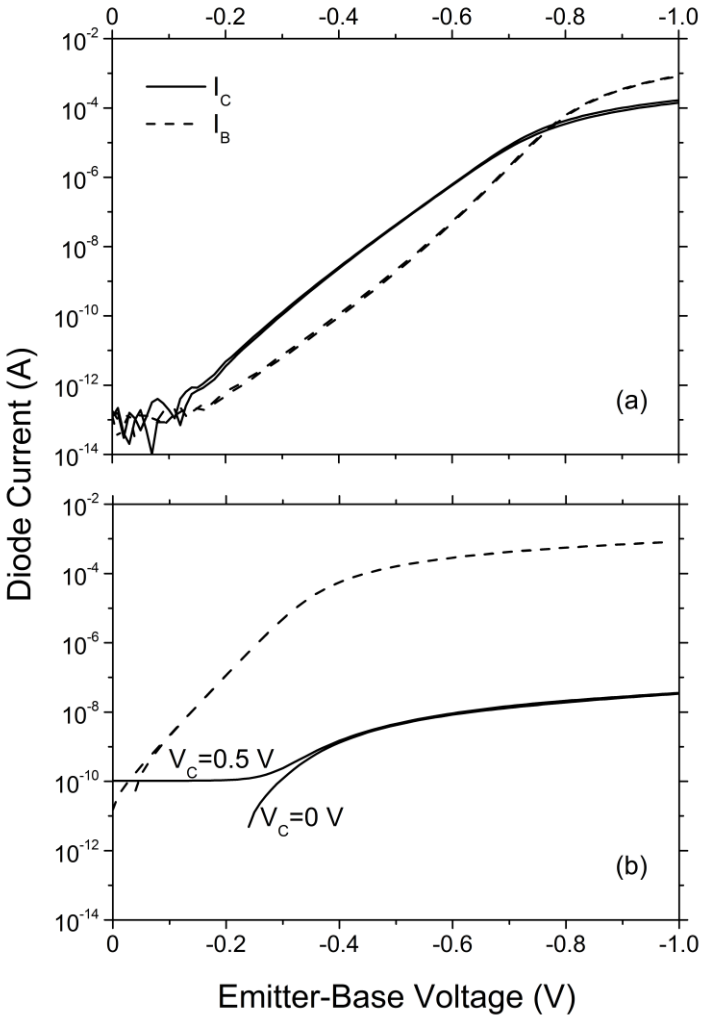


Fig. 3.10. Gummel plots of (a) an *npn* created by annealing at 1200 mJ/cm^2 and (b) a Schottky lateral transistor (no laser anneal).

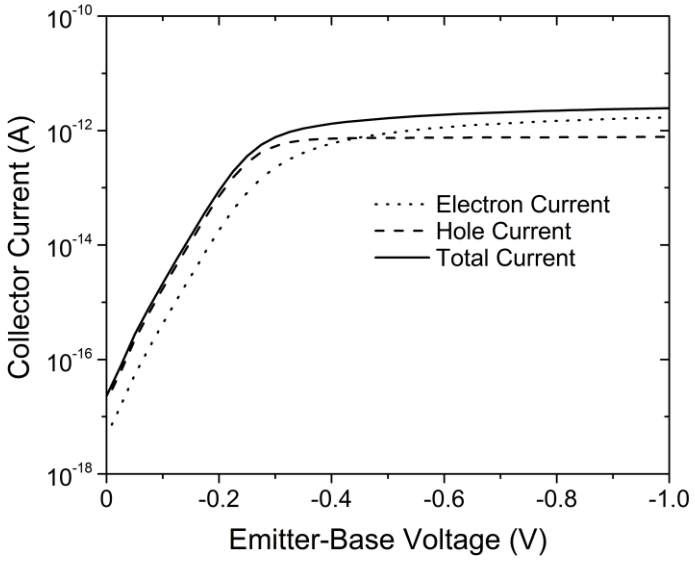


Fig. 3.11. Simulated collector current of a Schottky lateral transistor with V_{CB} = 0 V; the *SBH* is 0.61 V.

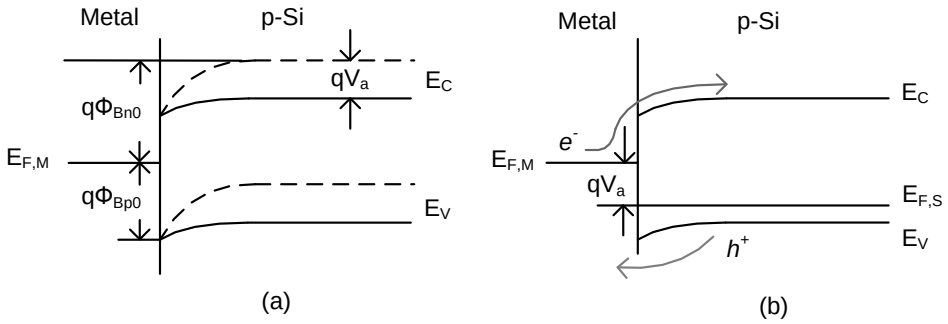


Fig. 3.12. Energy diagram of a Schottky diode under forward-bias (a) with the corresponding electron and hole injection indicated in (b).

Thus the origin of the collector current can be described as follows, the transportation process being illustrated in Fig. 3.13: under forward biasing, the emitter (Schottky) diode injects electrons from the metal side into the base region (*p*-Si). After diffusing across the base region, these electrons reach the collector (Schottky) diode that does not present a barrier for them and they are therefore collected by the collector diode. This process is also verified by device

simulations as the one shown in Fig. 3.14, where it should be noted that the electron flow is opposite to that of the current.

The injected excess electron concentration can be described as

$$\delta n_p = n_{p0} \cdot [\exp(V_a / V_T) - 1] \tag{3.3}$$

where n_{p0} is the minority carrier concentration under thermal equilibrium, V_a is the actual voltage drop over the emitter-base junction and V_T is the thermal voltage. Given that

$$V_{EB} = V_a + I_D \cdot R_S \tag{3.4}$$

where R_S is the diode series resistance. When the emitter diode current is high as in the Schottky case, the series resistance will have a large effect also on a small collector current. Therefore the bending off from the exponential characteristics is observed at very low forward-biasing for this current. Thus with the same dimension, the Schottky diode emitter injects fewer electrons into the base than the *p-n* junction diode emitter at -1.0 V since Schottky-diode sees the series resistance much earlier than the *p-n* junction diode.

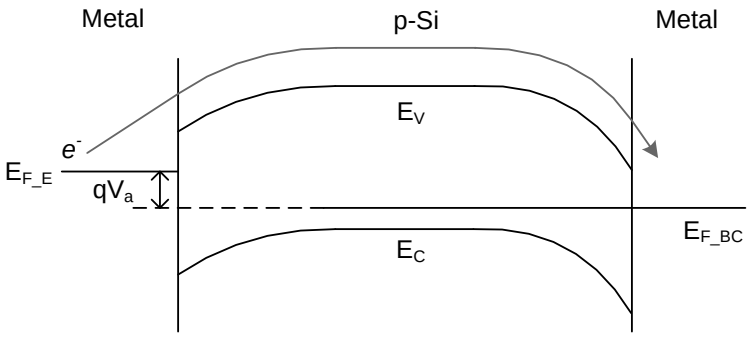


Fig. 3.13. Energy diagram along the surface of a Schottky lateral transistor illustrating the transport of electrons from the forward-biased emitter to the collector.

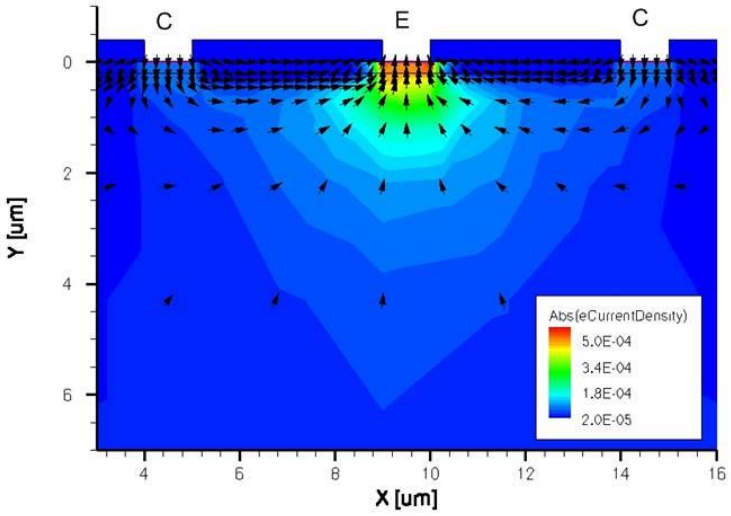


Fig. 3.14. Device simulation of the electron current in a Schottky lateral transistor with V_{EB} = -1.0 V, *SBH* = 0.61 V, and the substrate doping $N_A = 1 \times 10^{15}$ cm^{-3}.

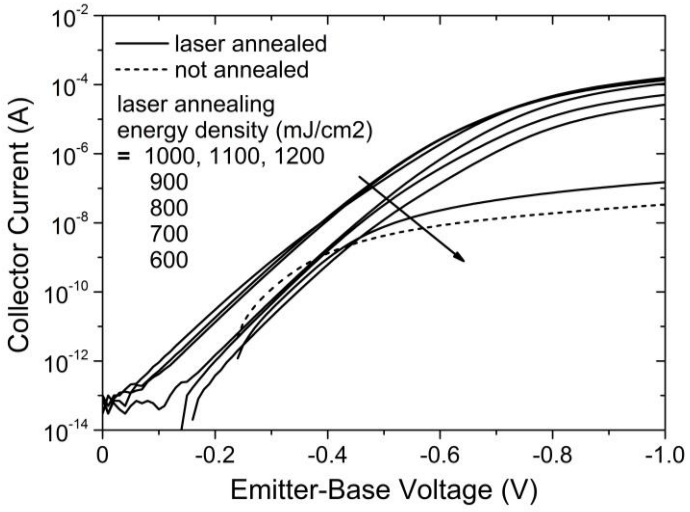


Fig. 3.15. Collector current measured in the lateral transistor configuration for diodes annealed at different laser energy densities, with W_E =1 μm, L_E=20 μm, W_B=4 μm.

In Fig. 3.15 the collector current is plotted for all laser energies. The very early bending off of the curves for the 0 and 600 mJ/cm^2 cases, shows that only in these two cases do we have the very high hole base current, much higher than

the collector electron current. In the other cases the electron current has a more significant contribution to the total current, showing that a doping of the surface is effectively increasing the barrier for hole injection.

3.5 Transition from *p*-Schottky to *p-n* Junction Characteristics

In Table 3.3 the results are summarized with respect to the type of junction behavior determined from the two measurement techniques. The non-annealed diode and the one annealed at 600 mJ/cm^2 display Schottky diode characteristics indicating that no effective counter-doping is present. For the diodes annealed at 1000-1200 mJ/cm^2, a complete counter-doping of the surface has been achieved, while the intermediate energies from 700-900 mJ/cm^2 have only resulted in a very shallow counter-doping. This only becomes an effective source of electron injection at large forward biasing below which these diodes behave as fully-depleted *m-n-p* junctions. This anomalous behavior is seen in the *I-V* characteristics shown in Fig. 3.16 for a diode annealed at 900 mJ/cm^2, where also a comparison is made to diodes either non-annealed or annealed at 1200 mJ/cm^2. From the forward biasing characteristics the *SBH* is estimated to be 0.82 V and 0.61 V for the 900 mJ/cm^2 and non-annealed cases, respectively. As described in [7], the modulation of the *SBH* by doping can be expressed as

$$\Delta\phi = \left(q \cdot N_d \cdot \alpha^2\right) \Big/ \left(2\varepsilon_s\right) \tag{3.5}$$

where $\Delta\Phi$ is the change in the *SBH*, N_d is the doping concentration of the *n*-doped region, ε_S is the permittivity of Si and α is the doping depth. Assuming N_d to be equal to 10^{19} cm^{-3}, then the corresponding doping depth α would be 5.1 nm. This is close to the expected width, ~ 7.5 nm, of the depletion at the metal-Si interface at zero bias. Thus under small forward bias the *n*-region is fully depleted by the metal-semiconductor depletion region and the diode shows the electrical characteristics of a *p*-Schottky. However, the current is much lower than the pure Schottky junction case without laser annealing due to the high effective *SBH*. When increasing the forward-bias voltage, the current increases exponentially with the applied voltage but at the point ① in Fig. 3.16 the diode current starts to saturate. The current level at this point is more than one decade lower than at the points ② where the series resistance starts to limit the diode

current. This abnormality suggests that at point ① the depletion region width becomes smaller than the doping depth so that the heavily doped *n*-region becomes undepleted. With a further increase of the forward-bias voltage, the diode behaves just like a *p*-*n* diode conducting a diffusion current.

Table 3.3. Type of diode behavior for diodes annealed with different laser energies

Laser energy [mJ/cm^2]	Forward biasing		Type of diode behavior
	0.1 V	1.0 V	
0	Schottky	Schottky	*m*-*p* Schottky
600	Schottky	Schottky	
700	Schottky	*p*-*n*	fully-depleted *m*-*n*-*p*
800	Schottky	*p*-*n*	
900	Schottky	*p*-*n*	
1000	*p*-*n*	*p*-*n*	omhic-contacted *m*-*n*-*p*
1100	*p*-*n*	*p*-*n*	
1200	*p*-*n*	*p*-*n*	

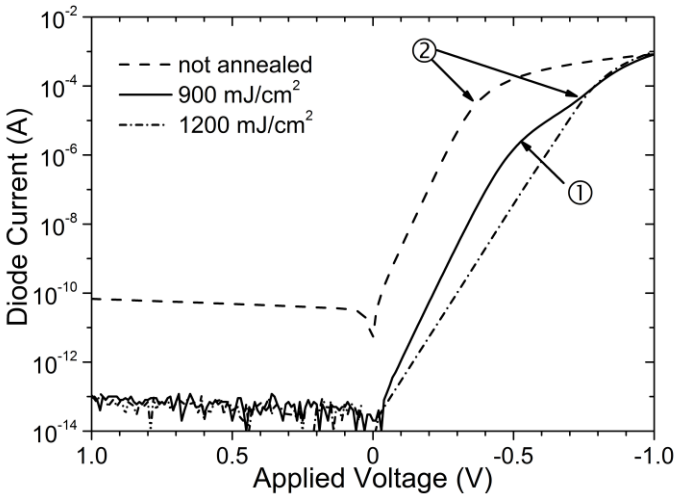


Fig. 3.16. Measured *I*-*V* characteristics for a diode annealed at 900 mJ/cm^2 and the comparison to diodes that are either non-annealed or annealed at 1200 mJ/cm^2. The diode area is 20×1 μm^2.

3.6 Test structure Layout Considerations

The sensitivity of both the parallel-diode and the lateral-transistor measurement methods is increased by minimizing the distance between the emitter and collector as well as by minimizing the parasitic currents that do not contribute to the interaction between the emitter and collector, i.e., the area of the diodes should be minimized. As already touched upon in Section 3.4.2, for the parallel-diode configuration the measurements will only be effective if the level of non-ideal leakage currents does not dominate over the ideal currents spreading into the substrate. For this reason it can also be advantageous to work with minimum dimension diodes. These design guidelines are the same as those for optimizing the current gain of lateral *pnp* transistors, for which the most optimal and compact structure is known to be a minimum dimension (circular) emitter surrounded by a single minimum-dimension ring-shaped collector placed as close as possible to the emitter. For such a configuration the collector would be able to collect as much as possible of the laterally diffusing minority carriers, which will make the structure more effective. Nevertheless, for the lateral-transistor measurement method, punch-through of the base should be avoided by a having sufficient integral base doping.

Here the only available test structures are the finger diode structures. With these the influence of the layout parameters could be illustrated by the measurements presented in Fig. 3.17 and Fig. 3.18, where the results for a *m-p-n* diode annealed at 1200 mJ/cm^2 are compared to those of a non-annealed *m-p* Schottky diode. In Fig. 3.17 the diode length L_E is varied from 1 to 40 µm of all the three diodes while the width W_E is fixed at 1 µm. In Fig. 3.17a it is seen that $\Delta I/I'$ decreases with increasing L_E, which is understandable since the perimeter to area ratio is decreasing and the weight of the perimeter current is lowered. In contrast, the Schottky diodes display a very small $\Delta I/I'$ over the whole range as would be expected. For the corresponding lateral-transistor collector current shown in Fig. 3.17b, the collector current increases linearly with L_E, in accordance with (3.2) where

$$A_{el} = L_E \cdot d_{jun} \tag{3.6}$$

In Fig. 3.18 the W_E of the middle diode is varied from 1 to 40 µm while the L_E is fixed at 40 µm. This gives a significant decrease of the perimeter to area ratio and accordingly for *p-n* junction diodes, there is a considerable decrease in

ΔI/I' that becomes less than 20% for the large 40×40 μm^2 diode. For the lateral-transistor configuration the collector current of both the *p-n* junction diodes and the Schottky diodes is seen to be significantly lowered by increasing W_E. The increasing emitter area will entail an increase in emitter current for the same forward biasing and thus the diode current will be attenuated by the series resistance at a smaller forward biasing voltage. Therefore, the actual voltage over the emitter-base diode is lowered as in (3.4) and the injected minority carrier concentration is lowered as in (3.3). This leads to a lower collector current as seen in Fig. 3.18b, showing that it is preferable to use a minimum value for W_E.

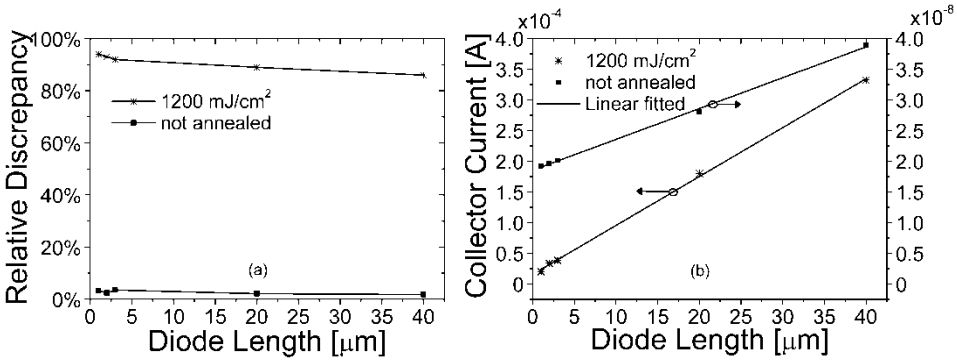


Fig. 3.17. (a) The current discrepancy measured in a parallel-diode configuration with a forward bias of 0.3 V and (b) the collector current in the lateral-transistor configuration for both an *npn* created by annealing at 1200 mJ/cm^2 and a Schottky lateral transistor (no laser anneal) for an L_E from 1 to 40 μm with a fixed W_E = 1 μm.

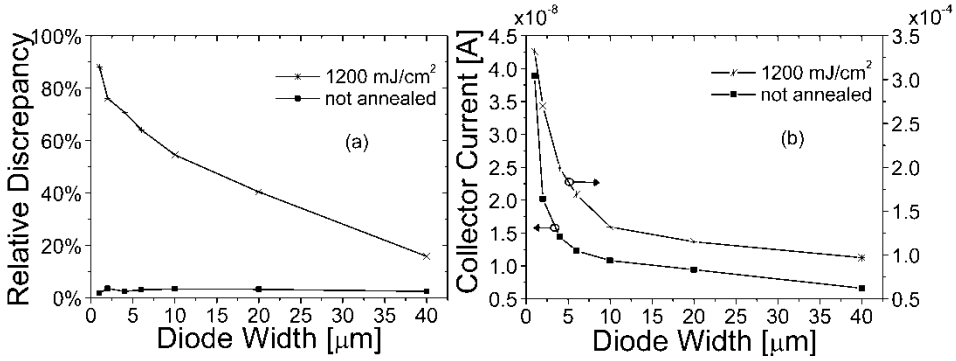


Fig. 3.18. (a) The current discrepancy measured in a parallel-diode configuration with a forward bias of 0.3 V and (b) the collector current in the lateral-transistor configuration for both an *npn* created by annealing at 1200 mJ/cm^2 and a Schottky lateral transistor (no laser anneal) for a W_E from 1 to 40 μm with a fixed L_E = 40 μm.

3.7 Test Structures applied to PureB Depositions

In the past PureB deposition at 700 ℃ was investigated using vertical *pnp* structures [26, 41]. With a series of vertical *pnp* with emitter lengths of about a micrometer and larger it is quite straightforward to accurately determine the Gummel number of the laterally uniform part of the emitter region formed by the PureB deposition. This is because the laterally uniform base and collector regions under the emitter scale with the emitter. From such measurements it was concluded that the PureB emitter Gummel number was comparable to that of conventional heavily-doped implanted emitters, and corresponded to a total doping of about 10^{15} cm^{-3}.

In the lateral *pnp* test structures the focus in this chapter has been on the presence of a hole current being injected into the substrate forming the base, which, for the bipolar measurement configuration corresponds to a collector current. In this set-up, the effectiveness with which the I_C is collected depends on the exact base width W_B. The wider the base, the more current will be running as a diode current between the emitter and base connected at the back of the wafer. This also means that the minority carrier current injected into the emitter cannot be separated from the high emitter-base diode current. Therefore the lateral bipolar test structures are not readily suited for extracting the emitter Gummel number.

Both the 700 ℃ and 400 ℃ depostions were evaluated using the lateral bipolar test structure. As observed in the previous chapter, for a low-temperature PureB diode deposited at 400 ℃, although the electrical behavior is more like a Schottky diode as shown in Fig 2.12, but it exhibited *p-n* junction like behavior with high minority carrier injection level as shown in Fig. 2.14. Here, lateral bipolar test structures have been fabricated with PureB diodes of which the PureB layer is deposited at 400 ℃ or 700 ℃, under the same condition as described in Section 2.3.1. With the parallel-diode characteristics method as discussed earlier, the current discrepancy of the 700 ℃ deposited 40×1 μm^2 PureB diode is more than 80%, while for the 400 ℃ deposited PureB diode, the discrepancy is only 3%, suggesting a Schottky-diode behavior, which is in consistence with the result shown in Fig. 2.12.

Lateral-transistor characteristics are shown in Fig. 3.19 for both high temperature and low-temperature deposited devices and are compared to

measurements using vertical *pnp's*. Both structures with 700 ℃ deposited PureB emitters have similar minority carrier injection level. However, the base current of the vertical *pnp* is smaller than that of the lateral *pnp*. This is due to the fact that not all the injected minority carriers go to collector because some of them are attracted directly to the base contact, thus becoming part of the base current in the lateral *pnp*.

As shown in Fig. 3.19b, although the base current levels of vertical and lateral *pnp's* with 400 ℃ deposited PureB emitters are quite high, the emitters still inject minority carrier holes into the substrate and the collector current level is similar to the 700 ℃ deposited device. This result suggests that there is an effective *p*-doping. The base currents are higher than the 700 ℃ case but much lower than the Schottky case, suggesting that the metal is only partly playing a role. To understand the difference, in the next chapter a study of the as-deposited layers without influence of metal will be conducted.

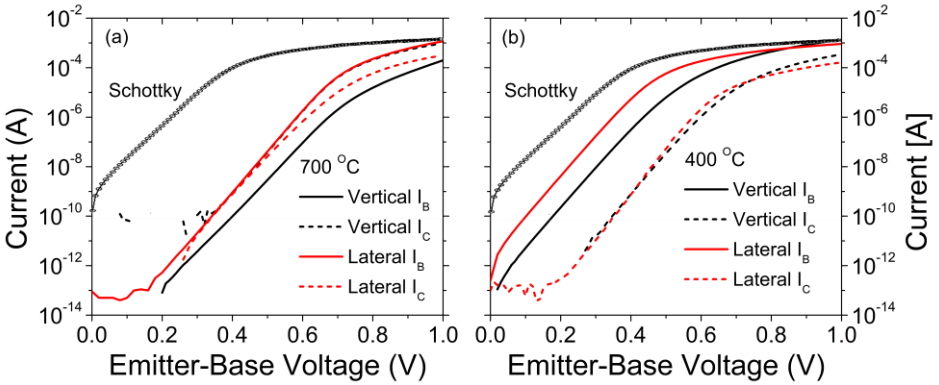


Fig. 3.19. Gummel plot of PureB lateral and vertical *pnp* bipolar transistors with (a) 700 ℃ deposited PureB emitters and (b) 400 ℃ deposited PureB emitters. The emitter area is 40×1 μm^2 and a Schottky diode current with the same emitter dimension is plotted for comparision.

3.8 Conclusions

The presented lateral-transistor test structure is straightforward to fabricate and use. The experimental results, supported by simulations, demonstrate that the *I-V* measurements made possible by different biasing of the structure give a means of determining the separate hole and electron currents through the diode.

The lateral-transistor measurement configuration is more robust with respect to non-ideal diode leakage currents than the parallel-diode configuration. However, the parallel-diode structure is more robust with respect to the influences of substrate depletion and associated doping levels. The evaluation of the minority carrier injection level into the substrate provides valuable information on the effective doping of the diode surface. For the series of laser-annealed diodes studied here, it was possible to distinguish between the pure Schottky and *p-n* junction case as well as identify an intermediate region where the surface doping is fully-depleted under certain bias conditions. With these methods, the low temperature, 400 ℃, deposited PureB diodes have also been studied, although the single diode *I-V* and parallel-diode characteristics show Schottky-like behavior, the lateral-transistor characteristics suggest that the device has *p-n* junction-like behavior. The methods have also been successfully used in [55, 56] to verify minority carrier injection in diodes made with new deposition techniques.

Chapter 4

Sheet Resistance along the PureB Layer and Si Interface

It is well-established that 700 ℃ pure boron (PureB) depositions on Si can form ideal, nanometer shallow p^+-n junctions with leakage currents as low as those of conventional implanted/diffused junctions. Recently, similar qualities were also demonstrated for a PureB deposition temperature of 400 ℃ [39]. The PureB is deposited at temperatures from 400 ℃ - 700 ℃ and varying deposition times and the high-resolution transmission-electron-microscope (HRTEM) images of the interface with Si are shown in Fig. 4.1 where an alignment of each B-atom to a Si-atom is visible for all temperatures. Therefore, even though the PureB layer is amorphous the termination at the Si interface has a distinct regular ordering. In this case, it has been proposed that the chemical bonding of the B atoms to the Si atoms of a 400 ℃ PureB deposition at the surface creates a monolayer of acceptor states filled with electrons. This attracts holes to the interface forming an inversion layer that can account for *I-V* characteristics of the 400 ℃ diodes: for the first, the Gummel number of the p^+-region is very high and corresponds well with the number of atoms on the Si surface, ~ 10^{15} atoms/cm^2, and secondly, the gradient of the hole concentration gives a high electric field up to the surface that increases photodiode responsivity by suppressing the injection of electrons into the anode.

The fact that the 400 ℃ deposition can be applied as a post-metallization step makes this a particularly interesting process module for integration of potent photodiodes in CMOS. However, for the design of high-speed detectors it is critical that the lateral sheet resistance of the anode can be made low enough, something that is not obvious for the 400 ℃ deposition where there is no doping of the bulk Si.

Part of this chapter have been published in *IEEE Electron Device Lett.*, **36**, 102 (2015) [57]

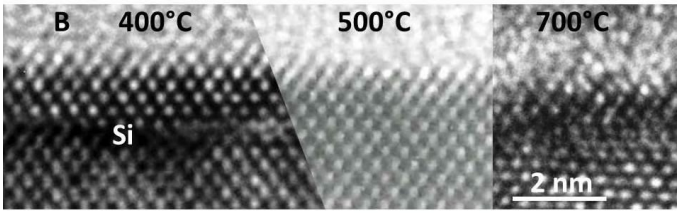


Fig. 4.1. HRTEM images of the PureB-to-Si interface for layers grown at 400 ℃, 500 ℃ and 700 ℃.

In this chapter, the design and fabrication of in-line structures for sheet resistance measurement of the Si under the PureB layer are presented. The goal was monitor the as-deposited layer by designing structures that are suitable for probing with needles directly on the Si, thus avoiding all post-processing steps. In this way the sheet resistance resulting from a 400 ℃ PureB deposition could be investigated and compared to PureB diodes deposited at higher temperature. It was also possible to investigate the influence of post-deposition processing steps.

4.1 Test Structures for Sheet Resistance Measurement

4.1.1 Fabrication

Two main types of test structures were designed and fabricated in a simple process flow as shown in Fig. 4.2 that allowed electrical *I*-*V* measurements directly after the PureB deposition. Only 2 masking steps are required. The starting substrates are of (100) 1-10 Ωcm *n*-type Si wafers that are first thermally oxidized to a layer thickness of 235 nm. Then 0.5-μm-deep *p*-type probe-needle contact regions with a surface doping of 10^{19} cm^{-3} are formed by B^+ implantation and annealed in argon gas for 20 min at 950 ℃. Windows to these regions and all other regions to be deposited with PureB are then opened. The opening of these regions is very crucial since any damage to the silicon surface will affect the quality of the PureB deposition, which can lead to enormous difference in the sheet resistance measurements, especially for the low-temperature deposition like 400 ℃. Thus these structures can also be used to monitor the quality of the PureB deposition. Here we open the windows with wet landing on Si in HF 0.55%. The native oxide is removed by dip etching in HF 0.55% followed by Marangoni drying and the PureB layer is then deposited at 400 ℃，500 ℃ and 700 ℃ separately for various times. At the end the

devices are alloyed in the forming gas at 400 ℃ to improve the contact of PureB layer to the silicon surface.

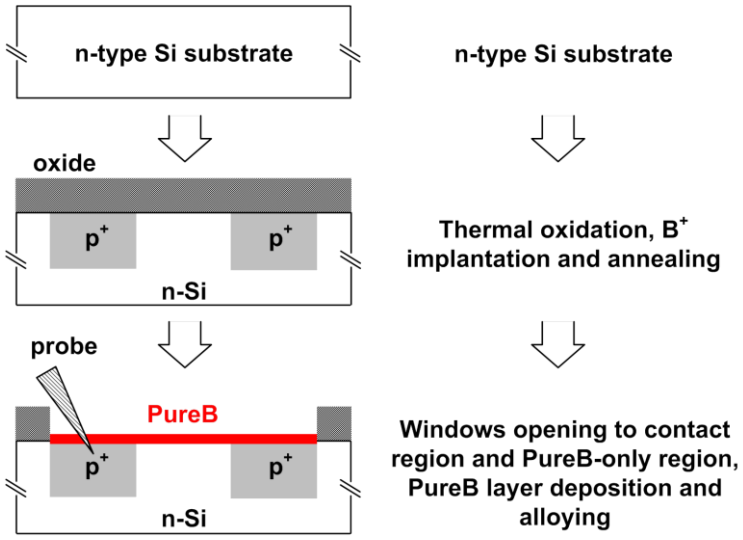


Fig. 4.2. Schematic process flow for fabrication of the contact region and PureB-only region of the sheet resistance measurement structures.

4.1.2 Verification of test structures

A Van der Pauw Sheet Resistance Test Structure

The designed and fabricated Van der Pauw structure is shown in Fig. 4.3. These are the preferred test structures for monitoring R_{SH} because they can be measured currentlessly with, in principle, a single measurement that is independent of the series resistance through the contacts. For probing we use four tungsten needles that will easily penetrate the PureB layer to reach the p^+-implanted region. Experiments have shown that all PureB layers, independent of deposition temperature from 400 ℃ to 700 ℃, make ohmic contact to the Si [28]. Therefore, the overlap between the corners of the central square and the p^+-contact regions ensures the electrical connection to the PureB layer to be monitored. By forcing the current (I) through two of the neighboring contacts and by measuring the voltage drop (V) across the other two contacts, the sheet resistance value can be extracted as:

$$R_{SH} = 4.53 \bullet V/I \tag{4.1}$$

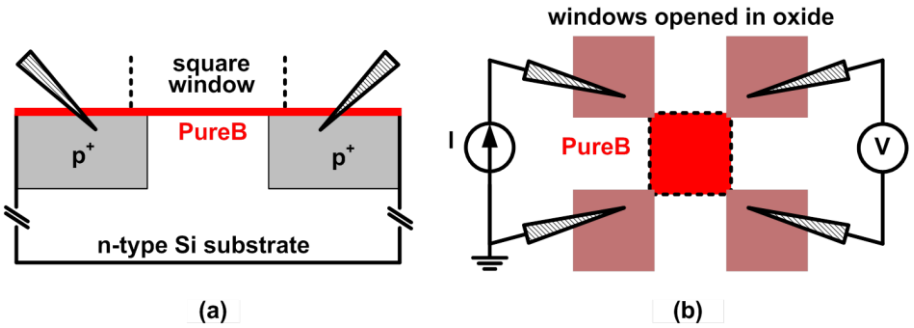


Fig. 4.3. Schematic cross section (a) and layout (b) of the Van der Pauw sheet resistance test structure.

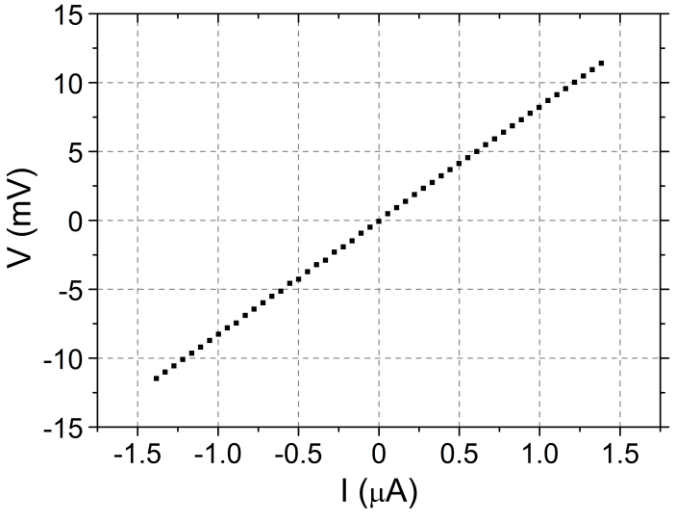


Fig. 4.4. Measurement results of a 20 min PureB deposition at 400 ℃. The sheet resistance is 36.3 kΩ/sq.

The measurement results of a 20 min PureB deposition at 400 ℃ is shown in Fig. 4.4, the results have shown a very good linear relation between the measured voltage and the forced current, indicating that a robust measurement has been achieved, giving a sheet resistance value of 36.3 kΩ/sq.

To eliminate the possibility that the measurement is measuring the surface conducting channels, the measurement is performed again after the surface is covered with photoresist, the sheet resistance R_{SH} remains the same, indicating

that the measurement is actually measuring the interface between the PureB and silicon surface.

B. Ring Sheet Resistance Test Structure

To be sure that the Van der Pauw R_{SH} is reliable, sets of circular ring-shaped structures were also designed with the basic design illustrated in Fig. 4.5. Each ring structure has a fixed radius of 164 µm so the total perimeter is always the same despite of the different width of the rings. Sets of each 5 ring structures are designed as in Fig. 4.6 with the ring width L equal to 10 µm, 20 µm, 40 µm, 100 µm, and 200 µm.

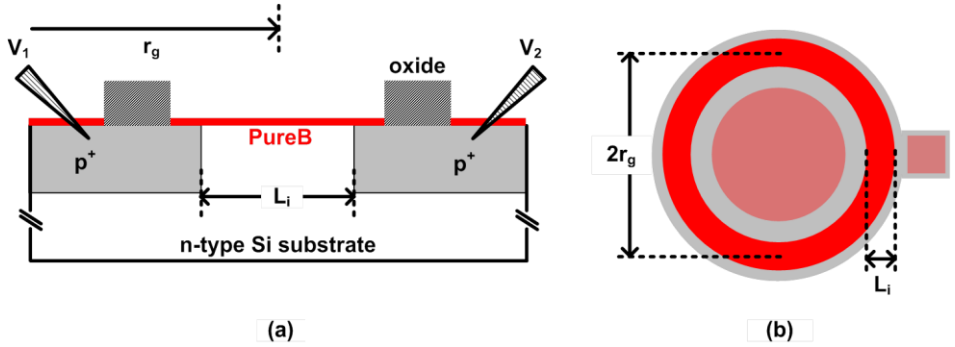


Fig. 4.5. Schematic cross section (a) and layout (b) of the ring sheet resistance measurement structure. The perimeter of the PureB-only region is constant and equal to $2\pi r_g$.

Sets of different types of ring structures are designed. The first type has a p^+-ring covering the whole perimeter region as illustrated in Fig. 4.6a. This is done for 2 reasons: for the first, any perimeter leakage due to a deficient PureB coverage at the oxide window is then eliminated, and, secondly, if the R_{SH} is very high, the low-ohmic p^+-ring will nevertheless ensure a rotational symmetric current flow from the inner to outer p^+ ring. In other sets of ring-structures, the p^+-ring is removed as shown in Fig. 4.6b. With these, any diode leakage problems at the oxide perimeter can be identified, which, due to the expected high R_{SH}, may become significant even at low levels. If these sets deliver R_{SH} measurements similar to the p^+-ring sets, it can be concluded that parasitic series resistance and leakage current are not influencing the measurement.

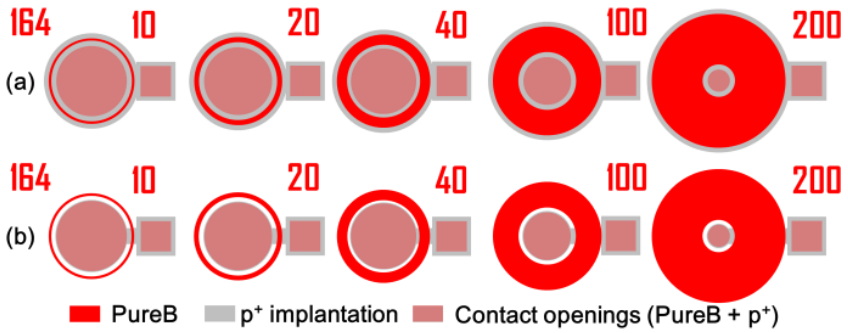


Fig. 4.6. Mask layout of a set of ring structures for sheet resistance measurement. The (a) structures have a p^+-ring covering the PureB ring perimeter and for the (b) structures this p^+-ring is omitted.

To extract the R_{SH} a differential measurement technique is applied as described in [58] to eliminate the series resistance associated with the contacts that cannot be measured directly. Since the sets of ring structures are designed with an identical total perimeter, only two variables are important for the extraction, i.e., R_{mi}, the measured resistance from the *I-V* measurement, and the ring width L_i, where the indices $i = 1,\ldots,n$ refer to each specific test structure in the given set of n structures. For the following calculations the structures are organized so that $L_i < L_{i+1}$ and $i < j$. Since the structures are ring-shaped, the radial spreading of the current in the perimeter regions γ_{ij} must be taken into account. In this paper, we take the approximation $L_i << L_j \cong r_g$ as described in [58], so the sheet resistance R_{SH} can be calculated as:

$$R_{SH} = \frac{R_{ij}}{\gamma_{ij}} = \frac{R_{mj} - R_{mi}}{\gamma_{ij}} \tag{4.2}$$

where R_{ij} is the differential resistance between 2 ring structures and

$$\gamma_{ij} = \frac{1}{2\pi} \ln\left(\frac{(r_g - \frac{1}{2}L_i)\cdot(r_g + \frac{1}{2}L_j)}{(r_g + \frac{1}{2}L_i)\cdot(r_g - \frac{1}{2}L_j)} \right) \tag{4.3}$$

The measurement results are shown in Fig. 4.7 for a 20 min PureB deposition at 400 ℃. To compare the result with the previous extracted sheet resistance value in Fig. 4.4 with the Van der Pauw structure, the measured device is from the same die of the wafer to minimize the influence of the deposition non-uniformity. The measurements are performed with the structures

in Fig. 4.6a, and from the measurement results in Fig. 4.7, the R_{ij} and γ_{ij} are very well linearly correlated, giving a sheet resistance R_{SH} equals to 37.8 kΩ/sq, which is very close to the extracted value with the Van der Pauw structure. And the same measurements and extraction are performed with structures in Fig. 4.6b too, giving very similar results.

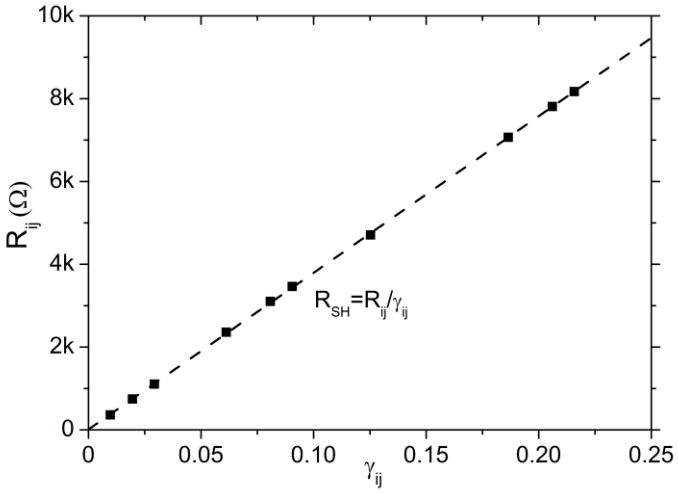


Fig. 4.7. Differential resistance measurements with linear fit (dashed line) for a 20 min PureB deposition at 400 ℃. The sheet resistance R_{SH} equals to 37.8 kΩ/sq.

The R_{SH} values measured on the same die with either the Van der Pauw or ring-structures are compared in Fig. 4.8 for 20-min PureB deposition at 400 ℃, 500 ℃ and 700 ℃. The measured R_{SH} values at each temperature follow each other closely and the small discrepancy can be accorded to the non-optimal design of the Van der Pauw structure [59]. In any case there was no indication that undesirable parasitics are playing a role.

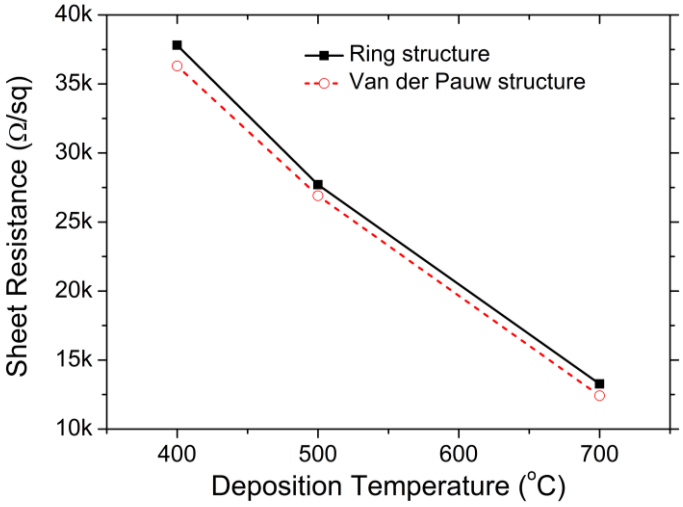


Fig. 4.8. Extracted sheet resistance of a 20-min PureB deposited at 400 ℃, 500 ℃ and 700 ℃ as measured with the two types of test structures.

4.2 Sheet Resistance of the *p*-type PureB Region

From the ring structures, a very accurate determination of the R_{SH} can be made but the extraction requires five *I-V* measurements and a complex calculation. With the Van der Pauw structure a quick measurement over the whole wafer can be made. The PureB layer itself has a sheet resistance in the 10^8 Ω/sq range [60] and therefore does not contribute to the measured R_{SH} values shown in Fig. 4.9 for different deposition temperatures and substrate biasing. At 700 ℃ the R_{SH} of ~10 kΩ/sq is dominated by the B doping of the bulk Si during the deposition, the limits of which are set by the solid solubility of $2x10^{19}$ cm^{-3} and the deposition time [26].

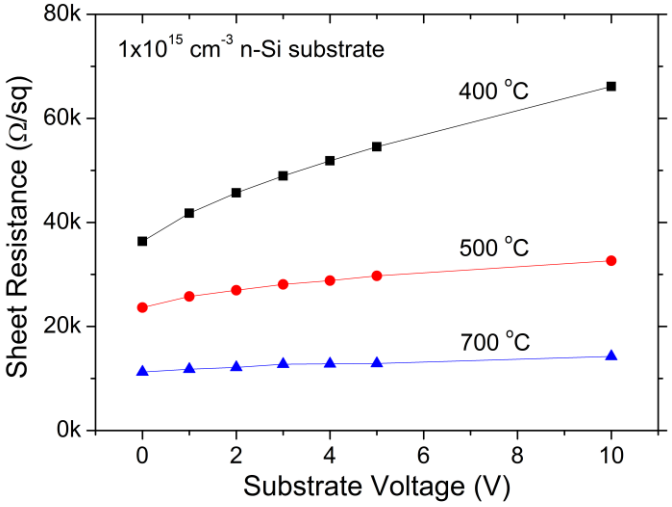


Fig. 4.9. Measured sheet resistance of PureB depositions for a 20 min deposition as a function of deposition temperature and substrate voltage.

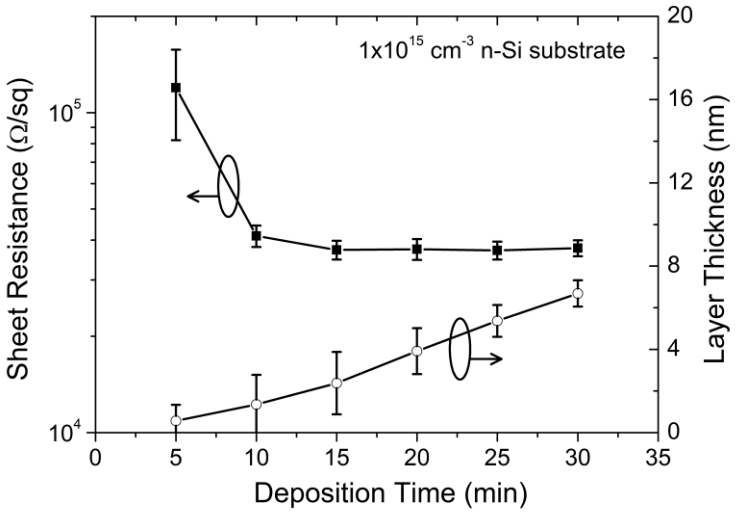


Fig. 4.10. Measured sheet resistance of PureB depositions as a function of deposition time at 400 ℃, with error bars indicating the standard deviation for across-the-wafer values and deposited layer thickness with error bars indicating the roughness.

From many other experiments with less ideal conditions it was found that a non-perfect deposition surface, for example with native oxide residues, or post-processing damage of the PureB layer would invariably increase the R_{SH}. This is presumably due to rupturing of the interface acceptor coverage exposing the charge carriers to defects. The effect of a non-perfectly covered interface can also be seen from the results shown in Fig. 4.10 where the 400 ℃ R_{SH} is plotted as a function of deposition time. For the short deposition times, where an imperfect coverage is expected, the R_{SH} goes up to ~100 kΩ/sq. For a 15-min deposition giving a layer thickness of 2.3 nm and longer depositions, the R_{SH} value stabilizes at 37 kΩ/sq. This value is reproducible from run to run with low spread across the wafer and it substantiates that the bulk Si is not being doped via a thermal diffusion process at 400 ℃ but instead it is the first monolayer coverage with B that determines the conductance along the interface.

The results can be explained in a simple model assuming a monolayer of acceptor states at the interface that fill with electrons to give a monolayer of fixed negative charge. Furthermore, it can be assumed that the high resistivity of the very thin PureB layer acts as a semi-insulating layer allowing an inversion layer of holes to be built up as illustrated by the energy band diagram in Fig. 4.11. The monolayer of *n*-charge represents a very high electric field that binds the holes to the interface and limits their mobility similar to the way a vertical electrical field attenuates the inversion layer mobility in MOS devices [61]. The holes furthest away from the interface will have the highest mobility and may dominate the lateral conductance. From a simplistic calculation using bulk Si mobility values, the number of holes needed to provide the measured conductance would be about $5x10^{11}$ cm^{-2}. In fact, a significant decrease in conductance is measured when the substrate doping is increased or if a reverse bias is applied as seen in Fig. 4.9. The bias-dependent decrease fits well with an increasing depletion of holes in the 10^{11} cm^{-2} range. For increasing substrate doping, an attenuation of the hole mobility must be taken into account. The relationship between bulk values of hole mobility, calculated as in [62], and the measured sheet conductance is plotted in Fig. 4.12. It is almost linear as would be expected for holes moving in the bulk Si away from the interface.

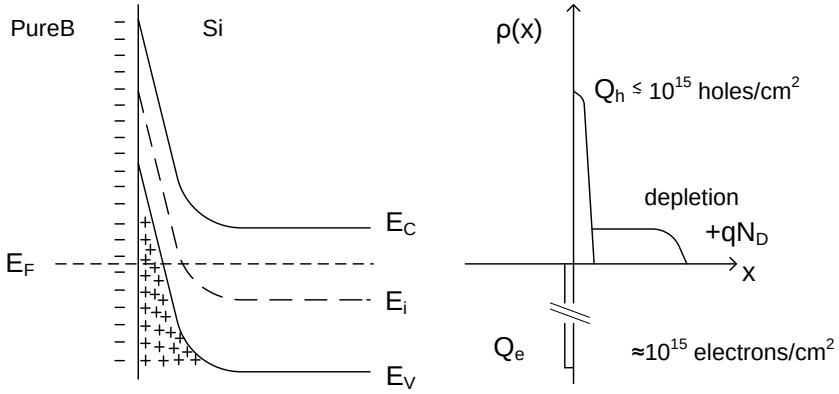


Fig. 4.11. Energy band diagram (left) and charge distribution (right) illustrating the proposed model that a monolayer of acceptor states is formed at the PureB-Si interface. The fixed electrons at the interface are indicated with (-) and the inversion layer distribution of holes with (+).

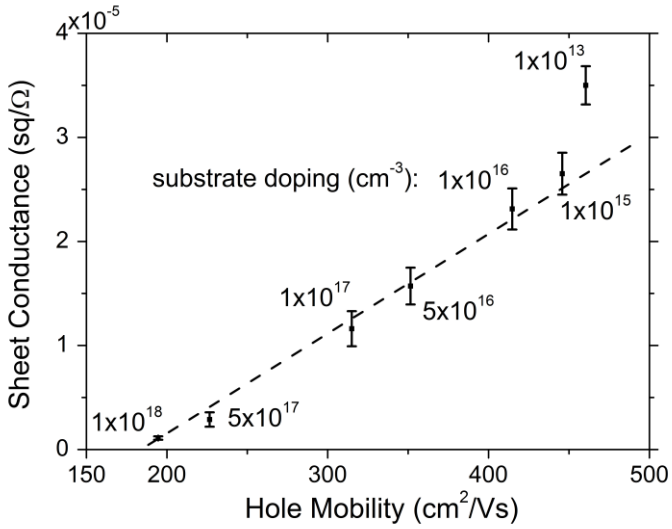


Fig. 4.12. Measured sheet conductance with linear fit (dashed line) for a 20 min PureB deposition at 400 ℃ as a function the hole mobility as calculated for the given *n*-doping of the substrate. The exact doping level of the almost intrinsic substrate marked 10^{13} cm^{-3} is uncertain.

4.2.1 Comment on perimeter *I-V* behavior

If a layer of holes is created at the PureB-Si interface it means that the perimeter will mark an abrupt termination of this layer, reducing the Gummel number at this point. The effect of this would be a relatively high injection of electrons from the substrate into the *p*-region of a PureB diode at the perimeter. This effect can in fact explain the effect of introducing a p^+ guard ring at the diode perimeter that is seen in the diode *I-V* characteristics shown in Fig. 2.8. The diode saturation current is reduced by about 2 decades when a guard ring, which represents a high Gummel number, is added. Notably, the effect is exactly the same for both a 400 ℃ and a 700 ℃ deposition, which supports the model that it is the interface bonding between the B and Si atoms that is electrically important in both cases. A similar shift of the current level is seen in Fig. 2.12 for a 700 ℃ PureB diode without guard ring when the perimeter of the diode window is covered with oxide. In this way the metal sink for electrons is replaced by a wide bandgap material which is also a way of increasing the perimeter Gummel number.

4.2.2 Temperature dependent measurements

In Fig. 4.13 temperature dependent measurements of the R_{SH} are shown along with the temperature coefficient

$$\alpha = \left(R_{SH2} - R_{SH1}\right) \Big/ R_{SH1} \bullet \left(T_2 - T_1\right) \tag{4.4}$$

where the sheet resistances R_{SH2} and R_{SH1} are measured at temperature T_1 = 25 ℃ and T_2, respectively. The α are negative for all PureB deposition temperatures, with values ranging from -0.11/℃ to -0.001/℃. In general Si resistors will have a negative α of about -0.07/℃ when the defect level is insignificant [63]. For implanted/diffused resistors α is mainly positive due to the influence of impurities/defects and for high-ohmic resistors the charging/de-charging of bulk and particularly surface defects gives a high variability that limits the tolerance. In contrast, for deposition on a clean Si surface the 400 ℃ PureB conductance is found to be very stable.

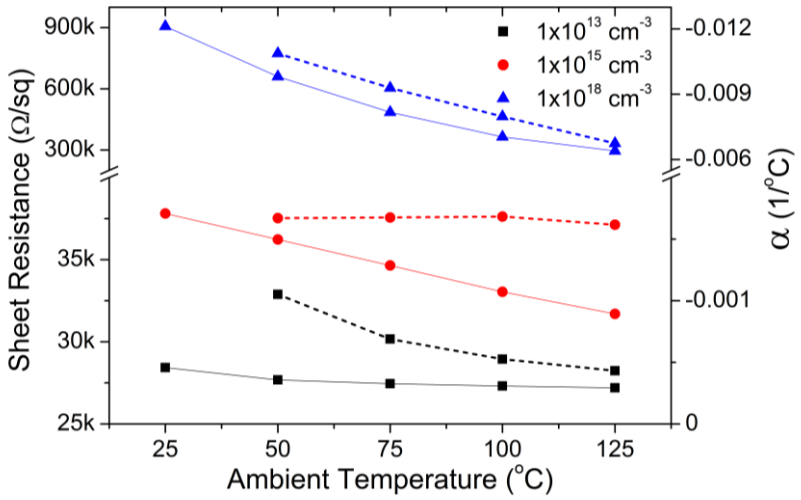


Fig. 4.13. Measured sheet resistance (solid lines) and temperature coefficient (dashed lines) of a 20 min PureB deposition at 400 ℃ as a function of ambient temperature for several substrate doping concentrations.

4.3 Influence of Post-Processing Steps

With the Van der Pauw structure fast in-line R_{SH} measurements can be made. The influence of the post-processing after PureB deposition can also been evaluated in terms of R_{SH}. When the PureB layer is integrated as a light entrance window in the front-end processing [38], several post-processing steps will be performed, including (i) 10-min metal cleaning in HNO3 99%, (ii) metal sputtering of pure Al followed by removal in HF 0.55% and (iii) alloying in forming gas at 400 ℃ to improve metal to PureB contact. Although the PureB has an extremely low etch- rate in both buffered and diluted HF, thin spots, for example due to contamination on the Si surface, may become pin-holes if the etching is not stopped in time. Where a pin-hole exposes the Si to air, oxide may form and become a source of generation-recombination centers.

The measurement results are shown in Fig. 4.14. The R_{SH} for the 700 ℃ PureB device is essentially independent of any extra processing steps. In contrast, for the 400/500 ℃ devices, the metal cleaning step nearly removed all the deposited PureB so that the R_{SH} could not be extracted. The R_{SH} of the 400 ℃ device increased significantly after metal removal while the 500 ℃

showed only a slight increase. This is related to the surface roughness that is also associated with a higher density of pin-holes. These allow the deposited metal to reach and deteriorate the PureB-Si interface.

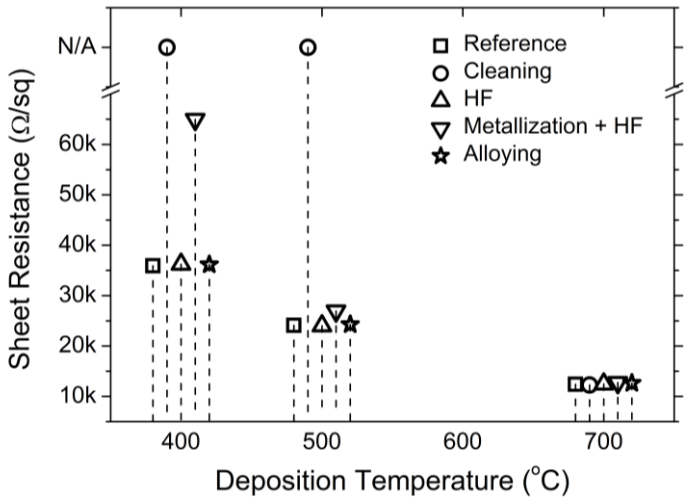


Fig. 4.14. Measured sheet resistance of 20-min PureB diodes depositied at 400 ℃, 500 ℃ and 700 ℃ with different post-processing steps.

4.4 Conclusions

In-line structures that are suitable for probing with needles directly on the Si were fabricated for measuring the sheet resistance of the *p*-type as-deposited PureB region without the need of post-processing metal contacts. The structures are straightforward to fabricate, and the accuracy was validated by measurement of the 700 ℃ PureB deposition. The sheet resistance of the *p*-type region created by a 400 ℃ PureB deposition was determined for the first time, and a detrimental influence of imperfect deposition window conditions and some post-processing steps could be clearly monitored.

With respect to both diode characteristics and the electrical interface conductance properties, the 400 ℃ PureB junctions behave like conventional p^+n junctions. All in all, the measurements support the picture that the vertical diode currents are determined by a p^+-region with the equivalent of about a monolayer of holes while the lateral conductance is determined by only a small percentage of these holes. The conductance is reproducible and stable

suggesting that the carriers with the highest mobility are screened from the interface by the holes held there by a fixed monolayer of electrons.

A well-defined reproducible high-ohmic sheet resistance is formed along the PureB-Si interface, which is attractive for several applications. For large photodiodes with PureB-only front-entrance windows this conductance helps keep the series-resistance low. Furthermore, for resistor applications the high sheet resistance and negative temperature coefficient are attractive for the fabrication of small dimension/capacitance high-ohmic resistors that could be added in the last stage of a CMOS process flow, also as a post-metal step.

Chapter 5

PureB Single-Photon Avalanche Diodes: Design and Fabrication

This chapter, work was performed to investigate the application of PureB photodiodes as avalanche devices. In particular, the aim was to create small devices suitable for operation in Geiger-mode, so-called single-photon avalanche diodes (SPADs). Besides small size, good reproducibility and uniformity over the wafer are the requirements that must be fulfilled to enable fabrication of reliable highly sensitive imaging arrays with micrometer-sized pixels. First an overview is given of the basic parameters that are important for Geiger-mode operation: dark-count rate (*DCR*), photon detection probability (*PDP*) and afterpulsing. The SPADs are operated above breakdown, which means that it is of critical importance to have good control of the breakdown voltage. This is first studied here on existing large-area PureB diodes with and without different types of guard rings. In general it is attractive to have a design where the breakdown point is moved away from the diode perimeter to the diode center. Achieving this together with the requirement of small device dimensions complicated the processing, in particular the opening of the light-entrance windows. These aspects will be discussed in this chapter.

5.1 SPAD Fundamentals

5.1.1 Geiger-mode operation

Single-photon avalanche diodes just like classical avalanche photodiodes as described in Chapter 1, are *p-n* junction devices. But unlike APDs, SPADs can be biased well above the breakdown voltage without avalanching and can then work in Geiger-mode. The device is very sensitive in this region and can respond to single photons.The basic operation circuit for operating the SPAD in Geiger-mode is shown in Fig. 5.1 for passive quenching and passive recharge

---

Part of this chapter have been published in *Proc. IWJT*, 70 (2013) [64] and *Proc. SBMicro*,1 (2014) [65].

via a ballast resistor R_Q chosen to be 100 kΩ in this case. The device is biased above breakdown (V_{BD}) by a voltage known as the excess bias (V_{EB}) so that the operating voltage is $|V_{OP}| = |V_{BD}| + V_{EB}$. With the resulting high electrical field, an avalanche event can be triggered by an incoming photon or an internal mechanism.

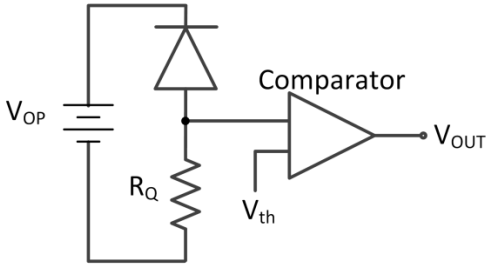


Fig. 5.1. Electronic circuit schematic of a SPAD with passive quenching and passive recharge.

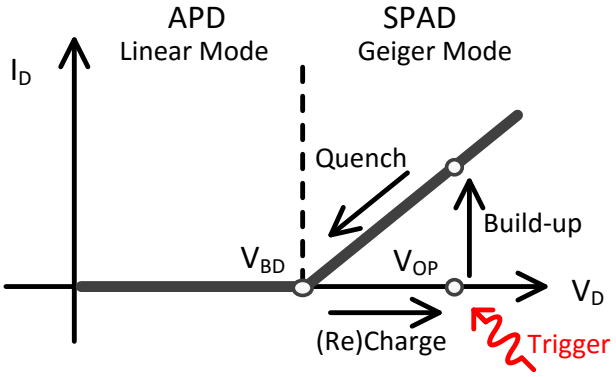


Fig. 5.2. Reverse *I-V* characteristics of APD operation and SPAD operation with working cycle in Geiger-mode.

When an operation voltage above the breakdown voltage is applied as shown in Fig. 5.2, within a very short time frame, the device will not reach the breakdown state, but it will be very sensitive and ready to respond to any trigger from either the outside or inside the photosensitive region. When exposed to a light signal, the incident photons can trigger an avalanche breakdown giving a high avalanche current that must pass through the quenching resistor R_Q, creating a voltage drop over the resistor and bringing the voltage across the diode below breakdown. Thus the avalanching is stopped, the diode biasing is restored to the initial values, where after a new incoming photon can be detected.

This cycle takes an average time known as the dead time. The avalanche pulses are sensed using a comparator with an appropriate threshold voltage V_{th}, thus converting the Geiger pulses into digital signals for photon counting. An oscilloscope image of Geiger pulses is shown in Fig. 5.3 where the output is connected to an oscilloscope.

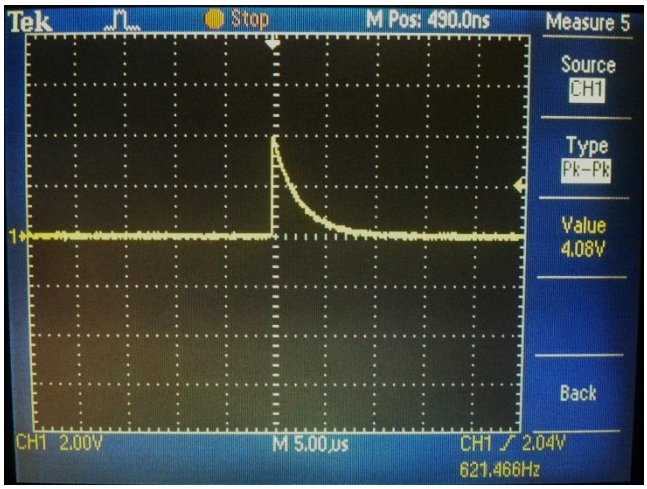


Fig. 5.3. An oscilloscope image of Geiger pulse.

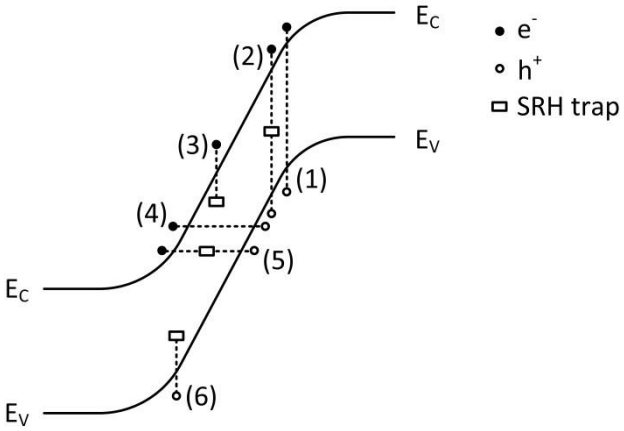


Fig. 5.4. Energy band diagram showing *DCR* generation mechanisms in a SPAD: (1) thermal-direct generation, (2) trap-assisted thermal generation, (3) trap-released electrons, (4) band-to-band tunneling, (5) trap-assisted band-to-band tunneling, and (6) trap-released holes.

5.1.2 Dark Count Rate (*DCR*)

In addition to photon-induced avalanching, avalanches can also be triggered by non-photon-induced carriers, such as those originating from diffusion from the neutral regions, Schottky-Read-Hall (SRH) thermal direct or trap-assisted generation, direct or trap-assisted band-to-band tunneling, or by the release of trapped carriers as shown in Fig. 5.4 [66]. All these mechanisms result in dark counts, characterized by a parameter called the dark count rate (*DCR*), which represents the number of avalanche events in darkness per unit time. The *DCR* will increase with the excess bias which will increase the avalanche probability.

5.1.3 Photon Detection Probability (*PDP*)

The Photon Detection Probability (*PDP*) is defined as the percentage of incoming (external) photons that trigger an avalanche pulse at the incident light wavelength λ:

$$PDP(\lambda) = \frac{A - DCR}{P} \tag{5.1}$$

where A is the avalanche pulse rate sensed by the SPAD in Hz and P is the incoming photon flux, given in Hz at wavelength λ, with which the active region of the SPAD is illuminated. The *PDP* increases as the excess bias increases [67, 68]. Thus the most fundamental trade-off in the operation of SPADs is between *DCR* and *PDP* because both of them will increase at a larger excess bias where the avalanche probability is increased whether an induced photon or dark carriers trigger the event.

A schematic of the *PDP* measurement setup is shown in Fig. 5.5. To get light with a specific wavelength, a wide spectrum light source generated by a halogen lamp is first filtered by a monochromator. Then the light goes through a color filter to remove any unanticipated spectral regions, and lastly the light is divided into two identical bundles, the one sent to the SPAD and the other to a reference diode. The avalanche pulse rate A is the SPAD count and the photon flux P is calculated by taking the current reading of the reference diode and, from a knowledge of all the areas involved, estimating the actual flux arriving on the active area of the SPAD. Due to some difference between the layout dimensions and the actual dimensions of the device there may be an error made when calculating the *PDP*. The P is controlled to prevent pile-up by adjusting the power of the halogen lamp.

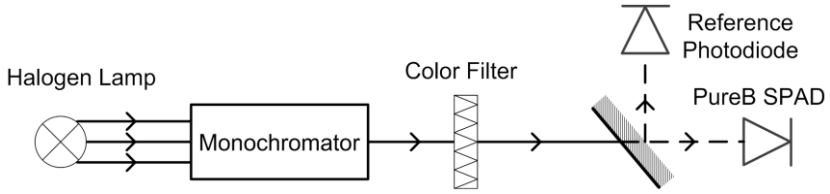


Fig. 5.5. Schematic configuration of *PDP* measurement [69].

5.1.4 Timing jitter

Timing jitter is the time-interval uncertainty from the arrival of the photon to the avalanche event. It describes the total uncertainty for a SPAD that is operated together with a time measurement device. Every photon-induced carrier must first travel to the high electric-field region of the depletion layer before triggering an avalanche and some carriers also first have to diffuse to the depletion region. Thus different delays in the avalanche process are introduced and there will not be an identical build-up for every injected carrier [70]. Timing jitter is important to time-correlated applications, such as TOF PET 3-D images.

In this thesis, jitter performance is measured with the SPAD exposed to a 40 MHz pulsed laser source at a wavelength of 405 nm, and the light is attenuated to the single-photon level by an NDF (neutral density filter) to prevent pile-up as described in [71]. Timing jitter is normally quantified by the Full-Width-Half-Maximum (FWHM) of the time distribution of counts taken from the moment of photon absorption to the triggered avalanche process.

5.1.5 Afterpulsing

During an avalanche process, the carriers released from deep-level traps can cause secondary avalanche processes known as afterpulsing [72]. Afterpulsing is a kind of noise. It can cuase overestimation of the *PDP* and *DCR* and therefore needs to be avoided. For a given SPAD, the probability of afterpulsing can be reduced by operating at lower excess bias, this lowers the electric field thus lowering the probability of carrier release from traps and defects. Using active quenching is also an efficient way of preventing afterpulsing.

When there is no light, dark counts behave like shot noise and the time interval between dark counts should follow Poisson statistics. However, due to the afterpulsing, the dark-count distribution will not exactly be a pure

exponential curve. Thus the afterpulsing probability places the overall counts above the fitted exponential line of the total counts [71].

5.1.6 Dead time

When an avalanche process is triggered, by an incident photon or a dark carrier, there will be a short time frame that the SPAD is unable to detect any signal. This time frame is dead time, which includes both quenching time and recharge time. The dead time can be measured together with the afterpulsing probability, as it is just the time interval where the most counts occur. Dead time limits the maximum count rate of a SPAD, i.e., the saturation count rate.

5.2 Device Fabrication

5.2.1 Fabrication flowchart

A schematic cross section of the process flow for fabricating PureB SPADs is shown in Fig. 5.6.

Starting with *p*-type (100) 2-5 Ωcm Si substrates, a 1.0-μm-thick n^- epitaxial layer is grown on an n^+ buried-layer, which is contacted by implanted n^+ plugs. An *n*-enrichment is created by implanting phosphorus through a 30-nm thermal silicon oxide, which defines the active region of the detector. A 300-nm LPCVD TEOS is then deposited and the implants are annealed at 950 ℃ for 20 min in argon gas. The anode contact windows are plasma-etched to the Si with soft landing and native oxide is removed by dip etching in HF 0.55% followed by Marangoni drying. The PureB layer is then deposited from diborane in an ASM Epsilon 2000 CVD reactor as described in Chapter 2. The deposition time and temperature, 6 min at 700 ℃, have been calibrated to give a 2.5 nm PureB deposition on bare Si wafers. Due to global and local loading effects it is expected that the PureB thickness in the anode windows can be about a nanometer thicker [28, 73]. A drive-in for 1 min at 850 ℃ is then performed to increase the doping of the Si and make the p^+-*n* junction more robust with respect to the processing of the light-entrance window that needed to be developed for these small micrometer-sized windows. Due to the reaction with the Si a small thinning of the PureB layer may occur in this thermal step but the overall results suggest the effect is insignificant for this thermal budget. Then the anodes and cathodes are contacted with either Al or Al with 1% Si and the interconnect is patterned. The light entrance windows are then opened, exposing

part of the PureB anode region. Lastly, a 400 ℃ alloy step in forming gas is performed to improve the contact resistivity of the Al to the PureB / Si surfaces and passivate the Si/SiO_2 interface.

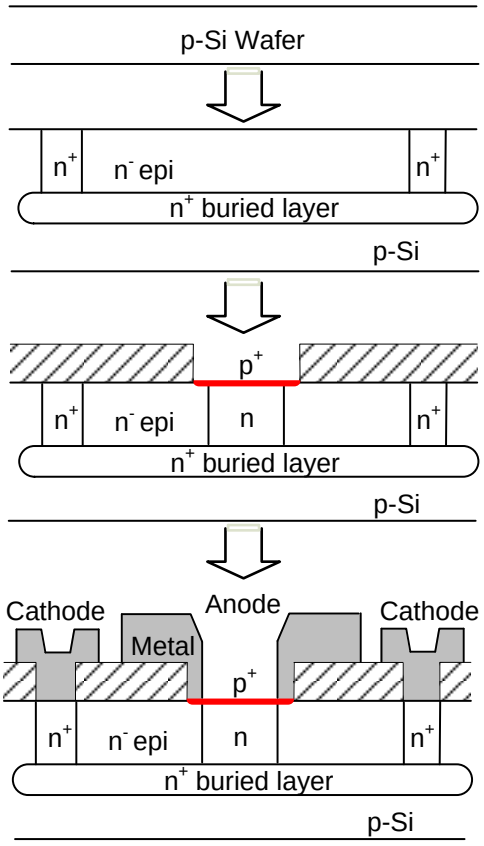


Fig. 5.6. Schematic process flow for the fabrication of a PureB SPAD.

5.2.2 Fabrication considerations

To arrive at a fabrication method that delivered high-quality, low noise level PureB SPADs, several aspects were investigated, such as the doping concentration of the *n*-type epi-layer, the geometry of the device and the implantation dose of the *n*-enrichment region. These will be discussed in the following.

A Guard rings

To prevent premature edge breakdown, a guard ring is generally implemented around the active area, which often is a circle of 5 to 50 µm in diameter as shown in Fig. 5.7a. The requirement of small micrometer-sized device dimensions complicates the processing of the guard rings since they readily will consume too much space. As a solution, an implicit guard ring is implemented by using an *n*-enhancement implantation in the central region of the diode as first described in [74]. This is illustrated in Fig. 5.7b: the breakdown point away from the perimeter and a large active region in the center of the diode is realized. The lack of a deep peripherally diffused *p*-type guard ring also required the development of more critical processing for contacting of the very thin p^+ anode and for removal of the anode metallization on the light-entrance window in a fill-factor effective manner.

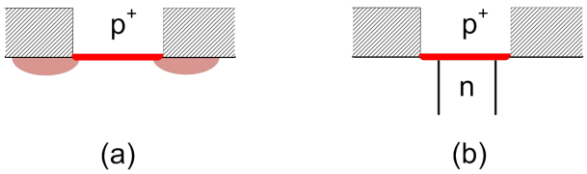


Fig. 5.7. Schematic of (a) a diffused guard ring and (b) an implicit guard ring with *n*-enrichment implantation.

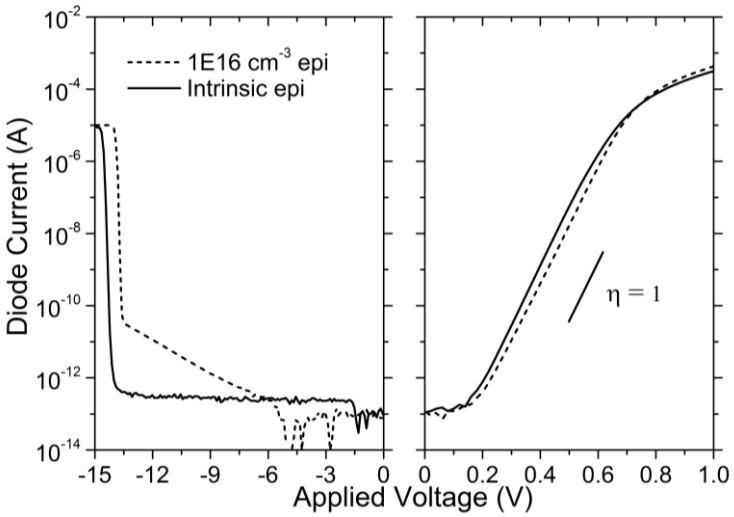


Fig. 5.8. *I-V* characteristics of two diodes with different epi-layer doping concentrations and an *n*-enrichment implantation of 5×10^{-12} cm^{-2} at 300 keV plus 10^{-12} cm^{-2} at 40 keV. The diameter of the diodes is 8 µm. The cutoff value of the reverse current is set to 10 µA to prevent the devices from becoming damaged. The thickness of both epi-layers is around 1.0 µm.

B Doping concentration of the epi-layer

Two types of n^- epitaxial layer are used in the fabricated SPADs. The one is *n*-doped to 10^{16} cm^{-3} and the other one is not intentionally doped, but in this case, due to phosphorus up-diffusion from the *n*-Si substrate and the background doping of the epi-reactor, the epi-layer will also be *n*-doped to an estimated concentration of around 10^{15} cm^{-3}. The influence of the epi-doping on the *I-V* characteristics of two devices with light *n*-enrichment implants is compared in Fig. 5.8. Both diodes have very good forward characteristics as well as reverse *I-V* characteristics that display abrupt breakdown. The forward current level of the *n*-enriched diode is lower which can be connected to the higher Gummel number, i.e., integral doping, of the *n*-substrate. For the diode with the intrinsic epi-layer, the reverse current is below the noise floor until the onset of avalanche breakdown, while for the diode with the 10^{16} cm^{-3} epi-layer, the reverse current becomes higher and increases with increasing bias voltage. With the higher electrical field at the perimeter in this case, trap-assisted tunneling at the oxide interface is more likely to occur and this leads to a steady increase of the leakage current. To minimize the peripheral electrical field, a low-doped epi-layer is preferable.

C Geometry of the device

For SPAD operation a phosphorus *n*-enrichment implantation is placed in a lightly-doped epi-layer. As indicated in Fig. 5.9, the anode p^+-region has a diameter *D1*, while the light entrance window, as well as the *n*-enrichment region, has a diameter *D2* at a distance *L* away from the edge of the anode. To evaluate the impact of the geometry on the effectiveness of the implicit guard ring, three devices with the same p^+-anode area are compared in Table 5.1 and the *I-V* characteristics are plotted in Fig. 5.10. The devices have the same *n*-enrichment implantation. All three devices show near-ideal forward characteristics with ideality factors η very close to 1 indicating that there are very few defects in the depletion region even though the PureB junction is created at only 700 ℃. Very sharp and abrupt breakdowns are observed and the breakdown voltages have a very small spread around -14 V. The dark current before breakdown is below the detection limit and it increases to hundreds of microamperes past breakdown. To maximize the fill factor, a small distance *L* is preferable.

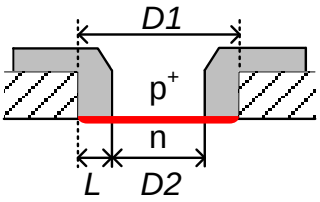


Fig. 5.9. Schematic of a diode with *n*-enrichment implantation and light entrance window.

Table 5.1. Geometry and measured parameters of devices with different *n*-enrichment areas but the same epi-layer and an *n*-enrichment P^+ implantation of 5×10^{-12} cm^{-2} at 300 keV plus 10^{-12} cm^{-2} at 40 keV.

Device	**D1 (µm)**	**L (µm)**	**D2 (µm)**	**η**	**V_{BD} (V)**
1	4	1.5	1	1.01	14.2
2	4	1.0	2	1.02	14.1
3	4	0.5	3	1.01	14.0

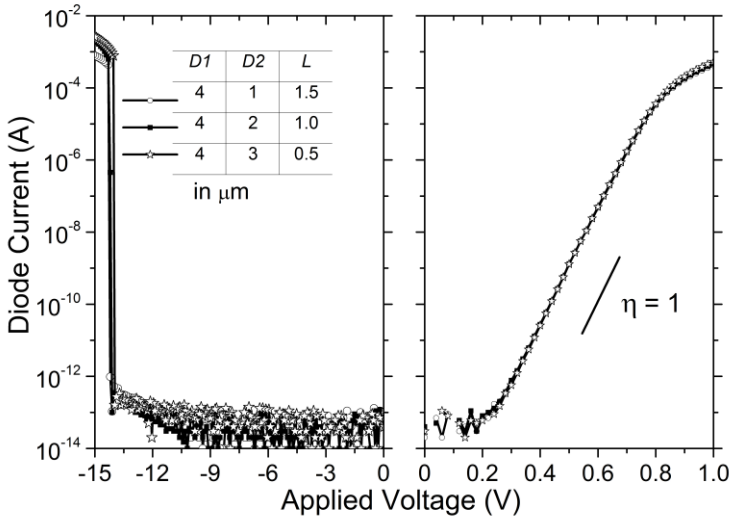


Fig. 5.10. *I-V* characteristics of the set of diodes with different *n*-enrichment implantation areas listed in Table 5.1. The diodes have an intrinsic epi-layer and a diameter of 4 µm, with an *n*-enrichment P^+ implantation of 5×10^{-12} cm^{-2} at 300 keV plus 10^{-12} cm^{-2} at 40 keV.

D Implantation dose of the n-enrichment region

Devices have been studied with four different *n*-enrichment regions created by phosphorus implantation of 5×10^{-12} cm^{-2} at 300 keV plus 10^{-12} to 8.5×10^{-12} cm^{-2} at 40 keV. From the process simulations shown in Fig. 5.11 we can see that the junction depth is as shallow as 12 nm for a 10^{-12} cm^{-2} implantation at 40 keV and it can be even shallower with higher implantation doses. All the devices show very sharp breakdown as seen in Fig. 5.12, but the transition from dark current below the measurement limit to breakdown becomes more gradual for devices with the heavier implantations. This is due to the fact that higher doping concentration gives a more narrow depletion region and thus higher electric field for the same bias, therefore inducing more band-to-band tunneling current and a smaller breakdown voltage.

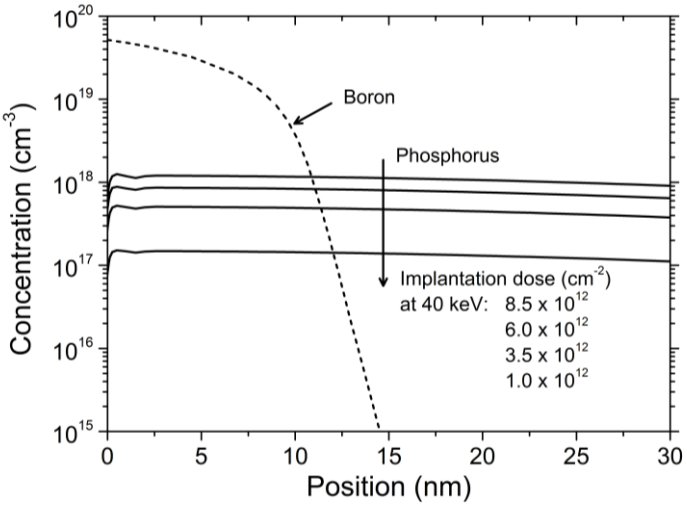


Fig. 5.11. Simulated doping profiles in the Si as a result of a 6-min PureB deposition at 700 ℃ and drive in for 1 min at 850 ℃ on an *n*-epi layer with doping 10^{15} cm^{-3}, and 4 different phosphorus implantations at 40 keV added to an implantation at 300 keV to a dose of 5×10^{-12} cm^{-2}. The boron is diffused from a constant surface concentration of 2×10^{-19} cm^{-3}.

The noise level of a SPAD can be characterized by a parameter called dark count rate (*DCR*), the pulses generated by non-photon-induced carriers, such as those originating from diffusion from the neutral regions, Schottky-Read-Hall (SRH) thermal direct or trap-assisted generation, direct or trap-assisted band-to-band tunneling, or by the release of trapped carriers. The *DCR* is measured at room temperature as a function of excess bias voltage V_{EB}. The measurement

results are plotted in Fig. 5.13 and listed in Table 5.2. The *DCR* can be as low as 5 Hz at room temperature with the low dose implantation. At the same excess bias, the *DCR* increases significantly with the doping concentration, this is also due to the band-to-band tunneling induced carriers. Thus, in order to make an effective guard ring as well as a low noise device the best trade-off is an implantation dose of 10^{-12} at 40 keV in this case.

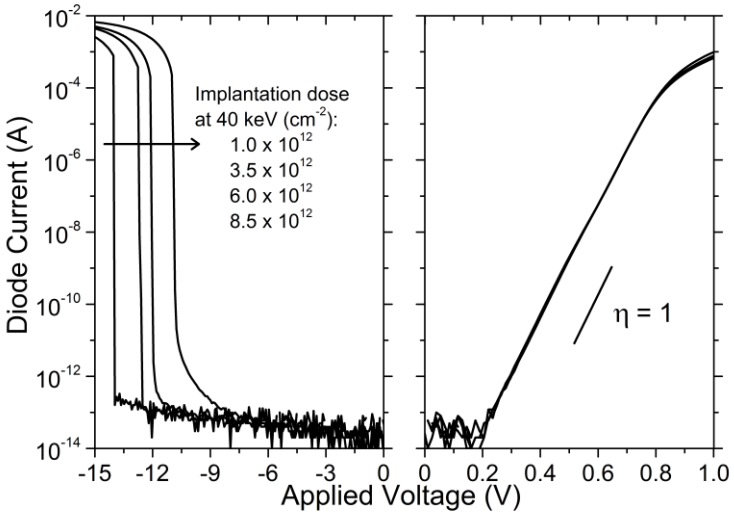


Fig. 5.12. *I-V* characteristics of a set of diodes with different *n*-enrichment implantations. The diodes are with intrinsic epi-layer, the diode diameter is 4 μm and that of the light-entrance window is 3μm.

Table 5.2. Measurement results of diodes with different phosphorus *n*-enrichment P^+ implants at 40 keV.

Dose (cm^{-2})	**Junction Depth (nm)**	**η**	**V_{BD} (V)**	***DCR* (Hz) at V_{EB} = 2 V**
1E12	12.1	1.01	-14.0	41
3.5E12	11.4	1.02	-12.5	2304
6E12	11.2	1.02	-11.8	35630
8.5E12	10.9	1.01	-10.9	198160

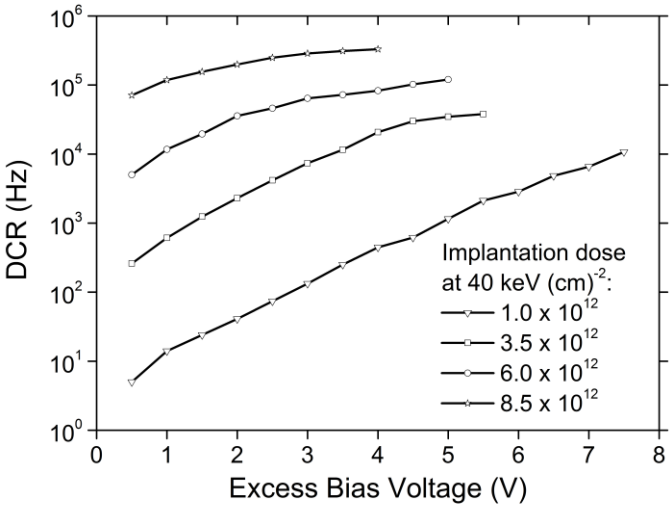


Fig. 5.13. *DCR* measurements of a set Φ4-µm PureB Si photodiodes with different *n*-enrichment implantations as a function of excess bias voltage at room temperature. The diameter of the light-entrance windows is 3 µm.

E Opening of light-entrance windows

For micrometer-small PureB diodes, the processing of a PureB-only light-entrance window becomes much more critical than for larger windows. Two possible process flows were tested as illustrated in Fig. 5.14. Right after the boron deposition, the following steps were performed:

- with process P-Al a 675-nm pure-Al layer is sputtered directly onto the PureB layer at 350 °C after which the cathode contact windows to Si are opened by plasma etching. Another 675-nm Al/Si(1%) layer is deposited at 50 °C. After metal patterning, the light-entrance windows are opened first by plasma etching until 100 nm – 200 nm Al is left which is removed by wet etching in HF 0.55% for 3 to 5 min.

- with process P-OX a 400-nm PECVD TEOS layer is deposited directly on the PureB layer at 350 °C. Both anode and cathode windows are opened by plasma etching with wet landing in HF 0.55% or Buffered HF (BHF, $HF:NH_4F=1:7$). A 1.4 µm Al/Si(1%) layer is deposited to make contact to the Si surface of the cathode and the PureB of the anode. The metal interconnect is then patterned. Finally the light-entrance windows are opened by plasma

etching to remove the Al/Si(1%) and wet etching in HF 0.55% or BHF (1:7) to remove the PECVD TEOS.

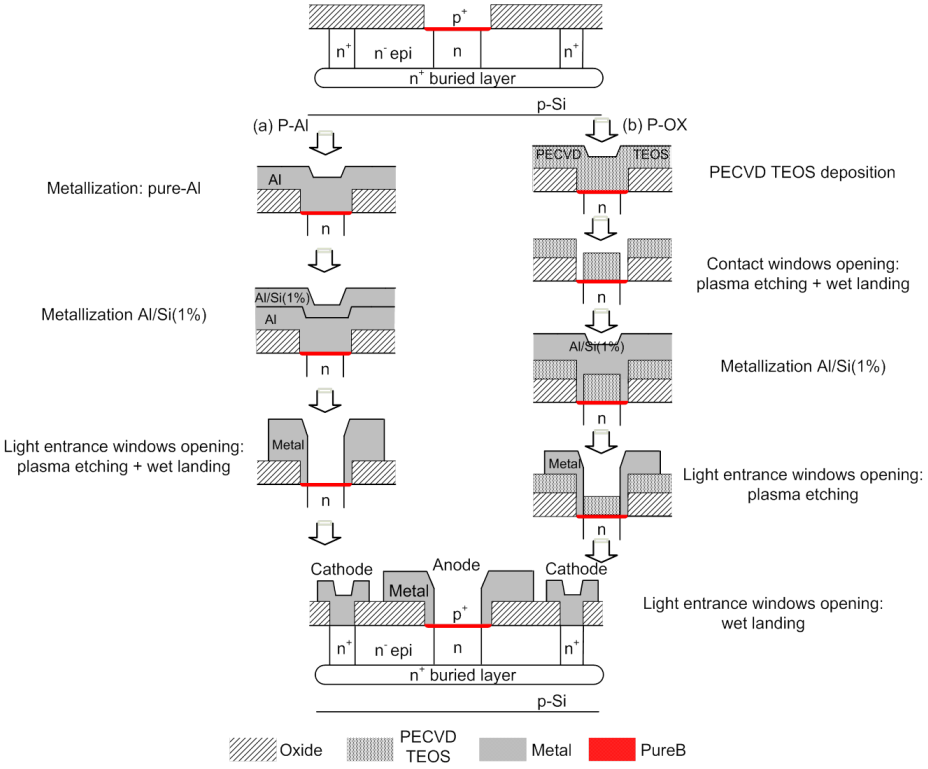


Fig. 5.14. Two schematic process flows for achieving a PureB SPAD with PureB-only light-entrance window; (a) P-Al and (b) P-OX.

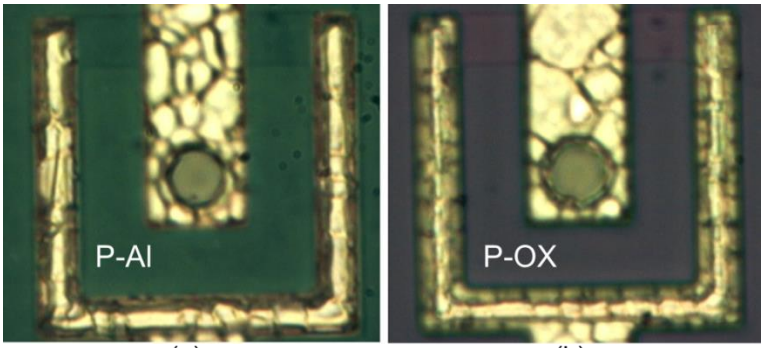


Fig. 5.15. Microscope images of diodes fabricated by the methods P-Al and P-OX. The diameter of the light-entrance windows is 4 µm.

Microscope images of light-entrance windows opened by the two processing methods are shown in Fig. 5.15. Visually there is no clear difference between the two windows.

The electrical *I-V* characteristics of the fabricated devices are measured from anode to cathode on a probe station. As shown in Fig. 5.16a, under forward bias, there is no clear difference between the diodes that both exhibit a near-ideal electrical behavior with ideality factors η very close to 1.0. In the small reverse bias regime, between 0 and -1 V, the reverse diode current remains small for both diodes. However, with increasing reverse bias voltage, the depletion region becomes wider and wider, and more crystal defects, impurities and (interface) traps, etc., may be encompassed and be a source of generation-recombination leakage current. As seen in Fig. 5.16b, the P-OX device displays a higher reverse diode current which increases at a higher rate just before breakdown, suggesting that defects created at the surface during window processing are then in the vicinity of the depletion region where they become active perhaps via a trap-assisted tunneling effect.

DCR measurements are also performed for the two devices. The oscilloscope images of the *DCR* results are shown in Fig. 5.17. The minimum *DCR* of the P-OX diode is high, up to 30 kHz, as shown in Fig. 5.17b while the *DCR* of the P-Al diode shown in Fig. 5.17a is only around 500 Hz at even higher excess bias.

A SPAD works above the breakdown voltage. As the reverse bias voltage is increased, the depletion region becomes wider by extending both into the the p^+-region at the surface and into the *n*-epi layer of the substrate. The only difference between the two types of diodes under investigation is the processing of the light-entrance window directly after boron deposition. The effect of this processing on the PureB layer itself was examined by using in-line ellipsometry to determine the thickness, a method that has acceptable accuracy and good repeatability for smooth layers [75]. Three quantities are compared: the mean square error (MSE) that gives a measure for how well the measured values fit the numerical model of the material, the thickness of the boron layer and the roughness of the PureB/Si interface. The ellipsometry results showed that for PureB layers processed on non-patterned Si wafers, the wafer-to-wafer spread of the average boron thickness is less than 3% and the on-wafer thickness spread is less than 4%, confirming that the PureB deposition-process itself has

good reproducibility. Some of the post-processing steps after PureB deposition were investigated:

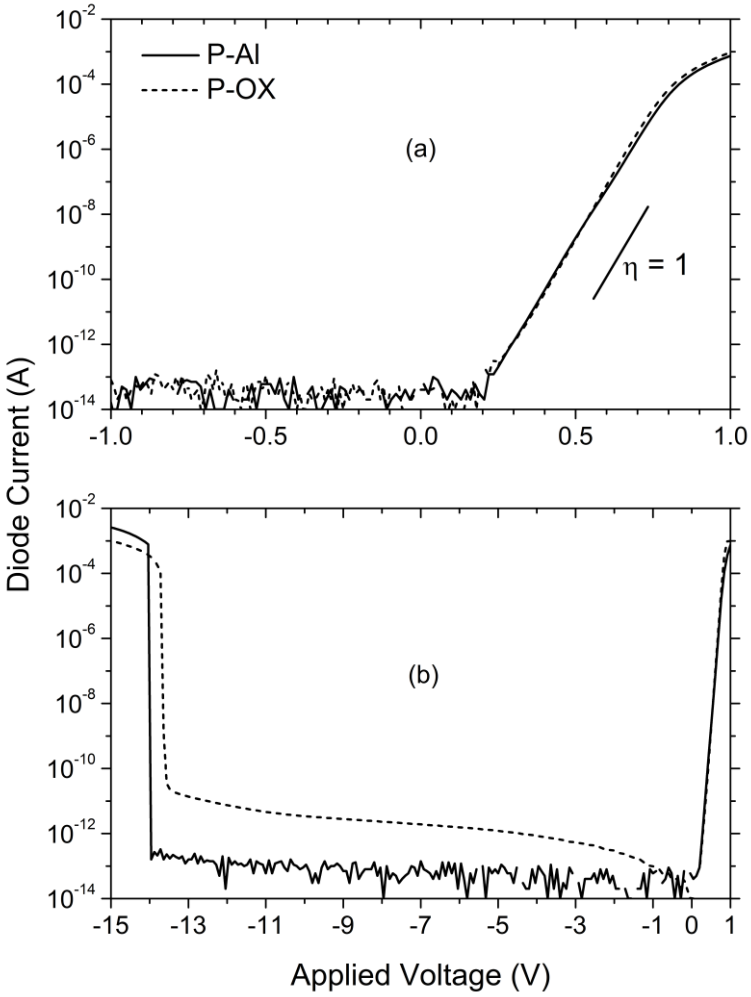
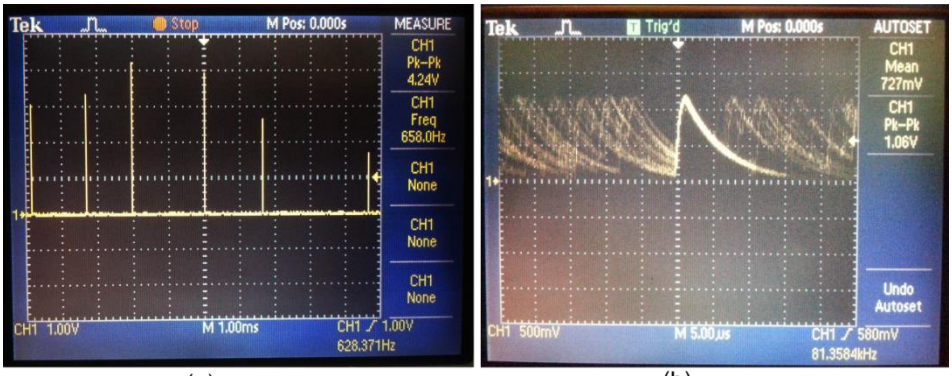


Fig. 5.16. *I-V* characteristics of diodes (a) in forward and a small reverse regime and (b) in a large reverse regime. The diameter of the diodes is 6 μm with an opening of 4 μm in diameter.



(a) (b)

Fig. 5.17. Oscilloscope image of (a) a P-Al diode on the scale 250 µs/div and a P-OX diode when V_{EB} is 4.5 V and (b) a P-OX diode with 25 µs/div when V_{EB} is 1.0 V. The sampling rate was sub-sampled in (a) in order to show more avalanche pulses, which is why the amplitude of the pulses is not always exactly V_{EB}.

Wet etching: HF 0.55% and BHF (1:7)

Light-entrance windows are opened with wet landing in HF 0.55% or BHF (1:7). To completely open the windows, an overetch is applied and the PureB layer is then directly in contact with the solutions. The effect of these etchants on a virgin PureB layer is tested by first putting as-deposited wafers in the solutions for 1 min. After rinsing and drying, the PureB-layer thickness is measured. This procedure is then repeated on the same wafers but with etching times of 5 min and 10 min. The measurement results are listed in Table 5.3.

Table 5.3. Ellipsometry measurement results after etching in HF. and BHF solutions

	Dip-etch time	MSE	Thickness (nm)	Roughness (nm)
HF 0.55%	0	6.01	2.42	0.70
	1 min	6.01	2.41	0.68
	1 min + 5 min	5.98	2.40	0.69
	1 min + 10 min	5.97	2.39	0.69
BHF 1:7	0	6.09	2.39	0.73
	1 min	5.96	2.38	0.73
	1 min+ 5 min	6.00	2.36	0.74
	1 min + 10 min	6.02	2.35	0.75

The measurement results indicate that any change to the PureB layer and the boron/Si interface is negligible. In general, however, it is not advisable to

use prolonged (B)HF etching, particularly with HF, since pinholes in the boron layer can become more pronounced and lead to local oxidation of the Si surface. This is detrimental for the photodiode robustness [38, 40].

Direct Al metallization sputtering process

Pure Al is sputtered onto the PureB layer at a high temperature (350 ºC) to be sure that closed grains are formed that are stable during the subsequent thermal steps. The 675-nm-thick Al layer is plasma etched to leave about 200 nm that is removed by wet etching in HF 0.55%. As seen in Table 5.4 the measured PureB thickness before and after Al removal suggests that there is no clear influence of the sputtering process in this respect.

Table 5.4. Ellipsometry measurement results after Al sputtering

	MSE	Thickness (nm)	Roughness (nm)
Before	6.18	2.41	0.78
After	6.06	2.39	0.73

Metallization through PECVD TEOS

A 400-nm-thick PECVD TEOS is deposited at 350 °C and removed with wet landing. In this case there is a clear change in the PureB layer thickness and roughness as seen in Table 5.5. During the PECVD process, TEOS is deposited in an oxygen plasma environment where finally the oxygen bombards the PureB layer and can possibly also oxidize the Si through pinholes. The exposure to the oxygen plasma appears to have 2 effects: first, the boron layer surface is slightly modified, supposedly by roughening and maybe also oxidation, which leads to a thinning of the layer as a result of HF dip-etching, and second, the increased leakage current and reduced breakdown voltage of the P-OX diode as seen in Fig. 5.16b suggests that the interface with Si is deteriorated. This could be the result of Si oxidation through pinholes. The thinning of the PureB layer and the increased roughness also give reason to believe that the density of pinholes will have increased. Si oxidation in pinholes is known to be a source of interface states and associated generation-recombination centers. These can contribute to increasing the *DCR* which is in fact seen for the P-OX diode in Fig. 5.17b. These effects can possibly be counteracted by applying a thicker PureB layer deposition.

The two device types are compared in terms of *I-V* characteristics and noise measurement. The influence of some post-processing steps during the light-entrance window opening to the as-deposited PureB layer thickness is also investigated and a summary is given in Fig. 5.18. The present and past results suggest that the oxidation of pinholes in the PureB layer will lead to interface states promoting generation-recombination events that increase both reverse leakage currents and *DCR*. For the same deposited PureB thickness, capping with a plasma oxide has more detrimental effects than a capping with sputtered Al layer. Thus, in the following experiments devices have been used that were fabricated with the P-Al processing flow to expose the PureB-only light-entrance window.

Table 5.5. Ellipsometry measurement results after PECVD processing

	MSE	Thickness(nm)	Roughness(nm)
Before	6.11	2.42	0.76
After	6.05	2.18	0.87
Change	1%	9.9%	14.5%

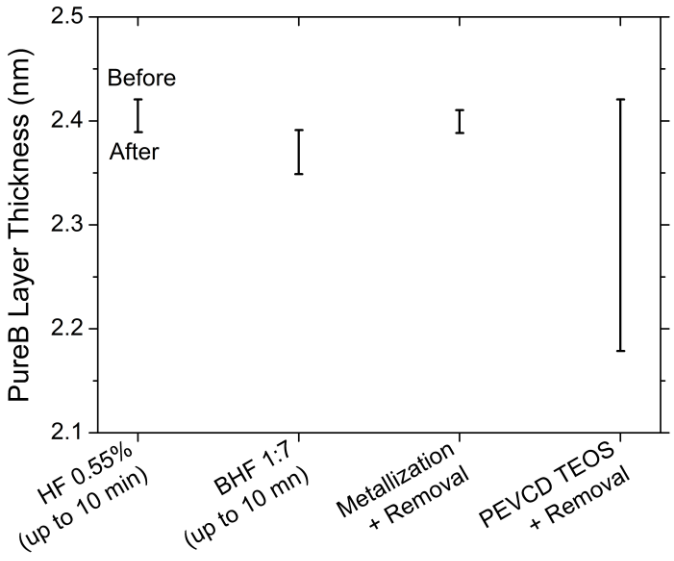


Fig. 5.18. The influence of some post processing steps on the thickness of the as-deposited PureB layer.

5.3 Conclusions

Micrometer-sized PureB diodes with electrical characteristics suitable for functioning as SPADs were successfully fabricated with windows covered only by PureB for the light detection. The diodes were evaluated with respect to the fabrication parameters defining the *n*-enrichment implantation and opening of the light-entrance windows. It was shown that a high-quality, low-noise-level device can be fabricated with an intrinsic epi-layer and *n*-enrichment region created by a phosphorus implantation of 5×10^{-12} cm^{-2} at 300 keV plus 10^{-12} cm^{-2} at 40 keV. The implicit guard consumes less space than the conventional diffused guard ring and good results were demonstrated when th *n*-enhancement region was placed as little as 0.5 µm within the diode area. For the processing of the light-entrance window, covering the PureB with a PECVD oxide layer was detrimental for the dark-count rate, probably due to oxidation to the Si interface through pin-holes in the PureB layer. The standard process of depositing and back-etching Al directly on the PureB gave the lowest DCR values.

Chapter 6

PureB Single-Photon Avalanche Diodes: Characterization

Based on the device design and fabrication considerations discussed in Chapter 5, the most promising device configuration was chosen for electrical and optical characterization in Geiger-mode operation. The breakdown behavior of the device was evaluated by simulation of the electric field distribution created by the *n*-enhancement implantation. Electrically, the dark-count rate, photon detection probability and afterpulsing were measured. The performance when a PureB SPAD responds to photons and low-energy electrons was characterized as well.

The device which is characterized in this section was created with an intrinsic epi-layer (around 10^{15} cm^{-3} actual doping concentration) grown on a bare 2-5 Ω-cm Si wafer. The *n*-enrichment region was created by a phosphorus implantation of 5×10^{-12} cm^{-2} at 300 keV plus 10^{-12} cm^{-2} at 40 keV to define the active region. The light-entrance windows were only 1 μm smaller in diameter than the PureB anode window, i.e. the edge to edge distance from the anode perimeter to light-entrance window / *n*-enrichment region was only 0.5 μm. The light entrance window was opened by Al plasma etching with a wet landing in HF 0.55% on the PureB.

6.1 Device validation

To validate the efficiency of the implicit guard ring, a device simulation in TCAD was performed. A 4-μm wide p^+-anode region is defined at the Si surface with a constant doping concentration of 10^{19} cm^{-3} and a junction depth of 12 nm. The bulk Si is *n*-type with a doping concentration of 10^{15} cm^{-3}. The *n*-enrichment region is right underneath the p^+ region but 1 μm smaller in width, and it is *n*-type with a constant doping concentration of 10^{17} cm^{-3}. The *n*-

---

Part of this chapter have been published in *IEEE Trans. Electron Devices,* **61**, 3768 (2014) [76] and *Opt. Lett.*, **40**, 300 (2015) [77]

enrichment region extends into the Si and is connected to the n^+ buried layer. The cathodes are also connected to the buried layer through an n^+ plug. As described in [78] for one-sided abrupt junctions with a background doping of 10^{17} cm^{-3}, the maximum electric field at breakdown in Si is approximately 5×10^5 V/cm. From the simulated electric-field-distribution graph in Fig. 6.1 we can see that the maximum electric field lies at the junction between the p^+ region and the *n*-enrichment region. In the implicit guard-ring region, the electric field is reduced to less than half of the maximum electric-field value, thus preventing premature edge breakdown. Due to the ultra-shallow nature of the junction, the electric field in the p^+ region is close to the maximum value and it stays quite high through the depletion region to fall off abruptly in the *n*-enrichment region beyond the depletion region as is illustrated by Fig. 6.2. Thus, the avalanche multiplication region reaches to the surface and overlaps the light-absorption region, which should make the sensitivity to (V)UV light and low-energy electrons optimal. A light-emission test is shown in Fig. 6.3 for a Φ4-μm PureB SPAD with a light-entrance window equal to 3 μm. The result confirms that the onset of the breakdown is within the *n*-enrichment region and not at the anode edge.

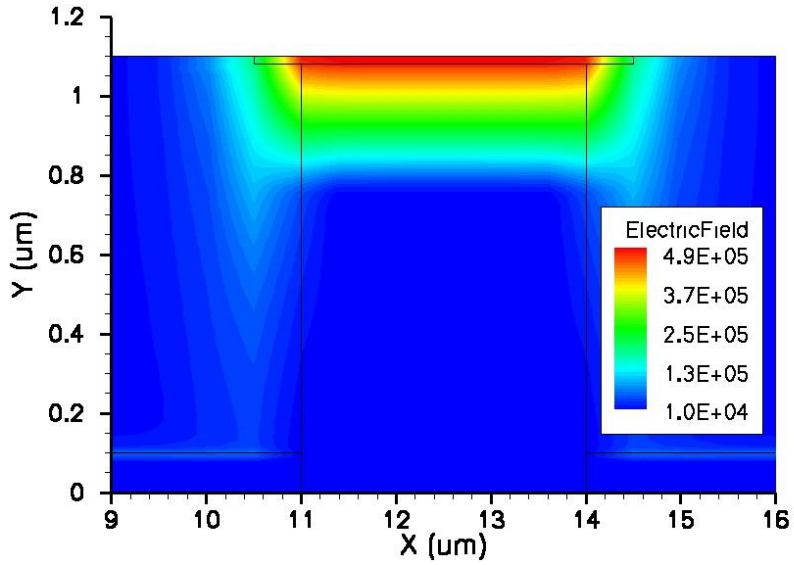


Fig. 6.1. Simulated electric-field distribution in Si when the maximum electric field reaches approximately 5×10^5 V/cm, i.e., the maximum electric field for a one-sided abrupt junction with a background doping of 1×10^{17} cm^{-3} in Si. The device is created by following the process flow of the fabricated devices [79].

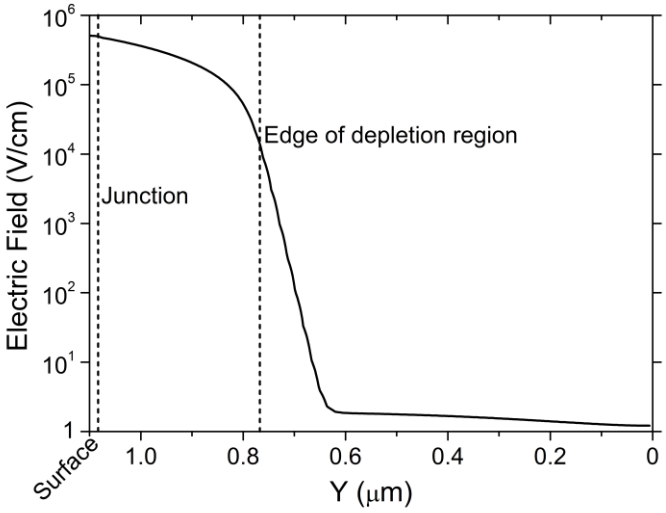


Fig. 6.2. Simulated electric-field profile in the Y (vertical) direction along the center of the device (X = 12.5 μm) where the maximum electric field reaches approximately 5×10^5 V/cm. Around X = 0 the electric field in the p^+-region should drop to zero but the simulation grid is too course to reproduce this.

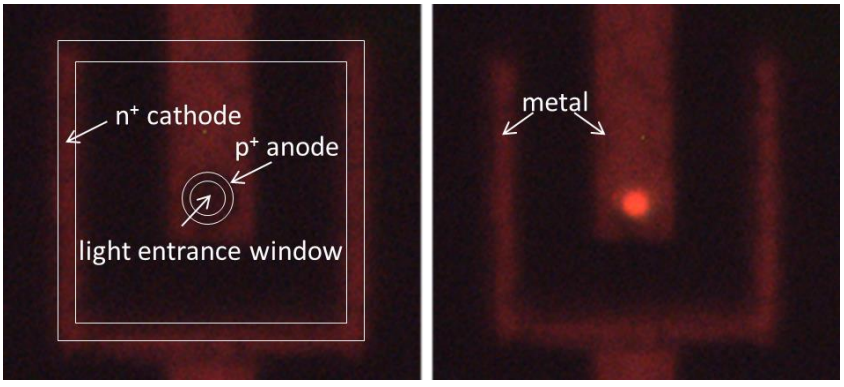


Fig. 6.3. Light-emission test for a Φ4-μm PureB SPAD operating at a reverse voltage of 14 V, the diameter of the light-entrance window is 3 μm.

6.2 Electrical and optical characterization

6.2.1 Dark Count Rate (DCR)

As seen from Fig. 5.13 in the previous chapter, for a Φ4-μm PureB SPAD,

the *DCR* values are extremely low, down to 5 Hz when V_{EB} = 0.5 V, i.e., the noise level at room temperature is very low and could be further reduced by cooling the device. The measured *DCR* as a function of temperature is shown in Fig. 6.4 for three different excess bias voltages. All curves show a good exponential relationship to the ambient temperature, suggesting that the *DCR* is dominated by the thermally generated carriers rather than field-assisted generation. The latter occurs without the help of a phonon and has, compared to the thermal generation, a relatively small impact [80] that is hardly reduced by lowering the temperature. This sets a limit to the reduction of the *DCR* that can be achieved by cooling the device [67].

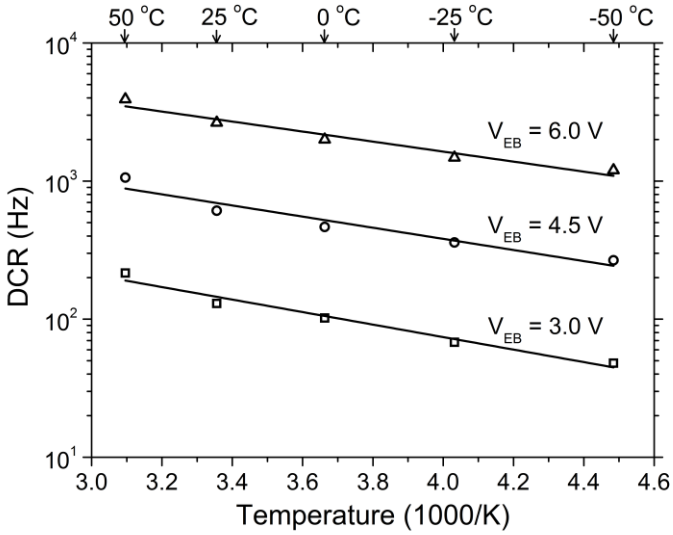


Fig. 6.4. Measured *DCR* (symbols) with exponential fit (lines) as a function of temperature for an excess bias of 3.0 V, 4.5 V or 6.0 V.

6.2.2 Spectral response

The spectral sensitivity for a Φ4-μm PureB SPAD is evaluated by illuminating the device at different wavelengths with a light-source spot that is much larger than the diode area. The measured photocurrent I_D is compared with the photocurrent I_{REF} measured on a reference photodiode with an area larger than the spot size and for which the quantum efficiency is known for all wavelengths of interest. The ratio I_D/I_{REF} is plotted as a function of wavelength in Fig. 6.5 for the operating voltages of -10 V (below breakdown), -14 V (breakdown) and -20 V (Geiger-mode). The sensitivity shows a peak at 330 nm

in Geiger-mode, where the optical gain is a 1000 times higher than when operating below breakdown and a 100 times higher than when operating right at the breakdown voltage.

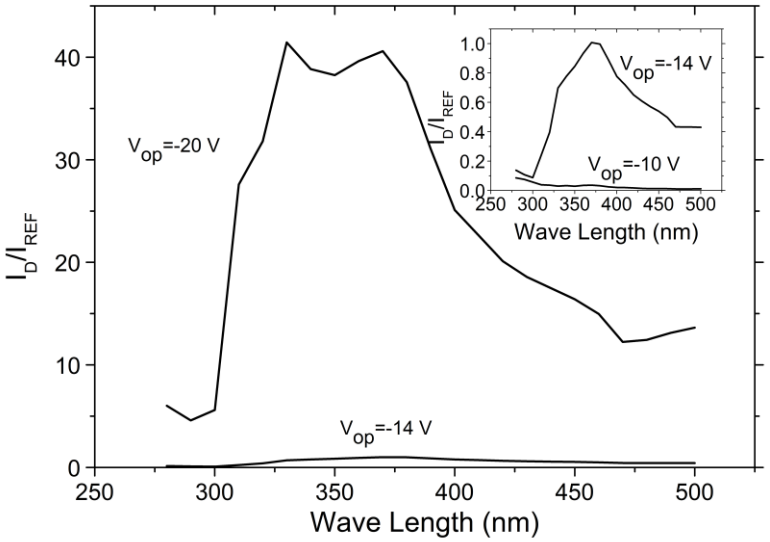


Fig. 6.5. I_D/I_{REF} of a PureB SPAD with a diameter of 4 µm in the UV spectrum for various operating voltages V_{OP}.

6.2.3 Photon Detection Probability (PDP)

The *PDP* for a Φ4-µm PureB SPAD at different excess bias voltages as a function of incident light wavelength is plotted in Fig. 6.6. It increases with increasing excess bias since more photons can be collected and counted at higher electric fields. The results display a good selectivity to UV light, with a maximum *PDP* of around 11% at 370 nm when the excess bias voltage is 6.0 V. For this device, the peak of the *PDP* is in the UV spectrum, unlike the SPADs normally produced in CMOS technology, for which the peak is in the visible light spectrum [81]. This is in accordance with the fact that the p^+-*n* junction here only has a junction depth of ~ 12 nm and although the PureB layer itself is absorbing, it is only about 2-3 nm thick. For UV light, the penetration depth in Si is less than 100 nm and the photon-generated carriers (electron-hole pairs) outside the depletion region can easily reach the multiplication region and cause an avalanche. However, for visible light, the penetration depth in Si increases with the wavelength and becomes hundreds of nm already at a wavelength of 500 nm. It is then more probable that the generated carriers will be swept into or

be isolated in the substrate, therefore recombining outside the multiplication region where no avalanche can be triggered.

Due to the limitations of the measurement setup, the *PDP* measurement could only be performed down to 360 nm. Nonetheless, from the high VUV responsivity of PureB photodiodes in general, the *PDP* at shorter wavelengths such as 330 nm is expected to be significantly higher than 11%.

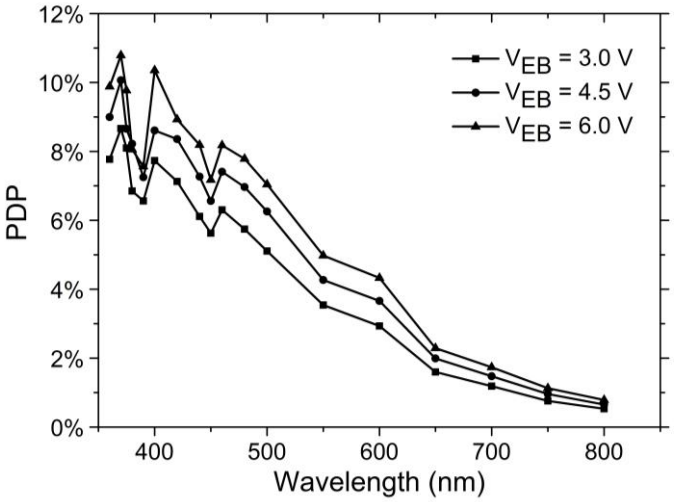


Fig. 6.6. Photon detection probability (*PDP*) for a PureB SPAD with diameter of 4 μm as a function of wavelength with excess bias V_{EB} = 3.0 V, 4.5 V or 6.0 V.

6.2.4 Timing jitter

As described in Section 5.4.2, the timing response for a Φ4-μm PureB SPAD is measured and plotted in Fig. 6.7 for an excess bias voltage of 4.5 V. The measurement is obtained using the embedded time discriminator of a LeCroy WaveMaster 8600A. The measured Full Width at Half Maximum (FWHM) jitter is 436 ps. The jitter performance shows a good Gaussian distribution with no diffusion tail, suggesting that most of the avalanching occurred within the multiplication region and secondary avalanche processes are essentially absent. The timing jitter can be further reduced by increasing the excess bias voltage as shown in Fig. 6.8. This results in higher electric field so that the avalanche process can be triggered faster.

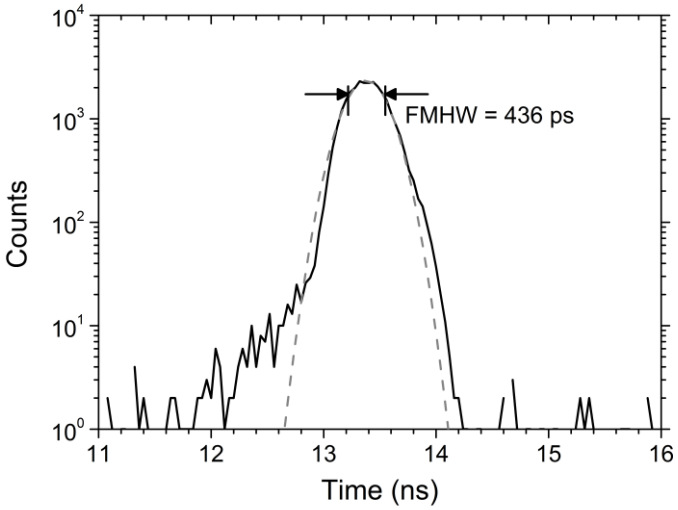


Fig. 6.7. Measured jitter performance (black solid line) and Gaussian fitting (gray dashed line) of a PureB SPAD with a diameter of 4 μm when operated in Geiger-mode with an excess bias V_{EB} = 4.5 V.

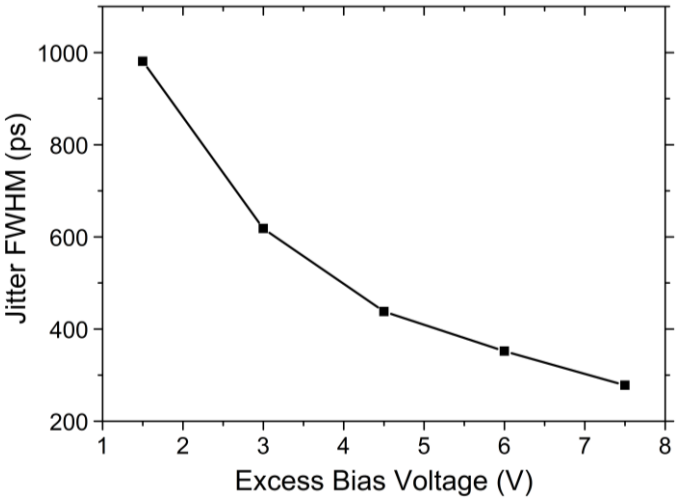


Fig. 6.8. Timing jitter (FWHM) of a PureB SPAD with a diameter of 4 μm when operated in Geiger-mode as a function of excess bias.

6.2.5 Afterpulsing and dead time

Following the procedure described in Section 5.4.3, the afterpulsing probability for a Φ4-μm PureB SPAD was measured at room temperature at three different excess bias voltages, namely 4.5 V, 6.0 V and 7.5 V. As seen in

Fig. 6.9, in all three cases, the afterpulsing distributions show very good exponential behavior and the afterpulsing probabilities are less than 1%, which is also an indication that the trap density in the device is very low and proof that a high-quality device has been achieved. The dead time, is around 6 μs as can be measured with high excess bias voltage above about 6 V or higher. Here we use passive quenching and recharge with an external circuit but if suitable active circuitry is employed, the dead time can be very significantly reduced.

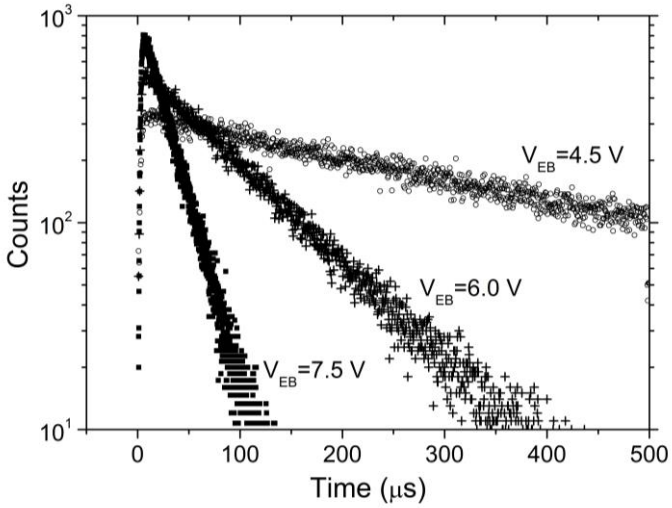


Fig. 6.9. Afterpulsing distributions of a PureB SPAD with a diameter of 4 μm when operated in Geiger-mode with excess bias V_{EB} of 4.5 V, 6.0 V and 7.5 V.

6.3 PureB SPAD response to low-energy electrons

In this section the PureB SPADs are characterized for exposure to low-energy electrons down to 200 eV that have a penetration depth of less than 5 nm in Si. Unlike illumination with UV light, a beam spot size well below a micrometer can be implemented. By scanning this over the detector surface the 2-D spatial uniformity of the anode dead layers and the avalanching mechanism that governs the response of the detector can be evaluated. The former is critical due to the nm-shallow penetration depth of the electrons and the latter, for CMOS-integrated visual SPAD imagers, is often found to be non-uniform due to variation in the breakdown voltage across the active area of the device [82]. This has been attributed to a non-uniform electric field distribution stemming

from the structural design of the device perimeter and metallization. This will often have a larger impact for radiation detected near the surface.

I-V characteristics are shown in Fig. 6.10 for the fabricated PureB SPAD with diameters of the anode and front-entrance window of 6 μm and 5 μm, respectively. The diode ideality factor is almost 1 and the dark current remains below a pA up until breakdown, indicating that there are very few defects in the depletion region over the junction created by the PureB deposition. A very sharp and abrupt breakdown increases the current to hundreds of microamperes and the breakdown voltage, V_{BD}, is found to be around -13.7 V. The *DCR* is measured here at room temperature as a function of excess bias voltage V_{EB} and plotted in Fig. 6.11. The values are extremely low, down to around 10 Hz when V_{EB} = 0.5 V, i.e., the noise level at room temperature is very low. All the measurements in this section are performed at room temperature.

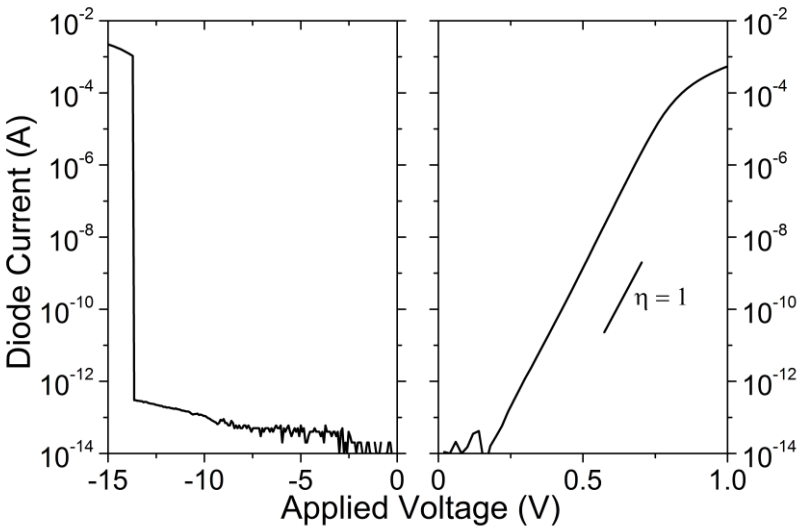


Fig. 6.10. *I-V* characteristics of a PureB SPAD with a diameter of 6 μm.

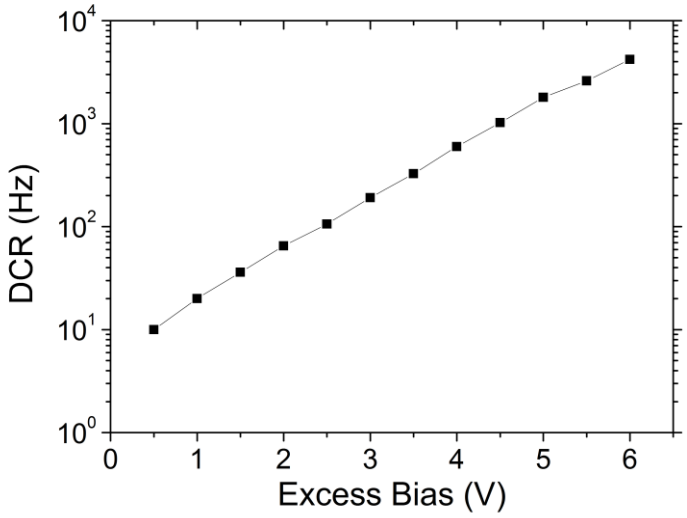


Fig. 6.11. Measurement of the dark count rate for PureB Si photodiode with a diameter of 6 μm as a function of excess bias voltage V_{EB} at room temperature.

To measure the response to low-energy electrons, the PureB SPADs to be tested are mounted in a DIL-24 package and placed in the SEM system right under the electron gun. The device is connected to the electrical measurement circuit outside the SEM system through wires as shown in Fig. 6.12 and the Geiger pulses are read with an oscilloscope. In Fig. 6.13a a SEM image, taken by the systems back-scatter electron (BSE) detector, is shown for a PureB SPAD with a diameter of 6 μm. An excess bias V_{EB} of 0.5 V is applied to the SPAD and it is exposed to electrons accelerated with a voltage of 350 V, scanned across the image field with a beam of less than 10 nm in size. The avalanche current pulses that are triggered can be imaged as shown in Fig. 6.13b. Each white dash in the picture represents an avalanche event that is either induced by an incident electron or by an intrinsic event that gives a dark count. The *DCR* is very low at this V_{EB} as is verified by the very low density of white dashes outside the anode area. Nearly all the avalanche events are located at the position of the front-entrance window, which again confirms that the lowest breakdown in the device is uniformly distributed across the *n*-enrichment region. Images of the corresponding Geiger pulses as measured by the oscilloscope are shown in Fig. 6.14b and Fig. 6.14a, with and without irradiation, respectively.

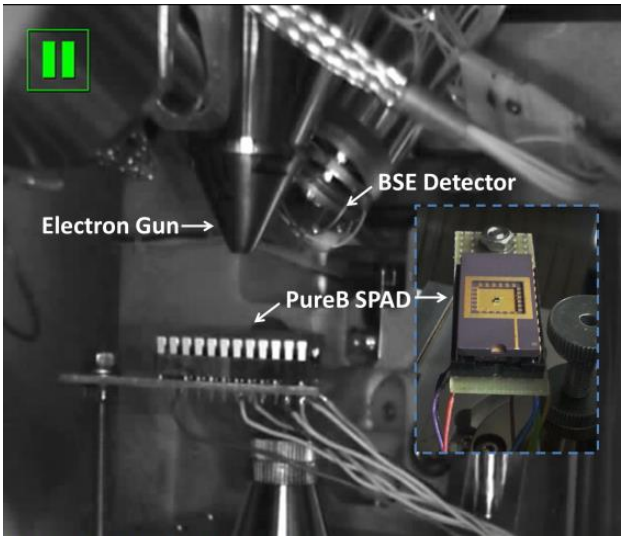


Fig. 6.12. Measurement setup for detecting low-energy electrons with a PureB SPAD chip mounted in a DIL-24 package, also shown in the inset from a top view.

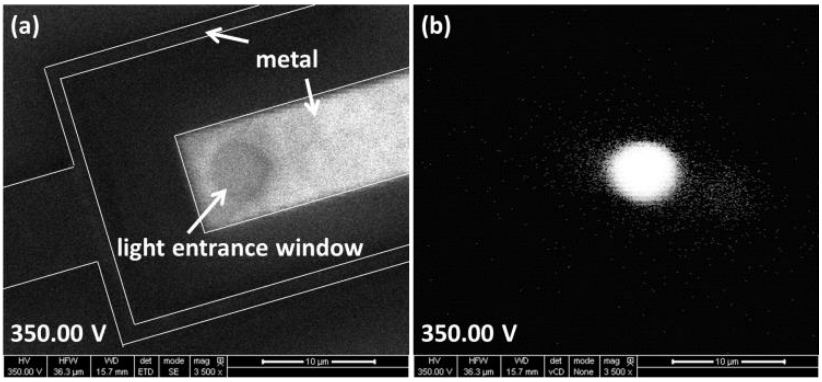


Fig. 6.13. (a) SEM image of a PureB SPAD with a diameter of 6 µm and (b) the corresponding image of current pulses from avalanche events when V_{EB} = 0.5 V and the electon accelerating voltage is 350 V.

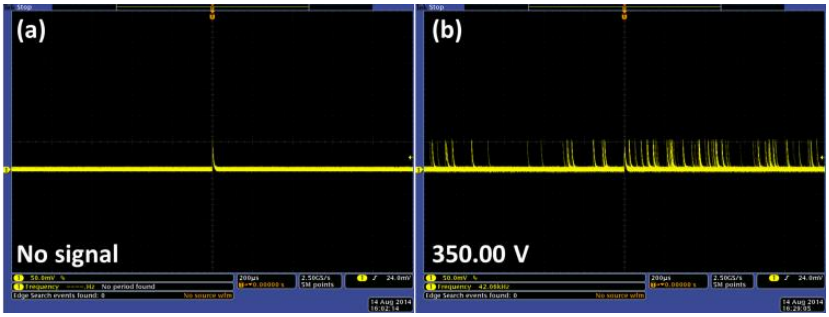


Fig. 6.14. Oscilloscope image of Geiger pulses at V_{EB} = 0.5 V (a) when there is no signal and (b) when responding to electrons with an accelerating voltage of 350 V.

A series of images were taken with a beam current of less than 1.3 pA. An image of the Geiger pulses registered at 200 V is shown in Fig. 6.15a, verifying the good sensitivity also at this voltage. The image in Fig. 6.15b is obtained by integrating the alvalanche current images of 16 scans. The SEM spot quality is often not perfect at such very low voltages and low currents. This is revealed by the extremely high sensitivity of the photodiode as a shadow of the main spot is seen mainly on its right side. In Fig. 6.16 images are also shown for the detection of electrons with accelerating voltages of 500 V and 2000 V. The density of avalanche-current dashes increases with the electron energy and for these energies integration of several scans is not necessary for obtaining a dense picture.

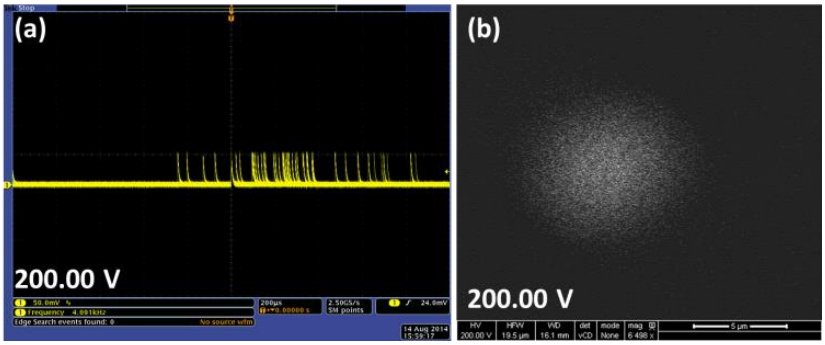


Fig. 6.15. (a) Oscilloscope image of Geiger pulses at V_{EB} = 0.5 V and (b) the corresponding image of the avalanche current of a PureB SPAD with a diameter of 6 µm when responding to electrons with an accelerating voltage of 200 V.

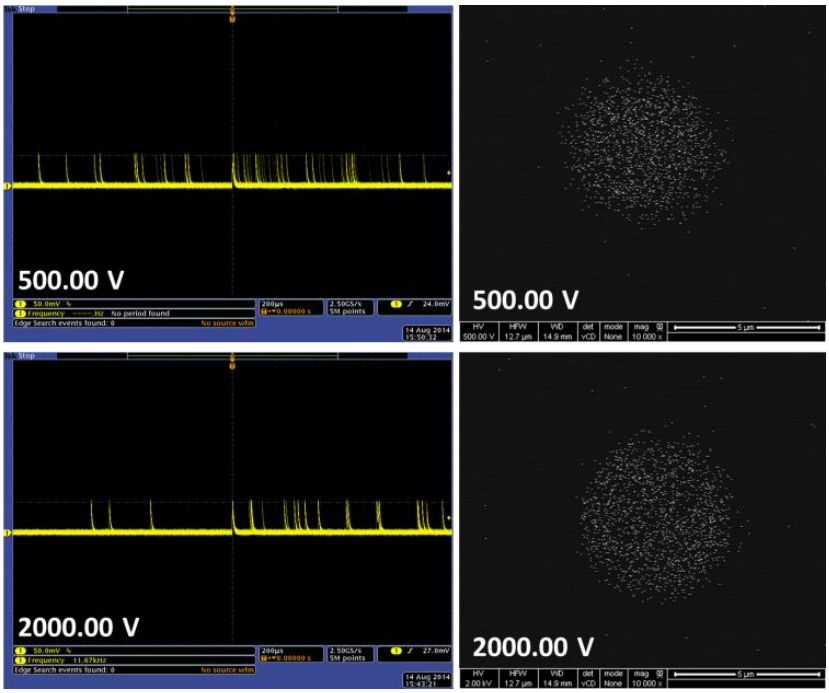


Fig. 6.16. Oscilloscope images of Geiger pulses at V_{EB} = 0.5 V and the corresponding images of the avalanche current of a PureB SPAD with a diameter of 6 µm when responding to electrons with an accelerating voltage of 500 V and 2000 V.

In all cases the scanned images display a good uniformity over the whole of the front-entrance window. At 200 eV the edge of the window has a slightly lower density of dashes but for this energy the focusing of the beam line is difficult to perfection. From previous studies of the PureB layer thickness across micrometer-sized windows it has been concluded that there is no thickening of the layer at the window edges because the mobility of the deposited B-atoms is very high before sticking, with centimeter long diffusion lengths on both the Si and the surrounding SiO_2 at a temperature of 700 ℃ [28]. In principle the perimeter of the *n*-enhancement layer could be a source of lower sensitivity but this is not evident from the uniformity seen for the 3 higher accelerating voltages of 350 eV, 500 eV and 2000 eV.

The interaction of one primary electron with the Si creates Auger electrons, secondary electrons and inelastically backscattered electrons, all of which can generate electron-hole pairs. For example, the signal gain for 500 eV electron exposure of PureB photodiodes operating in a low-voltage linear mode has

previously been found to be about 50 [38]. The passive quenching circuit used here is quite slow with at dead time of ~ 6 µs and the output is very readily flooded which can lead to overload that could damage the device. For this reason it was necessary to keep the V_{EB} low.

6.4 Conclusions

The PureB SPADs that were optically characterized in this chapter exhibit a very low frequency of dark counts at room temperature, more than 11% *PDP* in the UV region at 370 nm, and an afterpulsing probability less than 1%. The device performance can be further improved by increasing the excess bias voltage and in the studied range up to V_{EB} = 6 V there is no clear indication that the noise level in the form of timing jitter and afterpulsing performance, increases despite the increasing *DCR*.

This work is the first demonstration of low-energy electron detection with SPADs and it confirms that with Si PureB technology a high and uniform sensitivity across micrometer-sized front-entrance windows can be achieved in the energy range from 200 eV to 2000 eV. Limitations of the SEM system did not allow measurement at lower energy but it is expected that the SPADs will at least be sensitive down to 100 eV. With an active quenching circuit the excess bias could also be increased above what has been possible here, which would mean a significant increase in sensitivity. All in all, PureB SPADs appear to be very suitable for the integration of arrays for sensitive imaging with low-energy electrons and UV light.

Chapter 7

Photodiodes with PureGaB Technology

In this chapter investigations for the fabrication of photodiodes where a pure Ga deposition is applied to form the p^+-anode are presented. The motivation for examining this possibility was two-fold. For the first, just like boron and aluminum, gallium is a group III material that can be incorporated in Si as an acceptor impurity. However, Ga is not often applied as a dopant in Si because as such it has less attractive properties than B. This can be seen from Fig. 7.1 showing the solid solubility and diffusivity of B, Ga, and Al in Si. The Ga solid solubility in Si at temperatures above 900 ℃ is factors lower than for B and the diffusivity is higher, making it unattractive for ultrashallow junction formation using conventional high-temperature rapid thermal annealing. At 700 ℃ the solid solubility of Ga in Si of 8×10^{18} cm^{-3} [83] is lower than that of B. Moreover, the energy level of Ga as an impurity in Si is 0.072 eV as compared to 0.045 eV for B. Nevertheless, for deposition at 400 ℃, Ga has the attraction that the reaction temperature with Si is lower than Al and much lower than B. Moreover, the available Epsilon CVD system was especially equipped with trimethylgallium (TMGa), making it potentially possible to deposit nanometer thin layers of Ga with high accuracy. Therefore, in the search for methods of fabricating PureB-like (photo)diodes at post-metallization temperatures, replacing B deposition with Ga deposition was an obvious option.

A second reason for investigating Ga on Si deposition was that one of the limitations of the PureB layer as light-entrance window is the high resistivity. As found from the lateral sheet resistance measurements presented in Chapter 4, the sheet resistance for 400 ℃ PureB deposition on 2-5 ohm-cm wafers is a minimum of 33 kΩ/sq. If the PureB was replaced, albeit partially, by a metal with resistivity in the μΩ·cm range, even a 3 nm thick layer could possibly contribute to lowering the sheet resistance. Bulk Ga has a resistivity of 27 μΩ·cm, which is decades lower than the resistivity of boron of more than 500

Ω·cm. In reality, for such thin layers the sheet resistance will be negatively influenced by sidewall scattering and the actual conductivity cannot be directly predicted from the bulk values.

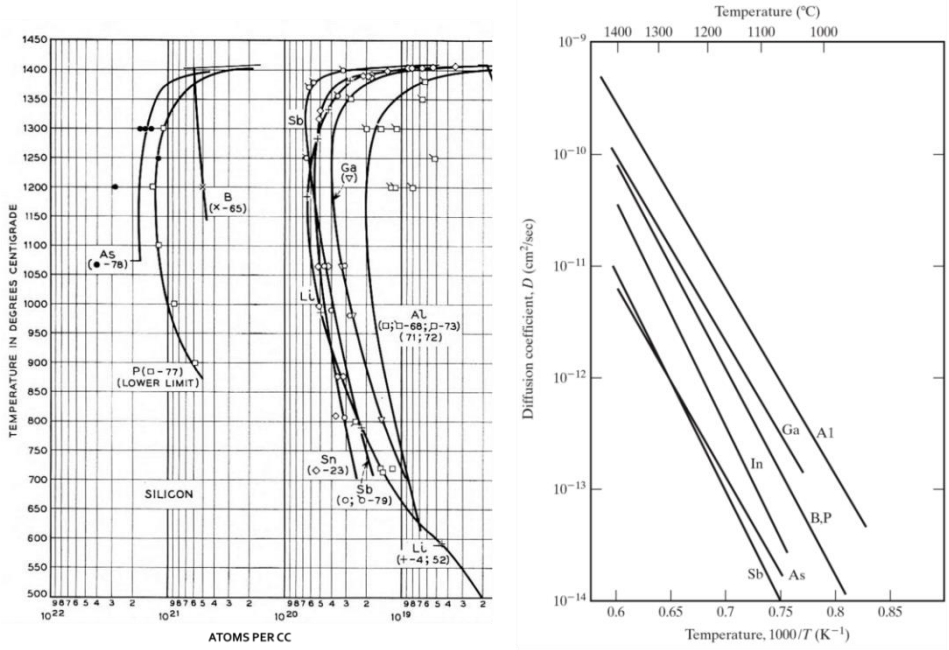


Fig. 7.1. Solid solubility (left) [83] and diffusivity (right) [84] of different elements in Si.

In the literature, the main interest in the deposition of Ga on Si comes from the compound semiconductor industry, particularly GaAs and more recently GaN have found industrial applications and this area of research is expanding rapidly. These Ga compounds have in the past been deposited by MBE [85] and MOCVD [86] systems, and today MOCVD is a widely used industrial solution. For Si/SiGe CVD systems like our ASM Epsilon 2000, equipping with metal-organic precursors is not standard, but by using low arsine-concentrations, processes for GaAs deposition have been developed that proved compatible with the standard Si/SiGe depositions [87]. When growing Ga-based compounds on Si, the properties of Ga have led to the development of process flows that avoid the deposition of Ga directly on the Si substrate. Moreover, apart from our work there are very few accounts of pure Ga deposition on Si with the purpose of creating a *p*-type region [55]. Nevertheless, from all reports it is clear that Ga can be difficult to work with. While B is a semi-metal with a

very high melt temperature of 2076 °C, Ga is a metal that melts already at 29.8 °C [88] and the eutectic temperature with Si is equally low [89]. Experiments with tens-of-nm-thick evaporated Ga layers show that it readily reacts with many materials such as Si and Al **[**90**]**. Upon sintering at temperatures as low as 350 °C, the Ga will, just like pure Al, alloy with the Si to form irregular spikes. For Al, a solution has been found to prevent spiking by depositing an alloy of Al and (1-2)%Si to pre-saturate the system with Si. Also due to the less controllable properties of Ga deposition on Si, for GaAs and GaN growth on Si by CVD the surface is first covered with another material before exposing the surface to the Ga precursor, even when the use of patterned wafers eliminates the need for buffer layers to absorb the stress from the lattice and thermal expansion coefficient mismatch **[**91**]**. For GaAs deposition in the Epsilon 2000 it was an advantage to start with exposure to AsH_3 to first built up a monolayer of arsenic [92]. For GaN, nitridation of the surface to form an nm-thin SiN layer is often reported [93, 94]. Nevertheless, due to the potential applications of these Ga-based materials, the last years have seen an increasing amount of research studying the formation of monolayers of Ga on Si by CVD [95, 96].

As part of this thesis work, both Al-contacted diodes and photodiodes with Al removed from the light-entrance window were fabricated with Ga deposition and characterized electrically and optically. In earlier work, reviewed in the following Section 7.1, deposition parameters were found for which pure Ga (PureGa) deposition delivered diodes with behavior similar to PureB diodes. In this chapter a more robust combination with also pure B deposition (PureGaB), originally developed for Ge-on-Si diodes, is shown to also have benefits for the fabrication of Si diodes. The PureGaB Si work was performed in parallel with the project to develop infrared PureGaB Ge-on-Si photodiodes. This Ge-on-Si work, shortly reviewed in Section 7.2, resulted in Ge diodes with exceptionally good *I-V* characteristics. The last sections present the new results on PureGaB Si diodes both with respect to the electrical and optical performance. In some aspects their performance is better than that of comparably processed PureB diodes.

7.1 PureGa Si diodes

For Ga deposition, TMGa is bubbled into the reactor and the following chemical reaction takes place:

$$2Ga\left(CH_3\right)_3 + 3H_2 \rightarrow 2Ga + 6CH_4 \tag{7.1}$$

In the first work on PureGa Si diodes reported in [55], Ga was deposited at reduced pressure using temperatures from 400 ℃ to 650 ℃. Through-wafer diodes were fabricated on *n*-substrates as shown in Fig. 7.2, but with B being replaced by Ga and no guard ring was included. In order to minimize the oxidation of the deposited Ga, wafers were taken immediately from the epi-reactor to the sputter coater for a 675 nm Al/Si(1%) deposition. The diodes were characterized without removal of the metal. The *I-V* characteristics are shown in Fig. 7.3a. The ideality factors of all the deposited diodes are very close to 1, indicating that good quality diodes have been fabricated. Compared to the Schottky diodes created when the Al/Si is deposited directly on the Si, the 500 ℃ and 400 ℃ Ga depositions significantly reduce the saturation current. The diodes were analyzed using lateral *pnp* structures and it was found that the 400 ℃ deposition delivered characteristics very similar to the p^+n diode behavior of PureB diodes, both with respect to the level of diode saturation current and the high level of injection of holes into the base of the *pnp*'s, as can be seen in Fig. 7.3b.

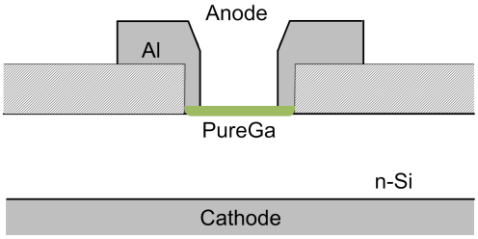


Fig. 7.2. Schematic cross-section of the fabricated PureGa diode.

A cross-sectional TEM analysis was made of the 400 ℃ deposition, as seen in Fig. 7.4. Directly after the Ga deposition, a 20-nm-thick layer of PVD α-Si was deposited at 50 ℃ to protect the thin Ga layer during preparation of the TEM sample. In this case, in view of the low melt-temperature of Ga, it cannot

be excluded that this extra deposition may have influenced the structure of the Ga layer. The alternative – not putting on any protective layer – would mean that the Ga would be exposed to air for several days before analysis. Since Ga_2O_3 is very readily formed in air, this option is also not ideal. The problematic concerning gallium oxide formation will be discussed further in connection with the PureGaB results presented in the following sections. In Fig. 7.4 only a very limited amount of deposited Ga is discernible. The interface is less distinct than for PureB deposition at 400 ℃ and the Ga atoms are not easy to identify, but it is clear that the affected region above the Si is about 1 nm thick.

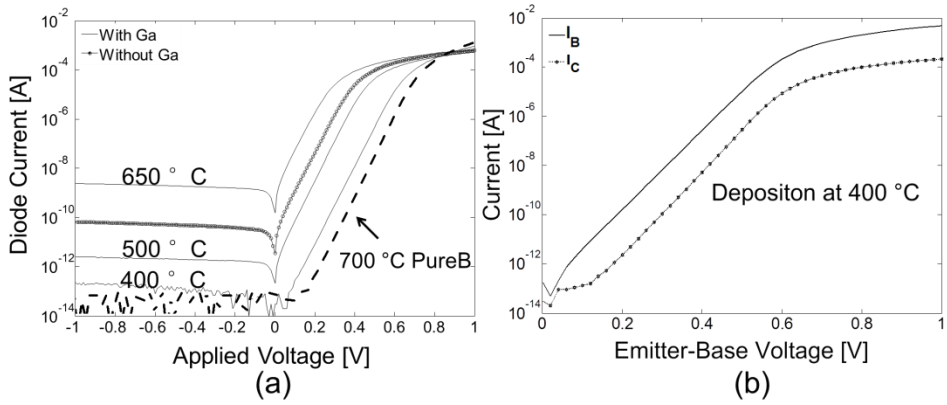


Fig. 7.3. (a) *I-V* characteristics of the diodes formed with and without first depositing Ga for various deposition temperatures and (b) Gummel plots measured on lateral *pnp* transistors with PureGa deposition at 400 ℃. The diode area is 40×1 μm^2 [55]. For comparison the *I-V* characteristics of a 700 ℃ PureB diode (dashed line) is added in (a).

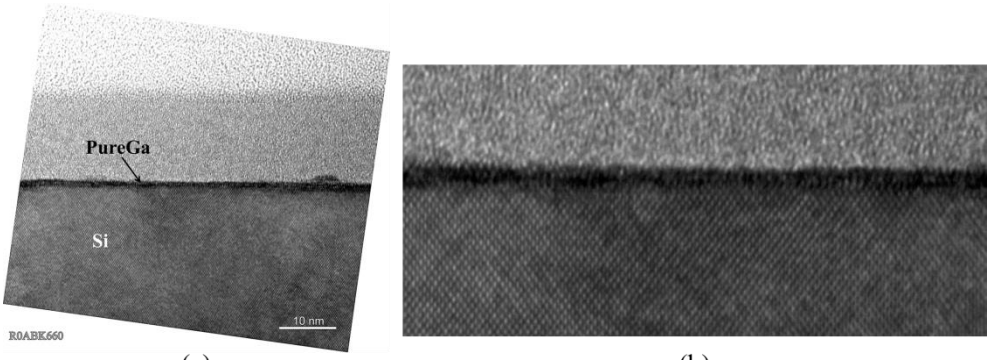


Fig. 7.4. (a) Cross-sectional TEM image of 400 ℃ deposited PureGa on Si [92]. Directly after deposition, the Ga layer is covered with 20-nm PVD α-Si deposited at 50 ℃ to facilitate the analysis and (b) close-up of the Ga-to-Si interface.

7.2 PureGaB Ge-on-Si diodes

The PureGaB technology was first developed for fabricating the Ge-on-Si diodes presented in [97]. Presumably due to the low boron solid solubility in Ge, PureB deposition did not provide an effective p^+ doping as observed on Si. In contrast, Ga has a high solid solubility in Ge of about 4×10^{20} cm^{-3} [83]. With this material a p^+n diode was achieved on the Ge by first depositing a layer of PureGa and covering with a layer of PureB to both prevent oxidation of the Ga and to create a barrier to the Al metallization. In principle the Al could then be removed to open a PureGaB-only light entrance window just like for the PureB Si photodiodes.

An example of the excellent *I-V* characteristics achieved with PureGaB Ge-on-Si diodes is given in Fig. 7.5. As a noteworthy point, not only dark currents as low as 35 μA/cm^2 were measured but also the spread over the wafer was very low. This good behavior is ascribed not only to the quality of the Ge-on-Si islands but for a great part to the damage-free processing of the PureGaB p^+-anode regions. In TEM images of the devices, an example of which are shown in Fig. 7.6, like for PureGa on Si, there is no clear layer discernible that can be attributed to the Ga deposition. In the EDS spectrum taken on the PureGaB and also shown in the figure, a very high peak of B is seen while the Ga peak is

almost lost in the background spectrum. All in all, it seems reasonable to assume that the Ga functions more like a wetting layer at the deposition temperature of 400 ℃. In the case of B on Si, temperatures above about 750 ℃ also do not lead to the building of a distinct layer. On one hand the reaction with Si, including diffusion into the substrate, starts to play an important role, and on the other hand, desorption from the surface starts to dominate [98, 99].

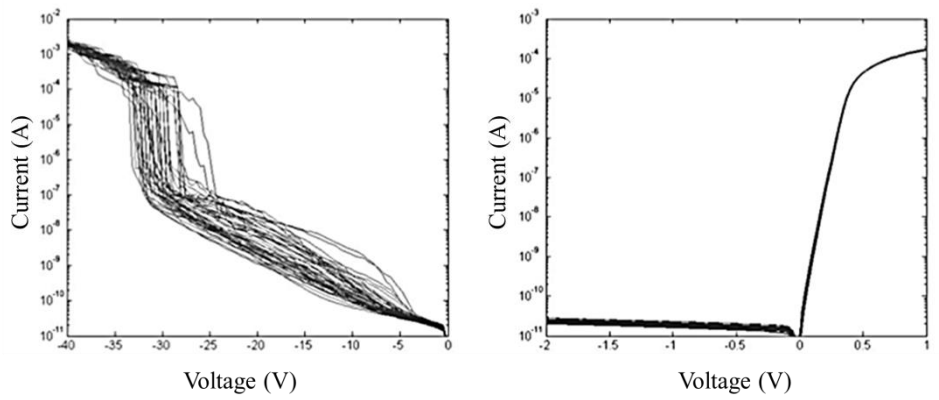


Fig. 7.5. The *I-V* characteristics of PureGaB Ge-on-Si diodes, each with an area of 400 μm^2 for 50 devices measured on one die [100].

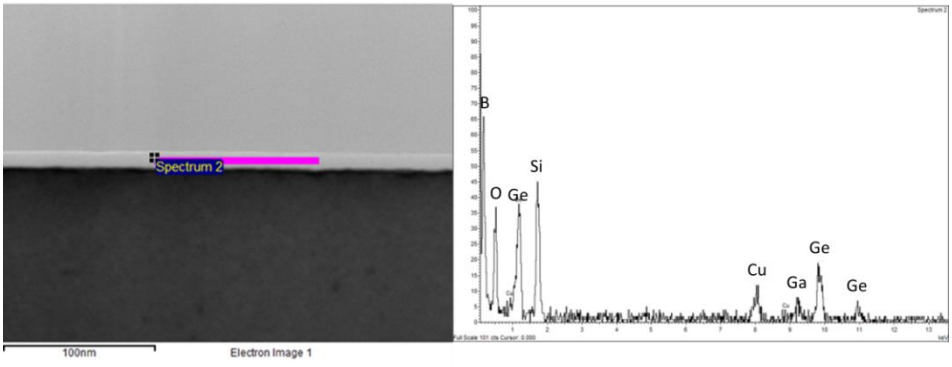


Fig. 7.6. Cross-section TEM image of PureGaB on Ge covered with PECVD SiO_2 and the EDS spectra on PureGaB.

7.3 PureGaB Si Diodes

For the fabrication of PureGaB Si diodes, Ga was first deposited on the Si surface at a temperature of 400 ℃ which, as discussed on Section 7.2, was shown in the PureGa devices to deliver a PureB-like saturation current. In nearly all experiments, unless otherwise specified, a pressure of 20 Torr and a deposition time of 20 min were applied. The Ga was then covered with B in a variety of ways: the B deposition temperature ranged from 400 ℃ to 700 ℃ and the deposition time was varied. The diodes were processed as described in Section 2.1, only with the Ga deposition as an addition. A schematic cross-section of the resulting PureGaB diode is shown in Fig. 7.7. The anodes and cathodes were contacted with Al and PureGaB-only light-entrance windows were in some cases opened by plasma etching with wet landing in HF 0.55%. The final step was the standard 400 ℃ alloying. In the following sub-sections the PureGaB diodes are electrically and optically characterized, and compared to their PureB and PureGa counterparts.

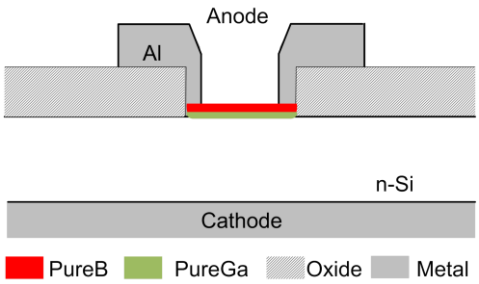


Fig. 7.7. Schematic cross-section of a fabricated PureGaB diode.

7.3.1 Sheet resistance measurements

The sheet resistance of as-deposited PureGa and PureGaB was studied by using the test structures described in Chapter 4. For the standard 20 min deposition of PureGa at 400 ℃, there was no contact between the p^+ rings of the test structures so no sheet resistance value could be extracted. In contrast to this, the PureGa diode characteristics clearly showed that an effective p^+ layer was formed similar to the PureB case. Two differences in the treatment of the Ga layer can be the origin of this seemingly inconsistency between the lateral and vertical current flows. For the first, in the diode structure all the Ga is

contacted by an Al-metallization layer so even if the layer is not uniform but made of disconnected islands, all parts will still operate as one large diode. Second, the Al is deposited directly after the Ga deposition so the time interval of exposure to air is very short whereas for the sheet resistance structures the PureGa layer becomes permanently exposed. Therefore, oxidation of the Ga is more likely to occur in the latter case. In view of the very limited Ga thickness, at most a few atom layers, it is easy to imagine that oxidation could result in non-active regions that laterally disconnect the active regions.

Although partial oxidation of the Ga gives a plausible explanation for the lack of conductivity along the Ga-to-Si interface formed in the sheet resistance structures, it also raises a number of unanswered questions about the formation and properties of the gallium oxide that may have been formed. In its crystalline form, Ga_2O_3 is a semiconductor that has interesting photodiode properties in itself. In research, β-Ga_2O_3 is well known as a transparent semiconductor compound with a band gap of ~4.9 eV, which is particularly suitable for solar-blind photodetection [101, 102]. It is recognized as a promising candidate for deep-ultraviolet transparent conductive oxides for solar-blind detection in the wavelength of 200 – 280 nm. It is unlikely that functional β-Ga_2O_3 would be formed by oxidizing the very thin PureGa layer. The lack of measurable sheet resistance indicates that if the Ga layer is modified by the exposure to air, then the new layer is at least not conductive.

With the PureGaB deposition, where the Ga layer was protected by a layer of boron, a well-defined conductivity was measured along the interface with the Si. Two situations were examined for the PureB component of all the devices, one with PureB deposited at the standard temperature of 700 ℃ for 6 min and the other at 400 ℃ for 20 min, the PureGa component is made with a deposition at 400 ℃ for 20 min. The resulting sheet resistance measurements are shown in Fig. 7.8 where a comparison is made to PureB layers made with the same deposition time but with the Ga deposition omitted. Taking the spread into account, the values are very similar for the same PureB deposition conditions. In Section 4.3 it was concluded that imperfections of the B-to-Si interface would cause an increase in the sheet resistance for the 400 ℃ deposition where the lateral resistance is directly related to the interface. This means that the lowest measured sheet resistance may result from the most ideal interface conditions. For the 400 ℃ deposition the lowest PureB sheet resistance is

around 33 kΩ/sq and for PureGaB it is around 35 kΩ/sq. This difference is so low that it could be explained by variations in the substrate doping, the effects of which are clear from Figs. 4.9 and 4.13 that relate the sheet resistance to respectively substrate biasing and doping. Even the higher spread of the PureGaB sample could be due to fluctuations in substrate doping. Unfortunately, due to the lack of metallization on the pads of the sheet resistance test structures it has not been possible to perform reliable *C-V* measurements to obtain the distribution of doping concentration across the substrates. For the 700 ℃ devices, the slightly lower sheet resistance and slightly higher spread of the PureGaB sample can also easily be due to fluctuations in the substrate doping that influences the mobility of the holes. All in all, with respect to the lateral sheet resistance measurements, the PureB and PureGaB samples appear to have quite comparable behavior, independent of the deposition temperature of the PureB. This suggests that the PureGaB layer provides a good coverage of the Si surface.

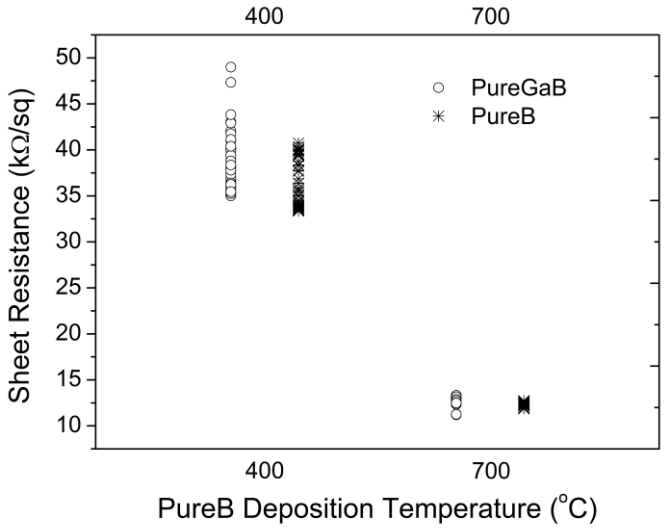


Fig. 7.8. Over the wafer measured sheet resistance of PureGaB and PureB layers with PureB depositions at 400 ℃ or 700 ℃. For all the devices, PureB is deposited for 20 min.

7.3.2 Diode *I-V* characteristics

Diodes were fabricated with and without Ga deposition and the PureB layer deposited at either 400 ℃ or 700 ℃. The diode *I-V* characteristics were measured at room temperature on both cm-large and µm-small diodes. In Fig. 7.9 the *I-V* characteristics of PureGaB diodes are compared to the PureB counterparts for the case where the PureB deposition was 6 min at 700 ℃. The large 1×1 cm^2 devices were processed with p^+ guard rings and the light-entrance windows were opened to the Pure(Ga)B layer. For the diodes with µm-sized dimensions, there were no guard rings and the diode surface remained covered with Al. As seen from the graph, for the PureGaB and PureB diodes with the same dimensions, the electrical performance is very similar. All of them exhibit very good *I-V* characteristics, the ideality factors are close to 1 and the dark currents are very low. This is another indication that an effective p^+-layer is formed also for the PureGaB samples.

In contrast to the 700 ℃ results, for the diodes where the PureB deposition was performed at 400 ℃ for 20 min, the electrical performance of the smaller diodes showed a large discrepancy between the PureGaB and PureB devices as seen in Fig. 7.10. Although the ideality factor remains close to 1, the current level of the PureB diode under both forward and reverse biasing is about 3 decades higher than the PureGaB diode. This difference, which is not seen for the larger diodes where the Al is removed, can be attributed to final processing with Al directly on the PureB. Compared to the 700 ℃ PureB layer, the 400 ℃ deposition results in layers with a very high surface roughness, the thickness of which is difficult to determine accurately from ellipsometry measurements. All indications are that these layers contain more pinholes than the 700 ℃ layers [30]. For both 700 ℃ and 400 ℃ layers it has in the past [56] been shown that Al can reach the Si and react with it when exposed to the alloying temperature of 400 ℃. Very small area Al-to-Si Schottky diodes can then be formed. As also shown in Fig. 7.6 these Schottky diodes have decades higher saturation current and even a small percentage of such regions can significantly increase the overall current levels of the PureB diodes. Apparently, the presence of the Ga layer under the PureB layer eliminates this degradation of the current. To understand this, it would be helpful to perform material analysis such as TEM and EDS but at the time of writing this thesis these were not yet available. However, from the present results two explanations appear reasonable. On one

hand, the Ga “wetting” layer could plausibly provide a better coverage of the Si and subsequently a more complete PureB coverage. This assumes that the B atoms more readily attach to the Ga atoms than to Si. On the other hand, with a starting layer of Ga, any pinholes in the PureB may lead to Ga oxidation resulting in an improved barrier to the Al. In this connection the PureGa Si diode results should be considered. The available Al-covered μm-sized PureGa diodes display a saturation current that is the same as for the 400 ℃ PureGaB diodes. This is surprising since the Ga is no more than a nm thick and it could be another indication that the Ga functions as a very good wetting layer. However, there is one important difference in the process flow that also may be the beneficial factor: the PureGa only devices were metalized with Al/Si(1%) instead of pure Al so any spiking reactions with the Si would be expected to be prevented. Instead, Si precipitates *p*-doped with Al [103] onto the Si-substrate is more likely and the formation of Al-to-Si Schottky diodes will be less probable. Another factor that may play a role for achieving low saturation-current is a degree of oxidation of the Ga. Nevertheless, this is expected to be very limited due to the very short time that the as-deposited samples were exposed to air.

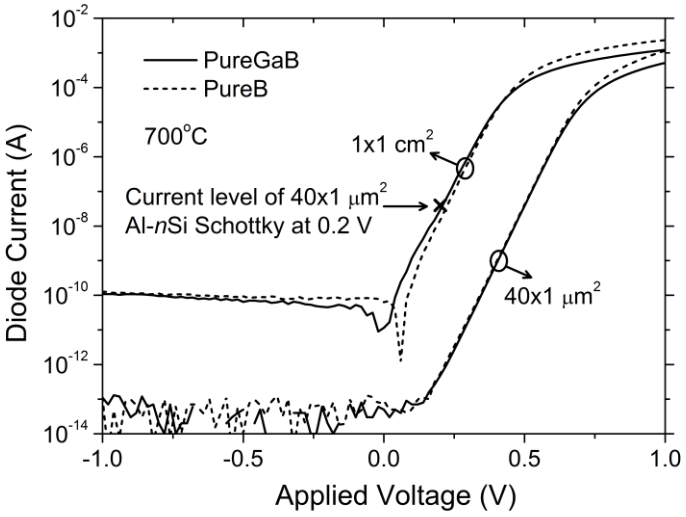


Fig. 7.9. *I-V* characteristics of PureGaB and PureB diodes with different dimensions. The PureB deposition for all the diodes is performed at 700 ℃ for 6 min. The cross marks the current level of a 40×1 μm^2 Al-to-*n*Si Schottky diode at 0.2 V forward bias.

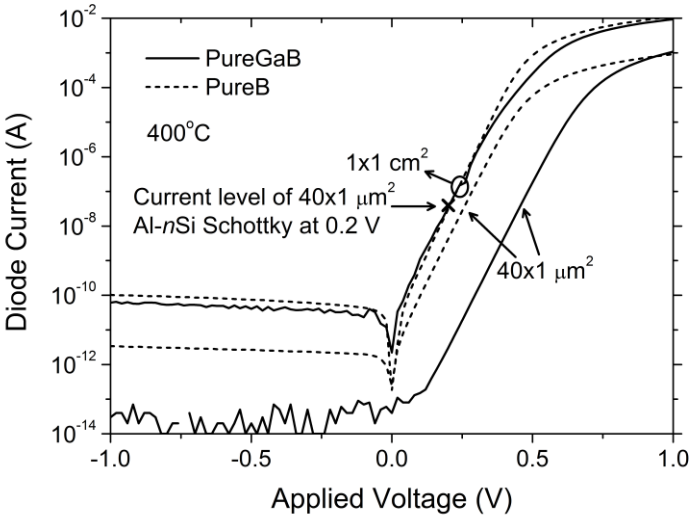


Fig. 7.10. *I-V* characteristics of PureGaB and PureB diodes with different dimensions. The PureB deposition for all the diodes is performed at 400 ℃ for 20 min. The cross marks the current level of a 40×1 μm^2 Al-to-*n*Si Schottky diode at 0.2 V forward bias.

7.3.3 Vertical an lateral *pnp* characteristics

To further investigate the properties of PureGaB diodes, lateral *pnp* bipolar transistors with PureGaB diodes as emitters were fabricated and measured as described in Chapter 3. From the Gummel plots shown in Fig. 7.11 (for 400 ℃ and 700 ℃ PureGaB diodes) and Fig. 7.3 (for PureGa diodes), the collector current is determined to be about 1 nA at V_{BE} = 0.4 V forward in all cases. This confirms that in all cases, holes are injected into a base region that is about the same in all cases, being defined by the *n*-substrate doping and the distance between the emitter and collector contact windows.

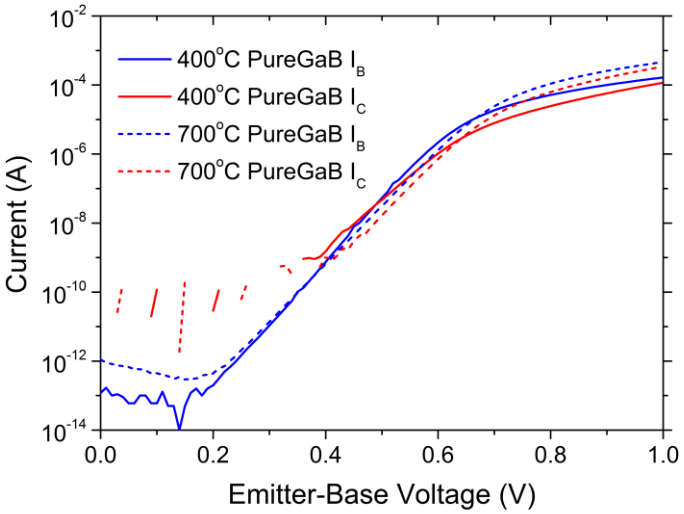


Fig. 7.11. Gummel plots of a *pnp* lateral transistor created with PureGaB diodes. The emitter area is 40×1 μm^2.

To further verify the results, vertical *pnp* transistor structure with PureGaB and PureB diodes as emitters were fabricated and measured as described in Chapter 2. For the PureB layer deposited at 700 ℃, as shown in Fig. 7.12, the PureGaB and PureB *pnp* transistors behave very alike. For the PureGaB and PureB *pnp* transistors with 400 ℃ deposited PureB layer, as shown in Fig. 7.13, although the base current caused by electron thermionic emission from the Al-Si contacts through pin-holes of PureB layer for the PureB transistor, is high. The collector current caused by the hole injection to the substrate is similar to the PureGaB transistor, this suggests that the PureB-Si junction is actually still behaves like a p^+-*n* junction.

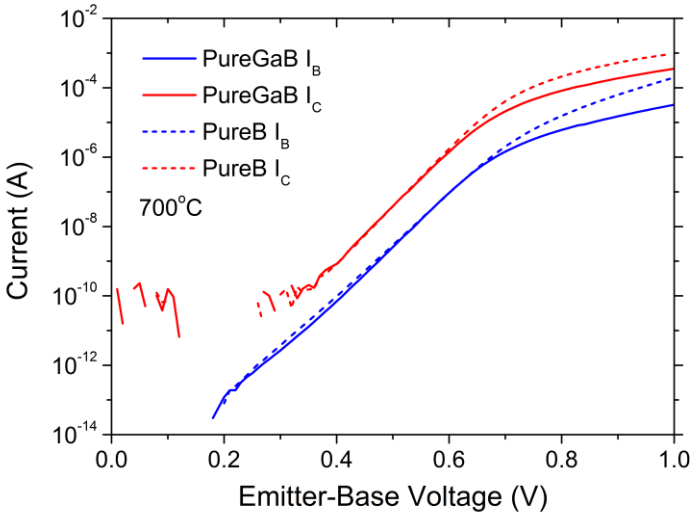


Fig. 7.12. Gummel plot of PureGaB and PureB *pnp* vertical transistors. The PureB deposition for all the diodes is performed at 700 ℃ for 6 min and the emitter area is 40×1 μm^2.

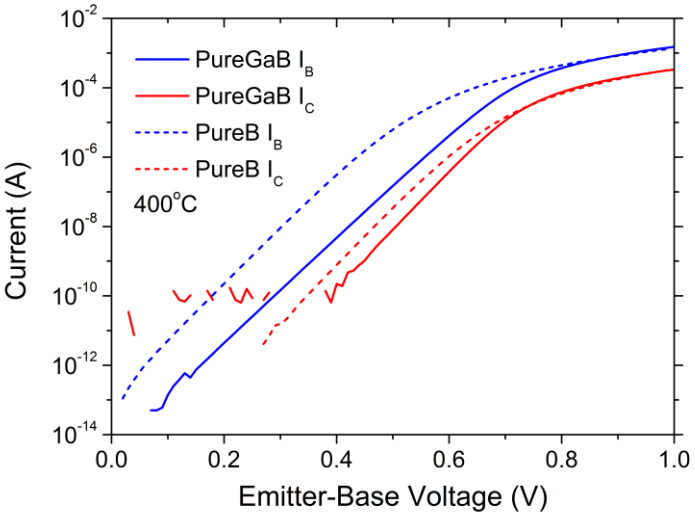


Fig. 7.13. Gummel plot of PureGaB and PureB *pnp* vertical transistors. The PureB deposition for all the diodes is performed at 400 ℃ for 20 min and the emitter area is 40×1 μm^2.

7.3.4 Low-energy electron detection

To investigate the optical performance of the PureGaB photodiodes, devices were mounted in DIL40 packages as shown in Fig. 7.14 and measurements with low-energy electrons were performed. Here the most interesting diodes where all depositions are performed at 400 °C are tested.

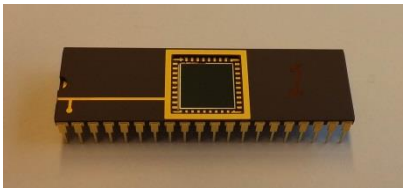


Fig. 7.14. PureB diode in a DIL40 package, the active area is 1 ×1 cm^2.

In [39] it was already shown that the 400 °C PureB photodiodes had a responsivity in the UV comparable to the 700 °C devices as well as an equally good signal gain and robustness for low-energy electron irradiation. To measure the electron detection efficiency, photodiodes were mounted in a SEM system and the electron gun was used as the electron source. The electron beam that arrives on the photodiode surface has an input current of I_{beam}, and the electron energy varies from 200 eV to 10 keV in this measurement. The electron signal gain, G_{PH}, is defined as the ratio of beam induced current between the detected electrons and the incident electrons, which can be expressed by the equation below

$$G_{PH} = \frac{I_{ph} - I_{dark}}{I_{beam}} \tag{7.2}$$

where I_{dark} is the photodiode dark current, which can be neglected for electron energies above 1 keV due to the fact that the value is typically a thousand times lower than the output current, I_{ph}, induced by the irradiation of electron beam, which is measured on an external picoampmeter. The electron signal gain for a PureGaB photodiode was measured and plotted in Fig. 7.15. The difference between a PureGaB and a PureB photodiode is very small and both values are close to the theoretical gain value G_{TH} which can be defined as [104]:

$$G_{TH} = \frac{E_{beam}(1-\eta)}{\varepsilon} \tag{7.3}$$

where E_{beam} is the energy of electron beam; ε is the mean energy to produce an electron-hole pair in silicon equal to 3.61 eV [15]; and η is the backscatter-coefficient, which is generally approximated to be around 5% for Si photodiodes. This result also supports the conclusion that the Ga layer is very thin, no more than a nm. Since Ga has a much higher atomic number than B (31 as compared to 5) a thicker layer would cause a higher scattering of the incoming electrons, thus significantly increasing the absorption in the dead layer.

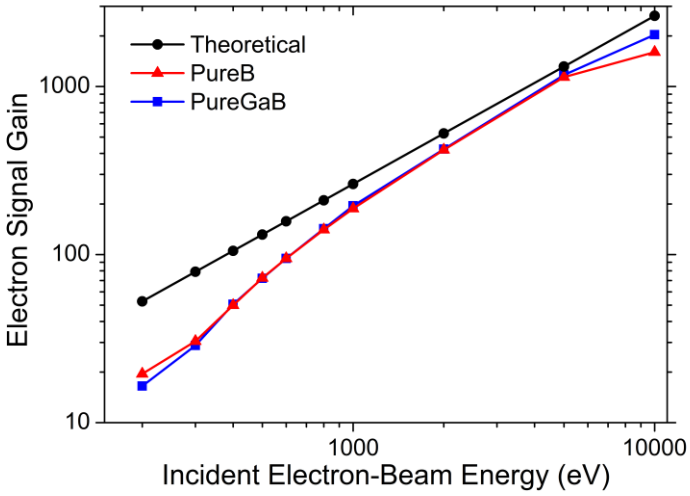


Fig. 7.15. Measured electron signal gain for PureGaB and PureB photodiodes deposited at 400 ℃, the theoretical value for a Si photodiode is plotted as well. The device area is 1×1 cm^2. The signal gain falls off near 10 keV because of the limited depletion width of about 1 μm.

The relative electron signal gain, G_R, is introduced as the ratio of photodiode gain to the theoretical gain [34]:

$$G_R = \frac{G_{PH}}{G_{TH}} = \frac{I_{ph} - I_{dark}}{I_{beam}\left(E_{beam}/\varepsilon\right)\left(1-\eta\right)} \tag{7.4}$$

The stability performance of PureGaB photodiodes was evaluated by exposing the diode to 30-min 1-keV high-dose electron irradiation with a dose rate of 52.4 μC/mm^2. As shown in Fig. 7.16, similar to the behavior of the 400 °C

PureB photodiode, a slight decrease in signal gain, about 2%, is observed. This can be caused by the build-up of carbon on the exposed diode surface [105], and a clear discoloration in the SEM image of the exposed area is observed as shown in Fig. 7.17.

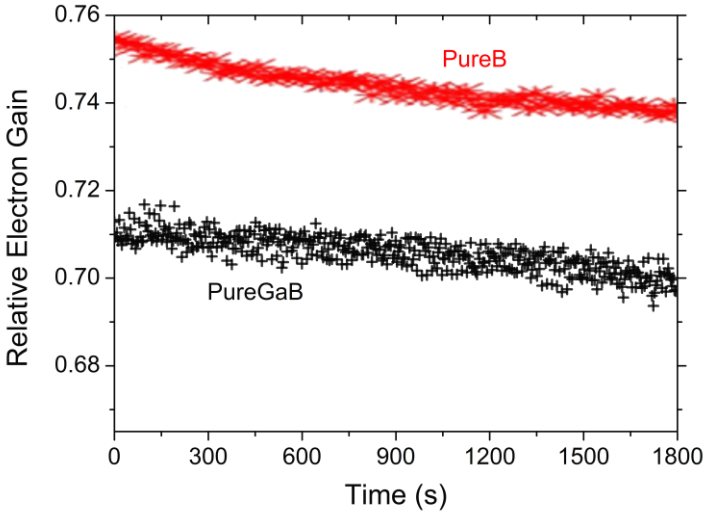


Fig. 7.16. Measured relative electron signal gain at 1 keV for PureGaB and PureB photodiodes deposited at 400 ℃. The device area is 1×1 cm^2.

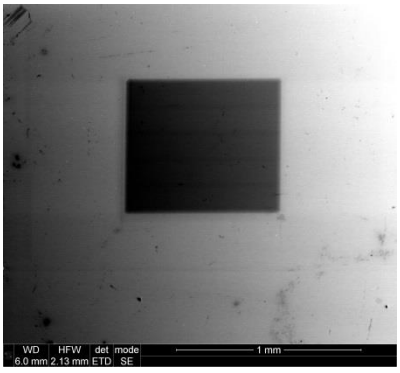


Fig. 7.17. SEM image of the exposure center of the PureGaB photodiode after 30-min 1-keV high-dose irradiation.

7.4 Conclusions

The study of photodiodes fabricated with PureGaB technology presented in this chapter has shown that the PureB and PureGaB diodes are very similar in many respects. The lateral sheet resistance value measured when PureGaB was deposited instead of solely PureB was comparable to that of the PureB-only case for the same PureB deposition conditions. This is understandable because, even though the resistivity of bulk Ga is much lower than that of B, it appears that no more than a nm of Ga actually remains on the Si surface. This very thin layer of Ga, deposited at 400 ℃ for 20 min, nevertheless delivered p^+-n junction diodes with I-V characteristics close to those of PureB diodes with the boron deposited at 700 ℃. By adding the PureB, either at 700 ℃ or 400 ℃, PureGaB diodes were created with I-V characteristics that were as good as those of the 700 ℃ PureB diodes. In contrast, when 400 ℃ PureB diodes were processed with Al coverage of the PureB, after the alloying step the forward current was increased by decades. This was accorded to Al-to-Si Schottky diodes being created through pin-holes in the very rough 400 ℃ PureB layer. A Ga coverage before B deposition resulted in a layer that had better performance as a barrier against the Al metal interconnect. When the Al is removed to have a PureGaB-only front-entrance window, the performance with respect to low-energy electron detection is comparable to the 700 ℃ PureB diodes, both with respect to signal gain and robustness. Overall, this work shows that 400 ℃ PureGaB photodiodes can equal the 400 ℃ and 700 ℃ PureB photodiodes in optical performance while having the added advantage of being more reliable as a barrier layer to metallization. This initial work on PureGaB p^+-n diodes shows that it could be an attractive alternative to PureB-only for low-temperature integration but more aspects of the material stack need to be investigated before a complete comparison can be made.

Chapter 8

Conclusions and Recommendations

8.1 Conclusions

The primary goal of this thesis was to explore and enhance the capabilities of PureB photodiodes in view of their excellent performance for the detection of low-penetrating-beams such as EUV/VUV/DUV light and low-energy electrons. Focus was placed on a further investigation of the properties of the PureB layer in relationship to the low saturation/dark current behavior and of the low-temperature deposition for enhancing CMOS compatibility also as a back-end step. Moreover, a process was developed for the integration of micrometer-sized photodiodes for sensitive imaging purposes. The main conclusions of this thesis are summarized as follow:

- Easy-to-fabricate lateral bipolar test structures were with profit used to separate diode currents into electron and hole currents when evaluating the effectiveness of surface doping to form ultrashallow junctions. From the level of minority carrier injection into the substrate and into the surface-doped region, the type of junction can be identified. With laser-annealed diodes made with different degrees of dopant drive-in, devices were found with electrical characteristics representative of either pure Schottky behavior or pure *p*-*n* junction behavior as well as the intermediate case where the surface doping became fully-depleted under reverse and low-voltage forward biasing conditions.
- The sheet resistance of the *p*-type region created along Si surfaces covered with PureB layers was reliably determined with new in-line test structures. The sheet resistance increases from 10 kΩ/sq to 35 kΩ/sq when going from a 700 ℃ deposition down to 400 ℃. The sheet resistance was influenced by the substrate voltage and substrate doping concentration as would be expected for a Si region with such sheet

resistance values. Only the temperature coefficients behaved differently: they were negative as opposed to the normally positive values for crystalline Si resistors.

- A physical model was proposed that could explain the unique electrical and optical behavior of PureB diodes. This model assumes that the chemical bonding of the B atoms to the Si atoms at the surface creates a monolayer of acceptor states filled with electrons. This attracts holes to the interface forming an inversion layer that, in particular, can account for the sheet resistance and *I-V* characteristics of the 400 ℃ diodes. For the first, the Gummel number of the p^+ region is very high and corresponds well with the number of atoms on the Si surface, ~ 10^{15} atoms/cm^2, and secondly, the gradient of the hole concentration gives a high electric field up to the surface that increases photodiode responsivity by suppressing the injection of electrons into the anode.
- The in-line sheet resistance measurements were a sensitive monitor for the perfection of the PureB-to-Si interface. Incomplete coverage, for example for short deposition times, or detrimental effects of post-processing steps could be detected. Particularly, the 400 ℃ PureB deposition proved sensitive to processing steps associated with Al deposition and removal, showing an increase in sheet resistance.
- The properties of 400 ℃ PureB diodes were improved by adding a Ga deposition before the B deposition. These “PureGaB” diodes were tested for low-energy electron detection and showed electrical and optical properties similar to 700 ℃ PureB diodes. In contrast to the B layer in 400 ℃ PureB diodes, the layer stack of Ga and B in PureGaB devices formed a good barrier to pure Al metallization.
- With the 700 ℃ PureB deposition it was possible to fabricate micrometer-sized SPADs with very low leakage-current (<<10^{-12} A) up to a breakdown that was marked by an abrupt current increase of 5 decades in less than 100 mV. The device exhibits a very low frequency of dark counts with a 5 Hz DCR at room temperature for a low excess-bias of 0.5 V, a more than 11% PDP in the UV region at 370 nm, and an afterpulsing probability of less than 1%. The PureB SPAD also showed high and uniform sensitivity across the front-entrance window when

detecting low-energy electrons in the energy range from 200 eV to 2000 eV.

8.2 Recommendations for Future Work

- On the basis of the available experimental data, a simple model was proposed to explain that the 400 ℃ PureB diodes behave electrically and optically like the 700 ℃ diodes. More investigations, also of the chemical nature of the B-Si bond, should be performed to further substantiate the theory. In particular, a model that can be employed in a simulation tool is needed for predicting the electrical and optical behavior.
- The sheet resistance test structures could be the source of much more information if metal contacts could be added without influencing the as-deposited layer so that also diode *I-V* and *C-V* measurements could be performed on the same structures.
- Methods to lower the resistivity of the PureB layer itself without increasing the layer thickness or deteriorating the layer robustness or diode quality would be of benefit for high-speed applications.
- PureGaB diodes have shown promising electrical and optical characteristics, but the structure and functioning of the Ga layer still needs to be studied in detail for an optimization of these devices as back-end add-ons to fully-processed CMOS wafers.
- In this thesis only discrete SPAD pixels have been fabricated and studied. In the future, work should be performed to enable mega-pixel arrays. In addition, the performace of the individual SPADs should be investigated with an active quenching circuit, preferably integrated along with the SPAD to increase the dynamic range and speed performance.
- The PureB SPADs showed high response to UV light down to 270 nm in wavelength and low-energy electrons down to 200 eV. This optical characterization should be extended to down to soft-xray wavelengths and electron energies at least down to 100 eV.

Bibliography

[1] International technology roadmap for semiconductors (ITRS), process integration devices, and structures summay, 2013.Edition [Online]. Available: http://www.itrs.net/

[2] L.K. Nanver, A. Sammak, V. Mohammadi, K.R.C. Mok, L. Qi, A. Šakic, N. Golshani, J. Derakhshandeh, T.M.L. Scholtes, W.D. de Boer, "Pure dopant deposition of B and Ga for ultrashallow junctions in Si-based devices," *in ECS Transaction 2012: 27th Symposium on Microelectronics Technology and Devices (SBMicro2012)*, Brasilia, Brazil, Aug. 2012, pp. 25-33.

[3] D. Girginoudi, N. Georgoulas, A. Thanailakis, and E.K. Polychroniadis, "Silicon damage and dopant behavior studies of rapidly thermally processed arsenic-implanted silicon," *Advanced Short-time Thermal Processing for Si-based CMOS Devices: Proceedings of the International Symposium*, vol. 2003, pp.397-402, The Electrochemical Society.

[4] L. Shi, S. Nihtianov, L.K. Nanver, and F. Scholze, "Stability Characterization of High-Sensitivity Silicon-Based EUV Photodiodes in a Detrimental Environment," *IEEE Sensors Journal*, vol. 13, Issue 5, pp. 1699-1707, May 2013.

[5] A. Gottwald and F. Scholze, "Advanced Si radiation detectors in the VUV and EUV spectral range," *Smart sensors and MEMS*, 2013, pp. 102-123, UK: Woodhead Publishing Limited.

[6] Francesco Sarubbi, "Characterization of pure boron depositions integrated in silicon diodes for nanometer-deep junction applications," *Ph.D. dissertation*, EEMCS, TU Delft, Delft, 2010.

[7] S. M. Sze and K.K. Ng, *Physics of semiconductor devices*, 3rd ed. 2008: Wiley India Pvt. Ltd.

[8] T. Stokes, "Tutorial: Avalanche photodiodes theory and applications," *Photonics Online*, Dec. 2005.

[9] S. L. Miller, “Avalanche breakdown in germanium,” *Physical Review*, vol. 99, pp. 1234–1241, Aug. 1955.

[10] “Avalanche photodiode: a user guide,” *Application note - high performance sensors*, 2010, Perkin Elmer Optoelectronics Co.

[11] G. V. Karve, “Avalanche photodiodes as single photon detectors,” *Ph.D dissertation*, University of Texas, 2005.

[12] Filip Tavernier, Michiel Steyaert, *High-Speed Optical Receivers with Integrated Photodiode in Nanoscale CMOS*, 2011, Springer Science & Business Media.

[13] Wayback Machine, SETi, http://www.s-et.com, accessed 2008.

[14] L. Shi, L.K. Nanver; S.N. Nihtianov, “Stability characterization of high-sensitivity silicon-based EUV photodiodes in a detrimental industrial environment,” in *37th Annual Conference of the IEEE Industrial Electronics Society (IECON 2011)*, Melbourne, Australia, Nov. 2011, pp. 2651 - 2656.

[15] F. Scholze, H. Rabus and G. Ulm, “Mean energy required to produce an electron-hole pair in silicon for photons of energies between 50 and 1500 eV,” *Journal of Applied Physics*, vol. 84, no. 5, pp. 2926-2939, Sept. 1998.

[16] F. Scholze, H. Henneken, P. Kuschnerus, H. Rabus, M. Richter and G. Ulm, “Determination of the electron-hole pair creation energy for semiconductors from the spectral responsivity of photodiodes,” *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 439, no. 2-3, pp. 208-215, Jan. 2000.

[17] C. S. Tindall, N. P. Palaio, B. A. Ludewigt, S. E. Holland, D. E. Larson, D. W. Curtis, S. E. McBride, T. Moreau, R. P. Lin, and V. Angelopoulos, “Silicon detectors for low energy particle detection,” *IEEE Transaction on. Nuclear Science*, vol. 55, no. 2, pp. 797–801, Apr. 2008.

[18] W. Dulinski, A. Braem, M. Caccia, G. Claus, G. Deptuch, D. Grandjean, C. Joram, J. Séguinot, and M. Winter, “Tests of a backside illuminated monolithic CMOS pixel sensor in an HPD set-up,” *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 546, pp. 274-280, Jul. 2005.

[19] R. Goldstein, S. Nikzad, M. Davis, R. Frahm, D. Slater, and T. J. Jones, “Results of measurements of the response of a delta-doped CCD to neutral and charged particle beams,” *Advances Space Research*, vol. 47, no. 11, pp. 1931–1936, Jun. 2011.

[20] Y. Degerli, M. Besancon, A. Besson, G. Claus, G. Deptuch, W. Dulinski, N. Fourches, M. Goffe, A. Himmi, Y. Li, P. Lutz, F. Orsini, and M. Szelezniak, “Performance of a fast binary readout CMOS active pixel sensor chip designed for charged particle detection,” *IEEE Transaction on. Nuclear Science*, vol. 53, no. 6, pp. 3949–3955, Dec. 2006.

[21] P. Morrissey, S. Kaye, C. Martin, J. Sheung, S. Nikzad, T. Jones, J. Blacksberg, M. Hoenk, and L. D. Bell, “A novel low-voltage electron bombarded CCD readout,” *Proceeding SPIE Astronomical Telescopes+ Instrumentation*, vol. 6266, p. 626610, Jun. 2006.

[22] W. Werner, “Tutorial on Electron Spectroscopies,” 20.10.2011. Available from: http://eaps4.iap.tuwien.ac.at/~werner/qes_tut.html#main

[23] JB Pawley, “LVSEM for high resolution topographic and density contrast imaging,” P. Hawkes (Ed.), *Advances in Electronics and Electron Physics*, vol. 83, pp. 203–273, 1992.

[24] O. Kurniawan and V. K. S. Ong, “Investigation of range-energy relationships for low-energy electron beams in silicon and gallium nitride,” *Scanning*, vol. 29, no. 6, pp. 280–286, 2007.

[25] Y. Kiyota, F. Yano, S. Suzuki, and T. Inada, “Role of hydrogen during rapid vapor-phase doping analyzed by x-ray photoelectron spectroscopy and Fourier-transform infrared-attenuated total reflection," *Journal of Vacuum Science and Technology A*, vol. 16, no. 1, pp. 1-5, 1998.

[26] F. Sarubbi, L.K. Nanver, T.L.M Scholtes, “High effective Gummel number of CVD boron layers in ultrashallow p+n diode configurations,” *IEEE Transactions on Electron Devices*, vol. 57, issue. 6, pp. 1269-1278, Jun. 2010.

[27] G.L. Vick, K.M. Whittle, “Solid solubility and diffusion coefficients of boron in silicon,” *Journal of the electrochemical society,* vol. 116, no.8, pp. 1142-1144, 1969.

[28] V. Mohammadi, S. Ramesh, L.K. Nanver, “Thickness evaluation of

deposited PureB layers in micro-/millimeter-sized windows to Si", *27th IEEE International Conference on Microelectronic Test Structures (ICMTS 2014)*, Udine, Italy, Mar. 2014, pp. 194-199.

[29] A. Šakic, T. L. M. Scholtes, W. de Boer, N. Golshani, J. Derakhshandeh and L. K. Nanver, "Arsenic-doped high-resistivity-silicon epitaxial layers for integrating low-capacitance diodes," *Materials*, vol. 4, pp.2092-2107, Dec. 2011.

[30] Lis K. Nanver, Lin Qi, Vahid Mohammadi, K.R.M. Mok, Wiebe B. de Boer, Negin Golshani, Amir Sammak, Thomas L.M. Scholtes, Alexander Gottwald, Udo Kroth, and Frank Scholze, "Robust UV/VUV/EUV PureB Photodiode Detector Technology with High CMOS Compatibility," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 20, issue 6, pp. 1-11, Nov. 2014.

[31] M. Kleefstra, "Use of the gummel" number in calculating the diffusion current density in schottky diodes," *Solid-State Electronics*, vol. 25, no. 1, pp. 63-66, 1982.

[32] H. C. de Graaff and F. M. Klaassen, *Computational microelectronics*, S. Selberherr, Ed. Springer-Verlag/Wien, 1990.

[33] P. Maleki, T.L.M. Scholtes, M. Popadic, F. Sarubbi, G. Lorito, S. Milosavljevic, W.B. de Boer, and L.K. Nanver, "Deep p+ junctions formed by drive-in from pure boron depositions," *10th International Workshop on Junction Technology (IWJT 2010)*, Shanghai, China, 10-11 May. 2010, pp. 1-4.

[34] Agata Šakic, "Silicon technology for integrating high-performance low-energy electron photodiode detector," *Ph.D. dissertation*, EEMCS, TU Delft, Delft, 2012.

[35] A. Šakic, L.K. Nanver, G. van Veen, K. Kooijman, P. Vogelsang, T.L.M. Scholtes, W. de Boer, W.H.A. Wien, S. Milosavljević, C.T.H. Heerkens, T. Knežević, I. Spee, "Versatile silicon photodiode detector technology for scanning electron microscopy with high-efficiency sub-5 keV electron detection," *2010 IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 6-8 Dec. 2010, pp. 31.4.1-31.4.4.

[36] L.K. Nanver, L. Qi, A. Sammak, K. R. C. Mok, M. Aminian, E. Charbon,

"Towards CMOS-Compatible Photon-Counting Imagers in the Whole 10 nm - 1600 nm Spectral Range with PureB Si and PureGaB Ge-on-Si Technology," *12th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT 2014)*, Guilin, China, Oct. 2014, pp. 644-647.

[37] A. Šakić, V. Jovanović, P. Maleki, T. L.M. Scholtes, S. Milosavljević, L. K. Nanver, "Characterization of amorphous boron layers as diffusion barrier for pure aluminium," *Proceeding International Convention MIPRO 2010*, Opatija, Croatia, 2010, pp. 52-55.

[38] A. Šakic, G. van Veen, K. Kooijman, P. Vogelsang, T. L. M. Scholtes, W. B. de Boer, J. Derakhshandeh, W. H. A. Wien, S. Milosavljevic and L. K. Nanver, "High-efficiency silicon photodiode detector for sub-keV electron microscopy," *IEEE Transactions on Electron Devices*, vol. 59, no. 10, pp. 2707-2714, Oct. 2012.

[39] V. Mohammadi, L. Qi, N. Golshani, K. R. C. Mok, W. B. de Boer, A. Sammak, J. Derakhshandeh, J. van der Cingel, L. K. Nanver, "VUV/Low-Energy-Electron Si Photodiodes with Post-Metal 400°C PureB Deposition," *IEEE Electron Device Letters*, vol. 34 , issue 12, pp. 1545 – 1547, 2013.

[40] L. Shi, S. Nihtianov, L. Haspeslagh, F. Scholze, A. Gottwald, and L.K. Nanver, "Surface-Charge-Collection-Enhanced High-Sensitivity High-Stability Silicon Photodiodes for DUV and VUV Spectral Ranges," *IEEE Transactions on Electron Devices*, vol. 59, pp. 2888-2894, Nov. 2012.

[41] L.K. Nanver, A. Sammak, V. Mohammadi, K. R. C. Mok, L. Qi, A. Šakić, N. Golshani, J. Derakhshandeh, T. M. L. Scholtes, W. D. de Boer, "Pure dopant deposition of B and Ga for ultrashallow junctions in Si-based devices", *ECS Transactions*, Vol. 49, No. 1, pp. 25-33, 2012.

[42] S. Sluyterman, I. Gestmann, E.G.T. Bosch, J. Derakhshandeh, L.K. Nanver and L.Y. Roussel, "New detection methods for fast analysis of nano-particles," *Microscopy Conference MC2013*, Regensbourg, Germany, August 25-30, ID 638.

[43] T. Knežević, T. Suligoj, A. Šakić, and L.K. Nanver, "Modelling of electrical characteristics of ultrashallow pure amorphous boron p+n junctions," *Proceedings of 35th International Convention MIPRO*, Opatija, Croatia, 2012, pp. 36-41.

[44] L. Qi, G. Lorito, L.K. Nanver, "Lateral-Transistor Test Structures for Evaluating the Effectiveness of Surface Doping Techniques," *IEEE Transactions on Semiconductor Manufacturing*, vol. 25, no. 4, pp. 581-588, Nov. 2012.

[45] D. Connelly, P. Clifton, C. Faulkner, and D. E. Grupp, "Ultra-thinbody fully depleted SOI metal source/drain n-MOSFETs and ITRS low-standby-power targets through 2018," *IEDM Technical Digest*, pp. 972–975, 2005.

[46] L.K. Nanver, H. Schellevis, T.L.M. Scholtes, L. La Spina, G. Lorito, F. Sarubbi, *et al*, "Improved RF Devices for Future Adaptive Wireless Systems Using Two-Sided Contacting and AlN Cooling," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 9, pp. 2322-2338, 2009.

[47] R.T. Tung, "Recent advances in Schottky barrier concepts," *Material Science and Engineering R: Reports*, vol. 35, pp. 1-135, Nov. 2001.

[48] D.K. Schroder, *Semiconductor material and device characterization*, 3rd ed. 2006: Wiley-IEEE Press.

[49] M. Popadic, G. Lorito, L.K. Nanver, "Analytical model of I-V characteristics of arbitrarily shallow p-n junctions," *IEEE Transactions on Electron Devices*, vol. 56, pp. 116-125, 2009.

[50] H. K. Gummel, "Measurement of the Number of Impurities in the Base Layer of a Transistor," *Proceedings of the Institute of Radio Engineers*, vol. 49, pp. 834, 1961.

[51] Y. Civale, G. Lorito and C. Xu, "Evaluation of Al-doped SPE ultrashallow p+n Junctions for use as PNP SiGe HBT Emitters," *Proceedings of IEEE International Workshop on Junction Technology (IWJT 2008)*, Shanghai, China, pp 97-100, 15-16 May 2008.

[52] P.J. Chen, K. Misiakos, et al. "Analytical solution for two-dimensional current injection from shallow p-n junctions," *IEEE Transactions on Electron Devices*, vol. 32, no.11, pp. 2292-2296, Nov. 1985.

[53] J. Lindmayer and W. Schneider, "Theory of lateral transistors," *Solid-State Electronics*, vol.10, no.3, pp. 225-234, 1967.

[54] E. H. Rhoderick, "Transport Processes in Schottky Diodes," *Metal-Semiconductor Contacts, Institute of Physics, London*, pp. 3-19, 1974.

[55] A. Sammak, L. Qi, W.B. de Boer, L.K. Nanver, "Chemical vapor deposition of Ga dopants for fabricating ultrashallow pn junctions at 400 ℃," *Proceedings of 10th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT 2010)*, Shanghai, China, pp. 969 – 971, 1-4 Nov. 2010.

[56] Agata Šakic, Lin Qi, Tom L.M. Scholtes, Johan van der Cingel, and Lis K. Nanver. "Epitaxial growth of large-area p^+n diodes at 400 ℃ by Aluminum-Induced Crystallization," *Proceedings of the European Solid-State Device Research Conference (ESSDERC)* , Bordeaux, France, pp. 145-148, Sept. 2012.

[57] L. Qi and L. K. Nanver, "Conductance along the Interface Formed by 400°C Pure Boron Deposition on Silicon," *IEEE Electron Device Letters*, vol. 36, issue 2, pp. 102-104, Feb. 2015.

[58] S. B. Evseev, L. K. Nanver, S. Milosavljević, "Ring-gate MOSFET Test Structures for Measuring Surface-Charge-Layer Sheet Resistance on High-Resistivity-Silicon Substrates," *Proceeding International Conference on Microelectronic Test Structures (ICMTS 2006)*, Austin, USA, pp.3-8, 2006.

[59] L.J. van der Pauw, "A method of measuring the resistivity and Hall coefficient on lamellae of arbitrary shape," *Philips Technical Review*, vol. 20, pp. 220–224, 1958.

[60] N. Golshani, V. Mohammadi, S. Ramesh, L. K. Nanver, "High-Ohmic Resistors using Nanometer-Thin Pure-Boron Chemical-Vapour-Deposited Layers," *43rd Solid-State Device Research Conference (ESSDERC)*, Sep. 16-20, Bucharest, Romania, Paper ID 1401, 2013.

[61] D.S. Jeon and D.E. Burk, "MOSFET electron inversion layer mobilities - a physically based semi-empirical model for a wide temperature range," *IEEE Transactions on Electron Devices*, vol. 36, no. 8, pp. 1456-1463, 1989.

[62] D.B.M. Klaassen, "A unified mobility model for device simulation – I. Model equations and concentration dependence," *Solid-State Electronics*, vol. 35. no. 7, pp. 953-959, 1992.

[63] Raymond A. Serway, *Principles of Physics*, 2nd ed, Fort Worth, Texas; London: Saunders College Pub, p. 602, 1998.

[64] Lin Qi, K. R. C. Mok, Mahdi Aminian, Tom L.M. Scholtes, Edoardo Charbon and Lis K. Nanver, “Reverse Biasing and Breakdown Behavior of PureB Diodes,” *13th International Workshop on Junction Technology (IWJT 2013)*, Kyoto, Japan, 6-7 Jun. 2013, pp. 70-73..

[65] Lin Qi, K. R. C. Mok, Mahdi Aminian, Edoardo Charbon and Lis K. Nanver, “Fabrication of Low Dark-Count PureB Single-Photon Avalanche Diodes,” *Proceedings of SBMicro 2014*, Aracaju, Brazil, 1-5 Sept. 2014, pp. 1-4.

[66] R.H. Haitz, “Mechanisms Contributing to the Noise Pulse Rate of Avalanche Diodes,” *Journal of Applied Physics*, vol. 36, no. 10, Oct. 1965.

[67] S. Cova, M. Ghioni, A. Lotito, I. Rech, and F. Zappa, “Evolution and prospects for single-photon avalanche diodes and quenching circuits,” *Journal of Modern Optics*, vol. 51, no. 9, pp. 1267-1288, Jul. 2004.

[68] F. Zappa, S. Tisa, A. Tosi, and S. Cova, “Principles and features of single-photon avalanche diode arrays,” *Sensors and Actuators A-Physical*, vol. 140, no. 1, pp. 103-112, Oct. 2007.

[69] Mohammad Azim Karami, “Deep-submicron CMOS Single Photon Detectors and Quantum Effects,” *Ph.D. dissertation*, EEMCS, TU Delft, Delft, 2011.

[70] A. Gulinatti, P. Maccagnani, I. Rech, M. Ghioni, and S. Cova, “35 ps time resolution at room temperature with large area single photon avalanche diodes,” *Electronics Letters*, vol. 41, no. 5, pp. 272-274, Mar. 2005.

[71] Shingo Mandai, “Multi digital silicon photomultipliers for time-of-flight PET,” *Ph.D. dissertation*, EEMCS, TU Delft, Delft, 2014.

[72] S. Cova, A. Lacaita, and G. Ripamonti, “Trapping phenomena in avalanche photodiodes on nanosecond scale,” *IEEE Electron Device Letters*, vol.12, pp. 685-687, 1991.

[73] V. Mohammadi, W.B. de Boer, L.K. Nanver, “An Analytical Kinetic Model for Chemical-Vapor Deposition of Pure-Boron Layers from Diborane,” *Journal of Applied Physics*, vol. 112, nr.113501, 2012.

[74] A. Lacaita, M. Ghioni, and S. Cova. "Double epitaxy improves single-photon avalanche diode performance." Electronics Letters, vol. 25, no. 13, pp. 841-843, 1989.

[75] V. Mohammadi, W. B. de Boer, T. L. M. Scholtes and L. K. Nanver, "Pattern dependency and loading effect of pure-boron-layer chemical-vapor deposition", *ECS Journal of Solid State Science and Technology*, vol. 1, no. 1, pp. Q16-Q20, 2012.

[76] Lin Qi, K. R. C. Mok, Mahdi Aminian, Edoardo Charbon and Lis. K. Nanver, "UV-Sensitive Low Dark-Count PureB Single-Photon Avalanche Diode," *IEEE Transactions on Electron Devices*, vol. 61, issue 11, pp. 3768-3774, Nov. 2014.

[77] Lin Qi, S. Sluyterman, K. Kooijman, K.R.C. Mok and Lis K. Nanver, "PureB Single-Photon Avalanche Diodes for Low-Energy Electron Detection Down to 200 eV," *Optics Letters*, vol. 40, issue 3, pp. 300-303, Feb. 2015.

[78] S. M. Sze and G. Gibbons, "Avalanche Breakdown Voltages of Abrupt and Linearly Graded p-n Junctions in Ge, Si, GaAs, and GaP," *Applied Physics Letters*, vol. 8, issue 5, pp. 111-113, Mar. 1966.

[79] TCAD, Synopsys, http://www.synopsys.com/Tools/TCAD.

[80] G.A.M. Hurkx et al., "A new analytical diode model including tunneling and avalanche breakdown," *IEEE Transactions on Electron Devices*, vol. 39, p. 2090, 1992.

[81] E. Charbon, M.W. Fishburn. "Monolithic Single-Photon Avalanche Diodes: SPADs," *Single-Photon Imaging*, Springer Berlin Heidelberg, pp. 123-156, 2011.

[82] Jau-Yang Wu, Sheng-Di Lin, "Simulation of electric field distribution in CMOS single photon avalanche diodes at breakdown voltage," 2014 International Conference on Optical MEMS and Nanophotonics (OMN), pp.187,188, 17-21 Aug. 2014.

[83] F.A. Trumbore, "Solid solubilities of impurity elements in germanium and silicon," *Bell System Technical Journal*, vol. 39, no. 1, pp. 205-233, 1960.

[84] S.K. Ghandhi, *The Theory and Practice of Microelectronics*, John Wiley & Sons, New York, 1968.

[85] L. Imhoff, O. Heintz, V. Gauthier, C. M. de Lucas, and S. Bourgeois, "Chemical characterization of gallium droplets grown by LP-MOCVD," *Applied Surface Science*, vol. 253, no. 5, pp. 2820 – 2824, 2006.

[86] M. J. Bronikowski and R. J. Hamers, "The chemistry of gallium deposition on Si(001) from trimethylgallium: An atomically resolved STM study," *Surface Science*, vol. 348, no. 3, pp. 311–324, Mar 1996.

[87] A. Sammak, W.B. de Boer, A. van den Boogaard, L.K. Nanver, "Merging standard CVD techniques for GaAs and Si epitaxial growth," *ECS Transactions*, vol. 28, issue 5, pp. 237-244, 2010.

[88] R. W. Olesinski, N. Kanani, G. J. Abbaschian, "The Ga−Si (Gallium-Silicon) system," *Journal of Phase Equilibria*, vol. 6, issue 4, pp. 362-364, 1985.

[89] C. D. Thurmond and M. Kowalchik, "Germanium and Silicon Liquidus Curves," *Bell System Technical Journal*, vol.39, pp. 169-204, 1960.

[90] M. F. Stuckings, B. Fischer, G. Giroult, A. Cuevas, M. J. Stocks and A. W. Blakers, "Gallium Contacts on p-type silicon substrates," *Progress in Photovoltaics: Research and Applications*, vol. 9, issue 6, pp. 409-416, 2001.

[91] J. Z. Li, J. Bai, J.-S. Park, B. Adekore, K. Fox, M. Carroll, A. Lochtefeld and Z. Shellenbarger, "Defect reduction of GaAs epitaxy on Si (001) using selective aspect ratio trapping," *Applied Physics Letter*, vol. 91, issue 2, id. 021114 (3 pages), 2007.

[92] Amir Sammak, "Silicon-based integration of groups III, IV, V chemical vapor depositions in high-quality photodiodes," *Ph.D. dissertation*, EEMCS, TU Delft, Delft, 2012.

[93] Jingyun Huang, Zhizhen Ye, Lei Wang, Jun Yuan, Binghui Zhao, Huanming Lu, "Comparison of GaN epitaxial films on silicon nitride buffer and Si(111)," *Solid-State Electronics*, vol. 46, issue 8, pp. 1231-1234, 2002.

[94] Yoshinobu Nakada, Igor Aksenov, and Hajime Okumura, "GaN heteroepitaxial growth on silicon nitride buffer layers formed on Si (111) surfaces by plasma-assisted molecular beam epitaxy," *Applied Physics Letter*, vol. 73, no. 6, pp. 827-829, 1998.

[95] Jieun Cho, Manik Kumer Ghosh, and Cheol Ho Choi, "Adsorption Reactions of Trimethylgallium and Arsine on H/Si(100)-2x1 Surface," *Bulletin of the Korean Chemical Society*, vol. 30, no. 8, pp. 1805-1810,

2009.

[96] Han Woong Yeom, Kwonjae Yoo1, Dong-Hwa Oh, “Electronic structures of Ga-induced incommensurate and commensurate overlayers on the Si(111) surface,” *Surface Science*, vol. 605, issues 1-2, pp. 146-152, 2001.

[97] A. Sammak, M. Aminian, L. Qi, W.B. de Boer, E. Charbon, L.K. Nanver, ”A CMOS Compatible Ge-on-Si APD Operating in Proportional and Geiger Modes at Infrared Wavelengths,” *in Proceedings of International Electron Device Meeting (IEDM 2011)*, Washington DC, USA, Dec. 2011, pp. 8.5.1 - 8.5.4.

[98] N. Saitoh, T. Akamine, K. Aoki, and Y. Kojima, “Composition and growth mechanisms of a boron layer formed using the molecular layer doping process,” *Japanese Journal of Applied Physics,* vol. 32, no. 10, pp. 4404-4407, Oct. 1993.

[99] H.-C. Tseng, F. M. Pan, and C. Y. Chang, “Characterization of boron silicide layer deposited by ultrahigh-vacuum chemical-vapor deposition,” *Journal of Applied Physics*, vol. 80, no. 9, pp. 5377-5383, Nov. 1996.

[100] Amir Sammak, Lin Qi, Lis K. Nanver, “Restricted-access Al-mediated material transport in Al contacting of PureGaB Ge-on-Si p+n diodes,” *Journal of Electronic Materials*, vol. 44, issue 12, pp. 4676-4683, Dec. 2015.

[101] R. Suzuki, S. Nakagomi, and Y. Kokubun, “Solar-blind photodiodes composed of a Au Schottky contact and a β-Ga2O3 single crystal with a high resistivity cap layer,” *Applied Physics Letters*, vol. 98, issue 13, p. 1114, 2011.

[102] T. Oshima, T. Okuno, N. Arai, N. Suzuki, S. Ohira, and S. Fujita, “Vertical solar-blind deep-ultraviolet schottky photodetectors based on β-Ga2O3 substrates,” *Applied Physics Express*, vol. 1, no. 1, p. 011202, 2008.

[103] Y. Civale, L.K. Nanver, P. Hadley, E.J.G. Goudena, H. Schellevis, “Sub-500 ℃ Solid-Phase Epitaxy of Ultra-Abrupt p+-Silicon Elevated Contacts and Diodes,” *IEEE Electron Device Letters*, vol. 27, issue 5, pp. 341-343, 2006.

[104] A. Šakic, L. K. Nanver, T. L. M. Scholtes, C.Th.H. Heerkens, T. Knežević, G. van Veen, K. Kooijman, P. Vogelsang, “Boron-layer silicon

photodiodes for high-efficiency low-energy electron detection," *Solid-State Electron.*, vols. 65–66, pp. 38–44, Jul. 2011.

[105] A. E. Vladár and M. T. Postek, "Electron beam-induced sample contamination in the SEM," Microscopy and Microanalysis, vol. 11, no. 2, pp. 764–765, Aug. 2005.

Summary

Interface Properties of Group-III-Element Deposited-Layers Integrated in High-Sensitivity Si Photodiodes

by Lin Qi

In this thesis, the research on silicon-based CMOS-compatible PureB technology was continued with the goal of enabling a PureB process module that could be added as a back-end module to wafers from a CMOS foundry. The properties of PureB layers deposited at low-temperature, particularly those deposited at 400 ℃ were studied in more detail, among other things by introducing new electrical test structures. A new deposition method including gallium deposition, called PureGaB, was developed to alleviate some of the difficulties encountered when reducing the deposition temperature. Moreover, the capabilities of PureB technology were extended by a demonstration of highly-sensitive single-photon avalanche diodes (SPADs).

As described in Chapter 1, silicon *p*-*n*-junction-based photodiodes can be used to detect light as well as particle beams. To detect a signal, the basic method is to place a *p*-*n*-junction photodiode under zero or small reverse bias so that carriers (electrons and holes) generated by the incoming signal are forced to drift towards the cathode or anode, respectively, under the influence of the electric field across the depletion region, thus forming a generation current. For sensitive detection, this generation current should be high enough, preferably higher than the leakage current of the non-exposed photodiode itself. To improve increase the photo-sensitive region a *p*-*i*-*n* structure can be employed to achieve a wide depletion over the intrinsic region. Moreover, this can also be achieved by using a large reverse bias over a *p*-*n* junction photodiode. The high electric field in this working regime may cause the generation current to be multiplied by an impact ionization process. In addition, it is also possible to operate a *p*-*n* junction photodiode in Geiger-mode for counting single events.

This requires that the device can be biased well above the breakdown voltage without actually inducing breakdown. The device can then become extremely sensitive and can respond to single photons or particles.

In Chapter 2, an introduction to PureB technology is given. With this technology, nm-deep p^+-n junctions can be formed so that the photosensitive depletion region extends almost completely to the Si surface that can be covered solely by a nm-thin layer of pure boron. In earlier work it was shown that the PureB layer could be integrated as a robust and almost non-absorbing light-entrance window. The layer is conductive and does not oxidize, which means that it does not charge during irradiation. With PureB photodiodes, low-penetrating beams such as VUV/DUV and low energy electrons, of which the penetration depth in Si is only a few nm, can be detected with high efficiency. The sheet resistance value of the PureB layer itself is high but a metal grid can be deposited on top of PureB layer to reduce the series resistance of photodiode detectors. To lower the capacitance, the substrate can be covered with a thick ultra-low doped n-Si epi layer. In this way it was possible to achieve low RC values suitable for high-speed applications.

The use of PureB photodiodes in avalanche-mode operation was studied in this thesis work. For the first, the breakdown behavior was characterized for PureB diodes where the anode was fabricated in different ways. The anode windows, etched through oxide to the silicon were opened by four different methods: either entirely wet, by plasma etching with soft- or wet-landing, or by plasma etching about 1 μm into the Si. The reverse current was low and the leakage currents were mainly determined by the depletion of the oxide interface at the diode perimeter. The results support the picture that the PureB coverage is complete right up to the perimeter allowing high breakdown voltages even for diodes without guard rings or with trench-etched anode windows. Nevertheless, the p-type guard rings were found to have a large influence on the saturation current of the diodes, giving about a 2 decades reduction of the current level. This was explained as a result the PureB coverage being terminated at the diode perimeter.

One of the main questions that needed to be answered about the behavior of PureB diodes was the question of which mechanism is responsible for the low saturation currents. To obtain a fast method of evaluating the current flow in diodes processed under different deposition conditions, lateral bipolar test

structures were introduced as described in Chapter 3. In particular, for ultrashallow diodes the electrical behavior can vary from Schottky-like to a hybrid of Schottky and *p*-*n* junction behavior to pure *p*-*n* junction behavior. This depends on the degree of *p*-type counter-doping of the *n*-substrate, if any. Conditions that could lead to the three types of diode behavior were confirmed here by device simulations.

The lateral bipolar test structures were employed in two different measurement configurations. The one was the parallel-diode setup, with three neighboring diodes operated in parallel. By comparing the forward characteristics of the middle diode with and without biasing of the neighboring diodes, the diode type can be determined. For *p*-*n* junction-like behavior with large minority carrier injection to the substrate, the current in the middle diode in the two situations will differ but for Schottky diodes, dominated by thermionic emission of the majority carriers from the substrate, the current is unaffected. In the other setup the three neighboring diodes are biased as a lateral transistor and from the measured base and collector currents the level of minority carrier injection into the base and emitter can be evaluated. This gives information on whether the behavior of the emitter diode can be distinguished as either Schottky-like or *p*-*n* like. From the measurement of these test structures, it was concluded that the low-temperature, 400 ℃ deposited PureB diodes have *p*-*n* junction like behavior similar to the high-temperature PureB diodes deposited at 700 ℃.

Since the deposition of boron at 400 ℃ is not expected to dope the bulk Si, the origin of the high minority-carrier injection from the PureB region to the substrate was also sought by developing test structures to measure the sheet resistance along the PureB-to-Si interface. As discussed in Chapter 4, from all previous experiments it was clear that to get a “clean” measurement the influence of post-deposition processing steps should be eliminated. The new structures allowed a measurement of the sheet resistance directly after deposition and values for layers deposited at 400 ℃ were determined for the first time. To leave no doubt about the validity of the measurements, two different types of test structures were designed and fabricated. The most accurate extraction of the sheet resistance was performed on sets of ring-shaped test structures, but the measurements and extraction procedure are work-intensive. They were used to check the validity of more straightforward measurements on Van der Pauw test structures where the sheet resistance can be

extracted from one *I-V* measurement that can quickly be made over the wafer. Reliable results were obtained showing that the sheet resistance for 400 ℃ deposition was as low as 35 kΩ/sq. For the same boron exposure time, the lower the deposition temperature was, the higher the lateral sheet resistance along the interface of the PureB layers. At 700 ℃ there is some doping of the Si to a solid solubility of $2x10^{19}$ cm^{-3} which corresponds well with the measured sheet resistance of ~ 10 kΩ/sq. This sheet resistance is also insensitive to biasing of the substrate, unlike the 500 ℃ and 400 ℃ deposition for which the sheet resistance increases considerably with substrate-biasing and also with increasing substrate doping. Moreover, for the 400 ℃ deposited PureB layer, the sheet resistance decreases with deposition time, stabilizing after complete coverage is achieved which agrees with the assumption that no bulk doping occurs. Based on the overall results, a simple physical model is proposed for the electrical interface properties of the PureB-on-Si. A monolayer of acceptor states at the interface is assumed to fill with electrons to give a monolayer of fixed negative charge that attracts a monolayer of mobile holes. Besides giving an explanation for the sheet resistance behavior of the 400 ℃ layers, this model also gives an explanation for the very high Gummel number of both the 400 ℃ and the 700 ℃ layers, neither of which can be explained by bulk Si doping.

With the Van der Pauw sheet resistance test structure, some post-processing steps of the PureB layer were investigated. Unlike the 700 ℃ depositions, the lateral sheet resistance of the 400 ℃ and 500 ℃ PureB was very susceptible to these treatments indicating that they disturbed the perfection of the interface. For example, the metal cleaning step nearly removed all the PureB for these low-temperature layers and no sheet resistance value could be extracted. The sheet resistance of the 400 ℃ device increased significantly after metal removal while the 500 ℃ showed only a slight increase. This is related to the surface roughness that is also associated with a higher density of pin-holes. These allow the deposited metal to reach and deteriorate the PureB-Si interface. In general, for the as-deposited PureB layers the non-uniformity of the sheet resistance across the wafer becomes much higher as the deposition temperature is decreased. This is also to be expected since this is an interface property and not the result of bulk doping as for the 700 ℃ deposition.

The capability of PureB photodiodes was further extended by designing and fabricating highly-sensitive, micrometer-sized SPADs that responded to single-photons and electrons. In Chapter 5, the figures of merit of SPADs and the

fabrication process of PureB SPADs were presented. The PureB SPADs work in Geiger-mode, biased well above the breakdown voltage. To prevent edge breakdown, an *n*-enrichment region was implanted beneath the PureB layer to set the breakdown voltage and active region. A lightly-doped epi layer was used to lower the electric field around the edges and corners. The width of this virtualguard ring, i.e. the distance from the *n*-enrichment region to the edge of the nearest anode window was successfully made down to 0.5 μm. The implantation and anneal of this *n*-enrichment region was chosen to avoid an unnecessarily high implantation dose that would result in lower and less abrupt breakdown and higher dark counts. It was also found that the dark count rate increased significantly if plasma etching directly above the PureB layer was performed. Taking these precautions into account, the fabricated PureB SPADs exhibited very low leakage current, less than 1 pA before breakdown, and a very sharp and abrupt breakdown. The devices had very low dark count rate, as low as 5 Hz at room temperature for a device with a diameter of 4 μm.

In Chapter 6, the optical characterization of the fabricated PureB SPADs was presented. The devices displayed a good selectivity to UV light, with a maximum photon detection probability of 11% at a wavelength of 370 nm. The FWHM of timing jitter was 436 ps at an excess bias of 4.5 V and decreased with increasing excess bias voltage. The afterpulsing probability was less than 1% and the dead time was around 6 μs. The fabricated PureB SPADs were tested with low energy electrons, an irradiation with which they displayed a high response for energies down to 200 eV and the experiments indicated that they at least would be sensitive down to 100 eV.

In Chapter 7 a presentation is given of PureGaB photodiodes that were developed to improve the diode performance, particularly those fabricated with 400 ℃ depositions. Although the *p*-type interface in this process is created by first Ga deposition and then B deposition, the sheet resistance along the PureGaB interface proved to be similar to that of the PureB interface under the same PureB deposition conditions. As an advantage though, the PureGaB layer was a better barrier against the Al metallization. The performance in terms of UV detection and low-energy electron detection was similar to that of the PureB photodiodes. Nevertheless, PureGaB photodiodes are still in the initial development stage and the overall stability performance, also for VUV applications, still needs to be thoroughly tested. The results up until now do,

however, show that they have high potential, especially as a low-temperature CMOS-compatible process.

Samenvatting

Interface Properties of Group-III-Element Deposited-Layers Integrated in High-Sensitivity Si Photodiodes

door Lin Qi

In dit proefschrift wordt onderzoek naar op silicium-gebaseerd CMOS-compatibele PureB technologie voorgezet met als doel het bevorderen van een PureB proces module die toegevoegd zou kunnen worden als backend procesmodule voor wafers van een CMOS foundry. De eigenschappen van PureB-lagen gedeponeerd bij lage temperaturen, in bijzonder 400 ℃, worden bestudeerd in meer detail, onder andere door het introduceren van nieuwe elektrische teststructuren. Een nieuwe depositie methode gebruikmakend van ook gallium depositie, genaamd PureGaB, werd ontwikkeld om moeilijkheden in verband met het reduceren van de depositie temperatuur te verminderen. Ook worden de toepassingsmogelijkheden van PureB technologie uitgebreid door het demonstreren van zeer gevoelige single-photon avalanche diodes (SPADs).

Zoals beschreven in Hoofdstuk 1, kunnen silicium fotodiodes op basis van *p*-*n*-juncties gebruikt worden om zowel licht als deeltjes-stralen te detecteren. Het basisprincipe om een signaal te detecteren, is dat de *p*-*n*-junctie gebiased wordt met nul of een kleine sperspanning zodat ladingdragers (elektronen en gaten) gegenereerd door het invallende signaal worden gedwongen om naar respectievelijk de kathode of anode te vloeien onder invloed van het elektrisch veld over het depletie gebied: zo wordt een generatie stroom gewekt. Voor gevoelige detectie moet deze generatiestroom zo hoog mogelijk zijn, liefst hoger dan de lekstroom van de onbelichte fotodiode. Om de respons snelheid en het dynamisch bereik te verhogen, kan een p-i-n structuur gebruikt worden waardoor een brede depletie over het intrinsieke gebied gevormd wordt. Voor een hogere gevoeligheid kan een p-n junctie fotodiode gebiased worden met een hoge sperspanning. Het hoog elektrische veld in dit werkgebied kan veroorzaken dat de generatiestroom wordt vermenigvuldigd door een impact

ionisatie proces. Ook is het mogelijk om een p-n junctie fotodiode te laten werken in Geiger-mode voor het tellen van alleenstaande gebeurtenissen. Dit vraagt dat het device kan worden gebiased ver voorbij de doorslagspanning zonder dat een echte avalanche doorslagstroom wordt geïnduceerd. Zodoende kan een extreme gevoeligheid worden bereikt waarmee een enkele foton of deeltje een avalanche kan veroorzaken.

Hoofdstuk 2 geeft een introductie tot PureB technologie. Hiermee worden nm-diep p^+-n juncties gevormd zodat het fotosensitieve depletie-gebied zich uitstrekt bijna helemaal tot de Si oppervlakte. Deze kan bedekt worden met slechts een nm-dunne laag puur boor. In het eerdere werk werd duidelijk gemaakt dat de PureB laag geïntegreerd kon worden als een robuust en bijna niet-absorberend venster voor het invallende licht. De laag is geleidend en oxideert niet, wat betekent dat het niet verandert tijdens irradiatie. Met PureB fotodiodes kunnen stralen met een lage penetratie in Si, zoals VUV/DUV en laag energetische elektronen waarvan de penetratie diepte maar enkele nm is, worden gedetecteerd met hoge efficiëntie. De sheetweerstand van de PureB laag zelf is hoog maar een metalen rooster kan daarop worden gedeponeerd om de serie weerstand te verminderen. Om de fotodiode capaciteit te verminderen kan het substraat worden bedekt met een dikke zeer laag-gedoteerd n-Si epitaxiale laag. Op deze manier was het mogelijk om lage RC waardes te bereiken die geschikt zijn voor hogesnelheid toepassingen.

Het gebruik van PureB fotodioden in avalanche-mode operatie werd bestudeerd in dit promotie werk. In eerst instantie door het doorslaggedrag te karakteriseren voor PureB diodes waar de anode was gefabriceerd op verschillende manieren. De anode vensters die geëtst werden door het oxide tot aan het silicium werden geopend op vier verschillende manieren: of volledig nat, met plasma etsen gevolgd door zacht- en/of nat-landen, of met plasma etsen van ongeveer 1 µm in het Si. De sperstroom was laag en de lekstroom werd grotendeels bepaald door de depletie van het oxidegrensgebied aan het rand van de diode. De resultaten steunen het beeld dat de PureB bedekking compleet is helemaal tot aan de rand. Dit bevorderde hoge doorslagspanning zelfs voor diodes zonder beschermringen of die met anode vensters die een stuk in de Si geëtst zijn. Desalniettemin werd het duidelijk dat een *p*-type beschermring een grote invloed had op de saturatie stroom van de dioden. Zij bewerkstelligden een ongeveer 2 decade reductie van het stroomniveau. Dit kon verklaard worden

als een gevolg van het beëindigen van de PureB bedekking aan de rand van de anode gebied.

Een belangrijke vraag die nodig beantwoord moest worden over het gedrag van PureB diodes betreft het mechanisme dat verantwoordelijk is voor de lage saturatie stromen. Teneinde een snelle methode te verkrijgen om de verschillende ladingsdrager stromen te evalueren in diodes geprocest onder verschillende depositie condities, werden laterale bipolaire teststructuren ontwikkeld zoals beschreven in Hoofdstuk 3. Vooral voor zeer ondiepe diodes kan het elektrische gedrag variëren van Schottky-achtig tot een hybride van Schottky and *p*-*n* junctie gedrag tot puur *p*-*n* junctie gedrag. Dit is afhankelijk van het niveau van *p*-doping aan het oppervlak van het *n*-type substraat tijdens depositie, of als er überhaupt *p*-doping is. Condities die zouden kunnen voeren tot elk van de drie typen diodegedrag werden bevestigd door device simulatie.

De laterale bipolaire teststructuren werden gebruikt in twee verschillende meetconfiguraties. De ene was de parallel-diode opstelling met drie naast elkaar liggend diodes die in parallel werken. Door de doorlaatkarakteristieken van de middelste diode te vergelijken met en zonder biasing van de nabij liggende diodes kan het diode type bepaald worden. Voor *p*-*n* junctie-achtig gedrag met hoge minderheidsladingsdragers injectie in het substraat is de stroom in de middelste diode verschillend in de twee situaties maar voor Schottky diodes domineert de thermionische emissie van de meerderheidsladingsdragers van het substraat en de stroom blijft hetzelfde. In de tweede opstelling zijn de drie nabij liggende diodes gebiased als een laterale transistor en van de gemeten basis en collector stromen kan de injectie van de minderheidsladingsdragers in de emitter en basis geëvalueerd worden. Hierdoor kan het gedrag van de emitter diode bepaald worden als zijnde of Schottky-achtig of *p*-*n* achtig. Uit het meten van deze teststructuren wordt geconcludeerd dat de diodes met een laagtemperatuur depositie van 400 °C *p*-*n*-junctie-achtig gedrag hebben dat vergelijkbaar is met hoog-temperatuur PureB diodes met een 700 °C depositie.

Gezien het niet te verwachten is dat de depositie van boor bij 400 °C kan leiden tot doteren van het bulk Si, werd de oorsprong van de hoge injectie van minderheidsladingsdragers van het PureB gebied naar het substraat ook gezocht door teststructuren te ontwikkelen voor het meten van de sheetweerstand langs de PureB-tot-Si grensvlak. Zoals besproken in Hoofdstuk 4 was het duidelijk van alle voorgaande experimenten dat een “schone” meting alleen maar bereikt

kon worden als alle invloed van de processing na de depositie zou worden vermeden. De nieuwe structuren maakten een meting van de sheetweerstand direct na de depositie mogelijk en waardes voor de lagen gedeponeerd bij 400 ℃ werden bepaald voor de eerste keer. Om zeker te zijn van de validiteit van de metingen werden twee verschillende typen teststructuren ontworpen en gefabriceerd. De meest nauwkeurige sheetweerstand wordt gevonden op basis van metingen van sets van ringvormige teststructuren maar dit is een omslachtige methode. Zij vormde een goede check van een andere zeer eenvoudige meting op basis van Van der Pauw teststructuren waar de sheetweerstand wordt bepaald van een stroom-spanningsmeting die snel over de wafer uitgevoerd kan worden. Betrouwbare resultaten werden behaald die lieten zien dat de sheetweerstand voor 400 ℃ depositie niet hoger was dan 35 kΩ/sq. Voor dezelfde tijd van blootstelling aan boor betekende een verlagen van de depositie temperatuur dat een hoger laterale sheetweerstand werd gevonden langs het PureB laag grensvlak. Bij 700 ℃ wordt de Si gedoteerd met boor tot een oplosbaarheid van $2x10^{19}$ cm^{-3} wat goed overeenkomt met de gemeten sheetweerstand van ~ 10 kΩ/sq. Deze dotering is zo hoog dat de sheetweerstand ongevoelig is voor de biasing van het substraat, in tegenstelling tot de 500 ℃ en 400 ℃ deposities voor welke de sheetweerstand behoorlijk stijgt met de substraat-biasing en ook voor een verhoging van de substraatdotering. Voor de 400 ℃ gedeponeerde PureB lag valt de sheetweerstand voor langere depositietijden en het stabiliseert wanneer een complete bedekking is bereikt. Dit komt overeen met de aanname dat geen bulk dotering plaats vindt. Op grond van alle resultaten wordt een simpel fysisch model voorgesteld voor de elektrische eigenschappen van het PureB-op-Si grensvlak: monolaag acceptortoestanden aan het grensvlak worden gevuld met elektronen waardoor een monolaag van vaste negatieve lading veroorzaakt het aantrekken van een monolaag van mobiele gaten. Naast het verklaren van het sheetweerstand gedrag van de 400 ℃ lagen geeft deze model ook een verklaring voor de zeer hoge Gummel getal van zowel de 400 ℃ als 700 ℃ lagen die geen van beide verklaard kunnen worden op basis van bulk Si dotering.

De Van der Pauw sheetweerstand teststructuur werd ook gebruikt om enkel processtappen na de PureB depositie te onderzoeken. In tegenstelling tot de 700 ℃ deposities was de laterale sheetweerstand van 400 ℃ en 500 ℃ PureB zeer gevoelig voor nabehandelingen wat aangeeft dat zij de perfectie van het oppervlakte verstoren. Bijvoorbeeld, de metaal schoonmaakstap was genoeg om

bijna alle PureB te verwijderen voor deze laag temperatuursdeposities en geen sheet weerstand kon bepaald worden. De sheetweerstand van 400 ℃ devices steeg behoorlijk na het verwijderen van het metaal terwijl bij de 500 ℃ de stijging marginaal was. Dit heeft te maken met de oppervlakte ruwheid hetgeen ook een teken is van een hoge dichtheid van pin-holes. Deze laten toe dat het gedeponeerde metaal het Si kan bereiken en dit verslechtert het PureB-Si grensvlak. In het algemeen wordt de niet-uniformiteit van de sheetweerstand van de net gedeponeerde PureB laag over de wafer hoger voor lagere depositie temperaturen. Dit is te verwachten gezien dat het een grensvlak eigenschap is en niet de resultaat van bulk doping zoals voor de 700 ℃ depositie.

Het bewezen applicatie gebied van PureB fotodiodes was verbreed door het ontwerp en de fabricage van zeer gevoelig, micrometer-grote SPADs die konden reageren op enkel fotonen en elektronen. In Hoofdstuk 5 worden de 'figures of merit' van SPADs gepresenteerd als voorbereiding voor een beschrijving van de fabricage proces voor de PureB devices. Deze kon werken in Geiger-mode waar de bias spanning een stuk boven de doorslagspanning wordt ingesteld. Om doorslag bij de anode rand te verhinderen werd een *n*-verrijkt gebied ge ïmplanteerd onder de PureB laag anode. Dit bepaalde de doorslagspanning en het actieve gebied. Een licht gedoteerde epitaxiale laag werd gebruikt om de elektrische veld te verminderen rond de rand en hoekpunten. De breedte van deze virtuele beschermring, dwz de afstand tussen de *n*-verrijkingsgebied en het dichtstbijzijnde anode venster, was met succes maar 0.5 μm lang gemaakt. De implantatie en anneal van het *n*-verrijkingsgebied was gekozen zodanig dat een onnodig hoge implantatie dosis vermeden kon worden. Dit kan anders resulteren in een lage en minder abrupt doorslagspanning en hogere 'dark counts'. Deze werden ook aanzienlijk verhoogd door het plasma etsen direct boven de PureB laag. Daarom werd dit vermeden tijdens het processen. Met deze voorzorgsmaatregelen konden PureB SPADs gefabriceerd worden met zeer lage lekstromen, minder dan 1 pA met een doorslag die zeer abrupt was. De devices hadden zeer lage dark count rate, zo laag als 5 Hz bij kamertemperatuur voor een device met een diameter van 4 μm.

In Hoofdstuk 6 wordt de optische karakterisatie van de gefabriceerde PureB SPADs gepresenteerd. De devices vertonen een goede selectiviteit voor UV light, met een maximum foton detectie waarschijnlijkheid van 11% bij een golflengte van 370 nm. De FWHM van 'timing jitter' was 436 ps voor een

'excess' bias van 4.5 V en dit verminderde voor een verhoging van de excess bias spanning. De 'after pulsing' probabiliteit was minder dan 1% en de doodtijd ongeveer 6 µs. De gefabriceerde PureB SPADs werden getest met lage energie elektronen. Zij vertoonden een hoog respons voor elektronen energieën zo laag als 200 eV en de experimenten duidden aan dat zij ook gevoelig zouden zijn tot minstens 100 eV.

In Hoofdstuk 7 worden PureGaB fotodiodes gepresenteerd. Deze werden ontwikkeld om de prestaties van de diodes, vooral die gemaakt bij 400 °C depositie, te verbeteren. Al werd het *p*-type grensvlak in dit geval gecreëerd door eerst Ga en dan B te deponeren was de sheetweerstand langs het grensvalk met de PureGaB vergelijkbaar met dat van een PureB grensvlak, mits de zelfde PureB depositie condities werden gebruikt. Desalniettemin, verzorgde de PureGaB laag een betere barrière tegen de Al metallisatie. Ook bleek de PureGaB fotodiodes even goed te fungeren als de PureB fotodiodes in termen van UV and laagenergie elektronen detectie. Dit is nog maar de begin stadium van het ontwikkelen van PureGaB fotodiodes en de algemene stabiliteit, ook VUV applicaties moeten nog grondig getest worden. Toch is het duidelijk dat zij grote potentie hebben, vooral als een laagtemperatuur CMOS-compatibel proces.

Acknowledgement

Finally, I am typing the last words of my dissertation. Life is bright, when I look back on my PhD life, it is so precious, unique and memorable. What I have received, learned and experienced is far more than what I ever could have imagined. Here I would like to take the opportunity to show my appreciation for all the people that I met during these years, thank you for being part of my life.

First, I would like to thank Prof. dr. Lis K. Nanver, you are a truly exceptional supervisor and mentor. And don't be surprised, I know what "K." stands for. Thank you for your inspiration, for offering the opportunity to do the research, for the great supervision, for the patient and substantial guidance, for the kind help in improving my technical skills, for your enthusiasm and devotion to science. And also thank you for the careful review of this dissertation.

As one of the few female professors in the scientific world, your achievements are already beyond gender boundaries. It always amazed me that you have this unique instinct to reveal the facts behind the phenomena when it comes to science. I enjoy working with you. It was so great that I had the opportunity to benefit from your "open door policy", which was a very efficient way to solve daily issues, I could always go get directions and some inspiration. Thank you for the opportunities offered by conferences and workshops to get in contact with other experts in the world, talk to them, getting insights that I could never learn from just reading a scientific paper. Also, thanks for all those delicious dinners and sorry I may not have left enough for others. What's more important, I can be glad in most cases when facing difficult choices, I know how to make choice I know is right rather than the easy one. This cannot be achieved without a mentor of integrity.

I would like to thank Prof. Kees Beenakker, Prof. Lina Sarro and Dr. Ryoichi Ishihara, thank you for your work and support to Dimes, it was a great place to work, a world-class research institute allowing us to convert our ideas from paper into reality.

All the members of the Dimes IC-processing group, thank you for your patient, support and assistance: Alex van den Bogaard, Cassan Visser, Charles de Boer, Dr. Gregory Pandraud, Dr. Henk van Zeijl, Jan Cornelis Wolff, Jan Groeneweg, Johannes van Wingerden, Mario Laros, Ruud Klerks, Wim Wien, Wim van der Vlist and the Facility Four: Joost Berendse, Robert Verhoeven, Ron van Viersen and Jan Warmerdam.

Furthermore, I owe very special thanks to Silvana Milosavljevic for the safety course and cleanroom training; Hugo Schellevis for the sputter coating; Johan van der Cingel for the AFM; Koos van Hartingsveldt for the implantations; Loek Steenweg for the dicing and wire bonding; Peter Swart for the support in the measurement room; Wiebe de Boer for the great work on the Epsilon; Tom Scholtes, for almost everything; and Bert Goudena, for all the support, for the Dutch translation and for the wonderful trip in China.

Many thanks to Rosario Salazar Lozano, Bianca Knot, Marysia Lagendijk-Korzeniewski and Marian Roozenburg, thank you for your support and administrative tasks.

I would like to thank Prof. Edoardo Charbon, Dr. Mahdi Aminian and Dr. Shingo Mandai from TU Delft; Prof. Tomislav Suligoj and Tihomir Knezevic from University of Zagreb; Dr. Gerard van Veen, Dr. Seyno Sluyterman and Kees Kooijman from FEI. Thank you all for the advice, support, cooperation and inspiration, thank you for being such great research partners.

My dear colleagues and friends from the Silicon Device Integration group, it was such a great time to work with you and I was so lucky to know you all. Dr. Amir Sammak, you are a great office mate, thanks for the help in the work and all the fun during our spare time and many trips; Dr. Agata Sakic, how you are becoming an even more beautiful person these years; Dr. Caroline Mok, we have to get together more often and discover more good Chinese food. Also I would like to thank Dr. Ramses van der Toorn, Daniel Vidal, Dr. Francesco Vitale, Dr. Jaber Derakhshandeh, Dr. Milos Popadic, Dr. Lei Gu, Robert Setekera, Dr. Vladimir Milovanovic, Dr. Vladimir Jovanovic, we were such a great group, this would never have been achievable without you.

My appreciation to my colleagues: Dr. Aslihan Arslan, Aleksandar Jovic, Dr. Benjamin Mimoun, Dr. Bruno Morana, Dr. Chenggang Shen, Cinzia Silvestri, Dr. Fabio Santagata, Dr. Gianpaolo Lorito, Dr. Giuseppe Fiorentino, Dr. Hugo Perez Garza, Dr. Luigi Mele, Dr. Marko Mihailovic, Miki Trifunovic,

Dr. Negin Golshani, Dr. Vahid Mohammadi, Dr. Sten Vollebregt, Rene Poelma, Ronald Stoute, Dr. Sima Tarashioon and Dr. Thomas Moh. It was my pleasure to work with you brilliant people. Thank you for your help and support in these years.

How can I forget my dear Chinese friends: Bing Liu, Dr. Bo Han, Cheng Ma, Guangjun Lv, Dr. Huaiyu Ye, Dr. Jiaqi Tang, Jin Zhang, Dr. Jing Zhang and Pan Liu, Dr. Meng Nie, Pengfei Sun, Ronghui Zhang, Xin Guo, Xingyu Liu, Xueming Li, Yuanxing Xu. Thank you for the support, for the inspiration, for the delicious food, for the parties, for the company, and for the happy memories.

I would like to thank all my friends from all around the world, you have the magic to turn a strange city into a lovely place. The distance only bonds us even closer, the friendship is invaluable.

Finally, I would like to reserve the last piece to my family. Hang Yu, my beautiful and lovely wife, thank you for your love, understanding, encouragement, patient and support. Life is a journey, you are the perfect companion. And last but not least. I would like to thank my parents and my in-laws, for the confidence, dedication and support, they have always been a source of inspiration and encouragement.

List of Publications

Journals:

1. **L. Qi** and L. K. Nanver, "Conductance along the Interface Formed by 400°C Pure Boron Deposition on Silicon," *IEEE Electron Device Letters*, vol. 36, issue 2, pp. 102-104, Feb. 2015.
2. **Lin Qi**, S. Sluyterman, K. Kooijman, K.R.C. Mok and Lis K. Nanver, "PureB Single-Photon Avalanche Diodes for Low-Energy Electron Detection Down to 200 eV," *Optics Letters*, vol. 40, issue 3, pp. 300-303, Feb. 2015.
3. **Lin Qi**, K. R. C. Mok, Mahdi Aminian, Edoardo Charbon and Lis. K. Nanver, "UV-Sensitive Low Dark-Count PureB Single-Photon Avalanche Diode," *IEEE Transactions on Electron Devices*, vol. 61, issue 11, pp. 3768-3774, Nov. 2014.
4. **L. Qi**, G. Lorito, L.K. Nanver, "Lateral-Transistor Test Structures for Evaluating the Effectiveness of Surface Doping Techniques", *IEEE Transactions on Semiconductor Manufacturing*, vol. 25, no. 4, pp. 581-588, Nov. 2012.
5. A. Smmak, **L. Qi**, L.K. Nanver, "Restricted-Access Al-Mediated Material Transport in Al Contacting of PureGaB Ge-on-Si p^+n Diodes," *Journal of Electronic Materials*, vol. 44, issue 12, pp. 4676-4683, Dec. 2015.
6. K.R.C. Mok, **L. Qi**, A.H.G. Vlooswijk, L.K. Nanver, "Self-aligned two-layer metallization with low series resistance for litho-less contacting of large-area photodiodes," *Solid-State Electronics*, vol. 111, pp. 210-217, Sept. 2015.
7. S. Dutta, R.J.E. Hueting, A.J. Annema, **L. Qi**, L.K. Nanver, J. Schmitz, "Opto-electronic modeling of light emission from avalanche-mode silicon p^+n junctions, " *Journal of Applied Physics*, vol. 118, issue 11, p. 114506, Sept. 2015.

8. Lis K. Nanver, **Lin Qi**, Vahid Mohammadi, K.R.M. Mok, Wiebe B. de Boer, Negin Golshani, Amir Sammak, Thomas L.M. Scholtes, Alexander Gottwald, Udo Kroth, and Frank Scholze, "Robust UV/VUV/EUV PureB Photodiode Detector Technology with High CMOS Compatibility," *Journal of Selected Topics in Quantum Electronics*, vol. 20, issue 6, pp. 1-11, Nov. 2014.
9. V. Mohammadi, **L. Qi**, N. Golshani, K. R. C. Mok, W. B. de Boer, A. Sammak, J. Derakhshandeh, J. van der Cingel, L. K. Nanver, "VUV/Low-Energy-Electron Si Photodiodes with Post-Metal 400°C PureB Deposition," *IEEE Electron Device Letters*, vol. 34, issue 12, pp. 1545-1547, Dec. 2013.
10. A. Sammak, **L. Qi,** W. B. de Boer and L. K. Nanver, "PureGaB p^+n Ge Diodes Grown in Large Windows to Si with a Sub-300 nm Transition Region," *Journal of Solid-State Electronics,* vol. 74, no. 1, pp. 126-133, Aug. 2012.

Conferences:

1. **Lin Qi** and Lis K. Nanver, "Sheet Resistance Measurement for Process Monitoring of 400 ℃ PureB Deposition on Si", *28th IEEE International Conference on Microelectronic Test Structures (ICMTS 2015)*, Phoenix, Arizona, USA, Mar. 2015, pp. 169-174.
2. **L. Qi**, L.K. Nanver, "Fabrication of PureB-Only Light-Entrance Windows for VUV Sensitive Single-Photon Avalanche Diodes," *12th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT 2014)*, Guilin, China, Oct. 2014, pp. 855-857.
3. **Lin Qi**, K. R. C. Mok, Mahdi Aminian, Edoardo Charbon and Lis K. Nanver, "Fabrication of Low Dark-Count PureB Single-Photon Avalanche Diodes," in *Proceedings of SBMicro 2014*, Aracaju, Brazil, 1-5 Sept. 2014, pp. 1-4.
4. **Lin Qi**, Vahid Mohammadi, K.R.M. Mok, Alexander Gottwald, Udo Kroth, Frank Scholze and Lis K. Nanver, "CMOS Compatible PureB Technology for Robust UV/VUV/EUV Photodiode Detectors and Imagers," *Book of abstracts Tipp 2014*, Amsterdam, the Netherlands, Jun. 2014, p.163.

5. **Lin Qi**, K. R. C. Mok, Mahdi Aminian, Edoardo Charbon and Lis. K. Nanver, “UV-Sensitive Low Dark-Count PureB Single-Photon Avalanche Diode,” *IEEE-Sensors 2013 Proceedings*, Baltimore, USA, Nov. 2013, pp. 1883-1886.

6. **Lin Qi**, K. R. C. Mok, Mahdi Aminian, Tom L.M. Scholtes, Edoardo Charbon and Lis K. Nanver, “Reverse Biasing and Breakdown Behavior of PureB Diodes,” *13th International Workshop on Junction Technology (IWJT 2013)*, Kyoto, Japan, 6-7 Jun. 2013, pp. 70-73.

7. L.K. Nanver, **L. Qi**, A. Sammak, K. R. C. Mok, M. Aminian, E. Charbon, “Towards CMOS-Compatible Photon-Counting Imagers in the Whole 10 nm - 1600 nm Spectral Range with PureB Si and PureGaB Ge-on-Si Technology,” *12th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT 2014)*, Guilin, China, Oct. 2014, pp. 644-647.

8. A. Sammak, M. Aminian, **L. Qi**, W.B. de Boer, E. Charbon, L.K. Nanver, “Fabrication of Pure-GaB Ge-on-Si Photodiodes for Well-Controlled 100-pA-Level Dark Currents,” *ECS Transactions*, vol. 64, issue 6, pp. 737-745, 2014.

9. A. Sammak, M. Aminian, **L. Qi**, E. Charbon, L. K. Nanver, “A 270×1 Ge-on-Si Photodetector Array for Sensitive Infrared Imaging,” in *Proceedings of SPIE*, vol. 9141, Optical Sensing and Detection III, Brussels, Belgium, Apr. 2014.

10. L.K. Nanver, A. Šakic, V. Mohammadi, J. Derakhshandeh, K.R.C. Mok, **L. Qi**, N. Golshani, T.M.L. Scholtes, W.B. de Boer, "Applications of PureB and PureGaB Ultrashallow Junction Technologies," *11th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT 2012)*, Xi'an, China, Oct. 29 - Nov. 1 2012, pp. 303-306.

11. Mahdi Aminian, Amir Sammak, **Lin Qi**, Lis K. Nanver, Edoardo Charbon. "A Ge-on-Si Single-Photon Avalanche Diode Operating in Geiger Mode at Infrared Wavelengths," in *Proceedings of SPIE*, vol. 8375, p. 83750Q. 2012.

12. Agata Sakic, **Lin Qi**, Tom LM Scholtes, Johan van der Cingel, and Lis K. Nanver. "Epitaxial Growth of Large-Area p^+n Diodes at 400 ℃ by Aluminum-Induced Crystallization," in *Proceedings of IEEE European*

Solid-State Device Research Conference (ESSDERC 2012), Aug. 2012, pp. 145-148.

13. L.K. Nanver, A. Sammak, V. Mohammadi, K.R.C. Mok, **L. Qi**, A. Sakic, N. Golshani, J. Derakhshandeh, T.M.L. Scholtes, W.D. de Boer, "Pure Dopant Deposition of B and Ga for Ultrashallow Junctions in Si-Based Devices," *ECS Transactions 2012*, vol. 49, no. 1, 27th Symposium on Microelectronics Technology and Devices (SBMicro2012), Brazil, Bras ília, Sept. 2012, pp. 25-33.
14. A. Sammak, M. Aminian, **L. Qi**, W.B. de Boer, E. Charbon, L.K. Nanver, "A CMOS Compatible Ge-on-Si APD Operating in Proportional and Geiger Modes at Infrared Wavelengths," in *Proceedings of International Electron Device Meeting (IEDM 2011)*, Washington DC, USA, Dec. 2011, pp. 8.5.1 - 8.5.4
15. A. Sammak, W.B. de Boer, **L. Qi**, L.K. Nanver, "High-Quality p^+n Ge Diodes Selectively Grown on Si with a Sub-300nm Transition Region," in *Proceedings of European Solid-State Device Research Conference (ESSDERC 2011)*, Helsinki, Finland, Sept. 2011, pp. 359-362.
16. G. Lorito, **L. Qi,** L.K. Nanver, "Lateral Bipolar Structures for Evaluating the Effectiveness of Surface Doping Techniques", in *Proceedings of IEEE International Conference on Microelectronic Test Structures (ICMTS 2011)*, Amsterdam, the Netherlands, Apr. 2011, pp.108-113.
17. G. Lorito, **L. Qi**, L.K. Nanver, "Arbitrarily Shallow Arsenic-Deposited Junctions on Silicon Tuned by Excimer Laser Annealing," *10th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT 2010)*, Shanghai, China, Oct. 2010, pp. 972-974.
18. A. Sammak, **L. Qi**, W.B. de Boer, L.K. Nanver, "Chemical Vapor Deposition of Ga Dopants for Fabricating Ultrashallow pn Junctions at 400 ℃," *10th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT 2010)*, Shanghai, China, Oct. 2010, pp. 969-971

Workshops:

1. **L. Qi,** G. Lorito, L.K. Nanver, "Simple Method to Evaluate Minority Carrier Injection Levels in Schottky Diodes," in *Proceedings of ICT.OPEN: Micro technology and micro devices (SAFE 2011)*, Veldhoven, the Netherlands, Nov. 2011, pp. 1-3.
2. A. Sammak, W.B. de Boer, **L. Qi**, L.K. Nanver, "Large-Area Selective CVD Epitaxial Growth of Ge on Si Substrates," in *Proceedings of ICT.OPEN: Micro technology and micro devices (SAFE 2011)*, Veldhoven, the Netherlands, Nov. 2011, pp. 1-4.
3. A. Sammak, W.B. de Boer, L.K. Nanver, **L. Qi**, G. Lorito, "Chemical Vapor Deposition of Gallium on Silicon and SiO_2," in *Proceedings of SAFE 2009*, Veldhoven, the Netherlands, Nov. 2009, pp. 538-541.

About the Author

Lin Qi was born in Changchun, China, in 1985. He received his Bachelor of Science degree in microelectronics from Jilin University in 2008, and his M.Sc. degree in electrical engineering from Delft University of Technology, The Netherlands, in 2010. Having completed his master's thesis with the Laboratory of Electronic Components, Technology and Materials (ECTM) at Department of Microelectronics, he continued his research in Jan 2011 as a Ph.D. student in the Silicon Device Integration Group. His research interests include design, fabrication and electrical analysis of silicon devices, in particular high-sensitivity silicon photodiodes such as single-photon avalanche diodes (SPAD). In 2011, he entered the Huygens Scholarship Programme sponsored by the Dutch government.

In June 2015, he joined the transaction security division of Underwriter's Laboratory (UL), as a technical advisor.