A Highly-Linear Low-Power Down-Conversion Receiver for Digital Transmitter's Error Detection

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Supervised By: prof.dr. L.C.N. de Vreede

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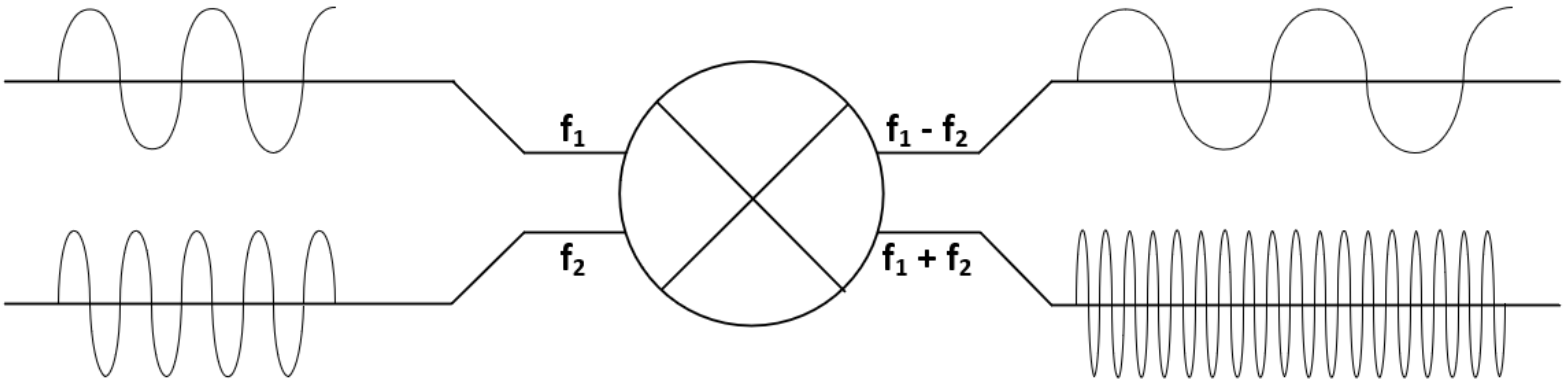

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A Highly-Linear Low-Power Down-Conversion Receiver for Digital Transmitters' Error Detection

by

Tariq Aziz

In partial fulfilment of the requirements to obtain the degree of

Master of Science in Electrical Engineering

at Delft University of Technology

August 31st, 2022

Student Number:	5259517	
Project Duration:	October 7, 2021 – August 31, 2022	
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ACKNOWLEDGEMENTS

The road to knowledge is long and full of obstacles, but it is exactly going over those obstacles that ultimately enlightens the individual and strengthens his spirit. I have been very fortunate to be given the opportunity to take the first steps in this road of knowledge, not alone, but accompanied by the warm-hearted support of my family. I revere the patronage and moral support extended with love, by my parents whose continuous passionate encouragement made it possible for me to excel in my MSc pursuit.

I would like to express my sincerest gratitude to my thesis supervisor prof. Leonardus de Vreede, whose technical insight and willingness to help and teach have played the most crucial role in the course of development of this thesis project. His commitment for being available and providing support throughout every step of this thesis project; despite his busy schedule, is the main foundation upon which this work was built upon.

On the same note, I also want to express my appreciation for dr. Morteza Alavi for his critical feedback throughout different stages of this thesis project that helped iron out which aspects needed improvement. Furthermore, his educational material related to mixers in the MSc courses he tutors were extremely useful throughout the devising of this thesis project.

I would like to acknowledge Rob Bootsman and Mohammad Reza Beikmirza, for providing me with a custom I/O pad and a clock-generator respectively. Their input helped fast-track the design portion of this thesis work.

My gratitude extends to Ampleon as well, for their funding of the whole duration of this thesis work. Without their financial support, I would not have been able to focus solely on this thesis work.

Finally, I would like to express my deep appreciation for the Justus and Louis van Effen foundation, for providing me with a full scholarship covering my education period at TU Delft. Without the financial stability they provided, I would not have had the opportunity to pursue my MSc degree here.

ABSTRACT

Wireless data traffic is projected to steadily increase in the near future, necessitating the demand for transceivers with higher linearity and efficiency. Digital power amplifiers have the potential to achieve these higher efficiency demands while digital pre-distortion can be used to improve their linearity. Digital pre-distortion requires a highly-linear wideband observation receiver to down-convert and monitor the output of the transmitter. An observation receiver architecture that relies on baseband error-detection has been previously proposed by ELCA to reduce the stringent requirements on the analog-to-digital converter (ADC) in such an observation receiver. This thesis work presents a novel extremely-linear wideband voltage-domain harmonic-reject mixer targeting these observation receiver applications. The choice for a voltage-domain mixer instead of a current-domain mixer is first discussed. Three novel voltage-domain mixer topologies are then evaluated for their advantages and disadvantages, yielding the preferred topology for implementation. This circuit was designed in TSMC40nm thin-oxide CMOS technology yielding promising performance metrics when compared to similar state-of-the-art publications in the open literature; specifically in domain of observation receiver applications.

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1 INTRODUCTION

1.1 WIRELESS DATA TRANSFER TRENDS

The world we live in today is a deeply interconnected one. Already a multitude of critical daily services for any individual in society depends on some form of data transfer between different communicating nodes (e.g., Internet, Mobile, Banking, Education, Medical Databases, etc...). This interconnection dependence is projected to steadily increase in the foreseeable future, and since data transfer is the backbone functionality of any communication network, it is projected to increase as well.

Wireless data transfer in particular has gained wide popularity in the last decade with the advancement of both high data-rate communication standards and RF compatible hardware technologies. This resulted in a steady increase in mobile data transfer every year. In a study by Ericson [1]-[2] related to mobile data traffic, it was found that this trend is projected to not only continue, but also to accelerate in the next decade, this is visualized in Fig. 1.1 and Fig. 1.2.

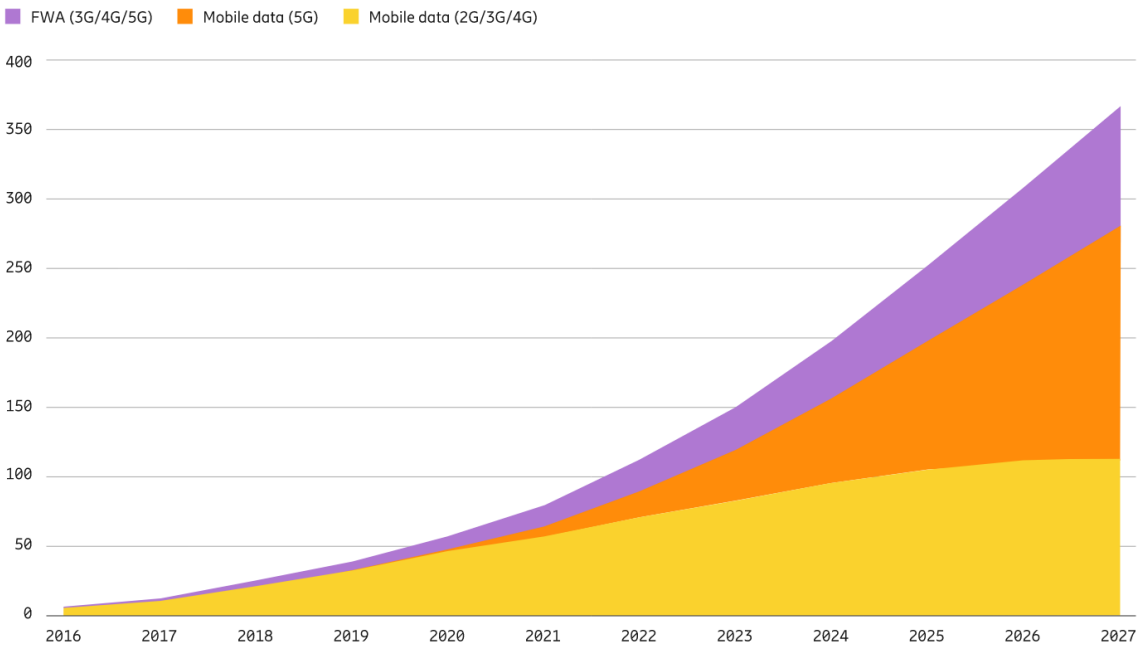

Figure 1.1: Global Annual Mobile Data Traffic (Exabyte/Month) [1]

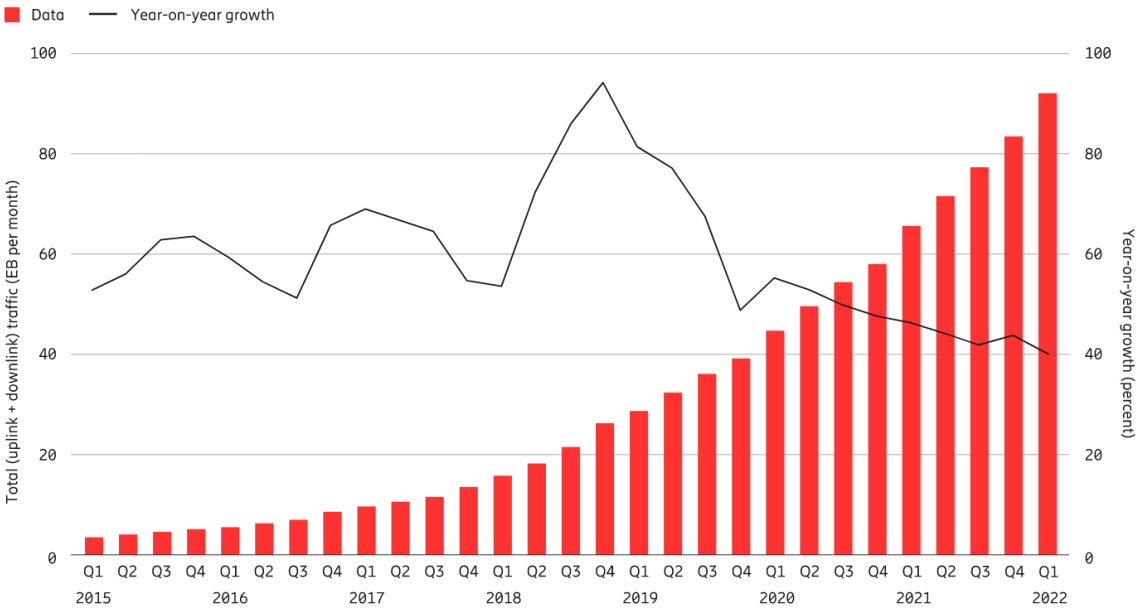

Figure 1.2: Global Quarterly Mobile Data Traffic and year-on-year Growth (Exabyte/Month) [2]

An increase in global data traffic translates into a demand for higher data-rate mobile communication standards. The fifth-generation of cellular networks (5G), aim to satisfy these demands using various techniques. Firstly, 5G aims to improve spectral efficiency by using higher-order data modulation schemes. Higher-order data modulation schemes involves coding more bits into a single symbol, this translates into smaller separations between the individual symbols in the constellation diagram, yielding higher requirements on linearity. Secondly, 5G aims to use larger signal bandwidths by shifting to higher-frequency carriers where more bandwidth is available. Higher-frequency carriers fade more quickly in the environment, especially when no line of sight between the transmitter and the receiver is available, necessitating the need for more communication nodes, yielding smaller wireless cells to sustain coverage. However, these smaller cells also allow for frequency re-use, again contributing to a higher data capacity. Thirdly, 5G aims to make use of beamforming, a method of increasing the antenna gain in a certain direction by coherent operation of multiple receivers and transmitters. Consequently, beamforming requires many transmitters and receivers as can be seen in Fig. 1.3.

In general, higher-modulation data schemes and higher bandwidths yield lower transmitter efficiency, increasing the demand for more energy efficient transmitters than currently provided by the conventional analog solutions. Digital transmitters have the

potential to provide high efficiency and higher bandwidths at higher integration and lower cost, facilitating future cost-effective implementations of 5G networks.

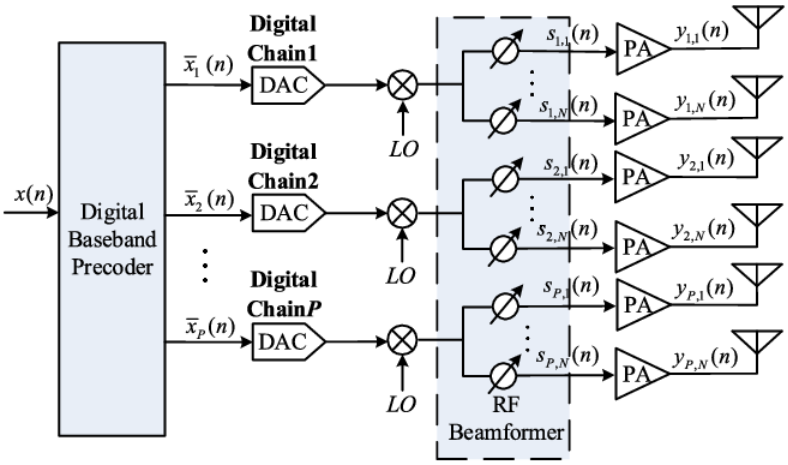

Figure 1.3: Transmitter Array Example using Analog Beamforming [3]

1.2 DIGITAL POWER AMPLIFIERS

The dominant consumer of power in any transmitter chain is the power amplifier. Analog power amplifiers with a fixed voltage supply; omitting any efficiency enhancement techniques, have an efficiency vs. output power roll-off that is visualized in a simplified form in Fig. 1.4. It is clear that the highest efficiency is only achievable at maximum output power. To conform to linearity requirements enforced by different communication standards, analog power amplifiers typically need to operate lower than their maximum output power, this is known as power backoff. Power backoff decreases the efficiency of power amplifiers. The strict linearity requirements of 5G enforces the use of even more power backoff lowering the efficiency even more.

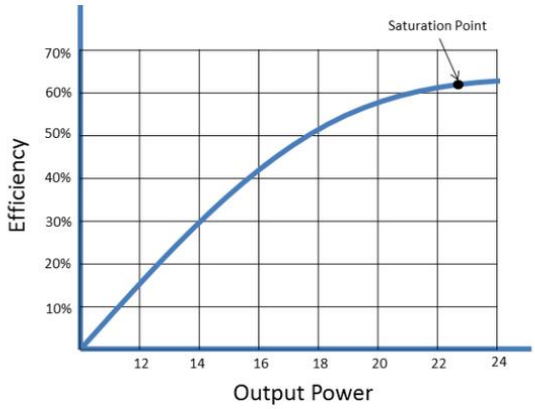

Figure 1.4: Efficiency vs. Output Power of Typical Class AB Amplifier [4]

The cause for this efficiency vs. output power back-off roll-off in a conventional power amplifier is that when the output power is reduced, the output stage is not effectively utilizing the full voltage swing set by its supply voltage. The remaining voltage headroom causes a DC voltage over the output stage which in combination with output current is dissipated and converted to heat.

Digital power amplifiers aim to improve the efficiency of transmitters. In an ideal switching digital power amplifier there is no overlap between the drain voltage and the drain current on the switching device at maximum output power, allowing for an ideal efficiency where all the power is transferred to the load. Of course, in a real digital power amplifier, the switching device is not an ideal switch, and there will still be some power consumed reducing the ideal efficiency, but this still provides better efficiency than in analog counterparts. In a conventional switching digital power amplifier, there is no direct way to control its output power, and consequently the amplitude of the output RF signal. There are different techniques to achieve output power control, e.g., g_m-scaled unit current sources can be used to set the output level. These still exhibit some form of efficiency vs. output power back-off roll-off. However, due to duty-cycle reduction, digital power amplifier's peak efficiency can be significantly improved compared to their analog counterparts. When combined with an efficiency enhancement technique like Doherty configurations, the average efficiency can further be improved. Digital power amplifiers directly benefit from the downscaling of CMOS technologies. In handsets, digital power amplifiers have already been realized [5]. However, in high-power base station applications, custom technologies such as LDMOS are required to realize the high RF output power, this complicates the design of a complete transmitter on the same chip.

Today's high-power base stations still employ analog power amplifiers, accompanied by high static power dissipation and low integration. An illustration of a conventional analog cartesian transmitter line-up is shown in Fig. 1.5a. The important thing to note here is that the point of conversion from digital to analog is in the baseband domain. Usually, the digital-to-analog converter (DAC), upconverter, and PA are on separate IC's, taking extra area and requiring interface circuitry. An analog PA is basically always "on", resulting in a relatively high static power dissipation due to its quiescent currents.

The ELCA group, together with its industry partners, specifically Ampleon and Nokia, are working towards integrating a complete digital transmitter for base-station applications that incorporates both LDMOS and CMOS IC's. A simplified schematic of a cartesian digital transmitter (DTX or RFDAC) is shown in Fig. 1.5b. As can be seen, the input bits are individually fed to an upconverter, implemented by an AND gate. The AND gates drive current sources that are implemented in a high-power LDMOS technology.

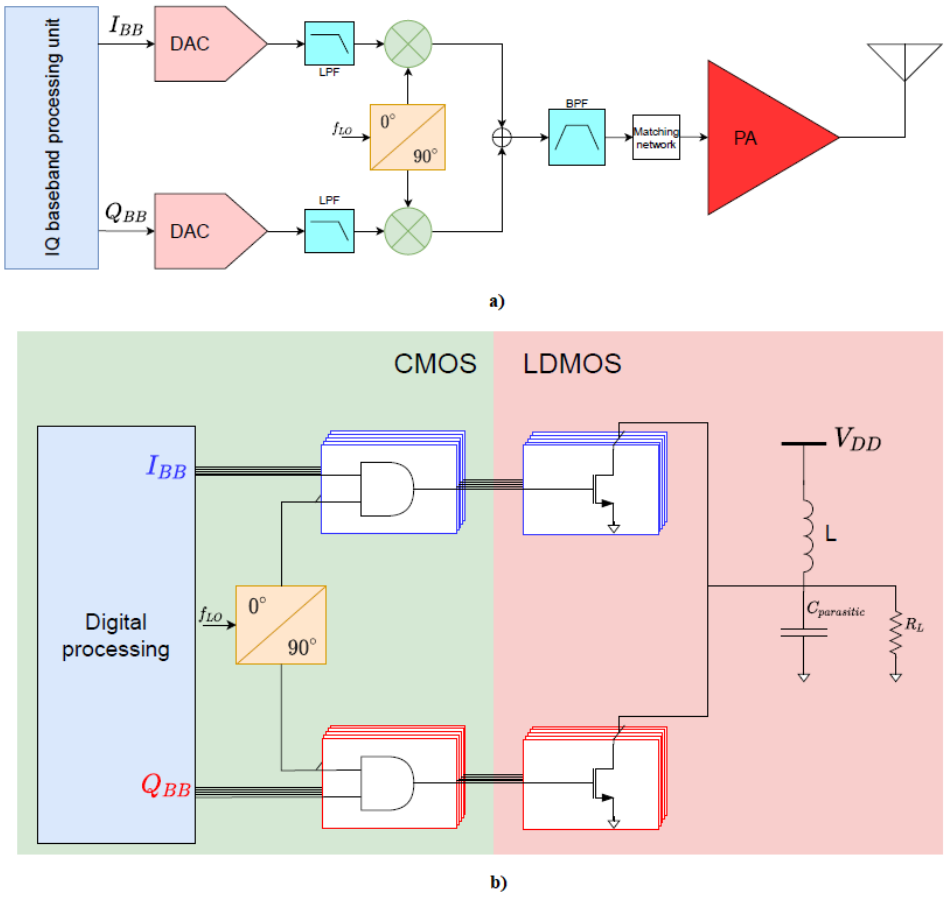

Figure 1.5: a) Conventional Analog Cartesian Transmitter – b) Proposed Digital Transmitter (DTX or RFDAC)

An important difference with the conventional topology is that the point of conversion from digital to analog is in the RF domain. In an analog power amplifier, the input voltage sets the output current through the g_m of the power device. In the proposed digital g_m-scaling power amplifier, the output power is set by the number of current sources that are switched on. This output current is converted to a voltage by the loading network. Compared to the conventional analog power amplifier, one source of non-

linearity is eliminated, namely the non-linear I_D-V_{GS} characteristic of a trans-conductance. In a digital g_m-scaling power amplifier, the mismatch between the current unit cells and their finite output impedance limits the linearity, while the number of unit current cells sets the resolution. The non-linearity caused by mismatch can be reduced by using unary bits. However, every unary bit needs its driver circuit and interconnect; increasing its power consumption, so a trade-off has to be made. The non-linearity from the finite code-dependant output conductance can be reduced by designing the parallel combination of the output impedance of each current steering cell to be much larger than the load resistor.

Another source of non-linearity stems from the fact that a digital power amplifier is driven by squarer waves, this results in a lot of harmonics specially at odd harmonics. Fig. 1.6 shows a simplified estimation of the resulting harmonics around our desired signal bandwidth of 400 MHz. In this work, our signal of interest is situated around a carrier of 3.5 GHz; a band that is employed by sub-6 GHz 5G, the third and fifth harmonics are showed at 10.5 GHz and 17.5 GHz respectively. The transmitter has an aimed linearity of 50dB, meaning that the intermodulation components must be 50dB below the signal of interest. The linearity specification is based on the 3GPP for documentation for LTE that gives a minimum Adjacent channel-leakage-ratio (ACLR) of -45dBc [6].

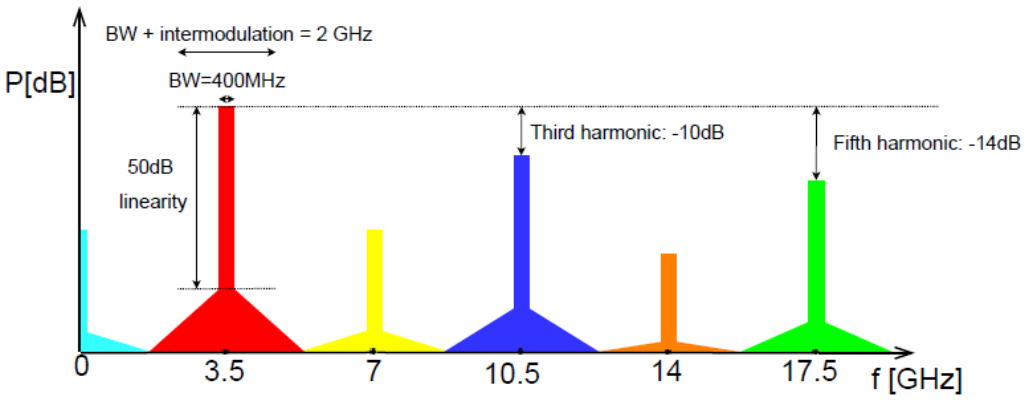

Figure 1.6: Simplified Output Spectrum of Digital Transmitter (RFDAC)

The digital power amplifier has an RLC output network. The inductor at the output sets the DC level and resonates out the parasitic output capacitance. The output capacitance

can be estimated from the required peak output power and the capacitance per watt RF power of the technology used.

The output network will bandpass filter the output. This additional filtering of the harmonic frequencies can be estimated using a simple simulation. The result of the parallel RLC network simulation shows a filtering of around 17dB at 10.5 GHz (being the 3rd harmonic of the aimed for 3.5GHz TX carrier frequency). Combined with the fact that the third harmonic of a square wave is about 10dB weaker than its fundamental, the signal content at 10.5 GHz is expected to be about 25-27dB weaker than the content at 3.5 GHz.

The digital transmitter system that is currently in development at ELCA aims to use a flip-chip approach to mount the CMOS-chip directly on top of the LDMOS chip. An artist illustration of the approach is shown in Fig. 1.7. Such an interface will have fewer parasitics due to the elimination of bond wires between the CMOS controller and the LDMOS mimic while offering an increased number of interconnections that will allow more unary bits. This flip-chip approach brings the complete integration of the transmitter much closer to reality.

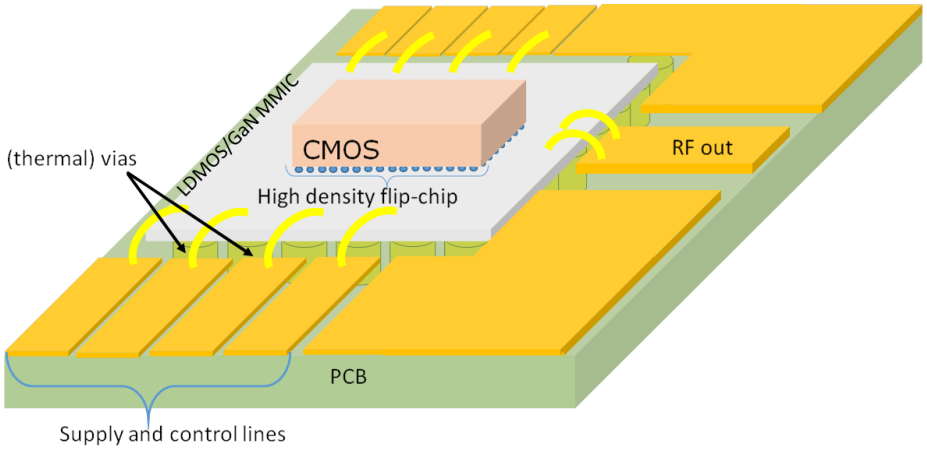

Figure 1.7: Artist Demonstration of aimed Flip-chip Approach

1.3 DIGITAL PRE-DISTORTION

For digital power amplifiers, the compression in their output stage also presents a linearity vs. efficiency trade-off. Digital pre-distortion can be used break this trade-off by compensating for these non-linearities in the digital domain.

The basic idea behind digital pre-distortion, is if the power amplifier has a certain non-linear input-to-output characteristic, then the inverse characteristic is applied to the digital baseband data to compensate for the non-linearity of the power amplifier, resulting in linear operation. This is visualized in Fig. 1.8.

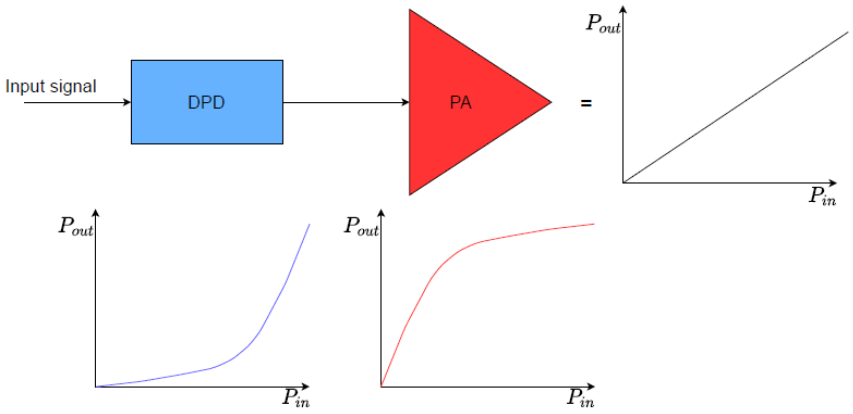

Figure 1.8: Simple Pre-distortion System

The DPD could in principle use a model based on a complete characterization of the PA under all possible conditions, but in reality, a more practical solution is using an observation loop. By comparing the down-converted transmitter output signal with the actual input signal, the DPD unit adjusts the transfer function until the output of the PA meets the linearity specifications. A transmitter setup including such a DPD is shown in Fig. 1.9.

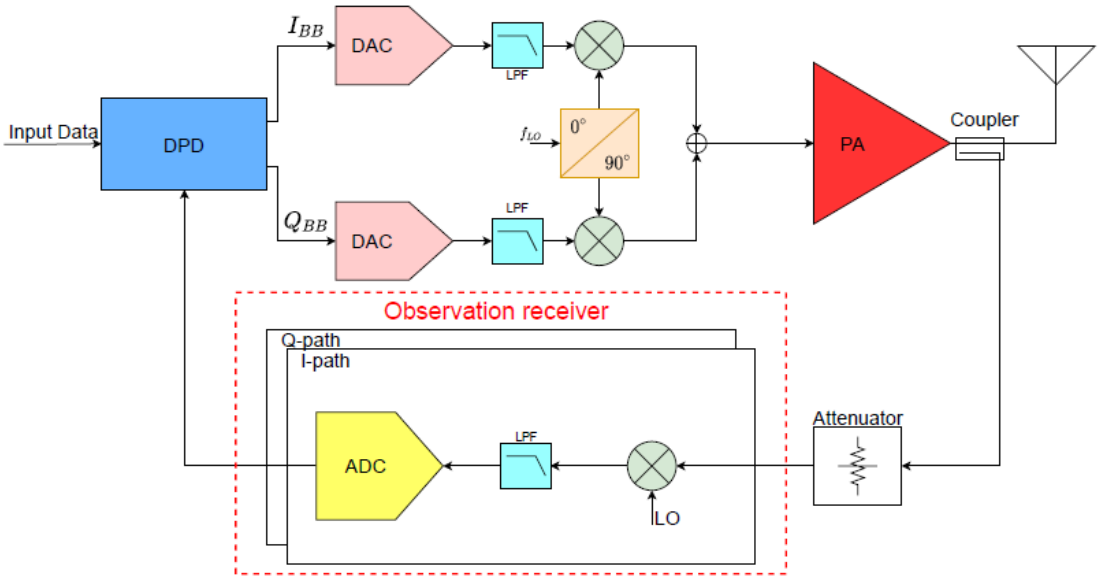

Figure 1.9: Typical DPD Transmitter Line-Up including a Simple Observation Receiver

1.4 OBSERVATION RECEIVER

A thorough comparison between different observation receiver architectures has been presented by Gilbert Hardeman at ELCA in [7], where the cons and pros of each was discussed. This thesis work follows from that research and hence is concerned with the correction loop architecture proposed in [7], which is given in Fig. 1.10.

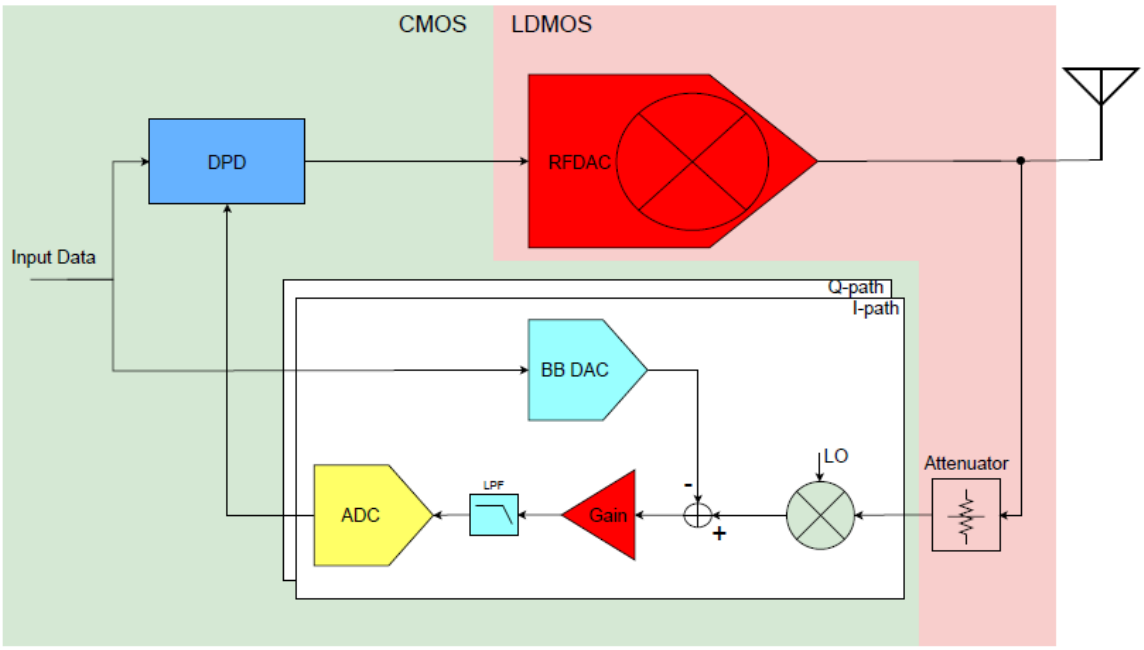

Figure 1.10: Proposed Observation Receiver with Error Measurement [7]

The main advantages of this architecture can be summarized as following:

- Employs direct TX error detection instead of TX signal monitoring. This approach significantly reduces the dynamic range requirements of the ADC to only 35 dB. An ADC bandwidth of 1GHz is still required for down-converting the output spectrum of a wideband RFDAC.

- Error measurement (signal subtraction) is done in baseband instead of at RF such that the reference DAC can be a baseband DAC. This reduces its power consumption, as well as makes it more linear. Furthermore, the error measurement (signal subtraction) enforces very stringent timing requirements in the range of 20 fS if it would be performed at RF which is not practical. Performing this action in baseband relaxes the timing requirements to around 400 fS.

- The required ACPR for the RFDAC to comply with the wireless standards is 50 dBc. In this work, the aimed ACPR linearity for the RFDAC was chosen 60 dBc (at maximum power) to leave some margin for fabrication non-linearities. This means that the aimed linearity of the observation receiver should at least be 65 dBc in order not to corrupt the linearity information coming from the RFDAC.

- Having the down-conversion mixer at the beginning of the correction loop forces the mixer to have the same linearity requirements as the whole observation receiver. Furthermore, it needs to have a harmonic rejection ratio of at least 40 dB to suppress the 3rd harmonic of the RFDAC output below 65 dBc after down-conversion, the remaining 25 dB of rejection results from the RFDAC's RLC output matching network as well as the implicit square wave attenuation of harmonics.

The aimed RFDAC has an average output power in the range of 5W. The observation receiver, in its future implementation, is targeted to not lower the system efficiency by more than 5%, this allocates a total of 250 mW for the observation receiver's power consumption. Due to the dynamic range reduction in the proposed error measurement observation receiver, an ADC with the required dynamic range and bandwidth consumes only around 20 mW of power [8]. Current DPD engines consume power within the range of 1W [9], the long-term goal for the DPD engines to be developed within ELCA with custom integration techniques is to consume power in the range of 0.1W. The mixer's power consumption should not exceed 50% of the DPD engine's power budget; thus, consuming a total of 50 mW. The remainder of the power budget is allocated to the baseband DAC. Fig. 1.11 presents the estimated power budget breakdown of the whole observation receiver.

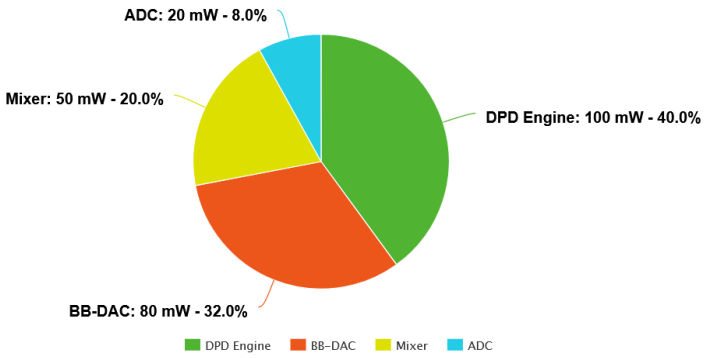

Figure 1.11: Observation Receiver Estimated Power Consumption Breakdown

The ADC succeeding the mixer is expected to have an input capacitance of ~250 pF and operates with a $1V_{FS}$. For maximum SNR output from the ADC, we would want the mixer to ideally be able to drive this capacitance with a $1V_{pp}$ IF signal. However; as will be seen in Chapters 3 and 4, in the proposed voltage-domain mixers the cancellation of the sum frequency IF component is not possible at the intermediate nodes of the mixer; thus, half of the swing will be lost on the sum frequency IF component, meaning ideally the mixer will only be able to drive the ADC with a maximum $0.5V_{pp}$ IF signal.

Finally, the mixer's input impedance must be constant versus time. A variable mixer input impedance will distort the input RF signal that is driving the mixer; producing harmonic content at the input of the mixer. This harmonic content can be down-converted by the harmonic components of the square-wave LO waveform as will be seen in Chapter 2, degrading the in-band linearity performance. Thus, a constant input impedance is desired to achieve highly linear mixer operation.

1.4.1 RFDAC – Mixer Interface

The maximum voltage swing amplitude of the LDMOS's RFDAC is 28V, this of course is not viable as an input signal to a conventional CMOS IC, hence, the input signal is attenuated to a maximum amplitude of 1.1V before being fed to the CMOS chip. Since we ideally want to draw zero power from the RFDAC, the attenuation stage can be implemented as a capacitive divider. This attenuation stage is illustrated in Fig. 1.12, where R_{mixer_in} models the mixer's constant input impedance. For the remainder of this document, the interface configuration in Fig. 1.12 will be referred to as the mixer's AC configuration, since the input signal to the mixer is purely AC.

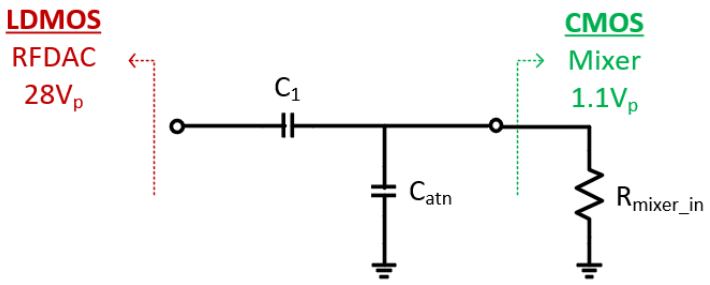

Figure 1.12: Mixer's Input AC Coupling with Attenuation

C_{atn} must be around 27 times larger than C_1 to provide an attenuation factor of 28, to reduce total area of the capacitors, C_1 is chosen as small as possible while still being

large enough not to be affected by parasitics. A value of ~30 fF was deemed small enough for C_1, making the value of C_{atn} ~800 fF. The mixer's resistive input impedance R_{mixer_in} is the only source of power consumption. At the intended $1.1V_p$ input RF amplitude and satisfying the maximum mixer power consumption set to 50mW, R_{mixer_in} thus has a minimum value of 12.1 Ω. Of course, R_{mixer_in} needs to be significantly larger than that as the clocking of the mixer will also consume power, so the total power consumption of the mixer cannot be all allocated to its input impedance. Therefore, R_{mixer_in} must be larger than 12.1 Ω. In addition, R_{mixer_in} should be large enough not to load the attenuation capacitor C_{atn}., if it does, then C_{atn} should be reduced to maintain the desired attenuation factor of 28.

As will be seen in Chapter 4, the need for a mixer input signal with DC bias will arise, yielding the RFDAC-Mixer interface configuration shown in Fig. 1.13. For the remainder of this document, the interface configuration in Fig. 1.13 will be referred to as the mixer's DC-biased configuration, since the input signal to the mixer now has a DC bias.

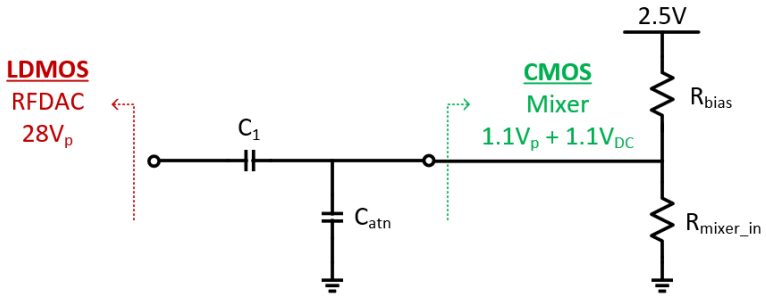

Figure 1.13: Mixer's DC-biased Input Coupling with Attenuation

In this configuration, the input impedance presented to the RFDAC is the parallel combination of the mixer's input impedance R_{mixer_in} and the DC biasing resistor R_{bias}. Both R_{mixer_in} and R_{bias} now consume both RF and DC power. R_{bias} cannot be sized arbitrary, a large R_{bias} will not load the mixer's input impedance, thus reducing the RF power consumption in R_{bias}, however, a large R_{bias} will reduce the DC bias at the mixer's input, ruining the mixer's operation. It was found in simulation that a choice of $R_{bias} \approx R_{mixer\_in}$ is a good trade-off for our proposed mixer topology. This yields a $1.1V_p$ input RF signal super-imposed on a $1.1V_{DC}$ bias at the mixer's input and satisfying the maximum mixer power consumption of 50 mW. In this DC-biased configuration, R_{mixer_in} has a minimum value of 74.2 Ω to meet the power consumption rerquiements.

As stated before and similar to the AC configuration in Fig 1.12, in the DC-biased configuration R_{mixer_in} needs to be significantly larger than 74.2 Ω as the clocking of the mixer will also consume power, therefore, R_{mixer_in} (and consequently R_{bias}) should be larger than 74.2 Ω. The proposed mixer topology presented later will limit the voltage stress on its internal active devices to $1.1V_p$.

In both configurations, a high input impedance for the mixer is desired to reduce the mixer's RF power consumption. However, increasing the impedance level in our proposed mixer implicitly raises its output impedance as well. A higher mixer output impedance will limit the IF bandwidth for a given loading capacitance, so there exists a tradeoff for how high or low the impedance level of the mixer can be.

1.5 PROJECT SCOPE

This master project focuses on the implementation of the mixer block inside the proposed observation receiver discussed in the previous section. Different mixer topologies are discussed including current-domain and voltage-domain mixers. A novel voltage-domain architecture is proposed that promises to achieve the very high linearity performance required while maintaining wideband capability. Its key advantage is that it can omit the use of an amplifying element, e.g., a TIA, which are difficult to realize with sufficient linearity in the intended bandwidth. Different flavors of the proposed mixer topology are discussed, with their advantages and disadvantages analyzed.

1.5.1 Project Objective

The objective of this thesis work is to explore the design and implementation of a novel highly-linear wideband harmonic-reject voltage-domain mixer satisfying the requirements of the observation receiver system.

1.5.2 Project Specifications

Based on the foregoing discussion, the mixer should meet the following specifications:

- The mixer must have 65 dBc linearity.
- The mixer must have at least 40 dB Harmonic Rejection Ratio.

- The mixer must have an IF bandwidth approaching 1 GHz.
- The mixer must consume as little power as possible with a ceiling of 50mW. This includes both RF power drawn from RFDAC, as well as LO power consumed in clocking generation.
- The mixer must be designed for a carrier frequency of 3.5GHz to be compatible with mMIMO applications.
- The mixer must approach 0.5 V_{pp} output swing for baseband IF (-2 dBm).
- The mixer's input impedance must be constant and as high as possible with an absolute minimum of 12.1 Ω (or 74.2 Ω in case of DC-biased configuration).
- The mixer must be able to drive a load of approximately 250 pF, that is considered to be the capacitive loading of the ADC that will follow the mixer in the observation receiver.

It must be noted that our mixer is designed to drive a capacitive load presented by the ADC input. This means that the use of the dBm unit at the mixer's output is somewhat arbitrary. Our dBm measurements follow the definition proposed by B. Razavi in [10], where any voltage-swing can provide a dBm value assuming an arbitrary 50Ω load, regardless of the actual impedance level at that voltage-swing. Using this approach, it's easier to directly compare with other works. However, for completion, the mixer's linearity will also be reported in dBV.

1.6 THESIS OUTLINE

Chapter 2 highlights basic mixer background relevant to the work of this thesis, it also provides a thorough comparison between voltage-domain and current-domain mixers, showcasing the motive behind choosing voltage-domain mixers for our intended application. Chapter 3 presents the three novel mixer topologies devised in this thesis work, compares them, and provides the motive behind the final mixer topology selected for implementation. Chapter 4 deals with the practical implementation aspects of the novel extremely-linear wideband voltage-domain harmonic-reject mixer in TSMC40nm thin-oxide CMOS technology.

2 MIXER BACKGROUND

2.1 HARMONIC REJECTION

Ideally, the mixing function can be implemented by the multiplication of the RF component with the LO frequency. This ideal multiplication of the sinusoidal signals in the time-domain is equivalent to their convolution in the frequency-domain. Hence, it is easy to see that this convolution results in the difference and sum of the two frequencies. This ideal mixing process is visualized in Fig. 2.1. Depending on the relation between the two frequencies, the mixer operation can provide either up-conversion or down-conversion of our RF input signal.

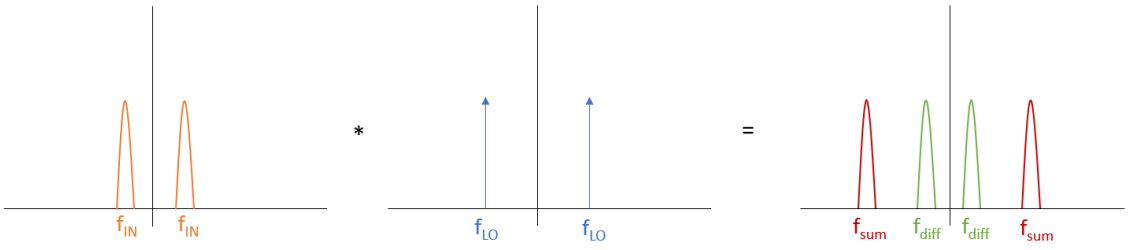

Figure 2.1: Ideal Sine-wave Mixing using a Double-Sided Spectrum Representation

In a practical mixer implementation, the multiplication is done using switches. However, this implies that continuous multiplication with a sine-wave is not possible, a switch has only two possible states; “on” or “off”. Consequently, the multiplication in a real circuit is always with a square wave. This still produces the sum and difference frequencies, but also produces many more frequency components due to the harmonic content of the square wave. This is illustrated in Fig. 2.2 where only the third and fifth harmonics are accounted for.

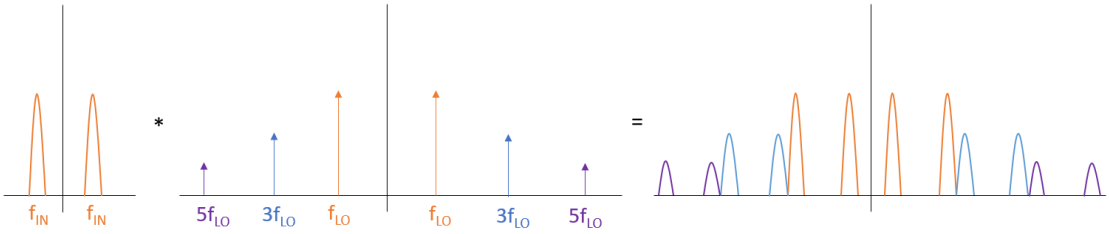

Figure 2.2: Practical Square-wave Mixing

As can be seen in Fig. 2.2, the mixing of the input signal with the harmonics of the square-wave result in unwanted components. This problem is more severe if the input signal itself has odd harmonics, since the mixing of these with the equivalent odd harmonic from the square-wave LO will result in components close to the fundamental bandwidth. This is the case for our application since our input signal is the square-wave output of the RFDAC which contains odd harmonics.

A clever solution to get rid of the LO harmonics involves shaping the LO waveform in a manner that will attenuate its harmonics [11]. This is known as harmonic rejection. An example of a harmonic rejection waveform is shown in Fig. 2.3.

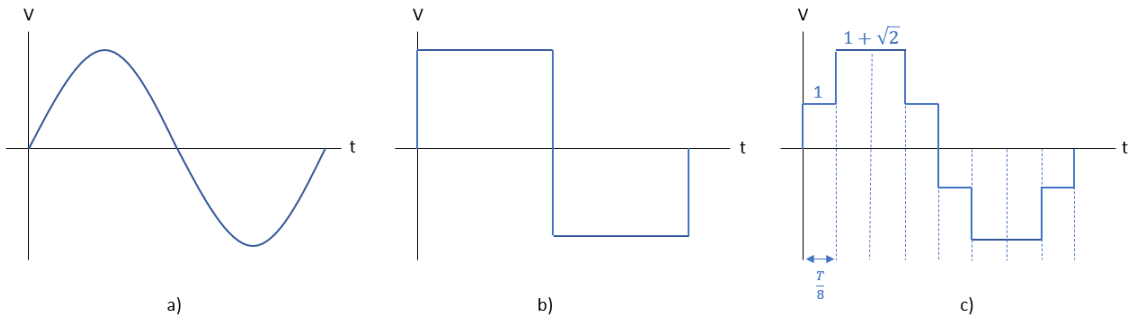

Figure 2.3: a) Pure Sine-wave – b) Pure Square-wave – c) Harmonic Rejection Waveform

Intuitively, we can see that the harmonic rejection waveform approaches the pure sine-wave waveform more than the pure square-wave, we should intuitively deduce then that the harmonics of the shaped waveform must be less than that of the pure square-wave. This is quantitively confirmed if we consider the harmonic rejection waveform as the summation of three shifted square-wave signals with different amplitudes and draw their phasor diagrams looking at the fundamental, third harmonic, and fifth harmonic frequencies respectively as shown in Fig. 2.4.

It is clear then from the phasor diagrams that this shaped waveform rejects the third and fifth harmonic of the square-wave LO, the two strongest harmonics. Any linear scaling of this harmonic reject waveform will maintain the same harmonic rejection property. This LO waveform can be implemented by using three mixers with three phase-shifted LO square-waves with equal amplitude, while the amplitude scaling of the LO waveforms can be done to the input RF signal itself. The summation of the resulting signals from all three mixers will have no third or fifth harmonic terms. The frequency domain representation of our harmonic reject waveform will be as shown in Fig. 2.5.

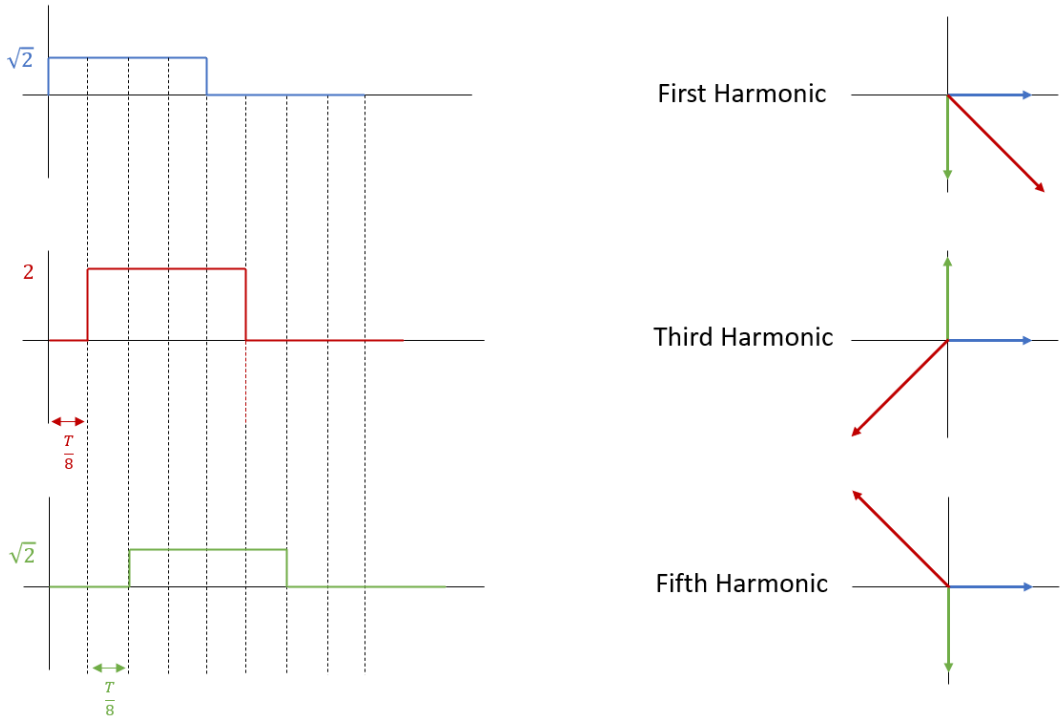

Figure 2.4: Harmonic Rejection waveform Decomposition and Phasor Diagram

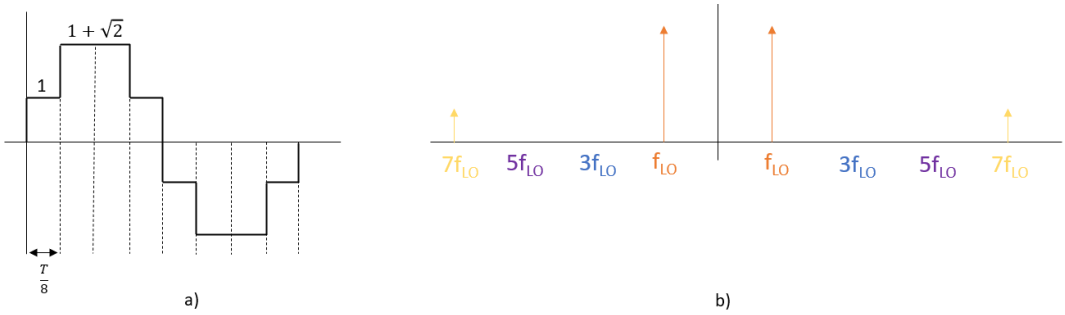

Figure 2.5: Harmonic Reject waveform in: a) Time domain – b) Frequency domain

It should also be noted that a continuum of harmonic rejection waveforms exists, where even more harmonics can be rejected. A general equation for harmonic rejection waveforms was derived in [12] as following:

$$A_{n,I} = \left|\sin\left(\frac{2n}{N}\pi + \theta\right)\right| \tag{2.1}$$

Where N is the number of samples taken from a pure sine-wave, n is an integer from 0 to N-1 representing the sample number, and θ is an arbitrary phase shift. All LO harmonics are rejected except harmonics at (kN±1)LO, where k is an integer.

In our chosen harmonic reject waveform, N is set to 8 yielding eight samples of the pure sine-wave, and θ is equal to $\frac{\pi}{n}$. If we include the quadrature part of the mixer as well, we can use the same equation but shifted 90 degrees.

$$A_{n,Q} = \left|\cos\left(\frac{2n}{N}\pi + \theta\right)\right| \tag{2.2}$$

Since these amplitudes represent the scaling of our RF input, if we want the input impedance of the mixer to be constant, we want the summation of these sampled amplitudes A_n and $A_{n,q}$ to be constant for all n. This is satisfied in our chosen harmonic rejection waveform with N = 8. An easier visualization of the above condition can be verified by looking at both the I and Q harmonic reject LO waveform with N = 8 as seen in Fig. 2.6. Assuming for each of the two scaled RF inputs we require a certain input impedance from that mixer path, it is clear that across the whole cycle the required impedance is constant as the I and Q mixers swap their required scaling, i.e., their input impedance.

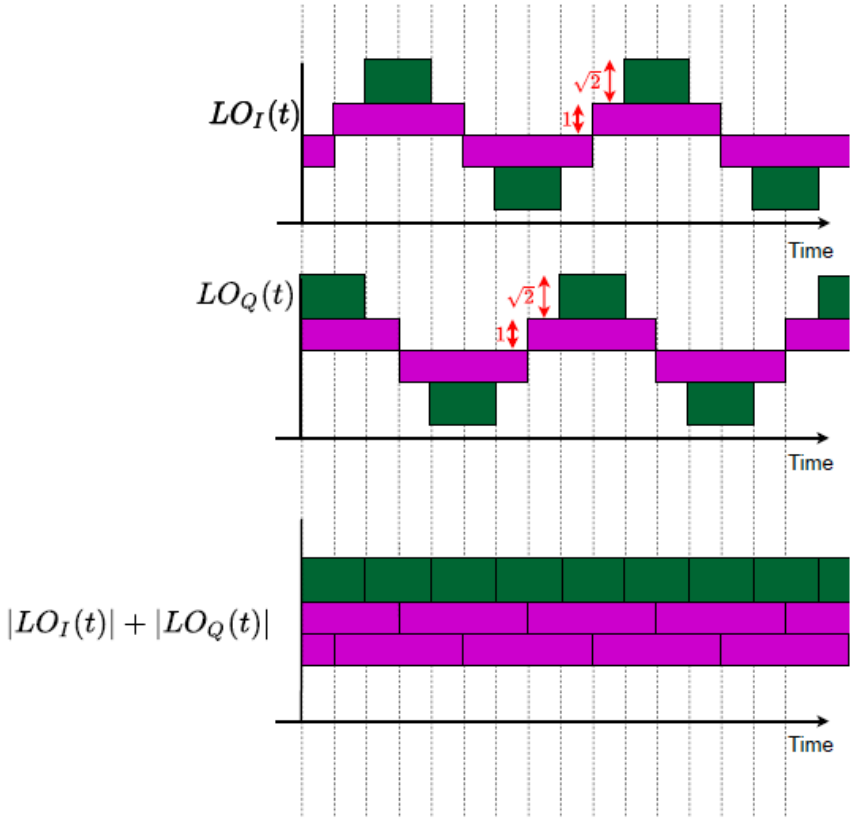

Figure 2.6: The combined I and Q paths present a constant input impedance over time

Higher values of N, i.e., more samples of the pure sine-wave meaning more shifted individual square-waves mixers, can reject more LO harmonics but at the expense of the constant input impedance. This conclusion can be verified by summing equations 2.1 and 2.2 with $N > 8$. For any value of θ, it will be found that the summation is no longer constant. However, in our application, the rejection of the third and fifth harmonic is deemed enough, hence our harmonic reject waveform with $N = 8$ is satisfactory.

Finally, it should be noted that the harmonic rejection functionality can be added to any mixer topology by combining the scaled paths. Therefore, it is not a redeeming function of any single topology over the other. In the next section, we will discuss current-domain and voltage-domain mixers in their most simple case without harmonic rejection, since it should be implicitly understood that harmonic rejection can be added to any of these mixer topologies with the right combination of scaled versions of them.

2.2 CURRENT DOMAIN MIXERS

The switching behavior required for mixing can be implemented by commutating (i.e., switching) currents between two branches. A simple single-balanced current-domain mixer is presented in Fig. 2.7. As can be seen, the simple current-domain mixer consists of three sub-blocks; a transconductance that changes the voltage signal into a current signal, two commutating switches that perform the mixing function in the current-domain, and a I-to-V converter in the form of the load resistor.

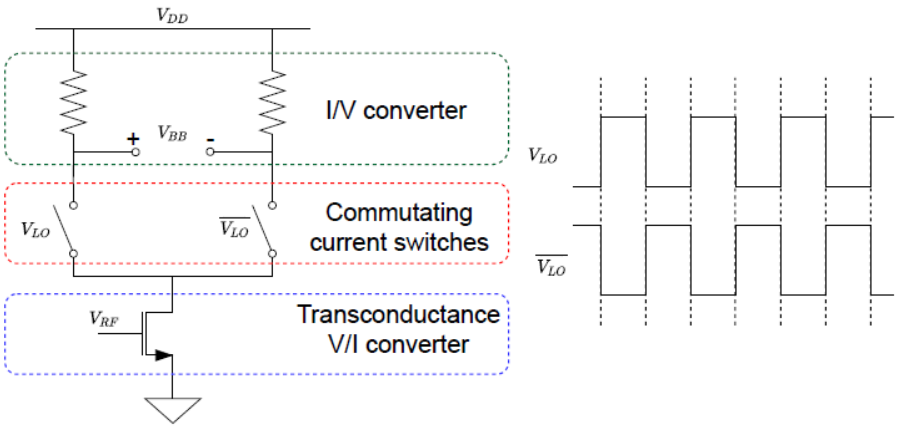

Figure 2.7: Simple Single-balanced Current-domain Mixer

In a single-balanced mixer, the LO clock is typically differential while the RF input is single-ended. Although the RF signal does not show up in the differential IF output, this

configuration does not offer any common-mode rejection for the RF signal. Furthermore, the single-balanced mixer suffers from significant LO-IF leakage. This will result in unwanted spurious tones at the output. To counter this problem, typically two single-balanced mixers are connected together such that their LO-IF leakage cancels each other, this implicitly also provides common-mode rejection for the RF signal since the RF signal is now also differential. This topology is called double-balanced mixer and is presented in Fig. 2.8.

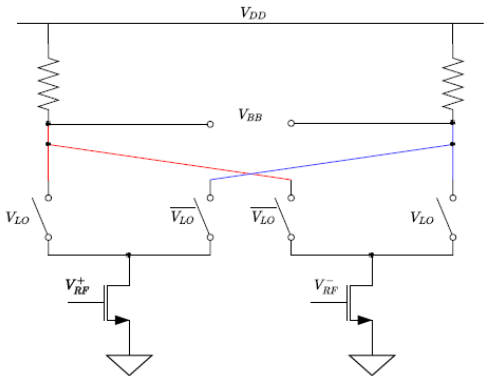

Figure 2.8: Simple Double-balanced Current-domain Mixer

One main source of non-linearity in the simple current-domain mixer is the I_D-V_{GS} non-linearity of the transconductance stage. To overcome that, a different topology is implemented where the input impedance of the mixer is chosen low enough such that the input RF signal is already considered a current-domain signal. This allows the switching functionality to be implemented with passive switches, followed by a transimpedance amplifier (TIA) stage. This topology is presented in Fig. 2.9.

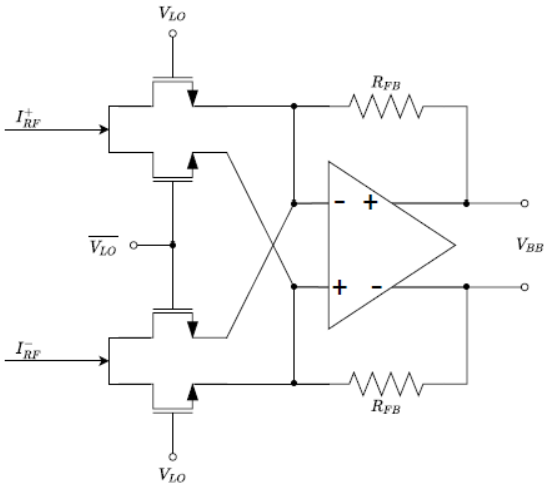

Figure 2.9: Double-balanced Current-domain Mixer with TIA

Both of the aforementioned topologies can be extended into a harmonic rejection implementation. For example, for the topology in Fig. 2.8, Weldon [11] demonstrated a harmonic rejection implementation were three active double-balanced mixers were used to implement the harmonic rejection. The circuit is shown in Fig. 2.10. The scaling has been implemented by scaling the transconductance stage and the summation is done in the current domain at the output node. Harmonic rejection can also be applied to the topology in Fig. 2.9., as was done by C. Andrews and A. C. Molnar [13] and is presented in Fig. 2.11.

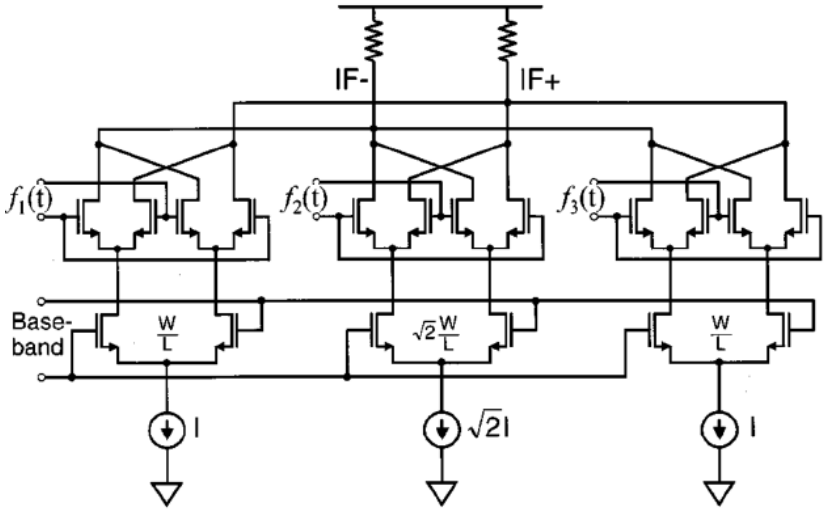

Figure 2.10: Harmonic rejection mixer using double-balanced active current-domain mixers [11]

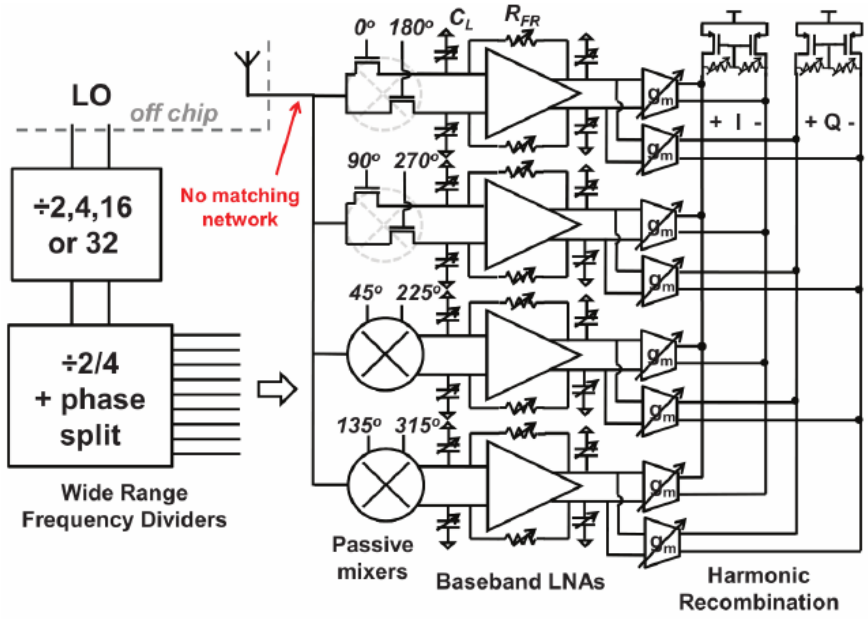

Figure 2.11: Current-domain mixer with harmonic rejection, as part of a mixer-first receiver [13]

In the implementation shown in Fig. 2.11, harmonic rejection was achieved by placing multiple mixers in parallel, this meant multiple transimpedance stages that consume more power and take up more area than necessary. An implementation where the scaled currents are added prior to the TIA stage was proposed by G. Hardeman in [7], this approach requires a single TIA for harmonic rejection, saving up on area and power consumption. The circuit is presented in Fig. 2.12.

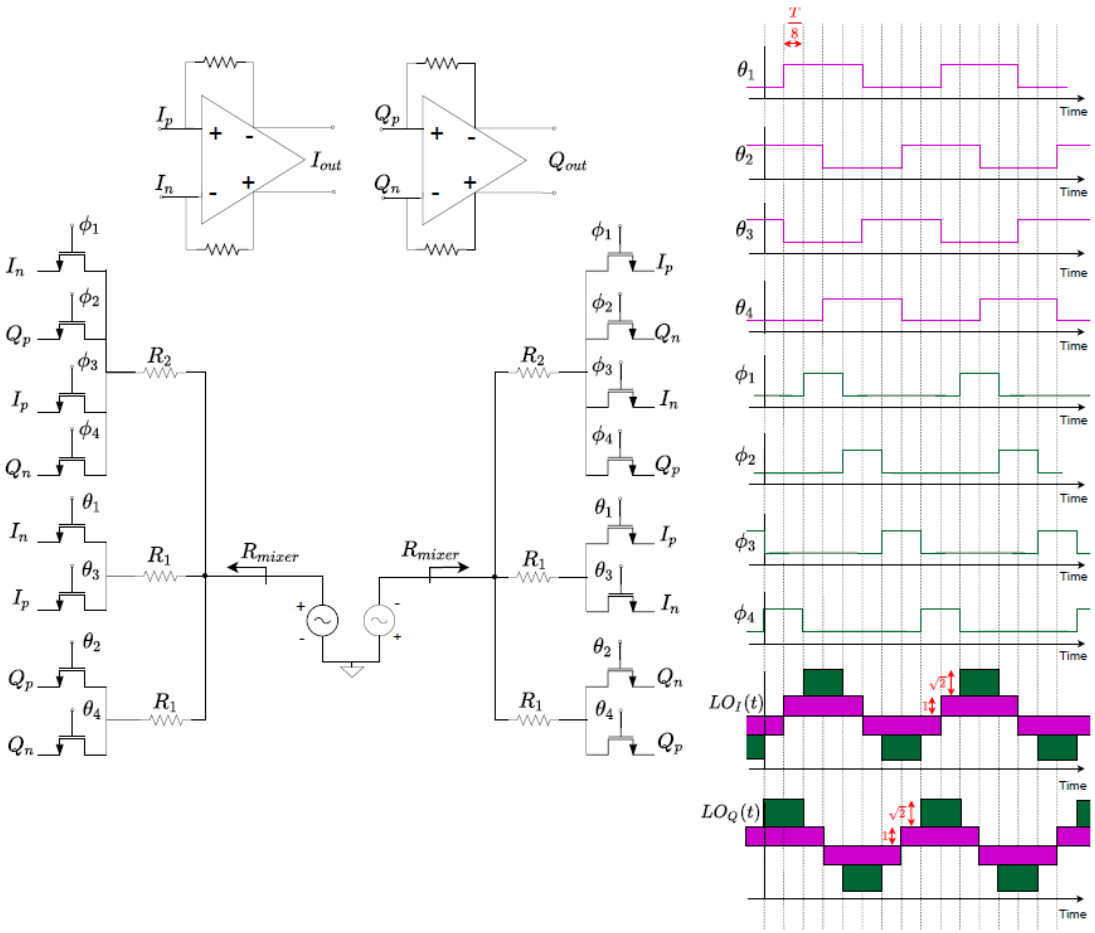

Figure 2.12: Proposed Mixer in [7], both In-Phase and Quadrature-Phase shown

In all of the aforementioned current-domain mixer implementations, there eventually is always either a transconductance stage or a transimpedance stage needed that limits the linearity performance of the mixer. The low-power g_m-cells that are extensively used for harmonic rejection amplitude scaling in [11] and [13], limits the in-band IIP3 linearity performance to < 0 dBm making these topologies less suitable for high-linearity applications such as our observation receiver. A remedy to get rid of the transimpedance or transconductance cells is to operate fully in the voltage-domain, these mixers are known as voltage-domain mixers.

2.3 VOLTAGE DOMAIN MIXERS

The simplest implementation of a single-balanced voltage-domain mixer is shown in Fig. 2.13a. As can be noticed, the multiplication here is being done in voltage-domain. This topology can easily be extended into a double-balanced topology as seen in Fig. 2.13b.

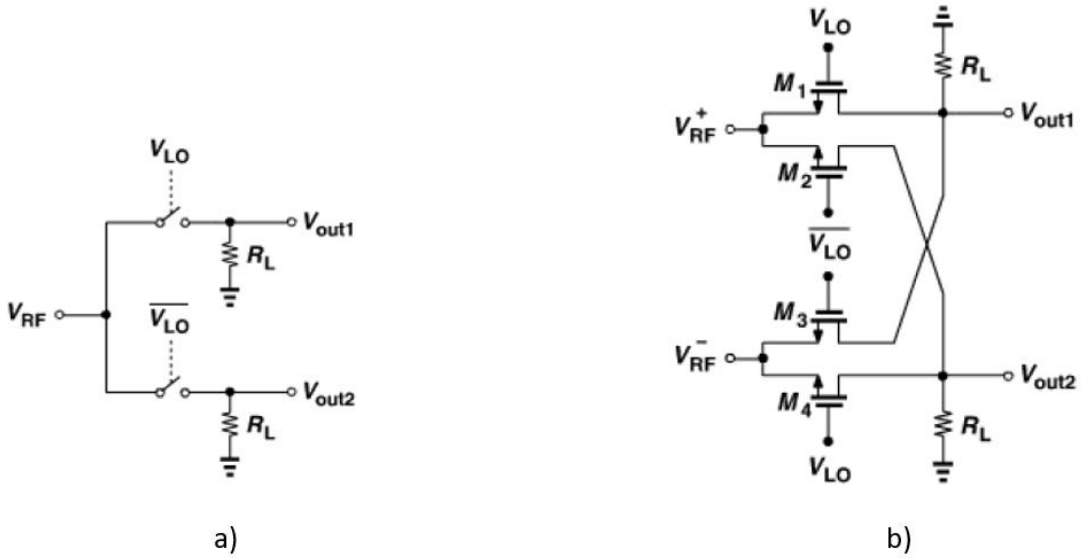

Figure 2.13: Simple Voltage-Domain Mixer: a) Single-Balanced – b) Double Balanced [10]

As there are no transconductance or transimpedance stages in a voltage-domain mixer, and since a voltage is desired at its IF output rather than IF power, the implementation is truly passive and ideally consumes zero power. Furthermore, the mixer linearity is no longer limited by the transconductance or transimpedance stages, meaning that voltage-domain mixers have the potential for achieving higher in-band IIP3 linearity than their current-domain counterparts, providing that other non-linearities do not dominate too much. Finally, the omittance of the transconductance and transimpedance stage can allow for more compact layouts, reducing the area of the whole mixer block.

The topology in Fig. 2.13 can be extended into a harmonic rejection topology as was demonstrated by K. Kibaroglu [14], in his implementation, eight scaled mixers are used in independent paths to achieve the scaling, the addition is done in the voltage-domain at the IF output ports. The circuit is presented in Fig. 2.14, and it managed to achieve an in-band IIP3 performance of around 20 dBm, a much better linearity performance than its current-domain counterparts.

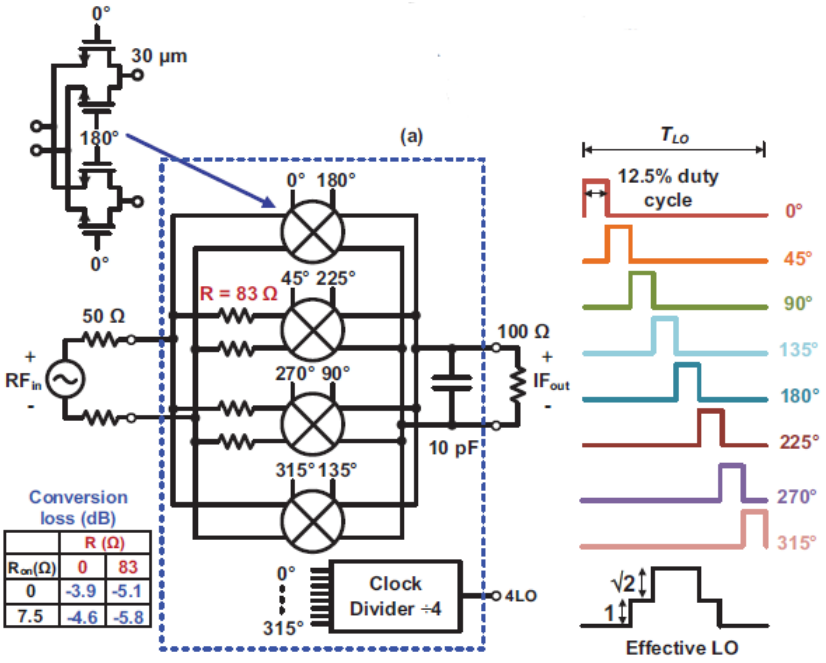

Figure 2.14: High-Linearity Voltage-Domain Harmonic Rejection Mixer [14]

The flipside of voltage-domain mixers is twofold. Firstly, the omission of all the transconductance and transimpedance stages means that the mixer has no amplifying capability being fully passive, this means that the conversion gain of a passive voltage-domain mixer is usually limited. It can be theoretically proven that the conversion gain of the topologies in Fig. 2.13 is limited to $\frac{2}{\pi} \approx -4\ dB$ [10]. Secondly, the source terminal of the switching transistor is now varying with the input voltage, resulting in a V_{GS} source of non-linearity as the R_{ON} of the switch now depends non-linearly on the input voltage. Bootstrapping is usually used to compensate for V_{GS} non-linearity; however, this involves the inclusion of a charge-pump block increasing complexity, area, and power consumption. Furthermore, at the high frequencies used in our mixer, it may not be directly feasible to design a charge-pump with sufficient bandwidth. Finally, it also can cause device reliability issues as more than one V_{DD} drop can occur.

The first short-coming; low-gain, is not a problem in our application. Since the observation receiver follows directly after the power RFDAC. Consequently, the input signal can be as large as the maximum allowed supply volage. This negates the need for any gain, unlike the case as in normal communication receivers that need to conform to very low sensitivity input levels. As for the second short-coming, if a topology can be devised that gets rid of the V_{GS} non-linearity by (somehow) fixing the source voltage of the switching elements, then better linearity can be achieved.

3 PROPOSED HIGHLY-LINEAR VOLTAGE-DOMAIN MIXER TOPOLOGIES

3.1 PROPOSED CONCEPT

We start with the most basic implementation of our proposed voltage-domain mixer concept and work our way from there towards three different variations; which will be referred to as topology A, B, and C, for which we will highlight the advantages and disadvantages and provide the basis for our final mixer topology selection.

Starting from the idea of cancelling out V_{GS} variation, a basic mixer topology can be extrapolated from Fig. 2.13a as shown in Fig. 3.1, where the source terminal of the switching transistor is now tied to ground. This means that the switching transistor no longer suffer from V_{GS} non-linearity, since the input signal no longer affects the controlling LO signal, meaning R_{ON} is no longer strongly input dependant. The IF output node still has the intended multiplication functionality that results in the mixing products, if the switch is on, the IF port output is tracking the input with a certain attenuation factor depending on values of R_1 and R_2, and if the switch is off, the IF output port tracks the RF port exactly. In essence, the input is being multiplied by a square-wave LO waveform just like in the topologies in Fig. 2.13, except now the LO square-wave waveform is switching between two different amplitudes. However, there is now a direct path from the RF to the IF output port, implying there is no RF rejection which is undesired.

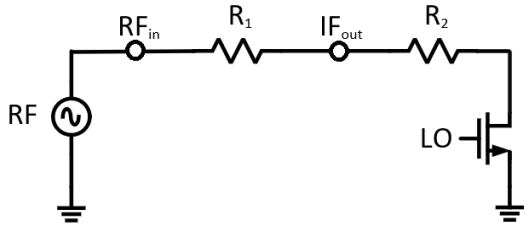

Figure 3.1: Simplest form of Proposed Concept

To cancel this RF feedthrough, one can extend the topology in Fig. 3.1 to include another mixer branch using opposite phase relations for the RF and LO signals, as such rejecting the RF signal at the output node, effectively providing a double-balanced mixer implementation directly, as is shown in Fig. 3.2.

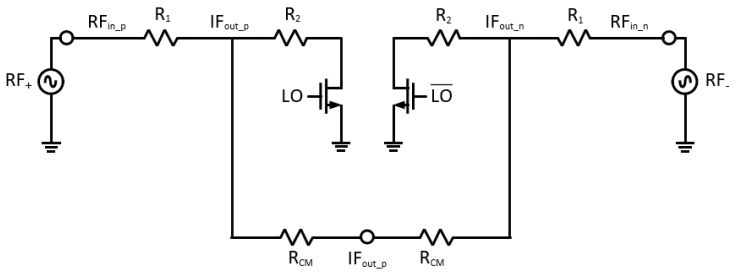

Figure 3.2: Double-balanced version of Proposed Mixer with no Harmonic Rejection

It must be noted that in this configuration, the output IF signal is a single-ended signal that can be sensed using two large resistors. These two large resistors are needed to avoid loading the mixer's scaling resistors R_1 and R_2. Unfortunately, with a capacitive load such as that of a baseband ADC which is following this mixer in our observation receiver, the IF bandwidth will be limited by the RC time constant formed by the large sensing resistors R_{CM} and the input capacitance of the ADC. This is a point that will be addressed in later voltage-domain mixer topologies variations.

The topology in Fig. 3.2 acts as the basis of the three proposed mixer variations in the following sections. All their pros and cons will be addressed. However, the main advantage of all of these topologies is the complete omission of V_{GS} non-linearity. To arrive at a double-balanced mixer implementation with differential IF outputs, the circuit in Fig. 3.2 can simply be duplicated with the RF inputs reversed. This is illustrated in Fig. 3.3. Differential IF output is a desired property to supress the impact of distorting or interfering signals on the IF signal of interest.

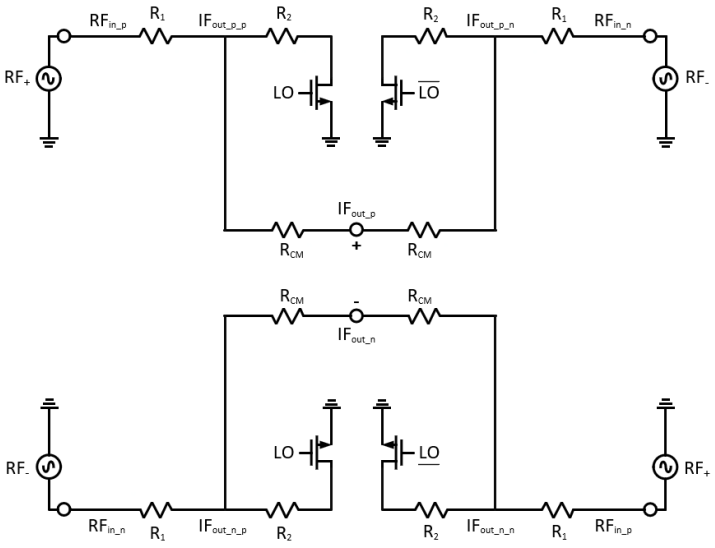

Figure 3.3: Double-balanced Proposed Mixer with Differential IF outputs and no Harmonic Rejection

It should be noted that since the RF signal is rejected in the topology of Fig. 3.2, we should expect its output to have a form similar to that of the waveform shown in Fig. 3.4. This waveform is the output of the single-balanced topology in Fig. 2.13a that implicitly rejects any RF feedthrough. It can be seen that the single-tone RF input signal's phase is reversed whenever the LO phase is reversed. Consequently, the IF signal resulting from the multiplication of the LO and RF signal will remain in phase as desired in both LO phases, while the RF feedthrough will be out of phase and hence cancelled as desired in both LO phases.

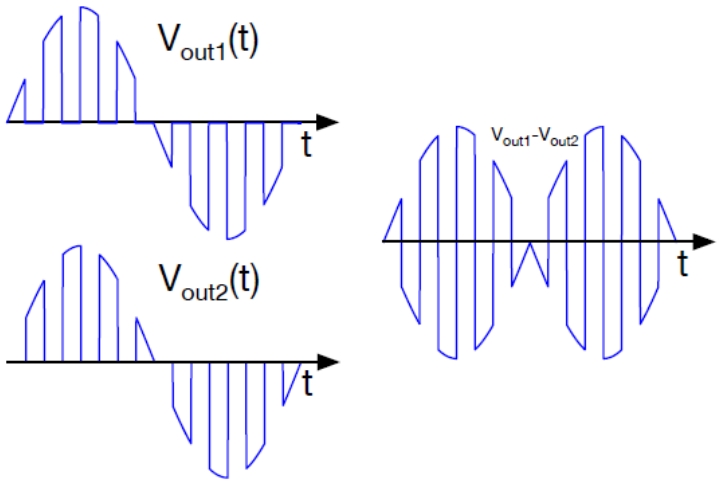

Figure 3.4: Single-Balanced Mixer's Output Waveform for a Single-Tone RF Input Signal

The topology in Fig 3.5 is different, since the individual outputs $IF_{out\_p\_p}$ And $IF_{out\_p\_n}$ do not return to zero as V_{out1} and V_{out2} in Fig. 3.4, instead they return to the full-scale RF input. It can be confirmed that the topology in Fig. 3.5 achieves an output form similar to the waveform shown in Fig. 3.4 by calculating the common-mode output signal in the two phases of the LO as following:

$$\begin{aligned} LO &\rightarrow \quad IF_{out} = IF_{out\_p} + IF_{out\_n} = \alpha \cdot RF_p + RF_n = (\alpha - 1) \cdot |RF| \\ \overline{LO} &\rightarrow \quad IF_{out} = IF_{out\_p} + IF_{out\_n} = RF_p + \alpha \cdot RF_n = -(\alpha - 1) \cdot |RF| \end{aligned} \tag{3.1}$$

Where α is a certain attenuationon factor depending on R_1 and R_2. It is clear then that the output attenuation factor (1 - α) is the same in both LO phases, the output signal will therefore provide an output waveform similar to the waveform in Fig. 3.4 as expected. This is visualized in Fig. 3.5. It must be noted that this is a special case since the attenuation factor (1 – α) is constant in both LO phases, in harmonic rejection

implementations this is not guranteed, as will be seen in Chapter 3. In that case, each indvidual IF output will have be to grounded for half of the LO period, to allow for correct summation of the two indvidual IF outputs to arrive to a similar waveform as the one shown in Fig. 3.4. The similarity in the output waveform of the topology in Fig. 3.2 to the one by the single-ended topology in Fig. 2.13a further confirms the RF-feedthrough rejection by this proposed topology.

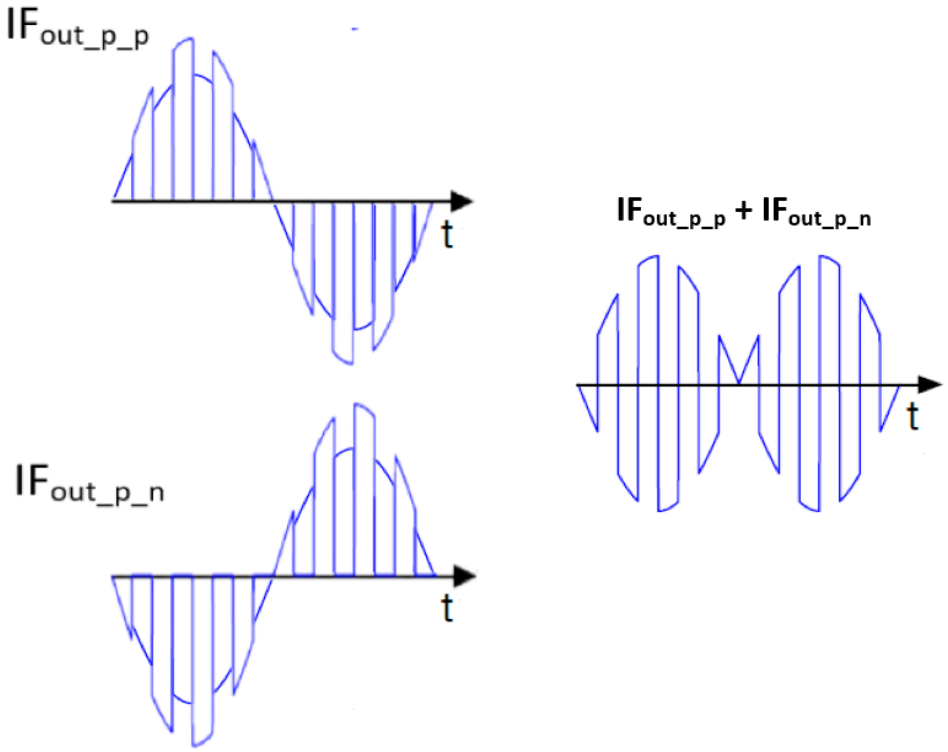

Figure 3.5: Proposed Mixer's Attenuated Output Waveform for a Single-Tone RF Input Signal

3.2 MIXER TOPOLOGY A

An extrapolation of the topology presented in Fig. 3.3 can be the inclusion of harmonic rejection as is shown in Fig. 3.6. In this topology, 8-phases of the LO clock with 12.5% duty-cycle are used in which each clock phase controls one switch. R_{big} and R_{small} are chosen such that the ratios between their respective potential dividers with R_1 is $1+\sqrt{2}$. This scaling ensures harmonic rejection is achieved while maintaining all the linearity improvements due to the omission of V_{GS} non-linearity.

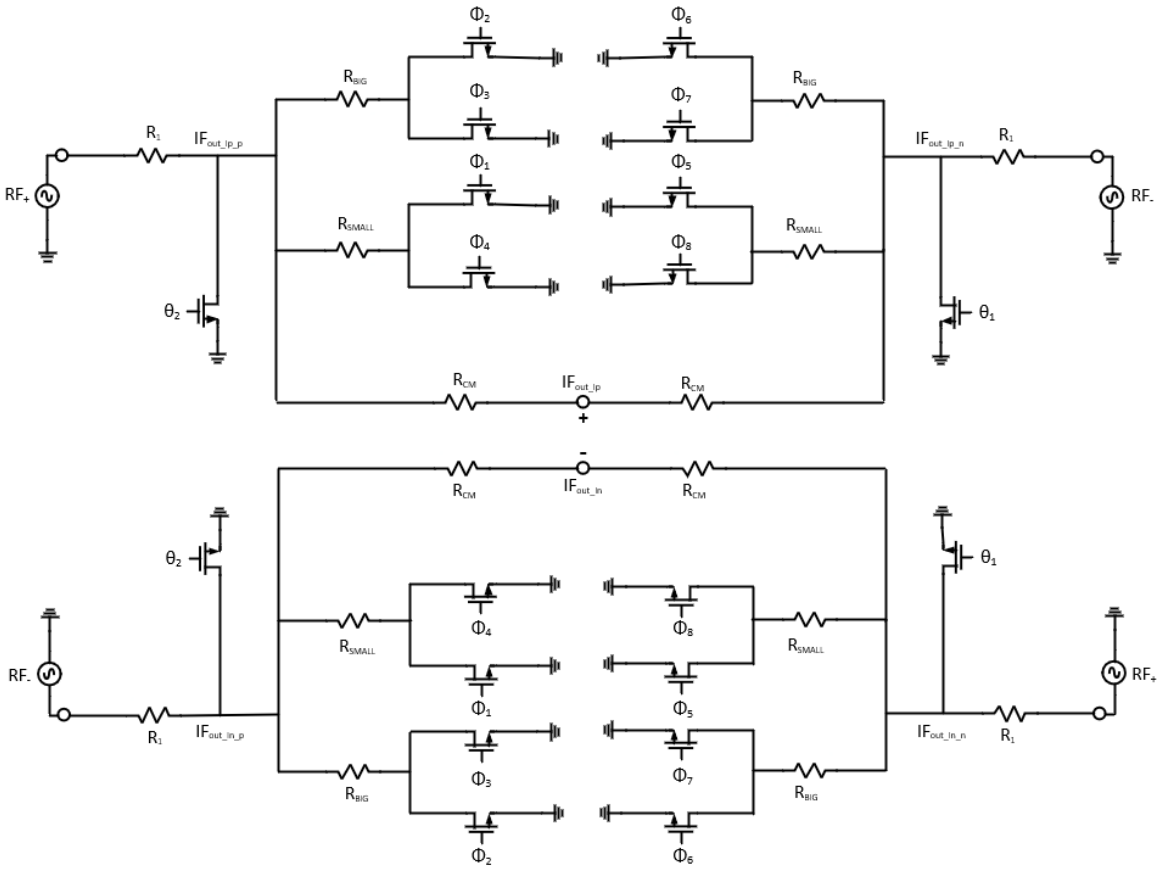

Figure 3.6: Mixer Topology A (In-Phase Mixer only)

Fig. 3.6 showcases only the in-phase mixer part, the quadrature-phase mixer is basically a copy of the same circuit with all the LO phases shifted by 90 degrees. The related clocking scheme is presented in Fig 3.7.

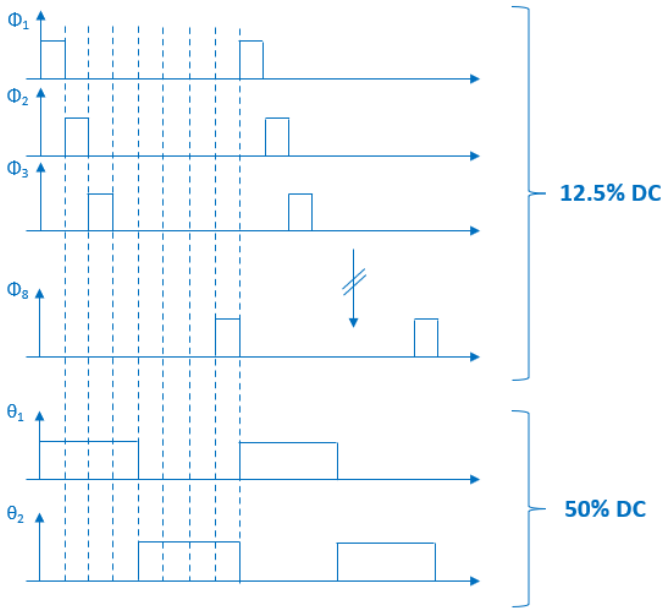

Figure 3.7: Mixer Topology A – Clocking Scheme

Analysis of the above topology taking into account the different clock phases as well as the not shown quadrature-phase mixer, will show that the full I/Q mixer presents a constant input impedance given by the following equation (assuming ideal $R_{ON} = 0$):

$$Z_{mixer\_in} = (R_1 + R_{big})//(R_1 + R_{small})//\frac{R_1}{2} \tag{3.2}$$

The conversion gain is also given by the following equation (assuming ideal $R_{ON} = 0$):

$$Conversion\ Gain = \frac{R_{big}}{R_{big} + R_1} \cdot \frac{2}{\pi} \tag{3.3}$$

There are four extra added switches with phases θ_1 and θ_2 in Fig. 3.6 compared to the original topology in Fig. 3.3. This is necessary to achieve an output waveform similar to the waveform in Fig. 3.4 and reject the RF component while maintaining harmonic rejection. If we focus on a single half of the mixer presented in Fig. 3.6, i.e., the upper half circuit producing IF_{out_p}, one "half" of this circuit needs to be zeroed such that the common-mode output signal (IF_{out_p}) is simply that of the other "half" of this circuit. This is the case here since if that switch was not added, the output common-mode signal (IF_{out_p}) will be a summation of the other "half" and the full RF signal from the now not grounded "half", this will ruin the harmonic rejection scaling. This was not the case in

Fig. 3.5 as there was no harmonic rejection scaling, there was only one scale factor (α) throughout both "on" phases of the LO signal.

This mixer topology was designed in TSMC40nm thin-oxide CMOS technology, the mixer was loaded by a 250 pF capacitor to mimic the ADC's input capacitive loading. R_1, R_{big}, and R_{small} were sized to achieve the correct scaling while satisfying the input impedance specification. The parasitics introduced by all of the switches add a phase-error that degrades the harmonic rejection performance, they cannot be sized too big so as to not add too much phase error, and they cannot be sized too small, since then their R_{on} would be comparable to R_{big} and R_{small} and V_{DS} non-linearity will start to be more significant. In the end, the linearity specification was achieved but the harmonic rejection was limited to around 35 dB due to the phase error introduced by the parasitics of the switches.

There is a total of 40 switches in this topology in the full I/Q mixer, this is a large number of switches to route for in the layout without introducing unbalances. In addition, the topology requires 12.5% duty-cycle phases, which at 3.5 GHz carrier frequency is not easy to achieve in TSMC40nm thin-oxide CMOS technology. To maintain acceptable harmonic rejection, the switches could not be sized up enough, so their V_{DS} non-linearity was evident. Finally, the IF bandwidth was limited by the RC time constant set by R_{CM} and the succeeding ADC's input capacitance. This motivated the search for other improved mixer topologies. Perhaps in a smaller technology node with less parasitics and faster clocks, this topology can still be interesting.

3.3 MIXER TOPOLOGY B

A variation on the mixer topology A presented in the previous section is shown in Fig. 3.8. As with the previous topology, only the in-phase mixer is shown, the quadrature-phase mixer is again basically a copy of the same circuit with the LO phases all shifted by 90 degrees. In this topology, the two resistors R_{big} and R_{small} are placed in series instead of in parallel to reduce the total number of mixing switches and allow for 25% duty-cycle LO waveforms. The mixing functionality is again achieved using switches with their source terminal's grounded, omitting V_{GS} non-linearity as desired.

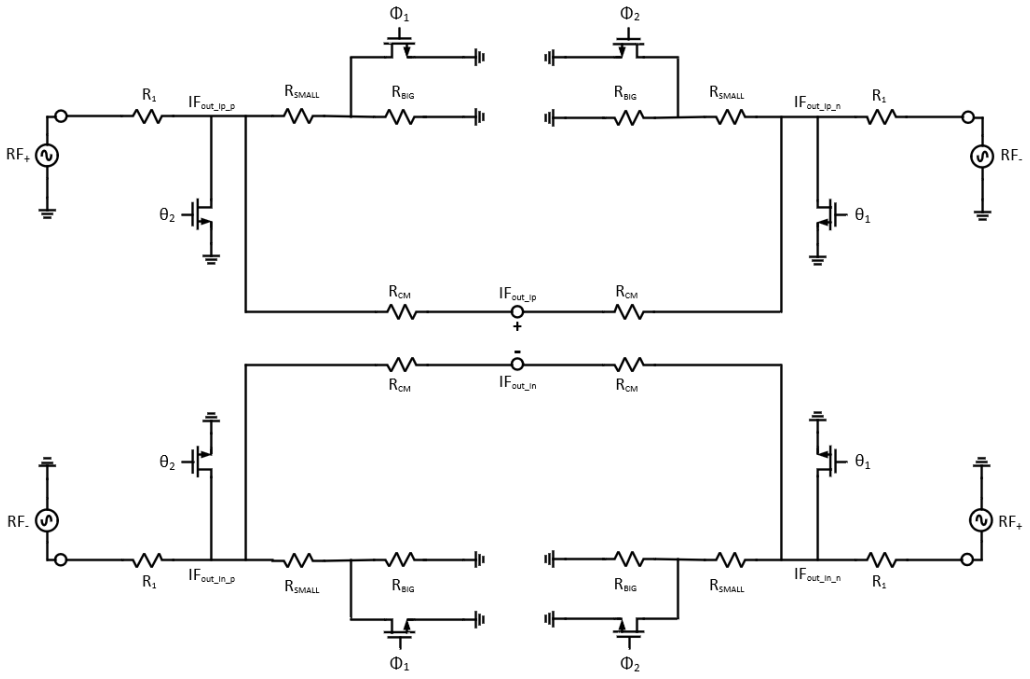

Figure 3.8: Mixer Topology B (In-Phase Mixer only)

Its clocking scheme is shown in Fig. 3.9, employing 75% duty-cycles (or 25% inverted) instead of 12.5% duty-cycles as in the previous topology. The operation is simple, when the mixing switch ($\phi_{1/2}$) is "on", R_{big} is shorted and the output voltage is scaled by the ratio defined between R_{small} and R_1, on the other hand when the mixing switch ($\phi_{1/2}$) is "off", the output voltage is scaled by the ratio defined by R_{small} + R_{big} and R_1, these scalings have a ratio of $1+\sqrt{2}$ to achieve the harmonic rejection waveform. As with the previous topology, four other switches ($\theta_{1/2}$) are employed to nullify the output from one "half" of the topology to achieve an output waveform similar to the waveform in Fig. 3.4, i.e., allow for a "negative" LO signal to be able to cancel out the RF feedthrough.

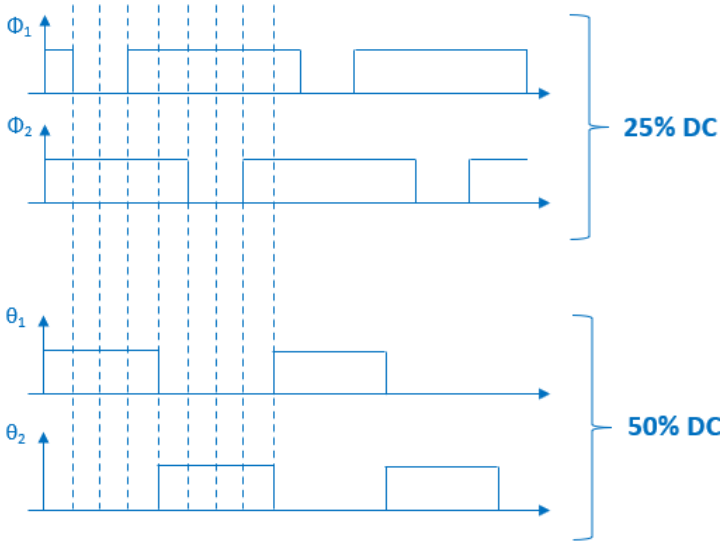

Figure 3.9: Mixer Topology B – Clocking Scheme

The replacement of 12.5% duty-cycles with 75% duty-cycles (or 25% inverted) relaxes the speed requirement on the CMOS technology applied. Furthermore, the number of switches is reduced to only 16 for the whole I/Q mixer, this allows for much easier clock routing. This topology also provides better harmonic rejection as well as better linearity than the previous topology. To understand why, we have to look at the capacitances of the switches when they are off. This is illustrated in Fig. 3.10 for both topologies at a certain LO phase.

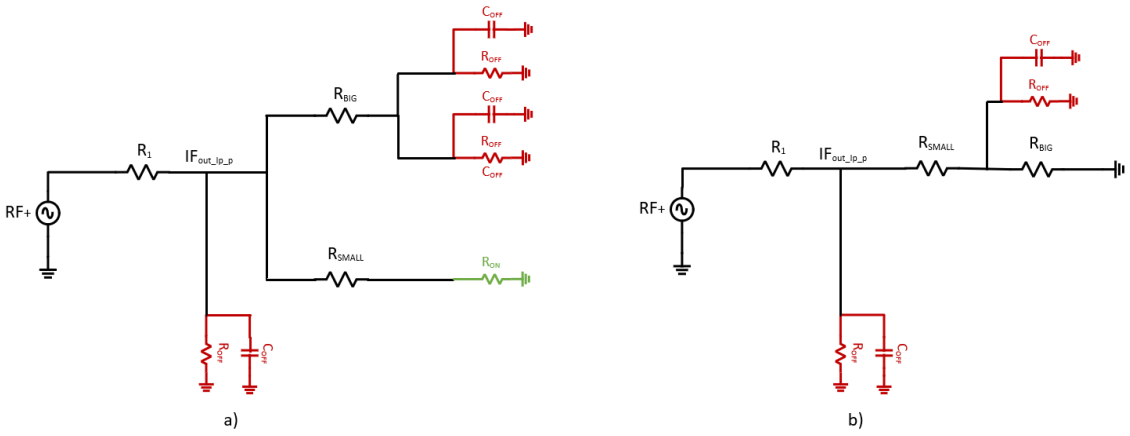

Figure 3.10: Impact of off-capacitance for: a) Mixer Topology A – b) Mixer Topology B

In Fig. 3.10a, we see the situation when one of the R_{small} LO phases is high, this means that the R_{big} LO phases are low. Since R_{off} is large, C_{off} would dominate the switches' off impedance. This means that $2C_{off}$ will form an RC network with R_{big}, this network

presents an undesired impedance in parallel with R_{small} + R_{on}. Hence, this will introduce a significant phase-error, degrading the harmonic rejection. Furthermore, we see that the output voltage is going to appear on $2C_{off}$ with a potential divider based on the ratio between R_{big} and $2C_{off}$, let's denote this attenuation factor as α_1 for now.

As for Fig. 3.10b, we see the situation when the LO phase is low, as in the other situation when LO phase is high the off capacitance will be shorted. In the illustrated case, we see that the parallel combination of C_{off} and R_{big} will form an RC network with R_{small}. It should be noted that R_{big} in this topology is equivalent to $R_{big} - R_{small}$ from Fig. 3.9a, meaning it can be small enough to reduce the effect of C_{off}, slightly improving the phase-error and hence the harmonic rejection. Furthermore, we see that the output voltage is going to appear on C_{off} with a potential divider based on the ratio between $C_{off}//R_{big}$ and R_{small}, if we denote this attenuation factor as α_2, it is clear that $\alpha_2 < \alpha_1$ meaning the drain voltage on the off switch is going to be smaller, hence the V_{DS} non-linearity will be less significant than in Fig. 3.9a. Finally, since the V_{DS} non-linearity effect is reduced, the same linearity performance can be achieved with smaller switches than in Fig. 3.9a, reducing the parasitic C_{off} to further improve harmonic rejection. In conclusion, this topology has the potential to achieve both better harmonic rejection and linearity.

Finally, careful analysis of this topology while taking into account the different clock phases as well as the not shown quadrature-phase mixer will show that the full I/Q mixer presents a constant input impedance given by the following equation (assuming ideal R_{ON}= 0):

$$Z_{mixer\_in} = \left(R_1 + R_{big} + R_{small}\right)//(R_1 + R_{small})//\frac{R_1}{2} \tag{3.4}$$

The conversion gain is also given by the following equation (assuming ideal R_{ON} = 0):

$$Conversion\ Gain = \frac{R_{small} + R_{big}}{R_{small} + R_{big} + R_1} \cdot \frac{2}{\pi} \tag{3.5}$$

This topology was also designed in TSMC40nm thin-oxide CMOS technology, the mixer was loaded by a 250 pF capacitor to mimic the ADC's input capacitive loading. R_1, R_{big}, and R_{small} were sized to achieve the correct scaling while satisfying the input

impedance specification. The switches were sized large enough such that R_{on} would be much smaller than R_{small} such that their V_{DS} non-linearity will not be significant. In the end, both the linearity and harmonic rejection specification were achieved simultaneously. The only problem for this topology was the achieved IF bandwidth, which is still limited by the large value R_{CM} in combination with the succeeding ADC's input capacitance; this problem is shared by both topologies A and B. To mitigate for that, a third topology was devised. This third topology starts off with the same R_{CM} limitation for direct comparison with these topologies, but then introduces a trick to remove R_{CM} yielding an improved IF bandwidth.

3.4 MIXER TOPOLOGY C

A topology close to the final mixer proposed is presented in Fig. 3.11, as with the previous topologies, only the in-phase mixer is shown, the quadrature-phase mixer is again basically a copy of the same circuit with all the LO phases shifted by 90 degrees. In this topology, the two resistors R_{big} and R_{small} are placed in parallel again similar to the topology presented in Fig. 3.6, the difference here is that the switches are placed in parallel with the resistors instead of in series. The motive behind placing the switches in parallel is to reduce the effect of C_{off} as discussed in the previous mixer topology B. The switches again have their source terminals grounded, omitting V_{GS} non-linearity.

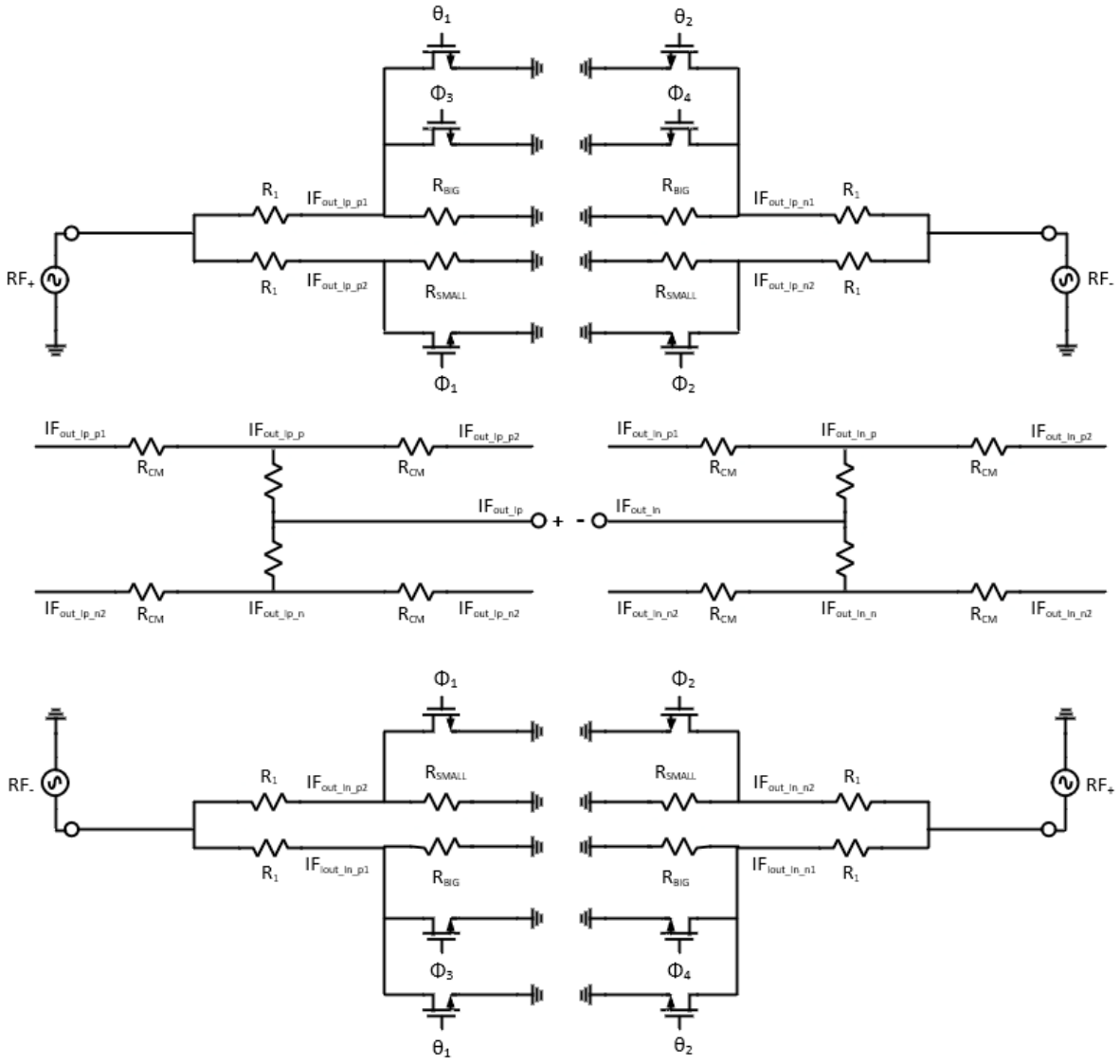

Figure 3.11: Mixer Topology C (In-Phase Mixer only)

The clocking scheme is shown in Fig. 3.12, employing 25%, 50%, and 75% duty-cycles. The operation is simple, when the mixing switch (ϕ_1) is "off", the mixing switch (ϕ_3) is "on". This results in R_{big} being shorted and the output voltage in that branch is nullified, while the other branch with R_{small} attenuates the input signal with a certain attenuation dependant on R_1 and R_{small}. On the other hand, when the mixing switch (ϕ_1) is "on", the mixing switch (ϕ_3) is "off". This results in R_{small} being shorted and the output voltage in that branch is nullified, while the other branch with R_{big} attenuates the input signal with a certain attenuation dependant on R_1 and R_{big}. R_{big}, R_{small}, and R_1 are chosen in a way such that the ratio between the two attenuations is $1+\sqrt{2}$ achieving harmonic rejection.

Similar to the previous topologies, four extra switches ($\theta_{1/2}$) are employed to nullify the output from one "half" of the topology to achieve an output waveform similar to the mixing waveform in Fig. 3.4, i.e., allow for a "negative" LO signal to be able to cancel out the RF feedthrough. The switches ($\theta_{1/2}$) and ($\phi_{3/4}$) could have been combined respectively into a single switch with their clocks OR'd together, however, this would result in 12.5% duty-cycles again, which are too fast for the intended technology kit for implementation. Finally, since the individual outputs are now split into two nodes, six summations are needed instead of just two, this is achieved with the summing network consisting of six R_{CM} on each side.

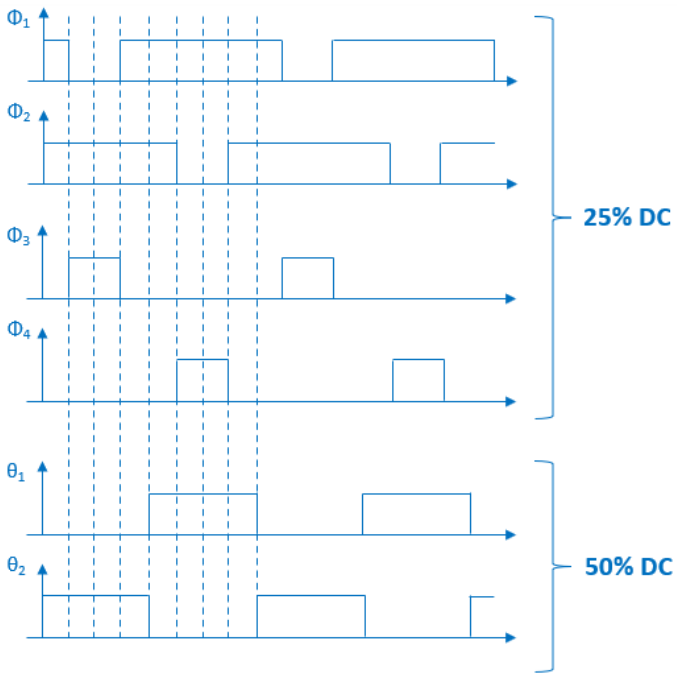

Figure 3.12: Mixer Topology C – Clocking Scheme

Finally, careful analysis of this topology while taking into account the different clock phases as well as the not shown quadrature-phase mixer will show that the full I/Q mixer presents a constant input impedance given by the following equation (assuming ideal $R_{ON} = 0$):

$$Z_{mixer\_in} = (R_1 + R_{small})//(R_1 + R_{big})//\frac{R_1}{6} \tag{3.6}$$

The conversion gain is also given by the following equation (assuming ideal $R_{ON} = 0$):

$$Conversion\ Gain = \frac{R_{big}}{R_{big} + R_1} \cdot \frac{2}{\pi} \tag{3.7}$$

The advantages of reducing the effect of C_{OFF} by connecting the switches in parallel is still present in this topology, meaning high linearity and harmonic rejection are achievable simultaneously. The full I/Q mixer circuit contains 24 switches which is more than topology B, so it will have somewhat more difficult clock routing in layout.

The main problem of topologies A and B is still present in this topology as well, namely the high output impedance limiting the IF bandwidth. In fact, this problem is even worse in this topology considering the fact that more summations are needed, increasing the output impedance from its original R_{CM} value. However, where this topology has an edge is that the summation network can be completely skipped to reach a much smaller output impedance, how to do so is highlighted in the next section.

3.4.1 Wideband Implementation

The goal of the summation network was to provide a point that cancels out the differential RF feedthrough while maintaining the common-mode IF signal. Careful analysis of the topology in Fig. 3.11 shows that such a node already exists in the mixer itself; namely, the grounded terminal of the scaling resistors. This is highlighted in Fig. 3.13 below. As with the previous topologies, only the in-phase mixer is shown, the quadrature-phase mixer is simply a copy of the exact same circuit with the LO phases all shifted 90 degrees. The clocking scheme remains the same as well as the general mixing operation remains the same, what changes is only the transfer function from the individual outputs to the summation node as well as a change in the output impedance of course.

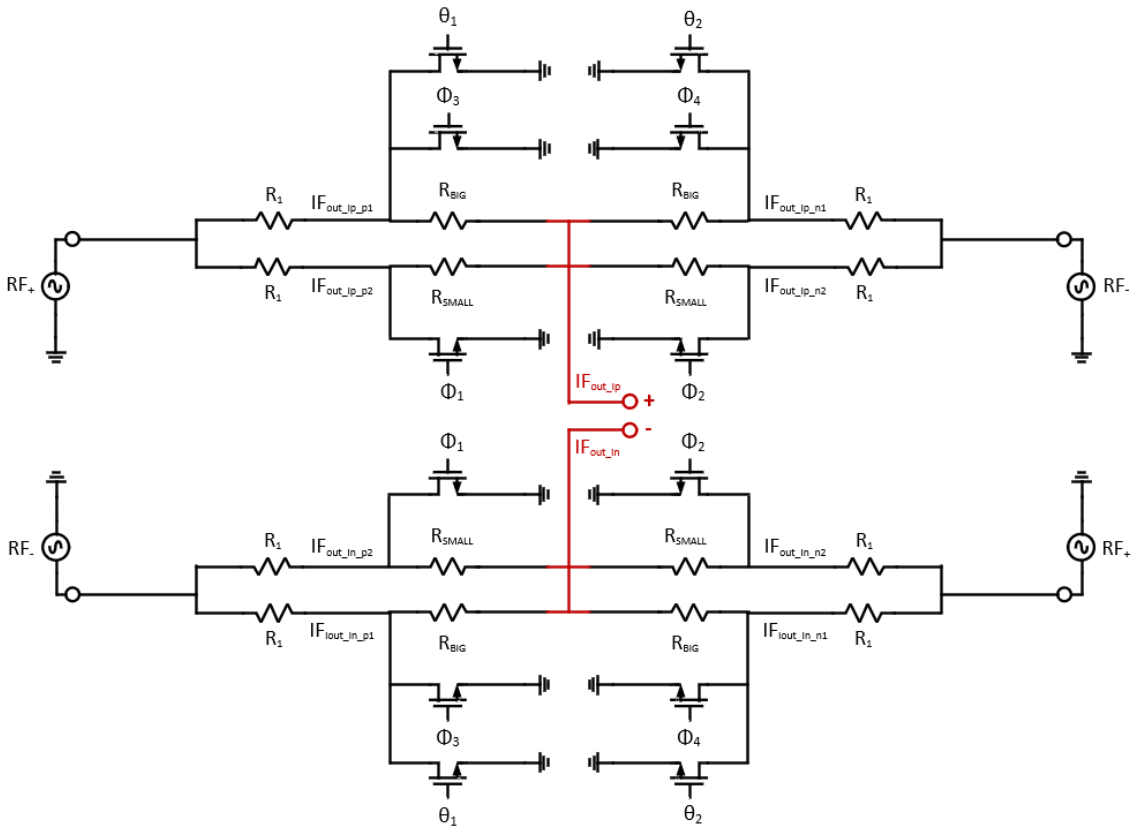

Figure 3.13: Mixer Topology C with Wideband Performance (In-Phase Mixer only)

The output impedance of the wideband topology can be expressed as following for one half (IF_{out_Ip} or IF_{out_In}) of the circuitry:

$$\begin{aligned} \boldsymbol{\varphi_1 \text{ or } \varphi_2 = \text{High}} \rightarrow \quad & Z_{mixer\_out} = \frac{R_{small}}{2} // R_{big} // \left(R_{big} + R_1\right) \\ \boldsymbol{\varphi_3 \text{ or } \varphi_4 = \text{High}} \rightarrow \quad & Z_{mixer\_out} = R_{small} // \frac{R_{big}}{2} // \left(R_{small} + R_1\right) \end{aligned} \tag{3.8}$$

This output impedance is much smaller than that of the previous topologies, this can be easily deduced by noting that R_{CM} had to be chosen at least ten times higher than R_{small} or R_{big} to not load the scaling factors in previous topologies. This significant reduction in output impedance allows for IF wideband operation.

However, the scaling equations are now not as simple since the differentiality is not fully satisfied anymore, in fact, the other half circuitry loads the scaling resistor R_{big} or R_{small}. To elaborate on that, consider the case when ϕ_1 is high in Fig. 3.13, if we assume that the switches' on resistance (R_{on}) is ideally zero and there are no off parasitic

capacitances (C_{off}), then the actual transfer function from the input RF_+ to IF_{out_Ip} is given by the following equation:

$$TF = \frac{R_{big} // \frac{R_{small}}{2}}{R_1 + R_{big} + R_{big} // \frac{R_{small}}{2}} \tag{3.9}$$

Of course, with real values of R_{on} and C_{off}, the transfer function becomes much more complicated, so much so that they are not that intuitive in designing. Instead, as an approximation, sizing is calculated where R_{on} and C_{off} are considered ideal, and then the correct sizing to compensate for their existence is found through perturbations around that solution in simulation.

This topology was also designed in TSMC40nm thin-oxide CMOS technology, the mixer was loaded by a 250 pF capacitor to mimic the ADC's input capacitive loading, R_1, R_{big}, and R_{small} were sized to achieve the correct scaling while satisfying the input impedance specification. In the end, both the linearity and harmonic rejection specification were achieved simultaneously while maintaining a wide IF bandwidth.

Ideal schematic simulations indicate that this topology is the most promising in terms of harmonic rejection, linearity, and bandwidth for the given application. Consequently, it was chosen for the final mixer implementation. The next chapter deals with the real implementation of the above circuitry, including clock generation, clock buffering, level-shifting, as well as loading of the I/O pads with ESD protection.

4 FINAL CIRCUIT IMPLEMENTATION

4.1 CLOCKING

Since the mixer topology was already decided upon on, the first step towards a full implementation of the mixer was to provide it with real clocking. This involves three steps; clock-generation, duty-cycle control, and level-shifting (if necessary). These are each discussed in the follow subsections. All blocks were implemented in TSMC40nm thin oxide CMOS technology.

4.1.1 Clock Generator

To fast-track the implementation process, the clock-generator block was borrowed from ELCA's internal design library. This clock-generator block was originally designed and implemented by Mohammad Reza Beikmirza at ELCA. This block is briefly described here to make the documentation of the mixer's implementation complete. The clock-generator block with its sub-blocks is presented in Fig. 4.1.

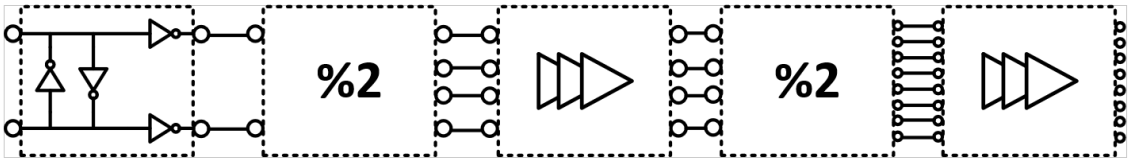

Figure 4.1: Clock-Generator Block Diagram

The clock-generator is fed with a differential clock at a frequency of $4f_{LO}$ which is 14 GHz. The clock-generator produces 8 phases at a clock frequency of 3.5 GHz having a 50% duty-cycle ranging between 0V and 1.1V. As can be seen, the block employs a phase-aligner, two separate divide-by-2 stages to generate the 8 phases, and some buffers. The divide-by-2 stages are implemented using digital latches of the C^2MOS topology. The unloaded generated output clock signals are shown in Fig. 4.2, as can be seen, the unloaded rise/fall-time was around 5 pS. The clock-generator has a power consumption of 9.28 mW.

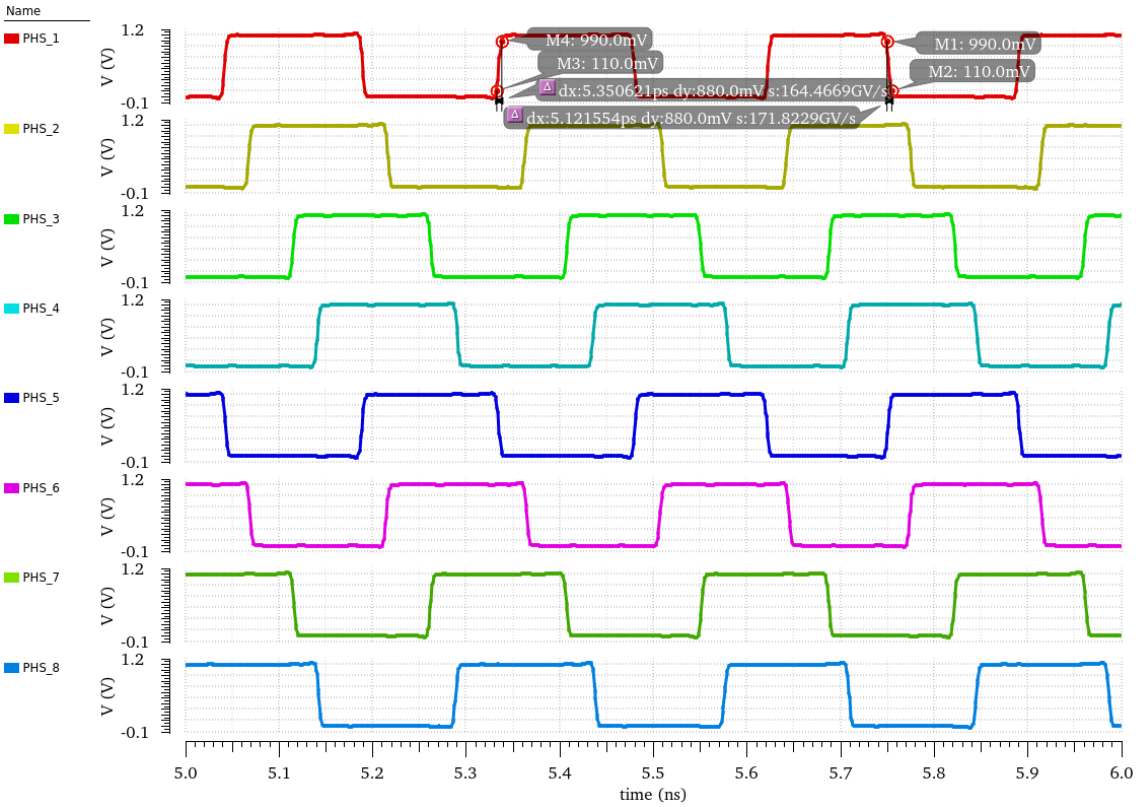

Figure 4.2: Unloaded Clock-Generator Waveforms

4.1.2 Duty-Cycle Control

This section discusses the digital circuitry that creates the required duty-cycle waveforms from the clock-generator presented in the previous section. In the following two sub-sections, the duty-cycle generator required in both the AC configuration and the DC-biased configuration of the mixer will be presented. As discussed in Chapter 1, the input to our mixer is originally intended to be purely AC through a capacitive attenuation stage so as to not draw any DC power. However, for reasons that will be elaborated on in the next section, a need for a DC-biased configuration arises.

Duty-Cycle Control for DC-Biased Configuration

The mixer is designed in TSMC40nm thin-oxide CMOS technology with transistors that operate in the 1.1V domain. Consequently, the intermediate signals appearing at the drain of the mixing switches are confined between 0V and 1.1V. This means that in the DC-biased configuration of the mixer, the LO clocking waveforms need to swing between 0V and 1.1V, this is readily available from the clock-generator block discussed in the previous section. Hence, the only remaining addition is the digital circuitry

creating the 25% and 75% duty-cycle LO waveforms, and the consequent buffering to be able to drive the mixing switches. This digital circuitry is presented in Fig. 4.3.

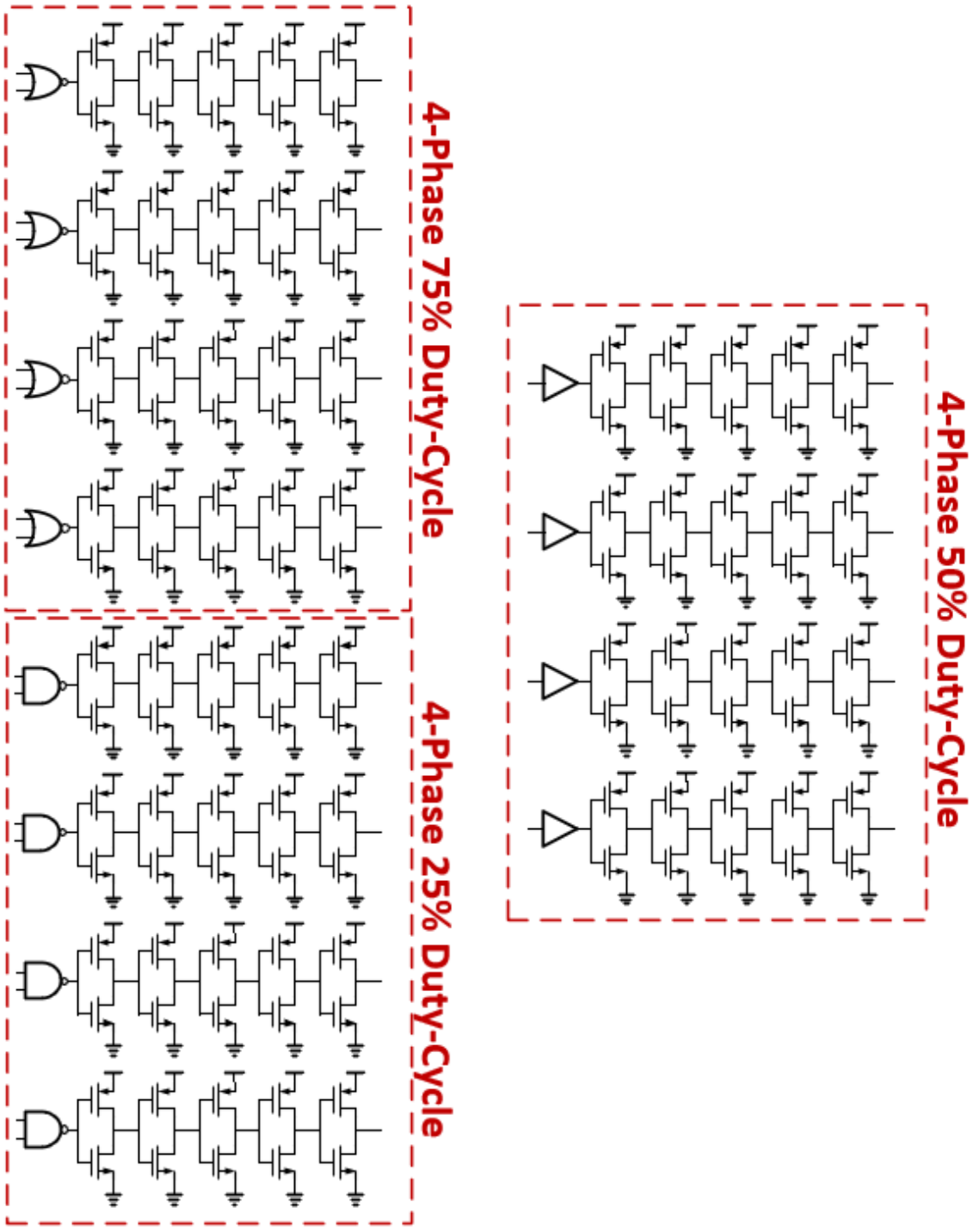

Figure 4.3: Duty-Cycle Generation and Buffering – DC Mixer Implementation

The 75% duty-cycle waveforms are created using NOR gates while the 25% duty-cycle waveforms are created using NAND gates. The logic gates are used from TSMC standard logic library, they provide almost identical delays for both NAND and NOR

gates which is their main advantage. The only problem with the standard logic gates is that they are not symmetric relative to their input signals; however, swapping the inputs did not result in any significant performance changes for the whole mixer, so they were deemed good enough to save on design time. Ideally, input-symmetric NAND and NOR gates can be designed to ensure perfect balancing with respect to the gate's inputs.

The buffering is implemented using a tapered inverter chain with a tapering factor of 3, it was found that the ideal number of stages was 5, yielding an inverting buffer chain. This explains why the 75% duty-cycle waveforms are created from NOR gates instead of NAND gates and vice versa. Finally, the 50% duty-cycle clocks were buffered as well using the same buffering chain, the first stage is a buffer from the TSMC standard logic library, it provides almost identical delay to the NOR and NAND gates so that all the duty-cycle waveforms maintain the correct phase relations. The final loaded LO clocking waveforms are presented in Fig. 4.4. As can be seen, 4 phases were created within one RF cycle as is needed for the whole I/Q mixer LO clocking. Finally, the rise/fall-time simulated was around 10 pS. The clock-generator and duty-cycle generator combined have a power consumption 21.25 mW.

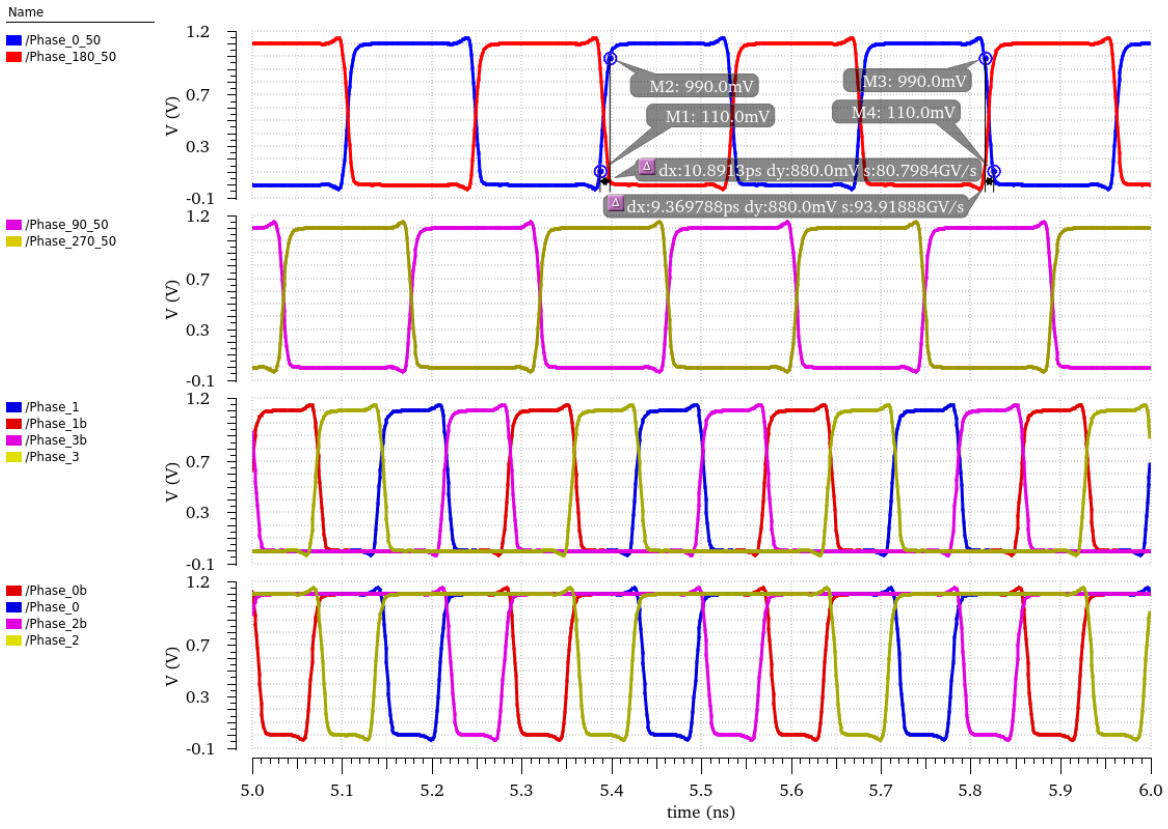

Figure 4.4: Final Loaded LO Waveforms – DC Mixer Implementation

Duty-Cycle Control for AC Configuration

The mixer is designed in TSMC40nm thin-oxide CMOS technology with transistors that operate with a maximum V_{GS}, V_{GD}, or V_{DS} of 1.1V. Consequently, the intermediate signals appearing at the drain of the mixing switches should be limited between -0.55V and 0.55V. This means that in the AC configuration of the mixer, the LO clocking waveforms will need to switch between -1.1V and 1.1V. This causes >1.1V V_{GD} when the mixing switches are off; however, since these are for only a maximum 12.5% duty-cycle, they were not deemed to be a severe reliability problem.

The larger voltage swing of the clock waveforms requires a level shifter block to be added after the duty-cycle generation, the level shifter implementation is discussed in the next section. In this sub-section, only the duty-cycle control part of the AC configuration is presented. The duty-cycle control for the AC configuration is very similar to the DC-biased configuration, the only difference is that the buffers are now driving a level shifter, which is a much smaller load than the mixer's switches. Hence, the large buffers were replaced by smaller buffers from the TSMC standard library, this is presented in Fig. 4.5. The buffers were tapered with a factor of 2. The larger buffers needed to drive the mixer's switches are now placed after the level shifter.

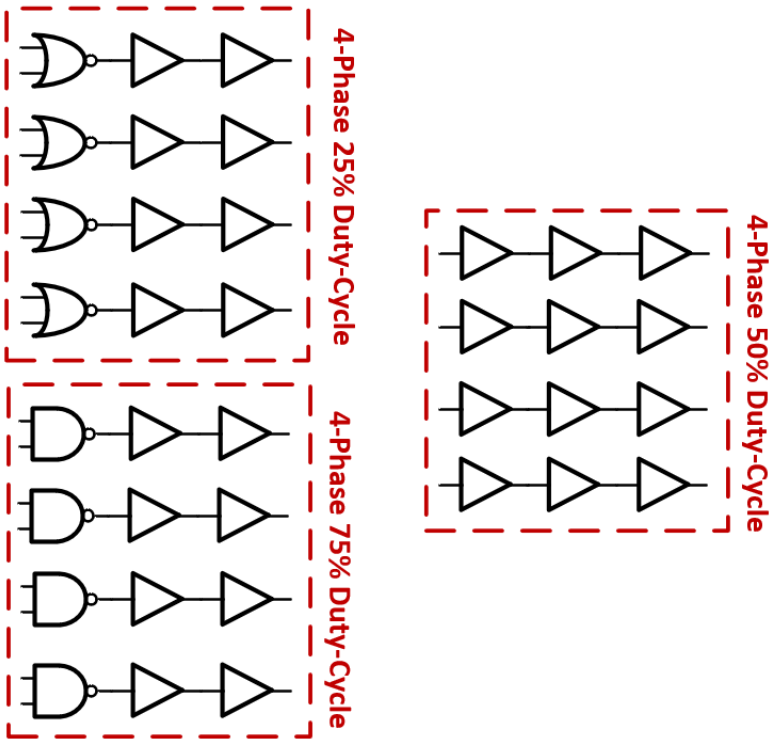

Figure 4.5: Duty-Cycle Generation and Buffering – AC Mixer Implementation

4.1.3 Level Shifter

The core of the level shifter block that was designed in this thesis work is shown in Fig. 4.6. It is a shift-down variation on a shift-up level shifter design originally proposed by Rob Bootsman and Ossama El Boustani at ELCA. The operation principle is simple, LO_p and LO_n are input differential waveforms from 0V to 1.1V, either both are 50% duty-cycle, or one is 25% duty-cycle and the other is its inverse; namely, a 75% duty-cycle. VDD_H and VDD_L are 1.1V and -1.1V respectively. $M_{3/4/5/6}$ are acting as cascodes and are always connected to 0V. $M_{9/10}$ are pulling the upper and center nodes to 1.1V according to LO_p and LO_n. $M_{1/2}$ act as a cross-coupled positive feedback loop where they switch LO_{p_L} and LO_{n_L} between 0V and -1.1V. The two capacitors couple the LO inputs onto the gates of $M_{1/2}$ to increase the speed of the cross-coupled settling, similarly, $M_{7/8}$ are used to speed up the discharging of the upper nodes to ground when $M_{9/10}$ are turned off, improving the total circuit speed. In conclusion, if LO_p and LO_n switch between 1.1V and 0V, then LO_{p_L} and LO_{n_L} are switching between 0V and -1.1V. In Fig. 4.6, all NMOS transistor bulks are connected to VDD_L while all PMOS transistor bulks are connected to VDD_H.

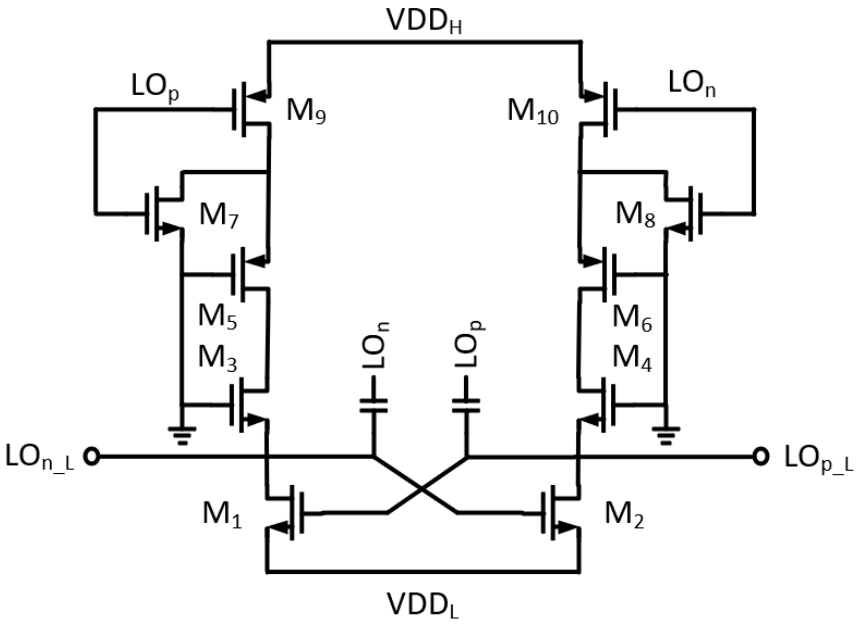

Figure 4.6: Level Shifter Core

The resulting waveforms from the level shifter core can be used to drive the buffers that will result in the final intended LO swing between 1.1V and -1.1V, this is presented in Fig. 4.7, where the complete level shifter block along with the buffers are shown.

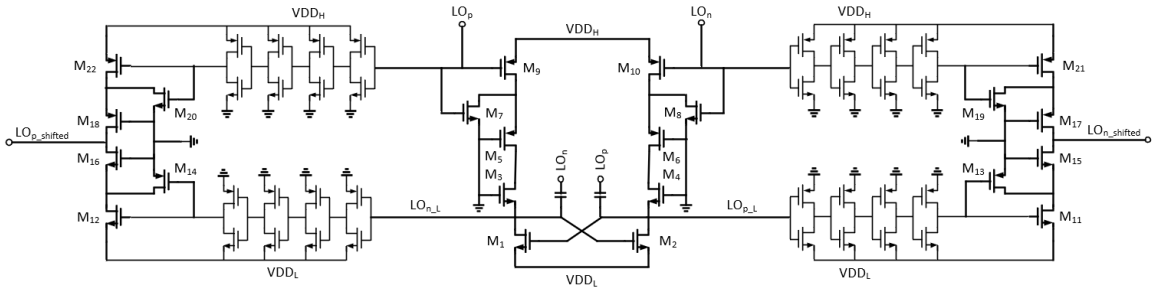

Figure 4.7: Complete Level Shifter with Buffers

The operation is as follows, there are two tapered inverter chains with a tapering factor of 3. These are the same first four buffer stages used in the DC-biased configuration's buffering chain, the only difference is the last buffer stage, since that needs to combine both $LO_{p/n}$ and LO_{p_L/n_L} into a single clock $LO_{p\_shifted/n\_shifted}$ swinging between -1.1V and 1.1V. $M_{15/16/17/18}$ are cascode transistors that are there to divide the voltage drop so that it is a maximum difference of 1.1V. $M_{13/14/19/20}$ are simply there to help pull the intermediate nodes to their correct voltages when the clock is switching, this increases the circuit speed meaning faster rise/fall-time. To equate the delays of the buffer chains, the NMOS transistor bulks of the upper buffer chain needs to be connected to 0V instead of VDD_L, meaning these NMOS transistors will have to be in a separate well. The final loaded and level shifted 4 phase LO waveforms for the whole I/Q mixer are shown in Fig. 4.8, the simulated rise/fall-time was around 18 pS. The clock-generator, duty-cycle generator, and level shifter have a total power consumption of 33.4 mW.

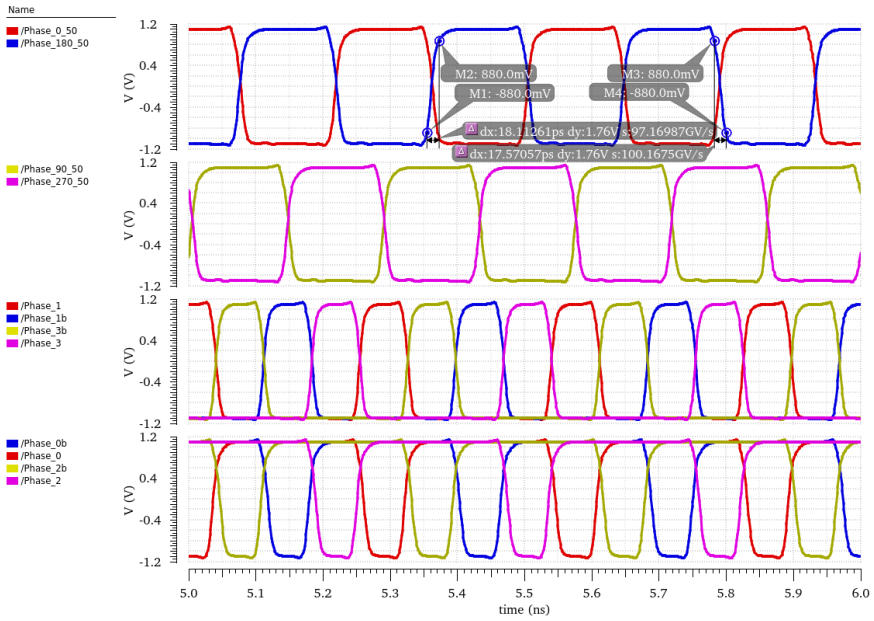

Figure 4.8: Final Loaded Level Shifted LO Waveforms – AC Mixer Implementation

4.2 FULL I/Q MIXER IMPLEMENTATION

This section is divided into two subsections; the first presents the AC configuration of the voltage-domain mixer design and the reason it was not feasible to implement using the TSMC40nm design kit. The second section presents the final DC-biased configuration of the voltage-domain mixer design and its simulated performance.

4.2.1 AC Configuration

The I/Q mixer design in the AC configuration is presented in Fig. 4.9.

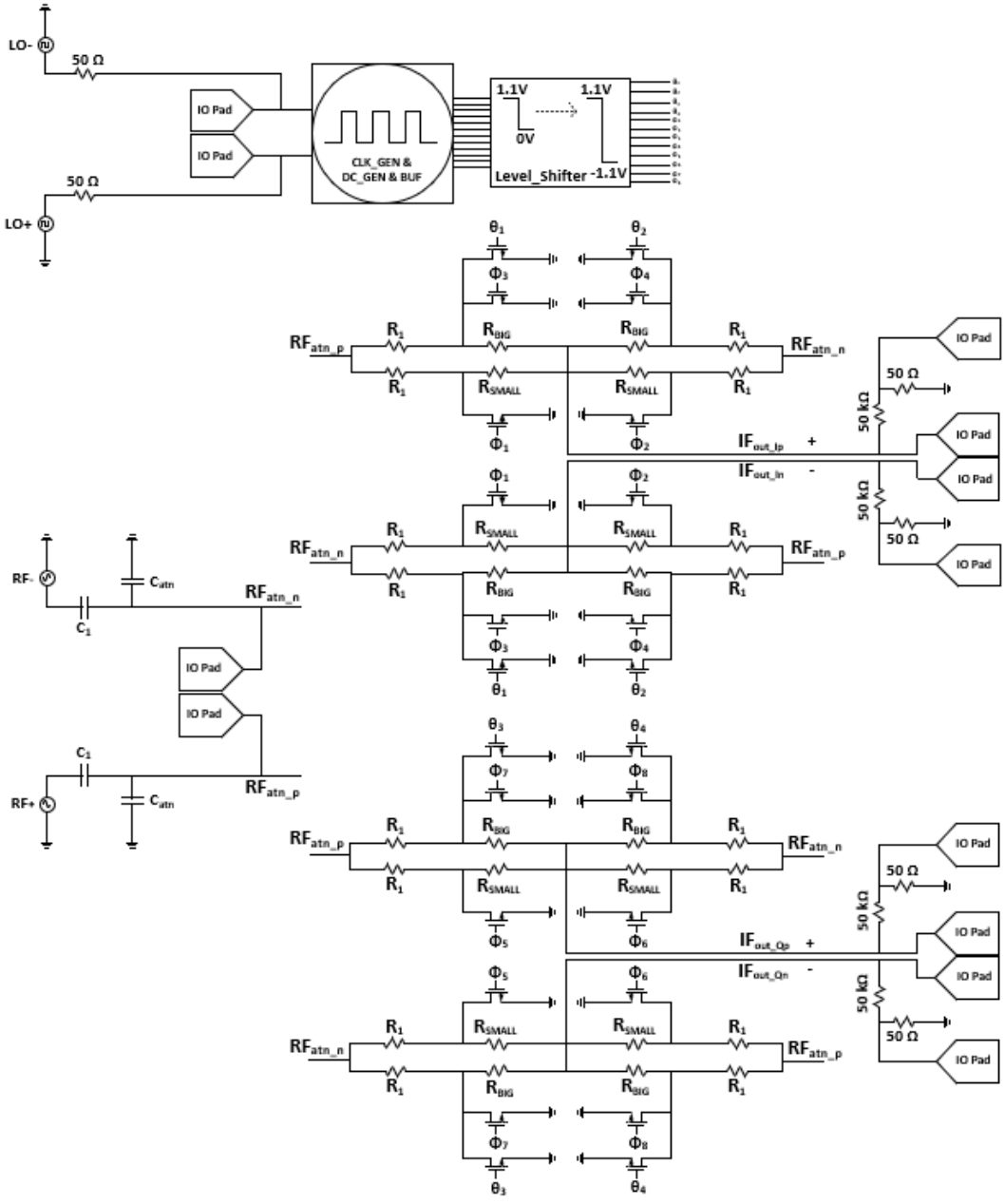

Figure 4.9: Full I/Q Mixer – AC Configuration

As can be seen in Fig. 4.9, the differential I/Q output of the mixer is fed to two I/O pads (with ESD protection) each, one is directly connected to the output and the other is connected through a 60 dB attenuation potential divider. The directly connected I/O pad has a loading capacitor of 300 fF; this is pretty close to the expected ADC's capacitive loading, so this I/O pad can mimic the ADC loading. The I/O pad adds some non-linearity of its own considering its capacitance is voltage dependant; however, it is low enough such that the degradation in linearity performance is not significant. This I/O pad is expected to be connected to an oscilloscope with high-input impedance. The second I/O pad is intended to be connected to a spectrum analyser with a 50Ω input impedance. Since the mixer is not designed to drive a resistive load, the 50Ω input impedance would completely overload the mixer and drop its output voltage swing. This would block the linearity measurements to be done at the output voltage swing of interest. Instead, the mixer's output is connected to this pad through a potential divider, this insures a much lower loading at the mixer's output such that its output swing does not drop significantly, while still providing a 50Ω output impedance to the spectrum analyser. Since the potential divider is pretty linear, then the measured linearity performance after attenuation can be traced back to the intended voltage swing needed to drive the ADC.

The RF input signal and the LO clocks are both fed through I/O pads as well. The RF input is first attenuated through a capacitive divider. For brevity, DC voltage supply and ground pads were omitted from Fig. 4.9; however, they are present in the actual implementation. As discussed in the previous sections, the original mixer's input signal was aimed to be purely AC such as that in Fig. 4.9 to not consume any DC power. A capacitive divider is used to avoid any RF power consumption in the attenuation stage as well.

The main problem with this however, is that TSMC40nm I/O pads do not allow for negative voltages that are required in the AC configuration. This was discovered rather late in the thesis work timeline, so there was not enough time to dedicate to the design of custom I/O pads (with ESD protection). Instead, the DC-biased configuration of the mixer was devised. It consumes DC power and has a lower input impedance as will be seen in the next section, so its total power consumption is not similar to the AC configuration. However, in terms of all other performance parameters, they are almost

identical. Therefore, the DC-biased configuration was deemed as a close enough first demonstrator of the novel mixer topology that is feasible to implement in TSMC40nm thin-oxide CMOS technology. So, the focus will now shift onto the mixer design with the DC-biased configuration as the main focus of this thesis work.

4.2.2 DC-biased Configuration

The final I/Q mixer design in the DC-biased configuration is presented in Fig. 4.10.

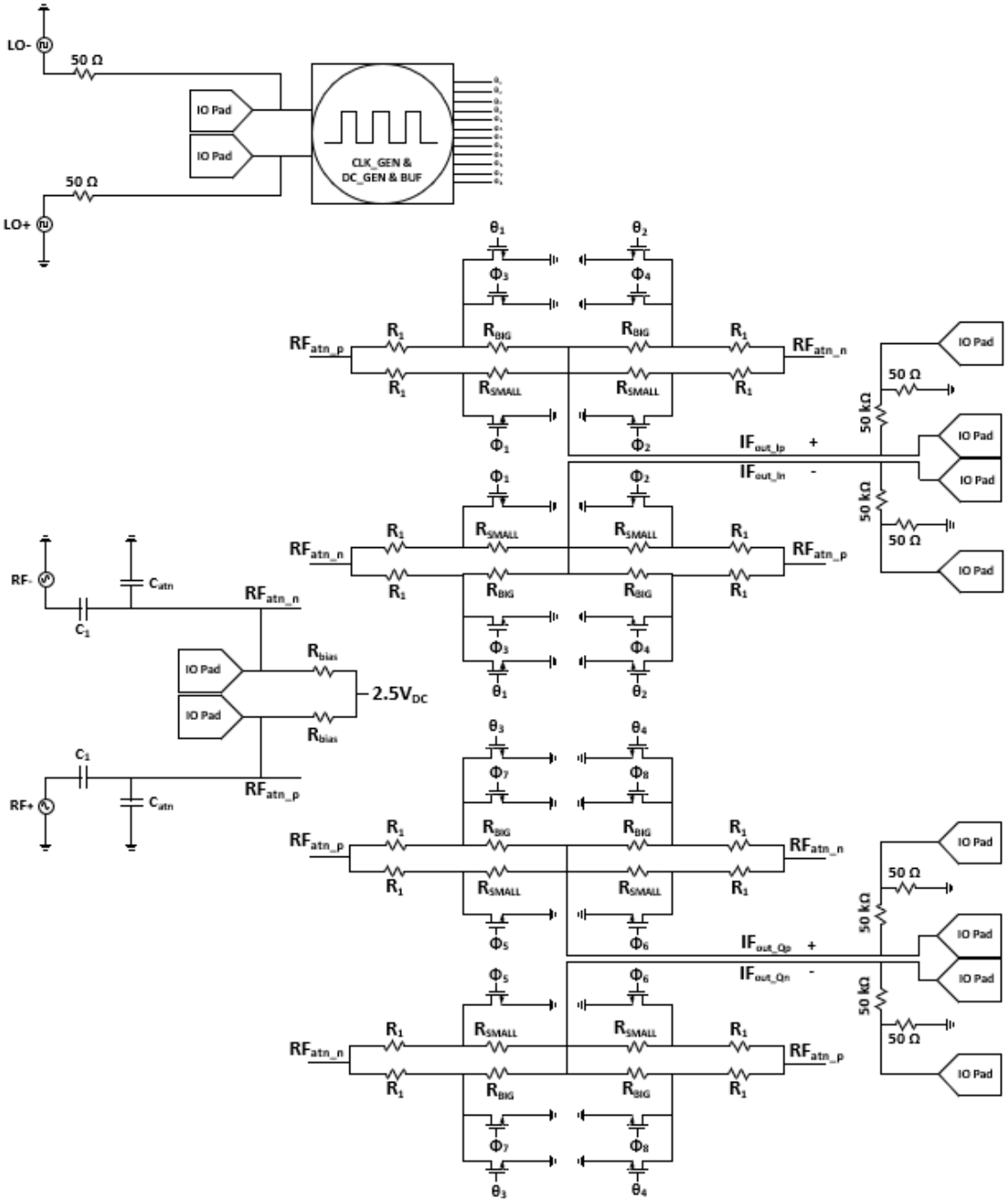

Figure 4.10: Full I/Q Mixer – DC-biased Configuration

The I/O pad setup is similar to the previously discussed AC configuration of the mixer. The only difference is that now since negative supply voltages are not needed, the TSMC40nm I/O pads can be used. In addition, the level shifters are no longer required to shift the LO clocks to a negative supply. In this DC-biased configuration, the RF input is now AC coupled to the mixer with a super-imposed DC shift through the biasing resistor R_{bias}. The attenuation stage is still capacitive so that stage does not consume any RF power.

The sizing of the mixer had to be changed to account for the smaller clock peak-to-peak swing in the DC implementation. The smaller clock peak-to-peak swing effectively lowers the switches' off impedance, affecting the harmonic rejection scaling as well as the conversion gain. Thus, to maintain the same harmonic rejection performance as in the AC configuration, the resistors had to be sized down. This lowered the input impedance R_{mixer_in} of the DC coupled mixer to 250Ω instead of 290Ω in the AC configuration of the mixer. In addition, the DC configuration now has a biasing resistor R_{bias} in parallel with the mixer's input impedance. As mentioned in Chapter 1, $R_{bias} \approx R_{mixer\_in} = 250\Omega$ was chosen as a good trade-off between attenuating the super-imposed DC shift too much and lowering the input impedance too much causing more power consumption. In conclusion, the total input impedance now presented after the attenuation stage is $R_{bias}//R_{mixer\_in}$ is 125Ω.

This lower input impedance consumes a total of 13.96 mW RF power. For comparison, the AC configuration consumed 6.8 mW RF power. Furthermore, the DC-biased configuration of the mixer also draws a DC power of 25 mW that is dissipated in both R_{bias} and R_{mixer_in}. In contrast, the AC configuration of the mixer consumed no DC power at all. However, the clocking power consumption of the DC-biased configuration was ~10 mW smaller than in the AC configuration as was shown in the previous sections. The power consumption of this DC-biased configuration then is not representative of the original AC configuration of the mixer. As for the remaining performance parameters, they were nearly identical, and those will be discussed next. The DC-biased configuration of the mixer was fully designed, simulated, and implemented in TSMC40nm thin-oxide CMOS technology.

Fig. 4.11 shows the simulated bandwidth for the I and Q IF outputs of the DC-biased configuration of the mixer, as can be seen, the 1dB bandwidth is 440 MHz and the 3 dB bandwidth is 800 MHz. In this work, the bandwidth is limited by the sizing of the resistors, which in turn are limited by the parasitic capacitors added by the mixing switches, if the topology is implemented in a more advanced technology node with less parasitics, the bandwidth will be improved even further.

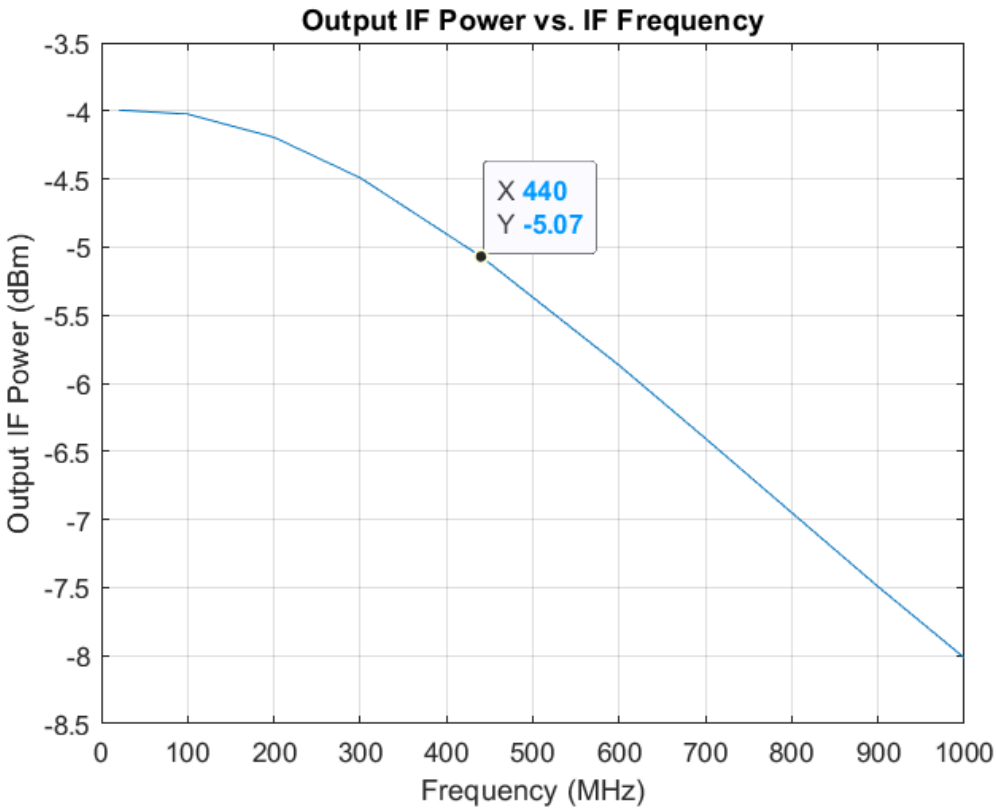

Figure 4.11: Output IF Power vs. IF Frequency

Fig. 4.12 presents the final harmonic rejection (HR3) performance vs. IF frequency. The required >40 dB harmonic rejection is achieved within the 1dB bandwidth of 440 MHz. The dependence of the harmonic rejection ratio on the IF frequency is due to the parasitic capacitances of the switches having an effect on both the scaling and phase relation of the harmonic rejection waveform. This is another performance specification that can be improved by moving to a more advanced technology node with less parasitics. Harmonic rejection was simulated at f_{LO} = 3.5 GHz by taking the difference between inputting a signal at a certain f_{IN_1} resulting in a specific f_{IF} and inputting the same signal but with $f_{IN\_2} = 3f_{LO} + f_{IF}$. In this way, the down-converted IF frequency does not change, but the LO harmonic responsible for down-conversions changes.

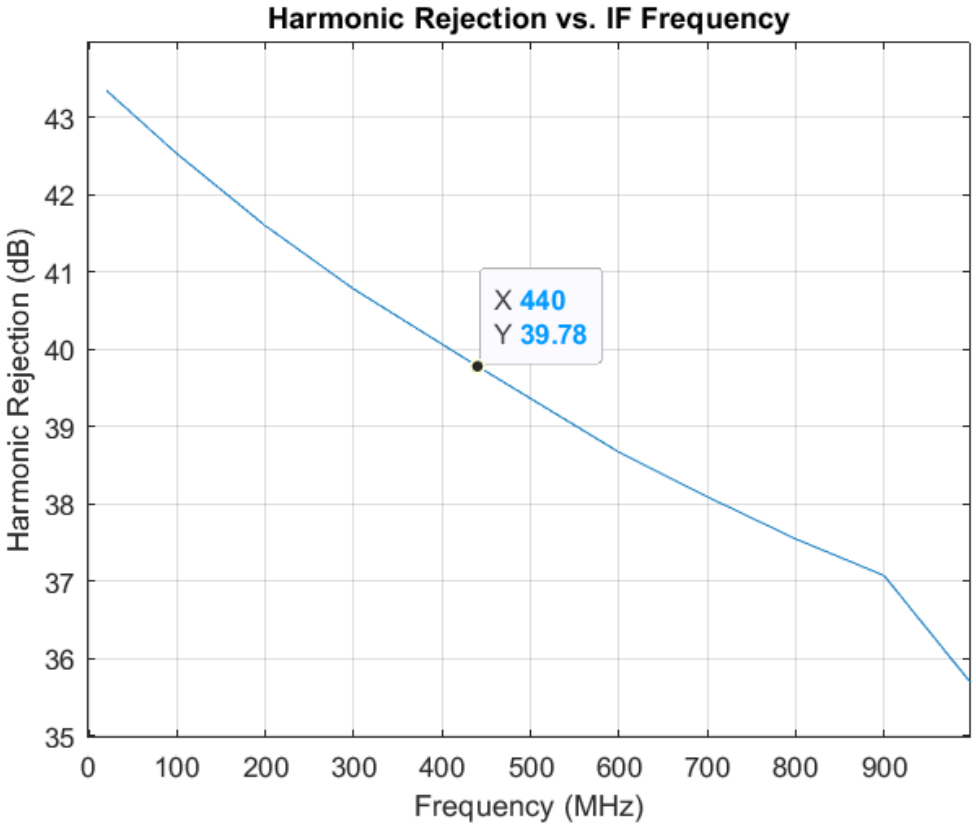

Figure 4.12: Harmonic Rejection vs. IF Frequency

Fig. 4.13 shows the linearity performance of the mixer, a two-tone signal is provided to the input of the mixer and its related output spectrum is as shown. We note that the IM3 linearity performance is -62.4 dBc. The second dominant spur after the IM3 non-linearity components are two other spurs around the third harmonic of the LO waveform, these two spurs are at -63.1 dBc. These spurs arise from the non-ideal clock, mostly due to duty-cycle errors. When driving the mixer circuitry with ideal clocks, these two spurs are much lower than the IM3 non-linearity components as to be expected. Therefore, moving to a more advanced technology node would allow for faster clock and duty-cycle generators that would decrease these two spur components. The IM3 performance did not meet the -65 dBc IM3 specification set out at the start of the project, however, it should be noted that that specification included a 10 dB margin. Furthermore, a more advanced technology node with fewer parasitics provides smaller C_{OFF} and R_{ON}, improving linearity performance by reducing secondary sources of non-linearity such as V_{DS} non-linearity. All in all, this work's IM3 performance was deemed good enough for a first demonstrator of the novel mixer topology. It is still much better than state-of-art linearity performance of voltage-domain mixers in other publications.

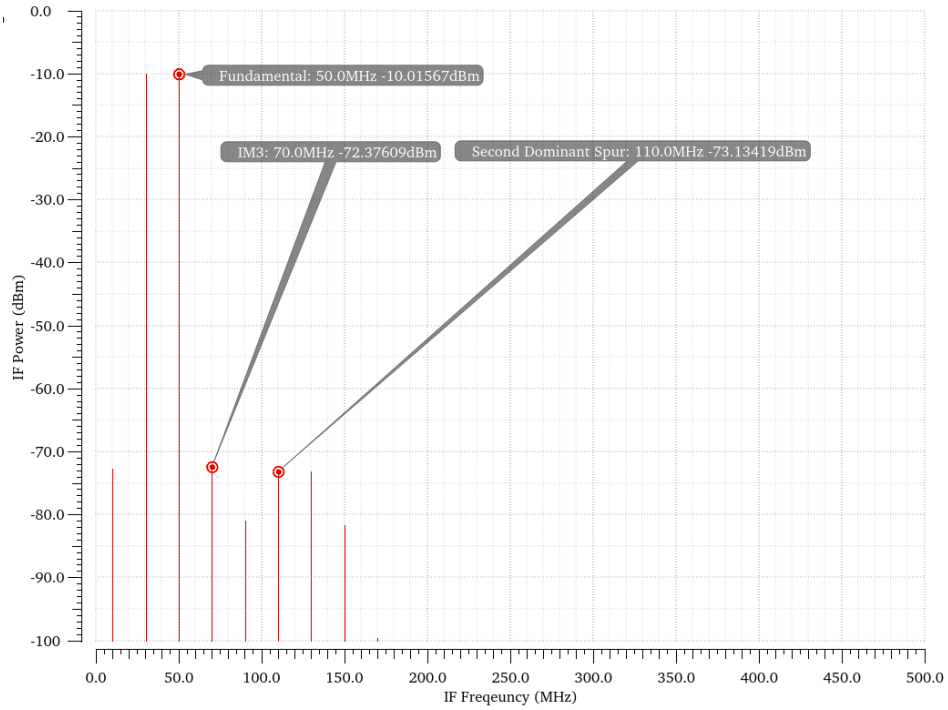

Figure 4.13: IF Output Spectrum – Two-Tone Simulation

Referring back to equation 3.9, a rough estimate of the conversion gain without taking the parasitics into account can be calculated using the following equation:

$$Conversion\ Gain \approx \frac{R_{big} // \frac{R_{small}}{2}}{R_1 + R_{big} + R_{big} // \frac{R_{small}}{2}} \cdot \frac{2}{\pi} \qquad (4.1)$$

Where the $\frac{2}{\pi}$ factor is the gain resulting from the differential LO square-wave waveform. In our mixer design: R_{big} = 3kΩ, R_{small} =1.75kΩ, and R_1 = 2kΩ. This results in an approximate conversion gain of -22.3 dB. The conversion gain was actually -22.5 dB in simulation, the difference is due to the inclusion of parasitics. The conversion gain is much lower than the ideal -4 dB theoretical limit. However, as mentioned before, this is not a problem for our application as this mixer is to be employed in an observation receiver. The high input-impedance specification forces R_1 to be large, to improve conversion gain R_{big} and R_{small} will have to be made larger, but that would increase output impedance and hence degrade IF bandwidth. Hence, the high-input impedance specification that is unique to our application forces this low conversion gain. Furthermore, as a voltage-domain mixer, the signal swing on the active devices at the intermediate nodes needs to be assured to not go beyond 1.1V, however, since the mixing operation produces both the sum and difference frequencies at the intermediate

nodes, half of the swing is unfortunately lost to the sum frequency, resulting in a relatively low conversion gain. In principle, explicit capacitors can be added at the intermediate nodes to filter out the sum frequency, but then they would also introduce phase-error to the harmonic rejection operation.

To the best of our knowledge, the best reported performance for a voltage-domain mixer is by K. Kibaroglu in [14]. A comparison table is provided below that summarizes the performance of our proposed voltage-domain mixer topology compared to the mixer of [14]. As can be seen, the novel topology in this thesis work provides significant improvements across all specifications except conversion gain, which is not an important specification for our observation receiver application as has been discussed before. For completion, the table also includes comparison with current-domain mixers [13] and [15], as well as a commercial high-end passive mixer from Marki Microwave for high linearity applications [16].

Table 4.1 – Performance Comparison

	Thesis Work	**[14]**	**[13]**	**[15]**	**[16]**
CMOS Technology	TSMC40nm	TSMC32nm	1P9M65nm	TSMC28nm HPC	GaAs MMIC
Mixer Domain	Voltage	Voltage	Current	Current	-
Mixer Type	I/Q	I Only	I/Q	I/Q	I/Q
IF Loading	300 fF	50Ω // 20 pF	-	50Ω	50Ω
Input Impedance	125Ω	50Ω	50Ω	50Ω	50Ω
RF Frequency	3.5 GHz	3.5 GHz	2.4 GHz	2 GHz	3.5 GHz
Conversion Gain	-22.5 dB	-7.5 dB	70 dB	32.4 dB	8.5 dB
3dB IF Bandwidth	800 MHz	200 MHz	10 MHz	260 MHz	7 GHz
Harmonic Rejection	40 dB	40 dB	35 dB	No HR	No HR
OIP3 Linearity	21.2 dBm	12.3 dBm	3 dBm	20.4 dBm	27.5 dBm
OIP3 Linearity	8.2 dBV	-0.7 dBV	-10 dBV	7.4 dBV	14.5 dBV
Output IF Power	-4 dBm	-	-	-	-
Output Swing	0.5 V_{PP}	-	-	-	-
IF Output Swing	0.4 V_{PP}	-	-	-	-
RF Power	13.96 mW	-	-	-	-
LO Power	22.94 mW	-	-	-	-
DC Power	25 mW	-	-	-	-
Total Power	61.9 mW	77.5 mW	70 mW	37.2 mW	1W

It must be noted that our harmonic rejection performance is reported only for the 3rd harmonic. Unfortunately, the RC phase-error introduced by the switches' parasitics is significantly different enough between the 3rd and the 5th harmonic that the 5th harmonic rejection ratio did not meet the specification. This can be improved by either lowering the switches' parasitics by moving to a more advanced node, or by reducing the resistances by reducing the impedance level of the mixer and drawing more RF power.

5 CONCLUSIONS

This thesis work provided a novel circuit topology for an extremely-linear wideband voltage-domain harmonic-reject mixer implemented in TSMC40nm. The topology's key advantage is the cancellation of the V_{GS} non-linearity source that dominates the linearity performance of conventional voltage-domain mixers. A complete I/Q mixer with realistic clocking, buffering, as well as I/O pad loading was designed as a practical proof-of-concept for this topology with performance results exceeding by far what is available in state-of-the-art publications or open literature.

5.1 FUTURE WORK

The direct next step for this thesis work is the physical layout implementation, fabrication, and the subsequent measuring of the performance. Most likely, the measured performance will somewhat be worse than that predicted by simulations. However, as the performance improvements achieved in simulations compared to those reported in state-of-the-art publications are quite significant, there is a good chance for a competitive edge over the state-of-the-art performance.

The longer-term improvement for this work is expected to follow from the implementation of the topology in a more advanced technology node. As was demonstrated previously, all the specification parameters of this mixer topology directly improve with the CMOS switching speeds and reduced device capacitances, especially the 5^{th} harmonic rejection which is currently lacking in performance in this implementation. When transitioning to a more advanced CMOS technology node, the topology will become even more suitable for serving extremely wideband observation receiver applications that formed the motivation of this research work.

Logically, the implementation of the full correction loop is the ultimate end goal of this project, such a complete implementation could significantly improve base station systems' performance at a reduced cost, while on a global scale saving significant amounts of power and CO_2 emissions.

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