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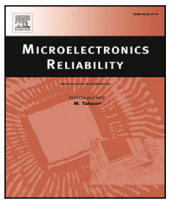

Research paper

Exploring the use of extreme temperatures to facilitate fault propagation in ReRAMs☆

T.S. Copetti [a,*], A. Chordia [a], M. Fieback [b], M. Taouil [b], S. Hamdioui [b], L.M. Bolzani Poehls [c]

[a] RWTH Aachen University, Germany
[b] Delft University of Technology, Netherlands
[c] IHP - Leibniz Institute for High Performance Microelectronics, Germany

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ABSTRACT

Resistive Random-Access Memories (ReRAMs) represent a promising candidate to complement and/or replace CMOS-based memories adopted in several emerging applications. Despite all their advantages – mainly CMOS process compatibility, zero standby power, and high scalability and density – the use of ReRAMs in real applications depends on guaranteeing their quality after manufacturing. As observed in CMOS-based memories, ReRAMs are also susceptible to manufacturing deviations, including defects and process variations, that can cause faulty behaviors different from those observed in CMOS technology, increasing not only the manufacturing test complexity but also the time required to perform the test. In this context, this paper proposes to study the use of temperature to facilitate fault propagation in ReRAMs, reducing the required test time. A case study composed of a 3x3 word-based ReRAM with peripheral circuitry implemented based on a 130 nm Predictive Technology Model (PTM) library was adopted. During the proposed study, a total of 17 defects were injected in different positions of the ReRAM cell, and their respective faulty behavior was classified into conventional and unique faults, considering three different temperatures (25, 100, and -40 °C). The obtained results show that the temperature can, depending on the position of the defect, facilitate fault propagation, which reduces the time required for performing manufacturing testing.

1. Introduction

As technology nodes reach sizes of a few nanometers, the miniaturization of Integrated Circuits (ICs) has become challenging. With the parallel increasing demand for emerging applications requiring high performance with rigid area and power consumption constraints, significant challenges arise for device technology and computer architecture [1]. Reliability, leakage, and cost represent the device technology walls that need to be addressed [1]. In addition, memory, power, and Instruction Level Parallelism (ILP) walls affect computer architectures, posing limits to von Neumann architecture [1]. In this scenario, memristive devices represent one of the most promising candidates to complement and/or replace CMOS technology due to their CMOS manufacturing process compatibility, zero standby power consumption, as well as high scalability and density [1,2]. In addition, memristive devices are able to implement not only memory but also computing elements [1]. When adopted as memory elements, a block composed of memristive devices is named Resistive Random-Access Memory (ReRAM), a non-volatile memory [3]. Nevertheless, the use of these emerging memories depends on being able to guarantee their quality after manufacturing as well as their reliability during their lifetime. Despite the lack of information regarding realistic manufacturing deviations, literature already describes that ReRAMs can be affected by unique faults [4–6], demanding the development of new manufacturing test procedures [7,8]. In [9], the authors provide a review of the memristive device manufacturing process and a discussion related to possible defects that may affect these novel devices, identifying the relation between manufacturing defects and faulty behaviors. In the last few years, some new manufacturing test strategies for ReRAMs were proposed in literature [10,11], since traditional March Tests, which explore the execution of predefined read and write operations applied at each memory cell, are extremely time-consuming and moreover not able to guarantee the detection of all unique faults. Thus, the manufacturing test of emerging memories is challenging due to not only the fact that these memories are affected by novel faults with a parametric nature, but also the fact that fault propagation of these faults is not easy and can be extremely time-consuming.

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* Corresponding author.
E-mail addresses: copetti@ids.rwth-aachen.de (T.S. Copetti), poehls@ihp-microelectronics.com (L.M. Bolzani Poehls).

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In this context, this paper proposes to analyze the ideal temperature to perform manufacturing tests of ReRAMs, aiming to reduce the time required for testing. In more detail, the use of extreme temperatures can facilitate the fault propagation depending on the defect size and location in the ReRAM cell. It is important to note that this paper is an extension of the work published in [12]. A case study composed of a 3 × 3 word-based ReRAM implemented using a 130 nm Predictive Technology Model (PTM) was adopted. A total of 17 defects were injected, assuming the Resistive Defect (RD) model, and 3 different temperature conditions (25, 100, and −40 °C) were investigated. The obtained results show that temperature can facilitate fault propagation depending on the defect position. In more detail, weak defects are more easily propagated considering extreme temperatures during testing.

The remainder of this paper is structured as follows. Section 2 presents the background related to redox-based memristive devices, fault models, and defect injection schemes. In Section 3, the experimental setup is detailed, and also how the simulation was performed, and in Section 4, a further classification of unique faults is presented. Section 5 summarizes the obtained results, and in Section 6 these results are discussed. Finally, in Section 7, we conclude the paper.

2. Background

This Section introduces the main concepts regarding redox-based memristive devices and summarizes the existing fault models and defect injection schemes that can be adopted for modeling manufacturing defects in ReRAMs.

2.1. Redox-based memristive devices

A redox-based memristive device is a passive element that consists of a metallic oxide between two metallic electrodes [13]. Physically, the working principle of redox-based memristive devices is based on the reversible formation of a Conductive Filament (CF) composed of oxygen vacancies generated during a Forming Stage. It is important to mention that the absence or presence and the size of CF directly influence the current flow in the device [13]. Also, the CF remains in the redox-based memristive device even when no voltage is applied, which classifies the device as non-volatile [13]. Polarizing the device in one direction increases the CF, which moves atoms to the active electrode and, as a consequence, increases the current flow, leading to the Low Resistance States (LRS). Polarizing it in the opposite direction will reduce the CF and the current flow, leading to the High Resistance States (HRS) [13].

The operation that causes the switching from HRS to LRS is called SET and occurs when applying a voltage V_{SET} with a value larger than its threshold voltage (V_{th}). The operation responsible for the LRS switch to HRS is called RESET, occurring when applying a V_{RESET} voltage of opposite polarity to the device [13]. To perform a read operation in the redox-based memristive device, a small V_{READ} voltage lower than both thresholds is applied, and the generated current is sensed, allowing the identification of the device's state. This voltage can be applied in any direction of the electrodes, and it needs to be lower so as not to change the state of the device [13].

2.2. Fault models

Like any other device, memristive devices are prone to manufacturing deviations, including process variation and manufacturing defects, that may result in different faulty behaviors [8,9,14]. Thus, a ReRAM cell can be affected by common faults found in CMOS-based memories [5], but also by faulty behaviors that are not observed in traditional memory technologies. In more detail, ReRAMs can be affected by faulty behaviors initially classified into two main fault models: (a) Conventional and (b) Unique [7]. Fig. 1 depicts the resistive states' intervals associated with LRS, HRS, as well as the faulty states (Undefined State, Extreme LRS, and Extreme HRS). Note that the conventional logical

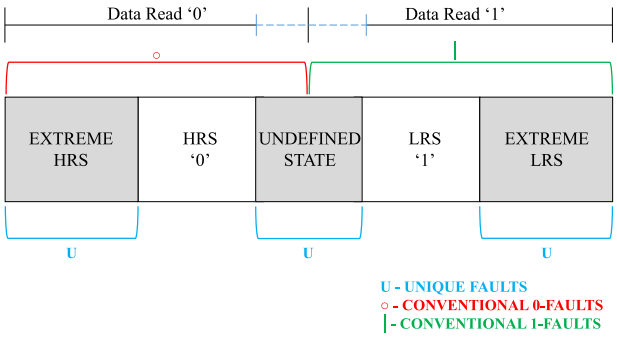

Fig. 1. Resistive states and faulty resistance intervals of ReRAM cells [16].

faults are the regions highlighted in green and red ('1' and '0'), which can present, for example, stuck-at and transition faults, and the regions highlighted in blue represent the areas of emerging faults related to the unique fault [15,16]. It can be noticed in the figure that the *U* state, the state between HRS and LRS, which is a region that is not ideal for the correct reading of the read circuit. So, this *U* state needs to be detected because it indicates misbehavior in the memristive device [8,17]. According to the literature, four unique faults of ReRAMs have already been described:

(1) Undefined Write Fault (UWF) [8], after a writing operation, the memristive device is in an undefined state *U* between '0' and '1' (HRS and LRS);
(2) Deep State Fault (DeepF) [17] occurs when the resistance in the cell is deep inside the boundaries of one state, being called Extreme HRS and Extreme LRS;
(3) Unknown Read Fault (URF) [8,17] occurs when the read operation's output is not reliable. Because it presents a random logic value as a result. A URF can occur when the memristive device stores a resistance very close to or exactly in the *U* state;
(4) Intermittent Undefined State Fault (IUSF) [18], in which the memristive device switches its mechanism intermittently from bipolar to complementary, leading to a *U* state after a write operation. The bipolar switching behavior is where SET and RESET occur at opposite voltage polarities, while complementary switching SET and RESET occur in the same polarity. For example, one device could inadvertently initiate a RESET behavior during a SET operation.

Finally, it is important to mention that all unique faults represent parametric faults since these faulty behaviors represent a change of electrical parameters' values associated with the resistive states of the ReRAM cell from nominal or expected values.

2.3. Defect injection schemes

In favor of properly simulating all possible faulty behaviors associated with manufacturing deviations, methods for injecting defects in a ReRAM cell are needed. Currently, two defect models are well established in the literature, the Defect Oriented (DO) and the Resistive Defect (RD) model. The DO model focuses on changing parameters in the memristive device itself to simulate faulty behaviors, being able to represent the non-linearity of the memristor device. In contrast, the RD model works by introducing a resistor at one specific point in the circuit to the model. A resistor in parallel with the ReRAM cell can lead to a *U* state during a write operation, for example. Note that the resistor values correspond to the strength of the defects [7]. Finally, it is important to note that for this work, due to its simplicity, the RD model was chosen to be used to inject defects in ReRAM cells.

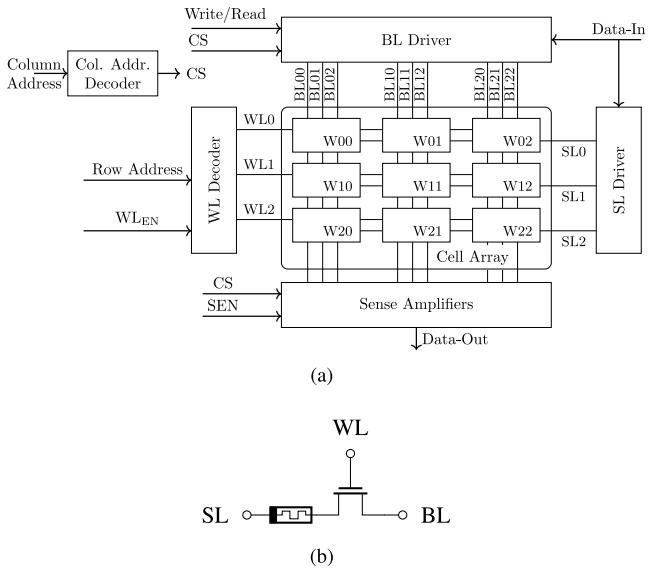

Fig. 2. The adopted case study (a) Block diagram, (b) 1T1R ReRAM cell [19].

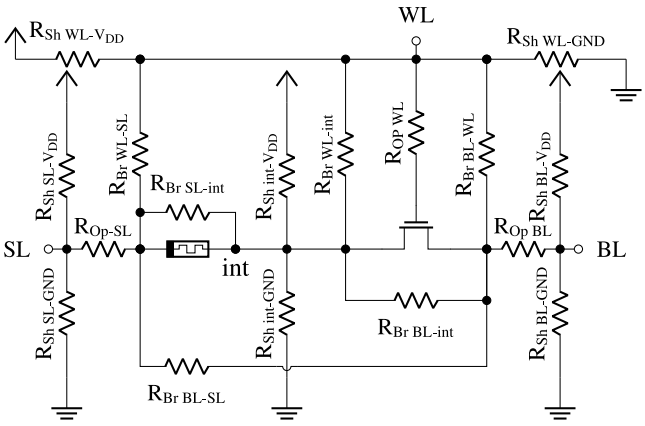

Fig. 3. Defect positions in a 1T1R ReRAM cell.

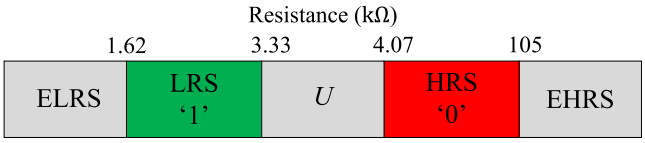

Fig. 4. Resistive states intervals of ReRAM cells.

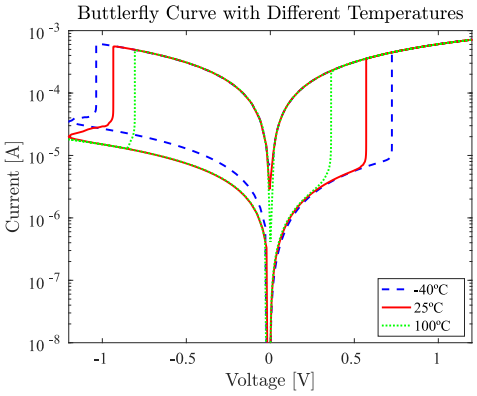

Fig. 5. Butterfly curve for three temperatures.

3. Experimental setup

In order to understand how and if the use of stress conditions can facilitate fault propagation, reducing the time required for performing manufacturing tests of ReRAMs, a case study composed of a 3 × 3 word-based ReRAM was adopted. The case study was implemented using a 130 nm Predictive Technology Model (PTM) for the CMOS-based circuits and the Valence Change Mechanism (VCM)-ReRAM compact model v1b proposed in [20,21]. The block is the same as used in our previous work published in [15,19], and is illustrated in Fig. 2(a). Every word consists of three 1T1R ReRAM cells, storing one bit of data, as in Fig. 3 without considering the resistors. All words on one row share the Word Line (WL) and Select Line (SL), while all cells in one column share a Bit Line (BL). Fig. 2(b) depicts a 1T1R ReRAM cell. In addition, peripheral circuitry is used to control the block. Note that the writing methodology adopted always performs a RESET operation at the beginning of each write operation (write '0' or write '1'), which ensures that the cells are not over-SET, which may lead to low reliability [22]. This RESET operation is performed by driving the SL to V_{reset} and the corresponding BL to Gnd. When the data to be written is a '1', a SET operation is subsequently performed on the ReRAM cell only. This is done by setting the BL to V_{SET} and the SL to Gnd. Fig. 4 depicts the resistance value regions defined in this work for each resistive state (LRS, HRS, U, ELRS, and EHRS).

A total of 17 defects were injected in a single ReRAM cell according to the RD model. Fig. 3 shows the resistors used to model the possible manufacturing defects in a ReRAM cell. It is important to note that this work introduces the manufacturing defects based on the work presented in [23]. In more detail, in [23], the authors identified all potential locations where a resistor could be added to model manufacturing defects in ReRAM cells. Assuming a defect-free ReRAM cell, one resistor at a time was introduced and its size was varied in order to represent different defect strengths and consequently, propagate different faulty behaviors. Note that this analysis does not consider possible impacts on neighboring cells. The resistors were named as in [23], and can be classified into three categories: shorts, bridges, and opens. The internal node of the cell was named *int*.

The temperature dependence of VCM-ReRAM switching is captured in the JART model through ambient temperature (T_0) and thermal resistance (R_{th0}). An increase in T_0 reduces the Joule heating required to activate ionic motion, resulting in lower SET and RESET voltages [21]. This behavior can be observed in Fig. 5, which depicts the butterfly curves at the three temperatures used in this work. The pattern presented is consistent with measurements in actual ReRAM devices [24]. Meanwhile, R_{th0} accounts for local self-heating; a higher value accelerates the operations without significantly affecting HRS or LRS currents [21], although at the lowest temperature, the RESET branch exhibits a slight current limitation, consistent with reduced thermal activation. These temperature-dependent variations in the I–V characteristics can improve the fault detection strategy by increasing the contrast between logic states.

The bit-cell model includes temperature effects as much as the available electrical models allow, although it remains a simplified circuit representation. Other blocks in the memory chain are also influenced by temperature: the Sense Amplifier (SA) varies due to transistor-level behavior, while interconnects have a negligible impact and act mostly as passive lines. Thus, the model covers the most relevant thermal effects for VCM-ReRAM devices.

Finally, it is important to mention that a dedicated tool implemented in Python was developed. The tool's flowchart is presented in Fig. 6. Note that the Python tool loads the circuit netlist described in Spectre and performs the simulations, setting the initial temperature at −40 °C, injecting the defect, and verifying possible fault propagation. If the tool identifies a faulty behavior, it changes the defect size by

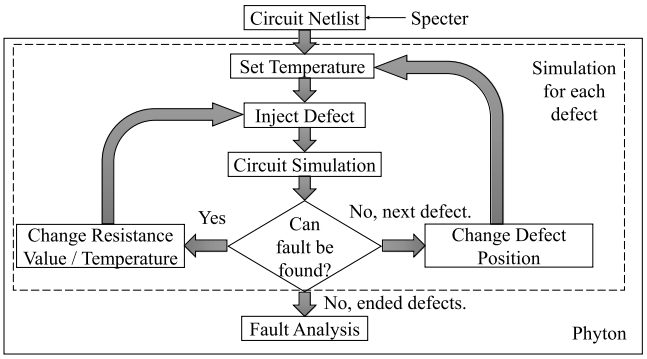

Fig. 6. Simulation flow.

Table 1
Unique fault models for single-cell static FPs.

S	F	R	FP	Unique fault model
0	U	–	$\langle 0/U/-\rangle$	USF0
1	U	–	$\langle 1/U/-\rangle$	USF1
0w1	U	–	$\langle 0w1/U/-\rangle$	UTF1
1w0	U	–	$\langle 1w0/U/-\rangle$	UTF0
0r0	U	0	$\langle 0r0/U/0\rangle$	UDRDF0
0r0	U	1	$\langle 0r0/U/1\rangle$	URDF0
1r1	U	0	$\langle 1r1/U/0\rangle$	URDF1
1r1	U	1	$\langle 1r1/U/1\rangle$	UDRDF1

adjusting the resistance value of the resistor and simulates the netlist again until reaching the limit of the faulty behavior. After the definition of the fault region, the tool increments the temperature value. In the end, the same analysis is performed for all defects and temperatures. It is important to mention that the developed tool is also able to classify the observed faulty behaviors properly. Note that the tool changes the resistors' values, from 1 Ω to 10 GΩ. In addition, the case study is simulated using Cadence's Spectre. The tool follows the test principle based on [25]. Each operation – write, read, or keep a value stored – is performed, after which the resistance of the cell is observed and related to a corresponding logic value. For read operations, the output of the SA is also recorded to verify correct functionality. Thus, for each defect size, when the simulation is concluded, the faulty behavior is identified, and all faults are categorized as conventional or unique. Details about this classification are provided in Section 4.

4. Fault analysis and classification

The faulty behaviors observed during simulations were classified as conventional and unique, where the conventional faults follow the standard classification of memory faults described in [25]. In the proposed analysis, we observed the following conventional faults: Stuck-at Fault (SF), Transition Fault (TF), and Incorrect Read Fault (IRF) [25]. For the unique faults, the following classification based on the observed faulty behaviors is adopted:

- Unique State Fault (USF) occurs when the ReRAM cell state goes to the U state, without performing any operation. Note that USF can be further classified as USF0 and USF1 when the expected ReRAM cell value is '0' or '1', respectively;
- Unique Transition Fault (UTF) happens when the ReRAM cell state goes to the U state when switching the cell, or in other words, when performing a transition. This type of fault can be UTF0 or UTF1;
- Unique Read Disturb Fault (URDF) occurs when the cell is in a U state, or changes to a U during the read operation, and the read output indicates a wrong logical value when assuming the expected ReRAM state considering the previous write operation;
- Unique Deceptive Read Disturb Fault (UDRDF) is observed when the cell is in a U state, or changes to an U during the read operation, and the read output shows the expected logical value when assuming the expected ReRAM state considering the previous write operation.

Note that USF0, USF1, UTF0, and UTF1 correspond to S0FU, S1FU, W0TFU, and W1TFU defined in [23], respectively.

For a better understanding of the Unique Fault Model, the Fault Primitives (FPs) of these faults are presented in Table 1. An FP is a fault behavior, which is a difference between the observed and expected memory behavior, and can be denoted by a common notation: $\langle S/F/R\rangle$ [25]. In this work, only the single-cell static FPs are considered, which are the faults observed in one cell with one or no operation performed [25]. S denotes the operation sensitizing sequence, $S \in \{0, 1, 0w1, 1w0, 0r0, 1r1\}$. F denotes the faulty state stored in the cell, for this case $F \in \{U\}$. And finally, R describes the logic output of the read operation, $R \in \{0, 1, -\}$.

5. Obtained results

This section summarizes the results obtained during the case study's simulations. In the following, the results will be presented in three main groups classified according to the defect type: short, bridge, and open. The obtained results are presented in Figs. 7, 8, and 9. Observing these figures, it is possible to see the faulty behavior observed depending on the defect position and strength (resistor value), considering three different temperatures, 25, 100, and −40 °C. In the x-axis, the defect's resistance is presented in a logarithmic scale. For each defect type, a complete explanation related to the observed faulty behavior is provided. Note that for short and bridge defects, the static faults are observed when assuming smaller resistance values, and for open defects, the opposite behavior is observed. The adopted highest temperature of 100 °C was selected based on the stability aspects of the adopted case study. Temperatures above this value were found to alter the resistive state intervals in the SA, altering the detection regions.

5.1. Short defects

Short defects are an unintended resistive path that connects a node to V_{dd} or ground [26]. Fig. 7 depicts the results obtained when injecting short defects into the ReRAM cell.

(1) **Defect $R_{ShWL-V_{DD}}$:** This defect does not able to impact the cell's behavior during writing operations, but it causes IRF0 when assuming smaller resistance values (strong defects) at −40 °C. This occurs because the current coming from the SA discharges earlier than expected during the read operation when assuming lower temperatures, putting the SA at '1'. The same SA misbehavior is also observed when considering other defect positions.
(2) **Defect $R_{ShWL-GND}$:** When assuming small defect sizes, the transistor does not turn on during the write and read cycles, causing mainly TF1 and TF0. However, the TF0 was visible first due to the adopted block's write protocol, which always executes a RESET before performing a write operation. Note that in this situation, temperature plays an important role in guaranteeing fault propagation, since some faults are propagated when assuming 100 °C only.
(3) **Defect $R_{ShBL-V_{DD}}$:** The first expected faulty behavior is a degraded SET operation performance because the BL cannot go to ground, and consequently, a TF0 is propagated, followed by a DRDF0 and an IRF1. When assuming this specific defect, the temperature variation plays a more significant role in fault propagation.

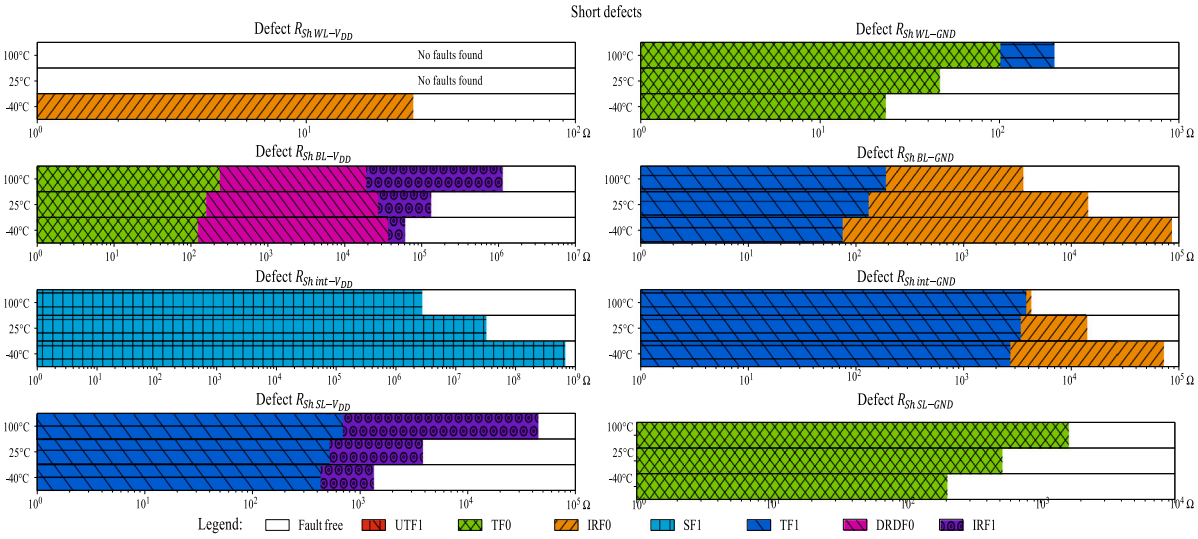

Fig. 7. Short defects: Faults propagated assuming different defect sizes.

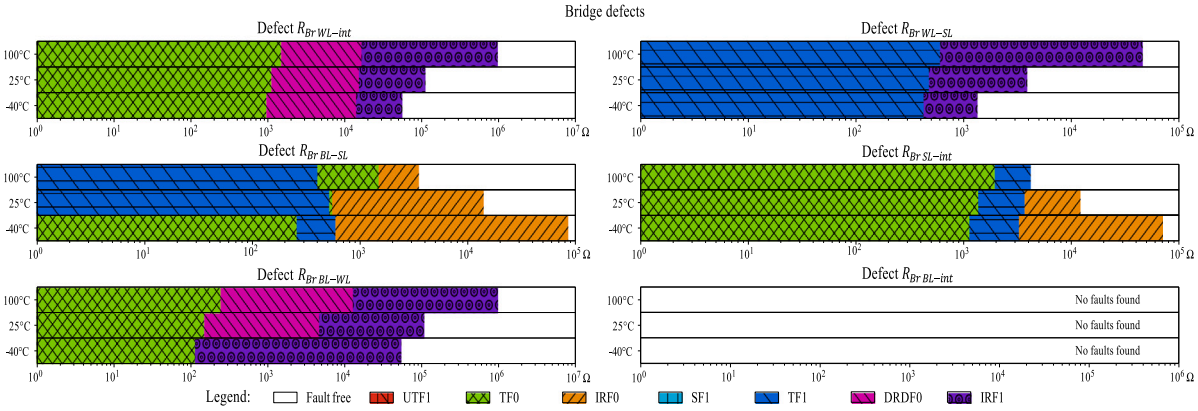

Fig. 8. Bridge defects: Faults propagated assuming different defect sizes.

(4) **Defect $R_{ShBL-GND}$:** When considering this defect, the fault behavior follows a pattern varying according to the assumed temperature. When assuming smaller defect sizes, TF1 occurs, and, as expected, as the temperature increases, the fault boundary becomes bigger. Note that the IRF0's behavior is affected by temperature in the opposite way.

(5) **Defect $R_{Shint-V_{DD}}$:** Until significant defect sizes are reached, SF1 is observed due to the path created through the memristive device, which causes the ReRAM cell to SET, independently of the performed operation. Note that temperature plays a crucial role when considering this specific defect because, at lower temperatures, it is significantly difficult to observe a fault-free operation.

(6) **Defect $R_{Shint-GND}$:** This defect impacts the cell behavior similarly to defect $R_{Sh\ BL\text{-}GND}$. However, here the defect range able to cause faults is bigger and, when assuming 100 °C only. Further, at this temperature, IRF0 is masked by TF1, hence, not observed.

(7) **Defect $R_{ShSL-V_{DD}}$:** This defect propagates faults during the SET operation, thereby causing TF1 initially and IRF1 when assuming big defect sizes. The temperature has an inverse impact on the fault propagation of IRF1 concerning the behavior observed when injecting defect $R_{Sh\ BL\text{-}GND}$.

(8) **Defect $R_{ShSL-GND}$:** As expected, assuming smaller defect sizes, the SL cannot be pulled up to significant voltages, and consequently, a satisfactory RESET cannot be performed, causing the cell to exhibit a conventional TF0. Further, although for a very small range of defect sizes not visible in this graph, the cell exhibits a UTF0.

5.2. Bridge defects

Bridge defects consist of a parallel resistance between two nodes that are not expected to be connected [26]. Fig. 8 shows the results obtained when considering bridge defects in the ReRAM cell.

(1) **Defect $R_{BrWL-int}$:** When injecting small defects in this specific position, the occurrence of TF0 is expected because, during any operation, the internal node of the ReRAM cell is pulled up when WL is active. This creates a current path through the memristive device, causing a constant SET. At bigger defect sizes, this current path becomes weak. Further increasing the defect size, a DRDF0 fault, followed by an IRF1 fault, was observed. The reason is that the SA receives the wrong current due to the *int* being pulled up during the READ operation. The ReRAM cell becomes fault-free as the defect size further increases, which represents weak defects. It is important to mention that temperature plays a crucial role here. As the temperature ranges from −40 °C to 100 °C, the fault boundary increases by 10-fold.

(2) **Defect $R_{BrWL-SL}$:** As expected, for small defect resistance values, the SET operation is affected, and a TF1 is observed. Afterward, an IRF1 is propagated.

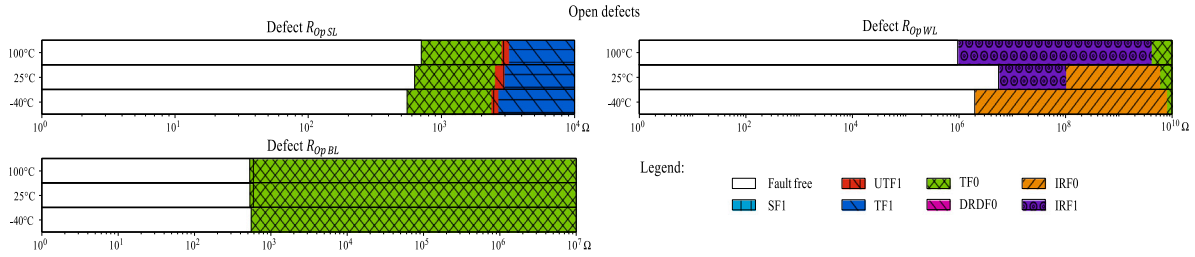

Fig. 9. Open defects: Faults propagated assuming different defect sizes.

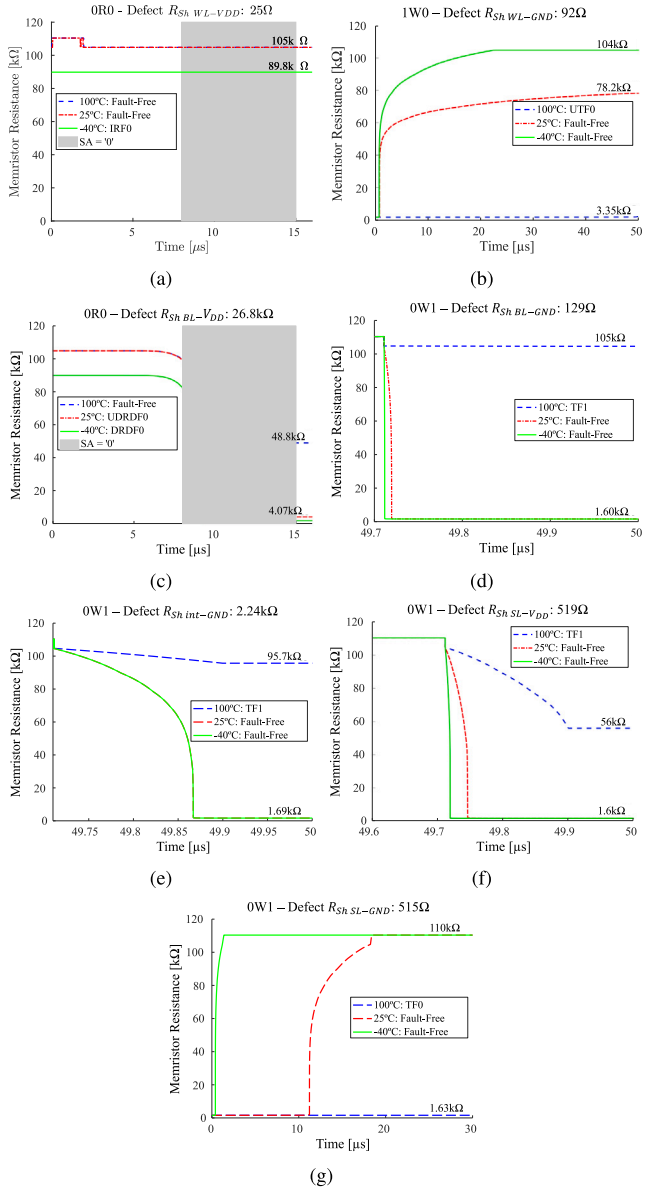

Fig. 10. Fault propagation related to short defects: (a) 0r0 - $R_{Sh\ WL\text{-}V_{DD}}$, (b) 1w0 - $R_{Sh\ WL\text{-}GND}$, (c) 0r0 - $R_{Sh\ BL\text{-}V_{DD}}$, (d) 0w1 - $R_{Sh\ BL\text{-}GND}$, (e) 0w1 - $R_{Sh\ int\text{-}GND}$, (f) 0w1 - $R_{Sh\ SL\text{-}V_{DD}}$, (g) 0w1 - $R_{Sh\ SL\text{-}GND}$.

(3) **Defect $R_{BrBL-SL}$:** When assuming small defect sizes in this specific position, no write or read operations are allowed due to the created short path between the BL and the SL; hence, both the TF0 and TF1 faults are propagated. Further, at higher defect sizes, an IRF0 fault is observed because the SA receives the wrong current.

(4) **Defect $R_{BrSL-int}$:** This defect is also similar to $R_{BR\ BL\text{-}SL}$, where both TF1 and TF0 faults coexist. The difference here is that at high temperatures, the IRF0 fault is masked and hence not observed.

(5) **Defect $R_{BrBL-WL}$:** This defect causes faults similar to the ones associated with $R_{BR\ WL\text{-}int}$ defect. When there is no defect, the WL is supposed to be pulled up during the RESET stage. However, these defects pull down the WL, causing a RESET stage error in the cell. Hence, similar behavior is observed both in terms of temperature and defect size variations. Note that when assuming low temperatures, this defect does not cause DRDF0.

(6) **Defect $R_{BrBL-int}$:** As expected, this defect is not able to cause any write or read issues, since the current easily passes through the memristive device.

5.3. Open defects

Open defects are defects that exist between the connection of the elements in the circuit [26]. Fig. 9 depicts the faulty behaviors associated with open defects.

(1) **Defect R_{OpSL}:** This defect disconnects the memristive device from the SL. As expected, for small defect sizes, no faults were observed. However, when increasing the defect size, both conventional, such as TFs, and unique faults were observed. Not only conventional faults, such as TFs, have been observed. Here, the defect can hinder the current from flowing through the ReRAM cell, preventing the cell from correctly SET/RESET.

(2) **Defect R_{OpWL}:** A strong defect is required in order to propagate any fault during a write operation. Before that, it is probable to see IRF happen due to the read operation being so short when compared to the write operation. Interesting to notice that the temperature variation changes the propagation of the IRF, where at −40 °C IRF0 is dominant, and for 100 °C it is the IRF1. Note that when assuming 25 °C, both faulty behaviors are observed. Analyzing the TF0, the temperature is also relevant, at −40 °C the fault starts to manifest at 300 MΩ, then 3 GΩ at 100 °C, being a variation of the fault manifestation of 10 times the assumed resistance value.

(3) **Defect R_{OpBL}:** Considering this specific defect position, small defects are not able to propagate any faulty behavior. When increasing the defect size, TF0 can be observed for the entire analysis range.

Exploring the overall trends, it is possible to identify some critical patterns: open defects, particularly $R_{Op\ SL}$, exhibit a larger range of unique fault propagation compared to short and bridge defects. Shorts and bridge defects predominantly generate conventional faults, whereas open defects are more prone to trigger unique faults within specific temperature and defect size ranges. Furthermore, temperature significantly modulates fault manifestation: certain faults only appear at −40 °C or 100 °C, such as IRF0 in $R_{Sh\ WL\text{-}V_{DD}}$ and TF1 in $R_{Sh\ WL\text{-}GND}$,

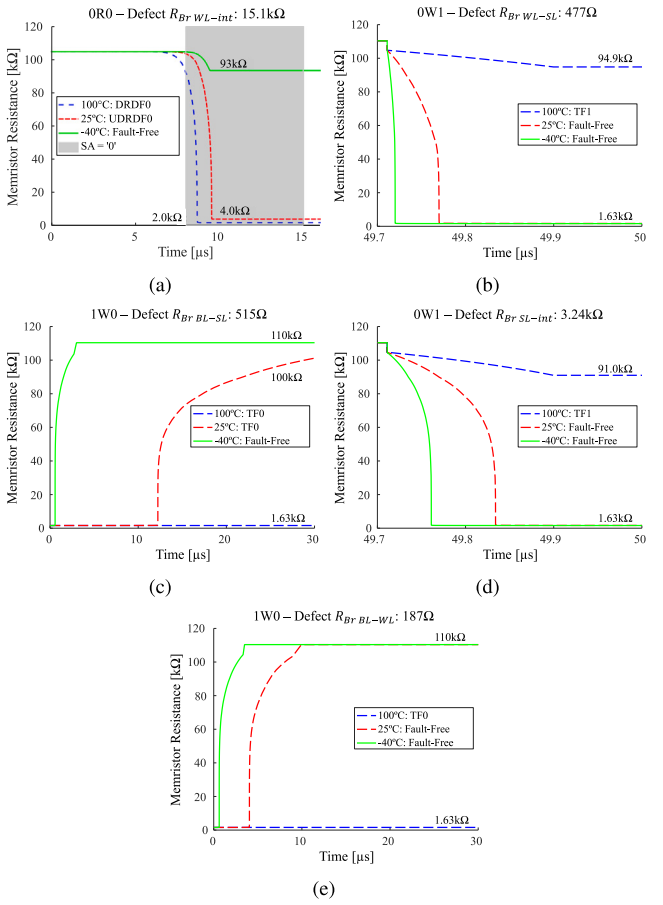

Fig. 11. Fault propagation related to bridge defects: (a) 0r0 - $R_{Br\ WL\text{-}int}$, (b) 0w1 - $R_{Br\ WL\text{-}SL}$, (c) 1w0 - $R_{Br\ BL\text{-}SL}$, (d) 0w1 - $R_{Br\ SL\text{-}int}$, (e) 1w0 - $R_{Br\ BL\text{-}WL}$.

while intermediate temperatures might suppress them. These observations provide a practical guideline for focusing on the most critical defect types and temperature conditions during manufacturing tests. These results highlight the need to robustly design the operational metal lines and consider different operating temperatures to detect small defects effectively.

6. Discussion

Analyzing the obtained results, it is possible to see that temperature can be adopted as a stress condition for facilitating fault propagation, since the same defect size can, in some situations, propagate or not propagate faults, depending on the assumed temperature. Note that some faults, such as RDF and URF, were also observed during the simulations, even if they do not appear in Figs. 7, 8, and 9. This occurs because the defect size region able to propagate these faults is too small and consequently, not visible in the bar graphs.

Overall, the results indicate that defect type and temperature interact to determine fault propagation behavior. Open defects consistently show a higher probability of unique fault manifestation, whereas shorts and bridges predominantly lead to conventional faults. Temperature can either facilitate or suppress specific faults, in some cases even inverting the expected faulty behavior for a given defect size. For instance, the defect $R_{Sh\ WL\text{-}V_{DD}}$ with a resistance of 25 kΩ triggers an IRF0 at −40 °C, but at 25 and 100 °C, the same defect shows no faulty behavior. These insights highlight the importance of targeting both defect location and testing temperature to optimize ReRAM manufacturing tests and reduce test time.

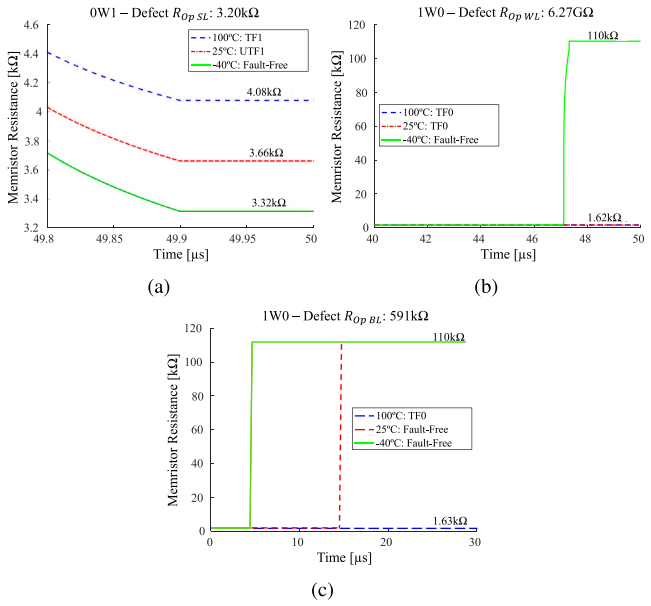

Fig. 12. Fault propagation related to open defects: (a) 0w1 - $R_{Op\ SL}$, (b) 1w0 - $R_{Op\ WL}$, (c) 1w0 - $R_{Op\ BL}$.

To exemplify the different fault propagation situations, Figs. 10, 11, and 12 depict some of the faulty behaviors assuming different temperatures with the defect size fixed in one specific resistance value, classified according to the defect type. Fig. 10(a) shows that at low temperatures, the memristor's resistance is affected during the read operation, causing an IRF0. In Fig. 10(b), it is possible to see the occurrence of a UTF0 at 100 °C, where the resistive state of the 1T1R ReRAM cell is about 3.35 kΩ, inside the *U* region. Note that when considering the other two analyzed temperatures, the transition was successful for the same injected defect. Similar behavior, but for the opposite write operation, can be seen in Fig. 12(a) with a TF1 at 100 °C, and a defect resistance value of 3.20 kΩ. After the write 0 operation, the memristor stores a resistance of 4.08 kΩ. At 25 °C, the memristor stays with 3.66 kΩ representing a UTF1. Finally, at −40 °C, the memristor's resistance is equivalent to 3.32 kΩ, representing a fault-free behavior.

Considering the graphs presented in Figs. 10(c) and 11(a), they present a complementary behavior, with the temperature affecting the graphs in the opposite way. In more detail, in 10(c) a DRDF0 occurs at −40 °C, and a UDRDF0 happens when simulating at 25 °C. Note that at 100 °C, no faulty behavior is observed in the ReRAM cell; however, the opposing behavior is visualized in Fig. 11(a). Figs. 10(d), 10(e), 10(f), 10(g), 11(b), 11(c), 11(d), 11(e), 12(b), and 12(c), show the propagation of TFs at different temperatures. It is important to mention that the defects $R_{Sh\ int\text{-}V_{DD}}$ and $R_{Br\ BL\text{-}int}$ do not cause any fault behavior, being omitted in this analysis. Finally, it is important to highlight that DeepFs were not observed during the performed simulations because the RD model is not able to properly model the possible defects able to cause these faults.

7. Final remarks

This paper analyzed the possibility of using temperature as a stress condition to facilitate fault propagation caused by manufacturing defects in ReRAM cells, which makes the reduction of the time required for testing ReRAMs at time zero possible. The fact that ReRAMs can be affected by not only conventional but also unique faults increases the complexity of manufacturing test strategies. In more detail, the parametric nature of unique faults makes their propagation at the logic level more difficult. The obtained results show that depending on the

defect position and size, temperature can make the propagation of different faulty behaviors easier. Although the analysis is not particularly new, it helps test engineers focus on the most critical ReRAM failure models. Some defects have a greater impact than others, and this study demonstrates their behavior, highlighting that temperature plays a key role: certain faults only manifest within specific temperature ranges, which should be considered when designing and testing ReRAMs. The use of new DfT strategies for testing ReRAMs at time zero, while exploring different temperatures, can significantly reduce the time required for testing these novel memories. As future work, we can suggest extending the proposed analysis by also considering the possible impact of single ReRAM cell defects on neighbor ReRAM cells, as well as other case studies implemented using industrial technology libraries. Finally, other memristive device models could also be explored, including aspects related to read noise, available in [21], assuming conditions of device-to-device variability.

CRediT authorship contribution statement

T.S. Copetti: Conceptualization, Methodology, Software, Validation, Formal analysis, Investigation, Resources, Data curation, Writing – original draft, Writing – review & editing, Visualization, Supervision. **A. Chordia:** Software, Validation, Formal analysis, Investigation, Data curation, Writing – Original Draft, Visualization. **M. Fieback:** Resources, Writing – review & editing. **M. Taouil:** Methodology. **S. Hamdioui:** Methodology, Resources. **L.M. Bolzani Poehls:** Conceptualization, Methodology, Writing – review & editing, Supervision, Project administration, Funding acquisition.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Data availability

Data will be made available on request.

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