Single Grain TFTs for High Speed Flexible Electronics

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Single Grain TFTs for High Speed Flexible Electronics

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To my love

Contents

Chapter 1

Introduction

In this thesis the challenge is faced of significantly improving the reliability and mobility of single-grain silicon thin-film transistors (SG-TFTs), and of developing a SPICE model of such devices. The development of systems on a chip, system in a package, large-area electronics and electronics on unconventional substrates has become a relevant research area nowadays, in view of the down-scaling limit on electronic devices and the gradual transition from the era of *Moore's law* to that of *More than Moore*. As a result, researchers have been focusing among other things on thin-film transistor (TFT) technology, which is fundamental for the development of large-area electronics, three-dimensional integrated circuits (3D-ICs), electronics on unconventional substrates like glass or plastic, active-matrix liquid-crystal displays (AM-LCDs), active-matrix organic light-emitting diodes displays (AM-OLEDs), or more recently electronic paper (E-Paper), which promises to find very wide application in consumer electronics. Among the various TFT technologies available, the fabrication of single-grain silicon thin-film transistors (SG-TFTs) by the μ-Czochralski process invented in the DIMES laboratories at TU Delft has succeeded in obtaining a mobility as high as that of silicon-on-insulator (SOI) MOSFETs despite the low process temperature, opening the way for a wide range of future applications.

This introductory chapter starts with a discussion of the evolution of TFT-electronics and a short description of single-grain silicon TFT technology and its potential applications. This is followed by a discussion of the motivation behind this study and an outline of contents of this thesis.

1.1 TFT technologies and their applications

While microelectronics and now nanoelectronics continue the trend towards smaller and smaller devices, there are also many in the electronics community pushing the idea that "bigger can be better". As revolutionary as microelectronic integrated circuits (ICs) have been, there are functions that are not well addressed by conventional microelectronic IC technology. While the advance of microelectronics and nanoelectronics has tended to make IC devices smaller and smaller, applications that require large-area electronics are difficult or prohibitively expensive to achieve with conventional IC technology. And three-dimensional (3D) applications that require devices built one on top of the other, or flexible electronics that require technologies to be produced on unconventional substrates are impossible to achieve with IC microelectronics because of the high process temperatures. These are the main reasons for the success of thin-film electronics that can be produced at low process temperatures. Thin-film electronics permit solutions that would not be economically viable or even possible with commercial IC microelectronics [1].

Thin-film electronics have evolved enormously during the past few decades. Hydrogenated amorphous silicon (a-Si:H) was one of the first active materials used for producing TFT that permitted the use of low process temperatures suitable for large-area glass substrates [2]. This material has a long-range ordered structure despite the amorphous nature, because hydrogenation efficiently passivates the midgap states associated with dangling bonds in the random network of silicon atoms. Due to the amorphous state of the active layer, off-state leakage currents in the sub-picoampere range and on-currents in the microampere range are typical values for a-Si TFTs. The requirement that TFTs in LCD pixels should have on/off current ratio greater than 10^6 is thus comfortably met. Mass production of large-area a-Si active-matrix liquid crystal displays (AMLCDs) began in the late 1980s.

Although there was no difficulty in achieving the desired large area, a-Si TFTs have a typical mobility below 1 cm^2/Vs. This limited the applications of this material to the AMLCDs, and was the main reason for the development of polysilicon (poly-Si) TFTs. These new devices showed an improved mobility (up to 150 cm^2/Vs) [3] permitting a higher display resolution because the transistor area needed for a given performance was less than that of a-Si TFTs [4]. Furthermore, the high mobility of poly-Si TFTs and the possibility of making both n- and p-type TFTs facilitated the development of driver circuits. A hybrid approach using a-Si TFTs for their low leakage current and uniform mobility as required for pixel switches in combination with high-mobility poly-Si TFTs for the peripheral circuits was also developed [5].

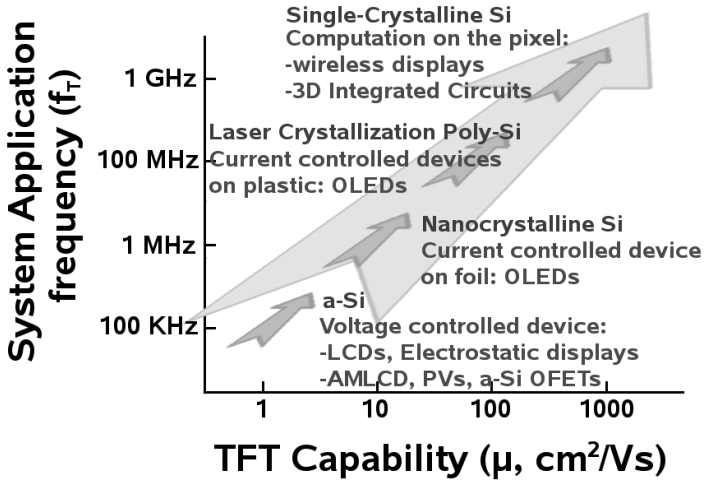


Figure 1.1: Schematic view of evolution of electronic system performance, shown in a plot of system application frequency against TFT capability [1].

As recrystallization techniques were improved, poly-Si TFT technology showed a gradual increase in mobility up to 350 cm^2/Vs. This improved mobility allowed poly-Si TFTs to be used in basic demonstration prototypes of LCD peripheral circuits other than display drivers, such as a CPU [6, 7], SRAM [8] and DRAM (NEC) which all embodied poly-Si TFTs on a glass substrate. However, the operating frequency of these circuits was not very high (below 10 MHz) and none of them has yet become a real product as a non-LCD application. The main reason for this are the limited mobility and the wide spatial variation of TFT characteristics due to the incorporation of random grain boundaries (GBs) in the active area of the TFT. Atoms in random GBs are highly disordered, giving rise to discontinuous lattice structures and hence high defect densities [9]. This leads to the formation of trapping states, which influence carrier conduction. A free carrier (hole or electron) is immobilized by the trap, creating a potential barrier that the carrier has to overcome and thus impeding its motion [10,11]. That limits the performance of poly-Si TFTs in terms of circuit frequency and consequently their field of application (Fig. 1.1). To improve TFT capability by enhancing the mobility, the random grain boundaries need to be spatially controlled. This led to the development of location-controlled grains [12].

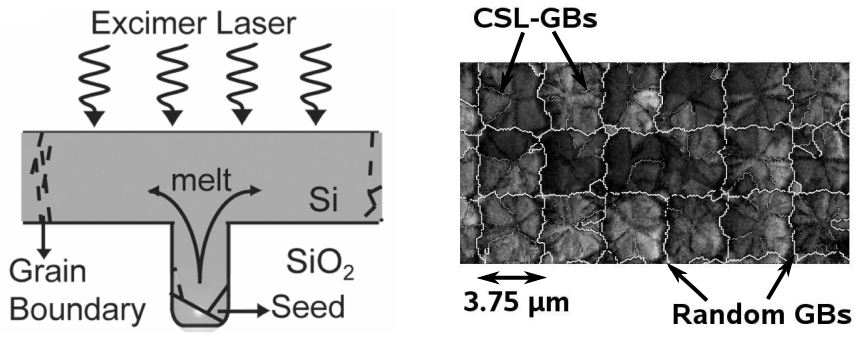
1.2 Single-grain silicon thin-film transistors fabricated by the μ-Czochralski process

Location control of the grain boundaries in the poly-Si layer improved the performance and enhanced the uniformity of TFTs by reducing the number of random grain boundaries in the active channel. In particular, if the grain is large enough to build the entire TFT inside it, this process yields a single-grain silicon TFT (SG-TFT) the performance of which is very close to that of a SOI MOSFET. Many new recrystallization techniques have been developed to improve the electrical performance of the poly-Si layer in this way, such as sequential lateral solidification (SLS) [13], CW-laser lateral crystallization (CLC) [14], phase modulated excimer laser annealing (PMELA) [15] and the μ-Czochralski process invented in the DIMES laboratories of TU Delft [16,17]. This last-mentioned process would seem to be particularly suitable as a basic for high-performance applications because of its many fundamental advantages over the other techniques mentioned such as:

- 2D location control of large grains (up to 8 μm)
- wide energy density windows within which location control is achieved
- high production throughput thanks to the one-shot process
- capability of crystallographic orientation control [18].

SG-TFTs fabricated by the μ-Czochralski process show highly competitive performance, with features such as an electron field-effect mobility of 600 cm^2/Vs and a hole field-effect mobility of 250 cm^2/Vs, an off-current of few pico-ampere and a subthreshold slope of about 200 mV/dec [17, 19].

Fabrication of a SG-TFT by the μ-Czochralski process The μ-Czochralski process is designed to build a TFT inside a single large grain of silicon, and to control the location of the grain precisely in two dimensions [12]. The latter objective is achieved by making a cavity 1 μm diameter cavity in an insulating layer and filling it with tetraethylorthosilicate (TEOS) by plasma-enhanced chemical vapor deposition (PECVD) at 350 °C to reduce the diameter of the hole to about 100 nm. Amorphous silicon is subsequently deposited to fill the remaining hole, after which excimer laser irradiation is used to initiate vertical growth in the cavity, where a small amount of unmelted Si at the bottom serves as a seed during crystallization. Grain occlusion occurs in the cavity during this phase; hence, the cavity is called a *grain filter*. As a



(a) (b)

Figure 1.2: Schematic view of draw grain filter and crystal growth in the μ-Czochralski process (a). Electron back-scattering diffraction (EBSD) image of location-controlled grains fabricated by the μ-Czochralski process (b), showing random GBs at the edge of single grains and CSL-GBs inside grains.

result of the filter effect, only one grain reaches the top of the cavity, where it acts as the seed for lateral growth of the single grain, as depicted in Fig. 1.2(a). Electron back-scattering diffraction (EBSD) analysis shows that random grain boundaries (GBs) are only found at the edge of grains, where they collide with one another. Inside the grain, on the other hand, the only defects observed are planar coincidence site lattice grain boundaries (CSL-GBs), dominantly $\Sigma 3$, $\Sigma 9$, and $\Sigma 27$, which have a much lower electrical activity than random GBs [20, 21]. Hence, a TFT can be built inside a single grain where it can serve as the basis for performace n- and p-channel devices. The structure of the resulting SG-TFT fabricated inside a grain grown by the μ-Czochralski process is indicated in Fig. 1.3, the main fabrication steps are summarized in Appendix A.

1.2.1 Potential applications of SG-TFTs fabricated by the μ-Czochralski process

Thanks to the performance indicated above, SG-TFTs fabricated by the μ-Czochralski process open the way to many interesting new applications. One such application on which may researchers have already been working is electronic paper (E-Paper). However, the low performance of conventional TFTs technology means that external driver circuits have to be connected to the pixels, making E-Paper as produced at present mechanically in-flexible.

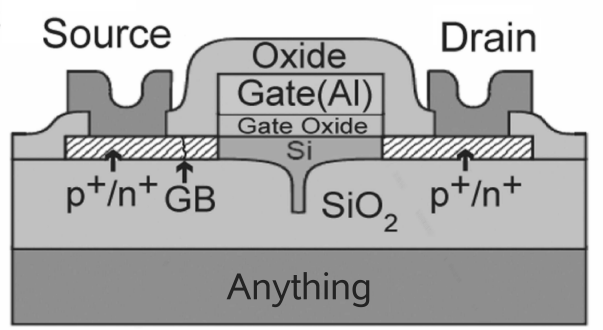


Figure 1.3: Schematic view of SG-TFT fabricated inside a grain grown by the μ-Czochralski process

SG-TFT technology, on the other hand, permits integration of the electronic display and signal processing elements to give a flexible display not unlike real paper. Displays produced on a flexible substrate material could use this technology not only for pixel switching but also for pixel addressing, signal processing and even communication electronics (both analog and digital), as indicated in Fig. 1.4. An E-Paper with a backplane based on SG-TFTs fabricated by the μ-Czochralski process is presented in Chapter 4of this thesis. The performance given by SG-TFTs fabricated by the μ-Czochralski process can also satisfy the high drive current and low drive voltage requirements of organic light-emitting diode (OLED) used to implement large, high-resolution active-matrix OLED displays. Other applications, such as wearable sensors, where a thin-film silicon sensor is integrated with interface electronics (e.g. A/D or D/A converters), RF communication circuitry and a silicon solar cell as a power source may also be enabled by SG-TFT technology. A PIN photodiode implemented in this technology could form the basis for image sensors on a flexible substrate as another possible application. The addition of wireless communication functionality makes it possible to realize short-range low data rate applications for two-way communication, which could be used in smart cards, wearable monitoring for biomedical implants or body area sensor networks. Furthermore, integrating the antenna and other passive elements directly with RF integrated circuits would allow a complete compact wireless SoC device to be offered. SG-TFT technology produced by the μ-Czochralski process could further enable three dimensional integrated circuits (3D-ICs)

as a means of increasing the integration density. In fact, the feasibility of stacking SG-TFTs on successive silicon layers has been demonstrated by the construction of a high performance monolithic 3D CMOS inverter [22].

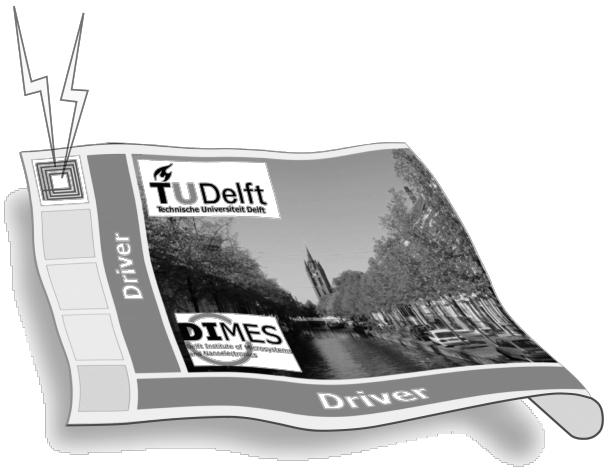


Figure 1.4: Example of flexible E-Paper

1.3 This thesis

1.3.1 Motivation and objectives

SG-TFTs fabricated by the μ-Czochralski process have already reached a performance as high as that of SOI MOSFET devices. However, one of the most important and challenging goals is extending SG-TFT technology to reach a higher level of performance than that achieved with SOI technology (fig. 1.1). This thesis considers two different aspects of this question. Firstly, given the proven potential of the μ-Czochralski process to provide high-quality crystalline silicon [12], it is also of interest to investigate whether the μ-Czochralski process could also be used to produce high-mobility semiconductor materials such as germanium (Ge) sputtered at low temperature as a medium for future thin-film transistor applications, since Ge is considered to be a potential replacement for silicon (Si) because of its much higher carrier mobility. Secondly, it is also worth while investigating whether the field-effect mobilities of n- and p-channel single-grain Si TFTs could be enhanced compared with to the most advanced strained-Si on SiGe MOSFET technology by applying strain with excimer laser crystallization, despite the low process temperature used.

The study of degradation phenomena in SG-TFTs under bias stress is also of fundamental importance for the reliability analysis of such devices. A method for degradation analysis of SG-TFTs under bias stress for 2D modeling by a TCAD simulator has therefore been developed as part of the present study. Such modeling aims to improve our understanding of high voltage applications. A prototype E-Paper with active-matrix quick-response liquid-powder display has been designed and developed with the aid of SG-TFT technology on this basis. The main issue in the development of such E-Paper is the requirement for a 70 V supply voltage. The necessary SG-TFT produced by the μ-Czochralski process must therefore be designed to operate at such a high voltage, and its fabrication process must be compatible with the μ-Czochralski process used to make standard SG-TFTs for the development of a fully integrated E-Paper with display and driver circuits.

No application using of SG-TFTs fabricated by the μ-Czochralski process would be possible without an accurate compact SPICE model of the intended device. Many SPICE models are commercially available nowadays for both MOSFET and Poly-Si TFT technologies. However, none of those is suitable for SG-TFTs. An accurate SPICE model of SG-TFT circuits designed for digital, analog and RF applications has been developed as part of the present study. In particular, a unified SPICE model has been obtained that is applicable both to SG-TFTs fabricated by crystallization at low laser energy (which have poly-Si-like performance) and to TFTs made by crystallization at high laser energy (which have SOI-like performance).

1.3.2 Outline of contents

After this introductory chapter, Chapter 2 is devoted to the SPICE model based on BSIMSOI and implemented in a SPICE simulator written in behavioral language Verilog-A. The DC BSIMSOI model has been modified and adapted to the SG-TFTs to take coincidence site lattice grain boundaries (CSL-GBs) into account. DC and RF parameters have also been extracted. A higher-order RF approximation model to improve the simulation of SG-TFT behavior at high frequencies is also introduced. This chapter ends with the description of a model of the transient effect in SG-TFTs.

Chapter 3 deals with the reliability analysis of SG-TFTs performed with the aid of a TCAD simulator, with special reference to the analysis of degradation mechanisms as a basis for prediction of electrical degradation of n-channel SG-TFTs under bias stress.

Chapter 4 presents the device design and process flow for the fabrication of reliable n- and p-channel SG-TFTs for high voltage applications, and the

results of experiments performed with the aid of these devices. This leads on to the description of a high-speed E-Paper with an active-matrix quick-response liquid-powder display realized with the aid of such high-voltage SG-TFTs.

The rest of the thesis is devoted to new technologies for the fabrication of other types of high mobility SG-TFTs. Chapter 5 deals with the material characterization of high-quality Ge grains. Measurements on p-channel Ge SG-TFTs and pseudo-TFTs show the potential of this technology for thin-film transistors. Chapter 6, by way of contrast, discusses the fabrication process and characterization of n- and p-channel strained single-grain silicon TFTs produced by excimer laser crystallization and the results of experiment on these devices.

Finally, the main conclusions derived from this study and recommendations for future work are given in Chapter 7.

Chapter 2

Modeling of single grain Si TFTs

Single-grain Si thin-film transistors (SG-TFTs) fabricated inside a location-controlled grain by the μ-Czochralski process using excimer laser crystallization have reached such high electrical performances as to be comparable with silicon-on-insulator metal-oxide semiconductor field-effect transistors (SOI MOSFETs) despite the low-temperature process at which they are produced (< 350 °C) [12, 17, 19].

An accurate, compact model of SG-TFTs for SPICE simulations is of a crucial importance for the design of digital, analog and RF circuits based on this technology [23, 24]. There are several commercially available SPICE models that are suitable for the modeling of bulk MOSFETs technology (such as the Berkeley Short Channel IGFET Model (BSIM), the Penn State Philips (PSP) model, the Enz-Krummenacher (EKV) model or the Hiroshima University STARC IGFET Model (HiSIM)), of SOI-MOSFETs (such as the BSIMSOI) or polysilicon TFTs (such as the Rensselaer Polytechnic Institute polysilicon TFT (RPI-TFT model)). None of these models is suitable for use with SG-TFTs fabricated by the μ-Czochralski process, however. These SG-TFTs have been shown to possess much better electrical performance than polysilicon TFTs due to the location control of the single silicon grains brought about by the μ-Czochralski process. The location control removes the random grain boundaries (GBs) in the channel, which strongly affect carrier mobility, and replaces them by coincident-site-lattice (CSL) grain boundaries in the channel. It has been shown that CSL-GBs have a much lower density of trap states than random GBs [20, 21]. They do still affect the carrier mobility slightly, however.

The SPICE model used in the present study for the modeling of SG-TFTs fabricated by the μ-Czochralski process is derived from the physically based SOI MOSFET SPICE model, suitably modified to take the physical behavior of SG-TFTs into account. The physical modification is implemented in a SPICE-like simulator with the aid of the behavioral language Verilog-A.

2.1 Physically based DC model of SG-TFT

Polysilicon TFTs are modeled using an approach in which the film is treated as an assembly of crystalline grains with a uniform effective state density throughout the film [10, 25–27]. This approach is valid for small or long channels, where grains and random grain boundaries (GBs) are not distinguished because many random GBs are included in the film. The effective mobility μ_{eff} is basically given by the following relation [25]:

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_G} + \frac{1}{\mu_{GB} exp(-\frac{qV_b}{kT})} \tag{2.1}$$

where μ_G is the intra-grain mobility and the second term accounts for the additional scattering at the random GBs that is described by the typical thermionic emission effect. Further, μ_{GB} is the mobility at a random GB and V_b the potential barrier formed at the random GBs. It follows that the effective mobility increases exponentially for low gate voltages, where the thermionic emission dominates, and is constant at high gate voltages. However, as shown by the transconductance characteristic (the transconductance is proportional to the field-effect mobility) of Fig. 2.1, SPICE models based on polysilicon TFT models such as the Rensselaer Polytechnic Institute (RPI) polysilicon TFT model [26], [27] do not fit the measured characteristic of SG-TFTs fabricated by μ-Czochralski technology.

SG-TFTs consist of large silicon crystals separated by few coincident site lattice grain boundaries (CSL-GBs), which have much lower electronic activity than random GBs [17, 20, 28, 29]. Hence, the mobility is much less affected by thermionic emission for low gate voltages and, once it reaches the maximum, gradually decreases for higher gate voltages due to the scattering by surface roughness. This behavior, which is evident from the measured transconductance characteristic shown in Fig. 2.1, is very similar to that of SOI MOSFETs owing to the absence of random GBs. It is not adequately reproduced by the RPI-TFT model, where the mobility only depends on the thermionic emission effect. In other words, the polysilicon model fails to give a proper representation of the physical reality of SG-TFTs and a new approach based

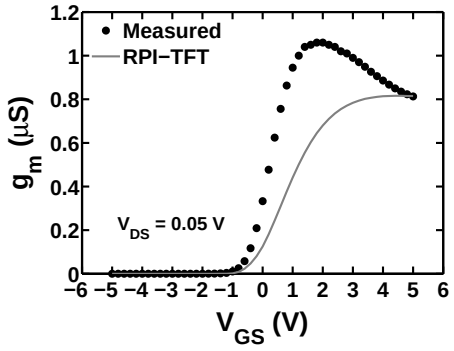


Figure 2.1: Measured transconductance characteristic of SG-TFT compared with simulation by RPI-TFT model.

on large grains must be developed. The basic Berkeley Short-channel IGFET Model (BSIM) SOI SPICE model [30] has been found to meet this requirement. BSIMSOI is a physically based SOI model. It gives a good description of mobility degradation due to scattering from surface roughness. Many other physical effects such as self-heating and the floating body effect are common to both SG-TFTs and SOI MOSFETs, due to the many similarities between these two types of devices. BSIMSOI also includes advanced features, such as short-channel and fully-depleted modeling, which are important for scaling and capturing the characteristics of the near-submicron TFTs needed to realize advanced analog and RF circuits. Furthermore, the model makes extensive use of smoothing functions, thus guaranteeing continuous and smooth modeling across all regions of device operation and ensuring that model remains robust and efficient when implemented in a SPICE simulator.

The new mobility model is obtained by considering total channel resistance as the sum of the resistance of silicon grains and CSL grain boundaries as follows (see Fig. 2.2):

$$R_{ch} = \int_0^L \rho_{eff} \frac{dy}{W t_{si}} \tag{2.2}$$

$$R_{ch} = \int_0^{nL_G} \frac{dy}{W t_{si} q \mu_G n_0} + \int_0^{nL_{GB}} \frac{dy}{W t_{si} q \mu_{GB} n_0 exp(-\frac{V_b}{kT})} \tag{2.3}$$

$$R_{ch} = \rho_{eff} \frac{L}{W} = \frac{nL_G}{W q \mu_G n_0} + \frac{nL_{GB}}{W q \mu_{GB} n_0 exp(-\frac{V_b}{kT})} \tag{2.4}$$

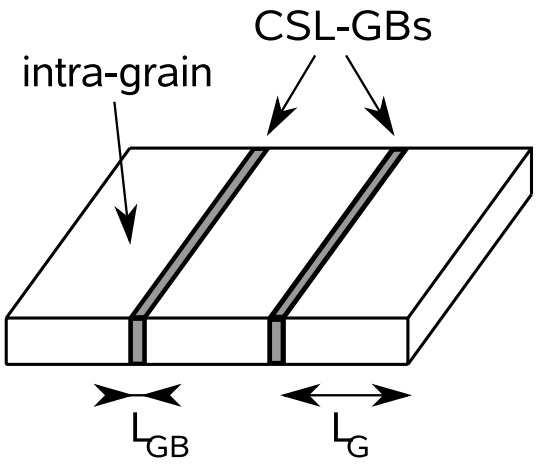


Figure 2.2: Schematic view of SG-TFT channel region with CSL-GBs.

where n is the number of grains separated by CSL-GBs; $L = nL_G + nL_{GB}$, W and t_{si} are the channel length, width and thickness respectively; L_G is the average intra-grain length and L_{GB} the average length of a CSL-GBs length; ρ_{eff} is the effective channel resistivity and n_0 is the carrier concentration. The total effective mobility μ_{eff} is defined as:

$$\frac{1}{\mu_{eff}} = \frac{1-\alpha}{\mu_G} + \frac{\alpha}{\mu_{GB} exp(-\frac{V_b}{kT})} \tag{2.5}$$

where $\alpha = nL_{GB}/L$; μ_{GB} is the inter-grain mobility (the mobility at the CSL-GB) which is estimated to be approximately 200 cm^2/Vs by 2D simulation as described in [20] and μ_G is the intra-grain (the mobility in the silicon grain) described in BSIMSOI by:

$$\mu_G = \frac{\mu_0}{1 + U_a(\frac{V_{gsteff}+2V_{th}}{T_{ox}}) + U_b(\frac{V_{gsteff}+2V_{th}}{T_{ox}})^2} \tag{2.6}$$

where μ_0 is the zero-field carrier mobility (equal to 670 cm^2/Vs for n-channel and 250 cm^2/Vs for p-channel silicon), U_a and U_b are the fitting parameters used to model the amount of degradation due to the average normal electric field, V_{th} is the threshold voltage and V_{gsteff} is the smoothing function given by the following expression:

$$V_{gsteff} = \frac{2n_b v_t ln(1 + \frac{V_{gs}-V_{th}}{2n_b v_t})}{1 + 2n_b C_{ox}\sqrt{\frac{2\phi_s}{qN_{ch}} exp(\frac{V_{gs}-V_{th}}{2n_b v})}} \tag{2.7}$$

where n_b is the ideality factor, v_t is the thermal voltage, C_{ox} is the oxide capacitance, ϕ_s is the surface potential, N_{ch} is the channel doping concentration, T_{ox} is the gate oxide thickness and V_b is the potential barrier height, which decreases with increasing gate voltage [25]. This dependency can be described by the following empirical equation:

$$V_b = \frac{V_{max}}{1 + \vartheta V_{gsteff}} \tag{2.8}$$

where V_{max} is the maximum potential barrier height, which is estimated to be approximately 20 mV by 2D simulation [20] and ϑ is a fitting parameter that describes the reduction in the grain boundary potential as the gate potential increases [25]. The parameter α is a measure of the number of CSL-GBs in the channel, and serves to harmonize the polysilicon and SOI models. It is equal to zero when there are no CSL-GBs in the channel, when the mobility model approaches the formulation used in BSIMSOI. For $0 < \alpha < 1$, the effective mobility varies in accordance with a weighted version of Mathiessen‘s rule, in which the effective mobility depends on the lower mobility term (the weighting ensures that one mobility term contributes more to the final result than the other). For SG-TFTs fabricated by the μ-Czochralski process, there are few CSL-GBs in the grain so α is small; as a result, the intra-grain mobility term μ_G gives a larger contribution to the effective mobility than the inter-grain mobility term μ_B.

The mobility equation employed for the present study uses a smoothing function to ensure continuous, smooth behavior across the thermionic emission and strong inversion region. In the subthreshold region, when $V_{gs} << V_{th}$, V_{gsteff} approaches $exp(V_{gs} - V_{th}/nv_t) << 1$, the intra-grain mobility becomes constant ($\mu_G \approx \mu_0$), and inter-grain mobility approaches $\mu_B \approx \mu_{GB}/exp(qV_{max}/kT)$. Hence, the effective mobility becomes:

$$\frac{1}{\mu_{eff}} \approx \frac{1-\alpha}{\mu_0} + \frac{\alpha}{\mu_{GB} exp(-\frac{V_{max}}{kT})} \tag{2.9}$$

reflecting the thermionic emission effect. In the strong inversion region, when $V_{gs} >> V_{th}$, V_{gsteff} approaches $V_{gs} - V_{th}$, the potential barrier V_b decreases leading to an increase in inter-grain mobility, while the intra-grain mobility

decreases due to the scattering by surface roughness and becomes the dominant term.

$$\frac{1}{\mu_{eff}} \approx \frac{1-\alpha}{\mu_G} \tag{2.10}$$

2.2 Parameters extraction

The accuracy of compact models in circuit simulation depends not only on the correct physical description of various physical phenomena in the device but also on the availability of a reliable, robust and unambiguous parameter extraction methodology. There are in principle two possible strategies for parameter extraction: group extraction and single-device extraction. The latter approach gives an excellent fit for the device under test, since it minimizes the average error between measured and simulated data points, but it does not give a good prediction of the behavior of other devices with different geometries. In group extraction, on the other hand, experimental data from a group of devices are used to extract a complete set of model parameters which also ensure channel scalability. Furthermore, parameters extracted by the group approach are physically more meaningful than those derived from single device extraction, but the resulting fit is characterized by greater error between measured and simulated data points for any single device. This strategy requires a special set of devices: a large base device, used to extract parameters independently for short and narrow channel effects, and two sets of smaller devices one with a fixed channel lengths but different channel widths and another with a fixed channel width but different channel lengths in order to separate the short and narrow channel effects. The group extraction strategy cannot be used for SG-TFTs, since a large device (e.g. W = 20 μm and L = 20 μm) cannot be treated as a SG-TFT. The device has to be included in a single grain, which typically has dimensions of about 6 x 6 μm^2. For that reason, a device with W = 5 μm and L = 5 μm is used as the base device. This device is slightly subject to short channel effects such as the channel length modulation (CLM) effect on output characteristics and the drain-induce barrier lowering (DIBL) effect on the transfer characteristics, and also to impact ionization, reflected in the kink effect on the output characteristics. It follows that short channel effects and impact ionization need to be taken into account even for the base device, making parameters extraction more difficult. Furthermore, the statistical variation of the properties of SG-TFTs means that the parameters have to be extracted from a device whose carrier mobility is equal to the mean value for the group under investigation. After the mobility model developed

has been implamented in BSIMSOI with the aid of the Verilog-A compiler as indicated above, parameter extraction is performed by fitting simulated data to the measured data to obtain a complete set of DC model parameters.

2.3 DC simulation results

Fig. 2.3 shows the comparison of simulated transconductance characteristics (solid lines) with measured results (dots) for n-channel SG-TFTs with 5 μm channel width and length for different excimer laser energies. When the excimer laser (LE) energy is 950 mJ/cm^2, many CSL-GBs are present in the channel and the characteristic is more polysilicon-like. However, the model gives a good fit with the measured results for $\alpha = 0.5$. With a higher laser energy (1070 mJ/cm^2), the mobility increases because there are fewer CSL-GBs in the channel. As a result, the transconductance characteristic is more SOI-like and it is well modeled with $\alpha = 0.25$. α is a crucial parameter directly related to the laser energy, which is also affected by variation. It follows that the typical variations in the fabrication process due to changes in laser-induced-crystallization can be simulated by varying α. Fig. 2.4(a) and 2.4(b) show a

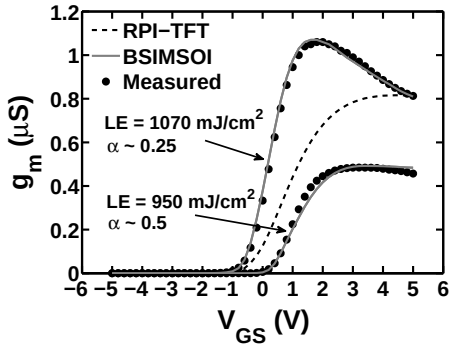


Figure 2.3: Measured and modified BSIMSOI simulation results for n-channel SG-TFTs transconductance characteristics with W = 5 μm and L = 5 μm for different excimer laser energies.

comparison of simulated transfer characteristic with measured data for n- and p-channel SG-TFTs with 5 μm channel width and length, while Fig. 2.4(c) and 2.4(d) show the corresponding comparisons for the output characteristics. Fig. 2.5(a), on the other hand, shows the comparison between measured and simulated output characteristics of n-channel SG-TFTs with a shorter channel length (1.5 μm). These figures illustrate the agreement between measured

characteristics and modified BSIMSOI simulation, and confirm the scalability of the model.

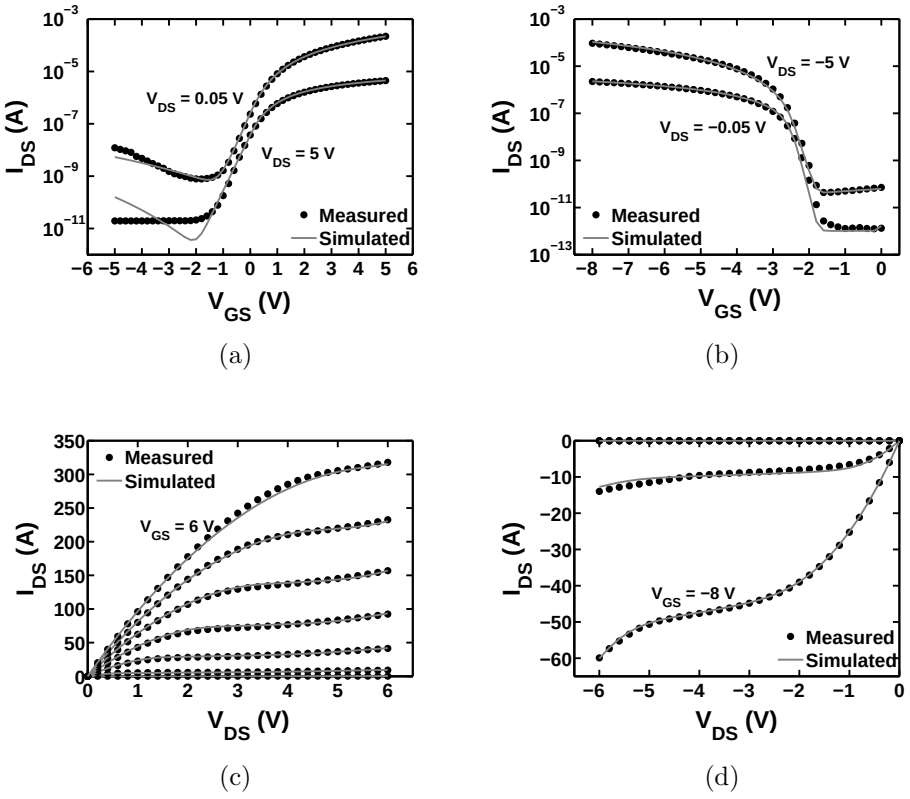
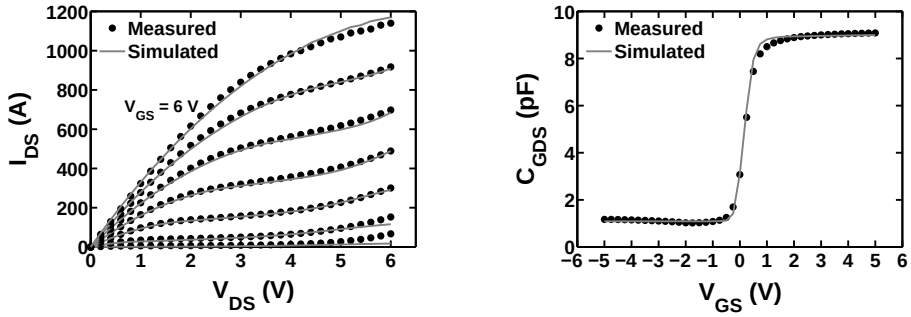


Figure 2.4: Measured and modified BSIMSOI simulation results for SG-TFTs with 5 μm channel width and length. (a) n-channel transfer characteristics (I_{Drain} vs. V_{Gate}) and (c) n-channel output characteristics (I_{Drain} vs. V_{Drain}). (b) p-channel transfer characteristics, and (d) p-channel output characteristics.

After DC parameter extraction and verification, the parameters required for BSIMSOI modeling of AC transistor behavior are determined. Firstly, the simulated capacitance between gate and tied source-drain of SG-TFT devices with 1650 μm equivalent channel width and 5.5 μm channel length is adjusted to fit the parasitic capacitances measured at a frequency of 1 MHz, yielding the results shown in Fig. 2.5(b).



(a) (b)

Figure 2.5: (a) Measured and modified BSIMSOI simulation results for SG-TFTs with 5 μm channel width and 1.5 μm channel length. (b) Measured and modified BSIMSOI simulation results for SG-TFTs with 1650 μm equivalent channel width and 5.5 μm channel length.

2.4 RF SG-TFT model and parameters extraction

For MOSFET operation at very high-frequencies, comparable with the inverse carrier transport time of the channel (non-quasi-static (NQS) regime), the temporal relaxation of the inversion and depletion charges has to be taken into consideration. Most of the MOSFET models used in SPICE are based on the quasi-static assumption (QSA), in which instantaneous charging of the inversion layer is assumed. Circuit simulations using such models will thus fail to predict the performance of the high-speed circuits accurately. The channel of a MOSFET is analogous to a bias-dependent distributed RC network. In QSA, the distributed gate-channel capacitance is lumped into discrete capacitances between the gate and source and drain nodes, ignoring the finite charging time arising from the RC product associated with the channel resistance and the gate-channel capacitance.

One approach used to get round this problem is to model the device by splitting it up into a number of devices (e.g. three), but this leads to an enormous increase in simulation time. Another approach is to use a "table model" obtained by collection of small-signal measurement data. This model can provide quite accurate simulations required for high-frequency circuit design without giving a complete understanding of the physical mechanism of the device. However, the table model does require interpolation functions to generate continuous data at points between data measurement points. Fur-

thermore, the table model is not predictive, because it is not based on device physics. It is only valid for a device operating under the same conditions as the device on which the actual measuremens were performed [31].

The complexity of high-frequency MOSFET modeling led to the macro-modeling approach, which makes use of a commercially available MOSFET model core such us the BSIMSOI model with lumped-element equivalent circuit extensions. The model core and lumped elements compose a sub-circuit representing a RF MOSFET. The macro-modeling approach is attractive for various reasons, such as its the ability to represent the bias and geometry scaling dependences of the RF behavior needed to obtain an accurate prediction of the small-signal characteristics of short channel devices at high frequencies. At the same time, it is important to ensure that all requirements to be met by a MOSFET model for low-frequency applications, such as the continuity, accuracy and scaleability of the DC and capacitance models, should also be met in the RF model. In addition, there are further important requirements on RF models:

- the model should accurately predict the bias dependence of small-signal parameters in RF operation
- the model should correctly describe the nonlinear behavior of the devices in order to permit accurate simulation of inter-modulation distortion and high-speed large-signal operation;
- the model should correctly and accurately predict HF noise; this is important for the design of such device as low noise amplifiers;
- the model should include the NQS effect so it can describe device behavior at very high frequencies where the NQS effect cannot be ignored;
- The components of the equivalent circuit model should be physics-based and geometrically scalable so that the model can be used for predictive and statistical modeling of RF applications.

To ensure that the above requirements are met, the model for the intrinsic device should be designed to include most if not all of the important physical features of a MOSFET device as well as the BSIMSOI model does. BSIMSOI also uses the macro-modeling approach, with the relevant non-quasi-static effects modeled by the lumped gate resistance R_{Gate} superimposed on the BSIMSOI core model developed for large-signal, low-frequency analog applications. Under DC conditions, the gate resistance has no effect. At low frequencies, the gate resistance consists mainly of the resistance of sheet of gate material

(poly-Si, metal). At high frequencies, however, two additional physical effects appear, which affect the value of the effective gate resistance. One is the distributed transmission line effect of the gate material R_{Geltd}, and another one is the first-order distributed channel effect (NQS effect) seen from the gate R_{Gch}, which is a function of both biases and geometry [32]. With the macromodeling approach characterized by the inclusion of the appropriate lumped element to account for RF behavior, the model remains valid under DC conditions.

2.4.1 Modeling extraction strategy

Successful modeling of the RF behavior of a SG-TFT with a modified BSIMSOI depends strongly on the accuracy with which DC curves and capacitances are modeled at low frequencies such as 1 MHz. The procedure used is as follows:

- DC and CV measurements.
- Extraction of modified BSIMSOI model parameters from the DC and CV measurements by the physically based extraction strategy illustrated in Fig. 2.4 above.
- The modeling of the output characteristics and the output resistance R_{out} is very important for the subsequent S-parameter measurements.
- Measurement of S-parameter and proper de-embedding of parasitics.
- The starting point of the S-parameter curves at the lowest frequency can be modeled by fitting the curves with DC and capacitance parameters.
- Extraction of the gate resistance from the input reflection S_{11}.
- Verification of the gate-drain overlap capacitance for the higher frequencies
- Extraction of the substrate resistance network parameters from S_{22}.
- If a good fit can not be found, additional peripheral elements like inductances at drain, gate or source should be added in further sub-circuits.

2.4.2 RF simulation results

Two-port S-parameters of n-channel, multi-finger SG-TFTs with 500 μm equivalent channel width (20 fingers and 5 rows of devices with 5 μm channel

width each) and 1.5 μm channel length are measured over a frequency range of 50 MHz to 6.05 GHz. The test structure designed for the RF characterization of SG-TFTs is shown in the microphotograph of Fig. 2.6. S-parameter data

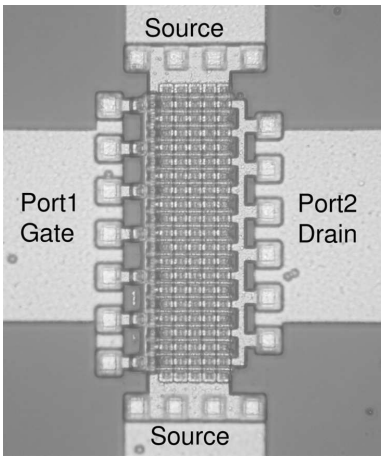


Figure 2.6: Microphotograph of multi-finger, multi-row SG-TFT with 500 μm equivalent channel width (20 fingers and 5 rows of devices with 5 μm channel length each) and 1.5 μm channel length.

is collected as the drain voltage is varied between 3 and 5 V, for gate voltages ranging from 2 to 4 V. Parasitic effects of the transistor test structures are removed by Y/Z-parameter de-embedding in order to obtain the intrinsic transistor behavior at RF [33]. This data is then used to determine the remaining RF parameters for the BSIMSOI model under RF condition. Fig. 2.7 shows the agreement between simulation and S-parameter data after fitting. The absolute RMS error between measured and simulated data is found to be less than 1% over the entire range of bias voltages and frequencies.

2.4.3 Improvement of RF SG-TFT model

As has just been mentioned, the RMS error remains small over a wide range of frequencies. The largest mismatch occurs at the highest frequencies, as shown for S_{11} in Fig. 2.7(a). This is due to the first-order approximations used in BSIMSOI model. The small-signal equivalent circuit of the BSIMSOI model is shown in Fig. 2.8, and the corresponding Y_{11} parameter is approximately given by the expression:

$$Y_{11}(s) \approx \omega^2 (C_{GS} + C_{GD})^2 R_G + j\omega(C_{GS} + C_{GD}) \tag{2.11}$$

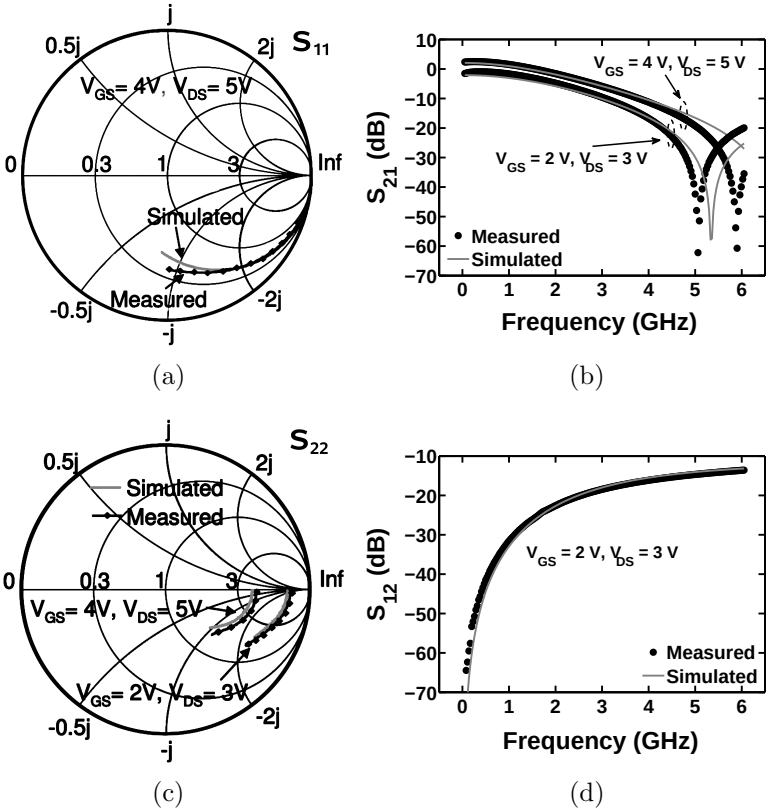


Figure 2.7: Measured and simulated S-parameters of multi-finger, multi-row SG-TFT with 500 μm equivalent channel width and 1.5 μm channel length.

The real part of Y_{11} has a quadratic dependence on the frequency, whereas the measured Y_{11} has a linear dependence on the frequency as shown in Fig. 2.10(a). The mismatch is due to the lossy Si channel with CSL-GBs in it which is better represented by a channel distributed RC effect. Therefore, the SG-TFT operating at radio frequencies is not able to be fully modeled by the first-order non-quasi-static effect, but by a distributed network Z_{ch} in series with the intrinsic device as shown in Fig. 2.9. If the additional lumped elements were resistances, the small-signal equivalent circuit would still approach at first-order approximation model retaining the lowest frequency pole of the original RC network. The corresponding Y_{11} would then be described by the equation:

$$Y_{11}(s) \approx \omega^2(C_{GS}^2 R_{GS} + C_{GD}^2 R_{GD}) + +j\omega(C_{GS} + C_{GD}) \tag{2.12}$$

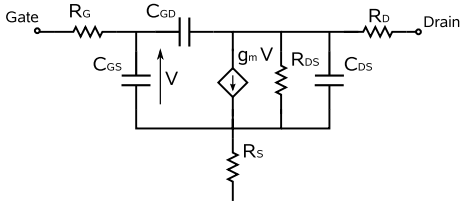


Figure 2.8: Small-signal equivalent circuit of BSIMSOI model.

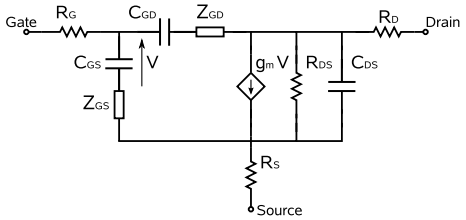


Figure 2.9: High-order small-signal equivalent RF model with additional impedance network.

where the real part of Y_{11} would still have a quadratic dependence on the frequency. At higher frequencies the lossy Si channel of the SG-TFT has to be modeled by means of a higher-order impedance. Since the BSIMSOI model does not include such a channel model, it is added here in the form of a behavioral model based on the Laplace transfer function represented by the following equation:

$$Z_{ch}(s) = \frac{\sum_{k=1}^{n} N_{n-k} s^{n-k}}{s^n + \sum_{k=1}^{n} D_{n-k} s^{n-k}} \tag{2.13}$$

This makes parameter extraction more complex, and the use of optimization algorithms become indispensable. Nevertheless, a good fit between simulated and measured Y_{11} is obtained by using $n = 4$, as shown in Fig. 2.10(a). Furthermore, the higher-order model yields good agreement between the other simulated and measured Y-parameters, as shown in the other graphs of Fig. 2.10.

The higher-order BSIMSOI model also yields a good fit between measured and simulated H_{21} (forward current transfer ratio), as shown in Fig. 2.11. This figure further reveals that the measured current gain-bandwidth f_T is about 6 GHz at $V_{DS} = 5$ V, while $V_{GS} = 4$ V for the n-channel SG-TFT with 500 μm equivalent channel width and 1.5 μm channel length. With unity gain

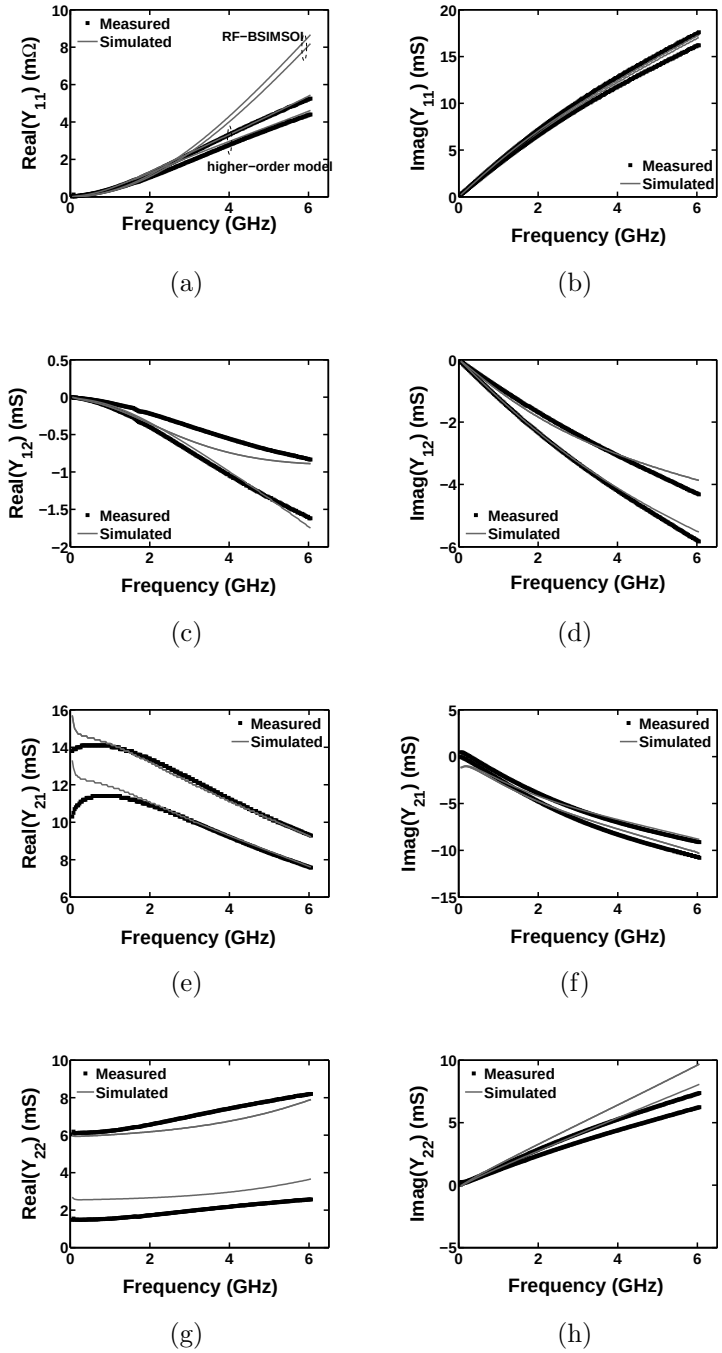


Figure 2.10: Measured Y-parameters of multi-finger, multi-row SG-TFT with 500 μm equivalent channel width and 1.5 μm channel length for $V_{GS} = 2$ V, $V_{DS} = 3$ and $V_{GS} = 4$ V and $V_{DS} = 5$ V, compared with values simulated with higher-order BSIMSOI model.

bandwidth in the 5-6 GHz range, amplifiers can be designed in the sub-1-GHz frequency ranges with expected gains on the order of 10 dB [23, 24].

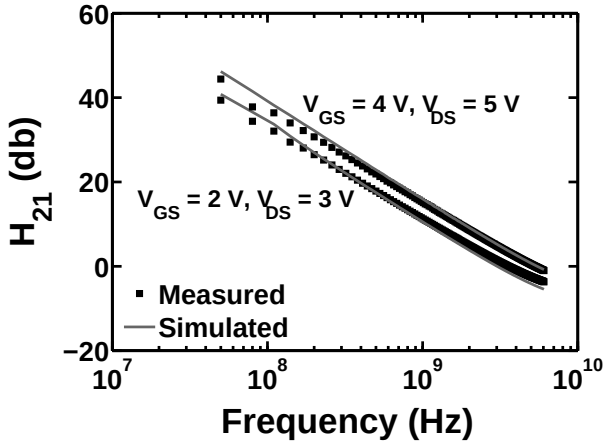


Figure 2.11: Measured H_{21} parameter of multi-finger, multi-row SG-TFT with 500 μm equivalent channel width and 1.5 μm channel length for two different biases, compared with values simulated with higher-order BSIMSOI model.

2.5 Transient SG-TFT model

The NQS model of the transient response of SG-TFTs fabricated by the μ-Czochralski process is described in this section. As mentioned above, circuit simulations are generally based on the quasi-static (QS) approximation, ignoring the carrier transit time along the channel. However, QS approximation models cause enormous errors in simulation of the response to applied voltages varying rapidly with respect to time. This is illustrated in Fig. 2.12 by comparing the results of simulation by a SPICE model embodying a QS approximation with those of 2D TCAD transient simulation. The 2D TCAD simulations were performed by coupling solution of the current, continuity and trap equations. The traps are considered to be uniformly distributed in the channel, and their density of state (DOS) is extracted by fitting the steady-state drain current modeled with $\alpha = 0$ (silicon-on-insulator) and $\alpha = 25\%$ (SG-TFTs) to the measured curves. The BSIMSOI model includes a physical effective gate resistance incorporating the first-order NQS effect. Its value depends on the mobility, which in its turn depends on the quality of the silicon

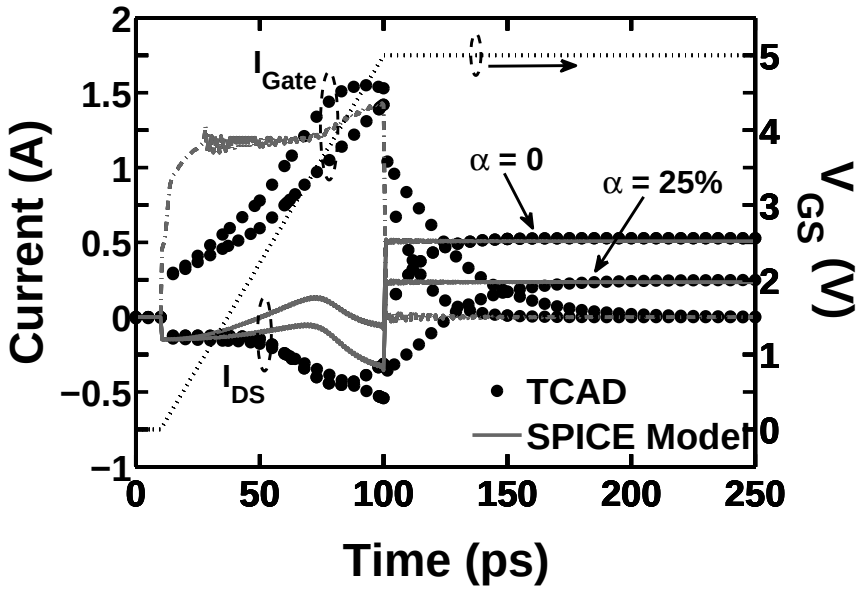


Figure 2.12: Mismatch between TCAD simulation and SPICE modeling embodying a quasi-static (QS) approximation of the drain (I_{DS} (solid lines)) and gate current (I_{Gate} (dash lines)) transient response when a gate voltage of transistor switches from 0 V to 5 V. The TCAD simulation are performed for different DOS distributions, while the SPICE modeling for different α.

layer as reflected by the parameter α in accordance with equation (2.5). As shown in Fig 2.13, the simulation results based on the first-order gate resistance models of Fig. 2.8 do not agree with the 2D TCAD transient behavior because the BSIMSOI transient gives a longer delay and higher gate current than those of the 2D TCAD model. In other words, the NQS model of the gate resistance proposed in BSIMSOI does not represent the transient effect of SG-TFTs adequately. According to the TCAD model, the increase in the density of trap states in the channel leads to a more gradual drain and gate current transient, rather than to a longer delay. Accurately prediction of circuit performance under transient conditions requires a NQS model that takes the carrier-transient delay into account. The delay mechanism could be modeled by segmenting the channel into n pieces, where each piece corresponds to an independent device. However, this approach would lead to a huge increase in calculation time due to the larger number of transistors to be considered. In the present study, the proposed NQS model for SG-TFTs fabricated by the

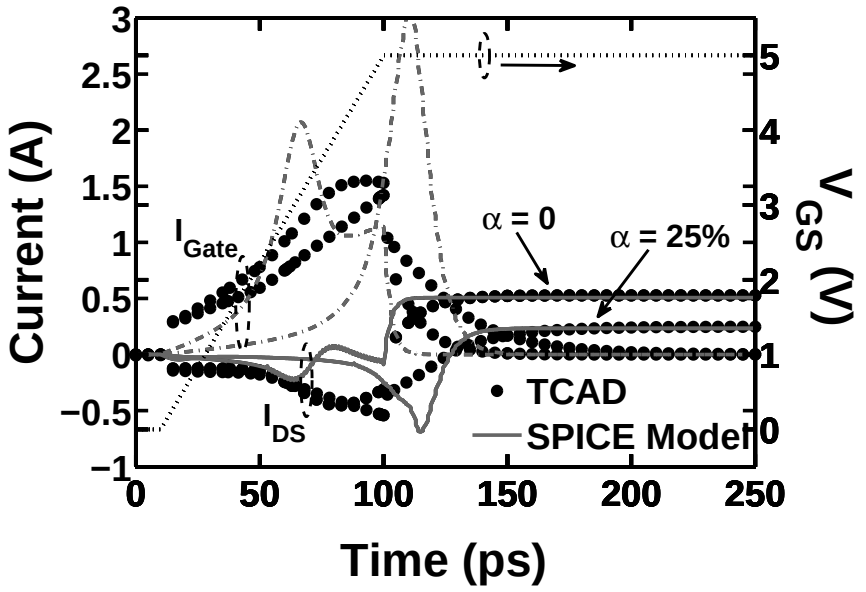


Figure 2.13: Mismatch between TCAD simulation and SPICE modeling embodying a non-quasi-static (NQS) transient BSIMSOI model of the drain (I_{DS} (solid lines)) and gate current (I_{Gate} (dash lines)) transient response when a gate voltage of transistor switches from 0 V to 5 V. The TCAD simulation are performed for different DOS distributions, while the SPICE modeling for different α.

μ-Czochralski process is based on the channel charge relaxation approach implemented in BSIM3 and then in BSIM4 [34, 35]. This model is implemented in the modified BSIMSOI model with the aid of Verilog-A. It consists of an internal node created to keep track of the amount of deficit or surplus channel charge needed to reach equilibrium [35]. As shown in Fig. 2.14, good agreement between the model having α equal to zero (SOI) and equal to 25% (SG-TFTs) with 2D TCAD simulations is obtained for both the drain and gate transient currents.

2.6 Conclusion

In this chapter, a SPICE model of SG-TFTs fabricated by the μ-Czochralski process it is proposed. It is based on the BSIMSOI model, but with a fun-

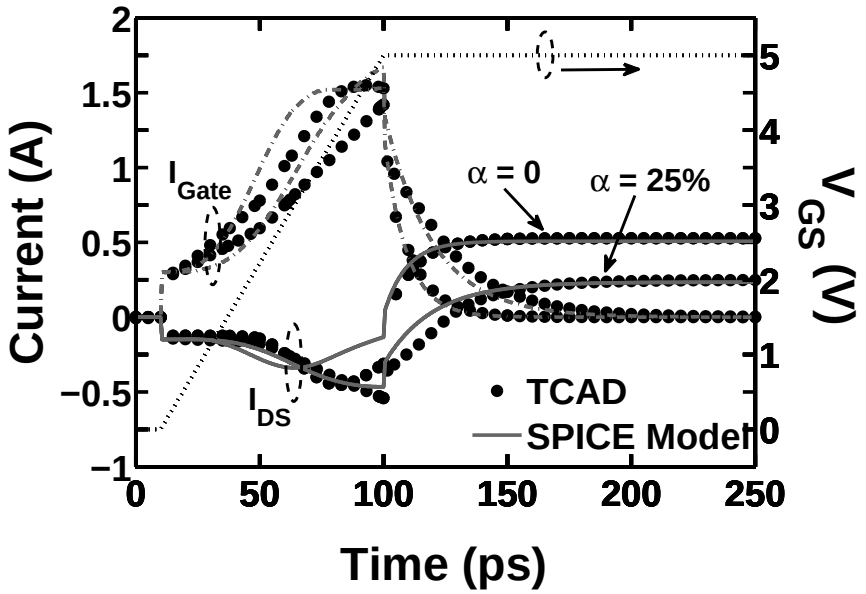


Figure 2.14: Good match between TCAD simulation and SPICE modeling embodying a channel charge relaxation approach to the simulation of SG-TFT drain (I_{DS} (solid lines)) and gate current (I_{Gate} (dash lines)) transient response. The TCAD simulation are performed for different DOS distributions, while the SPICE modeling for different α.

damental mobility modification in order to take the specific properties of SG-TFTs into account. By considering the thermionic emission effect across the CSL-GBs present in the SG-TFT channel, the proposed modified mobility model is able to give good simulation results for both poly-Si devices obtained by silicon crystallization at low laser energy density and SOI device obtained by silicon crystallization at high laser energy density. Furthermore, a distributed network taking the high-order effect of the lossy SG-TFT channel into account has been implemented in the intrinsic RF BSIMSOI model to ensure better matching of measured and simulated Y_{11}. Finally, a NQS transient model based on the channel charge relaxation approach has been added to the developed BSIMSOI model to account for transient behavior. As a result, the finished model gives better agreement with 2D TCAD SG-TFT transient simulations.

Chapter 3

Reliability analysis

The chapter contains an analysis of the reliability of n-channel SG-TFTs fabricated by the μ-Czochralski process with 2 μm channel width and length, an undoped channel 250 nm thick and a gate oxide layer 80 nm thick consisting of SiO_2 deposited by Inductively Coupled PECVD. The degradation effects most likely to occur in n-channel SG-TFTs under different bias-stress are characterized and modeled. In addition, the degradation phenomena to be expected in n-channel SG-TFTs under various bias-stress conditions are predicted. To this end, the relevant model parameters are extracted from the degradation model implemented on a Sentaurus TCAD simulation platform.

3.1 Introduction

Device reliability is an extremely important issue for the application of digital and analog circuits in particular for devices fabricated at low temperatures such as poly-Si TFTs. This is because degradation effects that are directly connected to the defect in the poly-Si layer, oxide, and at silicon-oxide interface are exacerbated at low process temperatures. In general, the reliability of poly-Si is attributed to various phenomena such as: trap generation and injection of charges into the oxide layer, which can have many effects such as mobility degradation, flat-band voltage shift, subthreshold characteristic degradation or an increase in drain and gate leakage currents [36–38]. SG-TFTs, on the other hand, have been shown to have better reliability than poly-Si TFTs due to the absence of random GBs [39]. It is nevertheless appropriate to carry out indepth analysis and modeling of the degradation mechanisms occurring in n-channel SG-TFTs under different bias-stress conditions, reflecting the physics of the trap-state generation in these devices. Such an investigation - the first

to be published, to the best of the author's knowledge - is described in this chapter.

3.2 Degradation model

The standard interpretation of degradation MOSFET devices is that it is an electro-chemical process involving the formation of dangling Si bonds at the Si/SiO_2 interface, most likely due to the breaking of Si-H bonds here [40]. These dangling bonds lead to an increase in the density of states (DOS) in the middle of the bandgap (*deep states*). In SG-TFTs, additionally to the breaking of Si-H bonds at the Si/SiO_2 interface, the degradation phenomena may involve the formation of acceptor-like DOS near to the conduction band (*tail states*) in bulk Si layer due to the deformation of Si-Si covalent weak bonds (bending or stretching) [41]. Experimental studies show that the main degradation phenomena observed in SG-TFTs occur when the device is bias-stressed in the linear region ($V_{DS} < V_{GS}$ - V_{th}) or at strong saturation ($V_{DS} \gg V_{GS}$ - V_{th}). The latter degradation is due to hot carrier generation induced by impact ionization, and is known as the DAHC (drain avalanche hot carrier) effect.

Experimental data on trap state kinetics shows that the time dependence of the generation of single trap can be described by the following power law [40]:

$$N_t = N_t^0 + \frac{N_{nb}^0}{1 + (\nu t)^{-\alpha}} \tag{3.1}$$

where N_t is the concentration of trap at time t, and N_t^0 and N_{nb}^0 are the initial concentrations of traps and bonds (Si-H and Si-Si weak bonds) respectively. The power factor α is stress-dependent, varying between 0 and 1, and ν is the reactor (depassivation) constant. Assuming $N = N_t^0 + N_{nb}^0$ is the total concentration of Si bonds which are able to appear as dangling ones, if hydrogen leaves the Si-H bonds, or stretching ones, if Si-Si weak bond deforms. The concentration of bonds (Si-H and Si-Si weak bonds) remaining after stress is $N_{hb} = N - N_t$ and follows the power law:

$$N_{hb} = \frac{N_{nb}^0}{1 + (\nu t)^{\alpha}} \tag{3.2}$$

Experimental observantion shows that α is equal to $0.5 + \beta$, where β is given by:

$$\beta = \beta_{\perp} F_{\perp} + \beta_{\parallel} F_{\parallel} \tag{3.3}$$

and $F_\perp$ and $F_\parallel$ are normal and parallel components of the electric field F, and $\beta_\perp$ and $\beta_\parallel$ are fitting parameters related to the power factor. An approximate value of ν is given by the Arrhenius equation:

$$\nu = \nu_A exp\left(-\frac{\epsilon_A^0 + \Delta\epsilon_A}{kT}\right) \tag{3.4}$$

where ϵ_A^0 is the activation energy of the bond (Si-H and Si-Si) and $\Delta\epsilon_A$ is the change in the activation energy due to the stretching of the bonds (Si-H and Si-Si) under the influence of the electric field [42] and the change in the chemical potential. It is given by the following equation:

$$\Delta\epsilon_A = \delta_\perp \mid F_\perp \mid^{\rho_\perp} + \delta_\parallel \mid F_\parallel \mid^{\rho_\parallel} + (1+\beta)\, kTln\frac{N - N_{nb}}{N - N_{nb}^0} \tag{3.5}$$

It should be noted that $(N - N_{nb})/(N - N_{nb}^0)$ is the concentration of traps generated expressed as a fraction of the total initial trap concentration; kT times the natural logarithm of this fraction multiplied by the fraction $1 + \beta$ gives the chemical potential of the bonds (Si-H and Si-Si) as the second term in equation 3.5. ν_A is determined from the relation $\nu_0 = \nu_A exp(-\epsilon_A^0/kT_0)$, where ν_0 is the reaction (depassivation) constant at equilibrium, for the passivation temperature T_0 and constant activation energy ($\Delta\epsilon = 0$). $\delta_\perp$, $\delta_\parallel$, $\rho_\perp$ $\rho_\parallel$ are the electric field related fitting parameters of the model. To extract the model parameters, we perform separate analyses of the degradation mechanisms of SG-TFT fabricated by the μ-Czochralski process under the stress of the normal channel electric field $F_\perp$ and parallel channel electric field $F_\parallel$. This can be done by applying the following two bias stress conditions:

1. $V_{DS} < V_{GS}$ - V_{th} corresponding to biasing the device in the linear region;
2. $V_{DS} \gg V_{GS}$ - V_{th} corresponding to biasing the device at strong saturation, where the degradation occurs by impact ionization.

The relation between DOS generation and the normal and parallel channel electric field strengths can be determined on this basis, as described below.

3.2.1 Degradation phenomena of SG-TFTs under linear bias stress

When SG-TFTs are biased in the linear region ($V_{DS} < V_{GS}$ - V_{th}) with a gate voltage of 6 V and a drain voltage of 1 V, the SG-TFT characteristics undergo degradation to an extent that increases with stress time as shown

in Fig. 3.1. The transfer characteristics after bias stress lasting up to 1000 seconds show an increase in subthreshold slope S and mid-gap voltage (V_{mg}) whereas the leakage current and mobility remain largely unchanged. This may be seen from the logarithmic transfer characteristics of Fig. 3.1(a) and transconductance characteristics of Fig. 3.1(b) respectively. Fig. 3.1(c), on the other hand, shows enhancement of gate leakage current when the device is bias-stressed for 100 and 1000 seconds.

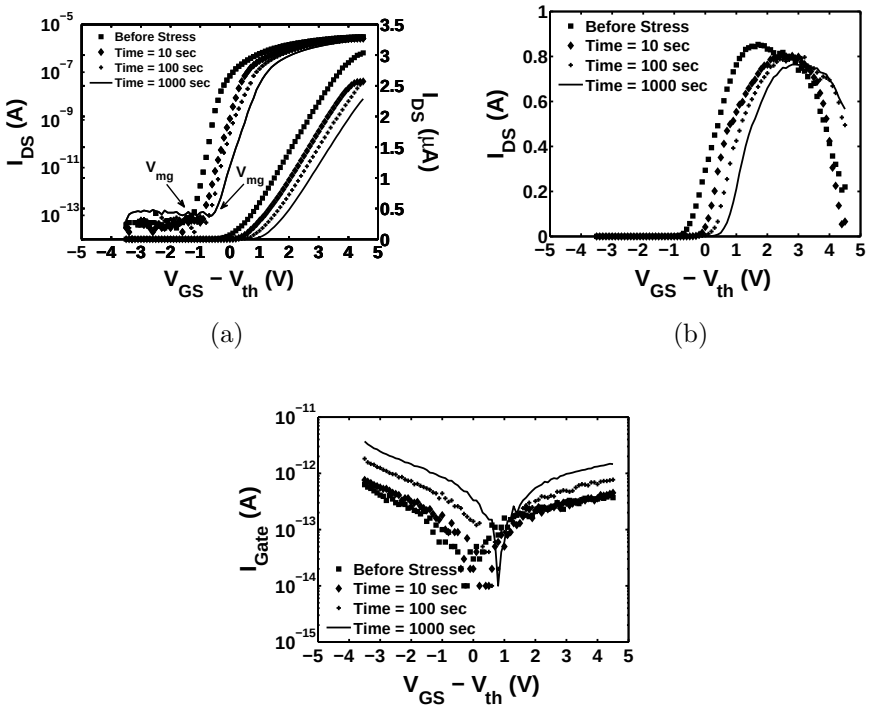


Figure 3.1: Logarithmic and linear transfer characteristics (a), transconductance characteristics (b) and gate current (c) of n-channel SG-TFTs before bias stress and after 10, 100 and 1000 seconds of bias stress with a gate voltage of 6 V and a drain voltage of 1 V.

This degradation mechanism can be explained as being due to the influence of normal electric field, which breaks Si-H bonds at the Si/SiO_2 interface, leading to an increase in DOS at deep levels near the Si/SiO_2 interface and thus influencing the subthreshold slope S. The normal electric field bias stress also damages the gate oxide layer, since the increase in the mid-gap voltage

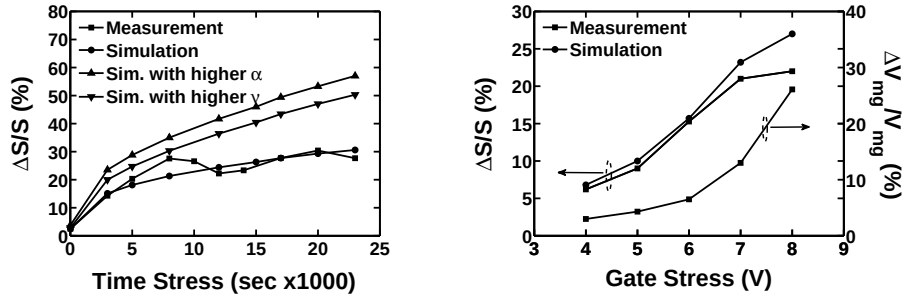
V_{mg} is due to injection of channel carriers (in this case electrons) into the gate oxide. It is important to noted that DOS at interface do not contribute any V_{mg} shift as do for the threshold voltage V_{th}, but a shift of V_{mg} is only due to trapped charge into the oxide as mention in the literature [43]. For that reason, the analysis of the oxide degradation will be focus on the the shift of V_{mg} instead of V_{th}.

The increase in gate leakage current is also caused by degradation of the gate oxide. The gate oxide, as insulator, has a high resistivity. However, current can flow through it due to a tunneling effect. Two kinds of tunneling effect may be involved here [43]: direct tunneling, which is dominant in thin gate oxide layers, and Fowler-Nordheim tunneling that is dominant in thick gate oxide layers as are found in the case studied here. The increase in gate leakage current when the device is under bias stress can be explained by the generation of traps in the oxide due to the release of hydrogen allowing more current to flow through the oxide layer since these traps act as *stepping stones* for tunneling carriers; this effect is known as trap-assisted tunneling [43].

Experimental results. Prolonged stress leads to an increase in mid-gap voltage V_{mg} due to the injection of electrons into the oxide, which modifies the applied effective normal electric field. The strategy used to extract the parameters of the physical degradation model under linear bias stress is designed to separate these two degradation mechanisms: increase of DOS and of mid-gap voltage V_{mg}. To this end, a gate-voltage bias stress as low as 4 V is applied to the device for 23000 seconds (slightly more than 6 hours). This leads to an increase of subthreshold slope S, as shown in fig. 3.2(a) whereas the mid-gap voltage V_{mg} is changed of only a few per cent.

In order to analyze the dependence of SG-TFT degradation on the normal electric field bias stress, the device under test was stressed by applying various gate voltages up to a maximum of 8 V for periods of 100 seconds each. Figure 3.2(b) shows linear degradation of the subthreshold slope S up to a gate voltage of 6 V. At higher gate-voltage bias stresses, the relative change in degradation is lower because of the reduction of the effective normal electric field due to the increase in V_{mg} caused by the electron injection into the oxide.

Parameters extraction. An inverse modeling approach was adopted, in which the subthreshold slope degradation $\Delta S/S$ and mid-gap voltage degradation $\Delta V_{mg}/V_{mg}$, which describe the degradation behavior of SG-TFTs under a normal electric field, were used as input for the 2D TCAD simulator (Sentaurus TCAD platform [44]). Device simulations were performed, where equations (3.1) and (3.2) of the degradation model were self-consistently solved with all



(a) (b)

Figure 3.2: (a) Measured and simulated degradation of the subthreshold slope $\Delta S/S$ after application of a gate voltage of 4 V and a drain voltage of 1 V for a period of up to 23000 seconds. (b) Measured and simulated degradation of the subthreshold slope $\Delta S/S$ and measured mid-gap voltage V_{mg} after application of different gate bias stresses for 100 seconds each.

transport equations.

Model fitting parameters such as the component of the power factor $\beta_\perp$, the ones of the normal electric field $\delta_\perp$, $\rho_\perp$, and the total concentration of silicon bonds, which are able to be broken becoming dangling bonds ($N(E)$), were determined by fitting the dependence of $\Delta S/S$ on stress time and gate-voltage bias stress to the experimental results. $N(E)$ were determined in the range of energy levels included between 0 eV and 0.2 eV (*deep states*) which influence only the subthreshold region. Fig. 3.3 shows the corresponding $N(E)$ extracted for different energy level normalized to an initial DOS distribution $N(E)_t^0$.

The mid-gap voltage degradation $\Delta V_{mg}/V_{mg}$, on the other hand, can be used for extracting the negative charge injected into the oxide. The remaining model parameters were determined in accordance with the procedures described in the literature [40, 45]: the equilibrium depassivation coefficient ν_0 as 8x10^{-10} sec^{-1}, the Si-H equilibrium activation energy ϵ_A^0 as 3.2 eV (see Table 3.1).

The simulation results are plotted in Fig. 3.2 together with the measured ones. Fig. 3.2(a) shows the simulated degradation of subthreshold slope $\Delta S/S$ in comparison with measured data together with simulation results for a higher power factor $\beta_\perp$ and a lower normal field parameter $\delta_\perp$, leading to higher values of α and ν respectively, and hence to a stronger degradation effect. Fig. 3.2(b) shows the measured and simulated subthreshold slope $\Delta S/S$ degradation for different gate bias stress conditions. The reduction of $\Delta S/S$ degradation for

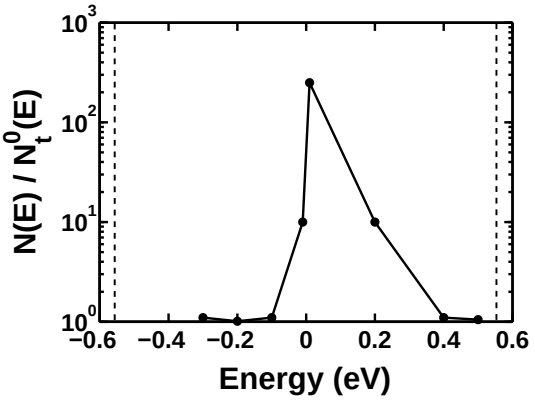


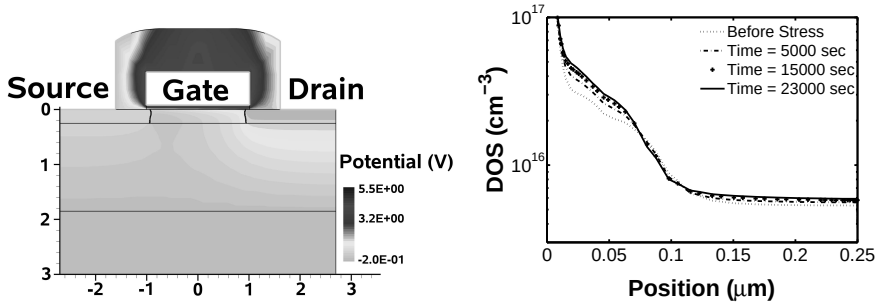
Figure 3.3: Total concentration of silicon bonds which are able to be broken becoming dangling bonds ($N(E)$) normalized to an initial DOS distribution $N(E)_t^0$.

gate bias stress higher than 6 V is also simulated, once the enhancement of V_{mg} is taken into account. Fig. 3.4 presents simulation results for a SG-TFT under linear bias stress with stress times up to 23000 seconds. Fig. 3.4(a) shows the potential profile of the device, while Fig. 3.4(b) shows the spatial generation of $\int_{Ev}^{Ec} N_t(E)\,dE$ perpendicular to the channel with stress times. This is physically consistent with the fact that dangling bonds are generated at Si/SiO_2 interface.

3.2.2 Degradation phenomena of SG-TFTs under strong saturation bias stress

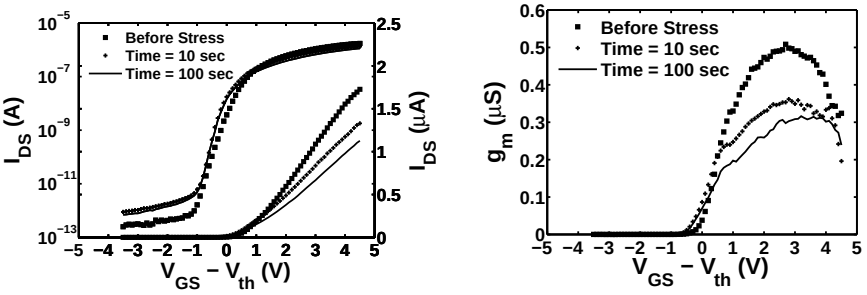
When the SG-TFT is bias-stressed at strong saturation ($V_{DS} \gg V_{GS}$ - V_{th}) with a drain voltage of 9 V and a gate voltage such as V_{GS} - V_{th} = 1 V, the SG-TFT characteristics show strong degradation with increasing stress time as may be seen from Fig. 3.5. The logarithmic transfer characteristics of Fig. 3.5(a) show that the subthreshold slope S is not substantially changed, the mid-gap voltage V_{mg} is slightly reduced and the leakage current is increased. On the other hand, the transconductance is drastically reduced, as may be seen from Fig. 3.5(b).

This degradation mechanism is due to the drain avalanche hot carrier (DAHC) effect. When a high drain voltage is applied to the device, hot carriers are generated close to the drain region where electric field is highest. These



(a) (b)

Figure 3.4: (a) Simulated potential profile of SG-TFT for gate voltage of 4 V and drain voltage of 1 V. (b) Simulated spatial DOS (uniformize in bandgap) perpendicular to the channel before stress and after a gate voltage of 4 V and a drain voltage of 1 V have been applied for periods up to 23000 seconds.



(a) (b)

Figure 3.5: (a) Logarithmic and linear transfer characteristics of n-channel SG-TFTs before stress and after 10 and 100 seconds of 9 V drain voltage and 1 V gate voltage bias stress. (b) Transconductance characteristics under the same conditions.

hot carriers can be injected into the oxide layer, flow through the oxide (giving rise to a current I_G), generate DOS near to the channel-drain junction and at interface or accumulate at the bottom of the channel region and act as the base current of a parasitic bipolar junction transistor (BJT) to induce positive drain current feedback known as the kink effect; all these effects are illustrated in Fig. 3.6. Furthermore, if the device has a body contact, some of the hot carriers can flow through to it as a body current (I_{BS}). As a consequence, a device must have body contact to characterize the kink effect. In the present

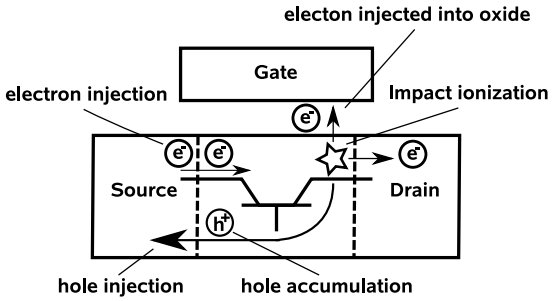


Figure 3.6: Schematic cross-sectional view of hot-carrier effects in TFTs subject to a floating body effect.

study, an H-gate SG-TFT is proposed as an example of a device with two such body contacts (see Fig. 3.7). Fig. 3.8(a) shows the output characteristics of

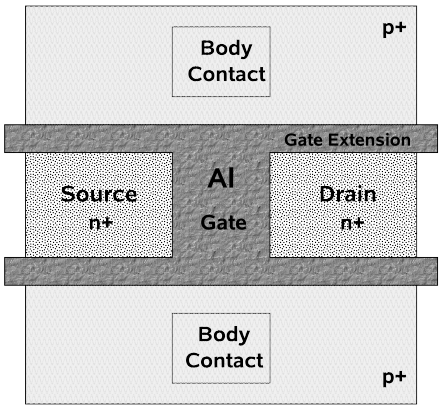


Figure 3.7: Schematic top view of H-gate SG-TFT

an n-channel H-gate SG-TFT for gate voltages sweeping from 0 to 5 V in 1 V steps. The typical drain current enhancement at high drain voltages due to impact ionization (the kink effect) may be clearly seen. The corresponding body current I_{BS} is plotted in Fig. 3.8(b). This graph shows two regions, one where the body current remains constant as the drain voltage increases but is dependent on the gate voltage, and the other one where the body current increases with the drain voltage. In the first region, the body current may be attributed to the parasitic PIN diodes of the H-gate structure. It increases with gate voltage because of the tunneling effect between the P+ body region

and the inversion layer under the gate extension due to the strong drain-body electric field [46]. In the second region, the body current arises from hot carriers induced by impact ionization. It may be seen from Fig. 3.8(b) that when the gate voltage is increased, the drain voltage at which the body current starts to arise also increases. This confirms that the body current is derived from hot carriers induced by impact ionization, when the device is biased at strong saturation. The highest body current occurs for gate voltage of 2 V. The plot of the measured body current of the n-channel H-gate SG-TFT against the gate voltage shown in Fig. 3.8(c) confirms that the highest body current corresponds to a gate voltage of 2 V and a drain voltage of 10 V. When the drain voltage is as low as 0.05 V, a leakage current flows through

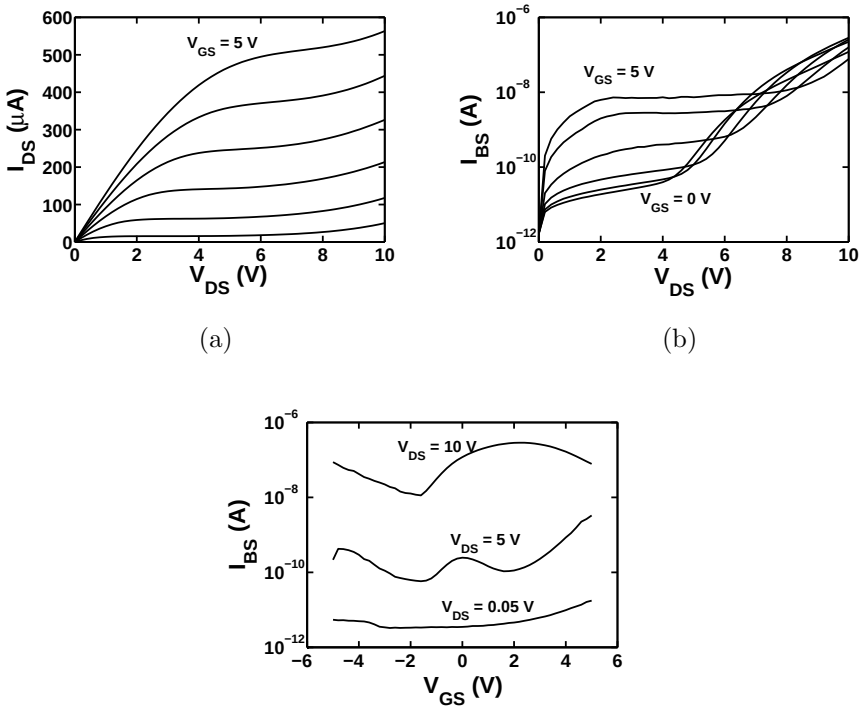


Figure 3.8: (a) Measured output characteristics of H-gate SG-TFT. (b) Body current I_{BS} of the same device as a function of drain voltage. (c) Body current as a function of gate voltage.

a body contact. This could be due to leakage from the parasitic PIN diodes of the gate extension. With drain voltage of 5 V, the body current peak is

around 0 V; this corresponds to the strong saturation condition where hot carriers are generated. After a slight dip, the body current then increases again with gate voltage. That is explained by the above-mentioned tunneling effect between the P+ body region and the inversion layer under the gate extension [46]. When a 10 V drain voltage is applied, the peak body current increases due to the strong saturation of the device leading to high generation of hot carriers. Finally, the maximum degradation due to the DAHC effect is found at maximum body current, where the highest hot carrier generation occurs.

Experimental results. In order to analyze the dependence of SG-TFT degradation on the parallel electric field bias stress, the device under test was stressed by applying drain voltage of 7 V and V_{GS} - V_{th}= 1 V up to 1000 seconds. This bias stress induces mobility degradation due to DAHC effect as shown by changes in the transconductance g_m in Fig. 3.9(a), while the subthreshold slope S is substantially unchanged, as may be seen from Fig. 3.9(b). That is due to the generation of acceptor-like DOS (*tail states*) near the edge of conduction band may be due to the bending or stretching of Si-Si weak bonds which only affects the mobility, whereas the subthreshold slope S remains unchanged as will be confirmed by the simulation results presented in section 3.3.

The mid-gap voltage V_{mg}, on the other hand, is reduced at the application of the first drain-voltage bias stress, then remains constant with increasing stress time (see Fig. 3.9(b)). That can be explained by self-limiting injection of positive hot carriers (holes) generated by impact ionization into the oxide.

Furthermore, various drain voltages up to a maximum of 10 V for periods of 100 seconds each is applied to the device under test. Figure 3.2(b) shows the transconductance g_m decreases with the bias stress due to mobility degradation, whereas the mid-gap voltage V_{mg} remains constant after a slight decrease due to hot holes injected into the oxide. The leakage current degradation is also independent of the stress time and is not a major degradation issue for SG-TFTs under bias stress. We will therefore not take it into account in our further considerations.

Parameters extraction. An inverse modeling approach was adopted, in which the transconductance degradation $\Delta g_m/g_m$, which describes the degradation behavior of SG-TFTs under a parallel electric field, was used as input for the 2D TCAD simulator (Sentaurus TCAD platform [44]). Device simulations were performed, allowing model parameters such as the component of the power factor $\beta_{\|}$, the parallel electric field parameters $\delta_{\|}$, $\rho_{\|}$, and to-

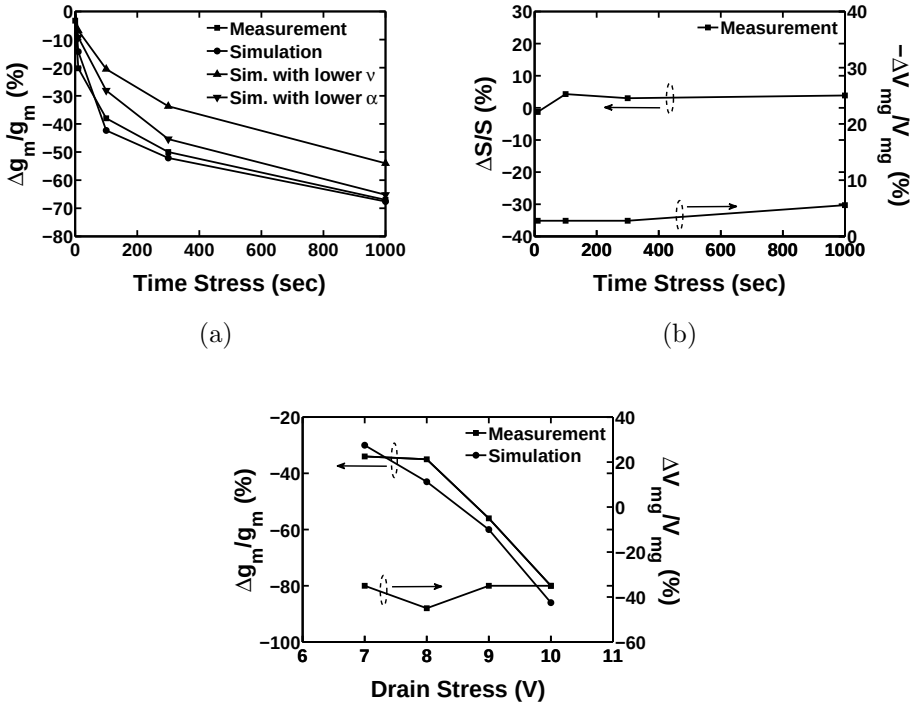


Figure 3.9: (a) Measured and simulated degradation of transconductance after application of a drain voltage of 7 V and a V_{GS} - V_{th}= 1 V for a period of up to 1000 seconds. (b) Measured degradation of subthreshold slope $\Delta S/S$ and mid-gap voltage V_{mg} under the same conditions. (c) Measured and simulated degradation of the transconductance and measured mid-gap voltage V_{mg} after application of different drain bias stresses for 100 seconds each.

tal concentration of silicon bonds, which are able to be stretched or bended becoming tail states ($N(E)$), to be determined by fitting the dependence of $\Delta g_m/g_m$ on stress time and drain-voltage bias stress to the experimental results. $N(E)$ were determined in the range of energy levels included between 0.4 eV and 0.5 eV (*deep states*) which influence only the mobility. Fig. 3.10 shows the corresponding $N(E)$ extracted for different energy level normalized to an initial DOS distribution $N(E)_t^0$.

The mid-gap voltage degradation $\Delta V_{mg}/V_{mg}$was used to extract the positive charge injected into the oxide. The remaining model parameters were determined as described above (see Table 3.1).

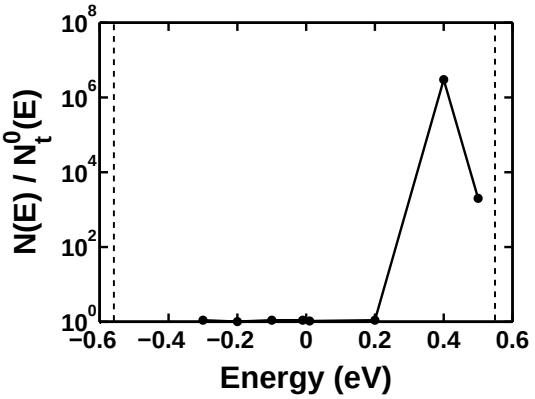


Figure 3.10: Total concentration of silicon bonds, which are able to be stretched or bended becoming tail states ($N(E)$) normalized to an initial DOS distribution $N(E)_t^0$.

The simulation results are plotted in Fig. 3.9. Fig. 3.9(a) shows the simulated degradation of the transconductance $\Delta g_m/g_m$ fitted to the measured data. It also shows that simulation with a lower power factor parameter $\beta_{\|}$ and a higher parallel field parameter $\delta_{\|}$, which lead to lower values of the parametes α and ν respectively, gives less degradation. Fig. 3.9(c) shows the measured and simulated degradation of the transconductance characteristic $\Delta g_m/g_m$ under different drain-bias stress conditions. The simulation results for a SG-TFT under strong saturation bias stress are plotted in Fig. 3.11. Fig. 3.11(a) shows the potential profile of the SG-TFT when a drain voltage of 7 V and a gate voltage of 1 V are applied to the device. Fig. 3.11(b) shows the corresponding impact ionization (which occurs in the channel region close the drain-channel junction), Fig. 3.11(c) the cross-sectional profile parallel to the channel where impact ionization occurs, and Fig. 3.11(d) the spatial generation of $\int_{Ev}^{Ec} N_t(E)\,dE$ parallel to the channel near to the drain-channel junction with stress times. It may be seen from this last-mentioned figure that DOS are mainly generated close to the drain-channel junction where impact ionization takes place. This may be explained by the fact that the high electric field causes stretching or bending of Si-Si weak bonds with consequential tail states formation. The complete list of extracted parameters are given in Table 3.1.

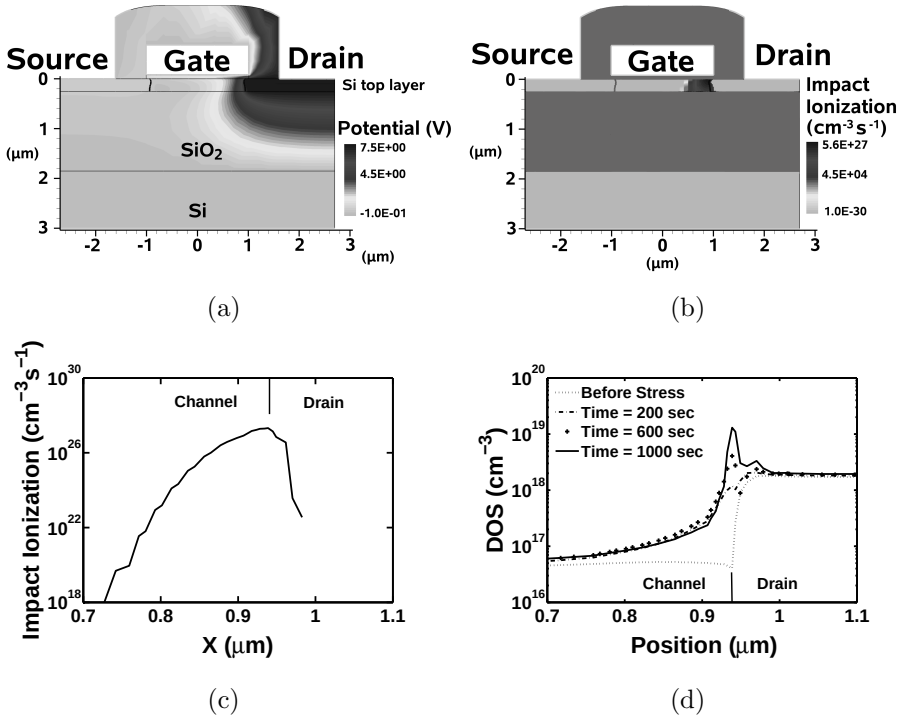


Figure 3.11: (a) Simulated potential profile of SG-TFT for drain voltage of 7 V and gate voltage of 1 V; (b) corresponding simulated impact ionization occurring in the channel near the drain region; (c) cross-sectional profile of impact ionization parallel to the channel; and (d) simulated spatial DOS (uniformize in bandgap) near to the drain-channel junction before and after application of bias stress of drain voltage of 7 V and gate voltage of 1 V applied for 200, 600, and 1000 seconds.

3.3 Simulation of SG-TFTs under bias stress

The degradation of SG-TFTs under bias stress may be predict as follows. After the DOS distribution of the SG-TFTs before stress has been extracted to model their transfer characteristic, the degradation of the SG-TFTs under linear and strong saturation bias stress is simulated with the aid of the extracted parameters (in Table 3.1 and plots of Fig. 3.4(b) and 3.11(d)) and is then compared with measured results of this degradation.

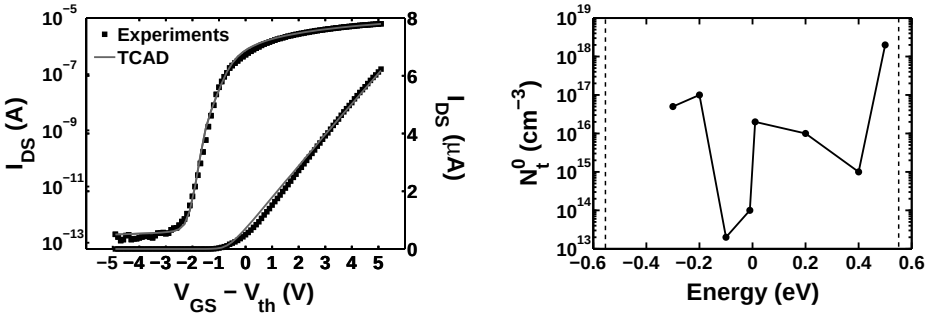
Model Parameters	
$\rho_{\perp}$	0.27
$\rho_{\parallel}$	0.33
$\beta_{\perp}$	-12.5x10^{-7} V^{-1}cm
$\beta_{\parallel}$	-4x10^{-7} V^{-1}cm
$\delta_{\perp}$	2x10^{-3} eVcm$^{\rho}$V$^{-\rho}$
$\delta_{\parallel}$	1.8x10^{-3} eVcm$^{\rho}$V$^{-\rho}$
ϵ_A^0	3.2 eV
ν_0	8x10^{-10} s^{-1}

Table 3.1: Extracted parameters of the degradation model under linear and strong saturation bias stress.

3.3.1 Modeling of SG-TFTs before bias stress

The electrical characteristics of poly-Si TFTs can be adequately described on the assumption of the presence of a density of states (DOS) uniformly distributed within the channel [47–49]. In particular, assuming large inter-grain defect densities to be present both in deposited polysilicon and in solid phase crystallized polysilicon [47], the DOS can be interpreted as a result of averaging DOS at grain boundaries, front and rear Si/SiO_2 interfaces. The energy distribution of the a-Si and poly-Si DOS is usually modeled in the TCAD simulator by four exponential terms, two of which are located in the lower half of the bandgap (*donor-like*) and two in the upper half of the bandgap (*acceptor-like*) [50] to obtain the typical U-shaped DOS distribution in the bandgap. This approximation would however not seem to be appropriate for SG-TFTs fabricated by the μ-Czochralski process, since the high crystallographic quality of the grains in these devices would suggest that the vast majority of defects will be concentrated at the CSL grain boundaries and the front and rear Si/SiO_2 interfaces. Hence, a more realistic approach to the analysis of SG-TFTs would be based on discretization of the active layer into crystalline grains separated by CSL grain boundaries [20, 51, 52]. However, this approach presents a major problem: the choice of the location of the CSL grain boundaries with respect to the drain junction. In fact, it has been shown that the electrical characteristics at high electric fields (both off-current and kink regime) are highly sensitive to the position of the trap states associated with the grain boundary, since the local electric field is strongly influenced by the local space charge [53], An additional consideration is that parameter extraction becomes much more complex under these conditions. This makes

the possibility of describing the electrical properties of SG-TFTs on the basis of the effective DOS model very attractive, in spite of the actual defect distribution in such material. The solution proposed here is to consider a specially uniform DOS distribution in the single silicon grain that takes into account the DOS distribution at CSL grain boundaries and at front and rear Si/SiO_2 interfaces. Furthermore, instead of using the typical U-shaped DOS distribution, a user-defined discrete DOS distribution is proposed in which each individual DOS is given as a pair of energies and the corresponding concentrations. This DOS model is favorable for two reasons: firstly, it gives a better fit with the SG-TFTs characteristics since the DOS distribution will not have the usual U-shape but will peak in the middle of the bandgap; and secondly, the degradation model will have an independent effect on each DOS level. The higher the number of DOS to be accounted for in the bandgap, the more accurate the fit is. However, the extraction complexity increases enormously with the number of DOS levels. The number of DOS levels used in the present study is 5. The discrete DOS distribution is obtained by fitting the simulated transfer characteristic to the experimental transfer characteristic measured at 0.05 V drain voltage. Donor-like trap states are used to fit the leakage current. The mid-gap acceptor-like trap states affect the subthreshold region, while the highest energy acceptor-like trap states influence the above threshold region. The extracted DOS distribution shown in Fig. 3.12(b) gives a good fit between simulation and measurement, as shown in Fig. 3.12. It should be pointed out



(a) (b)

Figure 3.12: (a) Measured and simulated transfer characteristics of SG-TFTs for $V_{DS} = 0.05V$ before stress. (b) Extracted DOS distribution before stress.

that the simulated characteristics are obtained by fitting only the energy level and concentration of the DOS distribution, keeping the capture cross-section of the trap states and the carrier mobility constant. Many authors have used

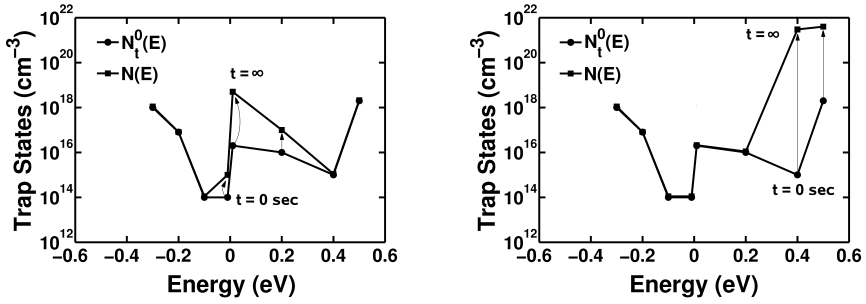
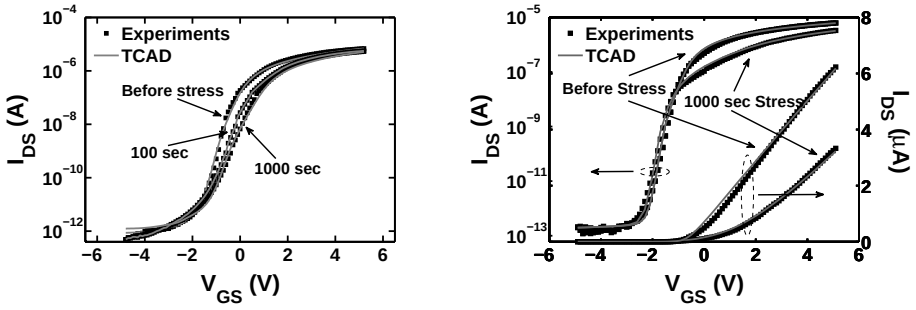


Figure 3.13: DOS distributions before and after a time approaching infinity under a gate-bias stress (a) and a drain-bias stress (b).

the carrier mobility as an additional fitting parameter in the above threshold voltage region [47–49, 52]. In the present work, the carrier mobilities are set to their bulk default values (1417 cm^2/Vs for electrons and 470.5 cm^2/Vs for holes) as determined by the contributions of the various relevant effects such as phonon scattering, doping dependence and interface degradation, and combined by means of Mathiessen's rule [44].

3.3.2 Modeling of SG-TFTs under bias stress conditions

The degradation of SG-TFT linear and strong saturation bias stress can be predicted by superimposing the degradation model described above and the extracted parameters listed in Table 3.1 and plotted in Fig. 3.3 and 3.10 on the SG-TFT model before stress. Fig. 3.13 shows the DOS distribution before and approaching infinity under linear and strong saturation bias stress. As may be seen from Fig. 3.13(a), the density of acceptor-like trap states in the middle of the bandgap is increased when gate-bias stress is applied to the device, while as may be seen from Fig. 3.13(b), application of a drain-bias stress leads to an increase in the density of high-energy acceptor-like traps near the conduction band. The resulting degraded transfer characteristics are shown in Fig. 3.14, which gives a good prediction of the SG-TFT degradation under bias stress. The degradation model predicts subthreshold slope S degradation and injection of negative changes into the gate oxide due to V_{mg} enhancement when a gate voltage of 8 V and drain voltage of 1 V are applied to the device for 100 and 1000 seconds stress, as shown in Fig. 3.14(a). It further predicts



(a) (b)

Figure 3.14: Measured and simulated transfer characteristics before and after V_{GS} = 8 V and V_{DS} = 1 V bias stress (a) and V_{DS} = 7 V and V_{GS} - V_{th} = 2 V bias stress (b).

the mobility degradation and positive charge injection into the gate oxide due to V_{mg} reduction, when a drain voltage of 7 V and V_{GS} - V_{th} = 2 V are applied to the device for 1000 seconds as shown in Fig. 3.14(b).

3.4 Conclusion

This chapter presents an analysis of the degradation mechanisms under different bias stress conditions in SG-TFTs fabricated by the μ-Czochralski process. The strategy used to extract the degradation model parameters is based on consideration of the response to linear and strong saturation bias stress. It has been found that application of a linear bias stress to the device leads to generation of deep acceptor-like states near the Si/SiO_2 interface and injection of electrons into the oxide, and thus to enhancement of the subthreshold slope S and mid-gap voltage V_{mg}. On the other hand, applications of a strong saturation bias stress to the device leads to the generation of acceptor-like tail states near the drain region and injection of hot holes into the oxide, and thus to a drop in mobility and mid-gap voltage V_{mg}. It has further been shown that the degradation of the transfer characteristic of SG-TFTs fabricated by the μ-Czochralski process under the two different bias stress conditions can be correctly predicted by 2D TCAD simulation with the aid of parameters extracted as described above.

Chapter 4

Electronic paper

The focus in this chapter is on the design and fabrication of electronic paper (E-Paper) based on SG-TFTs, with an active-matrix quick-response liquid-powder display (AM-QRLPD). QR-LPD is a technology developed by Bridgestone that shows excellent image stability, quick response, high resolution, clear threshold characteristics and low power consumption [54]. Bridgestone Corporation has demonstrated a functioning flexible QR-LPD E-Paper, with passive-matrix (PM) addressing [55] and active-matrix (AM) addressing by organic TFTs (OTFTs) [56]. While AM addressing offers obvious advantages over PM addressing, OTFTs used to implement AM-QRLPD have such low mobility that it is impossible to build driver circuits and make fully integrated E-Paper on this basis. As part of the present investigation, a study has been made of the possibility of designing an AM-QRLPD based on SG-TFT fabricated by the μ-Czochralski process, where the SG-TFTs used for the display operate at a high voltage (70 V) and are combined with the conventional low-voltage SG-TFTs employed for the driver circuits to obtain a fully integrated AM-QRLPD E-Paper.

This chapter is arranged as follows. After an explanation of the motivation behind this study in section 4.1 and a description of the frontplane QR-LPD technology developed by Bridgestone in section 4.2, the considerations underlying the design of the backplane are discussed in section 4.3. The heart of this chapter, a discussion of the development of reliable n- and p-channel SG-TFTs operating at 70 supply voltage (HV-SGTFTs) for use in E-Paper, is to be found in section 4.4. The chapter closes with a review of the display organization and of the means used to integrate the display with high-speed SG-TFT driver circuits operating at low supply voltage (LV-SGTFTs).

4.1 Motivation

Electronic paper, also called E-Paper, is a new display technology that unlike the conventional flat panel display, which uses a backlight to illuminate its display cells (pixels), reflects light like ordinary paper. It is capable of holding text and images for a very long time without power consumption. It is flexible and the aim is to make it actually rollable. Many companies are focusing research on this new and exciting field. The Bridgestone Corporation has succeeded in developing an E-Paper based on the quick-response liquid-powder display (QR-LPD) technology (Fig. 4.1). QR-LPD shows excellent image stability, quick response, high resolution, clear threshold characteristics and low power consumption. These features make it possible to design QR-LPD E-Paper with a passive-matrix (PM) addressing system [55]. The

Figure 4.1: A QR-LPD display developed by the Bridgestone Corporation.

main advantage of PM addressing is its simplicity. Only horizontal and vertical wires extending across the whole screen, are needed to drive the display. The drawbacks of PM addressing are the crosstalk between the wires and potentially low writing speed. Nevertheless, these drawbacks are dealt with in QR-LPD technology. As regards the crosstalk, QR-LPD has clear threshold voltages (35 V) and high supply voltage (70 V) that make it suitable for PM addressing because of the wide ON/OFF margin. Indeed, as shown in Fig. 4.2, when the first row is activated with 70 V, data applied to all column (data) lines can be written to the corresponding row without problems. Crosstalk to adjacent rows is excluded by the voltage margin of 35 V, which ensures that only the pixels on the activated row can have a potential difference higher than the threshold voltage (35 V). As regard the writing speed, QR-LPD achieves fast response time as 0.2 msec that makes it a fast display despite the PM

addressing [55]. AM display addressing is however needed in order to improve

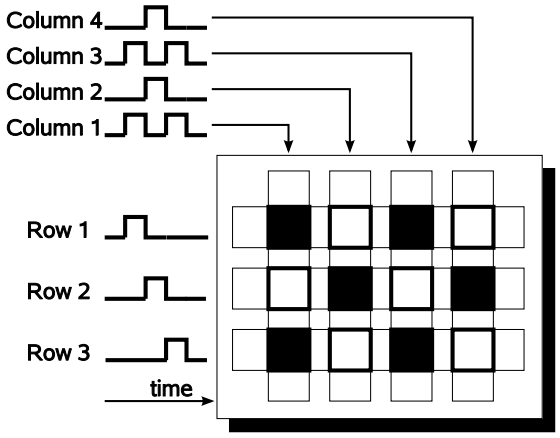


Figure 4.2: Basic driving matrix of PM-QRLPD.

the display from black/white to gray scale (where more threshold voltages are required, increasing the risk of crosstalk) or to increase the writing speed. In AM display, each single pixel is switched by a transistor, as shown in Fig. 4.3. AM addressing is not affected by crosstalk. To write a given line on the screen, the appropriate gate line (scan line) is selected so that the transistors on the selected row enable the voltage to be transferred from the data line (signal line) to the pixels, while the other gate lines remain inactive and the corresponding data pixels are not activated. The addition of a storage capacitor to each pixels makes the AM display more robust and less prone to noise. AM addressing also permits an higher frame rate than PM addressing, since an image can be written to the scan line in less than 0.2 msec required for PM addressing. However, AM-QRLPD can only be implemented with a technology that operates at a supply voltage of 70 V, is faster than the QR-LPD response time (0.2 msec) and is fabricated at low process temperature.

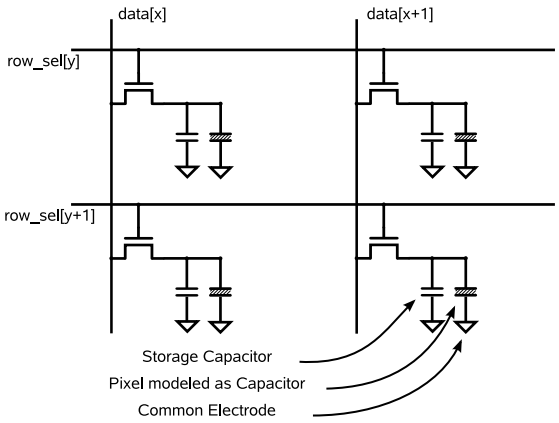


Figure 4.3: Schematic of active-matrix display

4.2 Frontplane display

The first step is to give an overview of the QR-LPD technology developed by the Bridgestone Corporation.

4.2.1 Liquid Powder

A key component of QR-LPD technology is the new material developed by Bridgestone, which behaves like a liquid despite its powder form. Two types of powders have been developed: a white powder with a negative charge and a black powder with a positive charge. A mixture of the two powders has a gray color. The individual particles in the powder do not require external friction for charging, as the charge is intrinsic to the particles them-selves. As illustrated in Fig. 4.4, when no electric field exists between the electrodes, negatively and positively charged particles are attracted to each other by a force F_a consisting of the Coulomb force and the Van der Waals force. When an electric field, E, is applied to the electrodes, the forces generated by the field are opposed to the to the force of attraction F_a, and if the field is strong enough the pair of charged particles will separate so that the positively charged particle travels towards the negative electrode and vice versa. At the surface of the electrode, the particle is subject to an attractive force similar to that between charged particles in the absence of a field, but also to an additional (repulsive) force due to the image charge caused by the polarization of the electrode by the charged particle. These attractive and repulsive forces between the particles

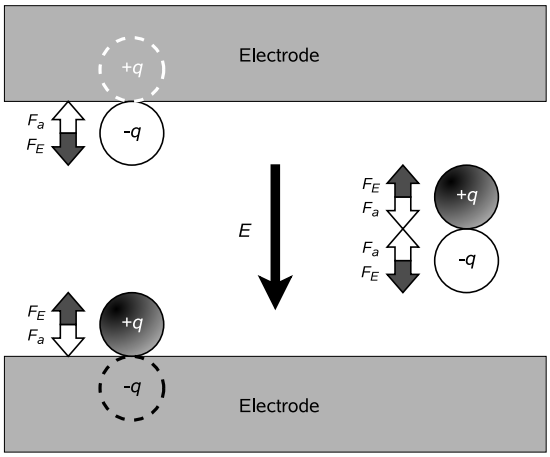


Figure 4.4: The force acting on the particles of the liquid-powder.

and electrodes make the QR-LPD bistable, so that an image can be retained on the display even when the power is switched off [54].

The reported particle transfer speed from one electrode to the opposite one is greater than 11.11 m/sec (40 km/hour) [54], resulting in fast pixel response of no more than 0.2 msec for both white-to-black and black-to-white pixel transitions, as shown in Fig. 4.5. The bistable nature of the liquid-powder particles is reflected in the hysteresis plot of Fig. 4.6. Depending on the current state of the particles, the applied voltage can switch them to a new state. However, a relative high voltage of 70 V is required for driving the QR-LPD, and the threshold voltage needed to overcome the force of attraction between the oppositely charged particle is about 35 V. The range of voltages between 35 V and 70 V can be used to set various gray-scale levels.

4.2.2 Quick-Response Liquid-Powder Display structure

The structure of the QR-LPD is shown in Fig. 4.7. The two types of powder materials (negatively charged white powder and positively charged black powder) are packed into an area between two patterned substrates. Ribs between individual cells prevent the powder from shifting, thus ensuring that the uniform distribution of the powders is maintained. The rest of the space is filled with air. When a negative voltage is applied to the upper transparent conductive oxide (TCO) electrode, the positively charged black powder moves

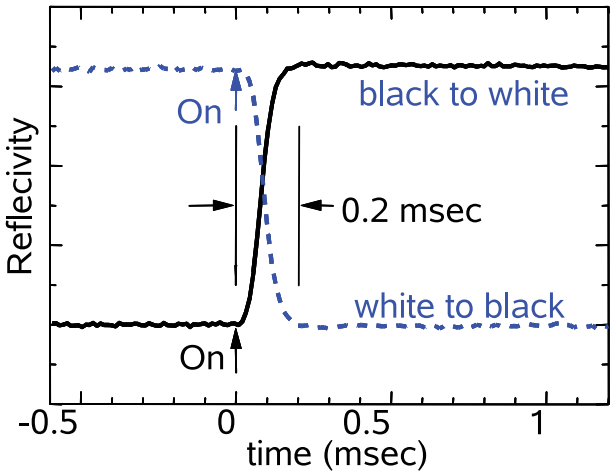


Figure 4.5: Pixel response times of white and black liquid-powders.

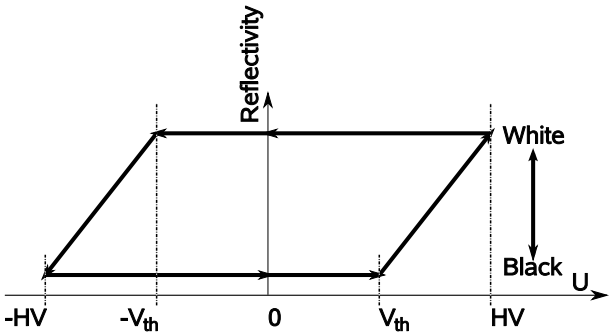


Figure 4.6: Hysteresis plot of reflectivity versus applied voltage. (HV stands for high voltage and V_{th} for the threshold voltage).

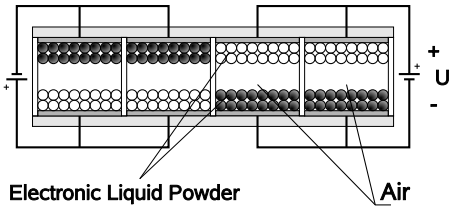


Figure 4.7: Four pixel cells of the QR-LPD display.

to the upper electrode, making it look black. The reverse bias causes the negatively charged white powder to be attracted to the upper, making it look white. The above-mentioned bistability means that the image on the display panel is retained without power, for up to several years. This feature dramatically decreases the power consumption of the display. Instead of needing +/- 70 V sources to change the polarity of a single QR-LPD cell, both the top electrode (named the common electrode) and the bottom one operate in the range from 0 to 70 V. Hence no negative voltage is required and the maximum voltage difference between the source and drain of the transistor during cell switching is 70 V instead of 140 V.

4.3 Backplane display

This section starts with a discussion of the organization of AM-QRLPD E-Paper based on HV-SGTFTs. This is followed by an explanation of the design of the backplane display. Section 4.4 goes into greater detail about the fabrication and experimental results of the HV-SGTFT technology used as a basis for the AM-QRLPD.

4.3.1 E-Paper design

An E-Paper can be organized as shown in the block diagram of Fig. 4.8. The AM backplane used to drive the QR-LPD frontplane consists of a matrix of HV-SGTFTs connected as shown in Fig. 4.9(a), with horizontal and vertical lines (wires) for the scan lines (rows) and data lines (columns) respectively. A gate driver and a data driver are appropriately connected to control the rows and columns respectively. Both drivers operate at low voltage. A high-voltage level shifter is inserted between the low-voltage gate driver and the the display rows, which operate at high voltage, while a DAC (digital-to-analog converter) forms the interface between the low-voltage data driver and the display columns (data lines). Fig. 4.8 also shows a timing control unit, which uses the horizontal and vertical synchronization control signals to regulate the timing of the gate driver and the data driver. All these blocks form the electronics required to drive the QR-LPD E-Paper. Others circuits such as μ-processors and more general logics could also be included to give a smart flexible E-Paper device.

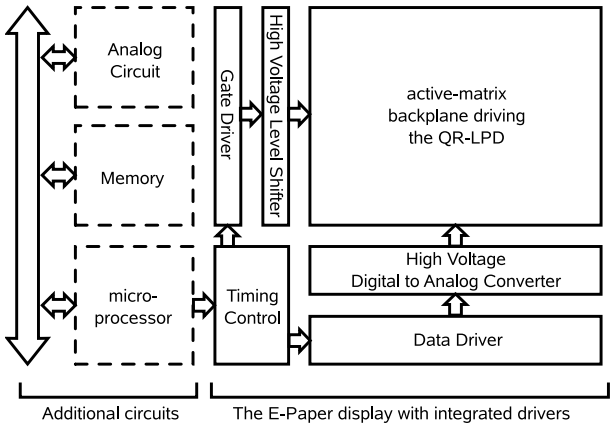
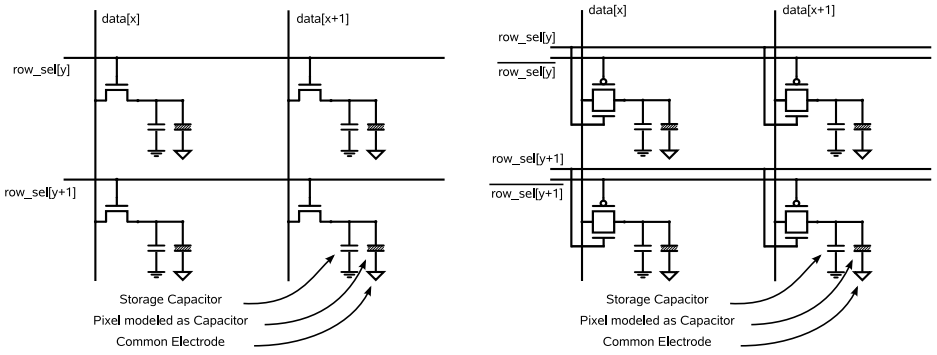


Figure 4.8: Block diagram of the E-Paper display with integrated drivers and additional circuits.

4.3.2 Pixel design

Fig. 4.9(a) shows the equivalent circuit of the pixels in which an n-channel TFT is connected by its gate to the scan (row) line and by its drain to the data (signal) line. The TFT switches each QR-LPD pixel (modeled in Fig. 4.9(a) as a capacitor) on and off. A storage capacitor is also connected in parallel with each QR-LPD pixel to improve the latter's stability. When the TFT is turned on by a positive voltage pulse applied to the gate electrode, the data voltage (voltage applied to the source electrode) can be transmitted to the drain, which is connected to the QR-LPD and the storage capacitor. At high data voltages, the pixel voltage (display electrode voltage) rises with the gate pulse up to a maximum that ideally equals the source electrode voltage. This voltage will then be maintained in the pixel throughout the frame time, until another gate voltage pulse changes the state of the pixel. The data voltage to be applied is 70 V or 0 V, while the common electrode should be 0 V or 70 V respectively, in order to obtain the required + or - 70 V pixel potential difference. In the n-channel TFT pixel configuration, however, the gate voltage must be higher than 70 V to keep the gate voltage above the threshold voltage and allow the pixel to reach the required 70 V. Otherwise the TFT will switch off and stop the pixel charging. This gate voltage restriction can be avoided by using the CMOS configuration shown in Fig. 4.9(b), where the p-channel TFT pulls the pixel voltage up to 70 V when its gate voltage is zero and the n-channel TFT pushes the pixel voltage down to 0 V when its gate voltage is 70 V.



(a) (b)

Figure 4.9: Schematic of AM display with n-channel (a) and CMOS (b) HV-SGTFTs.

4.4 High voltage SG-TFTs

Some key issues concerning the design and fabrication of SG-TFTs fabricated by the μ-Czochralski process and operating at high voltages such as 70 V are addressed in the present section. The above-mentioned kink effect (see sections 3.2.2 and 3.3) can be a serious problem for SOI and TFT technologies at high voltages. Transistors with a thick silicon layer have such layer partially depleted of carrier during operation. When the drain voltage is high enough, the channel electrons can acquire sufficient energy in the high electric field zone near the drain to create electron-hole pairs by impact ionization. The electrons generated move rapidly to the channel and the drain, while the holes migrate towards the region of lowest potential, which is known as the "floating body". The injection of holes into the floating body increases the body potential, leading to a drop in the threshold voltage. This threshold voltage shift due to the body effect induces an increase in the drain current [57]. If the silicon layer in a SOI or TFT is thin, the channel will be fully depleted of carrier and there will be no kink effect due to the influence of the floating body, since there is no neutral region in the channel in this case. However, the effect of drain current enhancement is still observed, but this is due to the parasitic BJT effect (often also known, confusingly enough, as the kink effect). In fact, it is found that the body-source V_{BE} junction is forward biased and increases hugely as the drain voltage increases, even more so than in the thicker device. This can be explained by the fact that the higher drain field in the thinner device causes more impact ionization current, which must be equalized by higher recombination rates that vary as $exp(V_{BE}/nV_T)$, where

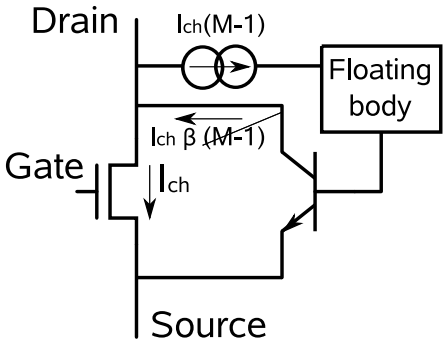


Figure 4.10: Schematic of parasitic bipolar junction transistor (BJT) in SOI MOSFET or SG-TFT. I_{ch} is the channel current, β the BJT gain and M the impact ionization factor. In the case of an n-channel device, $I_{ch}\beta(M-1)$ is the electron current amplified by the parasitic BJT and collected by the drain (collector), giving rise to positive feedback if $\beta(M-1) > 1$.

V_T is the thermal voltage. Furthermore, the recombination is restricted to thinner regions (smaller volumes), which means that an even higher V_{BE} is needed. However, the threshold voltage of the fully depleted device is not sensitive to the body bias V_{BE}, whereas that of the partially depleted device is. In partially depleted devices, V_{BE} effectively reduces the front-surface band bending required for strong inversion (inverse body effect). This reduces the threshold voltage by diminishing the depletion charge that must be supported by the gate. However, in the fully depleted device, the depletion (body) charge is fixed, and hence the threshold voltage is independent of V_{BE}. Since the V_{BE} induced in a fully depleted device is substantial, and even higher than that in thicker device, a significant BJT effect is found. Electrons are injected into the body (base) from the source (emitter) and are collected by the drain (collector). This extra drain current boosts the impact ionization, giving rise to positive feedback (Fig. 4.10). The result is latchup (loss of gate control) or even premature breakdown [58]. In general, p-channel devices show much less kink effect and higher breakdown voltages than n-channel device because of lower impact ionization factor. An HV-SGTFT with an undoped channel layer 250 nm thick will be nearly or fully depleted in operation. This is confirmed by the simulation result of Fig. 4.11 which shows that the hole concentrations in the channel for different gate voltages are clearly lower than the doping concentration. The fully depletion of the channel is also confirmed by the absence of the body effect as mentioned in the section 3.2.1. When fully depleted

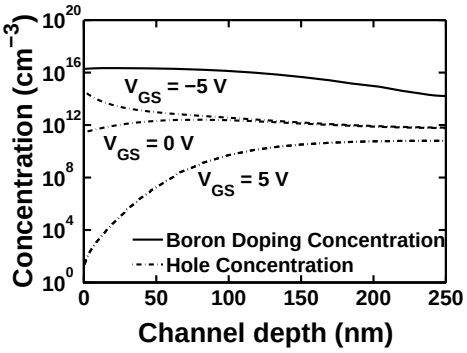


Figure 4.11: TCAD Simulation of the hole concentration and boron doping concentration obtained with a dose implantation of 2.5x10^{11} of an n-channel SG-TFT.

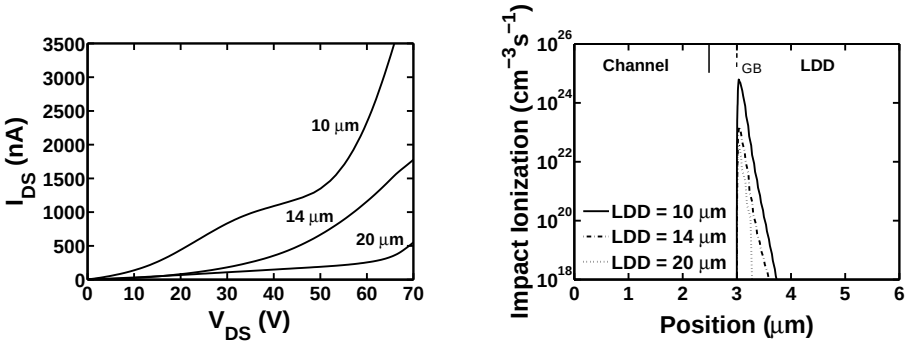
a HV-SGTFT is subject to the kink effect, which can lead to degradation of device characteristics in both analog and digital circuit applications and also to problems during transient operation such as transient leakage currents in the transmission gate, with possible consequences for the pixel display for example [57]. Furthermore, the kink effect and possible breakdowns become more serious when the channel length is short. In this context, the required channel width and length of the HV-SGTFT are related to the single grain size, since the channel must be fabricated inside the location-controlled grain in order to avoid random grain boundaries that reduce the carrier mobility and increase the leakage current. In the process batch investigated in the present study, the maximum grain size is designed-limited to 6x6 μm^2, and as a consequence 5 μm is the maximum channel length. The effective channel width can be increased by connecting several devices with 5 μm channel width in parallel. During transient operation, HV-SGTFT are liable to the kink effect. When the pixel electrode (drain) is at 0 V, the data line (source) at 70 V, and the scan line (gate) at 0 V, the HV-SGTFT will be biased at strong saturation ($V_{SD} \gg V_{GS}$ - V_{th}) with consequential kink effect, which is fatal for the device. A similar effect is found when the pixel electrode is at 70 V, the data line at 0 V, and scan line at 0 V ($V_{DS} \gg V_{GS}$ - V_{th}). To avoid such problems the HV-SGTFT must be provided with source and drain regions with a low doping level and low energy implantation (for the sake of convenience, we will refer to both of these regions from now on by the acronym LDD, which stands for “lightly doped drain”) to reduce the high electric field in the channel region which can lead to impact ionization and hence perfor-

mance degradation or even breakdown. The LDD regions do however have the drawback of a high series resistance. Since n-channel HV-SGTFT is more liable to impact ionization and possible breakdown than p-channel devices, TCAD simulations of n-channel HV-SGTFT with 5 μm channel width and length had to be performed to determine the minimum length of the LDD region needed to prevent breakdown effect. As will be seen from Fig. 4.12(a), an LDD length of 10 μm gives a severe kink effect that could lead to performance degradation when the drain voltage approaches 70 V. LDD lengths of 14 μm and in particular of 20 μm, on the other hand, give substantially lower kink effect to preserve from performance degradation. Inspection of the simulation results of Fig. 4.12(b) indicates that the improved reliability at LDD lengths substantially above 10 μm are due to the lower impact ionization produced under these circumstances. It may be seen that the impact ionization occurs at a position corresponding to that of the random GBs located inside the LDD region, and the simulated peak values are 6x10^{24} cm$^{-3}s^{-1}$, 1x10^{23} cm$^{-3}s^{-1}$, and 3x10^{22} cm$^{-3}s^{-1}$, while the mean values calculated along the LDD region are 2.6x10^{24} cm$^{-3}s^{-1}$, 8.9x10^{23} cm$^{-3}s^{-1}$, and 2.8x10^{23} cm$^{-3}s^{-1}$ for HV-SGTFTs with LDD length 10, 14, and 20 μm respectively. The simulated impact ionization values are from 3 to 5 orders of magnitude lower than those simulated in SG-TFTs with 2 μm channel length and width and 7 V drain voltage bias stress, which causes performance degradation as has been shown in section 3.3. The n- and p-channel HV-SGTFTs intended for use in the proposed QR-LPD system were therefore designed and fabricated with LDD lengths of 14, 20 and 26 μm.

4.4.1 Process flow for trial HV-SGTFTs

The fabrication process of the backplane CMOS HV-SGTFTs designed to meet the requirements outlined in the previous section consists of the following steps.

- creation of grain filters
- deposition of a-Si by LPCVD
- 2.5x10^{11} cm^{-2} boron channel implantation
- crystallization of a-Si by μ-Czochralski process
- island patterning
- deposition of 200 nm TEOS gate oxide



(a) (b)

Figure 4.12: (a) TCAD simulations of output characteristics of n-channel HV-SGTFTs with 5 μm channel width and length, and LDD lengths of 10, 14, and 20 μm, at a gate voltage of 70 V. (b) Simulations of impact ionization cross-sectional profile parallel to the channel of HV-SGTFTs with 5 μm channel width and length, and LDD length of 10, 14, and 20 μm. The origin of the X axis corresponds to the middle of the channel area. The channel-LDD junction is at 2.5 μm and the random GBs at 3 μm, for the case of 6 μm silicon grain length.

- Al sputtering for gate metal
- gate patterning
- dip etching with BHF 1:7 for 15 sec and 10 min rinsing
- p^- mask and LDD implantation with B^+ doping of 1x10^{12} cm^{-2} and energy 5 KeV (see Fig. 4.13(a))
- n^- mask and LDD implantation with As^+ doping of 1x10^{12} cm^{-2} and energy 5 KeV (see Fig. 4.13(a))
- excimer laser annealing at different energies
- TEOS passivation
- contact hole formation
- p^+ mask and HDD implantation with B^+ doping of 5x10^{15} cm^{-2} and energy 20 KeV (see Fig. 4.13(b))
- n^+ mask and HDD implantation with P^+ doping of 5x10^{15} cm^{-2} and energy 30 KeV (see Fig. 4.13(b))

- laser annealing at 300 mJ/cm^2
- Al sputtering for 1^{st} metal layer and patterning (see Fig. 4.13(c))
- TEOS passivation
- via formation
- Al sputtering for 2^{nd} metal layer and patterning of pads and pixel electrodes
- Alloying to 400 °C with fuming gas

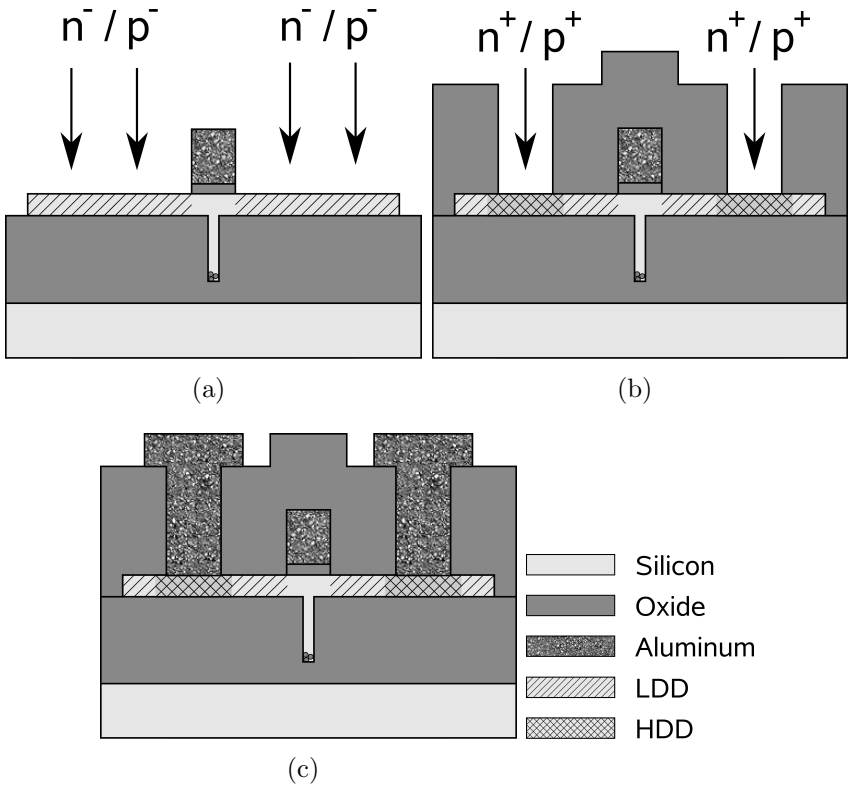


Figure 4.13: Successive stages in production of HV-SGTFTs for QR-LPD E-Paper compatible with LV-SGTFT integrated drivers. (a) LDD implantation, (b) contact hole formation and HDD implantation, (c) deposition of 1^{st} metal layer and patterning.

One advantage of this process is that the same mask can be used for the implantation of both LDD regions and the source and drain regions with a

high doping level (referred to from now on for the sake of convenience by the acronym HDD, which stands for "heavily doped drain"). HDD implantation occurs through the contact hole, using the oxide passivation as mask. The LDD length is defined here by the distance from the contact hole to the gate. The disadvantage of this arrangement is that the minimum distance between contact hole and gate length is defined by the design rule 0.6 μm. This can be a problem when it comes to the fabrication of LV-SGTFT technology, where LDD lengths less than 0.6 μm even down to zero in some cases may be desired. Fig. 4.14 shows the schematic cross-section of a HV-SGTFT fabricated by the above process, connected to a QR-LPD pixel and storage capacitance.

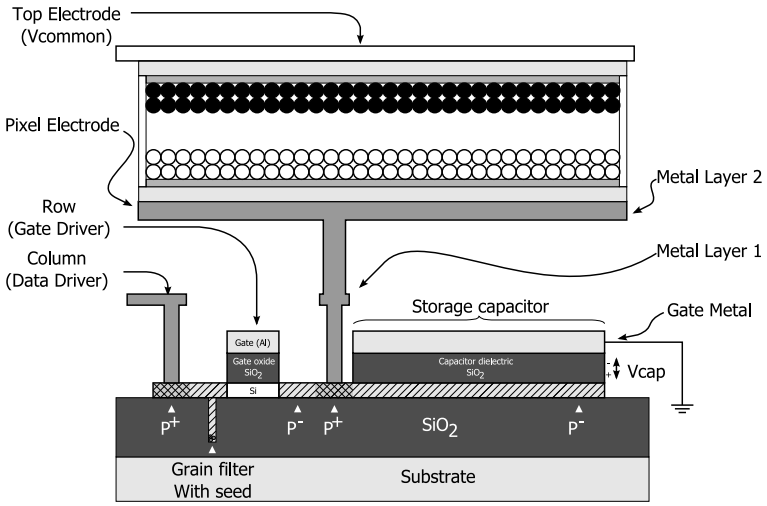


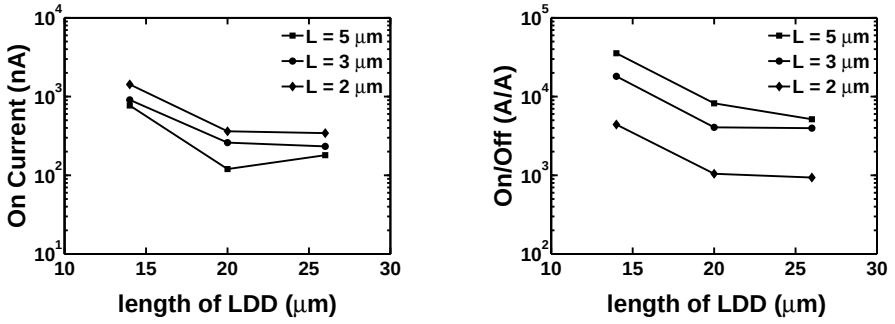
Figure 4.14: Schematic of pixel design with HV-SGTFT and QR-LPD.

4.4.2 Test results and discussion

The results of a series of tests performed on HV-SGTFTs fabricated as described in section 4.4.1 will now be presented and discussed. A distinction is made here between the results for p-channel and n-channel devices.

p-channel HV-SGTFT. Fig. 4.15(a) shows the mean measured value of the on current for V_{GS} = -70 V and V_{DS} = -70 V as a function of the LDD length for various channel lengths, while Fig. 4.15(b) shows the mean ratio of the on current to the leakage current measured at V_{GS} = 50 V and V_{DS} = -70 V, also as a function of the LDD length for various channel lengths. It will be seen that the on current increases with falling LDD length as does the on/off

ratio since the leakage current remains largely constant. On the other hand, the on/off ratio falls and the on current rises as the channel length decreases down to 2 μm, because of the higher leakage current due to a more pronounced short-channel effect and kink effect as shown in Fig. 4.16(a). The yield of p-channel HV-SGTFTs (which do not present any irregular characteristics such as abnormally high kink effect, high leakage current, low on current or low on/off current ratio) is extremely high as shown in Fig. 4.16(b). This confirms the reliability of p-channel HV-SGTFTs at supply voltage of 70 V. Fig. 4.17(a) shows the output characteristics of p-channel HV-SGTFT with

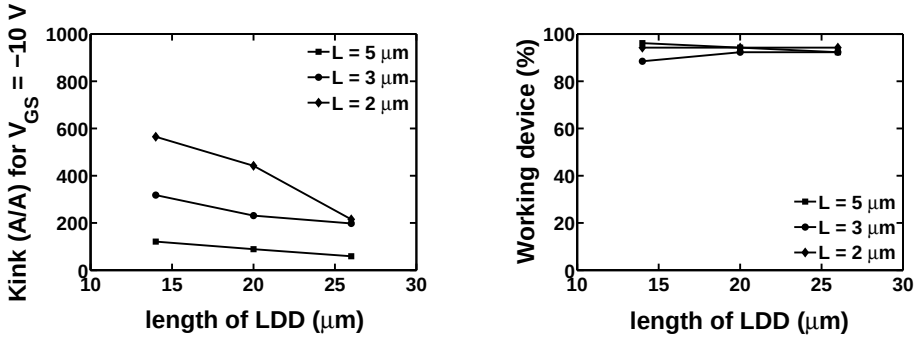


(a) (b)

Figure 4.15: (a) Mean measured drain current of p-channel HV-SGTFT for V_{GS} = -70 V and V_{DS} = -70 V (on current) as a function of the LDD length for various channel lengths L. (b) Mean ratio of on current to leakage current for V_{GS} = 50 V and V_{DS} = -70 V (off current), also as a function of the LDD length for various channel lengths L.

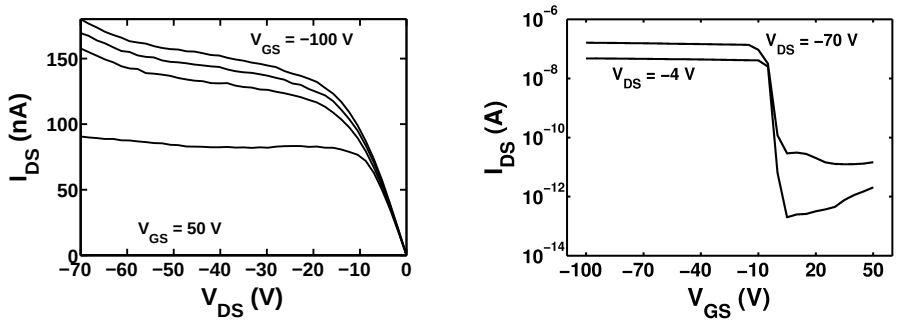
5 μm channel length and width and 26 μm LDD length, with various gate voltages from 50 V to -100 V. It will be seen that the output characteristics are not subject to a kink effect. As a result, the on/off current ratio is high (10^5), even for drain voltage of -70 V where a strong kink effect may induce high leakage current. Fig. 4.17(b) shows the transfer characteristics of the same device with drain voltages of -4 V and -70 V. This figure shows that the threshold voltage is around -10 V.

Fig. 4.18(a) shows the output characteristics of a p-channel HV-SGTFT with 5 μm channel length and width and a shorter LDD (length 14 μm), to which gate voltages ranging from 50 V to -100 V are applied. It will be seen that there is a slight kink effect at high drain voltages, which is however self-limiting. That may be due to the non-regenerative pnp parasitic transistor latchup, since the gain of the positive feedback loop is most probably less than



(a) (b)

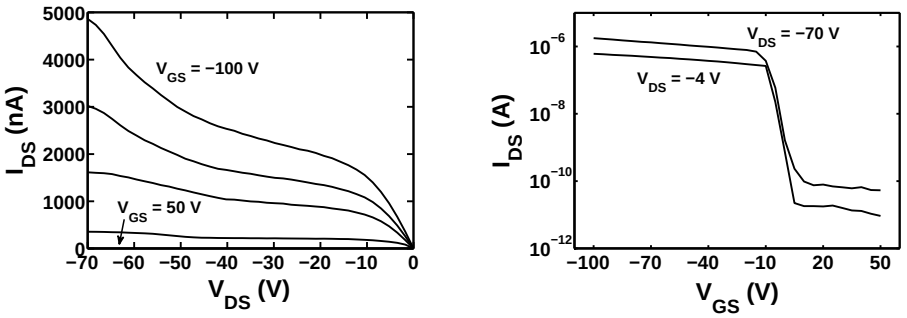
Figure 4.16: (a) Mean measured kink effect of p-channel HV-SGTFT evaluated as a ratio of on current to the drain current at V_{DS} = -35 V. (b) Yield of p-channel HV-SGTFT. Both curves are plotted as functions of the LDD length for various channel lengths L.



(a) (b)

Figure 4.17: Output characteristics for various gate voltages (a) and transfer characteristics for two drain voltages (b) of a p-channel HV-SGTFT with 5 μm channel width and length, and LDD length 26 μm.

one. Fig. 4.18(b) shows the transfer characteristics of the same device with drain voltages of -4 V and -70 V.

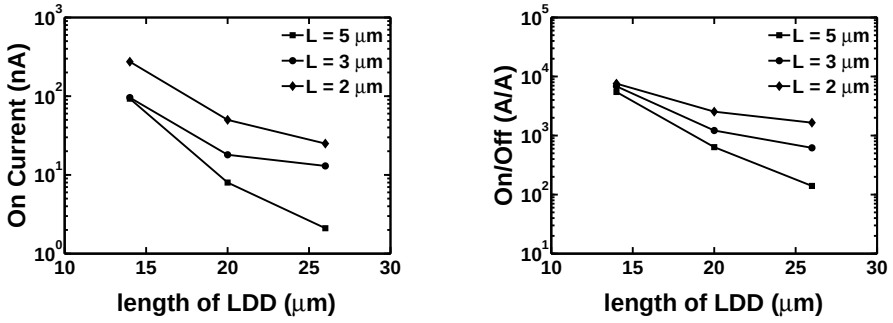


(a) (b)

Figure 4.18: Output characteristics for various gate voltages (a) and transfer characteristics for two drain voltages (b) of a p-channel HV-SGTFT with 5 μm channel width and length, and LDD length 14 μm.

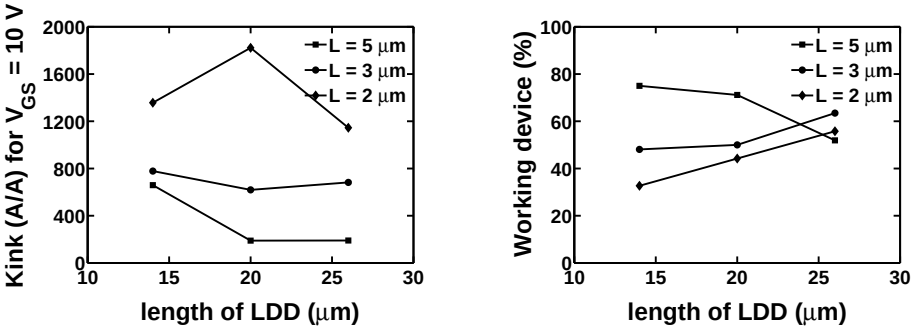
n-channel HV-SGTFT. Since the kink effect is a more serious issue in n-channel HV-SGTFTs than in p-channel device, arsenic LDD implantation was used to obtain shallower source and drain junctions than is possible with phosphorous doping. As a consequence, the n-channel devices have a higher series resistance than p-channel ones for the same doping level and energy. In line with this, as may be seen from Fig. 4.19(a) and 4.19(b), n-channel HV-SGTFTs have a lower on current and hence a lower on/off drain current ratio than p-channel devices. Furthermore, as shown in Fig. 4.20(a), the kink effect measured in n-channel devices is more pronounced than that in p-channel devices. Unlike the case with p-channel devices, the on/off current ratio of n-channel devices increases as the gate length falls. This is because no leakage current is induced by the kink effect in n-channel devices when the gate voltage is lower than -10 V, though the kink effect becomes substantial at higher gate voltages. However, the yield of n-channel HV-SGTFTs is lower than that of p-channel devices and decreases with the gate length (see Fig. 4.20(b)), possibly due to effects related to the shallow implantation depth of arsenic LDD region in the poly-Si layer.

Fig. 4.21(a) shows the output characteristics of an n-channel HV-SGTFT with 5 μm channel length and width and 20 μm LDD length with gate voltages ranging from -50 V to 100 V. It may be noted that the kink effect (which would be seen as an exponential rise in current) is completely absent here.



(a) (b)

Figure 4.19: (a) Mean measured drain current of n-channel HV-SGTFT for V_{GS} = 70 V and V_{DS} = 70 V (on current) as a function of the LDD length for various channel lengths L. (b) Mean ratio of on current to leakage current for V_{GS} = -50 V and V_{DS} = 70 V, also as a function of the LDD length for various channel lengths L.

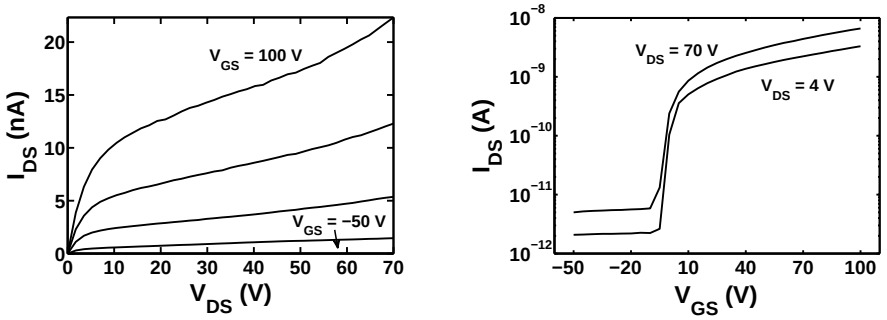


(a) (b)

Figure 4.20: (a) Mean measured kink effect of n-channel HV-SGTFT evaluated as a ratio of on current to the drain current at V_{DS} = 35 V. (b) Yield of n-channel HV-SGTFT. Both curves are plotted as functions of the LDD length for various channel lengths L.

Fig. 4.21(b) shows the transfer characteristics of this device for drain voltages of 4 V and 70 V.

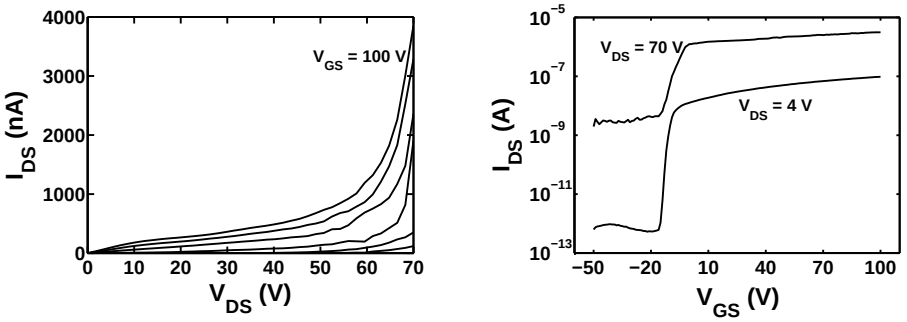
By way of contrast, Fig. 4.22(a) shows the output characteristics of an n-channel HV-SGTFT with 5 μm channel length and width and a shorter LDD region (length 14 μm) with gate voltages ranging from -50 V to 100 V. It will



(a) (b)

Figure 4.21: Output characteristics (a) and transfer characteristics (b) of an n-channel HV-SGTFT with 5 μm channel width and length, and 20 μm LDD length.

be seen that there is a strong kink effect visible as an exponential increase in drain current. Fig. 4.22(b) shows the transfer characteristics of the same device for drain voltages of 4 V and 70 V.



(a) (b)

Figure 4.22: Output characteristics (a) and transfer characteristics (b) of an n-channel HV-SGTFT with 5 μm channel width and length, and 14 μm LDD length.

It may thus be concluded that a gate length of 5 μm and LDD length of 15 - 20 μm appear to be give the most reliable n- and p-channel HV-SGTFTs working at 70 V, in terms of the highest on/off current ratio and yield. The low avalanche effect of p-channel HV-SGTFTs makes it possible to relax the requirements on the LDD region, thus permitting boron implantation

(instead of BF_2 that would give a shallower junction) that is deeper than arsenic implantation for the same doping level and energy. Thanks to this measure, the p-channel HV-SGTFTs used in this study have a lower source and drain series resistances and hence higher current densities than the n-channel ones. Furthermore, the on current can be increased by using a parallel configuration, but this has the drawback of giving higher leakage.

4.5 Transient measurements on HV-SGTFTs

The next step in the investigation was to estimate the transient response of CMOS transmission gates implemented with the aid of HV-SGTFTs. The transient measurements were performed using square wave input signals with a peak value of 70 V and an output probe with an impedance consisting of a capacitance C_L of about 200 pF in parallel with a resistance R_L of 10 MΩ (see Fig. 4.23). Fig. 4.24 shows the input (data) and output (QR-LPD electrode)

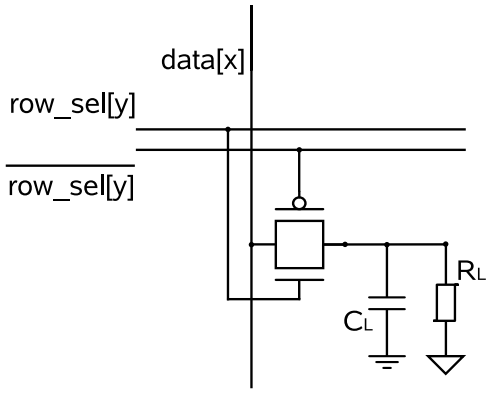


Figure 4.23: Test set-up for pixel with HV-SGTFT.

signals for an opened transmission gate (V_{Gp} = 0 V and V_{Gn} = 70 V) with various LDD lengths. The output reduction is due to the voltage drop over the resistive probe. This problem will not occur in the QR-LPD, since this represents a purely capacitive load. Fig. 4.25 shows the input and output signals for a closed transmission gate (V_{Gp} = 90 V and V_{Gn} = 0 V). The gate voltage must be made higher than 70 V here, to minimize the leakage current. Inspection of this figure shows that the longest LDD (26 μm) gives a high output voltage, because of the high leakage current. The minimum leakage current is obtained for a LDD length of 20 μm. Despite the high load impedance of the probe, the propagation delay of the pixel is acceptably low.

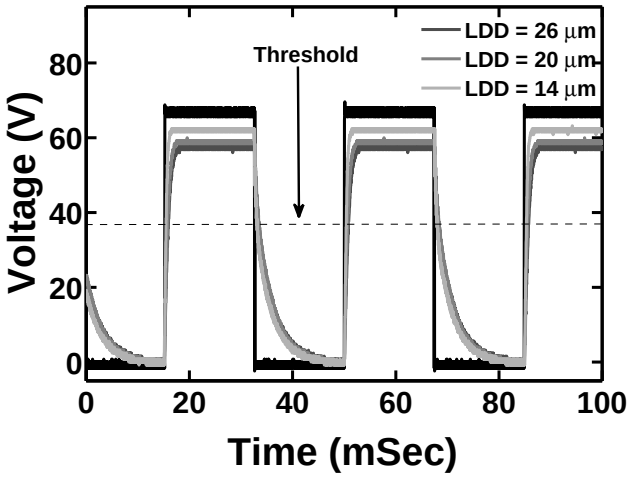


Figure 4.24: Square wave input (data) signal and output (pixel) signal of open ($V_{Gp} = 0$ V and $V_{Gn} = 70$ V) CMOS HV-SGTFT transmission gate for different LDD lengths.

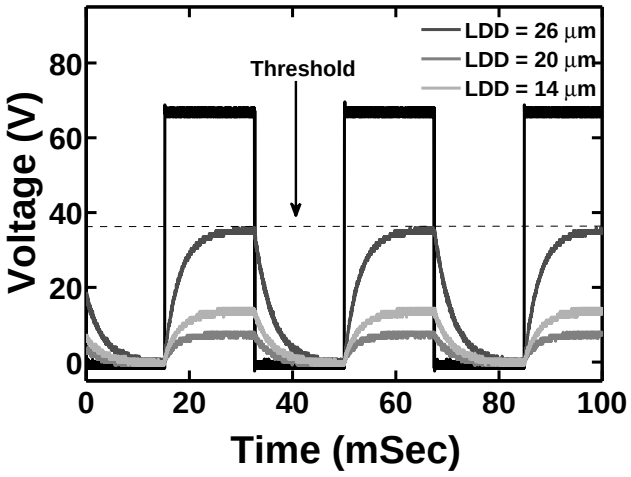


Figure 4.25: Square wave input (data) signal and output (pixel) signal of close ($V_{Gp} = 90$ V and $V_{Gn} = 0$ V) CMOS HV-SGTFT transmission gate for different LDD lengths.

The time taken to switch from the off state- to the on-state is no more than 0.7 msec for a LDD length of 14 μm, and about 1.5 msec for LDD lengths of 20 and 26 μm, as shown in Fig. 4.26. Switching from on to off takes longer, because of the lower speed of the n-channel HV-SGTFT compared with the p-channel device (4.27). With higher input frequencies, the output signal cannot make

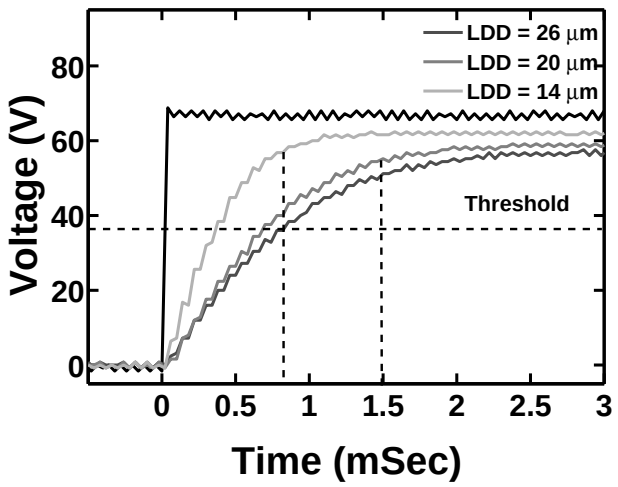


Figure 4.26: Propagation delay of CMOS HV-SGTFT transmission gate during on switching for different LDD lengths.

a full swing from high to low voltage when the transmission gate is open, as shown in Fig. 4.28. This issue can however be resolved by the new pixel design concept shown in section 4.6. A higher frequency is also beneficial for cutting down the leakage current when the transmission gate is closed, as shown in Fig. 4.29. The speed of the AM-QRLPD implemented with the aid of HV-SGTFTs can be predicted from the results of the measurements presented above. Firstly, the series resistance of the HV-SGTFT can be determined from the known input resistance of oscilloscope and the voltage drop over it formed at the steady-state condition. Secondly, the total load capacitance can be estimated by fitting the simulated results to measured propagation delay curve as shown in Fig. 4.30(a). It is predicted on this basis that the propagation delay can be reduced to as little as 100 nsec if the test probe is replaced by a QR-LPD pixel, which has a load capacitance of 10 fF as shown in Fig. 4.30(b).

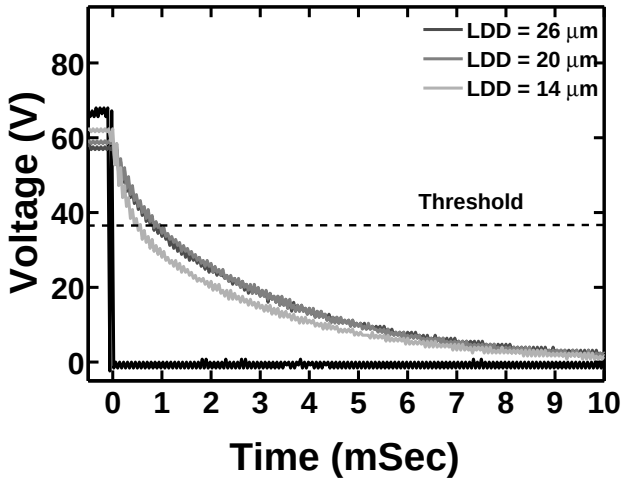


Figure 4.27: Propagation delay of CMOS HV-SGTFT transmission gate during off switching for different LDD lengths.

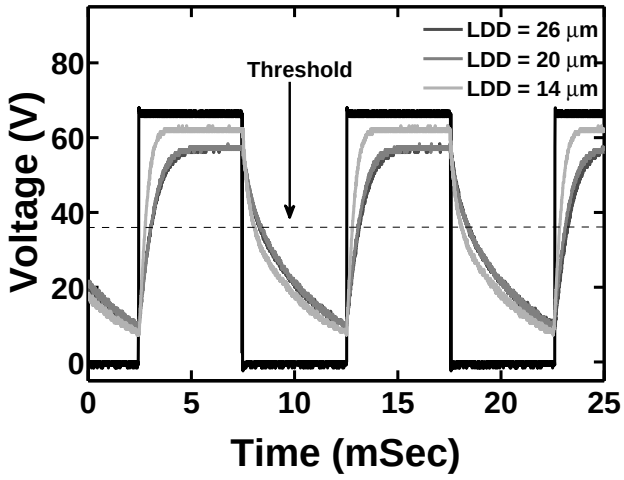


Figure 4.28: Square wave input (data) signal and output (pixel) signal of open (V_{Gp} = 0 V and V_{Gn} = 70 V) CMOS HV-SGTFT transmission gate for different LDD lengths operating at a higher frequency than that used for Figure 4.24 to 4.27.

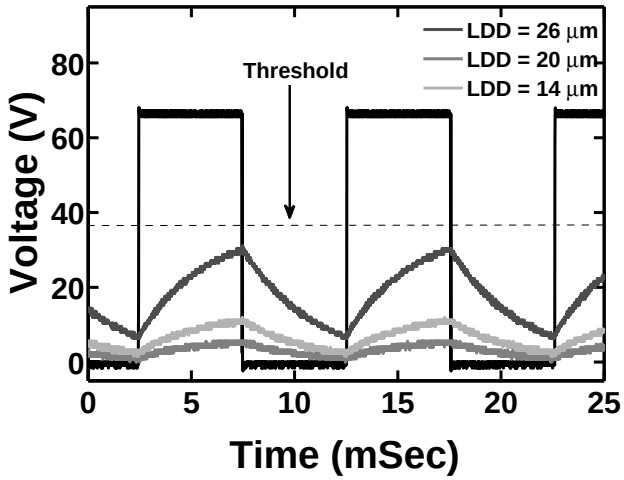
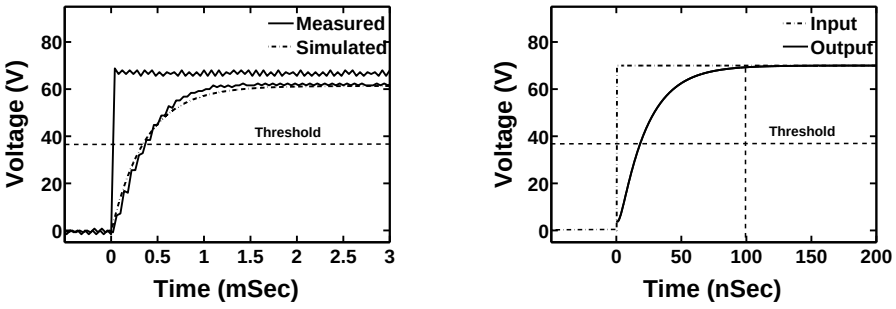


Figure 4.29: Square wave input (data) signal and output (pixel) signal of close ($V_{Gp} = 90$ V and $V_{Gn} = 0$ V) CMOS HV-SGTFT transmission gate for different LDD lengths operating at a higher frequency than that for Figure 4.24 to 4.27.



(a) (b)

Figure 4.30: (a) Fitting between measurement and SPICE simulation propagation delay for HV-SGTFT with 5 μm channel width and length. The SPICE simulation are performed by the modified BSIMSOI model and additional series resistances that describes the LDD regions. (b) Predicted propagation delay of QR-LPD driven by HV-SGTFT with 5 μm channel width and length.

4.6 A new look at the organization of the display

On the basis of the measurements and considerations gives above, a new improved design concept for AM-QRLPD E-Paper can now be proposed. The

main lines of this proposal are given in the present section. The schematic of an AM-QRLPD pixel is shown in Fig. 4.31. Writing is executed by activating a scan line (designated row-sel) via the level shifter of Fig. 4.32(a), and the data voltage is transferred through the p-channel HV-SGTFT to the QR-LPD and storage capacitor via the D/A converter shown in Fig. 4.32(b). The D/A converter is designed so that the data voltage can only range from 35 V to 70 V and voltages below the threshold voltage of 35 V are not used. The p-channel HV-SGTFT is adapted to transfer the maximum data voltage of 70 V to the pixel, because the p-channel HV-SGTFT remains on until the capacitive load is completely charged (The gate-source voltage is kept larger than the threshold voltage, i.e., $V_{GS} > V_{th}$). When the common electrode

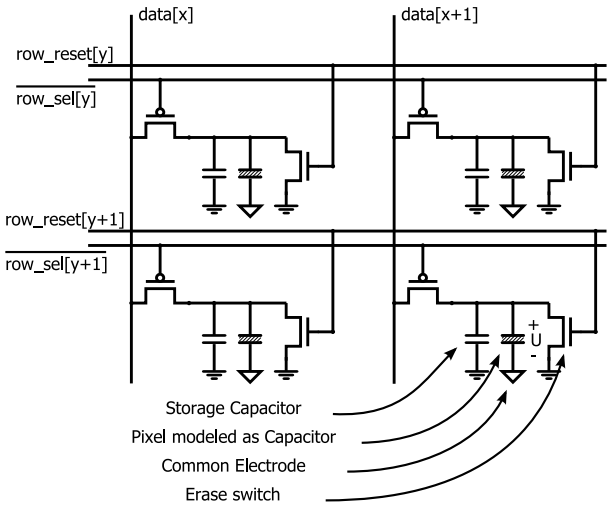
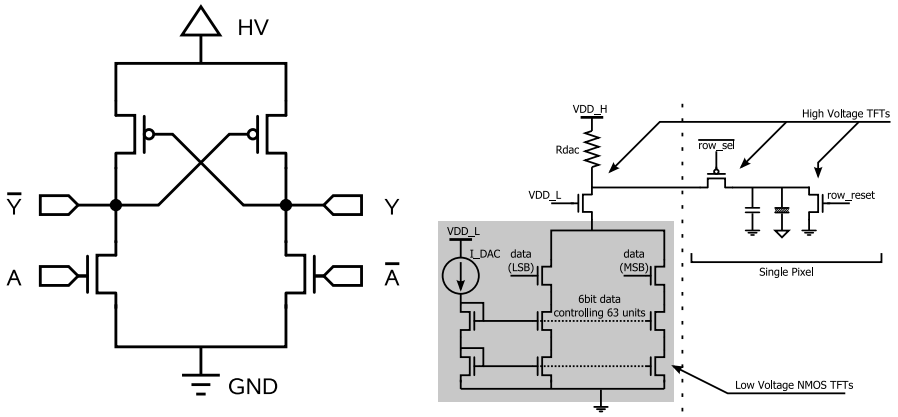


Figure 4.31: Schematic of AM-QRLPD pixel with p-channel HV-SGTFT for writing and n-channel HV-SGTFT for erasing.

is at 0 V, the potential difference between the two electrode can be between 35 V and 70 V. On the other hand, when the common electrode is at 70 V, the potential difference across the QR-LPD can range between -35 V and 0 V, which is below the threshold voltage. As a consequence, a pixel that has been made black cannot be erased (switched to white). The solution proposed for this problem is to use an n-channel HV-SGTFT connected as shown in Fig. 4.31, which erases the pixel and storage capacitor by pushing down to 0 V and thus providing the potential difference of -70 V required for switching to white. The storage capacitor makes the whole display more robust against noise and makes it possible to write faster than the pixel response time. In a PM display, writing each line must take at least 0.2 msec, which is the time required for the



(a) (b)

Figure 4.32: Schematic of level shifter used to select a row (a) and D/A converter used to feed a signal to the data line (b).

liquid-powder particles to settle (see Fig. 4.5). An AM display, on the other hand, it is possible to charge the storage capacitor quickly (in less than 0.2 msec), and continue with the following scan lines, while the storage capacitor ensures that the voltage over the pixel is held until the liquid-powder particles have settled (> 0.2 msec). The problem of slow switching from the on-state to the off-state can be definitively overcome with this new pixel design, since the QR-LPD is erased by n-channel HV-SGTFTs. Furthermore, the n-channel HV-SGTFT can be fabricated with an LDD drain and conventional HDD source, since high voltages can only occur in the drain region. A drawback of this construction is the additional load and the voltage partition caused by the n-channel HV-SGTFT.

4.7 Fabrication process for combined LV-SGTFT and HV-SGTFT technology

The AM-QRLPD E-Paper display system described in the previous section requires the combination of LV-SGTFTs and HV-SGTFT technologies. Once the grain filter has been created and the a-Si layer deposit as described in Chapter 1, the fabrication process continues as listed below:

- $2.5\text{x}10^{11}$ cm^{-2} boron channel implantation
- crystallization of a-Si by μ-Czochralski process

- island patterning (see Fig. 4.33(a))
- deposition of 200 nm TEOS as gate oxide for HV-SGTFTs (see Fig. 4.33(b))
- masking of HV-SGTFT technology area (see Fig. 4.33(c))
- dry etching of gate oxide down to 30 nm for LV-SGTFTs technology (see Fig. 4.33(d))
- Al sputtering
- gate masking combined with masking of HV-SGTFT technology area for gate patterning of LV-SGTFT technology (see Fig. 4.33(e))
- gate masking combined with inverted masking of HV-SGTFT technology area for gate pattering of HV-SGTFT technology (see Fig. 4.33(f))
- dip etching with BHF
- p- masking and LDD implantation with B^+ doping to 10^{12} cm^{-2} and energy 5 KeV (see Fig. 4.33(g))
- n- masking and LDD implantation with P^+ or As^+ doping to 10^{12} cm^{-2} and energy 5 KeV (see Fig. 4.33(g))
- p+ masking and HDD implantation with B^+ doping to $5x10^{15}$ cm^{-2} and energy 20 KeV (see Fig. 4.33(h))
- n+ masking and HDD implantation with P^+ doping to $5x10^{15}$ cm^{-2} and energy 30 KeV (see Fig. 4.33(h))
- excimer laser annealing with density energy of 300 mJ/cm^2
- TEOS passivation
- contact hole formation
- Al sputtering for 1^{st} metal layer and patterning
- TEOS passivation
- via formation
- Al sputtering for 2^{nd} metal layer and patterning of pads and pixel electrodes

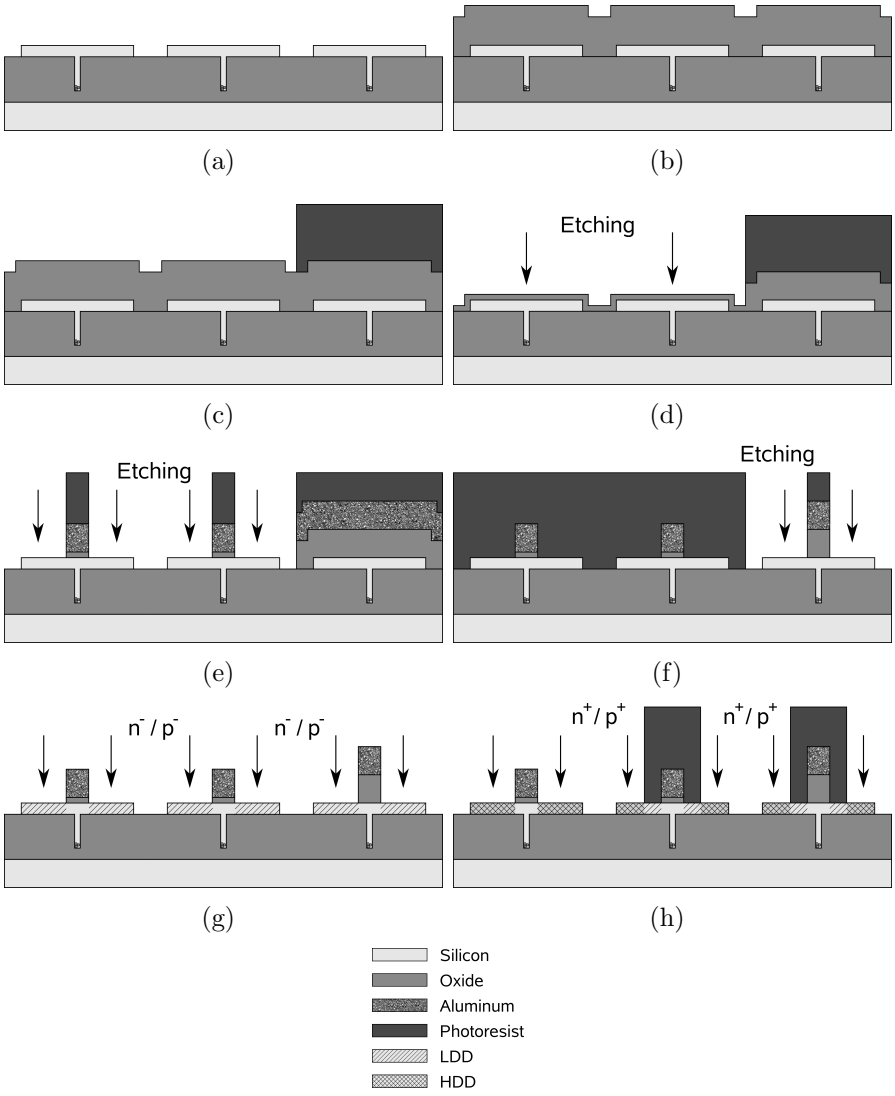


Figure 4.33: Successive steps in the fabrication of AM-QRLPD E-Paper pixels in which LV-SGTFT, LV-SGTFT with LDD, and HV-SGTFT technologies (shown in each picture from left to right, respectively) are integrated on a single chip. (a) island patterning, (b) deposition of gate oxide 200 nm thick for HV-SGTFT, (c) masking of HV-SGTFT technology area, (d) dry etching of gate oxide down to 30 nm thickness for LV-SGTFT, (e) gate masking combined with masking of HV-SGTFT technology area for gate patterning of LV-SGTFT, (f) gate masking combined with inverted masking of HV-SGTFT technology area for gate pattering of HV-SGTFT, (g) LDD implantation for n- and p-channel devices, and (h) HDD implantation for n- and p-channel devices. The remaining steps of the fabrication process are the same as in the conventional SG-TFT process.

- Alloying to 400 °C with fuming gas

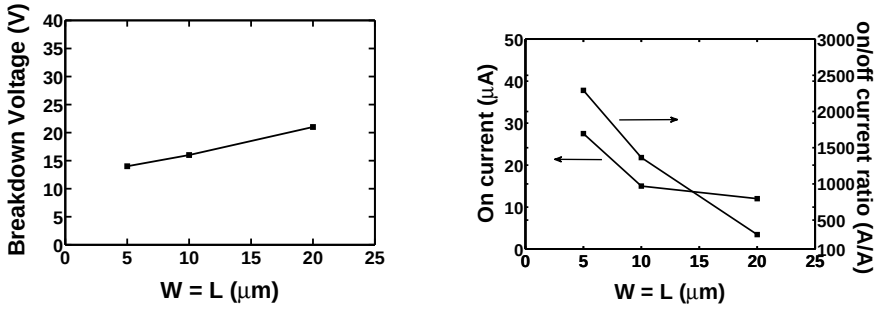
The disadvantage of this process compared with that described in section 4.4.1 is that two separated masks have to be made for LDD and HDD implantation, although the number of steps remains the same. The advantage is that there is no longer a lower limit on the length of the LDD region for the LV-SGTFT technology:any LDD length, down to zero, can be fabricated.

4.7.1 Polysilicon n-channel HV-TFT solution

Although the new design concept described above resolves many of the problems previously associated with n-channel HV-SGTFTs by using only one LDD region with a correspondingly lower series resistance, the reliability of the n-channel HV-SGTFT still needs to be improved by achieving a yield greater than the 80% obtained so far. This involves making the device with a channel longer than 5 μm, in order to relax the constraints on the drain LDD specifications. In such a way, the device with channel length longer than 6 μm (6x6 μm^2 is the size of a single grain) will have random grain boundaries in the channel (for the sake of convenience, we will refer to these devices from now on by "poly-Si TFTs"). Fig. 4.34(a) and 4.34(b) show that increasing the channel length in poly-Si TFTs without LDD region leads to a rise in breakdown voltage; but at the same time the on current falls because there are random grain boundaries in the channel, so the leakage current also rises. However, the LDD drain region needed to resist the supply voltage of 70 V could be much shorter than that required at a channel length of 5 μm. The solution would thus seem to be to choose a channel length greater than 5 μm and an LDD length less than 15 or 20 μm, the optimum combination being selected by trial and error so as to yield a higher on current than that obtained with 5 μm channel length and 15 or 20 μm LDD length. Furthermore, devices with a channel width of 5 μm could be connected in parallel to reduce the leakage current by avoiding the longitudinal random grain boundaries, which induce leakage current.

4.8 Conclusion

This chapter describes the design and the fabrication process of a prototype AM-QRLPD E-Paper system with reliable n- and p-channel HV-SGTFTs fabricated by the μ-Czochralski process so as to operate at a supply voltage of 70 V. A transmission gate developed with such n- and p-channel HV-SGTFTs has been found to have a measured propagation delay as low as 0.7 msec with



(a) (b)

Figure 4.34: Measured breakdown voltage (a); and on current and on/off current ratio (b) of poly-Si TFTs made without LDD region and with different channel widths W and channel lengths L. In all cases, W = L. The poly-Si channel layer is made by μ-Czochralski process with grain size of 6x6 μm^2.

about 200 pF load capacitance. On this basis, it is predicted that the propagation delay of the finished AM-QRLPD pixel could be no more than 100 ns. Finally, it has been shown that the HV-SGTFT developed as described above is fully compatible with the high-speed LV-SGTFT technology employed for driver circuits and more general logics.

Chapter 5

Location control of Ge grains for high mobility TFTs

The research presented in this chapter focuses on benchmarking single germanium (Ge) grains obtained by the μ-Czochralski process. Preliminary studies of Ge SG-TFT fabricated by the μ-Czochralski process are performed and a concept for the future technology required as a basis for functional n- and p-channel Ge SG-TFTs is proposed.

5.1 Introduction

The downscaling of complementary metal-oxide semiconductor (CMOS) transistors requires a new material with a higher carrier mobility to replace silicon for the channel. If this material could also be deposited in low-temperature process, then new applications such as ultra-wide-band wireless systems on a glass or flexible substrate could be devised [1]. Germanium is a promising candidate here, because of its high bulk mobility. In fact, p- and n-channel Ge MOSFETs have recently been fabricated, but their mobility was lower than expected [59]. This is mainly due to the high density of trap-states at the Ge-oxide interface. The requirement of a low-temperature production process is a further problem, adding to the existing technological challenges involved in the fabrication of Ge devices. A low-temperature process for the production of poly-Ge TFTs has been developed, but it still gives a low mobility and high leakage current [60, 61], because of the existence of random grain boundaries. The main objective for the developers of high-performance TFT electronics for large-area applications is thus to improve the quality of the low-temperature Ge layer. One promissing approach is to use the the μ-Czochralski process to

achieve 2D location control of the Ge grains, thus making it possible to fabricate single grain Ge TFTs, in a way similar to that described in section 1.2 for single grain Si TFTs [17]. Such devices with location-controlled Si grains fabricated by the μ-Czochralski process [12] have successfully achieved SOI-like performance thanks to the high quality of the silicon channel, even though the latter contains coincidence cite lattice grain boundaries (CSL-GBs) which do not affect carrier mobility [20]. As part of the present study, experience gained in the production of Si SG-TFTs was used as the basis for the fabrication of Ge grains with 2D location control at different process temperatures, excimer laser pulse widths, and with different grain filter stacks configurations. The Ge grains fabricated in this way were subjected to a series of tests. Electrical characterization shows that the μ-Czochralski process is a promising technique for the production of high-performance single Ge grain TFTs in a low-temperature process.

5.2 Germanium: electrical properties, problems, and objectives

There has been considerable interest in germanium of recent years as a material that can be used in high-performance applications; it is currently considered to be a potential replacement for silicon in many cases. The main advantage of Ge over Si is its superior electron and hole mobility, which make it possible to boost the drive current of transistors made with this material. The lower band-gap of Ge compared with that of Si should also permit further supply voltage scaling (see table 5.1). Finally, the lower temperature regime needed for dopant activation of a Ge-based MOSFET (around 500-600 °C compared with 1000-1100 °C for Si) also makes this material particularly interesting for use in high-k/metal gate technologies. Historical, the first (bipolar) transistors and integrated circuit were actually built using Ge substrates. However, Si rapidly supplanted Ge quickly mainly due to the remarkable properties of silicon dioxide, used as a surface passivation layer on the silicon substrate, as a high-quality gate insulator, and as field isolation between adjacent devices. Unlike Si, Ge does not have a stable natural oxide than can passivate its surface. GeO_2 is known to be thermodynamically unstable at around 400 °C due to the formation of volatile GeO. The incorporation of nitrogen in the GeO layer has however been shown to improve the thermal stability of the insulator, and to lead to better Ge surface passivation.

It is widely recognized that one of the most difficult challenges in the development of Ge MOSFETs is the choice of surface and gate dielectric.

Property	silicon	germanium
Electron mobility (cm^2/Vs)	1400	3900
Hole mobility (cm^2/Vs)	450	1900
Bandgap (eV)	1.12	0.66
Lattice constant (Å)	5.431	5.658
Dielectric constant	11.7	16.2
Intrinsic conc. n_i/cm^3	$1.5x10^{10}$	$2.5x10^{13}$
Melting temperature (°C)	1410	934

Table 5.1: Properties of silicon and germanium

That is due to the retention of charge neutrality at the interface brought about by Fermi-level pinning. It has been found that this effect is caused by exponentially decaying interface states filling the semiconductor gap as a result of the disruption of periodicity at the interface. These states are generally a mixture of acceptor-like conduction band and donor-like valence band states, with the charge neutrality level (CNL) marking the intersection of the curves of conduction band and valence band density of state (DOS) at which their densities are equal. Unlike the case with Si, the CNL for Ge lies close to the valence band edge or below it. In the absence of gate bias, the semiconductor Fermi level E_F is aligned with the CNL so that the interface is neutral. Application of a positive gate bias depresses the conduction and valence bands and raises E_F (higher than CNL), causing more acceptor-like conduction band states to be filled by electrons and building up a fixed negative charge at the interface that screens off the applied positive gate bias. In other words, the effect in the case of an n-MOSFETs will be to repels electrons away from the surface. This makes it difficult to build an inversion layer in a n-MOSFET and to switch the device on, with highly adverse consequences for the device's operation. In the case of a p-MOSFET, the negative charge trapped at the interface attracts minority holes, helping to invert the channel which can cause the device to never be switched off. In fact, the presence of a negative fixed charge at the interface could shift the threshold voltage of the p-MOSFET to positive values, resulting in a conductive channel at zero gate bias [62, 63]. The value of E_F for a lightly doped Ge layer is closer to the intrinsic level, so that more acceptor-like states could be filled which would aggravate the issue. More recently, high-k gate dielectrics have been studied as possible gate insulators for Ge-based MOSFETs and good device characteristics - mainly for p-channel devices - have been demonstrated by combining these high-k gate dielectrics with Ge and by ensuring that the Ge

surface is properly passivated [59].

5.3 Fabrication of single-grain germanium

The procedure for obtaining single germanium grains is as follows. Firstly, 1 μm diameter holes are formed in the oxide and a 820 nm thick SiO_2 layer is then deposited by plasma-enhanced chemical vapor deposition of tetraethylorthosilicale (TEOS-PECVD) at a substrate temperature of 350 °C in order to reduce the hole diameter to approximately 200 nm. A film of amorphous germanium (a-Ge) 250 nm thick is then deposited by sputtering at a substrate temperature of 100 °C, 400 °C, and 550 °C. Finally, a single XeCl (308 nm) excimer laser pulse 20 ns long is used to irradiate the Ge surface with energy densities ranging from 200 to 800 mJ/cm^2. The different Ge grains obtained in this way were subjected to a battery of tests. The test results are presented and discussed in the next section.

5.3.1 Test results and discussion

Fig. 5.1 shows the SEM image of location-controlled Ge grains after island patterning. Energy dispersive x-ray (EDX) spectroscopy was used to confirm the purity of both sputtered and crystallized Ge (see Fig. 5.2). The EDX scan did not detect any argon (Ar) atoms introduced into the Ge film by the sputtering process. Very small amounts of silicon and oxygen were detected in the layer. However, measurements at different beams energies led to a reduction in the height of the silicon and oxygen peaks, indicating that the detection of these atoms is due to the SiO_2 underneath the Ge layer and not to physical admixture of SiO_2 in the germanium. Fig. 5.3 shows a microphotograph of four arrays of Ge grains with different grain filter distances, crystallized with a laser energy density of 700 mJ/cm^2. It was observed that 8 μm Ge grains were successfully positioned on the grain filters. The location control of Ge grains is achieved with a lower energy density range than that of Si, as shown in Fig. 5.4. This is consistent with the fact that Ge has a lower melting point than Si. Furthermore, the size of the Ge grains increases more rapidly as a function of the laser energy density than that of Si grains. That leads to a narrower process window (about 100 mJ/cm^2) for Ge crystallization than for Si crystallization (about 250 mJ/cm^2). When the laser energy density is increased above 725 mJ/cm^2, the Ge grain size actually falls (to about 3 μm) and the 2D location control of the Ge grains is lost, since the Ge grains are placed at random positions. Increasing the energy density even more (to 800

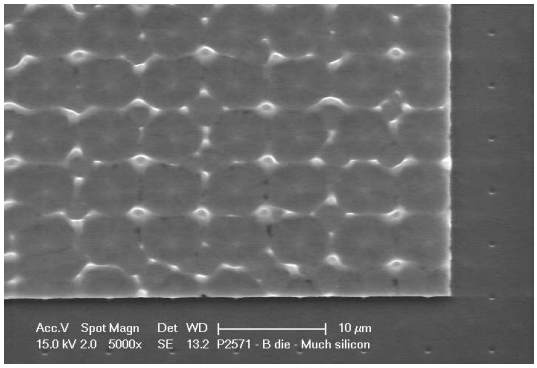


Figure 5.1: SEM image of single Ge grains grown by the μ-Czochralski process after island patterning.

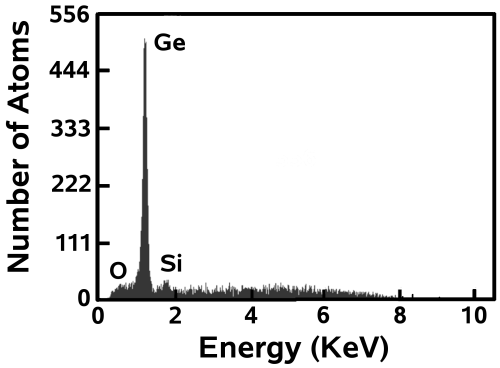


Figure 5.2: Energy dispersive X-ray (EDX) spectroscopy of single Ge grain before and after laser crystallization.

mJ/cm^2), leads to ablation of the Ge layer. Extending the pulse width of the excimer laser up to 480 ns is found to lead to successful production of Ge grains as much as 9 μm in size, as shown in Fig. 5.5. This is understandable, since a longer pulse duration means that the Ge will be molten for longer, thus prolonging the growth process through which the Ge grain is obtained from the seed placed at the bottom of the grain filter. These conditions also lead to a wider process window (about 150 mJ/cm^2). The effect of the a-Ge sputtering temparature on crystallization was also investigated. Decreasing the sputtering temperature of the a-Ge causes the laser energy density needed for Ge crystallization and the ablation threshold to drop, as shown in Fig.

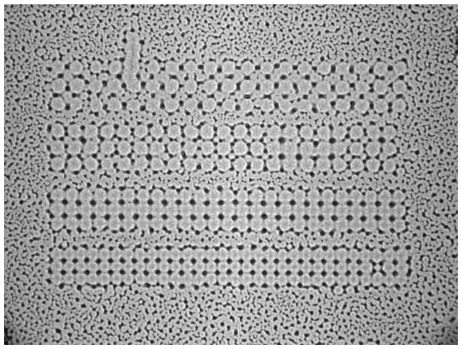


Figure 5.3: Microphotograph of single Ge grains sputtered at 550 °C and crystallized at 700 mJ/cm^2. Four arrays of single Ge grains with grain filter distances of 8, 7, 6, and 5 μm from top to bottom. This test structure served as a basis for a quick evaluation of the grain diameter. It is proved possible to grow 8 μm Ge grain in this set-up.

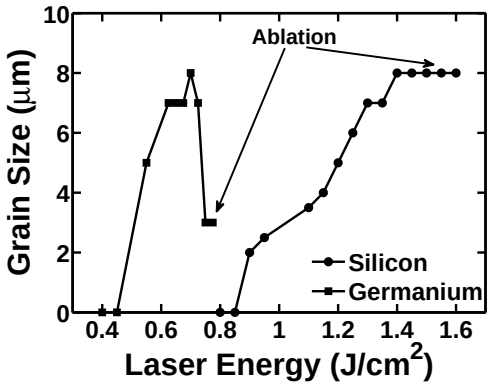


Figure 5.4: Grain size of location-controlled Ge sputtered at 550 °C and LPCVD Si deposited at 545 °C as a function of laser energy.

5.6. It also reduces the maximum grain size obtainable. At a sputtering temperature of 400 °C, the maximum possible grain size is 7 μm compared with the 8 μm obtained at 550 °C. At a sputtering temperature of 100 °C, the process window is slightly narrower ($<$ 100 mJ/cm^2) and the maximum grain size obtained is 5 μm. Fig. 5.7 shows the microphotograph of single Ge grains sputtered at 100 °C and crystallized at 500 mJ/cm^2. This figure confirms that a single Ge grain grown from a-Ge deposited at 100 °C can become as large as 5 μm. It is interesting to note that a-Ge sputtered at temperatures as low as

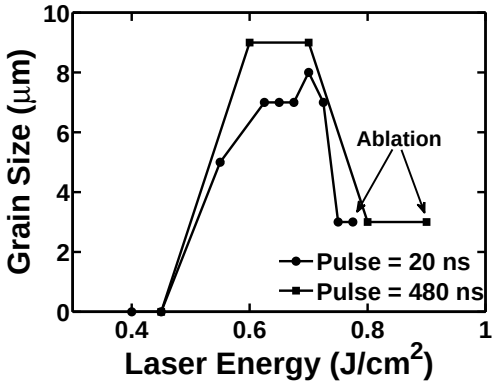


Figure 5.5: Grain size of location-controlled Ge sputtered at 550 °C and crystallized at different pulse widths as a function of laser energy.

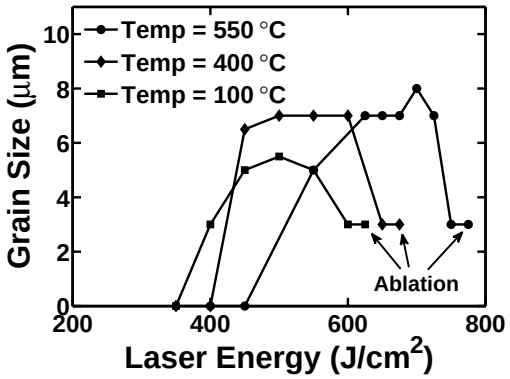


Figure 5.6: Ge grain size versus laser energy for different a-Ge sputtering temperatures.

100 °C can still fill the grain filters properly, as shown by the relatively large grains sizes achievable.

An important analytical tool that can be used to confirm the crystalline structure of the Ge layer is electron backscattering diffraction EBSD scan of the location-controlled Ge grains are shown in Fig. 5.8. As may be see from Fig. 5.8(a), Ge grains grown in 100 nm grain filters have a single-crystalline structure, with planar defects (mainly $\Sigma 3$ and $\Sigma 9$) originating in the grain filter holes. Random grain boundaries are only found on the edge of the grain,

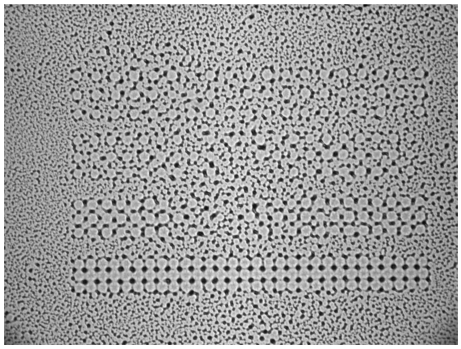
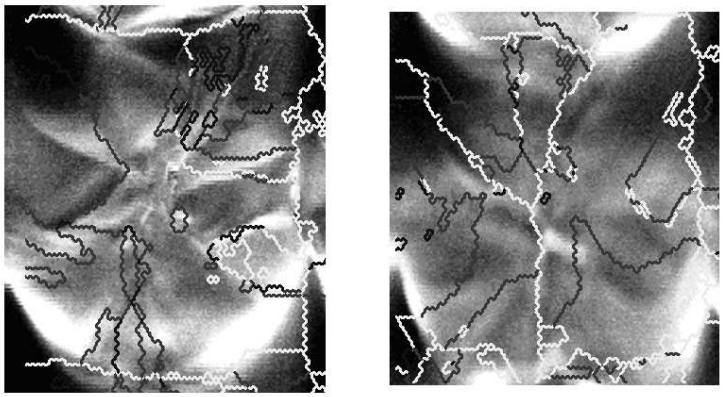


Figure 5.7: Microphotograph of single Ge grains sputtered at 100 °C and crystallized at 500 mJ/cm^2. Four arrays of single Ge grains with grain filter distances of 8, 7, 6, and 5 μm are shown from top to bottom. It proved possible to grow 5 μm Ge grain in this set-up.



(a) (b)

Figure 5.8: Electron backscattering diffraction (EBSD) images of Ge crystals grown using grain filter sizes of 100 nm (a) and 500 nm (b). The white lines are random grain boundaries, and the dark ones Σ3 and Σ9 CSL boundaries.

at the interface with other grains. Increasing the grain filter diameter can have an adverse effect on the crystalline quality of the Ge: as shown in Fig. 5.8(b), location-controlled grains grown in grain filters 500 nm in diameter have a significant number of random grain boundaries, which tend to be produced when the filtering of grains decreases.

5.4 Germanium SG-TFTs

The fabrication of single grain Ge TFTs (Ge SG-TFTs) is not straightforward. There are many issues to be resolved related to the water-soluble native Ge oxide that is typically present on the upper surface of a Ge layer. Once the single Ge grain has been grown and the active island patterned, cyclic dip etching with 1% HF and H_2O for 15 sec each with a total etching time of 5 min is used for effective surface oxide removal [64, 65]. The Ge layer is then nitrided by ICP-ECVD at 250 °C to form an interfacial layer of germanium oxynitride (GeON), which is stable and has better passivation properties than native Ge oxide [59, 66, 67]. The next step is to deposit 80 nm of SiO_2 without breaking vacuum. Aluminum is then sputtered on the SiO_2, and patterned by dry etching landed on the unetched SiO_2 layer. Source and drain implantation with a 10^{16} cm^{-2} dose of boron at an energy of 40 KeV is performed through the SiO_2 layer, followed by laser annealing. A passivation SiO_2 layer is deposited by TEOS PECVD, and the device is metalized after creation of the contact opening and cyclic dip etching. Test on p-channel Ge SG-TFTs prepared in this way gave encouraging results. By way of example Fig. 5.9 shows the transfer characteristic and hole field-effect mobility of a p-channel Ge SG-TFT with a a drain voltage of -0.05 V compared with those of a SOI-TFT. Since the equivalent oxide thickness $t_{eq} = EOT_{GeON} + t_{SiO_2}$ may be assumed to approach that of the silicon dioxide layer t_{SiO_2} because the equivalent oxide thickness of the oxynitride EOT_{GeON} is negligible [68], a hole field-effect mobility of 800 cm^2/Vs is successfully achieved, which is about four times higher than that found for the SOI-TFT. This result confirms the good quality of single Ge grains obtained by the μ-Czochralski process, despite the low a-Ge sputtering temperature of 100 °C used. Fig. 5.9 also shows the positive threshold voltage of these devices, confirming the existence of a pinning effect that induces a negative charge at the interface with consequential threshold voltage shift. The pinning effect that induces a high leakage current in p-channel Ge SG-TFTs (where the on/off ratio is measured to be about 10^2) and an extremely low on current in n-channel Ge SG-TFTs is an issues that still has to be resolved. It is not related to the quality of the single Ge grain but to the defective Ge-oxide interface - a matter which is still under investigation. The high leakage current in p-channel Ge SG-TFTs is also related to the existing Ge/buried-oxide interface that may generate current flow even in the absence of gate control. Details of a single Ge grain fabricated by μ-Czochralski process but deposited on a different buried oxide (alumina) as a possible solution to this problem are given in the next section.

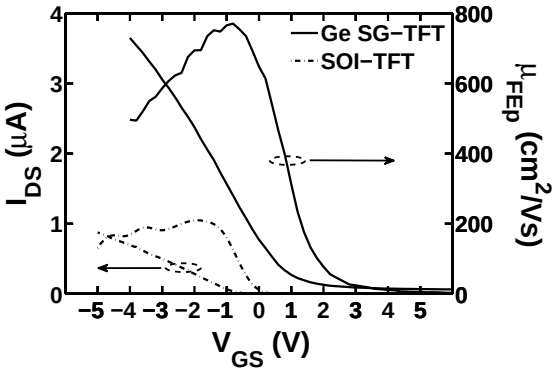


Figure 5.9: Linear transfer characteristics for V_{DS} = -0.05 V and field-effect mobility of Ge SG-TFTs obtained by crystallization of a-Ge sputtered at 100 °C compared with those for SOI-TFT.

5.5 Grain filter with Al_2O_3 buried oxide deposited by ALD

Many high-k technologies that might overcome the Ge-oxide interface issue are being studied. These include the use of Al_2O_3 as gate insulator, which has given encouraging preliminary results in both p- and n-channel devices [69]. Ge grain filters with Al_2O_3 grown by atomic layer deposition (ALD) have therefore been fabricated and tested as part of the present study. The process begins with formation of 1 μm diameter holes in the silicon oxide layer. A layer of TEOS 790 nm thick is then deposited by PECVD in each hole followed by 30 nm of Al_2O_3 deposited by ALD. Finally, a-Ge is sputtered at 550 °C and crystallized by excimer laser. The resulting structure is shown in Fig. 5.10.

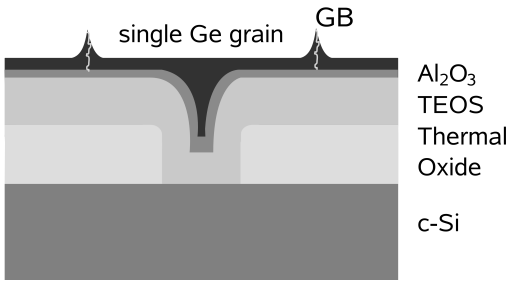


Figure 5.10: Single Ge grain grown on Al_2O_3 deposited by ALD and TEOS deposited by PECVD.

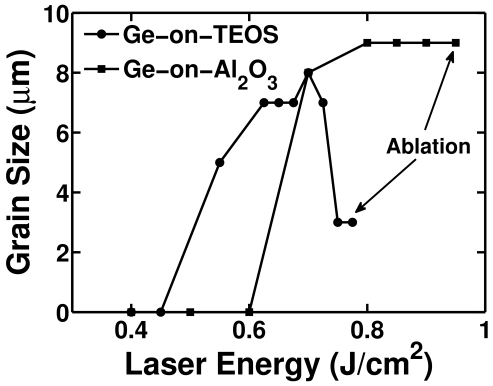
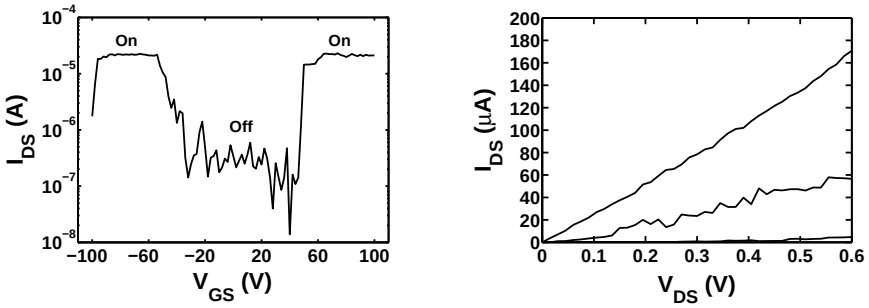


Figure 5.11: Size of single Ge grains grown from a-Ge sputtered at 550 °C on TEOS or stack of Al_2O_3 deposited by ALD on TEOS, as a function of the laser energy used for crystallization.

Single Ge grains as large as 9 μm have been successfully grown in this way. Fig. 5.11 shows the Ge grain diameters achieved as a function of the laser energy compared with the results for Ge sputtered directly on TEOS. These Ge grains have been used to pseudo-TFT devices by connecting two probes to the grain to form the source and drain terminals, while the substrate is employed as gate contact. Pseudo-MOSFET techniques were then used to extract key electrical data directly from the Ge active layer with very little processing [70]. When positive gate voltage are applied to the back gate in p-type Ge active layer, an inversion layer of electrons is formed at back Ge-oxide interface, and when such voltages are applied to the back gate in n-type Ge active layer, an accumulation layer of electrons is formed at back Ge-oxide interface. When on the other hand a negative gate voltage is applied to the back gate, an accumulation layer of holes is formed at the back gate of p-type Ge active layer and an inversion layer in n-type one. In this way, it is possible to characterize both n-channel and p-channel devices. Although as may be seen from Fig. 5.12(a) the on/off ratio of these devices remains of the same order of magnitude (about 10^2) as that measured above, the drain-induced barrier lowering is strongly reduced, as shown by the pseudo-output characteristics of Fig. 5.12(b) where the leakage current measured at zero gate voltage remains low as the drain voltage increases. More significantly, the pseudo-transfer characteristic of Fig. 5.12(a) shown that pseudo n-channel Ge devices do allow an electron inversion layer to be successfully built up, thus emulating the response to positive gate voltages found in n-channel Ge SG-TFTs. Summing up, it may be stated that an Al_2O_3 gate insulator deposited



(a) (b)

Figure 5.12: Transfer characteristic for $V_{DS} = 0.1$ V (a) and output characteristics (b) of pseudo Ge SG-TFT with stack of 790 nm TEOS and 30 nm Al_2O_3.

by ALD improves the quality of Ge/insulator back interface in Ge SG-TFT; and if it is also used as front insulator, it can successfully permit the inversion of n-channel Ge SG-TFTs.

5.6 Conclusion

It has been shown in this chapter that 2D location-controlled single Ge grains with a diameter of 8 μm can be successfully obtained by the μ-Czochralski process after sputtering the Ge at different temperature down to 100 °C. The energy density required for the crystallization was lower than for Si, because of the lower melting point of germanium. The process window needed to obtain Ge grains as large as 8 μm in diameter is narrower than that for silicon grains. It has also been found that single Ge grains have no random grain boundaries when a grain filter size as small as 100 nm is used. The high crystal quality of Ge grains obtained by the μ-Czochralski process is confirmed by the hole field-effect mobility of 800 cm^2/Vs measured in p-channel Ge SG-TFT, which is around four times higher than that measured in SOI-TFTs. It has furthermore been shown that the use of Al_2O_3 deposited by ALD as buried oxide consistently improves the quality of the Ge/insulator back interface. The Al_2O_3 makes it possible to achieve a low leakage current as the drain voltage increases in p-channel pseudo-TFTs, and to build up the desired electron inversion layer in n-channel pseudo-TFTs.

Chapter 6

Strained single grain Si TFTs

This chapter deals with the fabrication and characterization of single grain Si TFTs in which the Si grain is subjected to tensile strain induced by an excimer laser. This high tensile strain, the absence of random grain boundaries in the grain, the high quality of the Si/SiO_2 interface, and the insignificant roughness of the single grain surface fabricated by the μ-Czochralski process all contribute to the excellent electron and hole mobility of this device - 1.6 times higher than that measured in SOI-TFTs.

6.1 Strained silicon microelectronics

Strained-silicon technology is the most advanced microelectronics solution known at present for enhancing n- and p-channel mobilities and resolving the CMOS scaling issue. The technique normally used at the moment to generate tensile strain in silicon is to grow the silicon layer epitaxially on relaxed SiGe [71–73], as shown in Fig. 6.1. If the growth temperature exceeds a certain limit and the silicon layer is not allowed to grown up to its critical thickness, the silicon layer will be under biaxial tensile strain and the in-plane lattice constant will be increased above the equilibrium value. If these conditions are not met, dislocations will be formed leading to relaxation of the silicon layer. The biaxial tensile strain produced in this way affects the structure of the silicon's conduction and valence bands, as shown in Fig. 6.2. It causes the six-fold degenerate valley to split into two groups. The lower-energy group is two-fold degenerate, and the valleys have the longitudinal mass normal to the heterointerface and the transverse mass parallel to it. The other, higher-energy, group consists of four-fold degenerate valleys that have the transverse mass normal to the heterointerface. Moreover, the strain splits

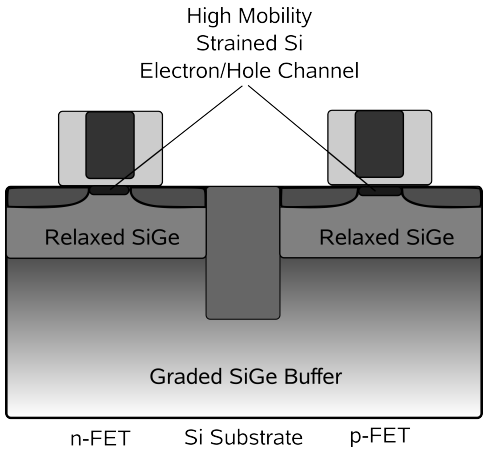


Figure 6.1: Schematic view of CMOS strained silicon on relaxed SiGe layer grown from silicon substrate.

the light-hole/heavy-hole degeneracy (valence-band degeneracy) at the Γ-point and shifts the spin-orbit band. This leads to enhancement of the electron and hole mobilities due to a drop in the carrier conductivity, effective mass and intervalley scattering rates [74]. The mobility enhancement factor depends on the tensile strain, which is a function of the germanium content of the relaxed SiGe layer, as reported by *S. Takagi et al.* for nMOS and *R. Oberhuber et al.* for pMOS (see Fig. 6.3). However, the high temperatures (> 750 °C) at which this technology is produced limit its use to IC microelectronics.

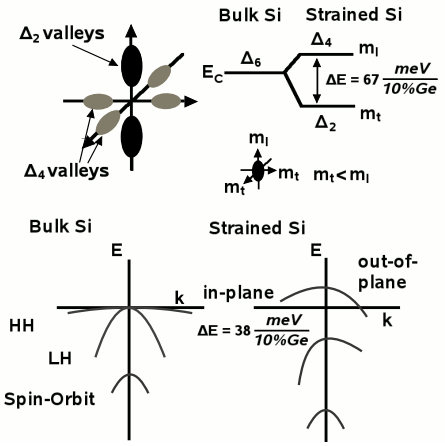


Figure 6.2: Effects of biaxial tensile strain on structure of silicon conduction and valence bands.

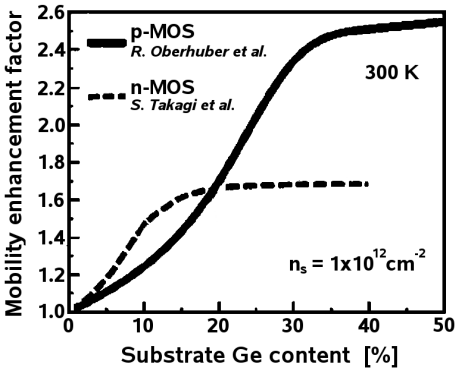


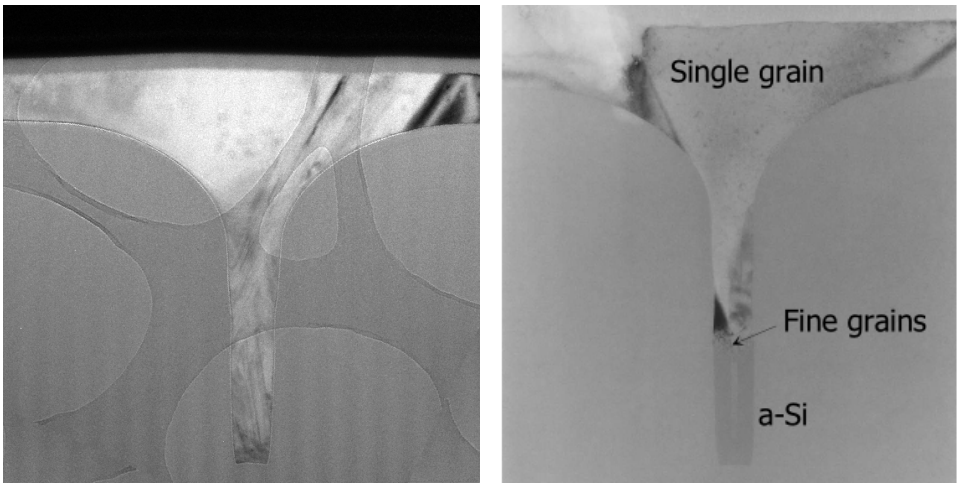
Figure 6.3: Enhancement factor of electron and hole mobilities due to tensile strain as a function of germanium content in $Si_{1-x}Ge_x$.

It is well known, on the other hand, that polysilicon crystallized by excimer laser has intrinsic tensile strain [75–77]. The microscopic origin of the strain lies in the thermal stress built up during crystallization, and could be due to the difference in thermal expansion coefficients between substrate and polysilicon film [76]. Mobility enhancement in poly-Si TFTs induced by intrinsic tensile strain has not yet been reported in the literature, however. As part of the present study, details of the electron and hole mobility enhancement due to the intrinsic tensile strain in single-grain silicon TFTs fabricated by the μ-Czochralski process and the high crystal quality of single grains were determined. The results of this investigation are summarized in the present chapter.

6.2 Fabrication of strained SG-TFTs

After the grain filters have been produced [12], a 250 nm thick a-Si film is deposited in each hole by LPCVD. After implantation of boron (B) ions at a concentration of 2.5x10^{11} cm^{-2} for threshold-adjustment in both n- and p-channel transistors, a single 20 ns long pulse of light from a XeCl (308 nm) excimer laser is used to irradiate the Si surface with very high energy densities, very close to the ablation. This causes the Si layer including the grain filter to be entirely melted and crystallized [28] as can be seen from Fig. 6.4(a), which shows the bottom part of the grain filter in a cross-sectional TEM image of the relevant Si crystal. This contrasts with the partial molten condition found in previous works [78], as shown in Fig. 6.4(b).

This procedure allows strained Si grains with diameters as large as 8 μm



(a) (b)

Figure 6.4: TEM images of single Si grain cross section after laser crystallization under complete (a) and partial (b) melt conditions. The difference between the complete and partial melt conditions may be seen by inspection of the bottom part of the grain filter.

to be obtained in predetermined positions with the aid of μ-Czochralski crystallization [16]. The silicon film is then patterned into islands by reactive ion etching, and an 80 nm SiO_2 layer is added as a gate insulator by inductively coupled plasma enhanced chemical vapor deposition (ICP-ECVD) at 250 °C [79]. Aluminum sputtered at room temperature forms the gate electrode. The source and drain are implanted with either P or B ions ($1x10^{16}$ cm^{-2}) depending on the device type, and activated by excimer laser annealing. After SiO_2 passivation and contact hole formation, Al interconnect metal is sputtered and patterned. SG-TFTs were fabricated inside the location-controlled grains obtained by the μ-Czochralski process as described above, where no random grain boundaries (GBs) but only a few coincident site lattice grain boundaries (CSL-GBs) were present. The position of the SG-TFT channel inside the grain was varied as described in a previous publication [17]. The channel can be placed in a central C position, from which CSL-GBs may radiate in all directions, or in positions X and Y, where radially grown CSL-GBs may be parallel or perpendicular to the carrier flow respectively, as depicted in Fig 6.5. TFTs were also fabricated on a silicon-on-insulator (SOI-TFTs) wafer with a doping concentration of silicon top layer of about $3x10^{14}$, to provide reference device. The devices fabricated as described above were subjected to a battery of tests. The test results are presented and discussed in the next

section, after a series of introductory remarks.

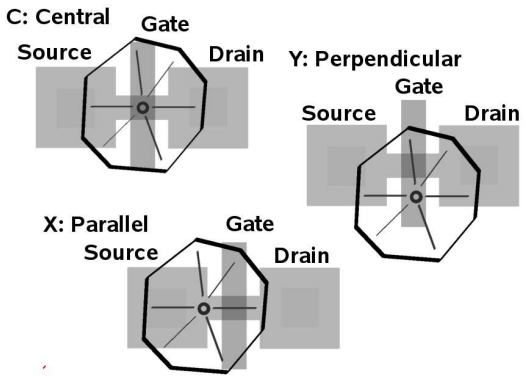


Figure 6.5: Position of TFT inside the grain.

6.3 Test results and discussion

Before the result of the measurements on the new strained single grain Si TFTs can be discussed in section 6.3.4, a number of aspects of devices of this type need to be examined.

Previous workers have established that polysilicon TFTs possess an intrinsic tensile strain [75–77]. However, the effect of this strain in increasing the electron and hole mobility of these TFTs was canceled out by a combination of the following effects:

- the presence of random grain boundaries in the channel
- high density of trap states at Si/SiO_2 interface
- elevated roughness of the Si surface

The random grain boundaries cause lattice discontinuities, leading to a high density of defects [9] with consequential formation of trapping states, which strongly affects carrier conduction. The high density of trap states at the Si/SiO_2 interface also affects the conductivity, especially in the subthreshold region. Furthermore, the rough silicon surface leads to additional scattering at the interface when a high gate voltage is applied to the TFT (see Fig. 6.6).

On the other hand, the electron and hole field-effect mobilities of SG-TFTs fabricated by the μ-Czochralski process can be made higher than those

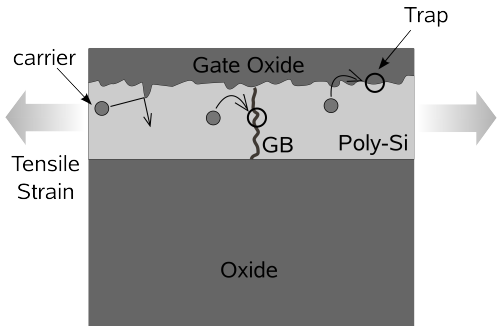


Figure 6.6: Schematic view of impeding strain-induced increase in mobility in poly-Si layer.

in SOI-TFTs, when the silicon layer is completely melted during crystallization as described in section 6.2. There are various reasons for this, which will be explained in the following sections.

6.3.1 Quality of strained single-grain silicon TFTs fabricated by the μ-Czochralski process with ICP-ECVD gate oxide

The only defects found in the channel of SG-TFTs fabricated as described in section 6.2 are CSL-GBs ($\Sigma 3$ and $\Sigma 9$) as shown in the EBSD image of Fig. 6.7; any random GBs that occur are found outside the channel area. The density of trap states computed for $\Sigma 9$ by *Ab-Initio* atomic simulation is much lower than that of random GBs, and the corresponding potential barrier is also much lower than that for random GBs. The potential barrier of $\Sigma 3$ CSL-GBs is so low as to be negligible. It follows that the carrier mobility is not affected by the CSL-GBs [20].

Interface defects mainly due to a lack of Si-SiO_2 bonds lead to the formation of trap states in the forbidden band-gap.

Those traps induce higher subthreshold slope S and lower mobility, since the carriers are not free to flow through the channel but are captured and scattered. However, the use of a SiO_2 layer formed by inductively coupled plasma enhanced chemical vapor deposition (ICP-ECVD) as gate oxide instead of the TEOS-PECVD used previously leads to a substantial improvement in the mobilities and subthreshold characteristic thanks to a density of interface trap states (D_{it}) as low as $2\text{x}10^{10}$ $eV^{-1}cm^{-2}$ (see Fig. 6.8) [79], which is close to the value obtained with thermal oxide despite the low deposition temperature (250 °C).

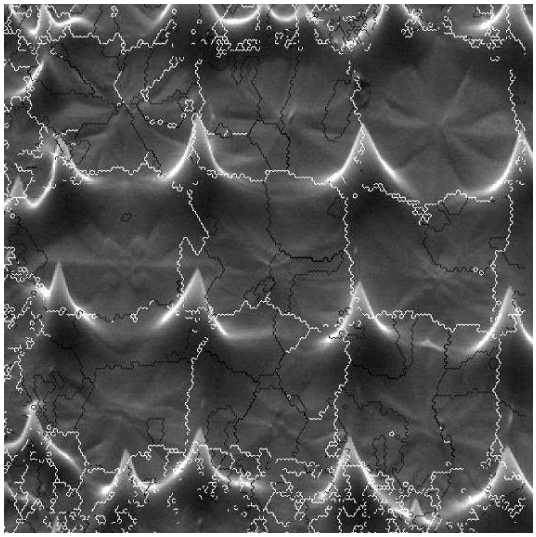


Figure 6.7: EBSD image of location-controlled strained silicon grains: bright lines are random grain boundaries, which are only found at the edges of single grains, while the darker lines are Σ3 and Σ9 CSL-GBs.

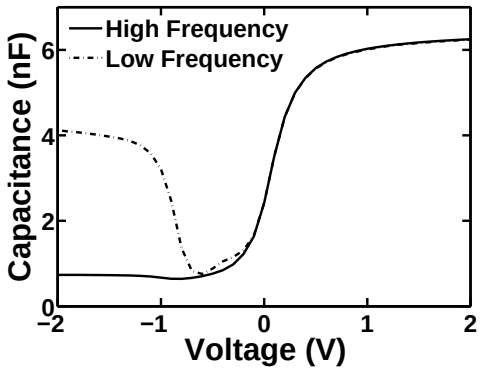
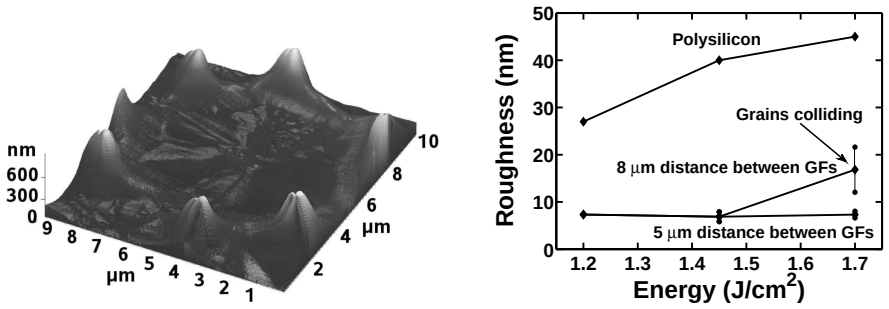


Figure 6.8: Measured capacitance-voltage curves for ICP-ECVD MOS capacitor at low and high frequencies. The extracted D_{it} is as low as $2x10^{10}$ $eV^{-1}cm^{-2}$.

6.3.2 Surface roughness of silicon

The roughness of the silicon surface also plays an important role. It leads to additional scattering at the interface with consequent mobility reduction

when the gate voltage is applied. Atomic force microscopy (AFM) was used to analyze the roughness of the silicon surface (see Fig. 6.9). This reveals that the surface roughness of single-grain silicon fabricated by the μ-Czochralski process is substantially lower than that measured for polysilicon. Furthermore, higher laser energy densities are associated with higher roughness in polysilicon. That is due to the formation of taller hillocks on the surface when grains collide. In the grains fabricated by the μ-Czochralski process, on the contrary, the surface hillocks are location-controlled out of the single grain, thus allowing the surface roughness of the single-grains to be kept uniformly kept as low as 7 nm, independently of the laser energy density used. In other words, increasing of the laser energy density is bad for the surface roughness of polysilicon but has no influence on the roughness of single-grain Si fabricated by the μ-Czochralski process. However, as shown in Fig. 6.9(b), if the distance between grain filters is such as to lead to major collisions between the grains grown by the μ-Czochralski process, then the in-grain surface roughness of this material is also affected by increasing the laser energy density.



(a) (b)

Figure 6.9: (a) AFM image of single grain fabricated by the μ-Czochralski process. (b) RMS value of surface roughness derived from AFM image for the μ-Czochralski process compared with polysilicon. The dependence of the RMS roughness of the Si grain by μ-Czochralski process on the distance between the grain filters (GFs) is also indicated.

6.3.3 Properties of tensile strained silicon layer

The tensile strain of the Si grains was also studies by Raman spectroscopy, as shown in Fig. 6.10. The measured Raman shift for a single grain is about -2.53 cm^{-1} for a laser energy density of 1400 mJ/cm^2. Increasing the laser

energy density to a level corresponding to the completely molten condition (1700 mJ/cm^2) causes the Raman shift to increase to -4.45 cm^{-1}. Careful checks showed that this shift was not due to heating of the sample by the Raman laser, since the Raman peak did not change when the Raman laser energy was increased. The full width at half maximum (FWHM) is just slightly greater than that for crystalline silicon, confirming the excellent crystal quality of the single-grain silicon fabricated by the μ-Czochralski process.

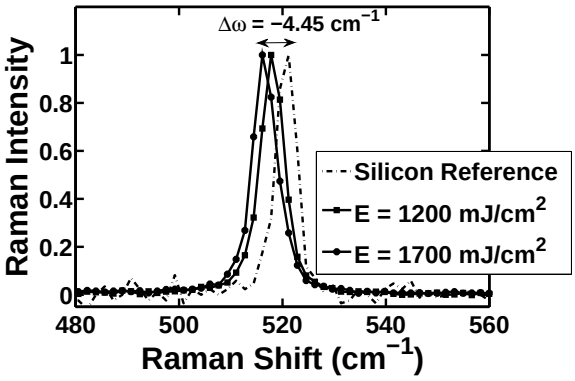


Figure 6.10: Raman spectroscopy of crystalline silicon reference and single grain silicon by μ-Czochralski process obtained by two different energy densities

The thermal stress σ_{th} can be estimated from the following expression [76]:

$$\sigma_{th} = (\alpha_f - \alpha_s)\Delta T \frac{E_f}{1 - y_p} \tag{6.1}$$

where α_f and α_s are the average thermal expansion coefficients of the film and the substrate respectively. ΔT is the difference between the crystallization temperature and the initial temperature of the film, E$_f$ is the elastic (Young's) modulus of the film and y$_p$ is the Poisson's ratio. The thermal stress built into the film is tensile if $\alpha_f > \alpha_s$, as is the case here. The estimate of the thermal stress derived from this analysis is about -1.22 GPa, which is in excellent agreement with the tensile stress calculated from the Raman shift using the conversion rule [76]:

$$\sigma_{th} = -0.27(GPa/cm^{-1})\Delta\omega(cm^{-1}) \tag{6.2}$$

where $\Delta\omega$ is the Raman shift. This yields a tensile stress of 1.20 GPa at the complete-melt condition. It should be noted, however, that the complete-melt region is close to the ablation region. That could cause manufacturing problems due to the statistical variation of the laser energy when large areas are to treated. In order to enlarge the process window of the complete-melt condition, a laser pulse width longer than 20 ns is needed for the crystallization of a-Si.

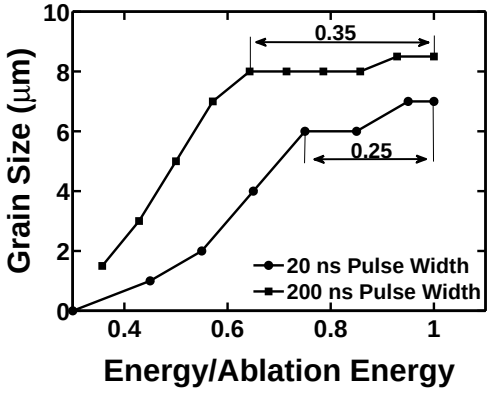


Figure 6.11: Single grain size of a silicon layer of thickness 100 nm as a function of the laser energy density normalized with respect to the ablation energy density, for two different pulse widths.

Fig. 6.11 shows the grain size as a function of laser energy density normalized with respect to the ablation energy. The grain size increases with the laser energy because the rise in the amount of heat stored in the SiO_2 delays the nucleation in the melt outside the grain. The complete-melt threshold of the grain filter corresponds to the point where the grain size/energy curve levels off. The existence of this threshold is due to the fact that the melting of the grain filter induces severe undercooling of the melt to initiate solidification, thus reducing the time difference between the onset of solidification and nucleation outside the grain. The measured energy density window of the complete-melt condition is only 25% of the total window for a pulse width of 20 ns and an a-Si thickness of 100 nm. When a 200 ns pulse width is used, the corresponding process window is enlarged up to 35% as shown in Fig. 6.11.

6.3.4 Results of measurements on strained SG-TFTs

The results of measurements of n- and p-channel strained SG-TFTs are presented in the this section. The field-effect mobilities were evaluated from the transconductance characteristic at drain voltage of 0.05 V [43]. Previous studies had shown that the measured field-effect mobility of n-channel SG-TFTs is about 600 cm^2/Vs over a wide range of energy densities [39]. At the complete-melt condition, a mean field-effect mobility value of 883 cm^2/Vs and peak of 1400 cm^2/Vs at the X position were found for the strained SG-TFTs investigated in the present study. Mean field-effect mobilities of 814 cm^2/Vs and 773 cm^2/Vs were obtained for our strained SG-TFTs at the C and Y positions respectively, as shown in Fig. 6.12. Similarly, the measured field-effect mobility of the p-channel SG-TFTs has previously been found to be about 250 cm^2/Vs over a wide range of laser energy densities [19]. In the present study, a mean field-effect mobility of 320 cm^2/Vs with a peak of 500 cm^2/Vs was found at at the complete-melt condition.

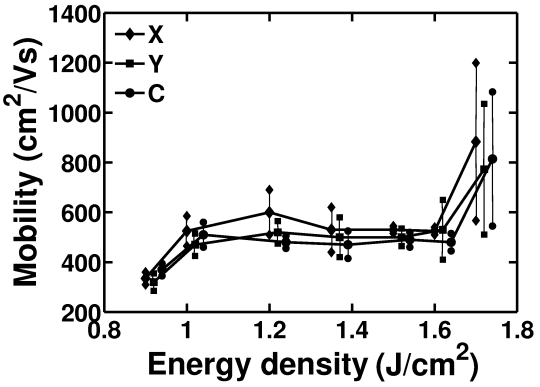


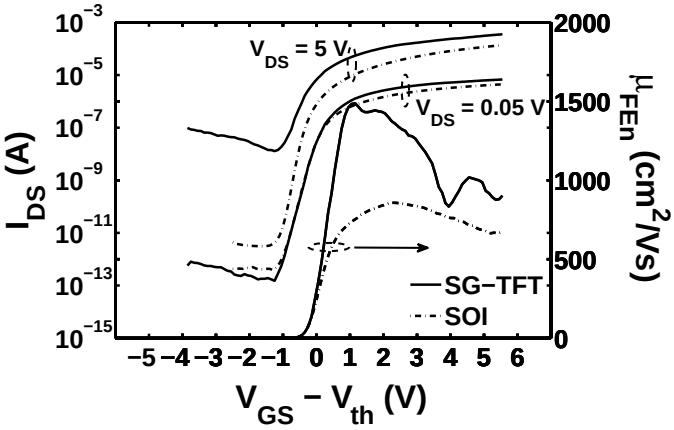
Figure 6.12: Electron field-effect mobility values calculated for strained n-channel SG-TFTs fabricated by different laser energy densities.

Figures 6.13 and 6.14 show the electrical characteristics of strained n- and p-channel SG-TFTs compared with those of SOI-TFTs. Fig. 6.13(a) gives the transfer characteristics and field-effect electron mobilities of strained n-channel SG-TFTs compared with those of the SOI counterpart, while Fig. 6.14(a) gives the corresponding output characteristics. Fig. 6.13(b), on the other hand, shows the transfer characteristics and field-effect hole mobilities of p-channel SG-TFTs compared with those of the SOI counterpart while Fig. 6.14(b) gives the corresponding output characteristics. It will be seen

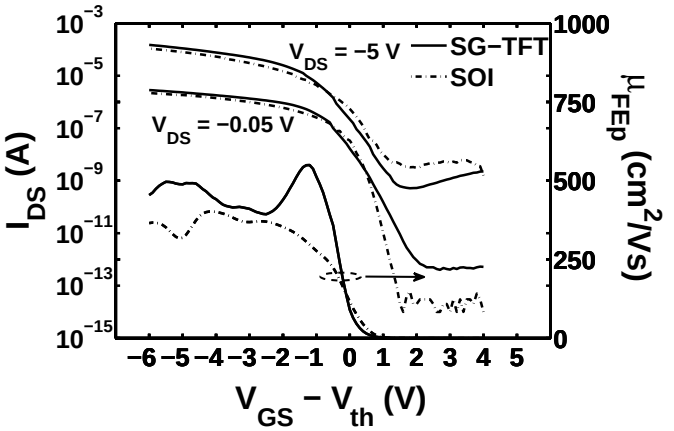
that strained SG-TFT yields field-effect mobility enhancements of a factor of about 1.6 for both electrons and holes. Such enhancements correspond to those found for strained Si grown on relaxed $Si_{80}Ge_{20}$ n- and p-channel MOSFETs (i.e. relaxed SiGe layer with 80% silicon and 20% germanium), according to the curves published by S. Takagi et al. [80] and R. Oberhuber et al. [81] respectively (see 6.3). Furthermore, our strained n-channel SG-TFT exhibits a subthreshold slope S as low as that of a SOI-TFT (106 mV/dec). Our strained p-channel SG-TFT shows a subthreshold slope S of 183 mV/dec, which is slightly higher than that of a SOI-TFT (156 mV/dec). The low subthreshold slope S shown by both n- and p-channel strained devices confirms the low D_{it} given by the used of an ICP-ECVD gate oxide, as mentioned in section 6.3.1. However, as shown in Fig. 6.12, the variation of the carrier mobility of strained SG-TFTs fabricated by the μ-Czochralski process increases at the complete-melt condition. This could be due to the greater dependence of the electron and hole mobilities on surface and in-plane orientations when the silicon layer is under tensile stress [74].

6.4 Device simulation results

Further confirmation that the field-effect mobility enhancement reported above is due to induced tensile strain was provided by simulation on the Sentaurus TCAD platform, making use of an advanced strained silicon model that computes second-order stress-dependence isotropic enhancement factors for low-field mobility [44]. The relevant parameters were first extracted by fitting n- and p-channel SOI-TFTs field-effect mobilities and transfer characteristics for drain voltages of 0.05 V and -0.05 V respectively [82]. The strained model with a tensile stress value of 1.20 GPa determined in section 6.3.3 was then added to the basic SOI-TFT extracted model. A good fit is obtained between the simulation and measurement results for both strained n- and p-channel SG-TFTs, as may be seen from the transfer and transconductance characteristics of Fig. 6.15. This provides the desired additional confirmation that the mobility enhancement effect in strained SG-TFTs is due to the tensile strain induced by the excimer laser, the low density of trap states at Si/SiO_2 interface, the low surface roughness and the high crystal quality due to inactive CSL-GBs of single-grain silicon fabricated by the μ-Czochralski process.



(a)

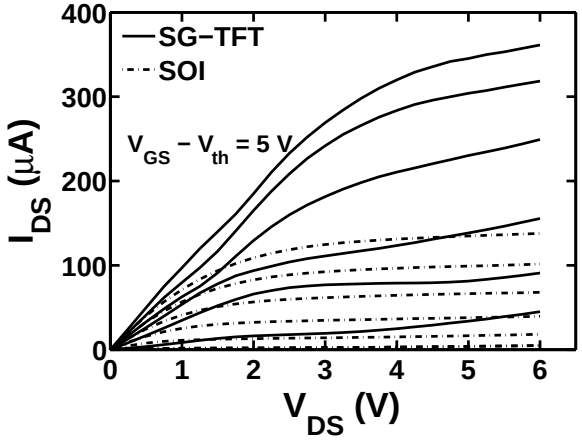


(b)

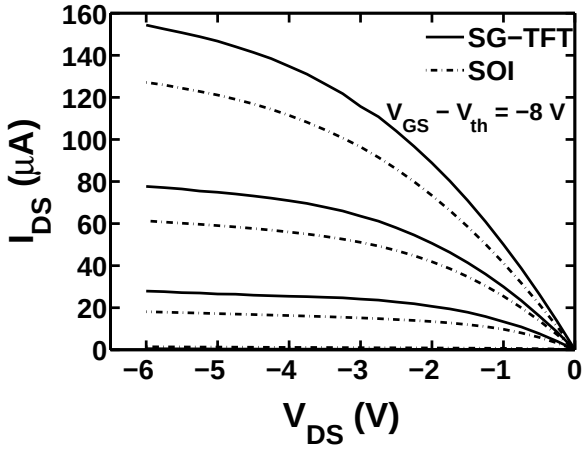
Figure 6.13: Transfer characteristics and field-effect mobility of n-channel (a) and p-channel (b) strained SG-TFTs compared with those found for SOI-TFTs.

6.5 Predicted RF performance of strained SG-TFTs

A prediction of the unity-gain bandwidth of strained SG-TFTs fabricated by the μ-Czochralski process is derived in this section. Firstly, the DC parameters of the BSIMSOI model were extracted from the characteristics of



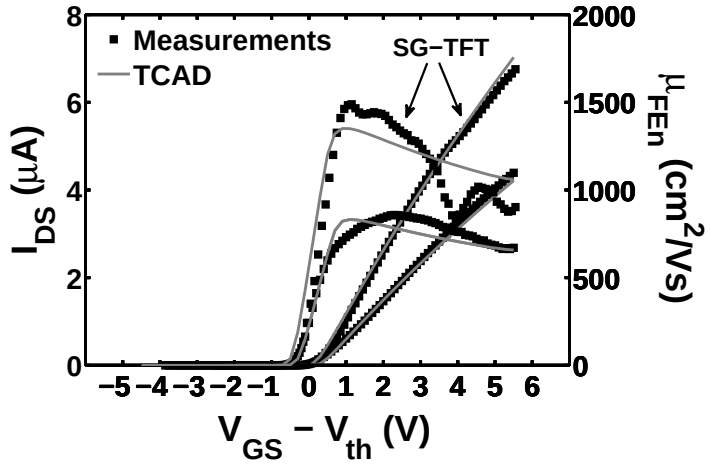
(a)



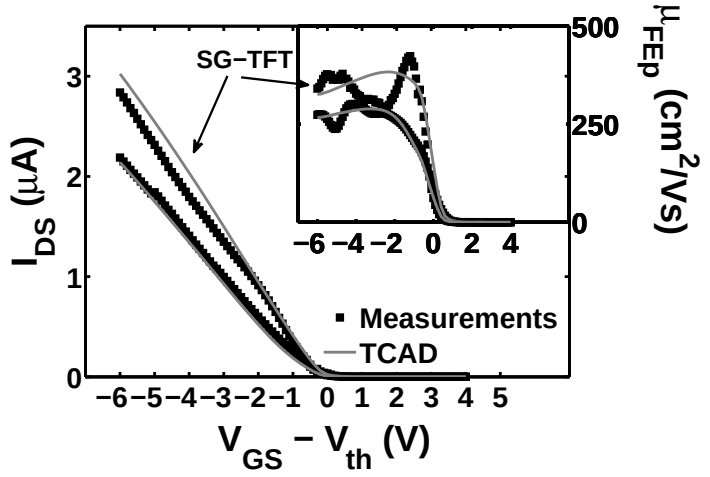
(b)

Figure 6.14: Output characteristics of n-channel (a) and p-channel (b) strained SG-TFTs compared with those found for SOI-TFTs.

the strained SG-TFTs given above. Unlike the situation described in Chapter 2, the main parameters extracted for the strained SG-TFTs were as follows: percentage of CSL-GBs $\alpha = 0$, in-grain mobility $\mu_G = 1000$ cm^2/Vs, and saturation velocity $v_{sat} = 1.2\text{x}10^6$ cm/s. These parameters yield a good fit between measured and simulated transfer and transconductance characteris-



(a)

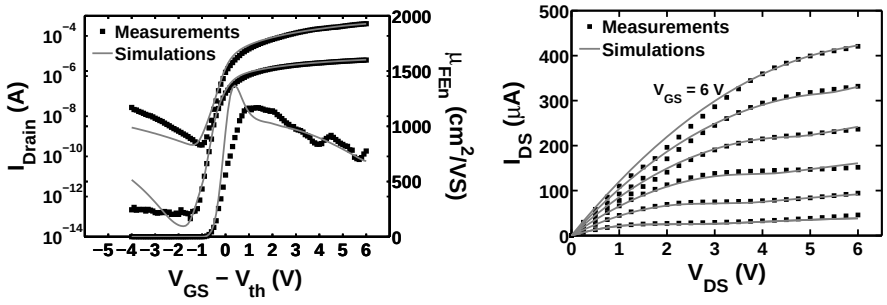


(b)

Figure 6.15: Measured and TCAD simulated field-effect mobility and transfer characteristics at 0.05 V drain voltage of n-channel (a) and p-channel (b) SOI MOSFETs and strained SG-TFTs.

tics, as shown in Fig 6.16. On the assumption that the remaining CV and RF parameters are identical to those for the technology discussed in Chapter 2, SPICE simulations were performed to predict the transit frequency f_T of strained SG-TFTs with the same channel dimensions and gate thickness as

the one measured in Chapter 2 (W_{eq} = 500 μm, L = 1.5 μm and t_{ox} = 30 nm). The predicted value of f_T is as high as 100 GHz, as shown in Fig. 6.17, and amplifiers can be designed in the units of GHz frequencies range with expected gains of the order of 10 dB. A possible application of this technology might be found in flexible plastic antennas incorporating flexible active circuitry operating in the $S-band$ (5 GHz) [1].



(a) (b)

Figure 6.16: Measured and BSIMSOI SPICE simulated field-effect mobility and transfer characteristics at 0.05 V drain voltage (a) and output characteristics (b) of strained n-channel SG-TFT.

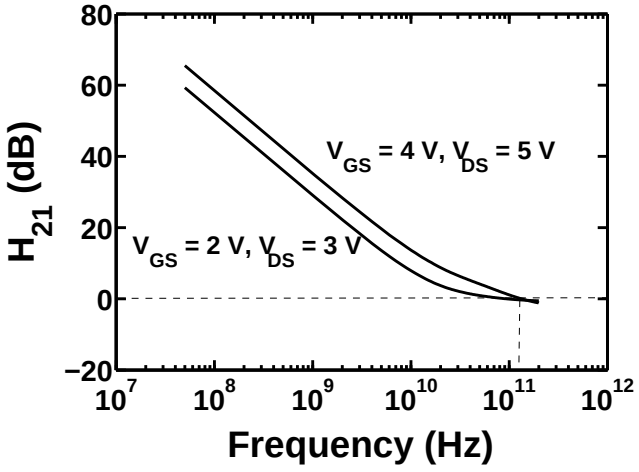


Figure 6.17: Predicted of H_{21} parameter of strained n-channel SG-TFT with W_{eq} = 500 μm, L = 1.5 μm and t_{ox} = 30 nm.

6.6 Conclusion

High performance n- and p-channel strained single-grain Si TFTs have been successfully fabricated by the μ-Czochralski process at low temperatures. It has been shown that the electron and hole field-effect mobility of such strained SG-TFTs at complete-melt condition can be enhanced by a peak factor of 1.6 times compared with SOI-TFTs. The higher carrier mobilities of these strained SG-TFTs compared with those of SOI-TFTs can be explained by the low DOS of CSL-GBs present in the channel, the low D_{it} at Si/SiO_2 interface, the low surface roughness of the silicon and the high tensile strain induced by the excimer laser at the complete-melt condition. The fact that the tensile strain induces the mobility enhancement has also been confirmed by TCAD device simulations. Furthermore, simulation of the H_{21} parameter of strained n-channel SG-TFTs fabricated by the μ-Czochralski process with W_{eq} = 500 μm, L = 1.5 μm and t_{ox} = 30 nm has shown that a transit frequency f_T as high as 100 GHz is consistently obtained.

Chapter 7

Conclusions and recommendations

7.1 Conclusions

This thesis has focused on three main aspects of SG-TFTs fabricated by the μ-Czochralski process: firstly, the development of a SPICE model for DC, RF, and transient simulations; secondly, reliability analysis of devices under bias stress, alongside the design and fabrication of reliable high-voltage backplane devices for AM-QRLPD E-Paper; and thirdly, enhancement of the mobility of SG-TFTs fabricated by the μ-Czochralski process either by using Ge instead of Si for the active layer or by straining the Si layer with the aid of excimer laser radiation. The main conclusions are as follows:

- The compact physical model of SG-TFTs fabricated by the μ-Czochralski process developed for the purposes of SPICE simulations is based on the BSIMSOI model, with modification of the mobility model to take the presence of CSL-GBs in the channel into account. The measured DC characteristics of the devices and their dependency on different excimer laser energy densities during crystallization of the Si show good agreement with the simulation results. It has further been demonstrated that the addition of a distributed network to the intrinsic model yields better agreement between the measured and simulated values of the Y_{11} parameter than that obtained with the first-order approximation included in BSIMSOI, because of the lossy SG-TFT channel. Finally, an NQS model taking the channel charge relaxation time into account has been incorporated in the model to account for the transient behavior of SG-

TFTs fabricated at different excimer laser energy densities.

- Reliability analysis of n-channel SG-TFTs has shown that two basic degradation mechanisms occur when the SG-TFTs are under bias stress. Under linear bias stress conditions ($V_{DS} < V_{GS}$ - V_{th}), the main type of degradation observed is an increase in subthreshold slope S and mid-gap voltage V_{mg} due to the generation of deep states near the Si/SiO_2 interface and the injection of electrons in the gate oxide. When the SG-TFT is under strong saturation bias stress ($V_{DS} \gg V_{GS}$ - V_{th}), leading to what is known as the drain avalanche hot carrier (DAHC) effect, the main degradation phenomena occurring are reduction in mobility and a drop in the mid-gap voltage V_{mg} due to the generation of tail states near the drain region and the injection of holes into the gate oxide. The parameters required for a TCAD degradation model have also been extracted as a basis for prediction of the degradation phenomena observed in SG-TFTs under bias stress. After a DOS distribution has been extracted from the measured transfer characteristics before stress, the degradation effects to be found in SG-TFTs after bias stress are predicted by TCAD degradation simulation using the extracted parameters.

- Reliability analysis has provided the insight required for the development of SG-TFTs operating at high voltages. It has been shown in this connection that n- and p-channel SG-TFTs fabricated by the μ-Czochralski process can successfully operate at a supply voltage of 70 V, with p-channel HV-SGTFTs exhibiting better performance than their n-channel counterparts. The p-channel devices have a higher drive current and on/off current ratio because the boron implantation used for their LDD region leads to a deeper junction and hence a lower resistance than the arsenic implanted at the same dosage and energy in n-channel SG-TFTs. This means that the p-channel devices are not exposed to high impact ionization, leading to performance degradation associated with the kink effect, because the hole impact ionization factor is lower than that for electrons. As a result, trasmission gates developed with n- and p-channel HV-SGTFTs can achieve a propagation delay as low as 0.7 msec with load capacitances of around 100 pF. This yields the prospect of AM-QRLPD pixels made on this basis that are as fast as hundred nsec.

Although SG-TFTs fabricated by the μ-Czochralski process have already reached a performance as high as that of SOI-like devices, the investigations

described in this thesis reveal the possibility of enhancing the mobility of such devices yet further, either by replacing the Si active layer in the SG-TFTs by Ge or by fabricating strained single grain Si.

- Germanium grains up to 8 μm in diameter have been successfully obtained at predetermined positions by the μ-Czochralski process, even using Ge sputtering temperatures as low as 100 °C. EBSD inspection shows that random grain boundaries are not present in the grains but only at the edges where the grains collide. This opens the possibility of building TFTs inside the single Ge grains. Promising results have been achieved with p-channel Ge SG-TFTs including a hole mobility of 800 cm^2/Vs - around four times higher than that measured in SOI-TFTs. This result confirms the good quality of single Ge grain. The main obstacle to the production of state-of-art Ge MOSFETs remains the Fermi-level pinning effect that leads to high leakage currents in p-channel devices and impedes electron inversion in n-channel devices. However, a pseudo-TFT fabricated by a μ-Czochralski process using an Al_2O_3 grain filter shows a leakage current that remains consistently low as the drain voltage increases in p-channel devices and successful electron inversion layer with a satisfactory measured drain current in n-channel devices.

- High performance n- and p-channel strained single-grain silicon TFTs have been successfully obtained by the μ-Czochralski process at low process temperatures. Such SG-TFTs can achieve electron and hole field-effect mobilities that exceed those of SOI-TFTs by a factor of up to 1.6 under complete-melt conditions. This enhancement is due to the low DOS of CSL-GBs present in the channel and the low D_{it} at the Si/SiO_2 interface, the low roughness of the silicon surface and the high tensile strain induced by excimer laser irradiation during Si crystallization. The fact that tensile strain can induce mobility enhancement has also been confirmed by TCAD simulation. It has further been shown that the predicted transit frequency f_T of strained SG-TFTs with 30 nm gate oxide thickness, channel width 500 μm and channel length 1.5 μm fabricated by the μ-Czochralski process is an impressive 100 GHz.

7.2 Recommendations for future work

On this basis of the investigations described in this thesis and the knowledge gained during the past four years, I would like to make the following recommendations for future research.

- In view of the interest in SG-TFTs fabricated by the μ-Czochralski process for high-speed digital and RF applications, it would be desirable to develop a unified NQS model for transient and RF simulations capable of dealing with both large and small signals. Since the study of such devices operating at high frequencies also requires noise simulation, there is a need to modify the SPICE model of SG-TFTs so are to take noise effects into account.

- Scaling technology is also essential for the development of deep submicron SG-TFTs for very high-frequency digital and RF applications.

- Physical model of the recovery effect needs to be developed to simulate SG-TFT devices subject to a negative gate bias stress, which leads to annihilation of the traps responsible for degradation.

- It would be desirable to investigate the effectiveness of lightly doped drains and sources in both n- and p-channel SG-TFTs fabricated by the μ-Czochralski process as a means of increasing the lifetime of such devices.

- In view of the growing interest in Ge transistor devices, including the CMOS configuration of such devices, there is a need to develop a reliable fabrication process for the production of n- and p-channel Ge SG-TFTs. As explained in this thesis, one promising way of achieving this is to use Al_2O_3 as gate insulator at rear- and front-interfaces.

Appendix A

Flow chart of SG-TFTs fabricated by the μ-Czochralski process

Main steps in fabrication of SG-TFTs by the μ-Czochralski process:

- **Substrate:** anything
- **Oxidation:** deposition of 750 nm oxide film
- **Masking:** masking of hole 1 μm in diameter for grain filter
- **Etching of oxide:** with plasma oxide etchant
- **Oxide deposition:** 870 nm PECVD TEOS oxide
- **Deposition of a-Si:** LPCVD 250 nm thick
- **Channel implantation:** Boron E = 10 KeV, Dose = 2.5x10^{11} cm^{-2}
- **Crystallization:** Excimer laser (λ = 308 nm, pulse duration = 20 ns) E = 900 - 1200 mJ/cm^2
- **Masking:** masking of active island in grain filter
- **RIE etching of poly-Si:** with plasma poly-Si etchant
- **Dip etching:** 0.55 % HF for 4 minutes
- **Gate oxide deposition:** PECVD TEOS oxide

- **Gate metal:** sputtering of 600 nm Al/Si thick
- **Masking:** gate masking
- **Aluminum etching:** with plasma Al etchant
- **RIE etching of oxide:** with plasma oxide etchant
- **Masking:** p-channel and n-channel implantation mask
- **Source and drain implantation:** Boron ions E = 20 KeV and phosphorus ions E = 30 KeV and Dose = 1x10^{16} cm^{-1}; care should be taken to ensure proper masking
- **Activation of dopants:** Excimer laser annealing E = 300 mJ/cm^2
- **Oxide deposition:** 800 nm PECVD TEOS oxide
- **Masking:** source and drain contact opening mask
- **Etching of oxide:** plasma oxide etchant for source and drain contact opening
- **Dip etching:** 0.55 % HF for 2 minutes
- **Metalization:** Sputtering of 1.2 μm Al/Si thickn
- **Masking:** for metal contact pad
- **Aluminum etching:** plasma Al etchant for contact patterning
- **Alloying:** Annealing at 400 °Cin fuming gas

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Explanatory list of abbreviations

3D-IC = three-dimensional integrated circuit
A/D = analog/digital
a-Ge = amorphous germanium
ALD = atomic layer deposition
AM = active matrix
AM-LCD = active-matrix liquid-crystal display
AM-OLED = active-matrix organic light-emitting diode display
AM-QRLDP = active-matrix quick-response liquid-powder display
a-Si = amorphous silicon
a-Si:H = hydrogenated amorphous silicon
AFM = atomic force microscopy
BHF = buffered hydrofluoric acid
BJT = bipolar junction transistor
BSIM = Berkeley short-channel IGFET model
BSIMSOI = Berkeley short-channel IGFET model of SOI MOSFET (see SOI and MOSFET)
CLC = CW-laser lateral crystallization
CLM = channel length modulation
CMOS = complementary metal-oxide-semiconductor
CNL = charge neutrality level
c-Si = crystalline silicon
CSL-GB = coincident site lattice grain boundary
CV = capacitance/voltage
D/A = digital/analog
DAC = digital-to-analog converter
DAHC = drain avalanche hot carrier
DC = direct current
DIBL = drain-induced barrier lowering

DIMES = Delft Institute of Microsystems and Nanoelectronics
DOS = density of states
DRAM = dynamic random access memory
EBSD = electron back-scattering diffraction
EDX = energy dispersive X-ray
FWHM = full width at half maximum
GB = grain boundary
GF = grain filter
HDD = highly doped drain
HV = high voltage
ICP-ECVD = inductively coupled plasma enhanced chemical vapor deposition
LDD = lightly doped drain
LPCVD = low-pressure chemical vapor deposition
LV = low voltage
LV-SGTFT = single-grain silicon thin-film transistor operating at a low voltage
MOSFET = metal-oxide-semiconductor field-effect transistor
μ-Czochralski process = **micro-Czochralski** process; a modification of the Czochralski process for the production of single silicon crystals, designed to obtain very small single silicon crystals in individual grains
NQS = non-quasi-static
OLED = organic light-emitting diode
PECVD = plasma-enhanced chemical vapor deposition
PIN photodiode = A photodiode with an intrinsic (undoped) region sandwiched between a p-doped and an n-doped region
PM = passive matrix
PMELA = phase-modulated excimer laser annealing
poly-Si = polysilicon
QR-LDP = quick-response liquid-powder display
QSA = quasi-static assumption
RIE = reactive ion etching
RMS = root mean square
SEM = scanning electron microscope
SG-TFT = single-grain silicon thin-film transistor
SLS = sequential lateral solidification
SoC = system on a chip
SOI = silicon-on-insulator
S-parameter = scattering parameter
SPICE = Software Process Improvement and Capability dEtermination

SRAM = static random access memory
TCAD = technology computer-aided design
TCO = transparent conductive oxide
TEOS = tetraethylorthosilicate
TFT = thin-film transistor

Summary

Single grain TFTs for high speed flexible electronics

by Alessandro Baiano

Flexible electronics that require technologies to be fabricated on unconventional substrates are impossible to achieve with the conventional IC microelectronics, mainly because of the high temperature of the production process and the high costs of large-area production.

Thin-film electronics, on the other hand, permit solutions that would not be economically viable or even possible with commercial IC microelectronics.

Thin-film electronics have evolved enormously during the past few decades. Significant advantages are achieved by basing this technology on single-grain silicon thin-film transistor (SG-TFTs) built inside a location-controlled grain crystallized by the μ-Czochralski process. These SG-TFTs offer a performance as high as that of SOI MOSFET devices, despite the low process temperature. The basic details of the process used to fabricate this type of technology are presented in **Chapter 1** of this thesis, together with the potential applications and advantages of this technology over other TFT technologies, and this discussion is placed briefly in the context of the history of TFT technologies.

Once a new technology has been created, a compact model must be developed that accurately describes the physical behavior of the device for purposes of SPICE simulation. None of the commercially available SPICE models was suitable for use on SG-TFTs fabricated by the μ-Czochralski process. The approach used to develop a SPICE model that can be used for SG-TFTs fabricated by the μ-Czochralski process is described in **Chapter 2**. The new model is derived from the physically based SOI MOSFET (BSIMSOI) SPICE model, suitably modified to take the thermionic emission effect across the coincidence site lattice grain boundaries (CSL-GBs) into account for more ac-

curate modeling of carrier mobility. Furthermore, a distributed network that takes into account the high-order effect of the lossy SG-TFT channel at high operating frequencies is included in the intrinsic RF BSIMSOI model to ensure better matching of the SPICE RF simulations with the experimental results. The modified physical model is implemented in a SPICE-like simulator with the aid of the behavioral language Verilog-A.

Study of degradation phenomena in SG-TFTs fabricated by the μ-Czochralski process is also of fundamental importance for the reliability of such devices under bias stress. A method for degradation analysis of SG-TFTs under bias stress, which provides a basis for 2D modeling by a TCAD simulator, has therefore been developed as part of the present study. It is described in **Chapter 3**. This analysis shows that application of a linear bias stress to the device leads to generation of deep acceptor-like states near the Si/SiO_2 interface and injection of electrons into the oxide layer, and thus to enhancement of the subthreshold slope S and mid-gap voltage V_{mg}. On the other hand, application of a strong saturation bias stress to the device leads to the generation of acceptor-like tail states near the drain region and injection of hot holes into the oxide, and thus to a drop in mobility and mid-gap voltage V_{mg}. Finally, the degradation of the transfer characteristic of SG-TFTs fabricated by the μ-Czochralski process under the two different bias stress conditions can be correctly predicted by 2D TCAD simulation with the aid of the above analysis.

The study of degradation phenomena also aims to improve our understanding of how SG-TFTs fabricated by the μ-Czochralski process operate at high voltages opening the way to many new applications such as electronic paper (E-Paper) with an active-matrix quick-response liquid-powder display (AM-QRLPD) requiring backplane transistors operating at a supply voltage of 70 V. After giving an overview of the quick-response liquid-powder display (QR-LPD) frontplane, **Chapter 4** presents the results of experiments on reliable n- and p-channel SG-TFTs fabricated by the μ-Czochralski process operating at high voltages such as 70 V (HV-SGTFTs) and describes the fabrication process combined with the low voltage SG-TFT (LV-SGTFT) technology needed for the driver circuits. The measured propagation delay of CMOS HV-SGTFT transmission gates has been found to be as low as 0.7 msec with a load capacitance of about 200 pF. On this basis, it is predicted that the propagation delay of the finished AM-QRLPD pixel could be no more than 100 ns.

SG-TFTs fabricated by the μ-Czochralski process have already reached a performance as high as that of SOI-like devices, but the investigations described in this thesis reveal two possibilities of enhancing the mobility of such devices yet further. The first way is dealt with in **Chapter 5**. This involves

replacing the Si active layer in the SG-TFTs by germanium (Ge) sputtered at low temperatures. It is found that high quality 2D location-controlled single Ge grains with a diameter of 8 μm can be successfully obtained by the μ-Czochralski process with Ge sputtered at different temperature down to 100 °C. This provides a basis for the fabrication of single grain Ge TFTs by the μ-Czochralski process in which the hole field-effect mobility is enhanced to 800 cm^2/Vs, around four times that measured in SOI-TFTs. It is furthermore shown that the Fermi-level pinning effect occurring at the two Ge-oxide interfaces in p-channel Ge SG-TFTs and leading to high leakage currents can be drastically reduced using Al_2O_3 deposited by atomic layer deposition (ALD) as buried oxide. It is also shown that the use of Al_2O_3 as gate oxide is a promising means of improving the Fermi-level pinning effect in n-channel Ge SG-TFTs and thus impeding the formation of the electron inversion layer in these devices.

The second way of improving the perfomance of these SG-TFTs is discussed in **Chapter 6**. This takes advantage of the mobility enhancement obtained by subjecting single Si grains to tensile strain induced by excimer laser irradiation under complete-melt conditions. Previous workers have established that polysilicon TFTs possess an intrinsic tensile strain, but that the effect of this strain in increasing the electron and hole mobility of these TFTs was canceled out by a combination of the presence of random grain boundaries in the channel, the high density of trap states at the Si/SiO_2 interface, and the elevated roughness of the Si surface. The μ-Czochralski process, on the other hand, leads to a location-controlled single grain having only CSL-GBs inside the grain which has a low density of states and hence offers negligible impedance to carrier mobility. The use of inductively coupled plasma enhanced chemical vapor deposition (ICP-ECVD) for the gate oxide and the low roughness of the silicon grain surface also reduce the impedance factor that would limit the mobility enhancement obtained by the high tensile strain (1.20 GPa) induced by excimer laser irradiation during Si crystallization under the complete-melt conditions. The measured electron and hole field-effect mobilities have been found to be up to 1.6 times higher than those of SOI-TFTs. The transit frequency f_T of the strained SG-TFTs with 30 nm gate oxide thickness, channel width 500 μm and channel length 1.5 μm fabricated by the μ-Czochralski process is predicted to be 100 GHz.

Finally, **Chapter 7** presents the conclusions of this thesis. The main conclusion is that SG-TFTs fabricated by the μ-Czochralski process makes it possible to develop an E-Paper and high-performance transistors for analog, RF, and digital circuits.

Samenvatting

Enkel-korrel TFTs voor snelle flexibele elektronica

Door Alessandro Baiano

Het is onmogelijk om flexibele elektronica, waarvoor technieken voor de fabricatie op onconventionele substraten nodig zijn, te realiseren met de conventionele IC micro-elektronica. Vooral vanwege de hoge temperaturen van het productie proces en de hoge kosten voor de fabricatie op grote oppervlakken.

Dunne film elektronica, daarentegen, laat oplossingen toe die met commerciële IC micro-elektronica niet economisch haalbaar of zelfs totaal niet mogelijk zijn.

Dunne film elektronica is enorm geëvolueerd tijdens de afgelopen paar decennia. Significante voordelen zijn gerealiseerd door deze techniek te baseren op enkel-korrel silicium dunne film transistoren (SG-TFTs) gebouwd in een locatie gecontroleerde korrel gekristalliseerd door het μ-Czochralski proces. Deze SG-TFTs bieden prestaties zo goed als die van SOI MOSFET, ondanks de lage proces temperatuur. De basisgegevens van het proces gebruikt voor de fabricatie van deze technologie worden gepresenteerd in **Hoofdstuk 1** van dit proefschrift, samen met de mogelijke toepassingen en voordelen van deze techniek over andere TFT technieken. Deze discussie wordt kort in de context van de geschiedenis van TFT technieken gehouden.

Zodra een nieuwe techniek is gemaakt moet er een compact model worden ontwikkeld waarmee accuraat de fysische werking van de transistor wordt beschreven voor het gebruik in SPICE simulaties. Geen van de beschikbare commerciële SPICE modellen was geschikt om gebruikt te worden met SG-TFTs gefabriceerd met het μ-Czochralski proces. De gebruikte benadering voor de ontwikkeling van een SPICE model dat gebruikt kan worden voor SG-TFTs gefabriceerd met het μ-Czochralski proces wordt behandeld in **Hoofd-**

stuk 2. Het nieuwe model is afgeleid van het fysisch gebaseerde SOI MOSFET (BSIMSOI) SPICE model, voldoende aangepast om het thermionische emissie effect over de *coincidence site lattice* korrelgrens (CSL-GBs) mee te nemen voor een meer accurate modellering van de ladingsdrager mobiliteit. Bovendien is een gedistribueerd netwerk dat de hogere-orde effecten van het lekkende SG-TFT kanaal op hoge operationele frequenties meeneemt toegevoegd aan het intrinsieke RF BSIMSOI model om een betere overeenkomst tussen de SPICE RF simulaties en de experimentele resultaten te verzekeren. Dit gemodificeerde fysische model is geïmplementeerd in een SPICE-achtige simulator met behulp van de gedragstaal Verilog-A.

De bestudering van degradatie fenomenen in SG-TFTs gefabriceerd door het μ-Czochralski proces is ook van fundamenteel belang voor de betrouwbaarheid van zulke transistoren onder bias stress. Een methode voor degradatie analyse van SG-TFTs onder bias stress, die een basis legt voor 2D modellering door een TCAD simulator, is daarom ontwikkeld als onderdeel van dit onderzoek. Deze wordt beschreven in **Hoofdstuk 3**. Deze analyse toont aan dat de plaatsing van een lineaire bias stress over de transistor leidt tot de generatie van diepe acceptor-achtige toestanden nabij de Si/SiO_2 grensvlak en injectie van elektronen in de oxide laag, en dus tot de verbetering van de subdrempel helling S en mid-gap spanning V_{mg}. Tenslotte kan de degradatie van de overdracht karakteristieken van de SG-TFTs gefabriceerd door het μ-Czochralski proces onder twee verschillende bias stress condities correct worden voorspeld door 2D TCAD simulatie met behulp van bovenstaande analyse.

Het onderzoek naar de degradatie verschijnselen richt zich ook op de verbetering van ons begrip hoe SG-TFTs gefabriceerd door het μ-Czochralski proces werken op hoge spanningen. Vele nieuwe applicaties worden hierdoor mogelijk, zoals elektronisch papier (E-Paper) met een actieve matrix snelle respons vloeistofpoeder scherm (AM-QRLPD). Deze applicatie heeft achterplaat (backplane) transistoren werkend op een voedingspanning van 70 V nodig. Nadat een overzicht is gegeven van het snelle respons vloeistofpoeder schermen (QR-LPD) voorvlak, presenteert **Hoofdstuk 4** de resultaten van experimenten aan betrouwbare n- en p-kanaal SG-TFTs gefabriceerd door het μ-Czochralski proces werkend op hoge spanningen zoals 70 V (HV-SGTFTs) en beschrijft het fabricatie proces gecombineerd met de lage spanning SF-TFTs (LV-SGTFTs) technologie benodigd voor de aanstuur elektronica. De gemeten propagatie vertraging van CMOS HV-SGTFT transmissie poorten is zo laag als 0.7 msec met een belastingscapaciteit van ongeveer 200 pF. Uit deze resultaten wordt voorspeld dat de propagatie vertraging van complete AM-QRLPD pixels niet meer dan 100 ns kan zijn.

SG-TFTs gefabriceerd door het μ-Czochralski proces hebben al prestaties bereikt zo hoog als die van SOI-achtige transistoren, maar het onderzoek beschreven in dit proefschrift onthult twee mogelijkheden om de mobiliteit van zulke transistoren verder te verbeteren. De eerste methode wordt behandeld in **Hoofdstuk 5**. Dit behelst het vervangen van de Si actieve laag in de SG-TFTs door germanium (Ge) gesputterd op lage temperaturen. Het blijkt dat 2D locatie gecontroleerde enkel- Ge-korrels van hoge kwaliteit met een diameter van 8 μm succesvol verkregen kunnen worden met het μ-Czochralski proces waarbij Ge gesputterd is op verschillende temperaturen tot 100 °C. Dit legt de basis voor de fabricatie van enkel-korrel-Ge TFTs door het μ-Czochralski proces waarbij de mobiliteit van de gaten is verbeterd tot 800 cm^2/Vs, rond vier keer van die gemeten in SOI-TFTs. Het is bovendien aangetoond dat het Fermi-niveau *pinning* effect dat plaatsvindt op de twee Ge-oxide grensvlakken in p-kanaal Ge SG TFTs en dat leidt tot hoge lekstromen drastisch kan worden verminderd als Al_2O_3, gedeponeerd door middel van atoomlaag depositie (ALD), als begraven oxide wordt gebruikt. Het is ook aangetoond dat het gebruik van Al_2O_3 als gate oxide een veelbelovende methode voor de verbetering van het Fermi-niveau *pinning* effect in n-kanaal Ge SG-TFTs is en dus de vorming van een elektronen inversie laag belemmert in deze transistoren.

De tweede methode om de prestaties van de SG-TFTs te verbeteren is behandeld in **Hoofdstuk 6**. Deze maakt gebruik van de mobiliteit verbetering verkregen door enkel-Si-korrels bloot te stellen aan trekspanning geïnduceerd door excimer laser bestraling onder volledige smelt voorwaarden. Vorige onderzoekers hebben vastgesteld dat polysilicium TFTs een intrinsieke trekspanning bezitten, maar dat het effect van deze spanning in het verhogen van de elektronen en gaten mobiliteit in deze TFTs wordt geneutraliseerd door een combinatie van de aanwezigheid van willekeurige korrelgrenzen in het kanaal, de hoge dichtheid van *traps* op het Si/SiO_2 grensvlak en de verhoogde ruwheid van het Si oppervlak. Daarentegen leidt het μ-Czochralski proces tot een locatiegecontroleerde enkel-korrel met slechts CSL-GBs in de korrel die een lage toestanddichtheid hebben en dus een verwaarloosbare belemmering voor ladingsdragers bieden. Het gebruik van inductief gekoppelde plasma versterkte chemische opdamping (ICP-PECVD) voor het gate oxide, en de lage ruwheid van het silicium korrel oppervlak verlagen ook deze belemmering. De belemmering limiteer de mobiliteitversterking, verkregen door de hoge trekspanning (1.20 GPa) geïnduceerd door excimer laser bestraling gedurende Si kristallisatie onder volledige smelt voorwaarden. De gemeten elektronen en gaten veldeffect mobiliteiten blijken 1.6 keer hoger te zijn dan die van SOI-TFTs. De voorspelde doorvoer frequentie f_T van de gespannen SG-TFTs met een gate oxide dikte van 30 nm, kanaalbreedte van 500 μm en een kanaallengte

van 1.5 μm gefabriceerd door het μ-Czochralski proces is 100 GHz.

Tenslotte presenteert **Hoofdstuk 7** de conclusies van dit proefschrift. De belangrijkste conclusie is dat SG-TFTs gefabriceerd door het μ-Czochralski proces het mogelijk maken om E-paper en hoogwaardige transistoren voor analoge, RF en digitale circuits te ontwikkelen.

List of publications

Journal papers

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About the author

Alessandro Baiano was born in Napoli, Italy, in 1979. He received his *Laurea* degree, cum laude, in electronics engineering from the University of Naples Federico II, Italy, in 2005, after completing his *Laurea* thesis within the Department of Microelectronics and Information Technology of the Royal Institute of Technology, Stockholm, Sweden, on analysis of deep submicron fully depleted Silicon-on-Insulator MOSFETs.

In October 2005, he joined the Faculty of Electrical Engineering, Mathematics and Computer Science, Delft University of Technology, Delft, the Netherlands, where he worked towards the Ph.D. degree within the Laboratory of Electronic Components, Technology and Materials (ECTM) of Delft Institute of Microsystems and Nanoelectronics (DIMES).

In April 2009, he received an invited presentation for his research work entitled "High Performance n- and p-channel Strained Single Grain Silicon TFTs using Excimer Laser" to the *MRS* conference.

His research interests include fabrication, characterization and modeling of high-performance single-grain thin-film transistors and its circuit applications.