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Energy-Efficient Self-Timed Zero-Crossing-Based Incremental $\Delta\Sigma$ ADC

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Delft University of Technology

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Energy-Efficient Self-Timed Zero-Crossing-Based Incremental $\Delta\Sigma$ ADC

Master of Science Thesis

For the degree of Master of Science in Microelectronics at Delft University of Technology

Chao Chen

November 29, 2012

Faculty of Electrical Engineering, Mathematics and Computer Science · Delft University of Technology

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Delft University of Technology
Department of
Electrical Engineering

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Energy-Efficient Self-Timed Zero-Crossing-Based Incremental $\Delta\Sigma$ ADC

by

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Master of Science Microelectronics

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Abstract

This thesis presents the world's first clock-free self-timed incremental $\Delta\Sigma$ ADC. Unlike conventional $\Delta\Sigma$ ADCs, it does not require a dedicated clock signal, thus saving energy and reducing system complexity. It is particularly suited for use in energy-constrained sensor applications in which conversions are triggered by infrequent and possibly irregular external events. As it autonomously powers down upon completion of a conversion, it can adapt to a wide range of conversion rates in an energy-efficient way. Moreover, its conversion time automatically adjusts to PVT variations, eliminating the need to design for worst-case conditions, as typically required in synchronous designs.

In contrast to asynchronous $\Delta\Sigma$ ADCs, which also operate without a clock, our self-timed $\Delta\Sigma$ ADC employs a discrete-time switched-capacitor loop filter and a clocked comparator, albeit self-timed, and therefore maintains the same noise-shaping characteristics as conventional, synchronous incremental $\Delta\Sigma$ ADCs. Zero-crossing based (ZCB) circuits are employed to implement the loop-filter's integrators, in which the completion of charge-transfer process can be detected by a zero-crossing detector (ZCD). An inverter-based ZCD is introduced to further improve the energy-efficiency of ZCB designs.

A prototype ADC has been implemented in NXP's 1P6M 0.16μm CMOS process to prove the concept. It includes the whole $\Delta\Sigma$ modulator, as well as the timing-critical part of the asynchronous digital state machine. Measurement results show that it can achieve 14.8-bit resolution and 14-bit linearity, with 500 incremental cycles. While operating, the whole chip consumes less than 20μA from a 1V supply.

Keywords: Incremental $\Delta\Sigma$ ADC, Self-timed, Zero-crossing-based circuits, Energy-efficient, Low-power

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Chapter 1

Introduction

In instrumentation and measurement (I&M), analog-to-digital converter (ADC) are normally used in converting low-bandwidth signals with very high absolute accuracy and linearity. The incremental $\Delta\Sigma$ ADC, which can be treated as a classical $\Delta\Sigma$ ADC running in transient mode, was found to be a well-suited structure for I&M applications in the last decade [11][12]. Most reported incremental $\Delta\Sigma$ ADCs are designed to operate with a dedicated constantly-running oversampled clock. That is, however, a significant overhead in some energy-constrained sensing applications, such as temperature and humidity sensors on RFID tags. This thesis proposes the first clock-free self-timed implementation of incremental $\Delta\Sigma$ ADC to address this problem. Some special circuit techniques are introduced to further improve the ADC's energy-efficiency while maintaining its performance. A prototype has been implemented to prove the concept and demonstrate the effectiveness of these techniques.

At the beginning of this introductory chapter, the motivation of this work are briefly described, as well as its relation to prior work. That is followed by a short discussion on the design challenge and the corresponding solution, as well as a system-level overview of the proposed self-timed ADC. Furthermore, the objective of this work is introduced. Finally, the organization of the thesis is given.

1-1 Motivation

The conventional implementation of discrete-time $\Delta\Sigma$ modulators, which is usually switched-capacitor (SC) based, relies on external synchronous clocks to divide the time-axis into different phases. The clock events serve as time bases that determine the order of charge sampling and transfer in each stage of the modulator. All the transient processes in the analog circuitry should have settled before the next clock cycle starts; in other words, the circuitry has to be designed in order to ensure settling within the clock cycle, as will be shown in the following example.

Consider a simple first-order $\Delta\Sigma$ modulator with conventional OTA-based SC integrator, as shown in Figure 1-1. In this circuit, all the switches are driven by a pair of complementary

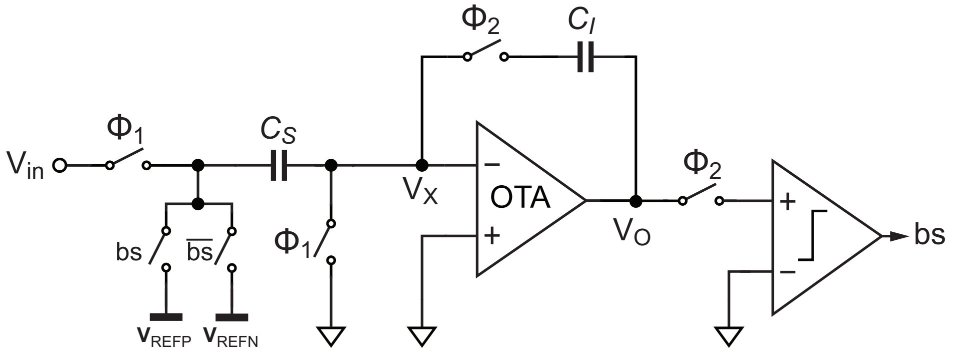

Figure 1-1: First-order ΔΣ modulator with OTA-based switched-capacitor integrator

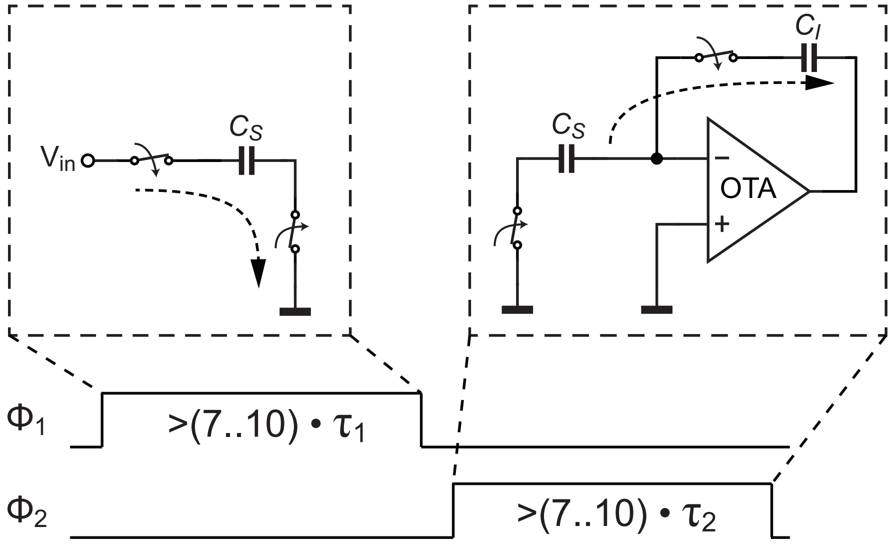

Figure 1-2: Timing diagram and circuit operation of first-order ΔΣ modulator

phase clocks, Φ_1 and Φ_2. Figure 1-2 illustrates the timing diagram and operation sequence.

In phase Φ_1, the input voltage is sampled on the capacitor C_S. To obtain the desired settling accuracy, the duration time of Φ_1 should not be shorter than N times of the exponential settling time constant τ_1:

$$T_{\Phi 1} > N\tau_1, \quad \tau_1 = 2r_{ON}C_S \tag{1-1}$$

The parameter r_{ON} represents the on-resistance of series switches, while the value of N varies from 7 to 10 for settling accuracy range from 0.1% to 0.005%.

In phase Φ_2, the charge sampled on C_S in Φ_1 is integrated on the capacitor C_I. Similarly, the minimum duration time of Φ_2 is given by:[1]

$$T_{\Phi 2} > N\tau_2, \quad \tau_2 \simeq \frac{C_S}{g_m} \tag{1-2}$$

where g_m is the transconductance of the OTA and N ranges from 7 to 10 as well.

---

[1] In this brief discussion the load capacitor at the integrator output is neglected for convenience.

Expressions (1-1) and (1-2) reveal the linking between clock periods and the speed constraint of analog circuits.

It is not difficult to explain the popularity of synchronous timing methodology in the design of $\Delta\Sigma$ ADCs. The dedicated clocks provide a deterministic approach to control the events that take place in both analog and digital circuits, as well as ensuring the uniform and well-defined sampling of the input signal. From the design perspective, the clock period can be simply selected in line with the worst speed condition to ensure the settling accuracy. Therefore, the synchronous approach is widely accepted in a broad range of applications. Unfortunately, it also brings several problems, especially when the energy-efficiency is of concern:

- ***Design redundancy***: As ADCs are normally designed to operate with a relatively wide range of environmental conditions, such as process, supply voltage and temperature (PVT), the impact of physical constraints on the circuit bandwidth should be fully considered. This usually leads to "over-design" since the synchronous clock period should be sufficiently long to satisfy the settling accuracy requirement of the worst case. For example, the on-resistance of switches $\mathrm{r_{ON}}$ and transconductance $\mathrm{g_m}$ in expressions (1-1) and (1-2) both vary with the process corners. This fact implies that the circuit should be assumed to operate with the slowest corner in the design phase, which however has very low probability in reality.

  Obviously over-design has negative effects on the energy-efficiency. On the one hand, a larger transconductance ($\mathrm{g_m}$) and hence more current are required to meet the specific frequency target; on the other hand, when the current budget is constrained, the OTAs should be kept operating in the active mode for longer, which increases the energy-dissipation as well.

- ***System redundancy***: The external clock is normally generated using on/off chip oscillators or phase-locked loops (PLLs). These auxiliary timing circuits increase the system complexity; moreover, they consume power themselves. This is not energy-economical when the clock is only required for the ADC, for instance in wireless sensing and portable medical systems where only a small section of back-end digital processing circuits are locally implemented with the ADC.

- ***Time redundancy***: In energy-constrained sensor applications, the conversions are often triggered by infrequent and possibly irregular events, like the threshold-crossing of input signals. For input signals with relatively low activity, a continuously running clock-network in over-sampling systems will keep burning power even in the idle time, which is not energy-efficient either.

To address the above problems, the most straightforward idea is to eliminate all the external clocks. One possible approach is to get rid of the entire timing control logic and, instead, to perform the $\Delta\Sigma$ modulation in a fully analog fashion. A well-known clock-less system based on this principle is the **asynchronous $\Delta\Sigma$ modulator (ADSM)**. It has been extensively discussed in [13], [14] and [15], and employed in some applications where only analog processing is required. As shown in Figure 1-3, an ADSM converts an analog input signal *u(t)* into a continuous-time square-wave output signal *y(t)* via duty-cycle modulation. It is essentially a free-running self-oscillator based on inherent limit-cycles. No clocked sampling or digitization is performed in the modulation loop, and consequently no quantization noise is introduced in.

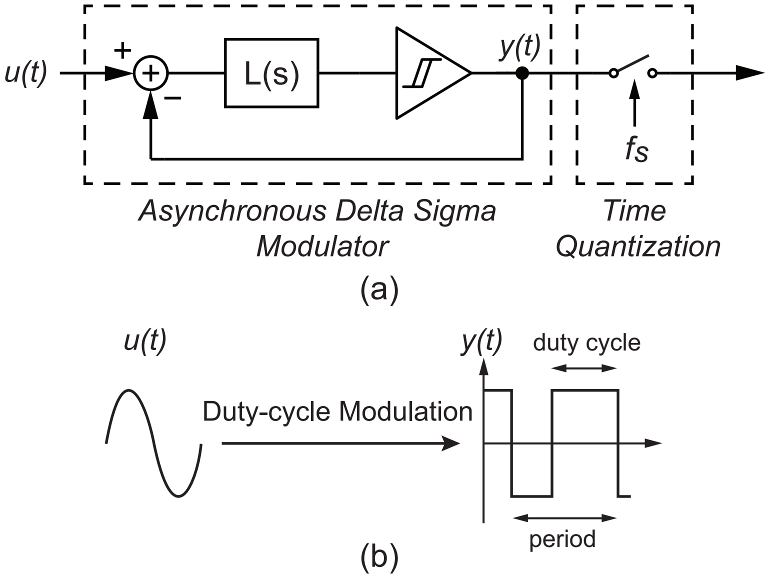

Figure 1-3: (a) Block diagram of asynchronous $\Delta\Sigma$ modulator with time quantization (b) Time-domain signal-processing diagram of duty-cycle modulation

However, when applied in analog-to-digital conversion, the fully analog nature of ADSM becomes its main drawback. To provide a multi-bit digital output, an external sampler [15] or a time-to-digital converter (TDC) [16] is still called for at the output of the modulator to perform quantization on the time axis. External reference clocks are demanded for this step, and therefore an ADSM-based ADC is not truly clock-less.

A more suitable technique for ADC implementation is to replace the external clocks with local timing control logics driven by internal events in the analog circuits. This technique can be referred to as the **Mixed-signal Self-timed approach**, succeeding to its counterpart in the digital design domain [17][18]. In this approach, the analog circuitry must be able to generate a completion signal to the local timing logic once the on-going process (e.g. amplification, integration, comparison, etc.) completes. After that, the timing logic proceeds to the next cycle and the analog circuitry changes its state. The mixed-signal nature of ADC calls for special collaborations (or “hand-shaking”) between the digital logic and the analog circuits, as indicated in Figure 1-4.

When compared with their synchronous counterparts, self-timed analog-to-digital converters show some appealing advantages:

- By removing the external clocks and the periphery circuits (e.g. oscillators and PLLs), the system and time redundancy problems can be avoided. The only expense is a small overhead on the timing control circuits which generate the local clocks and the completion signals.

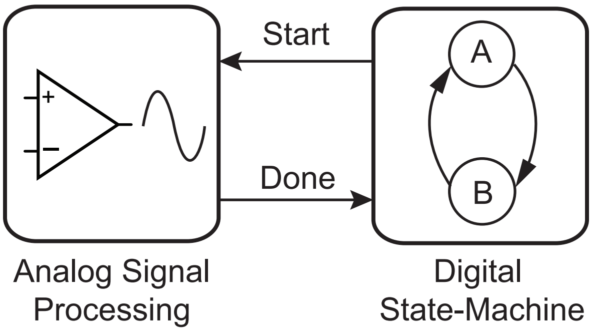

Figure 1-4: Principle of self-timed operation in mixed-signal circuits

- The generation of completion signal in analog circuitry takes the actual manufacturing and operating conditions into account. Thus, a self-timed converter can operate at the upper-limit speed adapting to the physical constraints such as process and temperature, which removes the “over-design” as well.

On the basis of the above discussions, we have reasons to believe that the self-timed methodology is particularly suited for analog-to-digital converters in energy-constrained sensing applications, especially the incremental ΔΣ ADCs. However, the implementation of self-timed ADCs is also associated with various challenges, as will be discussed in the next section.

1-2 Challenge and Solution

Up to now, to the author’s knowledge, the mixed-signal self-timed approach has only found its application in succesive-approxiamation (SA) ADC. Asynchronous SA-algorithm processing has been introduced in [19][20] to reduce the system-level power consumption. Its basic idea is to trigger the internal comparison from the most significant bit (MSB) to the least significant bit (LSB) one by one, as indicated in Figure 1-5. The comparator has a dual function: 1) performs the comparison between input signal and the DAC output; 2) generates a completion signal for the current bit and triggers the next one. In this way, the comparison sequence becomes self-driven and no over-sampled internal clocks is needed.

In conventional OTA-based discrete-time ΔΣ ADCs, however, the situation is a bit different. Due to the infinite approaching characteristic of an exponential settling process, there is no explicit “milestone” on the time-axis to indicate the completion of sampling or integration phases (Figure 1-6(a)). This feature prohibits the direct application of the self-timed methodology in ΔΣ ADCs.

This problem can be solved by changing the charge-transfer mechanism. Zero-crossing based (ZCB) circuits [21] [22], in which the OTAs are replaced with tailored comparators (or zero-crossing detectors, ZCD) and gated current sources (GCS), offers such an option. Unlike conventional OTA-based switched-capacitor circuits, ZCB designs utilize gated current sources to transfer the charge from the sampling capacitors to the integration capacitors. The charge-transfer process continues until the virtual-ground condition is detected by the ZCD (Figure 1-6(b)). The detected instant of the virtual ground condition can be used as a

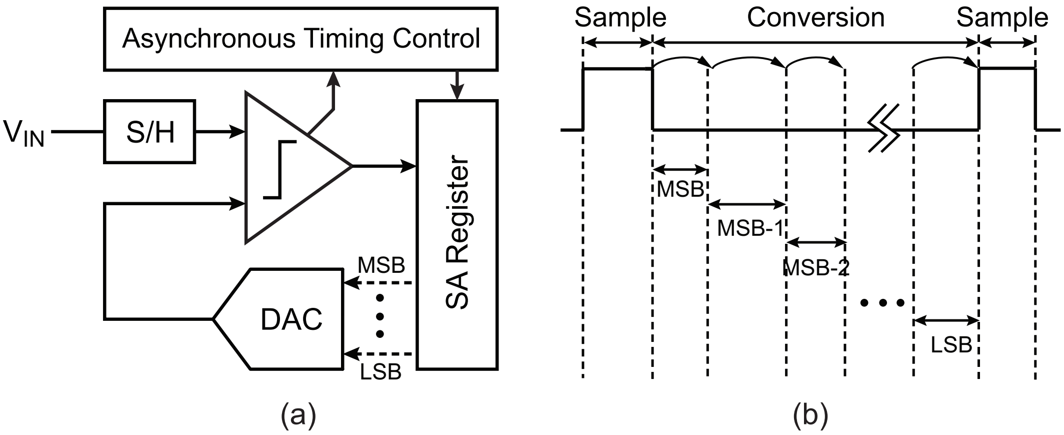

Figure 1-5: (a) Block diagram of Self-timed SAR ADC (b) Timing diagram of asynchronous SA-algorithm processing

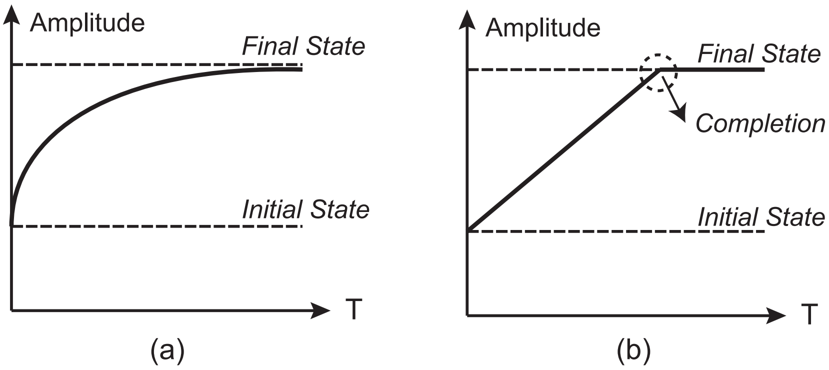

Figure 1-6: Charge-transfer mechanism: (a) Exponential settling (b) Current-source driven linear approaching with completion detection

completion signal marking the end of the current phase, which provides the possibility for self-timed operation.

The block diagram shown in Figure 1-7 turns this idea into practice. It consists of a second-order discrete-time $\Delta\Sigma$ modulator controlled by an asynchronous state machine. The modulator employs two zero-crossing based integrators and a clocked quantizer. Details of the modulator structure and other circuit implementations will be discussed in the following chapters.

The basic principle of the self-timed operation can be explained by the system-level timing diagram as illustrated in Figure 1-8. An external startup signal triggers one conversion, after which the state machine generates a pair of non-overlapping clock signals Φ_1 and Φ_2 that alternately switch the integrators between sampling and charge-transfer phases. Each zero-crossing based integrator generates a completion signal once it accomplishes the charge-transfer process. At that instant, the state machine proceeds to the next phase. Thus, the duration time of clock phases Φ_2 (state A) and Φ_1 (state B) is determined by the charge-transfer time in the first and second integrator, respectively. The same process repeats for a preset number of cycles (N). After that the integration capacitors are reset, and all circuitry

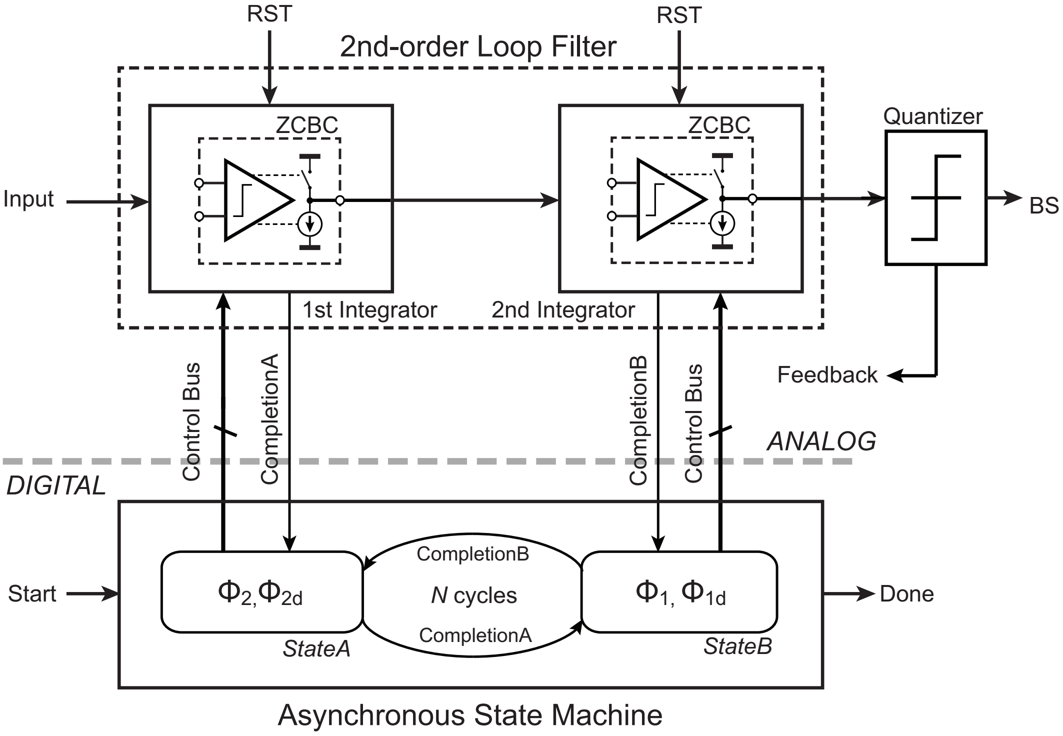
RST
RST
2nd-order Loop Filter
ZCBC
ZCBC
Quantizer
Input
BS
1st Integrator
2nd Integrator
Control Bus
CompletionA
CompletionB
Control Bus
Feedback
ANALOG
DIGITAL
Start
Φ_2, Φ_{2d}
CompletionB
N cycles
CompletionA
Φ_1, Φ_{1d}
Done
StateA
StateB
Asynchronous State Machine

Figure 1-7: Block diagram of a self-timed 2nd-order incremental ΔΣ ADC

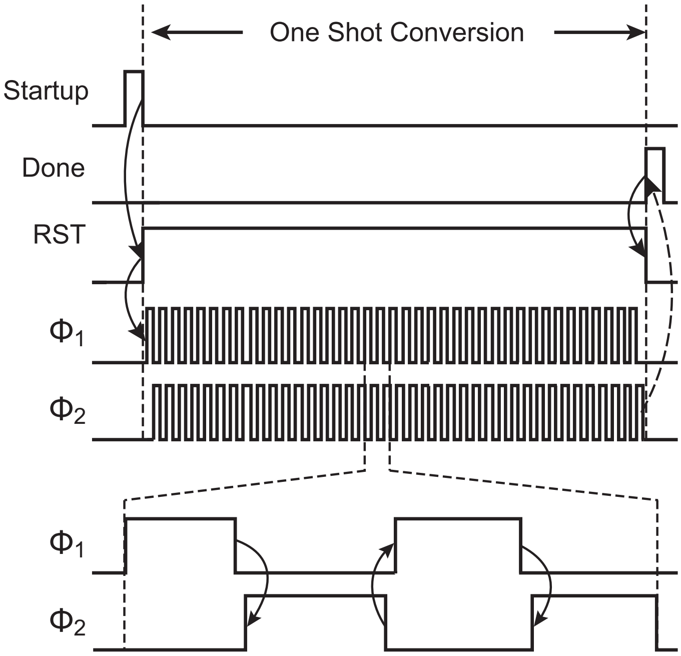
One Shot Conversion
Startup
Done
RST
Φ_1
Φ_2
Φ_1
Φ_2

Figure 1-8: System-level timing diagram of Self-timed operation

is powered down until the next conversion is requested.

1-3 Objectives

The aim of this thesis work is to implement the world's first purely self-timed incremental $\Delta\Sigma$ ADC based on zero-crossing technique. As stated in previous sections, the self-timed characteristic is expected to improve the energy-efficiency of incremental $\Delta\Sigma$ ADCs in energy-constrained sensing applications. In addition, some attractive properties of ZCB designs, such as the amenability to scaled CMOS technologies [21] , are also enjoyed by the proposed structure. Considering the inherent non-linearity problem of ZCB designs [22] [23][24] , special circuit techniques are called for to improve its linearity performance.

Table 1-1 lists the targeted specifications of the prototype self-timed ADC. The supply voltage is chosen at 1V to demonstrate the low-supply-voltage capability of the proposed structure. The effective number of bits (ENOB), which is an ADC quality measure for both resolution and linearity, is aimed at 13bit~14bit to meet the absolute accuracy and linearity requirements of common DC sensing applications.

Table 1-1: Design Targets of Prototype Incremental $\Delta\Sigma$ Self-timed ADC

Specification	Target
Technology	NXP 0.16μm 1P6M CMOS
Supply Voltage	1V
ENOB	13~14 bit
Resolution	>14 bit
Conversion Time	<1ms
Power Consumption	<20μW
Figure of Merit (FOM)†	<2pJ/conversion-step

† $\mathrm{FOM} = \dfrac{\mathrm{Power} \cdot \mathrm{T_{conv}}}{2^{\mathrm{ENOB}}}$

1-4 Thesis Organization

This thesis presents the basic principles and circuit implementations of a self-timed incremental $\Delta\Sigma$ ADC, which is apt for energy-constrained sensing applications. Apart from this introductory chapter, the rest of this thesis is divided into six chapters.

Chapter 2 discusses the basic operation principle of the zero-crossing based (ZCB) switched-capacitor integrator, which is the most critical block in the self-timed $\Delta\Sigma$ ADC. This chapter also provides a detailed analysis of the non-ideal effects in zero-crossing based circuits, including noise, offset and non-linearity. Some advanced circuit topologies for ZCB circuits are also introduced to improve the performance of the basic structure.

Chapter 3 and Chapter 4 contain the main innovations of this thesis to improve the energy-efficiency of incremental $\Delta\Sigma$ ADCs. Chapter 3 proposes a new class of zero-crossing detectors based on class-AB inverters, as well as discusses its advantages and limitations. An overview on the development of inverter-based analog circuitry is also given in this chapter.

Chapter 4 describes the complete design of the self-timed incremental $\Delta\Sigma$ ADC. The basic theory of incremental $\Delta\Sigma$ ADC is briefly reviewed, after which the design considerations on the second-order modulator structure are presented. The implementation of the fully-custom self-timed state machine is also covered in this chapter.

Chapter 5 describes the design details of the experimental prototype chip. It starts with a topology overview and introduces the transistor-level implementation of the sub-blocks one by one. Some design techniques for testability and the layout details are also included.

Chapter 6 contains the details of the measurement results. A brief introduction to the measurement methods and setups is also included.

Finally, Chapter 7 summaries the contributions of this thesis and discusses some performance limitations of the proposed structure. Furthermore, potential directions in future work are highlighted.

Chapter 2

Zero-Crossing Based Switched-Capacitor Integrator

With the continuous down-scaling of CMOS technologies, the design of operational transconductance amplifiers (OTA) in traditional switched-capacitor circuits has become increasingly problematic. The main challenges come from the scaled supply voltage and the reduced intrinsic gain of transistors. Along with a variety of design efforts to maintain the performance of the OTA while consuming more power [25][26], recently a number of OTA-less methods have been developed to address the problem from a new perspective [27][28][7]. The zero-crossing based (ZCB) circuit, which was originally referred to *comparator-based switched-capacitor* (CBSC) circuit, has gotten widespread attention after it was firstly introduced [29]. The well-known advantage of ZCB circuits is that the open-loop feature of zero-crossing detectors removes any stability concerns, which is energy-efficient because no frequency compensation is required for cascaded structures. Besides that, the charge-transfer mechanism in ZCB circuits is very different from that in traditional OTA-based switched-capacitor circuits. As will be shown in this thesis, it provides the potentia for purely self-timed operation in switched-capacitor circuits, especially in the switched-capacitor integrators of discrete-time $\Delta\Sigma$ modulators. Because of its importance, an intensive discussion on the zero-crossing based switched-capacitor integrators is given in this chapter.

As a start, the basic operation principle of the original ZCB/CBSC designs will be described first. Next, the non-ideal effects in ZCB switched-capacitor integrators are carefully investigated, including noise, offset and non-linearity. That is followed by a brief overview of prior work, mainly concerning the application of ZCB circuits in $\Delta\Sigma$ ADCs. After that, some advanced topologies are introduced to address the linearity limitation and further improve the energy-efficiency. The chapter ends with a short summary. The self-timed operation will be addressed in Chapter 4.

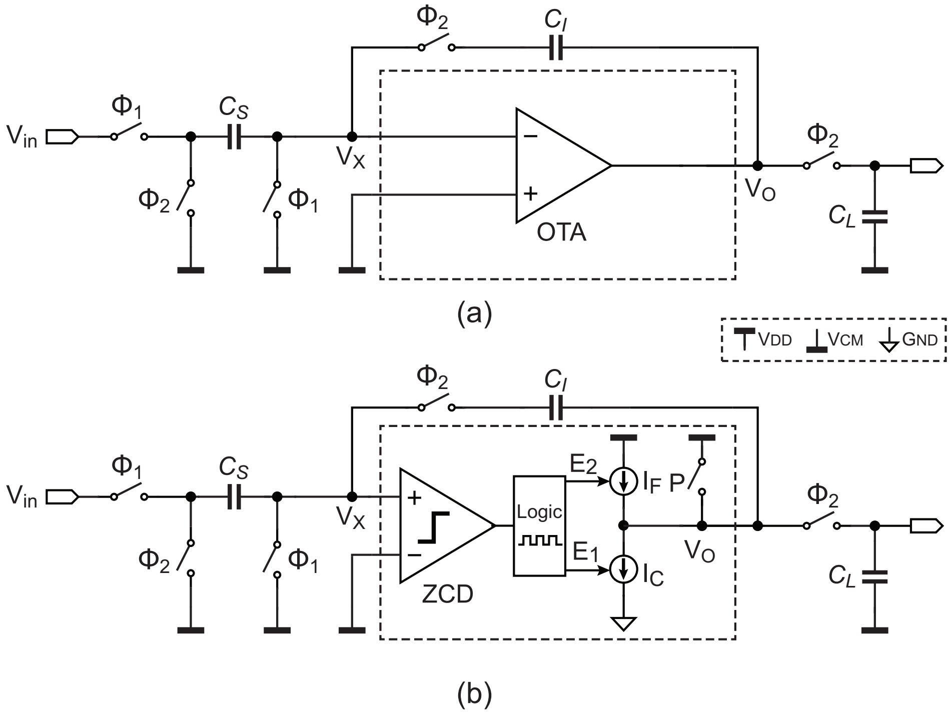

Figure 2-1: (a) OTA-based switched-capacitor integrator (b) ZCB switched-capacitor integrator

2-1 Basic Operation Principle

Figure 2-1 illustrates the typical implementations of both OTA-based and zero-crossing based switched-capacitor integrators. The topology of the ZCB switched-capacitor integrator is similar to its OTA-based counterpart, except that a zero-crossing-detector (ZCD) and a pair of gated current sources takes the place of the OTA. The output decisions of the ZCD control the on/off states of the current sources via local logic gates.

Like in the OTA-based circuit (Figure 1-1), the ZCB switched-capacitor integrator operates in a cycle of two non-overlapping phases: a sampling phase (Φ_1) and a charge-transfer (or integration) phase (Φ_2). Figure 2-2 shows its timing diagram in synchronous mode. The sampling phase is identical with that in conventional switched-capacitor circuits, during which the input voltage is sampled on the sampling capacitor C_S.

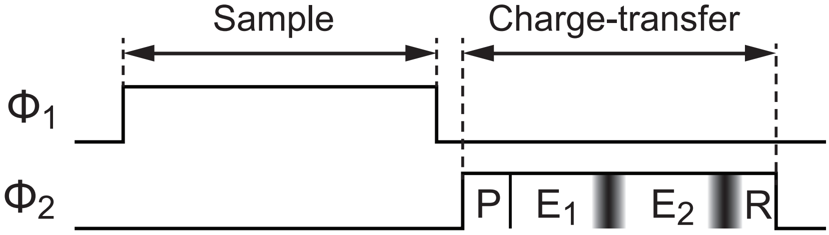

Figure 2-2: 2-phase timing of ZCB switched-capacitor integrator in synchronous mode (P: Preset; E_1: coarse phase; E_2: fine phase; R: redundancy)

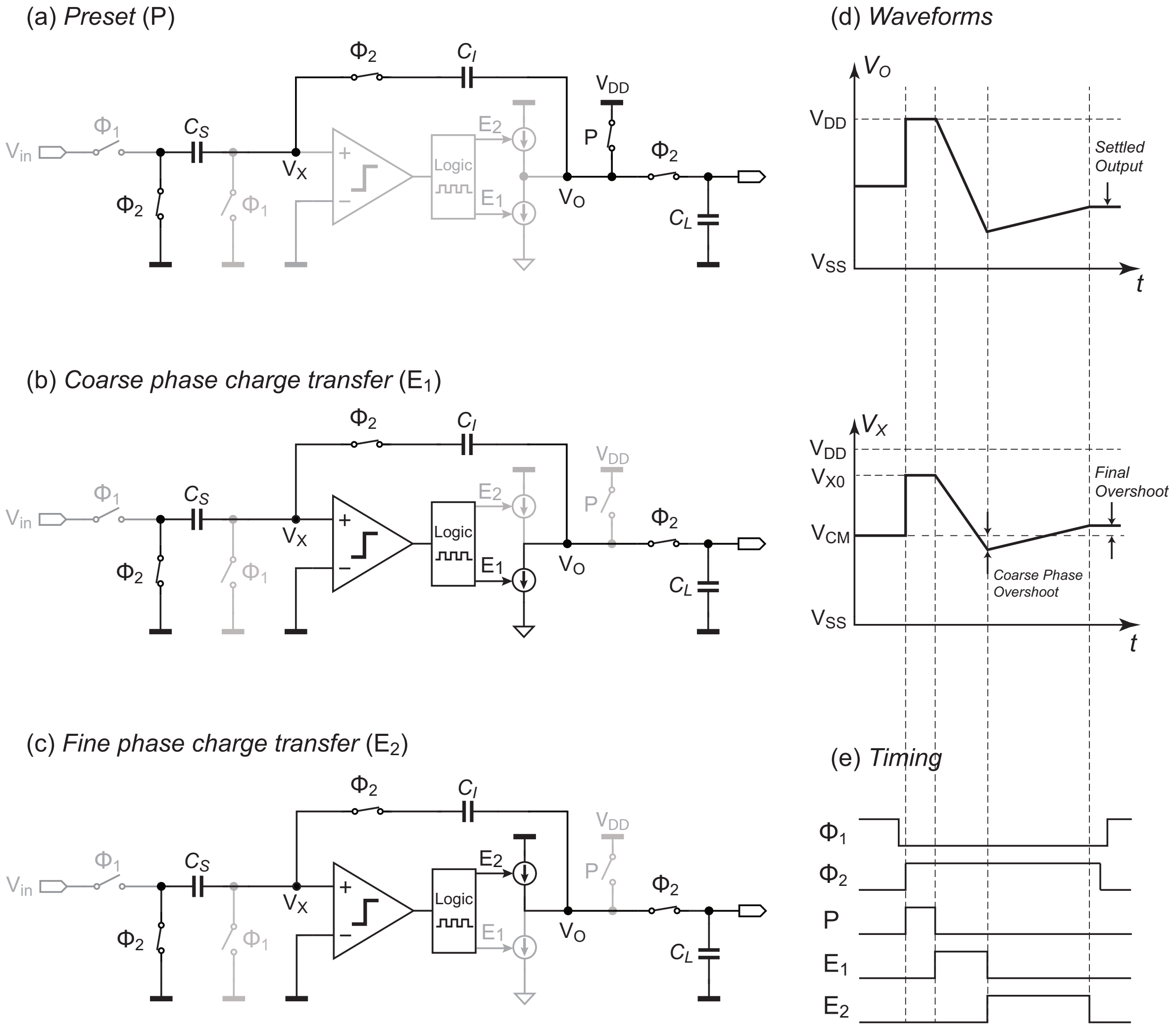
(a) Preset (P)
(b) Coarse phase charge transfer (E1)
(c) Fine phase charge transfer (E2)
(d) Waveforms
(e) Timing
Φ1
Φ2
CS
CI
Vin
VX
VO
VDD
P
E1
E2
Logic
CL
VSS
VX0
VCM
t
Settled Output
Final Overshoot
Coarse Phase Overshoot

Figure 2-3: Bidirectional charge-transfer process of conventional zero-crossing based switched-capacitor integrator

The charge-transfer phase of ZCB switched-capacitor integrator is, however, much more complicated. It can be divided in three successive sub-phases: preset (P), coarse phase (E_1) and fine phase (E_2). The preset phase has a short but fixed duration time, while the periods of the coarse and fine phase are both signal-dependent. In synchronous mode, there may be an interval of redundant time (R) between the completion of the fine phase and the falling edge of the charge-transfer phase-clock.

Figure 2-3 shows the operation flow of bidirectional charge-transfer process in conventional ZCB switched-capacitor integrators, including the corresponding waveform and timing sequence. During the preset phase (Figure 2-3 (a)), the output node of the integrator V_O is pre-charged to the supply voltage V_{DD}, thereby setting the virtual ground node V_X to a initial voltage V_{X0}. As the precondition for the successive zero-crossing detection, V_{X0} should be preset above the common-mode voltage. Its value can be derived from the charge conservation on V_X, as:

$$(V_{IN} - V_{CM})C_S + (V_O{}' - V_{CM})C_I = (V_{CM} - V_{X0})C_S + (V_{DD} - V_{X0})C_I \tag{2-1}$$

where V_{IN} is the input voltage and $V_O{}'$ is the integrator output voltage before preset. Assuming that $V_{CM} = \frac{1}{2}V_{DD}$, V_{X0} can be defined by the following equation:

$$V_{X0} = \frac{(V_{DD} - V_{IN})C_S + (\frac{3}{2}V_{DD} - V_O{}')C_I}{C_S + C_I} \tag{2-2}$$

To ensure $V_{X0} \geqslant V_{CM}$, we have

$$\frac{V_{IN} - V_{CM}}{V_{DD} - V_O{}'} \geqslant \frac{C_I}{C_S} \Rightarrow \frac{V_{IN} - V_{CM}}{V_{DD} - V_O{}'} \geqslant \frac{1}{\beta} \tag{2-3}$$

where $\beta = C_S/C_I$ is the scaling factor of the integrator. This inequality gives an extra constraint condition on the input voltage range and the integrator output swing, which should be considered in the $\Delta\Sigma$ modulator design (Chapter 4).

After the preset, the coarse current source I_C is switched on (E_1), discharging the capacitor network formed by C_S, C_I and C_L (integrator load). This process generates a rapid voltage ramp on nodes V_O and V_X. Once the zero-crossing detector recognizes the virtual ground condition ($V_X = V_{CM}$), the coarse current source is turned off immediately and the coarse phase charge-transfer is finished.

However, due to the finite response time of the zero-crossing detector and the steep ramp rate, there will be a large overshoot on V_X. To make a more accurate detection of the virtual ground condition, a fine current source I_F is turned on (E_2) right after the end of the coarse phase, recharging the capacitor network until the virtual ground condition is detected once again. The fine phase current is much smaller than the coarse phase current and of the opposite polarity, which results in a relatively small final overshoot (Figure 2-3 (d)). After the second virtual ground crossing, the charge-transfer from C_S to C_I is completed, and the corresponding voltage is sampled on C_L. Then the whole circuitry enters idle state until the next sampling phase starts.

The z-domain transfer function of zero-crossing based switched-capacitor integrator is identical with that of its OTA-based counterpart:

$$\frac{V_O(\mathrm{z})}{V_{IN}(\mathrm{z})} = \beta\frac{\mathrm{z}^{-\alpha}}{1 - \mathrm{z}^{-1}} \tag{2-4}$$

where α equals 1 for full-delay implementations and 1/2 for half-delay implementations.

It is noteworthy that the transition from the coarse phase to the fine phase is self-timed. Moreover, the time required to accomplish the charge-transfer is signal-dependent and varies from cycle to cycle. It is determined by the preset value of V_X, which depends on the input signal as well as the stored charge on the integration capacitor (Equation (2-2)) . In traditional synchronous-mode implementations, this feature is not enjoyed due to the fact the period allocated for charge-transfer must be long enough to ensure correct operation in all conditions, which degrades the circuit operation speed. Fortunately, we will find in Chapter 4 that when shifted to the self-timed mode this problem no longer exists.

2-2 Noise in ZCB Switched-Capacitor Integrator

Noise is one of the main limitations of accuracy in zero-crossing based switched-capacitor integrators, as is the case in traditional OTA-based designs. Except for the well-understood kT/C noise resulting from the sample operation in the front-end circuit, only the noise during the fine phase charge-transfer, especially at the instant of the threshold-crossing, has impact on the final output voltage of the integrator. A variety of noise sources contribute to this process, as listed in Table 2-1.

Table 2-1: Noise Sources in Charge-transfer Process

Index	**Noise Type**	**Contributor**
1	Thermal noise	Zero-crossing detector
2	Flicker noise	Zero-crossing detector
3	Flicker noise	Gated current source
4	Shot noise	Gated current source
5	Switch noise	Switches

While the noise from the gated current sources directly leads to error charge on the integration capacitor, the output noise of the zero-crossing detector results in jitter of the crossing-time decision, as illustrated in Figure 2-4. This feature brings some differences in the noise transfer function of the zero-crossing detectors.

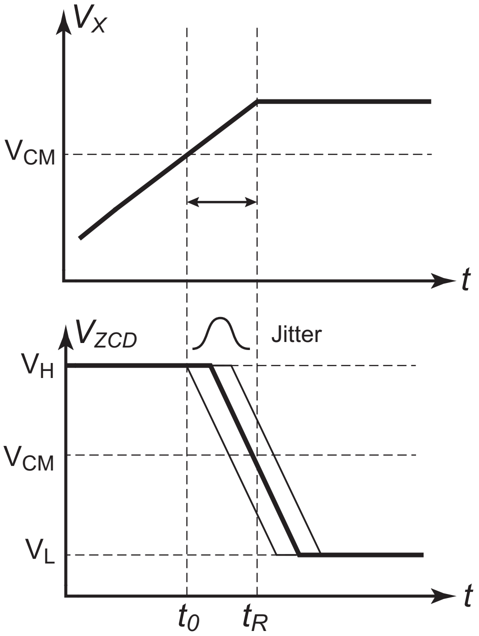

Figure 2-4: Noise-induced jitter in zero-crossing-based switched-capacitor integrator (V_X: virtual ground node voltage; V_{ZCD}: output voltage of the ZCD)

This section will present a brief investigation on the thermal noise in the zero-crossing detector[1], as well as a design-oriented overview of other noise sources.

2-2-1 Thermal Noise in the Zero-Crossing Detector

Traditional thermal noise analysis on OTA-based switched-capacitor circuits, such as [31], relies on the assumption that the amplifier operates in the steady-state. In other words, the statistics properties of the noise do not vary with time and can be measured with the well-known time-averaged root-mean-square (RMS) value. However, this assumption is not valid in the zero-crossing based switched-capacitor circuit, because it depends on the transient response of the zero-crossing detector and does not necessarily reach steady-state throughout its operation. The variance and hence the RMS value of the noise is not static with time. Therefore, conventional noise analysis based on frequency domain method is not applicable in ZCB switched-capacitor circuits.

A time-domain analysis method is proposed in [30] to address this problem, which is based on the autocorrelation between non-stationary random processes. It states the following:

For a white noise unit step input $u(t)$, the time-variant output variance of noise power $\sigma_n^2(t)$ can be modeled by the product of the integral of the impulse response in the time-domain and the double-sided white noise power spectral density (PSD), as follows:

$$\sigma_n^2(t) = S_{xx} \int_{-\infty}^{t} |h(\tau)|^2 d\tau \tag{2-5}$$

where S_{xx} is the double-sided white noise PSD and $h(t)$ is the system impulse response.[2]

Based on this theoretical conclusion, an estimation of thermal noise in zero-crossing based switched-capacitor integrators can be performed with a similar approach as that presented for OTA-based integrators in [31]. Firstly, a noise model of the zero-crossing detector should be established.

Noise Model

A zero-crossing detector is essentially a tailored wide-band continuous-time comparator. In order to reduce the input-referred noise of the ZCD, a low-noise band-limiting preamplifier is usually added in front of the wide-band crossing detector [30], as illustrated in Figure 2-5 (a). This preamplifier typically dominates both the noise performance and the speed of the ZCD. Unlike amplifiers in conventional switched-capacitor circuits, the preamplifier in the ZCD does not necessarily enter steady-state during its operation. However, its small-signal model at the instant of the crossing-response (t_R in Figure 2-4) can still be utilized for a first-order noise

---

[1] A comprehensive discussion on CBSC noise and the corresponding frequency-domain analysis techniques can be found in [30].

[2] To get an intuitive understanding on this formula, let's have a look at the traditional case. In steady-state systems, the time-invariant noise power is given by:

$$\sigma_n^{2\prime} = S_{xx} \cdot NBW_o \tag{2-6}$$

where NBW_o is the output noise bandwidth (double-sided). Therefore the integral of time-domain impulse response in Formula (2-5) can be regarded as the equivalent noise bandwidth in non-steady-state systems, albeit time-variant.

analysis, since only the noise power at that moment has impacts on the final decision. In the small-signal model, the preamplifier can be modeled as a simple transconductance amplifier loaded with a band-limiting capacitor, as shown in Figure 2-5(b).

In the following discussions the input-referred noise and noise-bandwidth of the preamplifier will be investigated. Before that, the output noise power and equivalent noise gain of the preamplifier should be calculated.

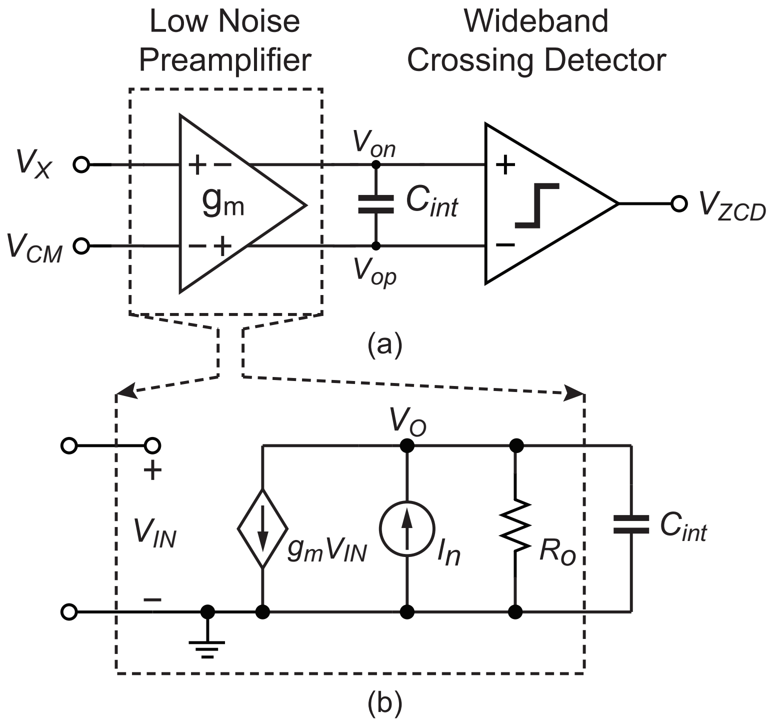

Figure 2-5: (a) Typical structure of zero-crossing detector; (b) Small-signal model of the preamplifier at the instant of threshold crossing

Output Noise of the Preamplifier

In a transconducance amplifier, the impulse response from the noise current source I_n to the output voltage V_o can be given by [30]:

$$h_i(t) = \frac{1}{C_{int}} e^{-t/\tau} \tag{2-7}$$

where C_{int} is the internal band-limiting capacitor in the ZCD, and $\tau = R_0 C_{int}$ is the time constant at the output of the transconductance amplifier.

The noise current source I_n can be modeled as a equivalent thermal noise transconductance g_n with a double-sided white noise PSD as:

$$S_{xxi} = 2kTg_n \tag{2-8}$$

Thus the time-variant output noise power of the preamplifier can be obtained by substituting Equation(2-7) and (2-8) into Formula (2-5), giving:

$$\overline{v_o^2}(t) = \frac{kT}{C_{int}} g_n R_o [1 - e^{-2t/\tau}] u(t) \tag{2-9}$$

where $u(t)$ is the unit step function.

The concerned output noise power of the zero-crossing detector can be obtained by substituting $t = t_R$ into the above equation, due to the fact that only the noise at the instant of the response time defects the accuracy of the integrator.

Noise Gain

As mentioned in previous sections, the output noise of a ZCD results in jitter of the zero-crossing decision time, which can be referred to the input ports in the form of noise voltage on the virtual ground node. Therefore, the noise gain of the preamplifier can be determined by the ratio of voltage slopes at the output and input ports:

$$|G_N| = \left(\frac{dv_o(t)}{dt} \bigg|_{t=t_R} \right) \bigg/ \left(\frac{dv_X(t)}{dt} \bigg|_{t=t_R} \right) \tag{2-10}$$

In zero-crossing based switched-capacitor integrators, the input voltage to the ZCD during the fine phase charging can be regarded as a slow ramp:

$$v_{IN}(t) = Mtu(t) \tag{2-11}$$

where $M = dV_{IN}/dt$ is the input ramp rate. According to [30], the time-domain response of a transconductance amplifier to a ramp input can be described by the following expression:

$$v_O(t) = A_0 M \left[t - \tau(1 - e^{-t/\tau}) \right] u(t) \tag{2-12}$$

where $A_0 = g_m R_o$ is DC gain of the transconductance amplifier at the instant of crossing-response. Thereby, the output voltage slope of the preamplifier is:

$$\frac{dv_O(t)}{dt} = A_0 M (1 - e^{-t/\tau}) u(t) \tag{2-13}$$

Consequently, the noise gain of the preamplifier is:

$$|G_N| = A_0 (1 - e^{-t/\tau}) u(t) \tag{2-14}$$

Input-referred Noise of the Preamplifier

On the basis of Equation(2-9) and (2-14), the input referred thermal noise power can be derived by:

$$\overline{v_{in,\mathrm{ZCD}}^2}(t_R) = \frac{\overline{v_o^2}(t_R)}{|G_N|^2} \tag{2-15}$$

$$= \frac{kT}{C_{int}} \frac{g_n}{g_m^2 R_o} \frac{1+e^{-t_R/\tau}}{1-e^{-t_R/\tau}} \tag{2-16}$$

$$= \frac{kT}{\tau} \frac{g_n}{g_m^2} \coth\left(\frac{t_R}{2\tau}\right) \tag{2-17}$$

Note that the term ${g_n}/{g_m}^2$ in the above expression can be regarded as the input-referred thermal noise resistance R_n in usual transconductance amplifiers. Thus the expression can be rewritten as:

$$\overline{v_{in,\text{ZCD}}^2}(t_R) = 4kTR_n \cdot \frac{1}{4\tau} \coth\left(\frac{t_R}{2\tau}\right) \tag{2-18}$$

All the above derivations are based on the time-domain analysis method. To make an interpretation from frequency-domain, consider the expression of input-referred noise power in usual steady-state amplifiers, which is the product of the input-referred thermal noise PSD and the corresponding noise bandwidth:

$$\overline{v_{in,\text{ZCD}}^2}(t_R) = 4kTR_n \cdot NBW_{i,ss} \tag{2-19}$$

Equivalently, the input-referred noise bandwidth in the non-stationary preamplifier can be defined as:

$$NBW_{i,ns} = \frac{1}{4\tau} \coth\left(\frac{t_R}{2\tau}\right) \tag{2-20}$$

It contains a hyperbolic function of the ratio of the preamplifier response time (t_R) to the time constant (τ). Two extreme conditions exist:

$$NBW_{i,ns} = \begin{cases} \dfrac{1}{4\tau}, & \text{for } t_R \gg 2\tau \qquad (2\text{-}21) \\ \dfrac{1}{2t_R}, & \text{for } t_R \ll 2\tau \qquad (2\text{-}22) \end{cases}$$

(2-21) is identical with the noise bandwidth in common single-pole steady-state systems; (2-22) shows an integrator-like noise bandwidth, which is inversely proportional to the integration (delay) time. This interesting characteristic offers an orientation to the design trade-offs of noise and speed in zero-crossing detectors. To be more precise, a plot showing the variation of the equivalent noise bandwidth with a wide range of preamplifier time constants and delay times is presented in Figure 2-6. The two extreme conditions are both highlighted on this plot. It reveals that:

- With a constant preamplifier response (delay) time, the noise bandwidth of the preamplifier shrinks as the time constant increases;
- With a fixed time constant, the noise bandwidth of the preamplifier reduces as the response time gets longer and the circuit operates slower.

Due to this noise-speed trade-off, a “sweet corner” in Figure 2-6, as is also highlighted, can be utilized as the optimal region for design choices. Within this region, the preamplifier time constant and response time follow the relationship as:

$$t_R \simeq 2\tau \tag{2-23}$$

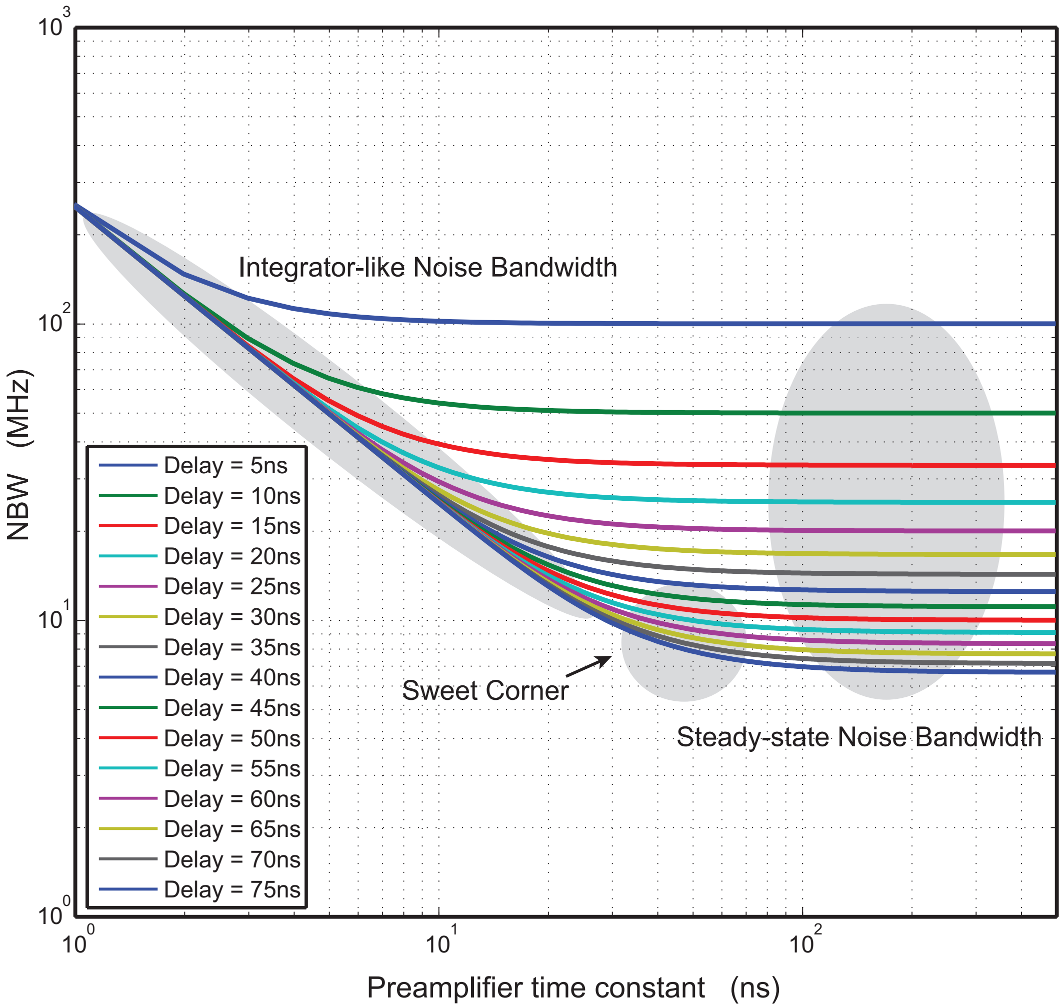

Figure 2-6: Equivalent noise bandwidth of the ZCD preamplifier

Accordingly, a relatively small noise bandwidth can be obtained without sacrificing the circuit operation speed too much. This rule of thumb can be applied for thermal noise estimation in the specific design of zero-crossing detectors, as will be shown in Chapter 5.

2-2-2 Flicker Noise

In semiconductor devices, flicker noise, also known as 1/f noise, is a type of frequency-dependent noise caused by fluctuations of carriers in the MOSFET channels [32]. Its single-sided power spectrum density can be modeled by the following expression [33]:

$$S_{x,1/\mathrm{f}}(f) = \frac{K}{C_{OX}WLf} \tag{2-24}$$

where K is a process-dependent constant, C_{OX} is the oxide capacitance per square of the MOS transistor and W, L are the width and length of the transistor gate, respectively. The magnitude of flicker noise is often measured with the so-called *corner frequency*, which defines the boundary between the 1/f noise dominant region and the “flat” white noise dominant region in the noise spectrum.

As is the case in most analog circuits, flicker noise dominates the low-frequency noise performance in zero-crossing based switched-capacitor integrators. Both the zero-crossing detector and the gated current sources generate flicker noise during the charge-transfer process. To reduce the effect of flicker noise in these circuit components, a variety of circuit techniques can be adopted, as discussed below.

Increasing the Dimensions of MOSFET Gates

Evidently and effectively, enlarging the area of MOS transistor gates ($W \times L$) can linearly reduce the flicker noise power density according to (2-24). The sizes of transistor gates can be increased properly until the flicker noise power within the desired bandwidth becomes negligible compared to other noise sources.The only penalty is an increase in the parasitic capacitance.

This method is applicable to gated current sources, which operate in a static rather than dynamic manner during the charge-transfer process. Moreover, the parasitic capacitance on their gates can even help in stabilizing the biasing voltage by decoupling the high frequency noise. One possible limitation comes from the switching speed of the gated current sources, which may be slightly degraded by the increased parasitic capacitance and should be taken care for in design.

In zero-crossing detectors, however, the cost is not free. Up-sizing input transistors of the ZCD will increase the parasitic capacitance on the virtual ground node, which introduces extra charge-loss during the charge-transfer process and aggravates the integrator leakage[3]. Therefore, it is necessary to search for other solutions.

Auto-zeroing

The auto-zeroing (AZ) technique is widely used in analog circuits for the cancellation of unwanted low-frequency disturbances such as offset and flicker noise [34]. The effect of AZ on the noise can be explained by Figure 2-7, where voltage source V_n and resistor R_n represent the input-referred noise voltage and noise impedance of the auto-zeroed analog module respectively. The operation of AZ process requires at least two phases: in the auto-zeroing phase (Φ_{az}), S_{az} is closed and V_n is sampled on the auto-zeroing capacitor (C_C); in the signal-processing phase ($\phi_{\overline{az}}$), S_{az} is opened and the time-invariant components of the sampled voltage on C_C are subtracted from the input or output signal, thus cancelling the low-frequency noise. In other words, the AZ process performs like a high-pass filter with an equivalent cutoff frequency related to the time interval between two auto-zeroing operations.

The discrete-time nature makes the AZ technique inherently applicable for zero-crossing based circuits. For example, the preamplifier of the zero-crossing detector can be auto-zeroed per cycle to attenuate the flicker noise generated from its input transistors, as will be shown in Chapter 3.

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[3] Further explanations can be found in Chapter 3.

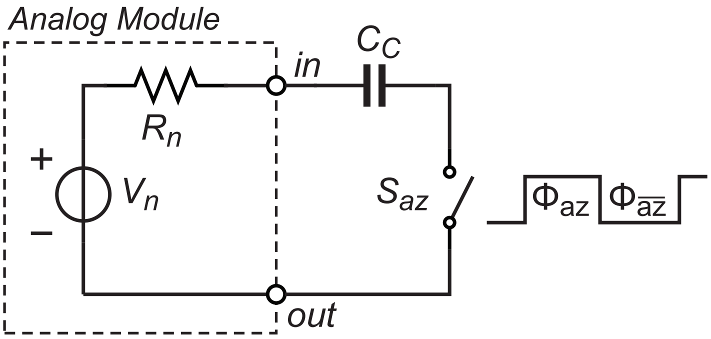

Figure 2-7: General operation principle of auto-zeroing process

The AZ technique also has drawbacks. It's essentially a type of sampling process, which leads to an increased white noise floor due to the folding of both thermal and flicker noise [34] [7]. Normally the foldover noise is dominated by the aliased thermal noise in the preamplifier, whose noise power spectral density can be estimated as:

$$S_{x,\text{thermal,fold}} = \frac{GBW}{f_s} \cdot 4kTR_n \tag{2-25}$$

where GBW is the gain-bandwidth product of the preamplifier and f_s is the sampling frequency in synchronous mode. This fact highlights the trade-off between accuracy and speed in the design of zero-crossing detectors again, being in line with the previous discussions in Section 2-2-1.

2-2-3 Other Noise Sources

Shot Noise

In electronic circuits, shot noise is a type of white noise that comes from the random fluctuations in electron charge conduction, such as a DC current flowing through PN junctions in semiconductor devices [35]. In contrast to thermal noise, shot noise is independent from temperature variation. With very tiny current and short charging time scale, the effect of charge fluctuation and hence the power of shot noise can be significant, otherwise it can be ignored. In zero-crossing based switched-capacitor circuits, the magnitude of the fine phase charging current is quite small (usually less than 1μA), arousing the necessity to make an examination of the impacts of shot noise.

According to the Schottky formula [36], the doubled-sided spectral power density of shot noise current in the fine phase current source can be given by:

$$S_{xx,shot} = qI_F \tag{2-26}$$

where I_F is the DC current magnitude of the fine phase current source.

During the zero-crossing delay time t_R, the mean square value of noise voltage across the integration capacitor can be estimated as: [**?**]

$$\overline{v_{o,shot}^2}(t_R) \approx \frac{S_{xx,shot}}{C_I^2} t_R = \frac{qI_F t_R}{C_I^2} \tag{2-27}$$

When referred to the input of the integrator, it becomes:

$$\begin{aligned}\overline{v_{in,shot}^2}(t_R) &\approx \frac{qI_F t_R}{C_I^2}\left(\frac{C_I}{C_S}\right)^2 \\ &= \frac{qI_F t_R}{C_S^2}\end{aligned} \tag{2-28}$$

Equation (2-28) reveals that shot noise power is positively related to the delay time of the zero-crossing detector and the fine phase current. For example, suppose that the fine phase current magnitude is 100nA, the response time of the zero-crossing detector is 100ns and the sampling capacitor is 1pF. The resulted input-referred shot noise voltage will be 40 μV$_{\text{rms}}$, which is not much a problem in over-sampling systems when compared with the thermal noise (see Chapter 5). What's more, in practice the shot noise will be even smaller than the prediction in Equation (2-28), as a result of the partial current-source-noise cancellation effect in the preamplifier [?]. Therefore, it is reasonable to expect that the shot noise will not bring about troubles in zero-crossing based switched-capacitor integrators.

Switch Noise

The finite on-resistance of series switches also contributes thermal noise during the charge-transfer phase. Its influence can be made negligible as long as the switch conductive resistance is small enough compared with the input-referred thermal noise resistance of the ZCD's preamplifier (R_n in (2-18)). Fortunately, this condition is quite common in practice due to the consideration on reducing switch-induced voltage-drops, as will soon be explained in the discussion on non-linearity effects (Section 2-3-1).

2-3 Error Sources in ZCB Switched-Capacitor Integrator

Like its OTA-based counterpart, zero-crossing based switched-capacitor integrators suffer from a number of circuit-level error sources which may cause offset and non-linearity. The problem mainly comes from the overshoot due to non-zero response delay of zero-crossing detectors, as well as a variety of non-ideal effects in the switches. In this section the generation mechanisms of these error sources will be analyzed in detail.

2-3-1 Offset

The finite response delay of zero-crossing detectors is the main source of offset in ZCB switched-capacitor integrators, especially in single-ended implementations. As depicted in Figure 2-8, a delay of crossing detection t_R at the end of the fine phase charging introduces an integrator output overshoot, as given by:

$$\Delta V_{OVO} = \frac{1}{C_T + C_L} I_F t_R \tag{2-29}$$

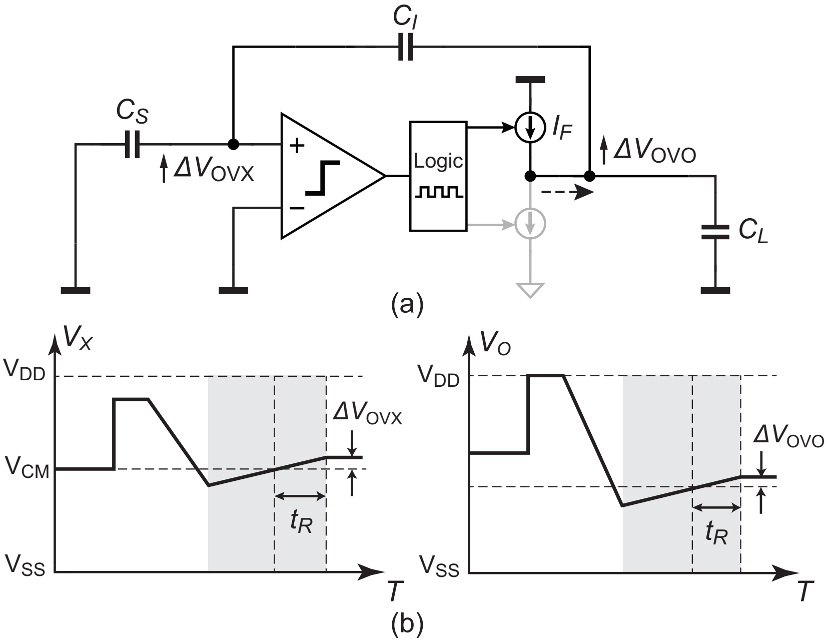

Figure 2-8: Effect of zero-crossing detector overshoots (a) Equivalent circuit topology in fine phase (b) Waveform on virtual ground V_X and integrator output V_O during fne phase charging

where $C_T = \dfrac{C_S C_I}{C_S + C_I}$ and I_F is the fine charging current flowing through the capacitor network. It results an overshoot at the virtual ground node:

$$\Delta V_{OVX} = \frac{C_I}{C_S + C_I}\Delta V_{OVO} \;\Rightarrow\; \Delta V_{OVX} = \frac{1/C_S}{1 + C_L/C_T} I_F t_R \tag{2-30}$$

The term $\dfrac{1/C_S}{1 + C_L/C_T} I_F$ represents the ramp rate at the input of the zero-crossing detector. The resulting error charge on the integration capacitor is:

$$\Delta Q = (\Delta V_{OVO} - \Delta V_{OVX})C_I \;\Rightarrow\; \Delta Q = \frac{1}{1 + C_L/C_T} I_F t_R \tag{2-31}$$

The signs of ΔQ and ΔV_{OVX} depend on the direction of I_F. For example, if $I_F < 0$, $\Delta Q < 0$, implying that there is charge loss during integration. Consequently, the effective sampled voltage V_{INE} on C_S can be defined by:

$$\begin{aligned} V_{INE} &= \frac{C_S V_{IN} + \Delta Q}{C_S} \\ &= V_{IN} + \Delta V_{OVX} \end{aligned} \tag{2-32}$$

It is equivalent to the situation that an effective input voltage of $V_{IN} + \Delta V_{OVX}$ is sampled in each cycle. The constant component in ΔV_{OVX} causes an offset, while the signal-dependent component due to variation of the ramp rate results in non-linearity.

The non-idealities of MOS switches can also cause offset problem. As with most sampling systems, the effects of charge-injection and clock-feedthrough [37] can introduce errors on the sampled output voltage during both sampling and integration phases. This error can be turned into a signal-independent offset with the aid of some well-developed circuit techniques like bottom-plate sampling and dummy switches [37]. As a result, it is conventionally recommended to minimize the sizes of switches on the charge-transfer path as long as the speed requirement is satisfied [38]. However, this design rule is not always appropriate for ZCB switched-capacitor circuits, particularly because of the constraint caused by voltage drops across the switches.

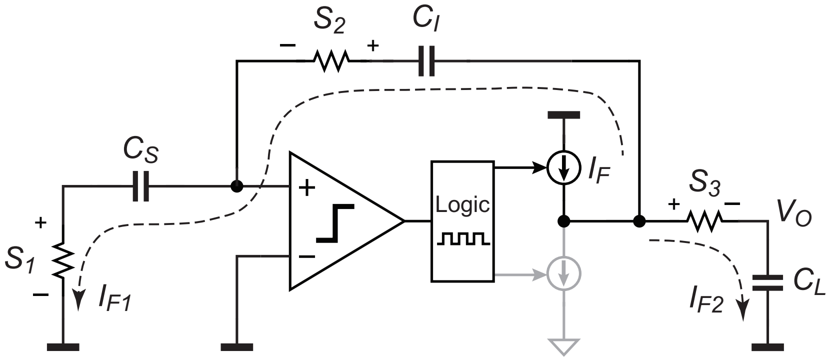

Figure 2-9: Effect of voltage-drop on series switches during charge-transfer process

The generation mechanism of these switch-induced voltage drops is illustrated in Figure 2-9. Unlike in exponential-settling switched-capacitor circuits, the current flowing through the capacitor-series switches is kept roughly constant throughout the charge-transfer phase. The finite on-resistances of switches S_1, S_2, S_3 produce a series of voltage drops on the charge-transfer path:

$$V_{d1} = I_{F1}R_{S1};\ V_{d2} = I_{F1}R_{S2};\ V_{d3} = I_{F2}R_{S3} \tag{2-33}$$

where $I_{F1} = I_F\dfrac{C_L}{C_L+C_T}$, $I_{F2} = I_F\dfrac{C_T}{C_L+C_T}$, and R_{S1}, R_{S2} and R_{S3} represent the on-resistance of switches S_1, S_2 and S_3, respectively. Theses voltage drops cause an integrator output voltage error as:

$$\Delta V_{O,vd} = -\frac{C_S}{C_I}V_{d1} + V_{d2} - V_{d3} \tag{2-34}$$

while the integrated error charge suffers from V_{d1} only:

$$\Delta Q_{vd} = -C_S V_{d1} \tag{2-35}$$

Therefore, the effective input voltage due to the voltage drops across the switches is

$$V_{INE,vd} = V_{IN} - V_{d1} \tag{2-36}$$

Expression (2-34) (2-35) and (2-36) reveal that only the switch connected in series with the sampling capacitor results in an input-referred error, while the voltage drop across the other switches just slightly shifts the output voltage of the integrator[4]. Like the overshoot-induced error, the constant portion in V_{d1} causes offset, while the portion that changes with input signal due to the variation of I_{F1} causes non-linearity.

Generally, the effect of V_{d1} is much less significant compared with the overshoot error. For instance, a constant fine phase current of 100nA flowing through a NMOS switch with 1kΩ on-resistance yields an input-referred offset of 100μV. It is far smaller than that contributed by the overshoot which is often in mV range. However, the situation can get worse in close-loop systems such as $\Delta\Sigma$ modulators, where the sampling capacitor is alternatively switched to different reference voltages for feedback purpose during charge-transfer phase. In this case, the value of R_{S1} may suffer from a wide dynamic range and produce dramatic linearity problems, as will be shown in the next sub-section.

All the above discussions are oriented to single-ended implementations. In differential implementations, the offset is dominated by the residue error of overshoots and switch voltage drops due to circuit component mismatches.

2-3-2 Non-Linearity

As mentioned in the previous sub-section, the signal-dependent portion in the overshoot and switch-induced voltage drop results in non-linearity. This signal-dependence mainly comes from the variation of charging current (I_{F1}) during the fine phase, and the changing on-resistance of critical switches[5]. Their generation mechanism and impacts are discussed below.

Variation of Charging Current

Figure 2-10(a) shows a typical topology of gated current source used in zero-crossing based switched-capacitor circuits. Both coarse and fine current sources are implemented with gate-controlled MOSFETs whose drain terminals are connected to the integrator output node (V_O). Due to the channel-length modulation [39], the drain current in both MOSFETs vary in response to the changing integrator output voltage, as illustrated in Figure 2-10(b).

According to the Shichman-Hodges model [40], the drain currents can be given as:

$$\begin{cases} I_C &= I_{C0}(1+\lambda_C V_O) \\ I_F &= I_{F0}[1+\lambda_F(V_{DD}-V_O)] \end{cases} \tag{2-37}$$

where I_{C0}, I_{F0} are constant terms and λ_C, λ_F are channel-length modulation coefficients for coarse and fine current sources respectively. In practice, λ_C and λ_F are not constant but slightly changing with the transistors' drain-to-source voltages as well. Accordingly, the charging currents reveal an approximately linear dependence on the integrator output voltage.

The large output swing of the integrator may turn this signal-dependence into a dramatic problem. As depicted in Figure 2-10(b), a stable integrator output can range from ground to

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[4] Here, the varying portions of V_{d2} and V_{d3} are neglected, which is reasonable in practice.

[5] Variation of capacitor network (C_S, C_I and C_L) can also introduce signal-dependent error. Nevertheless, the voltage-depenency of these capacitors is normally small in most applications of SC integrators. Therefore there's no need to discuss their impacts here.

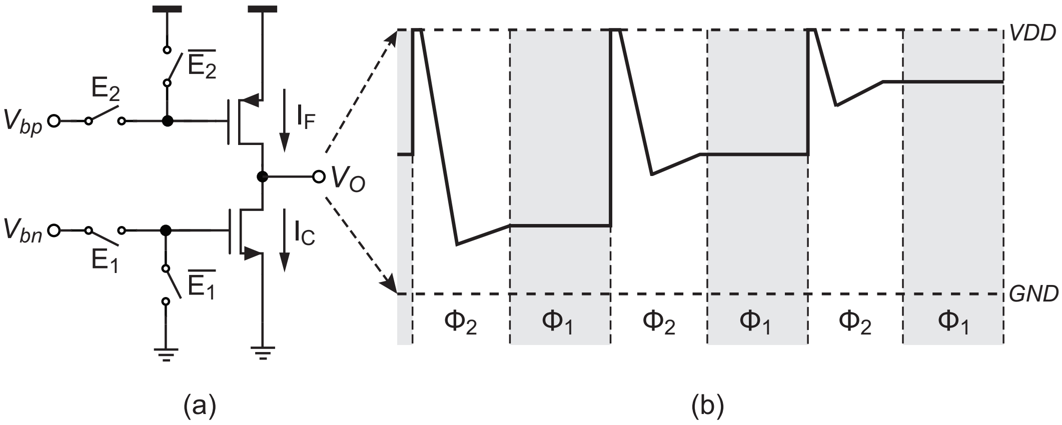

Figure 2-10: (a) Typical topology of gated current source in ZCB switched-capacitro integrator(b) ZCB switched-capacitor integrator output voltage swing

the power supply voltage maximally. This fact aggravates the variation of charging currents especially during the fine phase, thus ruining the charge-transfer linearity.

From another point of view, the value of $\lambda_{C,F}$ can be regarded as a measure of the finite output impedance of current sources, as described by:

$$\begin{cases} r_{OC} &= \dfrac{1+\lambda_C V_O}{\lambda_C I_C} \\ r_{OF} &= \dfrac{1+\lambda_F (V_{DD}-V_O)}{\lambda_F I_F} \end{cases} \tag{2-38}$$

A larger current source output impedance corresponds to a smaller channel-length modulation coefficient and hence better linearity. In an extreme case, $r_{OC,F} \to \infty$ when $\lambda_{C,F} = 0$, which indicates that with infinite current source output impedance the charging currents are absolutely stable against the integrator output signal.

Conventionally, there are two general methods to address the non-linearity problem caused by charging current variations: reducing the integrator output swing and increasing the output impedance of gated current sources. However, each method has its own demerit: the reduction of output swing often requires an aggressive scaling in the signal transfer function (STF), leading to degradation of the signal-to-noise ratio (SNR); on the other hand, traditional circuit techniques used for boosting current source output impedance, such as transistor cascoding [23], are not compatible with low-voltage circumstances which ZCB circuits are originally designed for. Based on the above reasons, creative ideas are called for to provide new solutions, and one of them will be presented in Section 2-5.

Mismatch of Switch On-resistance Due to Feedback

In some applications like discrete-time $\Delta\Sigma$ modulators, switched-capacitor integrators are often implemented in a close-loop configuration. To implement charge-balancing, feedback signals are usually applied at the input of the integrators during the sampling or the charge-transfer phase. The former scheme (Figure 2-11(a)) is generally not preferred in energy-constrained designs, because the extra sampling capacitor C_{FB} introduces extra kT/C noise

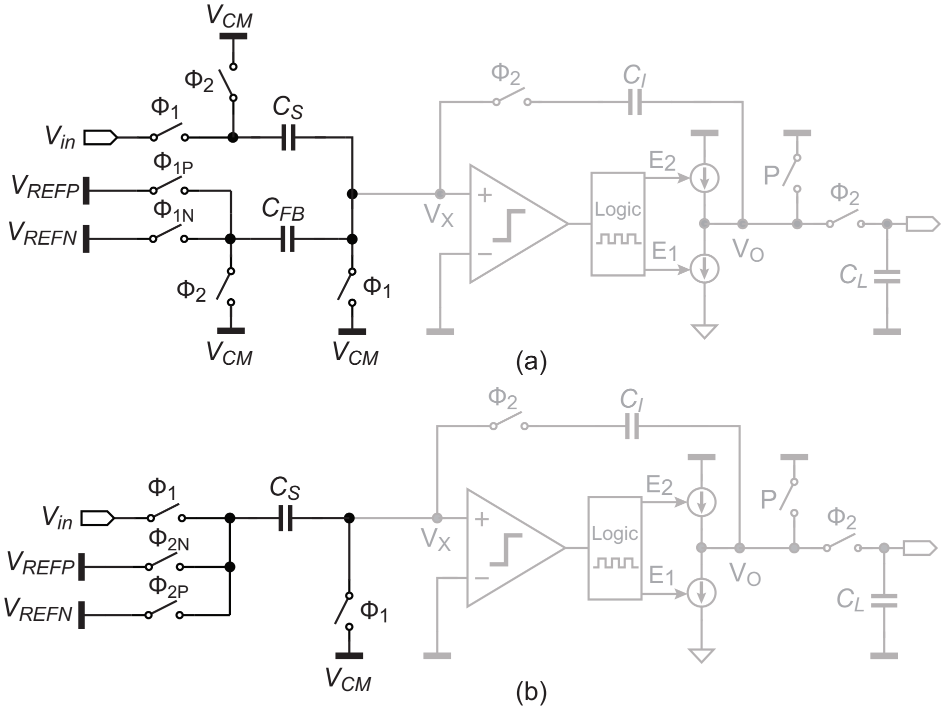

Figure 2-11: Feedback schemes in ZCB switched-capacitor integrator (a) feedback in sampling phase (b) feedback in charge-transfer phase

and gain error as well as more power consumption. The latter scheme (Figure 2-11(b)) gets rid of these problems by accomplishing the feedback operation in the charge-transfer phase, during which the top plate of the single sampling capacitor is switched to different feedback voltages. This topology is widely used in OTA-based switched-capacitor integrators, while in their ZCB counterparts the mismatches between the on-resistances of feedback switches may become problematic.

Figure 2-12 illustrates the cause of the problem. During the charge-transfer phase, the feedback MOSFET switches S_{1P} and S_{1N} are alternatively turned on according to the system output condition. Their on-resistances are given by [37]:

$$R_{on} = \frac{1}{K'\frac{W}{L}V_{od}} \tag{2-39}$$

where K' is a process-dependent parameter, $\frac{W}{L}$ is the designed switch dimension and V_{od} is the transistor overdrive voltage. Since the feedback switches are connected to different reference voltages (V_{REFP} and V_{REFN}), their overdrive voltages differ from each other. What's worse, given the fact that S_{1P} and S_{1N} are usually implemented with different types of MOSFETs (eg. NMOS and PMOS) and fabricated in different silicon substrates[6], the matching of process parameters and switch dimensions are both poor. As a result, the on-resistances of S_{1P} and S_{1N} suffer from a critical systematic mismatch and create different input-referred voltage error according to Figure 2-36. It's equivalent to disturbing the balance between the two feedback signals.

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[6] In standard single-well process, PMOS transistors are fabricated in n-type wells while NMOS transistor are fabricated in p-type substrate.

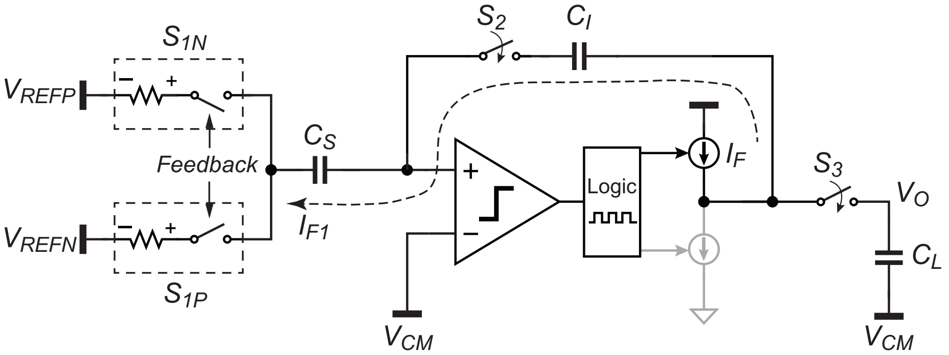


Figure 2-12: Topology of feedback-included ZCB integrator during charge-transfer process

Generally, the occurrence ratios of positive and negative feedback are correlated to the input signal magnitude. Consequently, the mismatch of feedback switches finally results in a system-level gain error if the variation of charging current is neglected. To reduce its impact, a feasible method is to increase the $\frac{W}{L}$ ratio of the MOSFETs thus minimizing the absolute value of switch on-resistance, at the cost of larger parasitic capacitance and hence more dynamic power consumption.

2-4 Prior Work

The zero-crossing based switched-capacitor circuit has been applied in various types of ADCs, performing as gain stages or integrators. Its first prototype was demonstrated in a pipeline ADC [21], where the opamps in pipeline gain stages were replaced by a general-purpose comparator and a pair of bidirectional current sources. In order to achieve a high gain, the comparator was implemented with multi-stage cascaded amplifiers, resulting in a considerable power consumption. In the follow-up designs, a more power-efficient zero-crossing detector took the place of the comparator. It was employed in both single-ended [22] and fully-differential [41] pipeline structures. Later on, a voltage-scalable zero-crossing based pipeline ADC was present in [42], demonstrating the low-voltage amenability of ZCB designs.

Typically, the target applications for pipeline ADCs, such as communication systems, require for high conversion speed (5MS/s to 200MS/s) and medium resolution (8b to 12b). Within this specification scope, the aforementioned non-linearity problem of ZCB circuits does not necessarily become the performance bottleneck. However, this problem does restrict the application of ZCB circuits in oversampling data converters which are commonly aimed at higher resolution and linearity (>13b ENOB or >80dB SNDR), such as discrete-time $\Delta\Sigma$ ADCs. The first comparator-based switched-capacitor $\Delta\Sigma$ modulator was reported in [23]. In spite of the usage of cascoded current sources at the cost of a relatively high supply voltage (1.8V), the design only achieved 65.3dB SNDR with a rather poor energy-efficiency (6.98pJ/step). When compared with the earlier OTA-based designs (eg. [25][7]), this performance is obviously not attractive.

To enhance the low-voltage operation capacity, a second-order zero-crossing based $\Delta\Sigma$ ADC targeting for MHz-level signal bandwidth was introduced in [24]. In this design, switched-resistor current sources were employed to improve the dynamic matching between differential charging and discharging currents. Since no transistors were used in the current sources, the required supply voltage was reduced as well. However, the poor output impedance of resistor-based current source also significantly degraded the converter's linearity performance. With a 1.1V supply, the ADC achieved 0.833MHz signal bandwidth by consuming 630μW power, while the peak SNDR was only 47.7dB.

In order to address the linearity problem, some modified ZCB topologies were proposed in recent years. In [43], a fourth-order comparator-based $\Delta\Sigma$ ADC was powered by 1V, while the cascoded current sources were driven by a higher voltage boosted from the low supply. In this way, the current source output impedance can be enhanced without disturbing the integrator output swing. The disadvantage is that a large bypassing capacitance between two voltages was required to minimize the impact of supply voltage deviation on the charging current. In addition, since the boosted voltage was used as a static power source, it raised reliability concerns such as latch-up. This design achieved 1MHz signal bandwidth and 63dB SNDR in 90nm CMOS process, with an energy consumption of 1.82pJ/step.

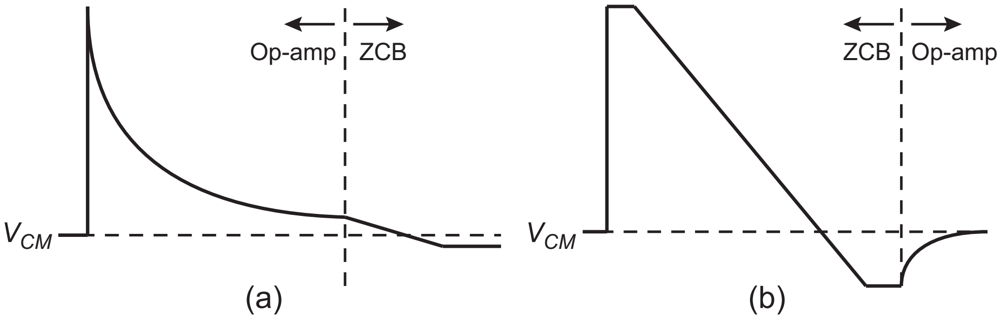


Figure 2-13: Opamp-assisted charge-transfer waveform on virtual ground node (a) ACBSC topology [1] (b) Hybrid opamp/ZCB topology [2]

Another interesting idea is to re-involve the opamps in the charge-transfer process. An amplifier and comparator based switched-capacitor (ACBSC) technique was present in [1]. By applying a low-gain amplifier across the integration capacitor, the output swing requirements of the current sources can be relaxed, hence the variation of charging current can be reduced. As shown in Figure 2-13(a), the charge-transfer process starts with an opamp-driven exponential settling, and the current sources and comparators are turned on subsequently to cover the remained error due to the finite amplifier DC gain. A third-order $\Delta\Sigma$ modulator was designed and simulated based on this technique. However, its effectiveness has not been demonstrated yet due to the lack of silicon verification.

The order of hybrid opamp/ZCB charge-transfer process can also be exchanged. In [2], the coarse phase charge-transfer was accomplished by a traditional ZCB topology, while the fine phase charge-transfer was performed by a low-gain amplifier (Figure 2-13(b)). In this way, the inaccuracy problem of the ZCB technique was overcome with the aid of the small-swing exponential settling. Although this technique was firstly developed for pipeline structures, it is apparently also suitable for $\Delta\Sigma$ ADCs. The common shortcoming of the above opamp-assisted ZCB topologies is the increased circuit complexity, as well as the degraded amenability to low supply voltage due to the involvement of opamps.

Table 2-2 summaries the performance of recent published $\Delta\Sigma$ ADCs based on zero-crossing detection technique.

Table 2-2: Performance Table of Prior CBSC/ZCB $\Delta\Sigma$ ADC

	[23]	[24]	[43]	[44]
Architecture	Second order	Second order	Fourth order	Second order
CMOS Technology	0.18μm	LP 45nm	90nm	TFT 3μm
Supply Voltage (V)	1.8	1.1	1.0	11.2
Bandwidth (MHz)	0.02	0.833	1	0.00156
OSR	64	30	48	128
Sampling Frequency (MHz)	2.56	50	96	0.4
Peak SNDR (dB)	65.3	47.7	66	65.6
Dynamic range (dB)	71	54.3	70	69
Power Consumption (mW)	0.42	0.63	5.94	63.3
Area (mm^2)	0.21	0.0448	0.33	26
FOM (pJ/step)†	6.98	1.91	1.82	13.03

† $\text{FOM} = \dfrac{\text{Power}}{2 \cdot \text{Bandwidth} \cdot 2^{\text{ENOB}}}$

2-5 Advanced Circuit Topologies for ZCB Switched-capacitor Circuits

As is mentioned in the previous section and proved by Table 2-2, the zero-crossing based technique has not yet revealed its charms in $\Delta\Sigma$ ADCs. The performance constraint mainly comes from the poor linearity and hence the limited energy-efficiency. Some advanced techniques designed for ZCB circuits, though not applied in $\Delta\Sigma$ ADCs yet, can be used in combination to overcome the challenge. As candidates, two types of recent reported circuit topologies are introduced in this section: the early-threshold detection technique, which improves the energy-efficiency of the charge-transfer process, and the asynchronous correlated level shifting (CLS) topology, which alleviates the non-linearity issue.

2-5-1 Early-Threshold Detection

In the original designs of zero-crossing based switched-capacitor circuits [21][23], a dual-phase bidirectional charge-transfer scheme (Figure 2-3) was employed to ensure accuracy. The basic idea is to perform two detections of the virtual ground condition, while the second one is more critical and hence is accomplished with a much slower crossing ramp-rate. However, this scheme has at least two drawbacks:

- It requires to detect bidirectional zero-crossings during a relative short time, which adds to the difficulty of the ZCD design. High gain and high speed preamplifiers are usually used at the expense of more power consumption, as is the case in [21].
- Due to the overshoot of the zero-crossing detector, the voltage on the virtual ground node goes across the threshold voltage twice within one cycle. It's equivalent to the situation that some charge is injected into the integration capacitor and then pumped out immediately, which results in unnecessary energy consumption and extra charge-transfer time.

To avoid the above defects, an unidirectional dual-phase charge-transfer scheme is introduced in [24] and [42]. As its name suggests, in this scheme both coarse and fine phase charging are of the same direction, and only one threshold-crossing on the virtual ground node is detected in each cycle. Instead of utilizing the first zero-crossing decision as the time-boundary between the two charging phases, an asynchronous charging controller triggers the transition from coarse phase to fine phase slightly earlier than the detection of the virtual ground condition, as if it can "predict" the zero-crossing event. This mechanism can be referred to as the **Early-threshold Detection** technique.

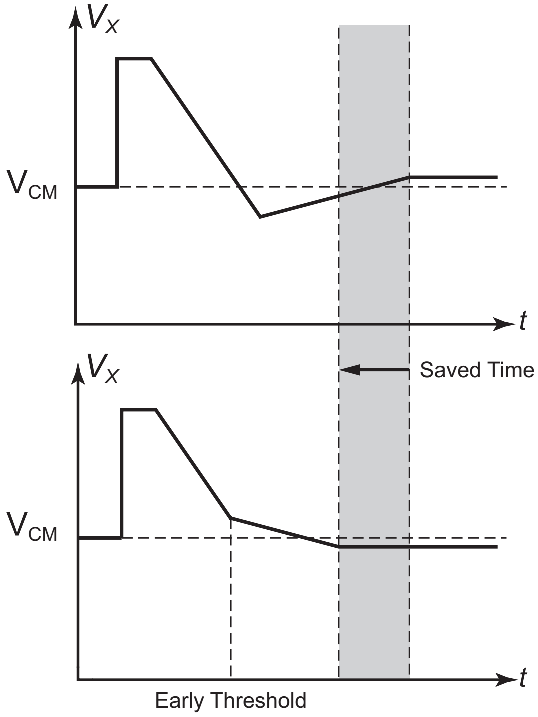


Figure 2-14: Conceptual illustration of bidirectional and unidirectional charging scheme. Ramp-rates in coarse phase and fine phase are identical in both schemes.

The conceptual difference between the unidirectional and bidirectional dual-phase charge-transfer scheme is illustrated in Figure 2-14. It is obvious that the virtual ground node voltage trajectory in unidirectional charge-transfer scheme is shorter than that in its bidirectional counterpart. This fact not only saves the unnecessary energy-consumption caused by overshoot recovery, but also increases the charge-transfer speed. Moreover, the single zero-crossing feature relaxes the response speed requirement for the ZCDs as well.

A side-benefit of unidirectional dual-phase charge-transfer scheme is the attenuation of spike disturbance caused by the charging phase transition [45]. In conventional ZCB designs based on bidirectional charging scheme, the turn-off of the coarse current sources and the turn-on of the fine current sources both happen during the phase transition, but not simultaneously due to the inevitable logic delay. The dramatic variation of impedance condition at the integrator output node may introduce significant voltage spikes that disturb the charge-transfer process, as shown in Figure 2-15. By contrast, in unidirectional charging scheme the fine current source can be turned on from the beginning of the coarse phase thanks to the identity of current direction, thus only the turn-off of the coarse current source is required during the phase transition. Consequently, the impedance variation at the integrator output node can be somewhat alleviated and the influence of voltage spikes can be attenuated. Another side-benefit is the reduction of phase transition time. Since the fine current source is already on when the fine phase starts, its parasitic capacitance doesn't introduce extra transition delay.

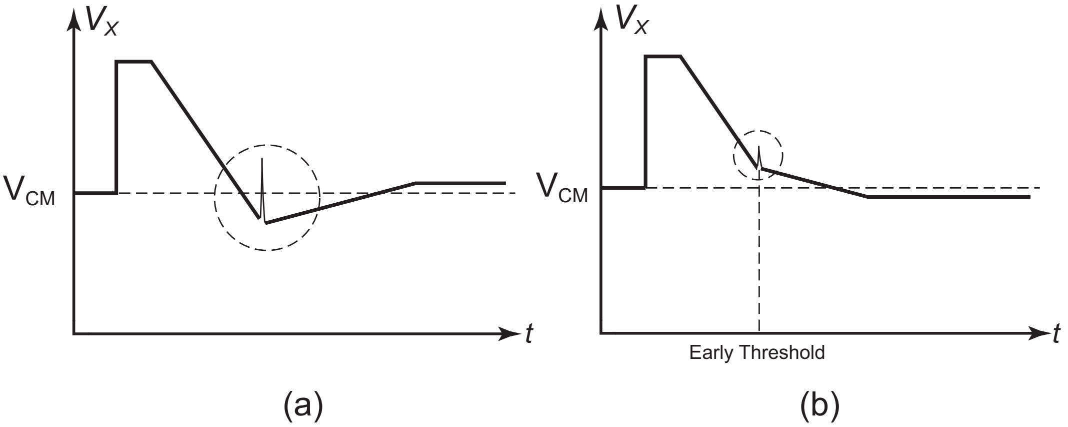


Figure 2-15: Illustration of voltage spikes during phase transition. (a) Bidirectional charge-transfer scheme (b) Unidirectional charge-transfer scheme

There are various types of circuit topologies available for the implementation of the early-threshold detection [24][42]. Their common essential idea is to insert a pre-defined offset into a parallel signal-processing path of the ZCD. Figure 2-16 shows one of such topologies. The output of the ZCD preamplifier is divided into two branches. One branch is directly supplied to the threshold detector to generate the normal zero-crossing decision, while an offset voltage is added to the other branch to generate the early decision. The offset voltage can be implemented with a periodically pre-charged capacitor, which is inherently compatible with the ZCB implementation. Detail circuit realizations and the consideration on the choice of the offset voltage will be discussed in Chapter 5.

2-5-2 Correlated Level Shifting

Traditional OTA-based switched-capacitor circuits suffer from non-linearity caused by the finite DC gain of the OTAs. The correlated level shifting (CLS) was firstly introduced in [46] as a power-efficient switched-capacitor technique to reduce the finite gain error while maintaining

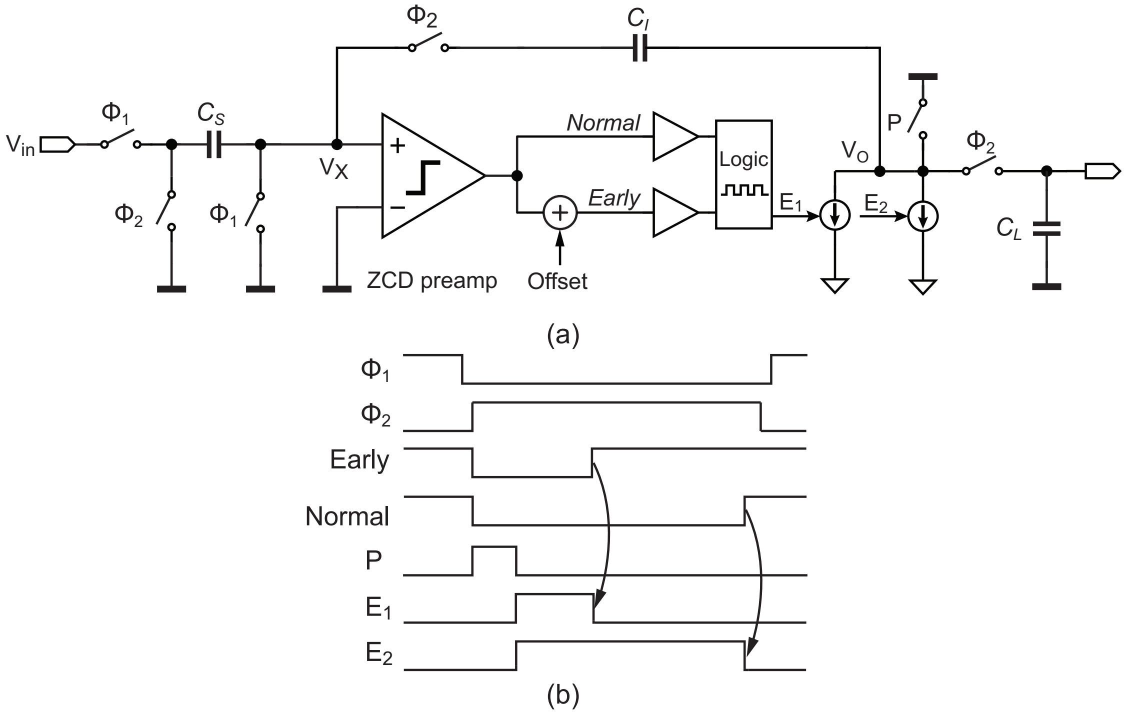

Φ2
CI
Vin
Φ1
CS
Φ2
Φ1
VX
+
−
ZCD preamp
Normal
Early
Offset
Logic
E1
E2
VO
P
Φ2
CL
(a)
Φ1
Φ2
Early
Normal
P
E1
E2
(b)

Figure 2-16: (a) Circuit realization of early-threshold detection. (b) Timing diagram

rail-to-rail output swing. The same idea can also be applied to zero-crossing based switched-capacitor circuits to reduce the current source non-linearity, as addressed in [47].

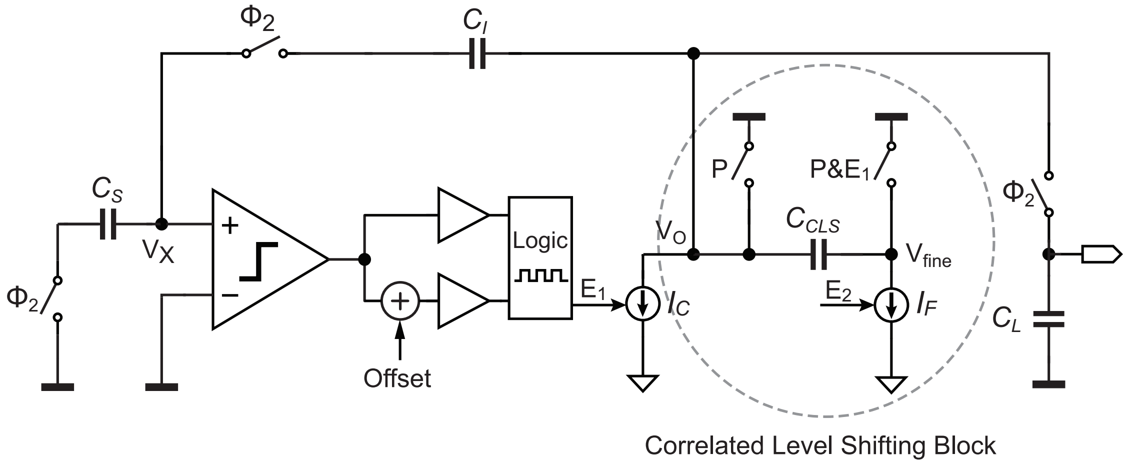
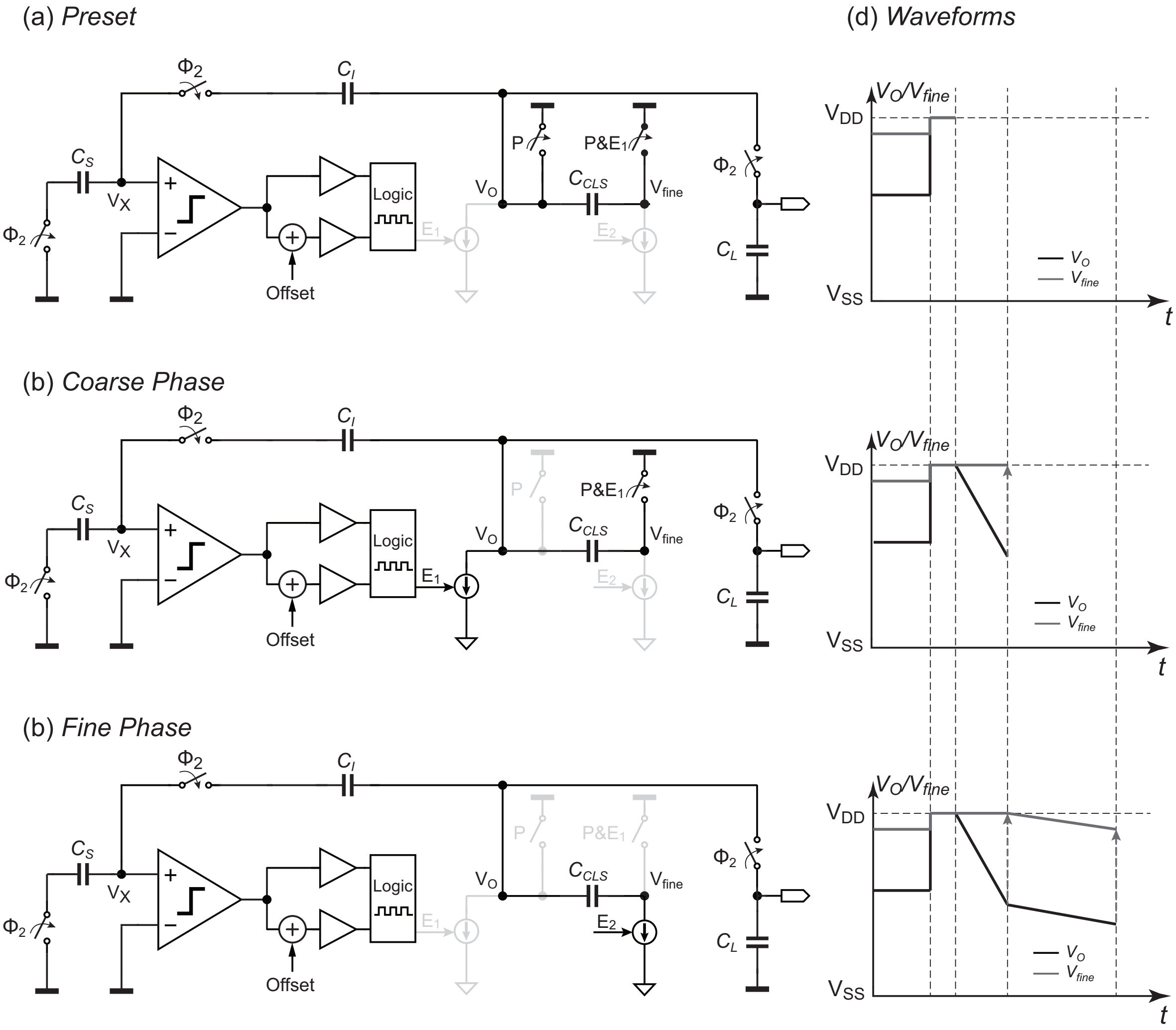

Φ2
CI
CS
VX
Φ2
+
−
Logic
Offset
E1
IC
VO
P
P&E1
CCLS
Vfine
E2
IF
Φ2
CL
Correlated Level Shifting Block

Figure 2-17: Topology of correlated level shifting circuit in ZCB integrator (only show charge-transfer phase)

A typical implementation of a ZCB integrator utilizing correlated level shifting is depicted in Figure 2-17. As shown in the schematic, the fine current source (I_F) is not directly connected but capacitively coupled to the integrator output via a level shifting capacitor C_{CLS}. An extra switch is connected to the fine current source output node to reset and sample the estimated output voltage. The unidirectional charge-transfer scheme is also included.


(a) *Preset*

(b) *Coarse Phase*

(b) *Fine Phase*

(d) *Waveforms*

Figure 2-18: Working Process of correlated level shifting in ZCB integrator (in charge-transfer phase)

It's worth noting that the utilization of CLS operation doesn't change the original working process of ZCB circuits, which is the beauty of this technique[7]. Figure 2-18 shows the charge-transfer process with CLS in a ZCB integrator. In the preset phase (Figure 2-18(a)), the integrator output node (V_O) and the fine current source output node (V_fine) are both pulled up to the supply voltage, thus resetting the level shifting capacitor. Next, V_O is released in the coarse phase (E_1) and the coarse current source starts to discharge the capacitor network, while V_fine is still stuck at the supply voltage(Figure 2-18(b)). As a result, by the end of the coarse phase the voltage difference between V_{DD} and the estimated value of V_O is sampled on C_{CLS}. In the fine phase (E_2), V_fine is level-shifted towards the supply voltage and the fine current source is switched on. In this way, the coarse and fine phase in the ZCB operation simultaneously perform as the estimation and level-shifting phase in the CLS operation.

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[7] In OTA-based designs, to employ CLS operation the charge-transfer process has to be deliberately divided into two phases (estimation and level-shifting) [46], which complicates the clock timing.

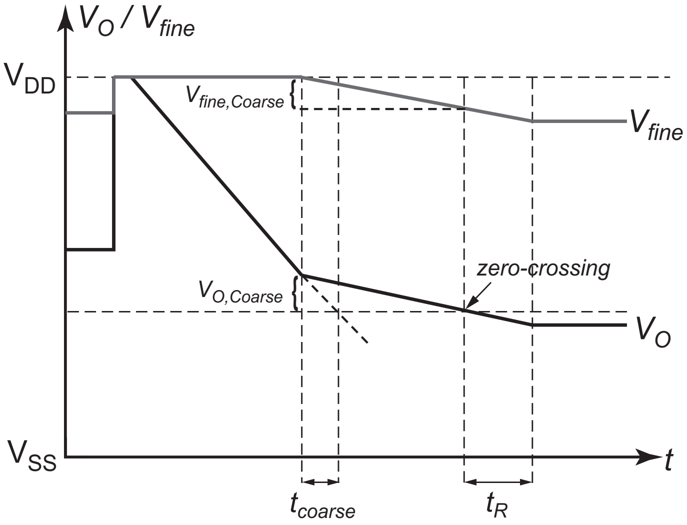

Figure 2-19: Timing diagram of correlated level shifting with unidirectional charging scheme

Thanks to the slow ramp-rate during the fine phase, the voltage swing seen by the fine current source is relatively small. What's more, the trajectory of V_{fine} starts from V_{DD} in each cycle, thus removing the dependence of the fine phase charging current on the integrator output voltage. In other words, the CLS technique eliminates the correlation between the full output swing of the integrator and the critical charging current. Therefore, the non-linear ramp-rate variation due to finite output impedance of current sources can be significantly reduced.

The benefit of CLS technique for the linearity of ZCB circuits can be theoretically demonstrated as well. For the convenience of discussion, the output voltage waveform of a CLS-assisted unidirectional ZCB integrator is redrawn in Figure 2-19. Given that only the relationship between V_O and the fine phase charging current is of interest, the fine phase ZCD response delay (t_R) can be neglected since it is relatively constant. As a rough approximation, the timing advance between the early-threshold response and the virtual coarse phase zero-crossing (t_{coarse}) can be assumed to be constant. According to (2-37), the fine charging current at the end of the fine phase is

$$I_{\text{fine}} = I_{\text{fine0}} - \frac{1}{\beta_{CLS}} \frac{V_{\text{O,coarse}}}{r_{\text{O,fine}}} \tag{2-40}$$

where I_{fine0} is the fine charging current at the start of the fine phase corresponding to $V_{\text{fine0}} = V_{DD}$, $r_{\text{O,fine}}$ is the output impedance of fine current source, and β_{CLS} is the capacitive dividing factor from V_{fine} ($V_{\text{fine,coarse}}$) to V_O ($V_{\text{O,coarse}}$), as given by

$$\beta_{CLS} = \frac{C_{CLS}(C_I + C_S)}{(C_{CLS} + C_L)(C_I + C_S) + C_I C_S} \tag{2-41}$$

The dependance of I_{fine} on V_O comes from the early detection voltage margin $V_{\text{O,coarse}}$, which can be derived by

$$V_{\text{O,coarse}} = t_{\text{coarse}} \left. \frac{dV_O}{dt} \right|_{\text{coarse}} \tag{2-42}$$

The term $\left.\frac{dV_O}{dt}\right|_{\text{coarse}}$ represents the ramp-rate of V_O at the end of the coarse phase. It can be approximated as

$$\begin{aligned}\left.\frac{dV_O}{dt}\right|_{\text{coarse}} &= \frac{I_{\text{coarse}}}{C_{CLS}+C_L+\frac{C_I C_S}{C_I+C_S}} \\ &= \frac{(I_{\text{coarse0}}+\frac{V_O}{r_{\text{O,coarse}}})(C_I+C_S)}{(C_{CLS}+C_L)(C_I+C_S)+C_I C_S}\end{aligned} \tag{2-43}$$

where I_{coarse0} is the constant portion in the coarse charging current and $r_{\text{O,coarse}}$ is the output impedance of the coarse current source.

By substituting (2-41)(2-42) and (2-43) into (2-40), we have

$$\begin{aligned}I_{\text{fine}} &= I_{\text{fine0}} - \frac{t_{\text{coarse}}}{r_{\text{O,fine}}C_{CLS}}\left(I_{\text{coarse0}}+\frac{V_O}{r_{\text{O,coarse}}}\right) \\ &= \underbrace{I_{\text{fine0}} - \frac{t_{\text{coarse}}}{r_{\text{O,fine}}C_{CLS}}I_{\text{coarse0}}}_{V_O\text{-independent}} - \underbrace{\frac{V_O}{r_{\text{O,fine}}}\left(\frac{r_{\text{O,coarse}}C_{CLS}}{t_{\text{coarse}}}\right)^{-1}}_{V_O\text{-dependent}}\end{aligned} \tag{2-44}$$

The V_O-dependent item in (2-44) reveals that, with the aid of the CLS operation the equivalent output impedance of the fine current source is boosted to

$$r_{\text{O,fine,CLS}} = r_{\text{O,fine}}\frac{r_{\text{O,coarse}}C_{CLS}}{t_{\text{coarse}}} \tag{2-45}$$

Equation (2-45) shows the positive correlation between the value of C_{CLS} and the ramp-rate linearity during the fine phase charge-transfer. For example, with $r_{\text{O,coarse}} = 1\text{M}\Omega$, $t_{\text{coarse}} = 10\text{ns}$ and $C_{CLS} = 200\text{fF}$, the output impedance of the fine current source can be enhanced by 20 times, or 26dB. This improvement is obtained at the cost of extra energy consumption on the charging/discharging of the level-shifting capacitor as well as a slower operation speed. Therefore, from the design perspective, the choice of C_{CLS} is a matter of balancing the circuit linearity and the overall energy-efficiency.

The CLS technique also brings an attractive side benefit. Because of the fact that V_{fine} is level-shifted to a small range closed to V_{DD}, the voltage headroom of the fine current source is significantly enlarged, which is compatible with some traditional impedance boosting techniques, such as transistor cascoding. This feature allows for further improvements in the charge-transfer linearity of CLS-assisted ZCB integrators, which are nevertheless almost no-cost[8]. A detailed design example will be given in Chapter 5.

2-6 Summary

In this chapter, the concept and design concerns of zero-crossing based circuits for use in switched-capacitor integrators have been introduced. By replacing the OTAs in conventional switched-capacitor integrators with zero-crossing detectors and gated current sources, ZCB designs gain a variety of attractive characteristics, such as compatibility with the continuous down-scaling CMOS technology, and the amenability to low supply operation.

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[8] If any, extra biasing circuitry is required.

A design-oriented noise analysis of ZCB circuits has been presented. It contains an intensive quantitative description of the thermal noise in zero-crossing detectors, which is not necessarily stationary and a special time-domain analysis method is required. Besides noise, the sources of offset and non-linearity in ZCB circuits have also been discussed. The offset is mainly generated from the finite response delay of zero-crossing detectors. The ramp-rate variation due to finite current source output impedance and the voltage drop across the switches contribute to the non-linearity during the charge-transfer.

The prior applications of ZCB integrator in $\Delta\Sigma$ ADCs have been briefly reviewed. As proved by these works, the non-linearity issue and the poor energy-efficiency have become the main bottleneck of ZCB circuits, especially when the absolute data conversion accuracy is of concern. To address these problems, two types of advanced circuit techniques, the early-threshold detection and the correlated level shifting, have both been briefly introduced. They will be employed in the prototype design to demonstrate their effectiveness.

Chapter 3

Energy-Efficient Inverter-Based Zero-Crossing Detector

The energy-efficiency of the zero-crossing detector (ZCD) is of special concern as it usually dominates the power dissipation of zero-crossing based switched-capacitor circuits [21]. Conventional designs, such as [23], [42] and [43], utilized zero-crossing detectors consisting of single or multiple stages of transconductance amplifiers in open-loop configuration, which usually leads to considerable static power consumption. As an alternative structure, a new class of zero-crossing detectors based on an auto-zeroed CMOS inverter is described in this chapter. Compared with its OTA-based equivalents, the proposed technique reveals a significant advantage in energy-efficiency even with lower supply voltages.

The chapter starts with an introduction to the motivation of using the CMOS inverters as an analog functioning element. After a concise overview of different types of inverter-based analog circuits, the operation principle of the inverter-based zero-crossing detector is presented. Furthermore, special attention is paid to the non-ideal effects caused by the parasitic capacitors and the poor ability of CMOS inverters to reject the power supply noise.

3-1 Motivation

Although the CMOS inverter is normally used as the basic logic element in digital circuits [17], it can also be considered as a simple amplifier [3] when both PMOS and NMOS transistors are turned on, as shown in Figure 3-1(a). Figure 3-1 (b) plots the relative variation of the DC gain and the gain-bandwidth product (GBW) of CMOS inverters as a function of the static biasing current I_0. When I_0 is smaller than the subthreshold current I_S, both MOSFETs operate in weak inversion; otherwise they operate in strong inversion. It is shown that a CMOS inverter provides a higher DC gain when biased in weak inversion, but has a faster operation speed (larger GBW) when working in strong inversion.

This phenomenon can be explained by the variation of MOSFET current-efficiency in different operation modes. The MOSFET current-efficiency is defined as the ratio of the

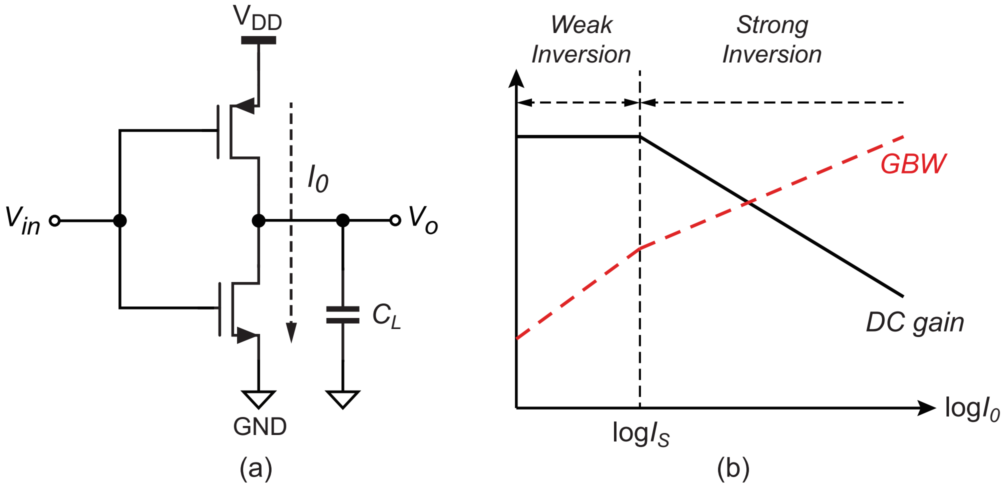

Figure 3-1: (a) Basic CMOS inverter topology (b) The DC gain and gain-bandwidth product (GBW) of CMOS inverters in static mode as a function of the biasing current I_0 [3]

transconductance g_{m} to the drain-source current I_{DS}. Given the fact that the output impedance of MOSFETs (r_O) is inversely proportional to I_{DS} in both weak and strong inversion regions, the MOSFET current-efficiency dominates the amplifier DC gain as

$$A_0 = g_{\mathrm{m}} r_O \propto \frac{g_{\mathrm{m}}}{I_{DS}} \tag{3-1}$$

Figure 3-2 plots the current efficiency versus the normalized I_{DS} with respect to the subthreshold current I_S [48]. In the weak inversion region, this ratio can be approximated by $\frac{q}{nkT}$, where n is a biasing-dependent process parameter. Normally the ratio value is around $25\mathrm{V}^{-1}$. In the strong inversion region, the current-efficiency is inversely proportional to the overdrive voltage ($V_{\mathrm{gs}} - V_{\mathrm{th}}$) and hence decreases dramatically, with a common value around

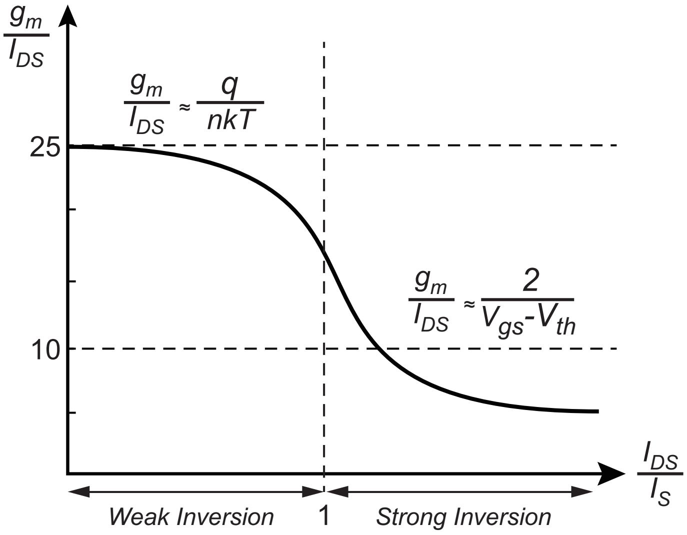

Figure 3-2: The current-efficiency of MOSFETs in weak inversion and strong inversion

$10\mathrm{V}^{-1}$. This fact suggests that it is beneficial to move the MOSFET operation region towards deep weak inversion for the purpose of improving the energy-efficiency. However, this benefit is limited by the reduction of GBW due to the decreased biasing current and hence smaller carrier density in the channels.

In order to obtain both high DC gain and fast operation speed, the CMOS inverter should be biased at the boundary between the weak and strong inversion regions [7]. The bias point of a static CMOS inverter can be self-determined with the unit-gain configuration, as shown in Figure 3-3. In the static state, $I_{\mathrm{op}} = I_{\mathrm{on}}$, i.e. V_{c} is the threshold voltage of the CMOS inverter. According to [39], V_{c} is given by

$$V_{\mathrm{c}} = \frac{V_{\mathrm{tn}} + \sqrt{\frac{\beta_{\mathrm{p}}}{\beta_{\mathrm{n}}}}\left(V_{DD} - |V_{\mathrm{tp}}|\right)}{1 + \sqrt{\frac{\beta_{\mathrm{P}}}{\beta_{\mathrm{n}}}}} \tag{3-2}$$

where V_{tp} and V_{tn} are threshold voltages of PMOS and NMOS transistors, and

$$\begin{cases} \beta_{\mathrm{n}} & = \dfrac{\mu_n C_{OX} W_n}{L_n} \\ \beta_{\mathrm{p}} & = \dfrac{\mu_p C_{OX} W_p}{L_p} \end{cases} \tag{3-3}$$

The boundary condition between weak and strong inversion regions is $V_{\mathrm{c}} \approx V_{\mathrm{tn}}$ and $V_{\mathrm{c}} \approx V_{DD} - |V_{\mathrm{tp}}|$, leading to

$$V_{DD,\mathrm{opt}} \approx |V_{\mathrm{tp}}| + V_{\mathrm{tn}} \tag{3-4}$$

where $V_{DD,\mathrm{opt}}$ is the optimal value of the supply voltage.

Equation (3-4) reveals a sweet benefit of inverter-based transconductance amplifiers: the amenability to low supply opeation. For example, in a $0.18\mu m$ standard CMOS process, the

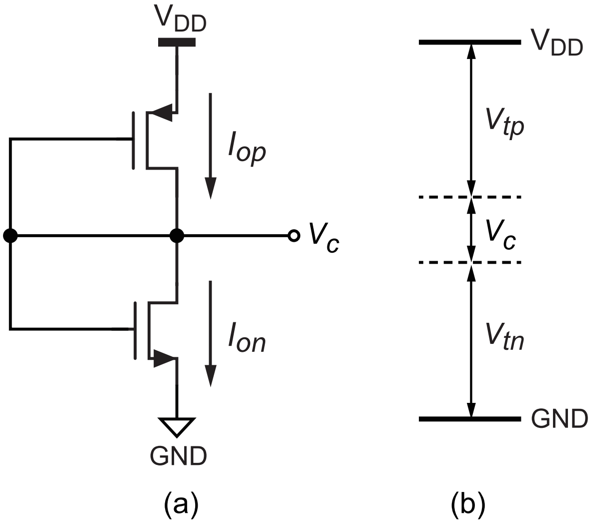

Figure 3-3: (a) Inverter in unit-gain configuration (b) Voltage scale

sum of NMOS and PMOS threshold voltages is around 0.9V~1V, which is far smaller than the typical 1.8V analog supply at this technology node [49]. What's more, since both transistors can operate in deep weak inversion (sub-threshold mode), the supply voltage can be even further down-scaled as long as the speed sacrifices can be tolerated. The only imperfection is that $V_{DD,\mathrm{opt}}$ does not scale linearly with the technology feature size [39].

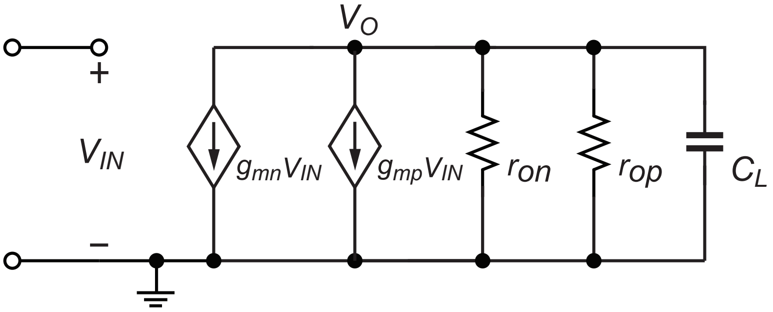

Figure 3-4: Small-signal model of an inverter-based transconductance amplifier in the steady-state

Another advantage of inverter-based transconductance amplifiers is the doubled current-efficiency. Figure 3-4 shows the small-signal model of an inverter-based transconductance amplifier in the steady-state. As interpreted by the figure, the overall transconductance of of the steady-state inverter is contributed by both PMOS and NMOS transistors, as given by

$$g_{\mathrm{m}} = g_{\mathrm{mp}} + g_{\mathrm{mn}} \approx 2g_{\mathrm{mn}} \tag{3-5}$$

Thus, the current-efficiency g_{m}/I_{DS} of a steady-state inverter-based amplifier is roughly two times of that of conventional opamps whose input stages only consist of single type of MOSFETs.

All the above discussions are based on the small-signal model of steady-state inverter-based amplifier. For large signals, a CMOS inverter behaves in a push-pull fashion [17]. As an analog amplifier, the inverter operates in the class-AB mode when $V_{DD} \geqslant V_{DD,\mathrm{opt}}$, while it operates as a class-C amplifier when $V_{DD} < V_{DD,\mathrm{opt}}$ [7]. If the input signal has a relatively slow changing-rate, the biasing condition of the inverter can vary with the signal dynamically. The current flowing in the inverter only reaches its maximum value in the steady-state when $V_{\mathrm{in}} \approx V_C$, where both transistors operate in the weak inversion region; otherwise the current is small as only one transistor is biased in the strong inversion region while another one is cut off. As such, the use of the static current can be concentrated around the instant when the inverter-based amplifier is biased in its quasi-steady-state condition, thus saving the static power consumption. This dynamic biasing capacity is particularly beneficial when the inverter is used as the preamplifier in zero-crossing detectors, as will be further discussed in Section 3-4.

To conclude, an inverter-based transconductance amplifier has the following advantages:

- Excellent compatibility to low supply circumstance. With a relaxed requirement on the operation speed, the amplifier can operate and provide sufficient DC gain even if the transistors are not fully turned on, thus eliminating the supply voltage limitation of conventional opamps;

- High current efficiency thanks to the weak inversion operation and the dual types of input transistors;
- Inherent dynamic biasing capacity when operating in the large-swing manner.

Because of all the above charming characteristics, inverter-based analog circuits have become an attractive candidate to perform the analog functions in energy-efficiency oriented designs [50][6][7]. Similar topologies can also be applied to zero-crossing detectors to replace the power-hungry cascaded amplifiers.

3-2 Control of Common-mode Voltage

The control of the common-mode voltage is an inherent problem of inverter-based analog circuits due to their singled-ended nature. Generally, there are two major types of circuit techniques that can be used to resolve this problem.

Replica Reference Inverter

The first method is to generate a reference voltage using a replica inverter in the unit-gain configuration, as shown in Figure 3-5(a). The simplicity of both topology and operation make this method suited for use in high-speed applications, such as in [51]. However, it is not energy-efficient for SC circuits as the static biasing current in the reference inverter consumes power constantly. What's worse, as revealed in (3-2) and (3-3), the reference voltage V_c suffers from the inevitable PVT variations, which makes the common-mode voltage unstable against different manufacturing and operating conditions.

Auto-zeroed Inverter

The second method is to auto-zero the inverter-based amplifier, as shown in Figure 3-5(b). With the addition of level-shift capacitor C_C and switches S_1, S_2 and S_3, the common-mode voltage can be moved to a desired level V_{CM} that is independent of the environmental conditions. When S_2 is closed, S_3 is open and S_1 is connected to the required common-mode voltage, the offset difference between V_{CM} and the unknown threshold voltage V_c is sampled on the capacitor C_C; this voltage is then subtracted from the input voltage V_in when S_2 is open, S_3 is closed and S_1 is switched to V_in, thus cancelling the effect of V_c. As no extra static biasing circuit is needed and hence no static power dissipation is consumed, this structure is preferred for low power designs. Furthermore, the auto-zeroing operation also brings a bonus to the noise performance, as will be explained in Section 3-3.

3-3 Overview of Inverter-Based Analog Circuitry

The inverter-based analog circuitry is by no means a brand-new topic. As early as in the 1980s, when the CMOS technology scaling had not yet entered the sub-micrometer range, a class-AB inverter-based amplifier had been proposed in [4] for use in low power audio-band

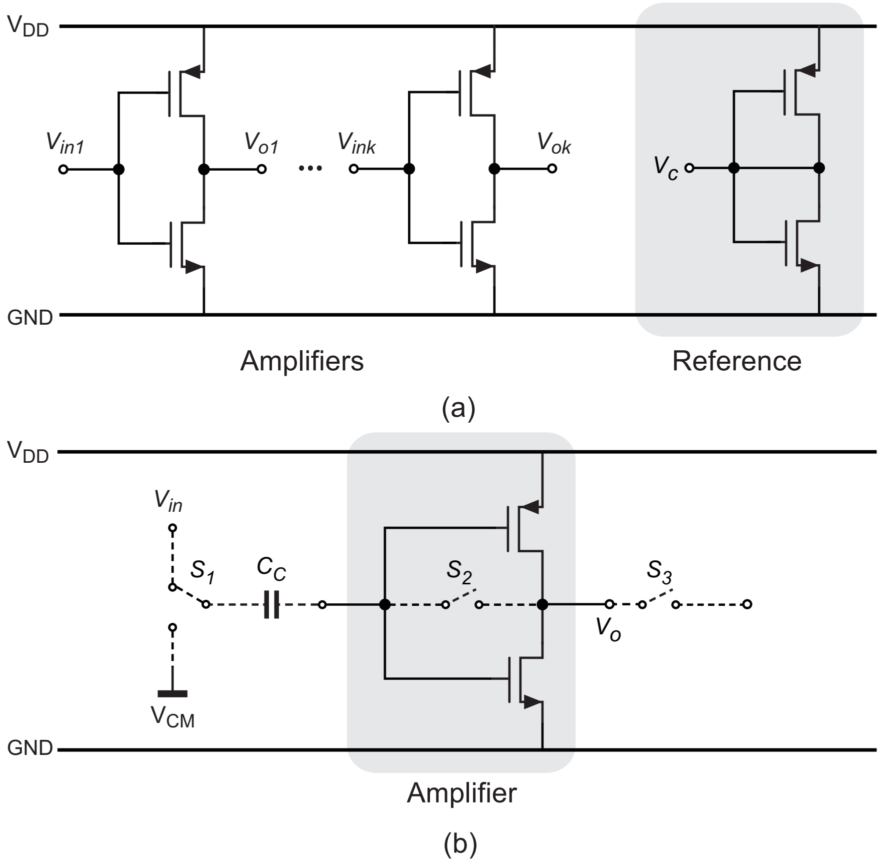

Figure 3-5: Different common-mode voltage control schemes in inverter-based analog circuits [4] (a) Replica inverters in unit-gain configuration for reference voltage generation (b) Auto-zeroed inverter-amplifier

switched-capacitor filters. Later on, cascoded structures were introduced in inverter-based amplifiers to improve the DC gain [5], as shown in Figure 3-6(a). In [51], a differential inverter-based transconductance element was developed for the implementation of g_m-C integrators in very-high-frequency (VHF) analog filters.

Recently, inverter-based amplifiers have attracted more and more attentions from ADC designers. In [6], multiple stages of cascaded inverters with frequency compensation were utilized as an opamp cell in a $\Delta\Sigma$ modulator, as illustrated in Figure 3-6(b). As a more aggressive attempt, the $\Delta\Sigma$ ADC family presented in [7] made use of single-stage auto-zeroed inverters as the active feedback elements in switched-capacitor circuits. Both works proved the significant energy-efficiency advantage of inverter-based SC circuits over conventional OTA-based designs.

The CMOS inverter can also perform as a threshold comparator, which is essentially an open-loop amplifier. Its first application appeared in [52], where auto-zeroed inverters were utilized as the comparator stages in a high-speed full-flash ADC. The auto-zeroing operation is used to cancel the threshold offset and to ensure an accurate voltage reference for the comparisons. That is, however, not always necessary for wide-band or low-resolution digitizations in which the requirement on the transfer linearity is not crucial. Consequently,

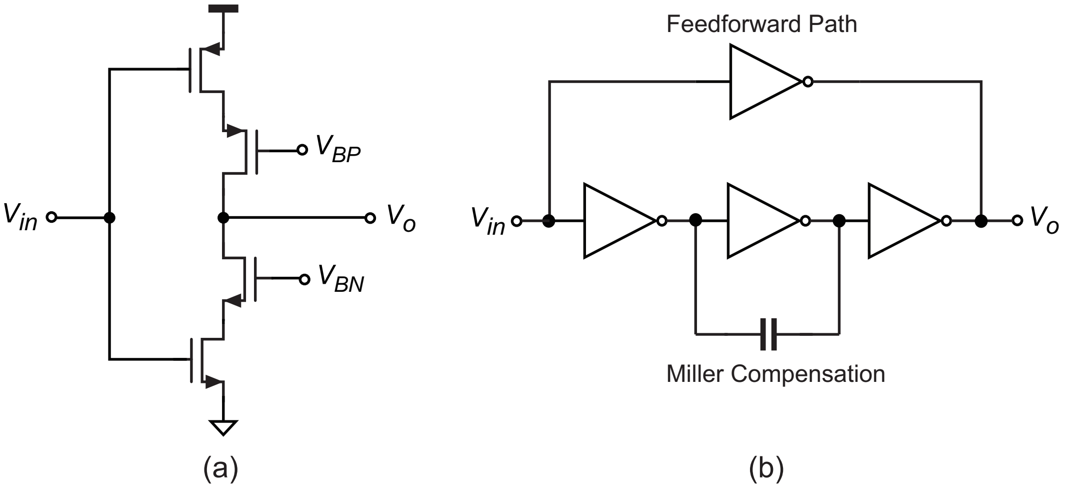

Figure 3-6: Some modified inverter-based amplifier structures: (a) Cascode inverter-amplifier [5] (b) Cascaded freqeuncy-compensated inverter-amplifier [6]

a non-offset-cancelled inverter architecture was adopted in some follow-up designs, such as the comparator columns in flash ADCs [53] [50] and the multi-bit quantization comparator in ΔΣ ADCs [6]. In the latter example, a 4-stage cascaded inverter chain was used to enhance the gain. By exchanging the accuracy with the circuit simplicity, the operation bandwidth of the comparator can be improved.

In this work, the inverter-based architecture is applied to the implementation of the zero-crossing detector, including both the low noise preamplifer and the wide-band crossing detector (see Figure 2-5(a)). A more detailed description is given in the next section.

3-4 Inverter-Based Zero-Crossing Detector

3-4-1 Topology

As shown in Figure 2-5, a zero-crossing detector consists of a low noise preamaplifier and a wide-band crossing detector. Both modules can be implemented with the CMOS inverter topology, but in different ways:

- As has been discussed in Chapter 2, an accurate and stable virtual-ground condition is of great importance for the overall linearity of the ZCB circuits. Therefore, the utilization of the auto-zeroed technique is necessary for the front-end low-noise preamplifier. In addition, to limit the noise bandwidth an explicit capacitor C_{int} is usually added at the load of the preamplifier;

- The wide-band crossing detector, on the contrary, is ideally a pull-push device which provides logic level outputs and only consumes dynamic power of

$$P_{\text{dyn}} = V_{DD}^2 C_L f \tag{3-6}$$

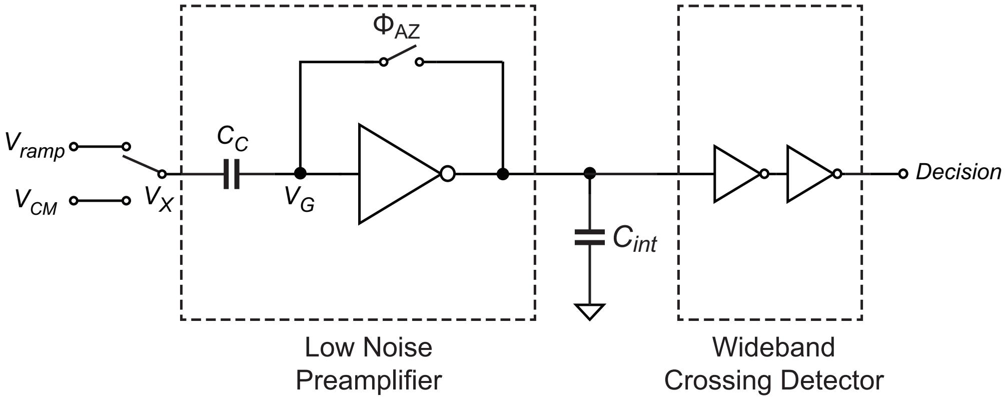

Figure 3-7: Topology of simplified inverter-based zero-crossing detector

where C_L is the loading capacitance at the output of the zero-crossing detector and f is the operation frequency. Accordingly, a simple inverter chain without any offset-cancellation serves the purpose. To minimize the signal propagation delay, the number of stages in the inverter chain should be determined according to the loading condition. Generally, a two-stage chain is adequate for this task as the output of the zero-crossing detector usually feeds to logic gates with small sizes.

Figure 3-7 illustrates the primary topology of the proposed inverter-based zero-crossing detector. Its operation principle is analyzed in the following sub-section.

3-4-2 Operational Principle

The inverter-based zero-crossing detector operates in a discrete-time manner, as depicted in Figure 3-8.

During phase Φ_{AZ}, the inverter in the preamplifier is shorted to form a unity-gain configuration. Thus, the voltage difference between the virtual ground level V_{CM} and the inverter threshold voltage V_{c} ($V_{OFF} = V_{CM} - V_{\mathrm{c}}$ [7]) is sampled on the capacitor C_C. During phase $\overline{\Phi_{AZ}}$, C_C is left floating and a voltage ramp is added on the virtual ground node V_X. When the virtual ground condition on V_X is achieved, the voltage on the node V_G should equal V_{c} due to the level-shifting effect of C_C. Upon that moment the inverter chain in the wide-band detector is triggered to make a crossing-decision and stop the voltage ramping.

During Φ_{AZ}, the zero-crossing detector stays idle. To be time-efficient the auto-zeroing can be performed simultaneously with the switched-capacitor sampling operation (Φ_1), as shown in Figure 3-8(c). Furthermore, the duty cycle of Φ_{AZ} need not be 50% as long as the auto-zeroing settling time is shorter than the length of the sampling phase[1], which is a common situation in low-speed I&M applications. The settling time constant of V_G during the auto-zeroing phase is inversely proportional to the effective transconductance of the unit-gain inverter, as given by:

$$\tau_{AZ} = \frac{C_C + C_{\mathrm{int}}}{g_{\mathrm{mn}} + g_{\mathrm{mp}}} \approx \frac{C_C + C_{\mathrm{int}}}{2g_{\mathrm{mn}}} \tag{3-7}$$

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[1] It could also be designed in the other way around, i.e. using a slow-settling process to reduce the noise-folding introduced by the auto-zeroing operation [7].

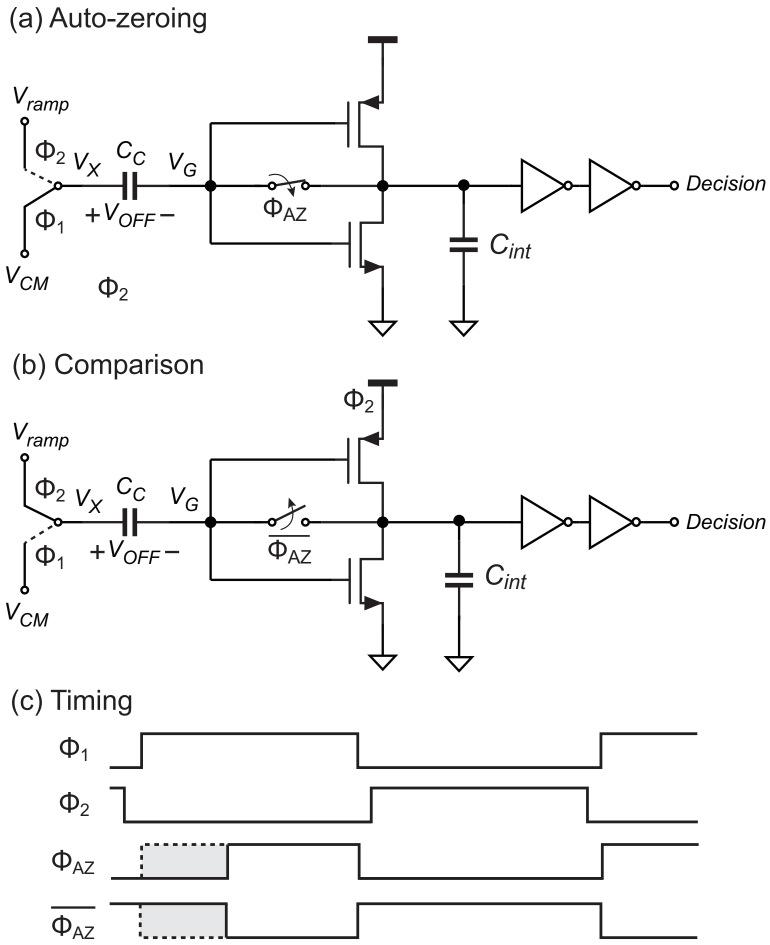
(a) Auto-zeroing
V_{ramp}
Φ_2
V_X
C_C
V_G
Φ_1
$+V_{OFF}-$
Φ_{AZ}
V_{CM}
Φ_2
C_{int}
Decision
(b) Comparison
Φ_2
V_{ramp}
Φ_2
V_X
C_C
V_G
Φ_1
$+V_{OFF}-$
$\overline{\Phi_{AZ}}$
V_{CM}
C_{int}
Decision
(c) Timing
Φ_1
Φ_2
Φ_{AZ}
$\overline{\Phi_{AZ}}$

Figure 3-8: Operation principle of auto-zeroed inverter

For example, with $g_{\mathrm{mn}} \approx 50\mu\mathrm{S}$, $C_C = 2\mathrm{pF}$ and $C_{\mathrm{int}} = 500\mathrm{fF}$, the minimal time required for auto-zeroing operation can be estimated as:

$$T_{AZ} \geqslant 10\tau_{AZ} \approx 25\mathrm{ns} \tag{3-8}$$

which is equivalent to an auto-zeroing frequency of 20MHz. This is relatively fast compared to the data sampling rate in traditional I&M applications, which is normally slower than 1MS/s [54][55][56].

The optimization of the auto-zeroing time is meaningful for the reduction of the unnecessary static power consumption caused by the auto-zeroed inverter. The multi-phase characteristics of the zero-crossing based charge-transfer enable the smart control of the auto-zeroing duty cycle, especially in self-timed implementations, as will be shown in Chapter 4 and Chapter 5.

Figure 3-9 shows the changing output voltage and biasing current of a typical inverter-based preamplifier during auto-zeroing and unidirectional charge-transfer phase. It's assumed that the preamplifier is deliberately designed to operate in the "sweet corner" that has been indicated in Figure 2-6 and the supply voltage is chosen to be $V_{DD,\mathrm{opt}}$ as presented in (3-4).

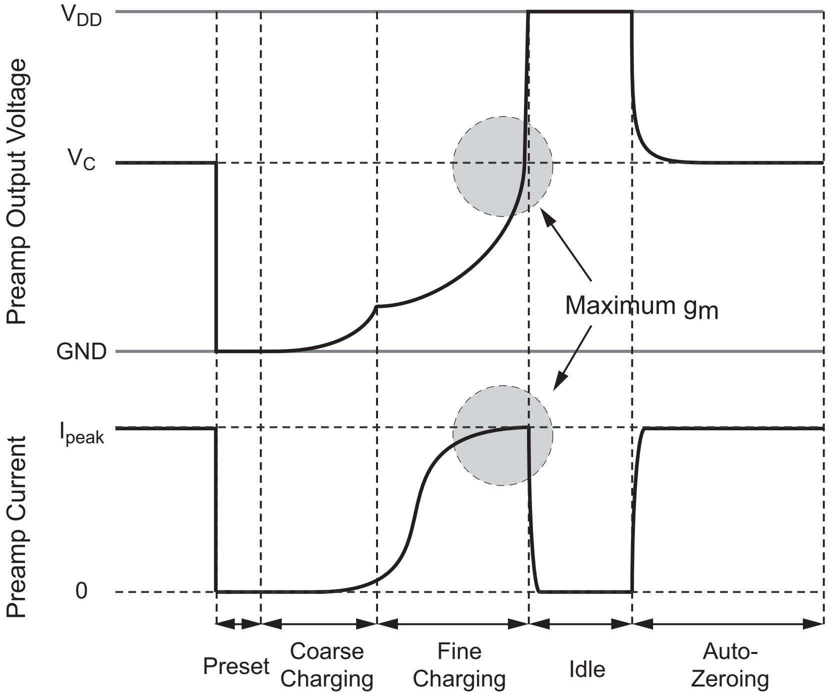

Figure 3-9: (a)Preamplifier output voltage (b) Current flowing in the preamplifier inverter

When the preamplifier output voltage is still far away from the threshold voltage (V_C)[2], the current flowing in the CMOS inverter is much smaller than the short circuit current (I_{peak}), resulting in a small overall transconductance (g_{m}). As the preamplifier output voltage approaches V_C in an integrator-like fashion, the current increases gradually and finally reaches I_{peak} around the zero-crossing instant. That is to say, the g_{m} of the inverter-based transconductance amplifier is only maximized when it is needed most. As has been interpreted in Section 3-1, the above inherent dynamic biasing capacity makes the inverter-based preamplifer more power-efficient than traditional ones based on class-A amplifiers. This mechanism is a bit similar with the capacitor-coupled dynamic biasing technique that has been used in opamp-based ZCDs [2], but possesses an extra beauty that no auxiliary circuits is required.

3-4-3 Further Improvement: Dynamic Power-Down

The energy-efficiency of inverter-based zero-crossing detectors can be further improved by introducing dynamic power-down. Figure 3-10 shows the circuit-level architecture of a dynamically powered-down ZCD and the corresponding timing diagram.

Since the wide-band detectors are not functioning during the sampling (auto-zeroing) phase, they can be powered down during Φ_1 to save the possible power dissipation caused by the non-logical-level voltage of V_{int}. What's more, it's also feasible to shut down the preamplifier in a portion of Φ_1 as it does not necessarily need to be auto-zeroed throughout the entire sampling phase. As such, the only static power consumption contributed by the

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[2] In the entire coarse charging phase and at the beginning of the fine charging phase.

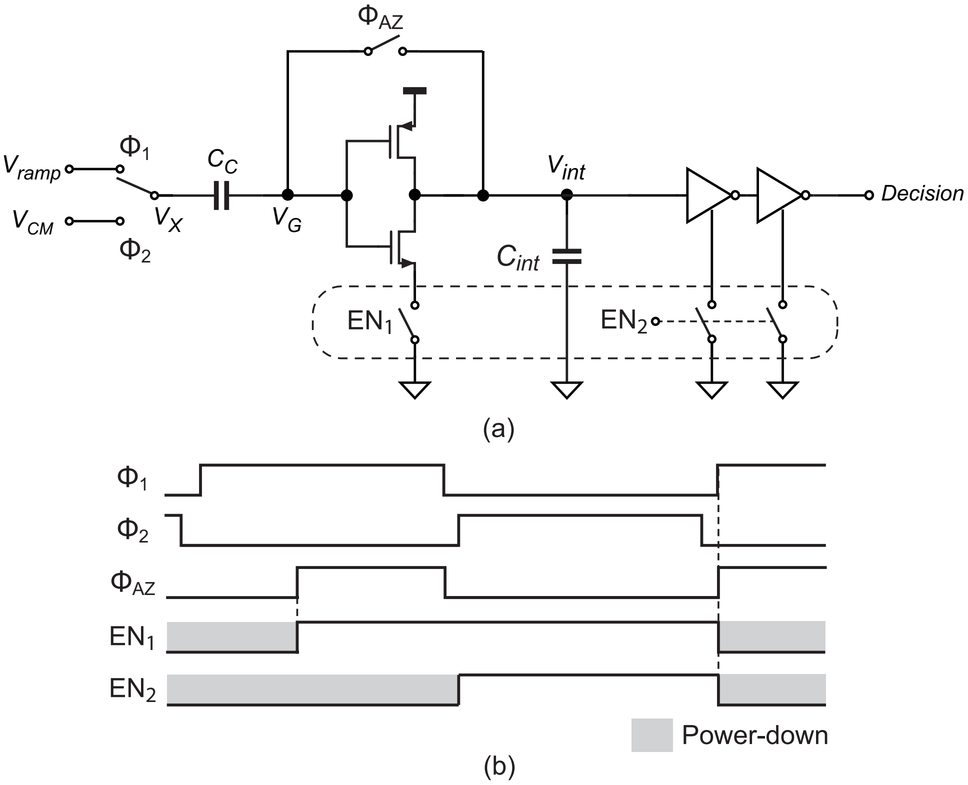

Figure 3-10: (a)Implementation of dynamic powered-down ZCD (b) Timing diagram of dynamic power-down

ZCD during Φ_1 comes from the auto-zeroing operation, whose duration time is also controlled as aforementioned.

The power-down operation can be realized by connecting a MOSFET switch in series with the inverter, as shown in Figure 3-10(a).

3-5 Non-ideal Effects

Silicon-based integrated circuits are by no means perfect but always suffer from a variety of non-ideal effects, such as interference noise and parasitics. For zero-crossing detectors implemented with auto-zeroed CMOS inverters, the major problem comes from the parasitic capacitors and the power supply noise. Without careful design considerations, these problems are likely to constrain the performance of ZCB integrators. Therefore, special attention is paid to these issues in this section.

3-5-1 Parasitic Capacitors

Figure 3-11 illustrates the distribution of parasitic capacitors in an inverter-based ZCB integrator. The one at the virtual ground node, C_{p1}, is caused by the joint parasitic capacitance of C_S, C_I and the connected MOSFET switches. The other one, C_{p2}, mainly comes from

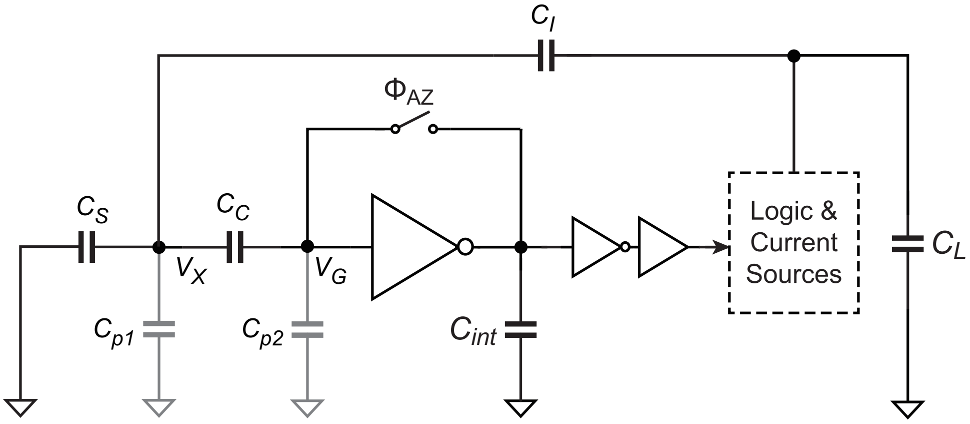

Figure 3-11: Parasitic capacitors in inverter-based ZCB integrator

the overlap parasitic capacitance at the gates of the inverter transistors (PMOS and NMOS), as well as the parasitic capacitance associated with C_C. The existence of C_{p2} changes the impedance condition at the inverter input, making C_C no longer floating during the charge-transfer process. As a result, the voltage overshoots at nodes V_X and V_G are no longer identical. The series connection of C_C and C_{p2} forms a voltage divider, giving:

$$\Delta V_{OVG} = \frac{C_C}{C_C + C_{\mathrm{p2}}} \Delta V_{OVX} \tag{3-9}$$

The effect of C_{p1} and C_{p2} on the charge-transfer accuracy can be investigated via the charge conservation on V_X, as follows:

$$\begin{aligned}&(V_{CM} - V_{\mathrm{in}})C_S + V_{\mathrm{CM}}C_{\mathrm{p1}} + (V_{CM} - V_{G0})C_C - Q_{\mathrm{n}} \\ &= (V_{CM} - \Delta V_{OVX})C_{\mathrm{p1}} + \Big[(V_{CM} - \Delta V_{OVX}) - (V_{G0} - \Delta V_{OVG})\Big]C_C - \Delta V_{OVX}C_S - Q_{\mathrm{n+1}}\end{aligned} \tag{3-10}$$

where Q_{n} and $Q_{\mathrm{n+1}}$ represent the stored charge on C_I in the n-th and the (n+1)-th cycles, respectively.

By substituting (3-9) into (3-10), the amount of charge that is converted to the integration capacitor in each cycle can be derived as:

$$Q_{\mathrm{n+1}} - Q_{\mathrm{n}} = \underbrace{\Big(V_{\mathrm{in}} - V_{CM} - \Delta V_{OVX}\Big)C_S}_{\text{Original}} - \underbrace{\Delta V_{OVX}\Big(C_{\mathrm{p1}} + \frac{C_{\mathrm{p2}}C_C}{C_{\mathrm{p2}} + C_C}\Big)}_{\text{Parasitic capacitor induced}} \tag{3-11}$$

where the first term on the right-hand side of the equation represents the transferred charge in each cycle including the original error charge described in (2-30) and (2-31), and the second term represents the error charge introduced by the parasitic capacitors.

Thus, when taking the impacts of parasitic capacitors into account, the effective input-referred error voltage turns out to be

$$\Delta V'_{OVX} = \Delta V_{OVX}\Big[1 + \frac{C_{\mathrm{p1}}}{C_S} + \frac{C_{\mathrm{p2}}C_C}{(C_{\mathrm{p2}} + C_C)C_S}\Big] \tag{3-12}$$

Expression (3-12) reveals the fact that the original virtual ground overshoot is magnified by a parasitic-associated factor due to the existence of C_{p1} and C_{p2}. This effect can be non-negligible in energy-constrained designs where the sampling capacitors are usually aggressively downsized. For example, with $C_S = 0.5\mathrm{pF}$, $C_C = 2\mathrm{pF}$, $C_{\mathrm{p1}} = 30\mathrm{fF}$ and $C_{\mathrm{p2}} = 100\mathrm{fF}$[3], the increment of ΔV_{OVX} caused by parasitic capacitors is around 25%. Particularly, the magnification of the signal-dependent portion in ΔV_{OVX}, which has been discussed in Section 2-3, deteriorates the non-linearity issue of ZCB integrators.

To alleviate the above problem, a careful control on the parasitic capacitance is required. The value of C_{p1} is mainly dependant on the process parameters and the layout methodology, while that of C_{p2} is more revelent to the circuit design strategy. As mentioned in Chapter 2, the dimensions of ZCD input transistors are preferred to be large in the consideration of noise performance. This is, however, conflicting with the minimization of C_{p2} for the purpose of preventing linearity deterioration. Consequently, it's necessary to strike a balance between noise and linearity on the sizing choice of inverter input transistors.

3-5-2 Power Supply Noise Rejection

Power supply noise is normally regarded as the most critical interference noise source for inverter-based analog circuits due to the poor power supply rejection ratio (PSRR) of the inverter structure [7]. As depicted in Figure 3-12, an inverter-based transconductance amplifier operating in the steady-state can be approximatively modeled as a resistor divider, and hence its intrinsic PSRR is only about 6dB. This feature does restrict the application of inverters in many analog circuits where a clean power supply is unavailable or costly [48] [4].

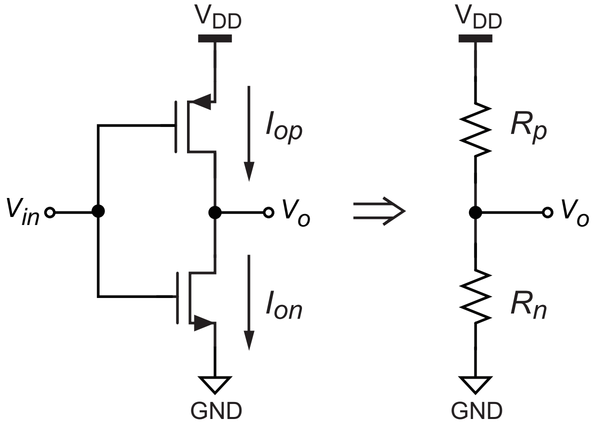

Figure 3-12: Estimation of power supply rejection ratio of steady-state inverter-based amplifier ($R_{\mathrm{p}} \approx R_{\mathrm{n}}$)

Fortunately, the power supply noise rejection ability of ZCB integrators utilizing inverter-based ZCDs and the aforementioned CLS technique can be, to some extent, rescued by the following mechanisms:

---

[3] The parasitic capacitor values are estimated on the basis of NXP 0.16μm CMOS technology [49].

[4] To obtain clean power supply, the traditional solution is either using low noise voltage regulators or applying aggressive on-chip supply bypassing. However, the former solution increases the system complexity, while the latter one is usually area-hungry.

- *Auto-zeroing of the inverter-based preamplifier in the ZCD.*

  As has been discussed in Section 2-2-2, the auto-zeroing technique is effective in cancelling low-frequency noise. This is also valid for the elimination of the noise on the power supply line [7], as the bandwidth of power supply noise can be easily limited to lower than 100kHz by the filtering effect of bypassing capacitors [57];

- *Correlated level shifting.*

  The utilization of correlated level shifting technique provides a supplementary improvement to the overall PSRR of a ZCB integrator. This fact has been theoretically analyzed in [47]. As an intuitive interpretation, the correlated level shifting capacitor (see Figure 2-17) establishes a capacitive isolation between the integrator output and the fine current source, thus partially obstructing the possible output disturbance from low-frequency power supply noise. Therefore, a smaller correlated level shifting capacitor is advantageous for improving the PSRR, but simultaneously degrades the linearity performance for the reason discussed in Section 2-5-2.

- *Noise shaping in the $\Delta\Sigma$ modulator.*

  The impact of power supply noise can be further attenuated when the ZCB integrator is adopted in $\Delta\Sigma$ modulators [7][58]. As a brief proof, consider the classical second-order Boser-Wooley $\Delta\Sigma$ modulator in Figure 3-13. The power supply noise (P_{n1}, P_{n2}) is injected into the $\Delta\Sigma$ loop-filter at the output of the integrators, thus enjoying a similar noise-shaping characteristic as the quantization noise (Q_{n}). Specifically, P_{n1} is first-order shaped to the high frequency range (20dB/dec), while P_{n2} is shaped with the second order (40dB/dec). More generally, in a k-th order $\Delta\Sigma$ modulator containing k integrators, the power supply noise in the j-th ($0 < j \leqslant k$) integrator is suppressed by a j-th order noise-shaping. As is the same with quantization noise, the attenuation ratio of in-band power supply noise is proportional to the oversampling ratio (OSR) [59]. This feature is particularly favorable for applications of incremental $\Delta\Sigma$ ADCs because of their feasibility for ultra aggressive oversampling [11], as will be explained in Chapter 4. An OSR of 500 ($10^{2.7}$), for instance, can bring about a PSRR increment of at least 40dB to a first-stage integrator with unity scaling coefficient [7].

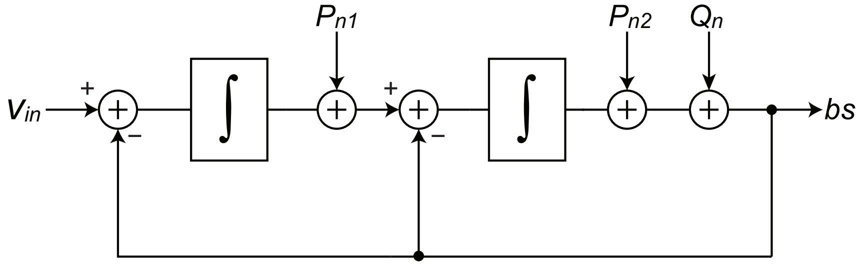

Figure 3-13: Power supply noise in a second-order Boser-Wooley $\Delta\Sigma$ modulator [7]

- *Differential architecture.*

  When applied in pseudo/fully-differential structures, the power supply rejection ability of ZCB integrators only depends on the circuit mismatches [7]. With a well mismatch control by means of good layout engineering, the impact of power supply noise can be significantly compressed.

The cooperation of the above mechanisms improves the overall power supply noise immunity of ZCB integrators. With the aid of the periodical steady-state (PSS) and the periodical transfer function (PXF) analysis in SpectreRF [60], the effectiveness of the auto-zeroing and the CLS technique on the power supply noise can be readily demonstrated. Figure 3-14 shows the simulated frequency response of PSRR of a single-ended CLS-assisted inverter-based ZCB integrator. As can be seen from the figure, the combined effects of the auto-zeroing and the CLS technique increase the PSRR by more than 10dB. Besides, the PSRR gets better with a smaller correlated level shifting capacitor, which agrees with the theoretical analysis. Taking into account the additional improvement from the loop-filter noise-shaping and the differential-mode noise attenuation, the overall PSRR of the inverter-based ZCB integrator can be enhanced to around 50~60dB[5], which is adequate for most applications.

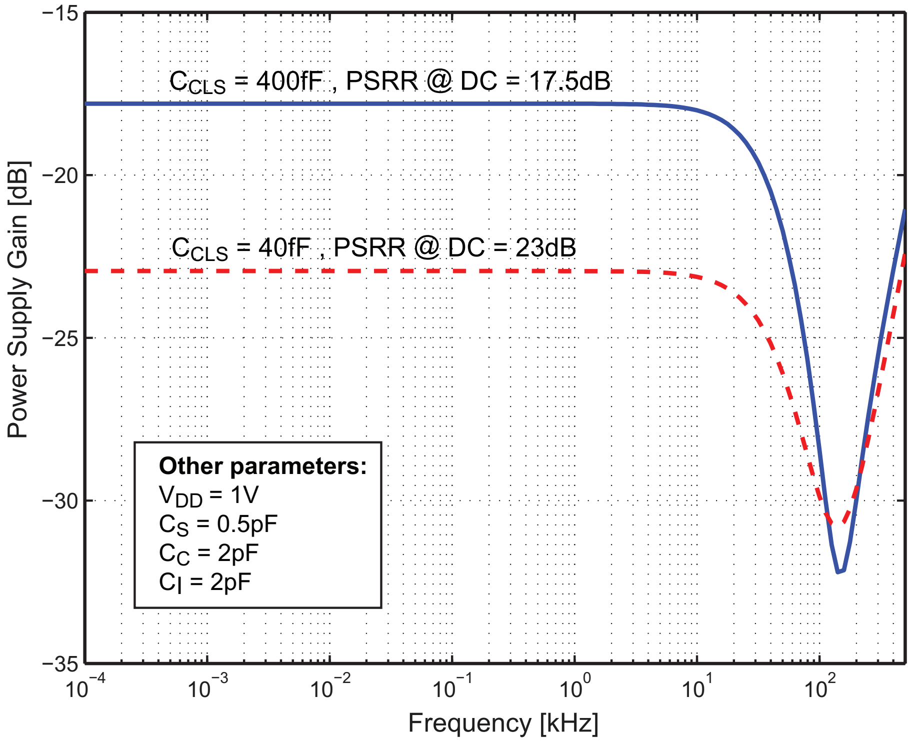

Figure 3-14: Simulated power supply gain (the inverse of PSRR in dB number) of a ZCB integrator utilizing inverter-based ZCD and CLS technique

The common ground of all the discussed mechanisms is that the poor PSRR of the simple inverter architecture is tolerated. Indeed, the intrinsic PSRR of the inverter can also be improved. This task is done by introducing a current source between the power supply and the PMOS transistor, forming a current-starved inverter [56] (Figure 3-15(a))[6]. The high output impedance of the tail current source makes the bias point of the inverter insensitive to the power supply, hence increases the associated noise immunity. Simulation

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[5] This is still a conservative estimation.

[6] Current-starved inverter is not a brand new architecture indeed. Before [56], it has been widely applied in frequency generation (VCO) or locking (PLL) [61], where it plays as a delay element.

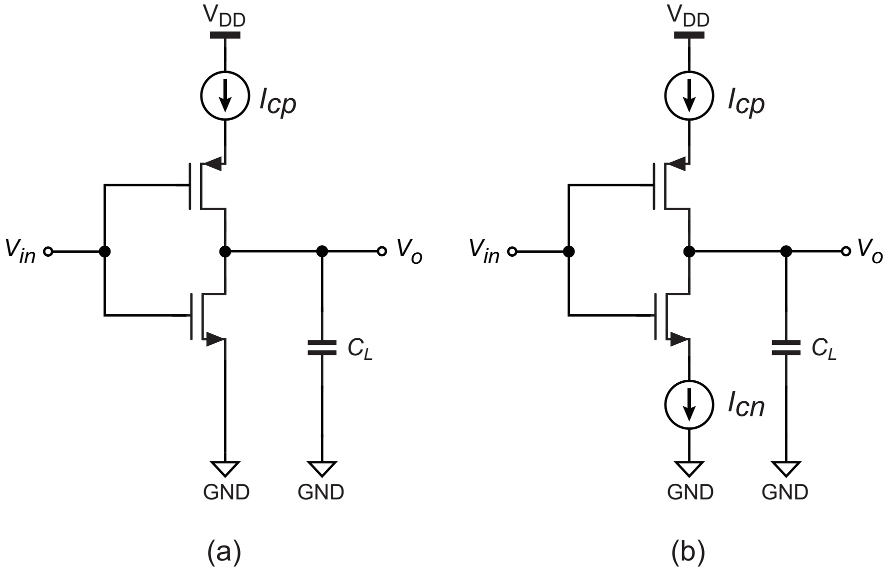

Figure 3-15: Current-starved inverter-based transconductance amplifiers

result shows that the intrinsic PSRR of a current-starved inverter can be easily boosted to above 60dB. Furthermore, another tail current source can be inserted between the NMOS transistor and the ground [62] (Figure 3-15(b)), thus suppressing the possible disturbance from the substrate noise. The drawback of the current-starving technique is the sacrifices of voltage headroom. In order to ensure the proper functioning of the tail current source, an increase of the optimal supply voltage relative to (3-4) is often required, which may degrade the low voltage amenability of inverter-based ZCDs.

3-6 Summary

This chapter has presented an energy-efficient ZCD architecture adopting CMOS inverters as the building elements. When used as an analog functioning element such as a tranconductance amplifier, the CMOS inverter displays a number of attractive properties, such as the amenability to low supply voltages, doubled current efficiency in the steady-state and inherent dynamic biasing capacity in large-signal operations. These features make the CMOS inverter an excellent candidate for many low-power low-voltage switched-capacitor applications, as has been introduced in this chapter.

The inverter-based ZCD utilizes an auto-zeroed inverter as the preamplfier, while a simple inverter chain serves as the wide-band detector. Their operation principles have been intensively described. To further improve the energy-efficiency, the inverters in both stages can be powered-down dynamically.

The inverter-based ZCD suffers from non-ideal effects caused by parasitic capacitors and the limited intrinsic PSRR of inverters. The parasitic capacitors may deteriorate the non-linearity problem of ZCB circuits described in Chapter 2, while the PSRR issue can be addressed by a series of auxiliary mechanisms or adopting the current-starving technique. Some simulation results have also been presented to demonstrate their effectiveness.

Chapter 4

Self-timed Incremental ΔΣ ADC

This chapter discusses the design of the self-timed incremental ΔΣ ADC. Unlike conventional ΔΣ ADCs, it does not require any dedicated clock signals, thus saving energy consumption and reducing system complexity. To realize the self-timed operation, the integrators in the ΔΣ modulator are implemented with the zero-crossing based switched-capacitor circuit, which has been introduced in the previous chapters. Via a handshaking protocol with these ZCB integrators, an on-chip asynchronous digital state machine is able to trigger the charge-balancing progress from one cycle to the next, thus eliminating the need for external driving clocks.

To start with, this chapter gives a brief introduction to the working principle of the incremental ΔΣ ADC. Specifically, the system-level design of a second-order modulator used in this project and the associated decimation filter are discussed. That is followed by a description of the self-timed operation in detail, including its timing procedure and the custom design of the digital state machine. A short summary is given at the end.

4-1 Incremental ΔΣ ADC

The incremental ΔΣ ADC is a special type of ΔΣ converter designed for static or quasistatic signal measurements [63] [64]. It is able to achieve excellent performance in the absolute accuracy of sample-to-sample conversions, namely resolution, linearity, offset and gain errors [8]. In contrast to conventional ΔΣ audio or radio converters where digitization is performed continuously, an incremental ADC converts each individual sample to a stream of binary pulses (bitstream), usually in a charge-balancing fashion, and takes the average or decimated value as the digitized output. Therefore, it is also referred to as an “single-shot ΔΣ ADC” or a “charge-balancing ΔΣ ADC” in the literature [65][38].

The theory of incremental ΔΣ ADCs has been intensively discussed in [11]. As such, this section will mainly focus on the design considerations of the incremental ΔΣ converter that is to be used in the prototype. But first, the basic operation principle of such ADCs will be briefly reviewed.

4-1-1 Basic Principle

The first incremental ΔΣ ADC was proposed in [66] as a alternative to the Nyquist-rate dual-slope converter, in a first-order architecture. Its conversion principle is similar to the dual-slope one in terms of applying charge-balancing, i.e. using the input and the reference to charge /discharge a capacitor so that the stored charge achieves a state of equilibrium. The main difference between both lies in the integration sequence of the input and the reference signals: while being separated from each other in the dual-slope converter, they are interleaved in the first-order incremental ADC [8].

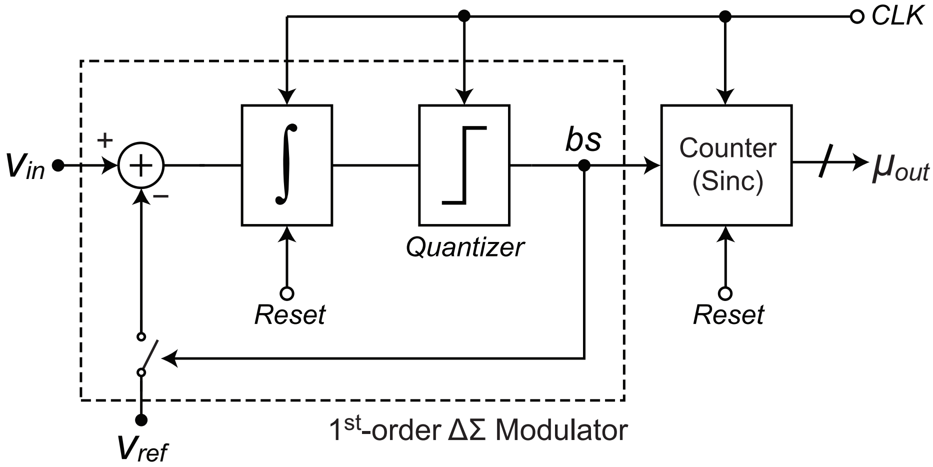

Figure 4-1: Block diagram of a first-order incremental ΔΣ ADC

As illustrated in Figure 4-1 [8], a first-order incremental ADC consists of a first-order ΔΣ modulator with a resettable switched-capacitor integrator, as well as a back-end digital counter which performs as a simple sinc filter. At the beginning of each conversion, the integrator and the counter are both reset, after which a predefined number of integration cycles ($N = 2^{n\text{ bits}}$) are performed, where n is the designed digitization resolution in bits. In each cycle, a charge packet with a fixed size determined by the reference signal is either pumped to the input capacitor or not, depending on the sign of the quantizer output. Thus, a feedback loop is established to help achieve the charge-balanced state. At the same time, the counter records he number of cycles in which feedback is applied, denoted as N_{FB}. After the conversion is accomplished, the digital representation of the input signal can be derived from the ratio between the input signal and the reference:

$$\mu_{\text{out}} = \frac{V_{\text{in}}}{V_{\text{ref}}} = \frac{N_{FB}}{N} + \frac{\epsilon_Q}{N} \tag{4-1}$$

where $\epsilon_Q \in [-0.5, 0.5]$ is the quantization error [11].

As is the case with dual-slope converters [67], first-order incremental ADCs suffer from the conversion speed limitation due to the fact that 2^n cycles are needed for a n bits conversion. This problem is resolved with the invention of higher-order incremental ADCs , as proposed in [68]. By replacing the first-order ΔΣ modulator in Figure 4-1 with a second- or higher-order one, leading to Figure 4-2, the required number of cycles can be dramatically reduced [64][1]. Correspondingly, the first-order sinc filter (counter) should be replaced with a higher-order digital decimation filter [11]. Their detailed operation principle will be explained in Section 4-1-2 and Section 4-1-3 by the case of a second-order incremental ΔΣ ADC, which is to be used in the prototype chip.

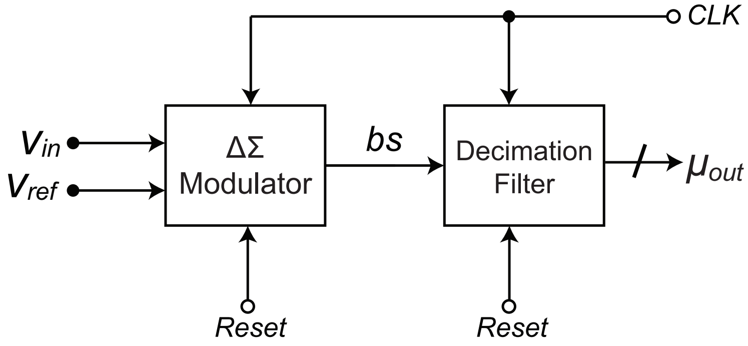

Figure 4-2: Block diagram of a higher-order incremental ΔΣ ADC [8]

It is noteworthy that incremental ΔΣ ADCs distinguish themselves from conventional ΔΣ ADCs in the following aspects [8]:

- Being designed for one-shot conversions of slowly varying signals, the ΔΣ modulator in the incremental ADC does not operate continuously, and the analog integrator as well as the decimation filter are both reset after each conversion. This is for the sake of preventing the possible performance degradation due to limit cycles (or pattern noise) associated with DC excitations [59];
- The incremental ΔΣ ADC shares similar oversampling characteristics as the conventional ΔΣ ADC. In the latter case, the resolution and noise performance can be improved by increasing the ratio between the sampling frequency and the signal bandwidth. However, in incremental ADCs whose input signal frequency is around DC, the same improvement can only be obtained by increasing the number of internal cycles instead of extending the sampling frequency. As such, the number of internal cycles can be regarded as the equivalent oversampling ratio (OSR), albeit in time-domain. This is an apparent advantage, because the increase of the OSR does not necessarily be restricted by the maximum frequency achievable of the specified technology, and extremely high resolution for DC-measurement can be easily achieved [12];
- In conventional ΔΣ ADCs, the spectral behaviour of the decimation process, such as the rejection ability of out-band noise and the steepness of the roll-off [71], is of special concern and usually adds to the design complexity. By contrast, the decimation filter

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[1] A number of other approaches have been proposed to reduce the conversion time. For example, SAR or other algorithmic converters were implemented at the end of the ΔΣ modulator to further digitize the residual error [69][70], which are named as extended-range or extended-counting ADCs. They are out of scope of this thesis.

of the incremental ADC can be implemented with a far simpler architecture compared with that in conventional ΔΣ converters [8]. More details will be discussed in Section 4-1-3;

- As the timing methodology is concerned, incremental ADCs are perfectly suited for self-timed implementations because of their transient-mode operation principle and the DC-measuring characteristic. In conventional ΔΣ ADCs, however, the self-timed operation inevitably results in non-uniform sampling, i.e. taking samples with non-equal-space in time. Its analysis calls for a more generalized version of the Shannon sampling theorem [72], which is still an advanced research topic in the field of signal processing [73].

4-1-2 ΔΣ Modulator Design

This section discusses the design of a second-order incremental ΔΣ modulator which is to be used in the prototype ADC. As a proof-of-concept, the design starts from the classical Boser-Wooley structure [74], as shown in Figure 4-3. This modulator consists of two cascaded half-delay integrators and a single-bit quantizer, as well as a feedback DAC. The values of modulator coefficients (a_1, a_2 and b) are derived from [59][2].

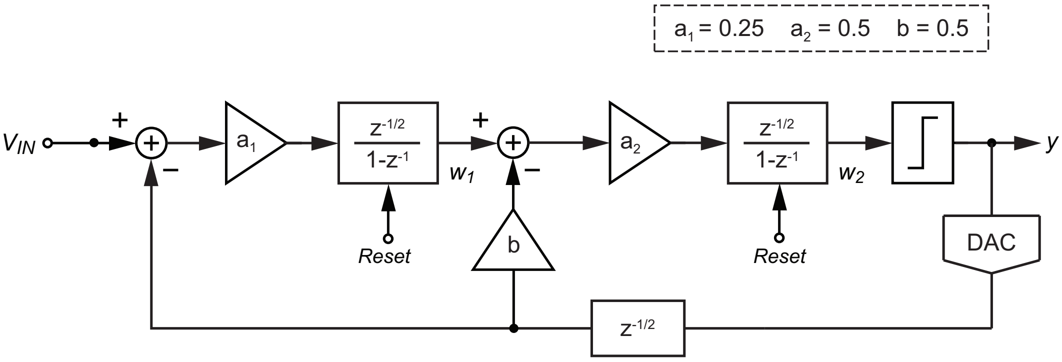
$a_1 = 0.25$ $a_2 = 0.5$ $b = 0.5$
V_{IN}
+
−
a_1
$\frac{z^{-1/2}}{1-z^{-1}}$
w_1
+
−
a_2
$\frac{z^{-1/2}}{1-z^{-1}}$
w_2
y
Reset
b
Reset
DAC
$z^{-1/2}$

Figure 4-3: Block diagram of a second-order Boser-Wooley modulator

Similar with the first-order modulator, both integrators in the second-order modulator are reset before the conversion starts. Within the conversion time, the modulator input signal V_{in} is assumed as constant. The output samples of the first and second integrators ($w_1[i]$ and $w_2[i]$, respectively) can be derived based on the iterative relationships in the time domain, as given by

$$w_1[i] = w_1[i-1] + a_1 V_{\text{in}} - a_1 y[i] V_{\text{ref}} \tag{4-2}$$

and

$$w_2[i] = w_2[i-1] + a_2 w_1[i] - a_2 b \cdot y[i] V_{\text{ref}} \tag{4-3}$$

where i is the sample time index, $y[i] = \pm 1$ is the single-bit quantizer output at the i-th sample and V_{ref} is the feedback reference voltage.

---

[2] In Boser-Wooley modulator, a coefficient ratio of $b/a_1 = 2$ should be maintained to achieve the desired signal transfer function (STF) and noise transfer function (NTF) [59].

The non-iterative expressions at the n-th sample can be obtained by summing all the items from $i = 1$ to $i = n$, resulting in

$$w_1[n] = a_1 n \cdot V_{\text{in}} - a_1 \sum_{i=1}^{n} y[i] \cdot V_{\text{ref}} \tag{4-4}$$

and

$$w_2[n] = a_1 a_2 \sum_{i=1}^{n} i \cdot V_{\text{in}} - a_1 a_2 \sum_{i=1}^{n} \sum_{j=1}^{i} y[j] \cdot V_{\text{ref}} - a_2 b \sum_{i=1}^{n} y[i] \cdot V_{\text{ref}} \tag{4-5}$$

Thereby, after M cycles the residual error at the output of the second integrator becomes

$$w_2[M] = a_1 a_2 \frac{M(M+1)}{2} \cdot V_{\text{in}} - a_1 a_2 \left\{ \sum_{i=1}^{M} \sum_{j=1}^{i} y[j] + \frac{b}{a_1} \sum_{i=1}^{M} y[i] \right\} \cdot V_{\text{ref}} \tag{4-6}$$

By rearranging (4-6), one gets the ratio between the input signal and the reference:

$$\frac{V_{\text{in}}}{V_{\text{ref}}} = \frac{2}{M(M+1)} \left\{ \sum_{i=1}^{M} \sum_{j=1}^{i} y[j] + \frac{b}{a_1} \sum_{i=1}^{M} y[i] \right\} + \frac{2}{a_1 a_2 M(M+1)} \cdot \frac{w_2[M]}{V_{\text{ref}}} \tag{4-7}$$

Owing to the modulator stability, $w_2[M]$ is bounded within the range of $[-V_{\text{ref}}, +V_{\text{ref}}]$. Hence, as long as $M \gg 1$, the second term in the right-hand side of expression (4-7) is negligible, and an estimation of $V_{\text{in}}/V_{\text{ref}}$ can be found as

$$\frac{\widetilde{V}_{\text{in}}}{V_{\text{ref}}} = \frac{2}{M(M+1)} \left\{ \sum_{i=1}^{M} \sum_{j=1}^{i} y[j] + \frac{b}{a_1} \sum_{i=1}^{M} y[i] \right\} \tag{4-8}$$

where $\frac{b}{a_1}$ equals to 2. The remained error of the above estimation is

$$E_Q = V_{\text{in}} - \widetilde{V}_{\text{in}} = \frac{2}{a_1 a_2 M(M+1)} w_2[M] \tag{4-9}$$

which can be regarded as an analog form of the quantization error [8]. Moreover, for an ideal noiseless analog-to-digital converter, the value of E_Q should be restricted by the extent of one LSB voltage, leading to

$$\frac{4}{a_1 a_2 M(M+1)} V_{\text{ref}} \leqslant V_{LSB} \tag{4-10}$$

where V_{LSB} can be derived based on the effective number of bits (ENOB) [67]:

$$V_{LSB} = \frac{2V_{\text{ref}}}{2^{ENOB}} \tag{4-11}$$

The combination of (4-10) and (4-11) can be employed in estimating the required number of cycles (M) for a specified ENOB. For instance, in order to achieve a 14-bit performance, M should be larger than 512. Further trimming is often required based on this estimation. On one hand, it is ideally conservative since the full swing of $w_2[M]$ is only a portion of $2V_{\text{ref}}$ due to stability concerns. On the other hand, in practical design the quantization error needs to be further suppressed when noise and other interference are concerned, hence the required number of cycles usually gets larger.

On the basis of the above analysis, the behavior of the incremental $\Delta\Sigma$ modulator can be modeled in MATLAB with custom-written codes. Figure 4-4 (a) plots the simulated quantization error with 14-bit scale, which corresponds to 500 cycles[3]. As illustrated, the variation of the quantization error is within $[-0.5LSB, +0.5LSB]$, which agrees well with (4-9) and (4-10). Its trend of going negative along the normalized input axis is associated with the input-dependence of $w[M]$.

The maximum output ranges (represented by the upper and lower limits) of the first and second analog integrators across the normalized input range are also investigated, with results presented in Figure 4-4 (b) and (c). It can be found that the average output of the first integrator (the dashed line in Figure 4-4(b)) is not remained zero (half-level of the full-scale). This is a particular case for distributed-feedback modulators with a constant input [38][59]. To null the input of the second integrator thus ensure the stability, the output of the first integrator should be proportional to bV_{in} [38]. The resulted increase of the peak-to-peak

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[3] The decimation process performed in these simulations essentially adopts the methodology of "matched" digital filters, as will be discussed in Section 4-1-3.

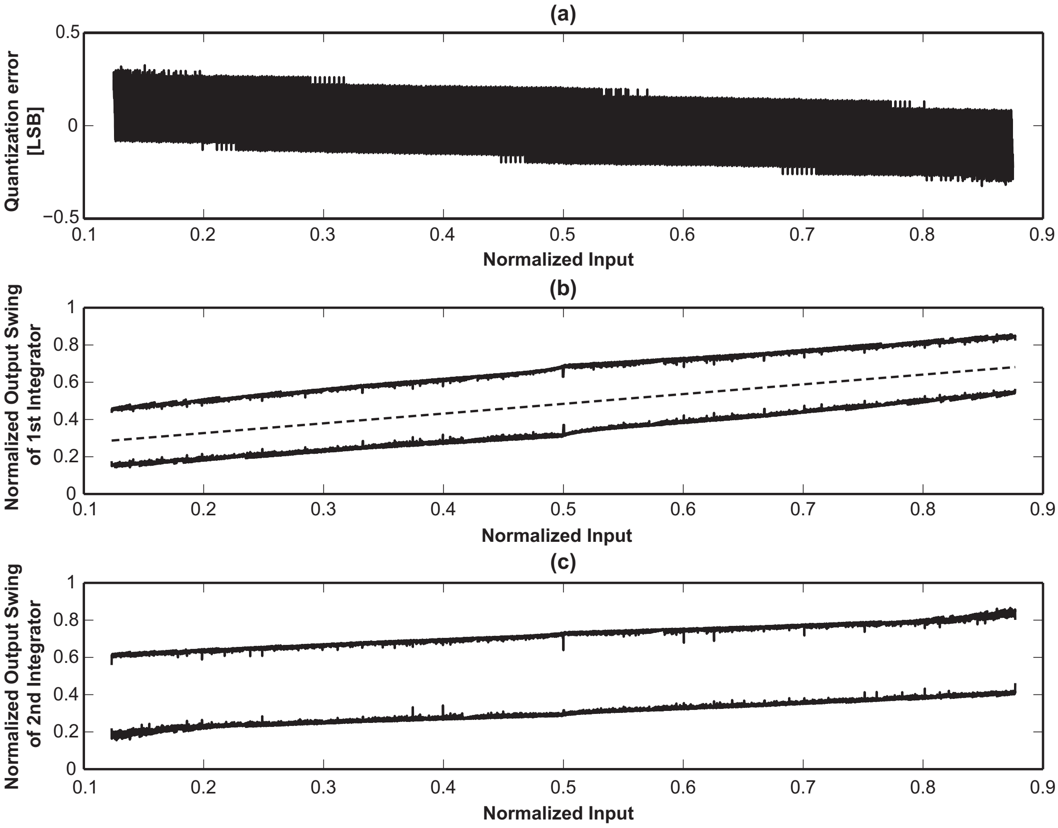


Figure 4-4: Behavior of the second-order incremental Boser-Wooley $\Delta\Sigma$ modulator based on MATLAB simulations. (a) Row-1: quantization error versus normalized input range (14-bit scale, 500 cycles); (b): output range of the first analog integrator versus normalized input range; (c): output range of the second analog integrator versus normalized input range.

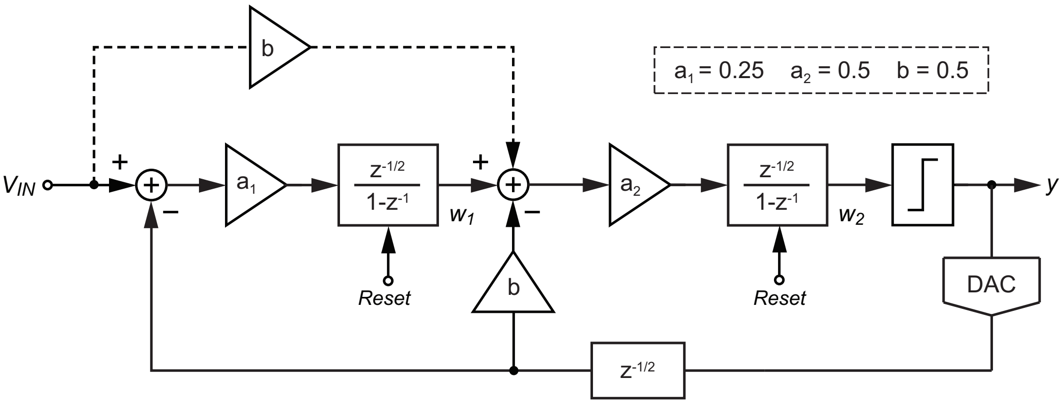


Figure 4-5: Block diagram of a second-order Boser-Wooley modulator with a input-feedforward path.

output swing of the first integrator is likely to degrade the circuit performance (e.g. power consumption and linearity) in practical implementations [75].

To stabilize the output of the first integrator, an input-feedforward path with a scaling coefficient of b is added across the first integrator [38], as shown in Figure 4-5. Thereby, the output sample of the second integrator becomes

$$w_2'[i] = w_2[i-1] + a_2 w_1[i] + a_2 b \cdot V_{\text{in}} - a_2 b \cdot y[i] V_{\text{ref}} \tag{4-12}$$

which leads to the non-iterative expression

$$w_2'[n] = \left\{ a_1 a_2 \sum_{i=1}^{n} i + a_2 b \cdot n \right\} \cdot V_{\text{in}} - \left\{ a_1 a_2 \sum_{i=1}^{n} \sum_{j=1}^{i} y[j] + a_2 b \sum_{i=1}^{n} y[i] \right\} \cdot V_{\text{ref}} \tag{4-13}$$

at the n-th sample. The new estimation of $V_{\text{in}}/V_{\text{ref}}$ after M samples can be derived in a similar way to (4-6)∼(4-9), as given by

$$\frac{\widetilde{V_{\text{in}}}'}{V_{\text{ref}}} = \frac{2a_1}{a_1 M(M+1) + 2b \cdot M} \left\{ \sum_{i=1}^{M} \sum_{j=1}^{i} y[j] + \frac{b}{a_1} \sum_{i=1}^{M} y[i] \right\} \tag{4-14}$$

while the new quantization error is

$$E_Q' = \frac{2}{a_1 a_2 M(M+1) + 2a_2 b M} w_2[M] \tag{4-15}$$

where $w_2[M]$ is bounded by $[-V_{\text{ref}}, +V_{\text{ref}}]$ as before.

With the modified structure, the quantization error as well as the output swings of the analog integrators are re-simulated and presented in Figure 4-6. As expected, the averaged output of the first integrator is stabilized, while the quantization error remains unchanged.

4-1-3 Decimation Filter Deisgn

As shown in Figure 4-2, a digital decimation filter following the analog modulator is required for the re-construction of the signal and the attenuation of out-of-band components, such as

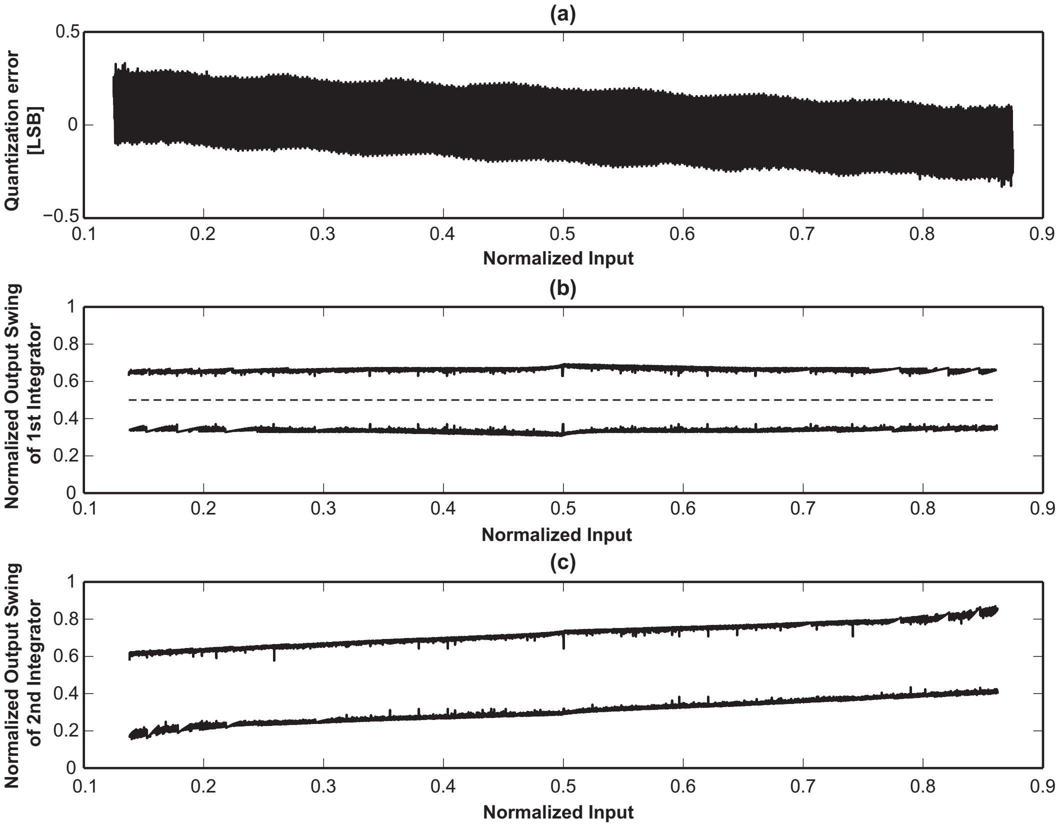


Figure 4-6: Behavior of the second-order incremental Boser-Wooley $\Delta\Sigma$ modulator with a input feedforward path based on MATLAB simulations. (a): quantization error versus normalized input range (14-bit scale, 500 cycles); (b): output range of the first analog integrator versus normalized input range; (c): output range of the second analog integrator versus normalized input range.

quantization error, circuit noise and other interference [58]. For an incremental $\Delta\Sigma$ modulator operating for M cycles, the decimation filter is essentially a finite impulse response (FIR) filter with length M [38]. In the practical design of high-order architectures, the choice of the decimation filter topology may have an influence on the ADC's resolution due to the existence of circuit noise and non-linearity. In view of this, an investigation of the system design approaches for high-order decimation filters is presented in this section. For design flexibility, the decimation filter in the prototype ADC is implemented based on a commercial field-programmable gate array (FPGA) device.

The most straightforward approach is to use a digital decimation filter with a "matched" impulse response with that of the analog loop-filter [38]. As revealed by expression (4-14), the input voltage of a second-order incremental $\Delta\Sigma$ ADC can be synchronously reconstructed at the output of the modulator, with the aid of a digital filter consisting of two cascaded digital integrators and a input-feedforward path, as shown in Figure 4-7. Such topology is also referred to as cascade of integrators (CoI) [64]. Since both digital integrators operate in the transient mode and keep pace with their analog counterparts, the possible conversion latency associated with the decimation process can be eliminated.

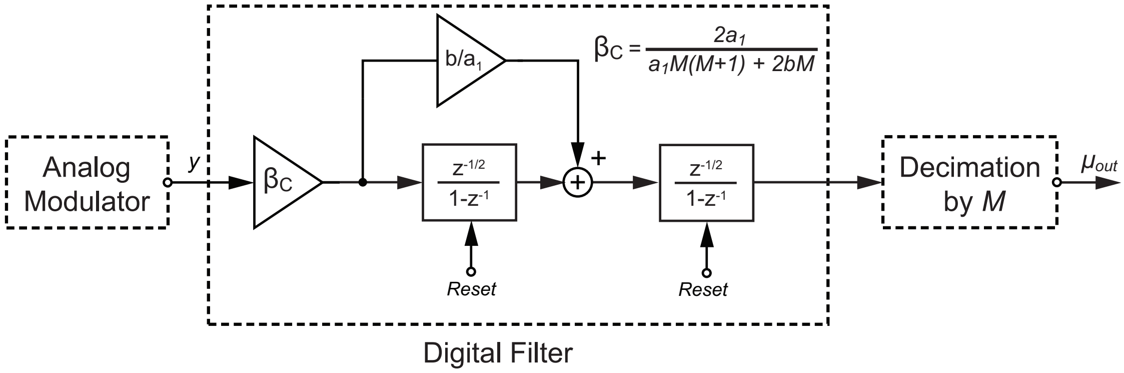

Analog
Modulator
y
β_C
b/a$_1$
$\beta_C = \frac{2a_1}{a_1M(M+1) + 2bM}$
$\frac{z^{-1/2}}{1-z^{-1}}$
+
$\frac{z^{-1/2}}{1-z^{-1}}$
Reset
Reset
Decimation
by M
μ_{out}
Digital Filter

Figure 4-7: Block diagram of a back-end digital filter and a decimator corresponding to (4-14)

The advantage of the CoI structure is its hardware efficiency. As interpreted by Figure 4-7, a CoI filter can be simply implemented with counters and accumulators. Its main drawback, however, is the poor capacity in the rejection of periodical noise, such as 50Hz noise from the supply [64] or dynamic noise caused by chopping or dynamic element matching (DEM) in the analog circuits [38]. This is essentially caused by the lack of notches in the frequency response of the CoI filters [38]. When the ADC's performance is limited by those periodical noise, a higher-order sinc^k filter can be used [64]. It can provide a better suppression on the spurious noise with the penalty of increased circuit complexity.

For the prototype design in this thesis, a simple CoI filter is adequate for achieving the targeted performance, due to the fact that no chopping or DEM is applied to the analog signal path, and the power supply of the chip is derived from a low-noise low-dropout regulators (LDO) (see Chapter 6). Higher-order sinc^k filters might be needed in future implementations which employ more novel dynamic error-cancellation circuit techniques.

4-1-4 Circuit Implementations

Figure 4-8 shows the circuit implementation of the described incremental second-order ΔΣ modulator in Figure 4-5. As proposed in the introductory chapter, the discrete-time integrators are deliberately realized with the discussed zero-crossing based switched-capacitor circuit, thus making it feasible to run the modulator in a self-timed way. A dynamic comparator following the cascaded integrators (see Chapter 5) is employed to perform the 1-bit quantization and control the charge-balancing procedure.

Different feedback strategies are chosen for the two integrators: a feedback capacitor C_{FB} and the associated S/H network is applied to the second integrator to realize the local-feedback coefficient b; on the contrary, as the feedback to the first integrator is "apparent" to the input signal, it's recommended to adopt the second scheme in Figure 2-12 to minimize the input-referred kT/C noise[4]. In addition to that, a capacitor C_F across the first integrator is included to implement the input-feedforward path.

---

[4] The elimination of the feedback capacitor can also reduce the gain-error caused by capacitor mismatches. However, this improvement is to some extent counteracted by the effect of the signal-dependent voltage-drop on the feedback switches (Section 2-3-2).

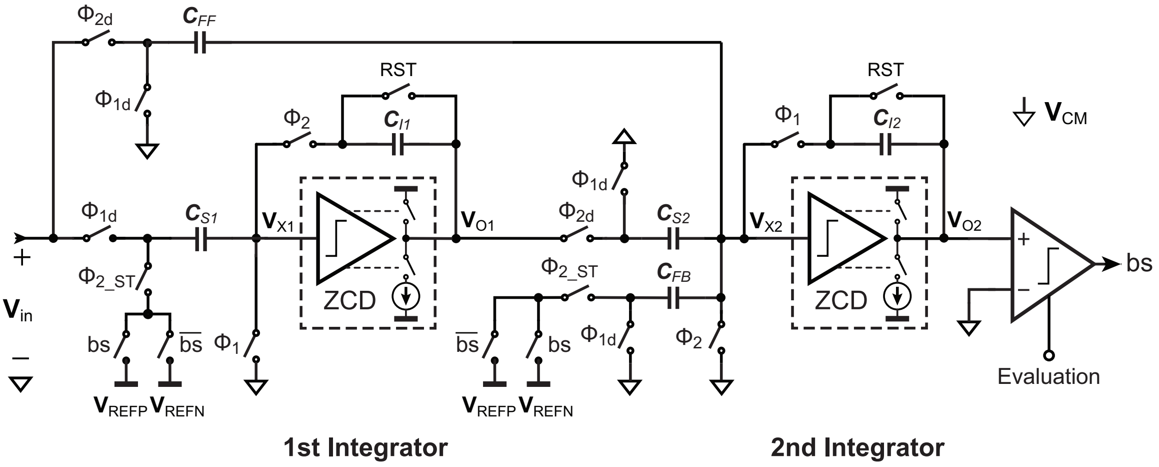


Figure 4-8: Circuit implementation of the proposed second-order incremental ΔΣ modulator

All the switched-control signals shown in Figure 4-8 are self-generated on the prototype chip via the mixed-signal handshaking and the asynchronous state machine (ASM). The timing procedure and implementation details of the ASM will be described in the next section.

4-2 Self-Timed Operation

This section describes the self-timed operation principle and the associated digital circuitry realizations. As aforementioned in Chapter 2, the zero-crossing based circuit offers the feasibility of detecting the completion of the charge-transfer process. The output decisions of the zero-crossing detectors, which are logic-level signals, can be utilized as the triggering events for the state transitions in an asynchronous state-machine. Based on this principle, the ΔΣ modulator presented in Figure 4-8 can operate without any external timing-control signals, or clocks. Its timing sequence is hence self-ordered according to the actual manufacturing and operating conditions in the analog circuitry, which is theoretically the most efficient timing methodology. To achieve this, a workable and robust asynchronous state-machine is required.

4-2-1 Asynchronous State-Machine

The general idea of a self-timed ΔΣ modulator is in a sense analogous to a ping-pong game. For a second-order modulator with cascaded half-delay integrators, the minimal duration time required for each phase is usually dominated by the charge-transfer process of the corresponding integrator.This condition is tenable as long as the on-resistance of the switches associated with the sampling settling is small enough (see expression (1-1)), leading to a relative fast sampling with respect to the charge-transfer. Fortunately, this is a common case in most I&M applications [11]. Inspired by this fact, one can design a smart “event-controller” to alternatively monitor the charge-transfer progress of each integrator, and determine the critical instants for phase transitions, as depicted in Figure 4-9. Such an event-controller can be readily implemented with an asynchronous state-machine, which operates in a cycle of two

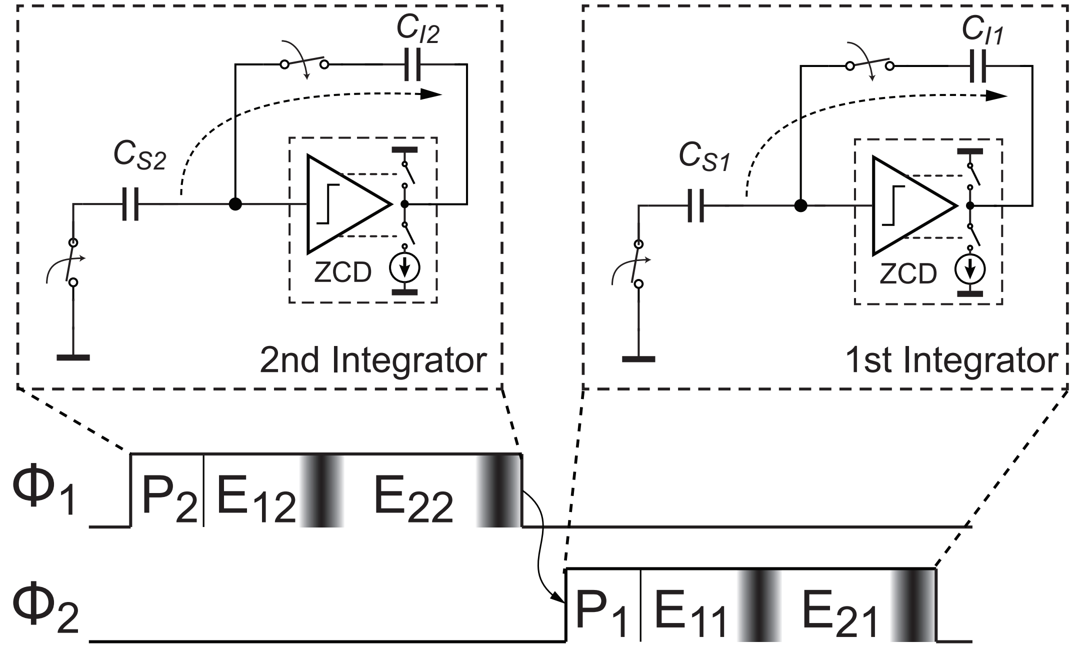


Figure 4-9: 2-phase timing principle of a self-timed zero-crossing based $\Delta\Sigma$ modulator.

time-interleaved states: Φ_1 (State-A) and Φ_2 (State-B). They are triggered by each other in a ping-pong manner, and ended by the completion signals from the zero-crossing detectors of the analog modulator, thus removing the time redundancy existing in Figure 2-2. Due to this characteristic, Φ_1 and Φ_2 are inherently non-overlapped with each other.

Figure 4-10 shows the block diagram of the self-timed incremental $\Delta\Sigma$ ADC with the described asynchronous state-machine. In order to make the incremental analog-to-digital conversion operating in a one-shot fashion, an initial start-up excitation and a conversion-cycle control are both included. The latter can be realized by a internal cycle-counter triggered by self-generated phase clocks. After operating for M cycles, the counter sends a termination signal to the state-machine and reset all memory elements (e.g. analog integrators in the modulator and digital registers in the decimation filter). On the other hand, the implementation of the start-up signal which kicks-off the state-machine can rely on certain kinds of burst information embodied in the input signal, such as the threshold-crossing of temperature. This mechanism can vary with different applications, depending on the property of the measured signal. In this way, the converter is only “waked up” when requested, which saves energy.

Figure 4-11 shows the overall timing diagram with details of the self-timed control signals of one of the integrators in the modulator (the other one operates identically). Regarding the multi-phase characteristic of zero-crossing based charge-transfer, the internal timing control in each phase state (Φ_1 and Φ_2) should be self-ordered as well. As stated in Chapter 2, the transition from the coarse charging phase to the fine charging phase is inherently self-timed even in synchronous implementations, as it is triggered by the early-threshold detection signal. However, the preset phase, which has a short but fixed duration time, is usually defined by external clocks and hence obstructs the realization of purely self-timed operation. A way to generate a self-timed preset signal is to insert a constant time-slot between the rising edge of the charge-transfer phase and the start moment of the actual charge-transfer process (Φ_{1_CT}

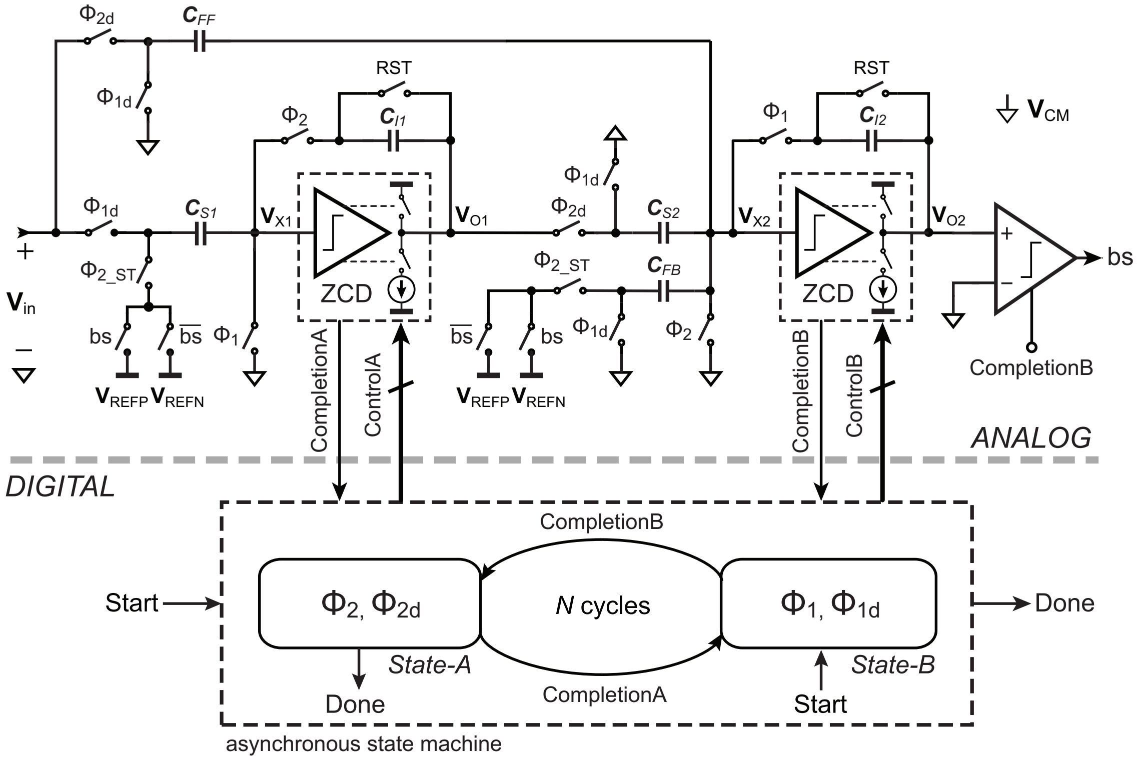

Φ_{2d}
C_{FF}
Φ_{1d}
RST
Φ_2
C_{I1}
Φ_{1d}
C_{S1}
V_{X1}
ZCD
V_{O1}
Φ_{2_ST}
+
V_{in}
−
bs
$\overline{bs}$
Φ_1
V_{REFP} V_{REFN}
CompletionA
ControlA
Φ_{1d}
Φ_{2d}
C_{S2}
Φ_{2_ST}
C_{FB}
$\overline{bs}$
bs
Φ_{1d}
Φ_2
V_{REFP} V_{REFN}
RST
Φ_1
C_{I2}
V_{X2}
ZCD
V_{O2}
V_{CM}
+
−
bs
CompletionB
CompletionB
ControlB
ANALOG
DIGITAL
CompletionB
Start
Φ_2, Φ_{2d}
N cycles
Φ_1, Φ_{1d}
Done
State-A
State-B
Done
CompletionA
Start
asynchronous state machine

Figure 4-10: Block diagram of the proposed self-timed incremental ΔΣ ADC with an asynchronous state-machine.

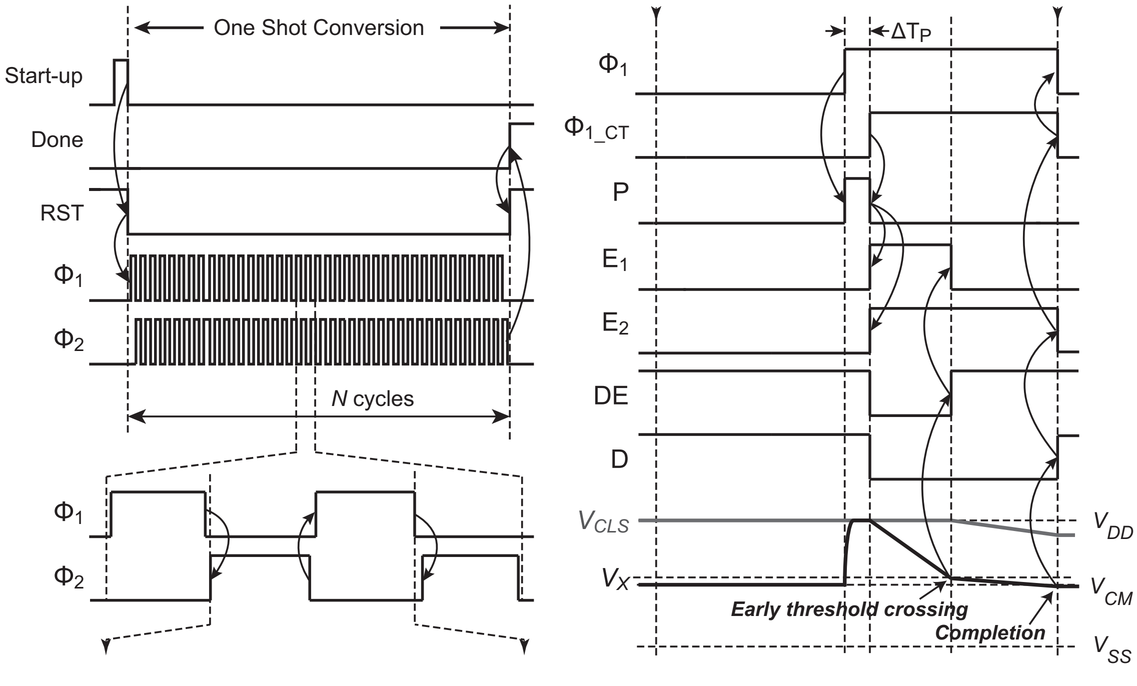

One Shot Conversion
Start-up
Done
RST
Φ_1
Φ_2
N cycles
Φ_1
Φ_2
ΔT_P
Φ_1
Φ_{1_CT}
P
E_1
E_2
DE
D
V_{CLS}
V_X
V_{DD}
V_{CM}
V_{SS}
Early threshold crossing
Completion

Figure 4-11: Timing diagram of the proposed self-timed incremental ΔΣ ADC

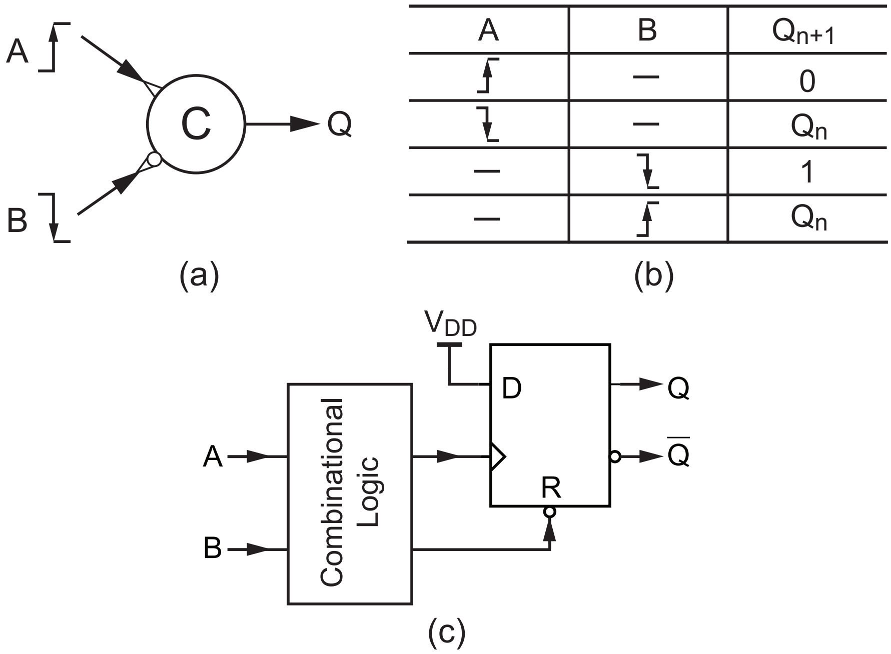
in Figure 4-11). The length of the time-slot should fulfill the following condition:

$$\Delta T_P > N \cdot \tau_P, \quad \tau_P = 2R_{\text{preset}}C_{\text{total}} \tag{4-16}$$

where R_{preset} is the on-resistance of the preset switch, C_{Total} is the total capacitance at the integrator output and N ranges from 5 to 7[5]. In circuit implementations, this time-slot can be configured as a controlled delay element, as will be discussed in the next section.

4-2-2 Self-Timed Logic Elements

The correct operation of the proposed self-timed ADC requires a strict ordering of signal events occurring in both analog and digital domain, as indicated by the arrows in Figure 4-11. In custom circuit design[6], this task can be performed by a handshaking logic element, whose macro model and truth table are depicted in Figure 4-12 (a) and (b). Its function is analogous to the famous Muller-C element [76] used in digital self-timed systems [17], except that here only edges of event clocks are detected to ensure the robustness of mixed-signal communication.



A	B	Q_{n+1}
↑	—	0
↓	—	Q_n
—	↓	1
—	↑	Q_n

Figure 4-12: Basic handshaking element used for self-timed mixed-signal system (a) Macro model (b) Truth table (c) Implementation example

As revealed by the truth table in Figure 4-12, the controlled circuit element (represened by C) must behave in response to different clock edges. Ideally, such type of logic element is equivalent to a D flip-flop (DFF) with double input clocks with different trigger edges. That is, however, difficult to be realized in practice[7]. A feasible solution is to center the logic element around a single-clock DFF with asynchronous reset, as presented in Figure 4-12(c). Since the asynchronous reset is level-triggered, a set of properly-designed combinational circuits may be needed to prevent any possible function failure caused by the conflict between the clock and the reset.

---

[5] The settling accuracy for the preset is not so critical as for the charge-transfer.

[6] This is with respect to the EDA-assisted automatic synthesis in SoC design flow. In the future work, the automatic synthesis approach may be employed for the implementation of the asynchronous state-machine.

[7] Recall that in synthesizable verilogHDL, a single register-type (*reg*) variable is not allowed to be assigned in multiple *always* blocks with different sensitivity-list [77].

Figure 4-13 explains how the proposed logic element works in a mixed-signal self-timed system. As shown in the figure, each handshaking logic element controls an individual state and has two inputs: a completion signal from the analog modules, and an output signal from other handshaking logic elements. Once an element receives a completion signal, it immediately terminates the current state and sends a falling edge to another element, which kicks-off the next state. In this way, the logic elements “shake hands” with each other and establish a self-driven timing sequence.

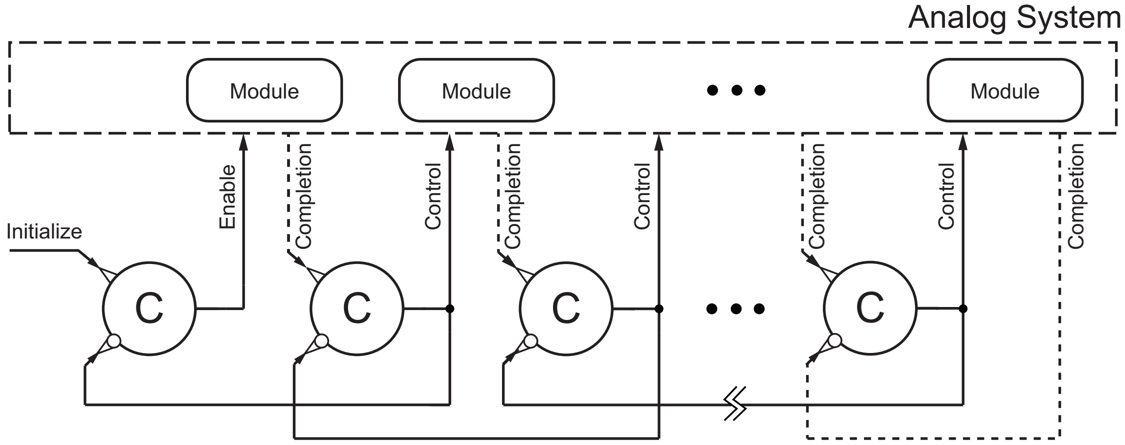


Figure 4-13: General principle of handshaking operation in self-timed mixed-signals systems using the proposed logic element

As an elaboration of the above concepts, the implementation details of several critical handshaking logic blocks in the asynchronous state-machine are presented below.

Generation of charging process control signals

The control signals for the coarse and fine phase charging process, E_1 and E_2, are simply generated by a D flip-flop, as depicted in Figure 4-14. They are both triggered by the falling edge of the preset signal, and reset to zero either by the early-threshold crossing decision or by the virtual ground crossing decision.

Generation of Φ_{1_CT}

As shown in Figure 4-11, the control signal Φ_{1_CT} defines the actual charge-transfer period, i.e. the charge-transfer phase without the preset time-slot. Its rising edge is delayed with respect to that of Φ_1 by ΔT_P, while its falling edge is triggered by completions signal of the fine charging phase (E_2). Figure 4-15 depicts the generation circuitry of Φ_{1_CT}, which is based on a DFF and a delay element for the generation of ΔT_P.

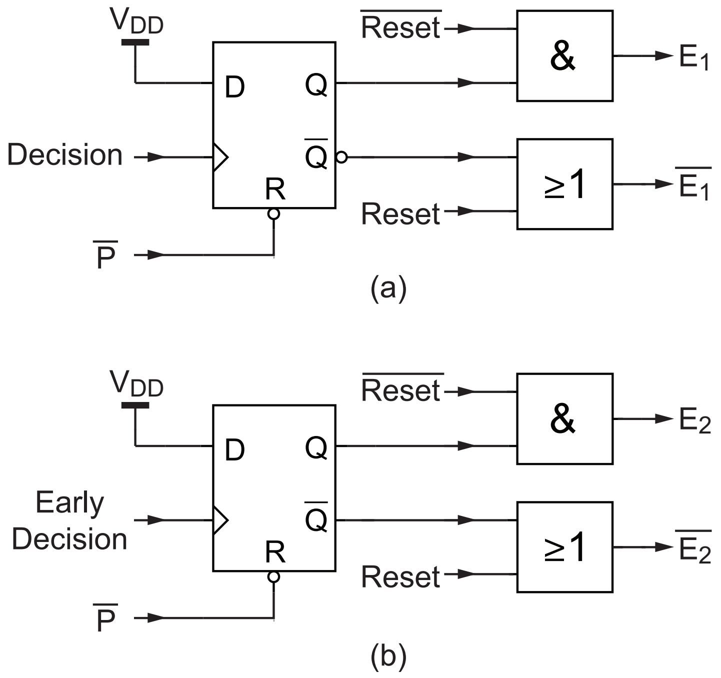

VDD
D
Q
$\overline{Q}$
R
Decision
$\overline{P}$
$\overline{Reset}$
Reset
&
≥1
E1
$\overline{E1}$
(a)
VDD
D
Q
$\overline{Q}$
R
Early Decision
$\overline{P}$
$\overline{Reset}$
Reset
&
≥1
E2
$\overline{E2}$
(b)

Figure 4-14: Logic implementation for the generation of charging phase control signals (a) Coarse phase control (b) Fine phase control

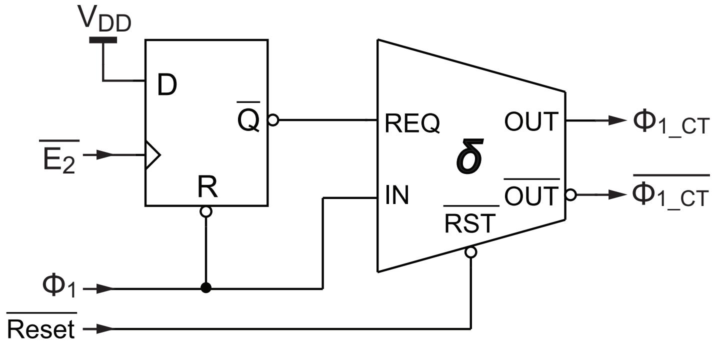

VDD
D
$\overline{Q}$
R
$\overline{E2}$
Φ1
$\overline{Reset}$
REQ
IN
δ
OUT
$\overline{OUT}$
$\overline{RST}$
Φ1_CT
$\overline{Φ1\_CT}$

Figure 4-15: Logic implementation for the generation of Φ_{1_CT} (The δ-block represents the preset delay element)

Preset Delay Element

Figure 4-16 presents the circuit diagram of the delay element used in Figure 4-15. It is essentially a logic controlled delay element based on a current-starved inverter, which was first proposed in [9]. Its delay time is a function of the delay capacitor C_{delay} and the current flowing in the core inverter (distinguished by the dashed box), hence can be adjusted by tuning the biasing of the starved current source. The *REQ* port and the set-reset (SR) latch provide a feasibility of asynchronous (or handshaking) control on the delayed output signal, which is the beauty of this structure. It is taken full advantage of in the design of the self-timed logic

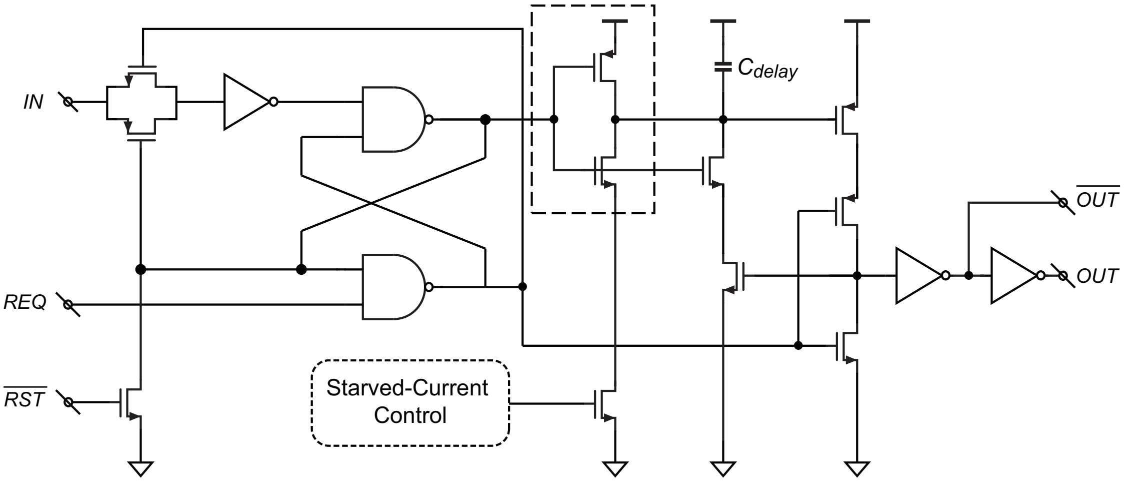


Figure 4-16: Circuit diagram of a low power tunable delay element for preset time-slot generation [9]

circuits, as displayed in Figure 4-15.

4-3 Summary

This chapter has studied the system-level behavior of the proposed self-timed incremental ΔΣ ADC. The discussion is concentrated on two aspects: the system-level design of the incremental ΔΣ ADC, and the operation principle and realization strategy of the self-timed state-machine.

As an attractive candidate for data conversions in I&M applications, the theory and implementation issues of incremental ΔΣ ADCs have been intensively analyzed in literature. Therefore, the introduction to the operation principle is kept concise, while more attention is paid to the design of the modulator and the associated decimation filter. A second-order ΔΣ modulator with a classical topology has been mathematically analyzed and simulated, which is going to be used in the prototype design. Besides that, a matched digital filter with low cost in hardware has been designed to perform the decimation process.

The transient-mode operation characteristic of the incremental ΔΣ ADC makes it particularly suited for the self-timed operation. That is assisted by zero-crossing based switched-capacitor circuits introduced in previous chapters, and an asynchronous state-machine described in this chapter. The custom realization of the asynchronous state-machine calls for special logic elements equipped with handshaking functionality. A macro model and a set of implementation instance of such logic elements have also been presented in this chapter.

Chapter 5

Prototype Chip

This chapter describes the implementation details of the self-timed incremental $\Delta\Sigma$ ADC prototype. The design strategies and circuit techniques introduced in previous chapters are employed in the prototype to demonstrate their effectiveness. The chapter starts with a system-level overview of the prototype chip. After that, the implementation details of the sub-blocks in the incremental ADC are discussed, including some auxiliary circuits like the bias generator and the clock boosters. Moreover, a set of design-for-testability (DFT) circuit techniques are also presented. Layout issues are briefly discussed at the end of the chapter.

5-1 System-Level Design

A system-level circuit diagram of the prototype ADC has been illustrated in Figure 4-10. As a proof-of-concept, a single-ended architecture is employed. It has been fabricated in NXP's 1P6M 0.16μm CMOS process, which is a shrinked version of a standard 0.18μm process [49]. To demonstrate the low-voltage amenability of the proposed structure, a supply voltage of 1V, which roughly equals the sum of the intrinsic threshold voltages of NMOS and PMOS devices in the technology used, is chosen to power both analog and digital circuits in the prototype chip. To enhance the range of the DC input signal, the feedback reference voltages, V_{refn} and V_{refp}, are defined as 0V and 1V, respectively. Accordingly, the common-mode voltage V_{CM} is specified as 0.5V.

As the supply voltage approaches the threshold voltages of the MOS transistors, the implementation of the analog switches in Figure 4-10 can be problematic [75]. While all switches in the analog modulator are NMOS-only transistors, their driving clocks are locally-boosted to around 1.8V to guarantee adequately low on-resistances. Implementation details of the clock-boosters will be introduced in the next section.

The sizing of the sampling capacitors (C_{S1} and C_{S2}) is based on an estimation of the noise budget, as discussed below. In general, for a N-bit ADC with an input voltage range of A[V], the allowed mean-square value of the input-referred noise can be calculated by [67]:

$$\overline{V_\mathrm{n}^2} = \frac{A^2}{10^{(6.02N+1.76)/10}} \tag{5-1}$$

Hence, in order to achieve a 14-bit resolution with a 0.6V (0.2V~0.8V) stable input range[1], we have $\sqrt{\overline{V_\mathrm{n}^2}} = 29.9\mu V$.

In practice, the zero-crossing based incremental ΔΣ ADC suffers not only from quantization errors, but also from other noise sources, such as kT/C noise from the sampling operation and the discussed thermal noise generated by the zero-crossing detectors. A good balance between the contributions of various types of noise sources is able to make the circuit implementation more economical [59], especially in energy. On one hand, an over-attenuated kT/C noise requires an excessively large sampling capacitor, resulting in a large power consumption. On the other hand, it is also not free to suppress the quantization error; making the modulator operate for more cycles inevitably increases the energy consumption. Therefore, it is suggested to achieve a balance between both, while thermal noise can be slightly larger [38][2].

For this work, a ratio of 55%:45% between the power of thermal noise and quantization error is chosen, leading to an equivalent quantization noise of 20.1μV (RMS) and a thermal noise of 22.2μV (RMS). The formal can be achieved by operating the modulator for 500 cycles, as has been shown in Figure 4-6. The latter is mainly determined by the sizing of the sampling capacitors, as well as the design choices of the zero-crossing detectors and the gated current sources. On the assumption that the noise contributions from the charge-transfer phase are negligible, the minimal value of the first-stage sampling capacitor can be calculated by

$$C_{S,\mathrm{min}} = \frac{kT}{\overline{V_\mathrm{n,thermal}^2} \cdot M} \tag{5-2}$$

With $\overline{V_\mathrm{n,thermal}} = 22.2\mu\mathrm{V}$ and the number of cycles $M = 500$, it gives $C_{S,\mathrm{min}} = 0.017\mathrm{pF}$. Note that this estimation ignores the contribution of ZCDs and the sampled thermal noise in the second stage.

As a conservative design, the sampling capacitor in the first integrator, C_{S1}, is chosen to be 0.5pF. Correspondingly, the sampling capacitor in the second integrator, C_{S2}, is scaled to 0.2pF to save energy.

5-2 Implementation of Sub-Blocks

This section provides a deep view of the sub-block implementation details, including short discussions on the pros and cons of specific design choices.

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[1] This is a conservative assumption in the design phase.

[2] Recommended ratios between the power of thermal noise and quantization error includes 50%:50%, 60%:40%, or 70%:30%.

5-2-1 Zero-crossing Detectors with Early-threshold Detection

Figure 5-1 illustrates the schematic of the employed zero-crossing detector. As discussed in Chapter 3, each ZCD consists of an inverter-based preamplifier and two inverter chains that gain up the preamp's output to logic levels representing the zero-crossing detection (D) and an early-threshold detection (DE). All inverters can be dynamically powered-down by turning off the switches controlled by EN_1 and EN_2. To further save energy, the auto-zeroing (AZ) process of the preamplifier inverter is synchronous with the coarse charge-transfer phase of the other integrator (Chapter 3).

The offset voltage for the early-threshold detection (Figure 2-16) is generated by a level-shifting capacitor C_{off}. In each charge-transfer phase, It is first precharged to a predefined voltage (V_{off}) during the preset time-slot (P), and then inserted between the input nodes of the inverter chains while the charge-transfer is on-going. A predefined voltage V_{off} is generated on-chip, but this can be replaced by a voltage generated using off-chip potentiometers for flexibility.

The sizing of the inverter-based preamplifiers follows the rule of thumb revealed in Section 2-2-1. Table 5-1 lists the simulated specifications of the inverter-based preamplifers in the first and second integrators, both of which fall in the optimal design region (the "sweet corner") shown in Figure 2-6.

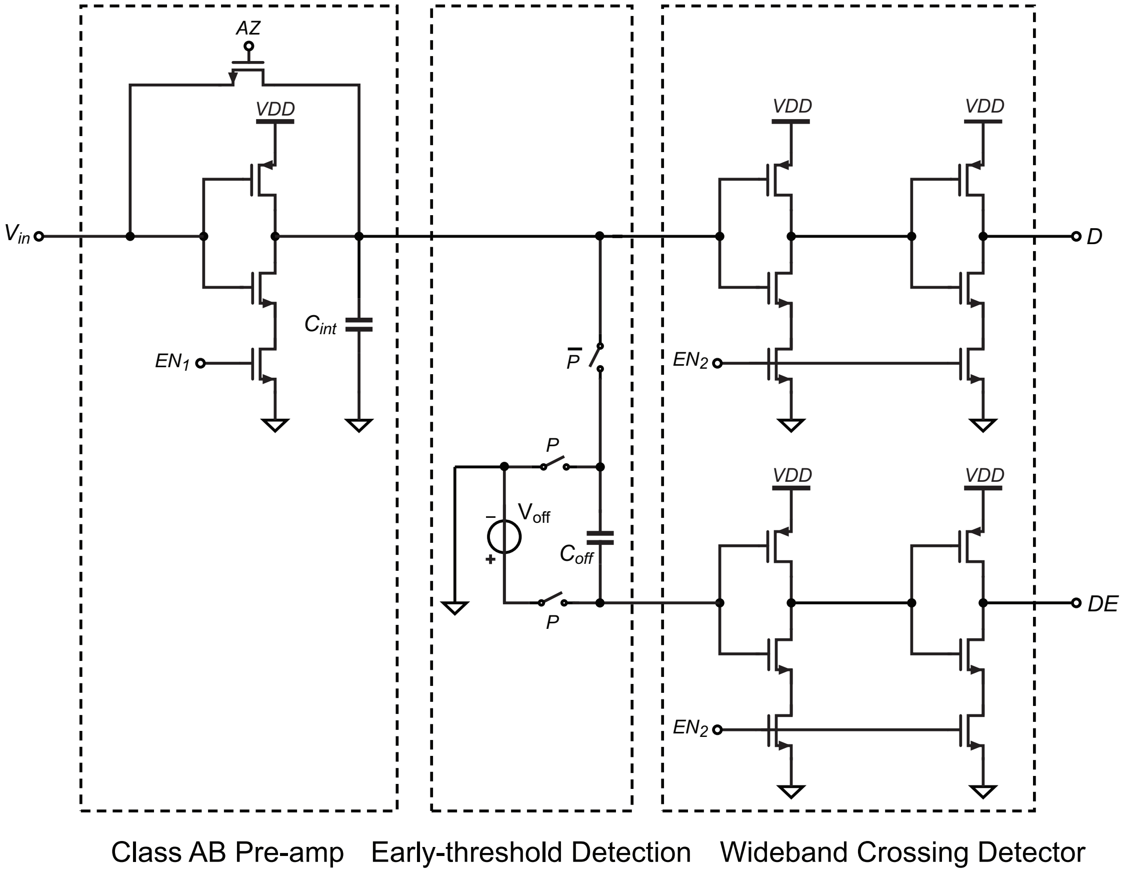


Figure 5-1: Schematic of the zero-crossing detector with early-threshold detection

Table 5-1: Design parameters and performance of the inverter-based preamplifiers in the ZCDs

Parameters	Symbol	1^{st} Int. Inverter	2^{nd} Int. Inverter
Unity-gain bias current	I_0	7.6μA	2.4μA
Unity-gain transconductance	g_{m}	$135\mu\mathrm{S} \times 2$	$40\mu\mathrm{S} \times 2$
Time constant	τ	75ns	75ns
Response time	t_R	65ns	50ns
Band-limit capacitor	C_{int}	150fF	30fF

5-2-2 Gated Current Sources with CLS

Figure 5-2 shows the detailed schematic of the gated current sources with correlated level-shifting. Its operation principle has been extensively explained in Chapter 2. As suggested in Section 2-5-2, a cascoded transistor is introduced in the implementation of the fine current source, which further boosts up the output impedance of the current source and hence improve the charger-transfer linearity.

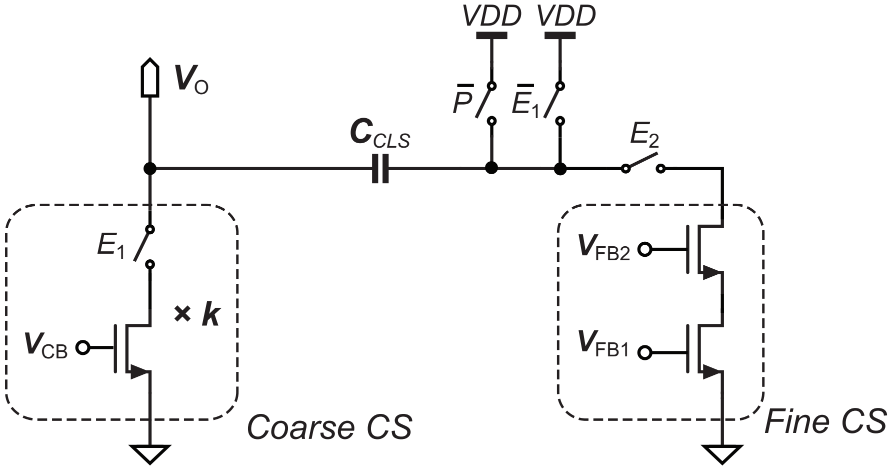


Figure 5-2: Schematic of the gate current source with correlated leveling shifting

As a trade-off between linearity, noise and power consumption, the correlated level-shifting capacitor (C_{CLS}) is chosen to be 400fF.

5-2-3 Bit-Decision Comparator

A dynamic comparator [10][7] is utilized as the single-bit quantizer in the $\Delta\Sigma$ modulator. As shown in Figure 5-3, this comparator consists of two cascaded stages. This first stage contains a NMOS input pair (M_1, M_2) with a pair of transfer gates (M_3, M_4), and a regenerative latch formed by crossed-coupled inverters (in dashed box) [78] with precharge switches (M_5, M_6). The second stage is an S-R latch triggered by the first stage.

The operation flow of this comparator is divided into two steps by the *Latch* clock. When

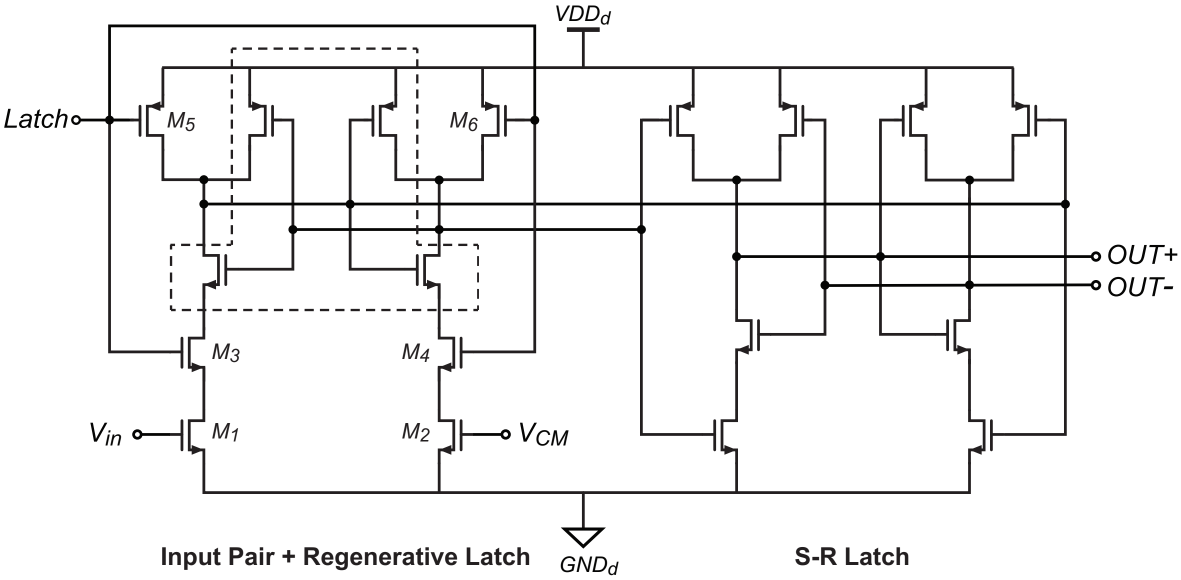


Figure 5-3: Schematic of the dynamic bit-decision comparator

Latch is low, M_3 and M_4 are turned off, while at the same time the regenerative latch is reset by the precharge switches M_5 and M_6. Once *Latch* goes high, the input voltage difference causes an imbalance in the equivalent resistance of M_1 and M_2, which drives the regeneration of the crossed-coupled inverter until the final state is reached. This final state is then latched in the second stage and provided as the bit-decision.

The reason for choosing a dynamic comparator as the single-bit quantizer is as follows. Compared with the commonly-used static comparators consisting of preamplifiers [38], the well-known shortage of the described dynamic comparator is the relatively large input-referred offset due to process variations and device mismatches, as well as the kick-back noise caused by large voltage variations on regeneration nodes [79]. When applied in incremental ADCs, however, the offset and noise of the bit-decision comparator are both suppressed by the high loop gain of the $\Delta\Sigma$ loop-filter, as is the case with the quantization error. Therefore, the requirement on the comparison accuracy of the $\Delta\Sigma$-loop quantizer is much relaxed, and the shortcomings of dynamic comparators can be tolerated. Moreover, the dynamic comparator enjoys a better amenability to the low-voltage (1V or even lower) operation thanks to its dynamic nature, while the lower-limit of the preamplifier supply voltage is critically restricted by the threshold voltages of transistors. Last but not least, the dynamic comparator requires no DC power consumption during operation, which is favorable for energy-efficient designs.

5-2-4 Biasing Circuit

A constant-g_m biasing circuit [37] is used to produce the reference current for the gated current sources and the tunable delay element in digital circuits (Figure 4-16). As indicated in Figure 5-4, a pair of NMOS transistors (M_1, M_2) with different dimensions are fed from an equally-sized PMOS current mirror (M_3, M_4). The difference between the gate-source voltages of M_1 and M_2 produces a bias voltage across the tail resistor R_bias , thus defining a transconductance that is first-order constant with the supply voltage and the MOS device parameters.

By neglecting the impact of body effects on the transistor threshold voltages, the bias voltage across R_{bias} equals to the difference between the overdrive voltages of M_1 and M_2. Suppose that both transistors operate in strong inversion, one gets [80]:

$$V_R \approx \sqrt{\frac{2I_{\text{out}}}{\mu_{\text{n}}C_{OX}(W/L)_1}} - \sqrt{\frac{2I_{\text{out}}}{\mu_{\text{n}}C_{OX}(W/L)_2}} \tag{5-3}$$

where μ_{n} and C_{OX} represent the carrier mobility and oxide capacitance per square of the NMOS transistors respectively, and $(W/L)_1$ and $(W/L)_2$ are aspect ratios of M_1 and M_2. Providing that $(W/L)_1 = k \cdot (W/L)_2$, the output current of the bias circuit can be described by [37]:

$$I_{\text{out}} = \frac{1}{R_{\text{bias}}^2} \cdot \frac{2}{\mu_{\text{n}}C_{OX}(W/L)_1}\left(1 - \frac{1}{\sqrt{k}}\right)^2 \tag{5-4}$$

Hence, the transconductance of M_1 is given by

$$\begin{aligned} g_{\text{m1}} &= \sqrt{2\mu_{\text{n}}C_{OX}(W/L)_1 I_{\text{out}}} \\ &= \frac{2}{R_{\text{bias}}}\left(1 - \frac{1}{\sqrt{k}}\right) \end{aligned} \tag{5-5}$$

which is independent of the supply voltage and MOS device parameters. In reality, the variation of R_{bias} with temperature and process might slightly degrade the consistency and accuracy of the transconductance achieved.

The value of the output current is chosen in line with the smallest fine-phase charging current, i.e. 100nA. This requires for a relatively large R_{bias}, which can be implemented with serpentine-shape polysilicon resistors in practice.

A low-voltage start-up circuit is included to drive the constant-g_{m} circuit out of its zero-current degenerate bias point [37] when the supply is turned on. Shown in Figure 5-4, this circuit is composed of transistors M_5, M_6 and M_7, where M_6 is a narrow and long PMOS device ($W/L = 1 : 400$) with grounded-gate. Upon start-up, M_6 is turned on immediately and raises the gate voltage of M_5, thus providing an auxiliary current path from M_4 to ground via M_5 and kicking off the biasing generator. Afterwards, M_7 is turned on as well, which pulls down the gate voltage of M_5 and hence cuts off the auxiliary current path. The static current flowing in the branch of M_6 and M_7 can effectively limited by the large channel resistance of M_7. What's more, a small Miller capacitor C_M is added across M_6 to prevent undesired ringing artifacts at the start-up moment.

5-2-5 Clock Boosting

To ensure the proper operation of single-transistor switches at low supply voltages, the clock-boosting technique [81][75] is applied. Figure 5-5 presents a classical implementation of a single-output clock booster [10] . It consists of a charge-pump circuit with feedback mechanism provided by a pair of cross-coupled NMOS devices (M_1, M_2) [81], as well as an output inverter

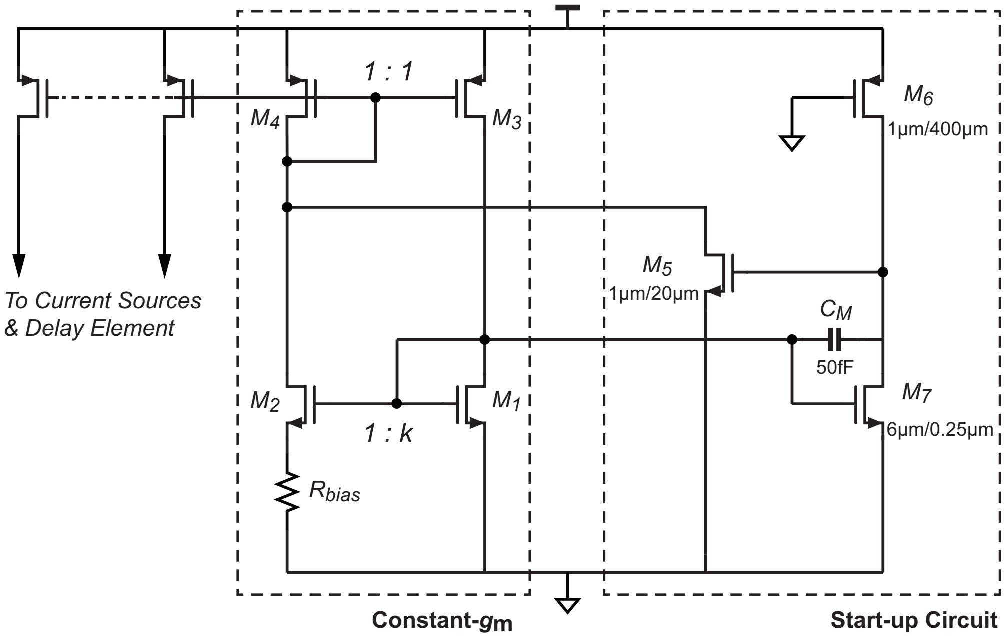

1 : 1
M4
M3
M6
1µm/400µm
M5
1µm/20µm
To Current Sources
& Delay Element
CM
50fF
M2
M1
1 : k
M7
6µm/0.25µm
Rbias
Constant-gm
Start-up Circuit

Figure 5-4: Schematic of the reference biasing current generator and the associated start-up circuit.

(M_3, M_4) powered by the boosted voltage. The nwell of M_3 is deliberately connected to its source terminal. When a square-wave input signal with a high voltage at V_{DD} is applied, the voltages on the boosting capacitors (C_{b1}, C_{b2}) are both self-charged to and maintained at V_{DD}, thus generating a copy of the input clock with a doubled voltage ($2V_{DD}$) at the output. In situations where complementary clocks are to be boosted, a dual-output clock booster shown in Figure 5-6 can be applied.

In practice, the actual voltage boost-ratio is affected by the parasitic capacitance at the

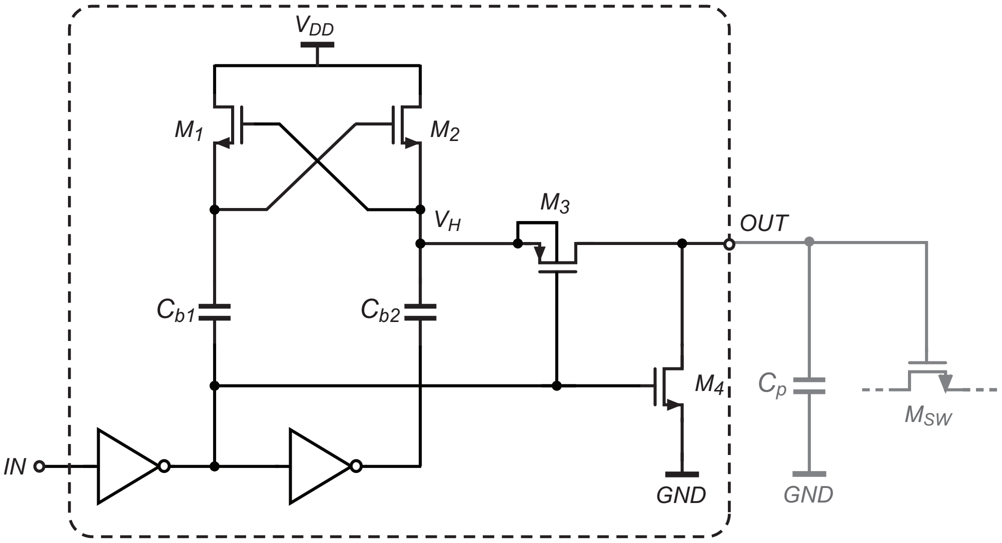

VDD
M1
M2
VH
M3
OUT
Cb1
Cb2
M4
Cp
MSW
IN
GND
GND

Figure 5-5: Schematic of single-output clock booster [10]

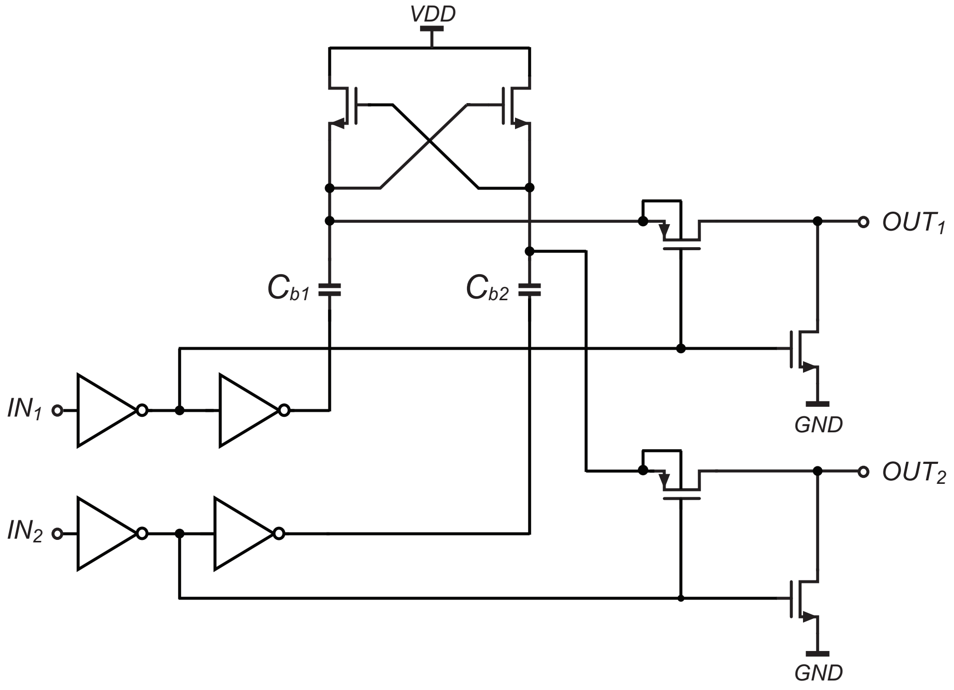


Figure 5-6: Schematic of the clock booster with double outputs

output node, which includes the gate capacitance of the driven NMOS switch(es) (M_{SW}) and the wiring parasitics associated with layout. This effect can be estimated with the equation below [10] :

$$\frac{V_{\mathrm{boost}}}{V_{DD}} = 2 \cdot \left(1 - \frac{C_{\mathrm{p}}}{C_{\mathrm{b2}} + C_{\mathrm{p}}}\right) \tag{5-6}$$

where C_{p} represents the total parasitic capacitance at the output of the clock-booster.

As revealed by (5-6), the existence of C_{p} brings a reduction factor to the voltage boost-ratio. A possible profit from this side effect is that, the existence of C_{p} might help in ensuring the reliability of the transistor whose ate is driven, M_{SW}, as long as the maximum allowable gate oxide voltage in the specify technology is not larger than two times of the supply voltage[3]. However, an overhead reduction of the boosted voltage can also dramatically increase the on-resistance of M_{SW}, which is definitely undesired. Based on the above considerations, a careful sizing of the boosting capacitors and a valid estimation of the layout parasitics are definitely necessary in practice.

5-3 Design for Testability

A testing-friendly chip should be sufficiently tunable and observable. To increase the accessibility and adjustability of the sub-circuits as well as to enable the chip to work in multiple operation modes, a set of design-for-testability (DFT) circuit techniques is included in the prototype design, which significantly improve the testing efficiency. An overview of these techniques is given in this section.

---

[3] This is the case in the design of prototype chip. The maximum allowable gate oxide voltage of the 0.16μm CMOS technology is 1.95V, while the supply voltage is 1V.

Analog Output Buffer for Internal-Node Probing

To facilitate observing the voltage waveforms of internal nodes without disturbing the normal circuit operation, such as the output nodes of switched-capacitor integrators and zero-crossing detectors, on-chip analog output buffers are utilized. As illustrated in Figure 5-7, the kernel of such an analog output buffer is a PMOS source-follower (M_{SF}), which is driven by a constant current source on the testboard. The source of M_{SF} is directly connected to a test I/O pad without any electrostatic discharge (ESD) protective devices[4]. Thereby, the voltage waveform on the gate of M_{SF} can be reproduced at the test I/O pad, albeit level-shifted, which can be readily probed. Regarding the heavy capacitive load on the I/O pad (C_{PAD}), a large transconductance of M_{SF} is called for to ensure that the source-follower is fast enough to track the probed signal [37].

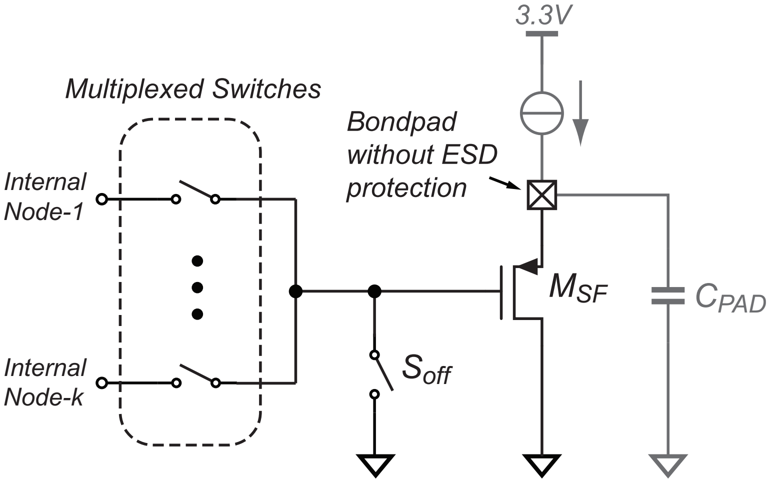


Figure 5-7: Schematic of the analog output buffer for internal-node probing

To increase the hardware efficiency, multiplexed switches are introduced so that each source-follower (and the associated test I/O pad) can be used for probing multiple internal nodes. These switches are controlled by the corresponding bits in the configuration command (see Table 5-2). When analog probing is not needed, all multiplexed switches can be turned off, and the input of the source-follower is grounded by a NMOS switch (S_{off}) to prevent undesired floating.

Shift-Register for Chip Configuration

A serial-in, parallel-out shift-register with output registers (Figure 5-8(a)) is used for the start-up configuration of the prototype chip. This is an I/O-efficient approach to endow the chip with multi-mode functionality, as only three extra digital I/O pins are needed: a command word serial input (*CMD_IN*), a command word read-in clock (*CMD_CLK*) and a configuration enable trigger (*CMD_EN*). The length of the shift-register equals to that of the configuration command word.

---

[4] In other words, the test I/O pad is simply a piece of metal.

Figure 5-8(b) shows the operation timing diagram of the proposed circuit. Before the core circuits (i.e. the $\Delta\Sigma$ modulator, the digital state-machine, and the biasing circuit) are started up, an n-bit configuration command word, which can be generated from an FPGA or data-acquisition device (DAQ), is serially written into the shift-register in pace with the external clock *CMD_CLK*. Upon completion, the contents of the shift-register are transferred to the separated registers on the rising edge of *CMD_EN*. The outputs of these registers ($CMD_{1\sim n}$) are then available for the configuration of the core circuits.

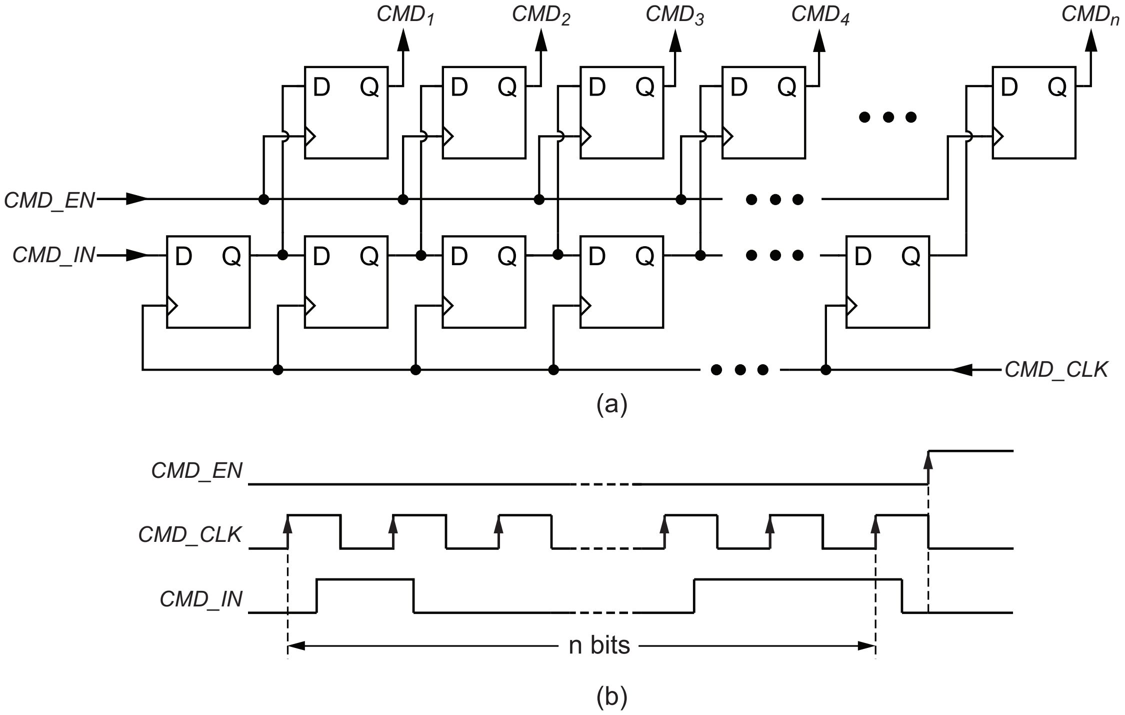


Figure 5-8: (a) Schematic of the configuration shift-register (b) Operation timing diagram

In the prototype chip design, a 22-bit configuration word is defined, which can be divided into 7 segments. The functionality of each segment is listed in Table 5-2.

5-4 Layout

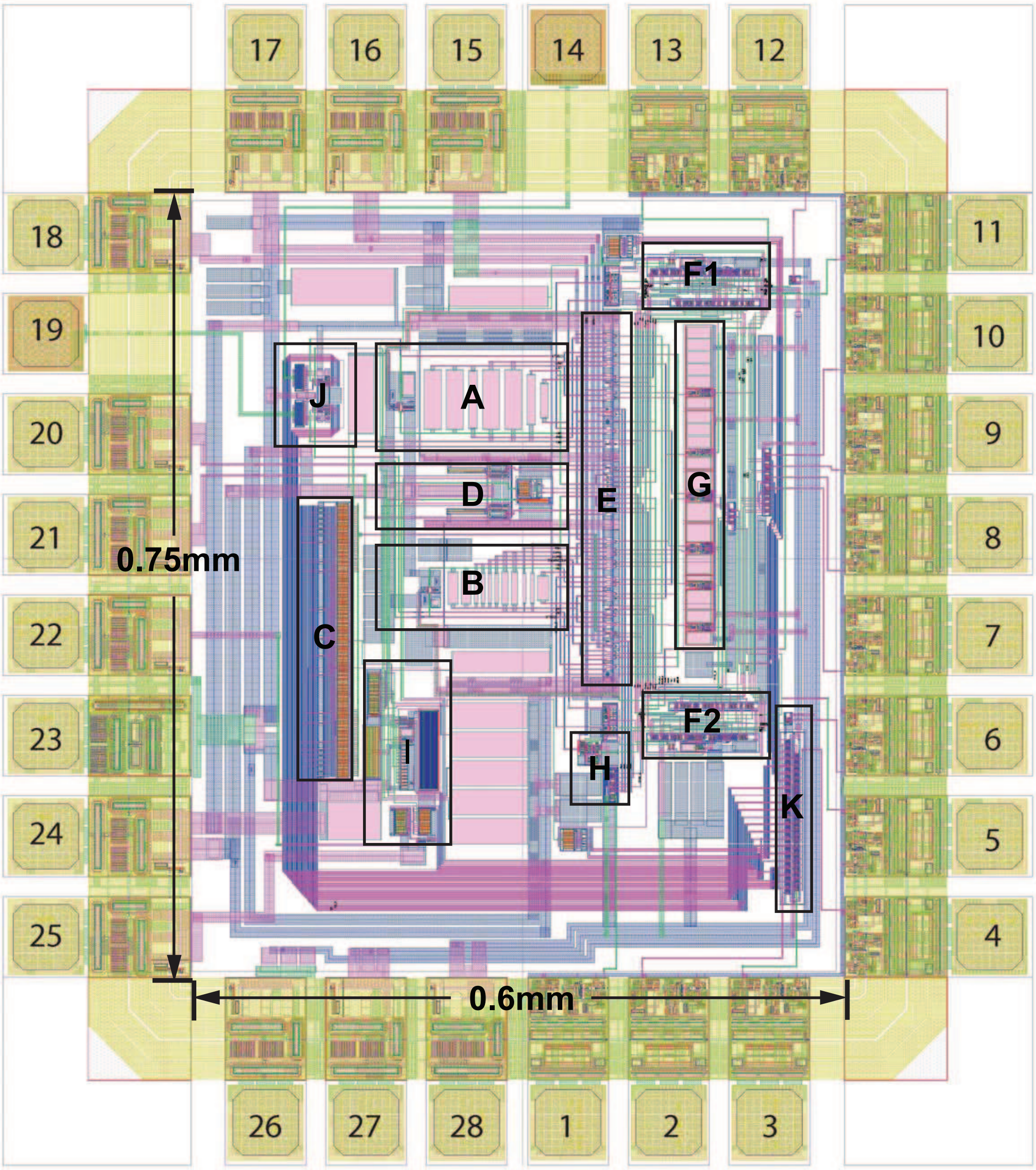
Figure 5-9 shows the layout diagram of the prototype ADC with critical sub-blocks labeled. The active area occupies 0.45mm^2 (0.6mm × 0.75mm). 28 I/O pads are used, in which 13 are digital, 13 are analog and 2 are metal pads without ESD protections for the analog output buffers.

Table 5-2: Contents of the 22-Bit Command Word

Segment	Bits	Function
1	1∼6	Enable or disable the analog output buffers of the output voltages of integrators and zero-crossing detectors.
2	7∼8	Choose between the on-chip and off-chip current references for the biasing circuits.
3	9	Enable or disable the on-chip offset generators for the early-threshold detection.
4	10∼15	Control the magnitude of the coarse charging current in each integrator with 3-bit dynamic range.
5	16∼19	Control the duration time of the preset delay in each integrator with 2-bit dynamic range.
6	20	Switch the $\Delta\Sigma$ modulator between the self-timed and synchronous operation mode.
7	21∼22	Control the digital output multiplexer.

5-5 Summary

This chapter has provided a top-down review of the implementation details of the prototype chip. Starting from a bird-eye view of the system level design, it has dug into the system by investigating the design of sub-blocks one-by-one. A set of techniques for enhancing the circuit's testability have also been introduced.


17
16
15
14
13
12
18
11
19
10
20
9
21
8
22
7
23
6
24
5
25
4
26
27
28
1
2
3
F1
J
A
G
D
E
C
B
0.75mm
I
F2
H
K
0.6mm

A: 1st Integrator **B**: 2nd Integrator **C**: Coarse Current Source **D**: Fine Current Source

E: Switches **F1/F2**: State-Machine **G**: Clock Boosters **H**: Bit-decision Comparator

I: Biasing **J**: Analog Output Buffer **K**: Shift-Register

Figure 5-9: Layout of the prototype ADC in 0.16μm 1P6M CMOS

Chapter 6

Experimental Results

This chapter presents the details of the prototype measurement. The testing of high-resolution ADCs is never an easy job; it's by no means a "black magic" [82] but requires a lot of efforts and knowledge in both hardware and software design. As such, a brief introduction to the setup of the measurement system is first given. That is followed by a presentation of measurement results about the commonly concerned specifications of incremental ADCs, such as resolution, linearity, measurement time and power consumption. A performance summary of the prototype chip is given at the end.

6-1 Measurement Setup

An overview of the measurement setup is presented in Figure 6-1. The kernel of the measurement system is a National Instrumentation USB-6259 M-series data-acquisition device (DAQ), which is controlled by PC-based Labview and the associated DAQ software. It governs the initialization of each one-shot conversion, the configuration of the 22-bit on-chip shift-register (Section 5-3) and the capture of the self-timed bitstream. Besides, the decimation of the bitstream is processed using an embedded C-program in Labview.

An Altera Cyclone-IV E-series FPGA (EP4CE22E22C6) is employed to implement the incremental cycle-counting, as well as non-timing-critical parts of the asynchronous state-machine and a watch dog timer which is able to reset the self-timed ADC in fault conditions. It also performs as a logic buffer between the TTL-level digital I/O ports of the DAQ [83] and the 1V I/O pins of the prototype chip[1]. To ensure the robustness of the inter-chip data communication, the FPGA is implemented together with the prototype ADC on a custom-designed testboard. The details of the testboard design are described in Appendix A.

The DC input voltage for the prototype ADC is generated by using a precision, low-noise current flowing through an on-board resistor (or I-V converter). This current is derived

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[1] Cyclone-IV E-series FPGA supports multiple I/O supply voltages for different I/O banks, ranging from 1.2V to 3.3V [84][85]. The rest of the logic level difference is bridged by a set of commercial bidirectional voltage translators.

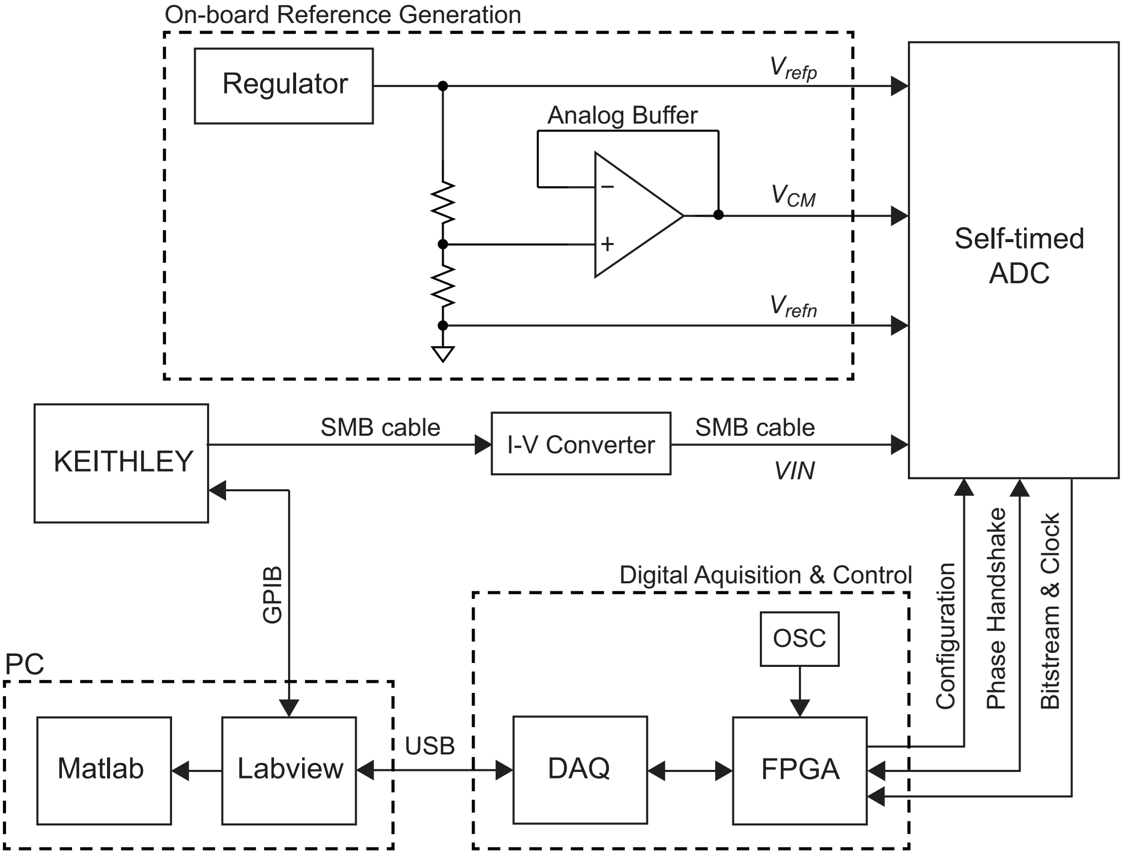
On-board Reference Generation
Regulator
V_{refp}
Analog Buffer
−
+
V_{CM}
V_{refn}
Self-timed ADC
KEITHLEY
SMB cable
I-V Converter
SMB cable
VIN
GPIB
Digital Aquisition & Control
Configuration
Phase Handshake
Bitstream & Clock
OSC
PC
Matlab
Labview
USB
DAQ
FPGA

Figure 6-1: Experimental Setup

from a Keithley-2400 precision current source meter, which can either generate or measure back a constant current with extremely low noise spectral density. The set-up of the output current magnitude and the read-out of the measured data can both be performed in Labview via a General Purpose Interface Bus (GPIB). This feature facilitates the automation of the linearity test (see the next section).

Furthermore, the ADC reference voltages, including the the modulator feedback references (V_{refp}, V_{refn}) and the common-mode voltage (V_{CM}), are all generated using on-board potentiometers, analog buffers and a low-noise regulator, as also depicted in Figure 6-1.

6-2 Measurement Results

This section presents the measurement results of the prototype ADC. Figure 6-2 shows a die micrograph with key areas identified.

6-2-1 Bitstream FFT

Figure 6-3 shows an FFT of the measured bitstream with a Kaiser window applied. As expected, a second-order noise-shaping is clearly shown in the plot.

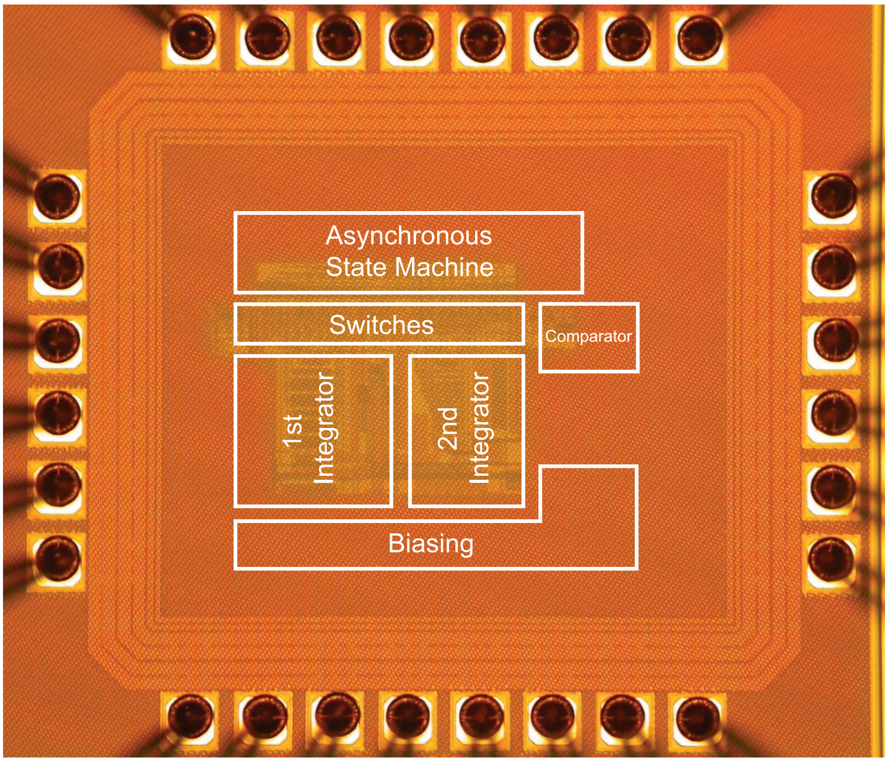

Figure 6-2: Die microphotograph with identifications of key areas

Note that due to the self-timed nature, the ADC does not have any fixed sampling frequency. As a result, the horizontal axis of the FFT plot is defined as the normalized frequency with respect to the average sampling frequency at the test input, which is given by

$$\mathcal{F}_{\text{average}} = \frac{M}{T_{\text{conv}}} \tag{6-1}$$

where M is the number of incremental cycles and T_{conv} is the corresponding conversion time.

6-2-2 Resolution

The derivation of ADC resolution was based on the measurement of the input-referred RMS noise. The latter was determined by performing 1000 conversions at a single input voltage and calculating the sample-to-sample standard deviation of the decimated outputs. As such, the resolution of the incremental ADC can be defined as follows:

$$\text{Resolution(bits)} = \left(20 \cdot \log \frac{\text{Stable Input Range}}{\delta_{\text{rms}}} - 1.76\right) \Big/ 6.02 \tag{6-2}$$

where δ_{rms} is the standard deviation of the decimated outputs.

Figure 6-4 shows the measured resolution of the ADC as a function of the number of incremental cycles M used to obtain a single decimated output. At $M = 500$, the ADC achieves a resolution of 14.8 bits, which corresponds to an input-referred RMS noise of 19.9μV with

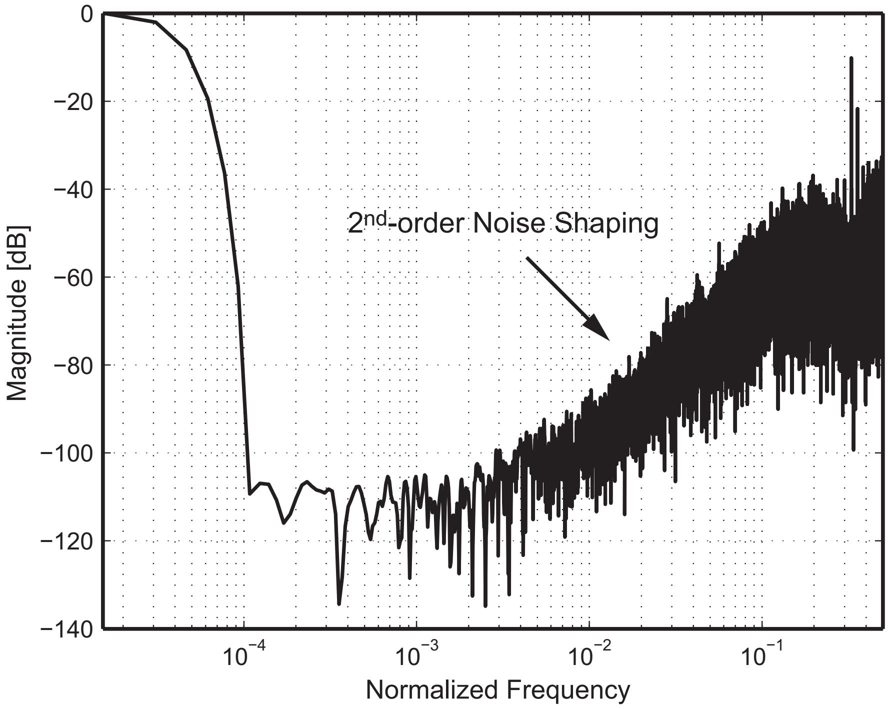

Figure 6-3: Measured FFT of 2^{16}-point bitstream with Kaiser window (frequency normalized to the average sampling frequency 750kHz).

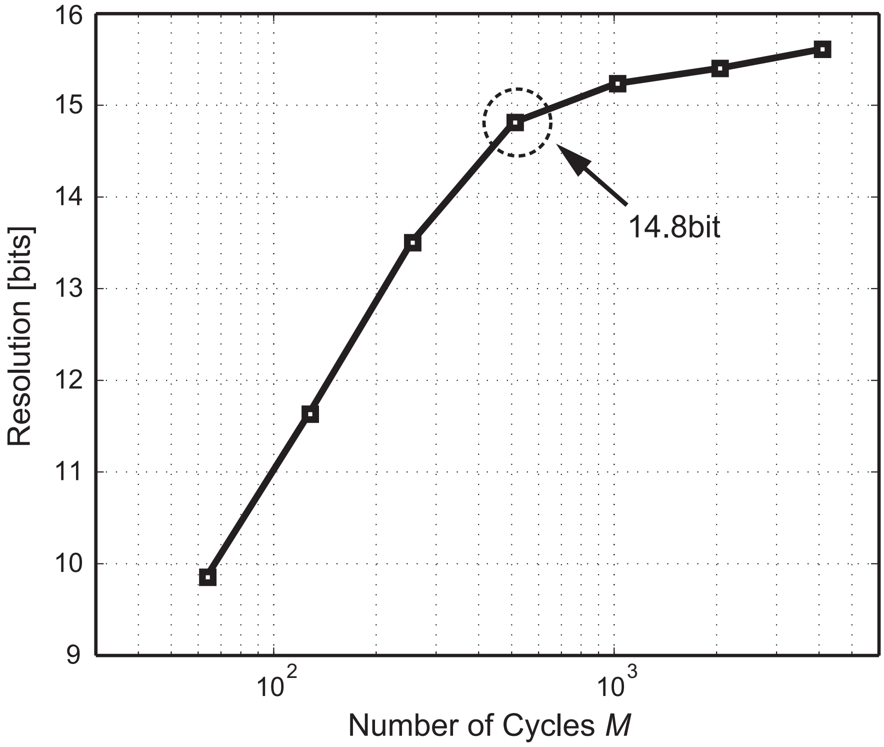

Figure 6-4: Measured ADC Resolution as a function of the number of cycles M.

respect to a stable input range of 0.7V. For shorter conversions ($M < 500$), it is quantization-noise limited[2], while above ($M > 500$) it is thermal-noise limited.

6-2-3 Linearity

The linearity measurement was performed by sweeping the DC-input signal across the stable input range and recording the decimated outputs. The ADC's integral nonlinearity (INL) [67] can then be obtained by calculating the point-to-point deviation between the decimated outputs and the first-order polynomial fitting curve.

In practical operation, the imperfections of the experimental equipments and all kinds of environmental interference can ruin the measured linearity. As countermeasures to these problems, several engineering approaches were utilized:

- Take multiple samples at each input voltage step and average the decimated outputs, thus minimizing the disturbance of noise on the measured data;
- Measure back the generated DC input voltage using a precision analog volt meter at each input step. In this way, the precision analog meter performs as a reference ADC, whose conversion results can be used to calibrate the inherent non-linearity of the input voltage ramp. The Keithley-2400 source meter is a perfectly adequate instrument for this task;
- To avoid picking-up undesired low-frequency frequency components, the time-interval between two adjacent ADC conversions is minimized. Moreover, the measure-back operation is interwoven with the ADC conversions for the same reason.

Figure 6-5 plots the measured INL of the prototype ADC, which is within -0.6 LSB to 0.4LSB with respect to 14-bit output codes. This result well demonstrates the effectiveness of the CLS technique and the associated design choices.

Figure 6-5 also shows the conversion time as a function of the DC input voltage, which is less than 0.75ms. Due to the self-timed nature of the ADC, the charge-transfer times and hence the duration of the clock phases and the total conversion time are slightly signal dependent.

6-2-4 Performance Summary

Table 6-1 summaries the performance of the prototype ADC. To quantify the energy-efficiency and facilitate the comparison with other ADCs, two types of figures of merit (FOM) are widely used in the open literature. The one we have presented in previous chapters is

$$\mathrm{FOM}_1 = \frac{\mathrm{Power}}{2 \cdot \mathrm{Bandwidth} \cdot 2^{\mathrm{ENOB}}} \tag{6-3}$$

where ENOB (bits) is associated with the Signal-to-noise and distortion ratio (SNDR) (dB):

$$\mathrm{ENOB} = (\mathrm{SNDR} - 1.76)/6.02 \tag{6-4}$$

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[2] According to (4-9), the quantization noise of a second-order incremental $\Delta\Sigma$ ADC is inversely proportional to M^2, which is line with the measured result when $M < 500$.

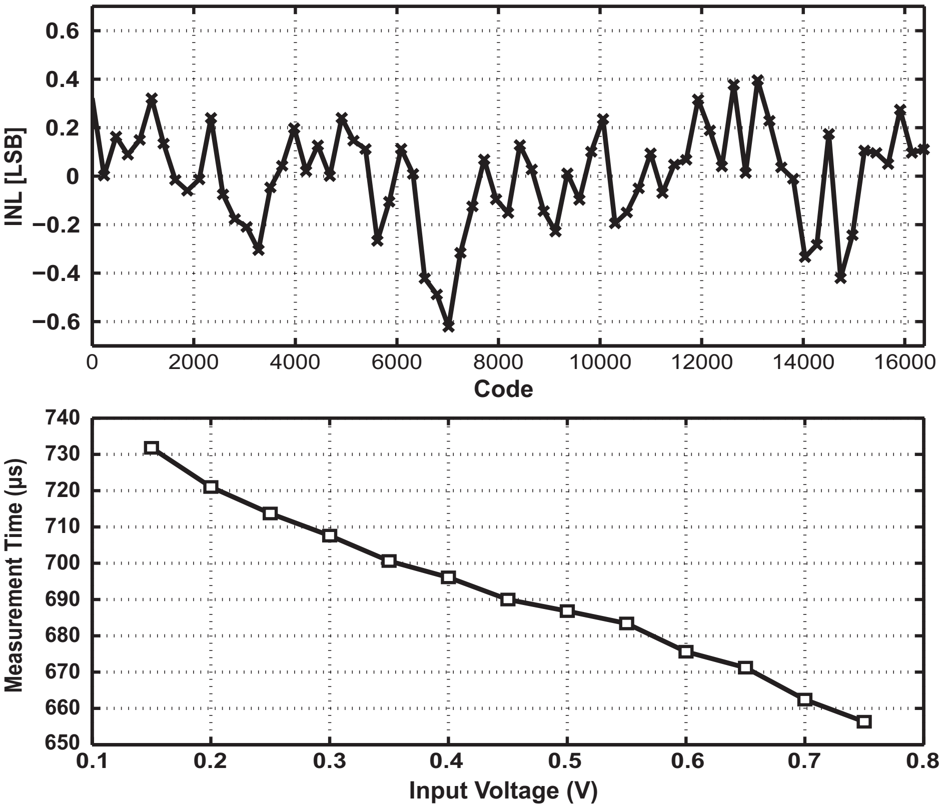

Figure 6-5: Measured INL and conversion time as function of input voltage

Expression (6-3) was first proposed by Walden in [86] and [87], thereby it is also referred to as "Walden FOM" [88]. It is based on the assumption that the ADC energy consumption increases by 2 times per bit of ENOB, which is derived from empirical facts in medium-resolution (SNDR < 70dB) ADCs [88].

The other type of FOM was suggested by Schreier in [58], being

$$\mathrm{FOM}_2 = \mathrm{DR} + 10 \cdot \log\left(\frac{\mathrm{Bandwidth}}{\mathrm{Power}}\right) \tag{6-5}$$

where DR is the dynamic range in dB. In contrast to the Walden FOM, the Schreier FOM assumes that the ADC energy consumption increases by 4 times per bit of DR, while the impact of distortions are not taken into account. It is particularly suited for use in evaluating high-resolution ADCs, in which the conversion resolution is dominated by the thermal noise [88].

For the evaluation of incremental ADCs, (6-3) and (6-5) can both be followed, except that the nyquist-rate bandwidth should be equivalently transformed to the inverse of the conversion time. Hence we have the following definitions:

$$\mathrm{FOM_W} = \frac{\mathrm{Power} \cdot \mathrm{T_{conv}}}{2^{(\mathrm{SNR}-1.76)/6.02}} \tag{6-6}$$

Table 6-1: Performance Summary

Specification	**Performance**
Technology	NXP 0.16μm 1P6M CMOS
Active Chip Area (mm^2)	0.45
Supply Voltage (V)	1
Supply Current (μA)	Analog: 10 Digital: 9.8
Conversion Time (ms)	< 0.75
Stable Input Range (V)	0.15 .. 0.85
Input-Referred RMS Noise (μV)	19.9
INL (LSB)	-0.6 .. 0.4†
FOM$_\mathrm{W}$ (pJ/conversion-step)	1.48
FOM$_\mathrm{S}$ (dB)	157.1

† Relative to a 14-bit output code.

and

$$\mathrm{FOM_S} = \mathrm{SNR} + 10 \cdot \log \frac{1}{\mathrm{Power} \cdot \mathrm{T_{conv}}} \tag{6-7}$$

Here the the signal-to-noise ratio takes the place of the dynamic range in (6-5), as DR $\approx$ SNR when the ADC is thermal-noise dominated.

Regarding the DC-input characteristic of incremental ADCs, the definition of SNR is slightly different with the convention:

$$\mathrm{SNR} = 20 \cdot \log \frac{\text{Input Range}}{2\sqrt{2} \cdot \text{Input Referred RMS Noise}} \tag{6-8}$$

where a crest factor correction of $2\sqrt{2}$ is included to enable a fair comparison with general-purpose ADCs that are characterized using a full-scale sine input.

As has been pointed out in Section 6-2-2, the prototype ADC is actually operating on the boundary of thermal-noise and quantization-noise dominated regions. As such, both Walden FOM and Schreier are presented in Table 6-1. It results in a Walden FOM of 1.48pJ/conversion-step and a Schreier FOM of 157.1dB. This energy-efficiency is comparable with the best (non-self-timed) $\Delta\Sigma$ modulators employing comparable zero-crossing-based circuits ([24] and [43] in Table 2-2), while it achieves a higher linearity.

6-3 Summary

The measurement details of the self-timed incremental ADC prototype are described in this chapter. The correctness and effectiveness of the circuit topologies discussed in previous chapters got fully tested and verified. It was proved that the self-timed timing methodology can be applied to the implementation of high-resolution and energy-efficient incremental $\Delta\Sigma$ ADCs. Operating without external clocks, the prototype ADC achieves a 14-bit linearity and a 14.8-bit resolution with 500 cycles, while only consuming 19.8μA from a 1V supply. Such a performance, together with the clock-less feature, makes the self-timed incremental ADC an attractive candidate for analog-to-digital conversions in energy-constrained sensing applications.

Chapter 7

Conclusion

7-1 Thesis Contribution

A clock-free self-timed incremental $\Delta\Sigma$ ADC targeted for energy-constrained sensor applications has been proposed in this thesis. This self-timed feature is achieved by taking advantage of a zero-crossing based switched-capacitor $\Delta\Sigma$ modulator and entrusting its timing control to an asynchronous state-machine. The elimination of dedicated external clocks can not only reduce the complexity of the A/D interface, but also brings benefits to the energy efficiency.

As a proof-of-concept, a prototype ADC has been implemented in a 0.16μm CMOS process and achieves expected performance. A set of advanced circuit techniques are involved and have been verified in silicon as well. With this result, we successfully demonstrate that:

- **The mixed-signal self-timed approach is suitable for the design of $\Delta\Sigma$ ADCs.**

  By employing zero-crossing based circuits to implement the discrete-time integrators in $\Delta\Sigma$ loop-filters, the completion of the charge-transfer process can be detected by the zero-crossing detectors. This feature can be used to trigger the transitions between clock phases, and on that basis, a self-timed two-state cycling in the timing logic can be readily realized via proper logic design.

- **Zero-crossing based circuits are adequate for the implementation of incremental $\Delta\Sigma$ ADCs.**

  Incremental $\Delta\Sigma$ ADCs are specifically designed for DC sensing applications which require high absolute accuracy of conversions, including high linearity, low offset and high resolution. The related performance of zero-crossing based $\Delta\Sigma$ ADCs in previously reported cases, however, is far from satisfying these requirements. The prototype ADC shown in this thesis alters this situation by exhibiting a 14-bit performance in both linearity and resolution, which is better than all the prior designs. It proves the feasibility of applying the zero-crossing based circuit technique to the implementation of high-performance incremental ADCs.

- **An inverter-based zero-crossing detector is feasible for ZCB integrators.**

  The CMOS inverter is attracting more and more attention from analog circuit designers, owing to its amenability to low-voltage operation and the doubled current-efficiency. In this thesis, an inverter-based zero-crossing detector is used to further improve the ADC's energy-efficiency, which also extends the application scope of inverter-based analog circuits. Being operating in a non-steady-state fashion, the inherent dynamic biasing capacity of the inverter-based ZCD further reduces unnecessary energy-dissipation during the charge-transfer process, which is an extra advantage of this technique.

- **The correlated level shifting technique is a valid solution for addressing the linearity problem of ZCB integrators.**

  The main performance bottleneck of ZCB integrators is the non-linearity caused by ramp-rate variations of the current sources. As a countermeasure, the correlated level shifting technique is applied in the prototype design to boost the equivalent output impedance of current sources, thus improving the charge-transfer linearity. With the effectiveness successfully proved by the measurement result, the CLS technique is expected to be widely adopted in future applications of ZCB circuits.

Supported by all the above achievements, we have reasons to believe that the self-timed incremental ADC is a promising concept for future event-driven sensing and instrumentation applications.

7-2 Future Work

Beyond the prototype chip, the proposed self-timed incremental ADC could be further improved by means of future work at both system and circuit level. A summary of several potential improvements is provided below.

- While this thesis presents a single-ended second-order ADC as a proof-of-concept, the self-timed concept could be readily extended to differential and higher-order loop-filter topologies. In that case, special attention should be paid to the local-synchronization between the differential branches and different stages which operate in the same phase.

- The offset resulting from the finite response time of zero-crossing detectors is not taken into account in the prototype design. In future differential implementations, this deficiency can be made up by introducing choppers into the gated current sources, which dynamically exchange the charging current directions thus removing the overshoot-induced offset. The flicker noise generated from the current source can also be suppressed by the chopping operation.

- The self-timed incremental ADC can be readily applied to the implementation of event-driven sensor interfaces, e.g. for temperature and humidity sensors. In these situations, a specific start-up module should be implemented at the sensor front-end to determine when to kick off the self-timed conversions.

- While the prototype chip is fabricated in a 0.16μm CMOS process with a 1V supply, it is definitely feasible to implement the self-timed incremental ADC using a more advanced technology with smaller feature size and an even lower supply voltage. This is thanks to the fact that both ZCB circuits and inverter-based ZCDs possess the amenability to technology scaling and low-supply operation.

Appendix A

Testboard Design

A custom 4-layer printed circuit board (PCB) is designed to assist the measurement of the prototype chip. It has the following functions:

- Deliver the power supply, input voltage and the associated reference voltages for the prototype ADC;
- Present a hardware platform for the automatic control of the measurement process, e.g. the start-up configuration of the prototype chip;
- Facilitate the capture of the self-timed bitstream.

Figure A-1 shows the layout and components of the testboard. Its “brain” is a Cyclone-IV E-series 144-pin FPGA, which can be configured using a JTAG interface. A +5V DC supply generated by an Agilent E3620A dual-output DC source has been used as the power supply of the whole testboard. It is converted to multiple DC levels (3.3V, 2.5V, 1V) via a set of LDOs to provide power for different modules. Moreover, in order to bridge the logic level difference between the prototype chip and the TTL-level DAQ I/O pins, a row of bidirectional voltage translators have also been implemented on the board.

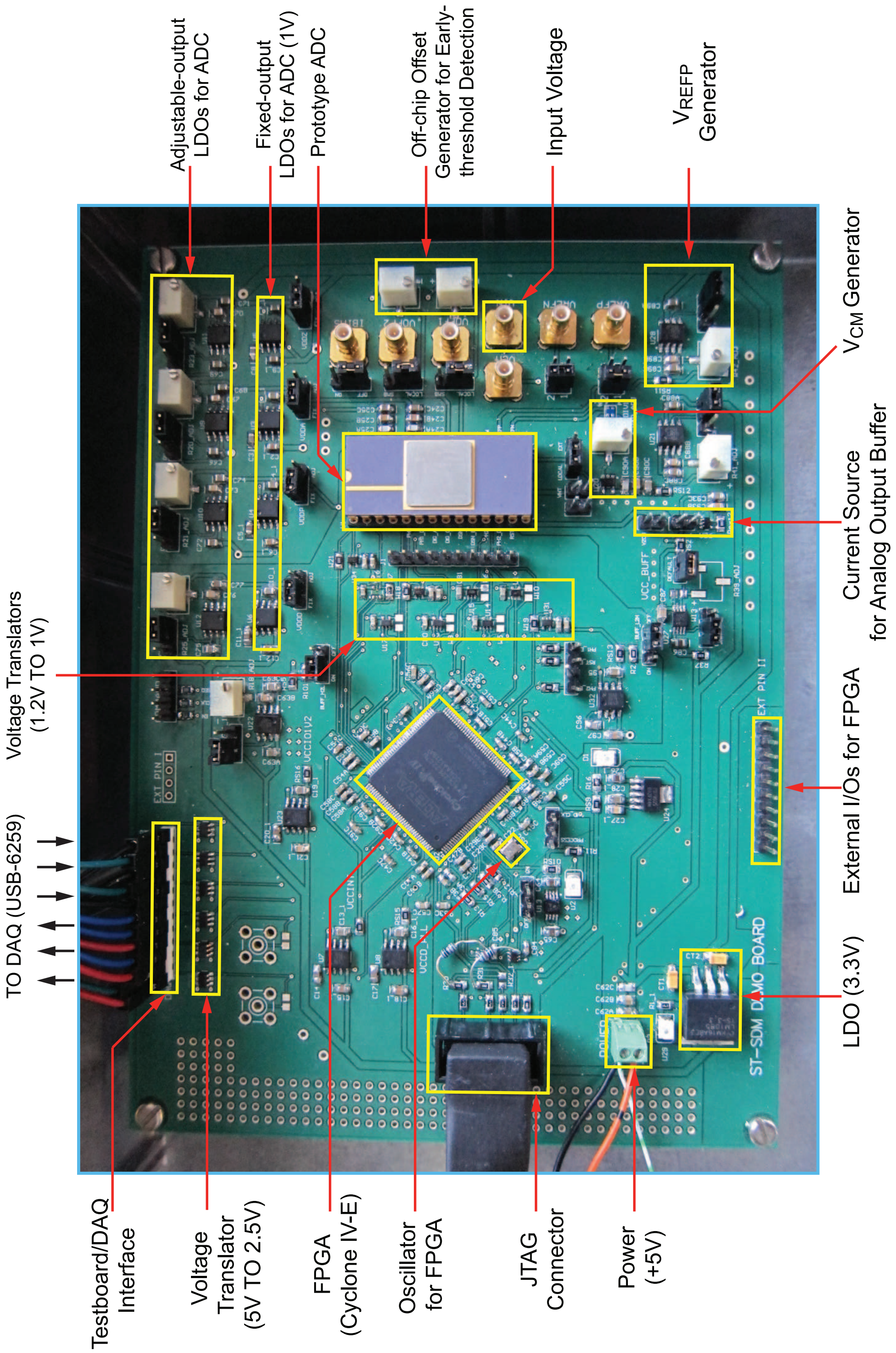
Adjustable-output LDOs for ADC
Fixed-output LDOs for ADC (1V)
Prototype ADC
Off-chip Offset Generator for Early-threshold Detection
Input Voltage
V_{REFP} Generator
V_{CM} Generator
Current Source for Analog Output Buffer
External I/Os for FPGA
LDO (3.3V)
Voltage Translators (1.2V TO 1V)
TO DAQ (USB-6259)
Testboard/DAQ Interface
Voltage Translator (5V TO 2.5V)
FPGA (Cyclone IV-E)
Oscillator for FPGA
JTAG Connector
Power (+5V)
ST-SDM DEMO BOARD

Figure A-1: Testboard Layout and Components.

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Glossary

List of Acronyms

ADC	analog-to-digital converter
ADSM	asynchronous $\Delta\Sigma$ modulator
SC	switched-capacitor
STF	signal transfer function
NTF	noise transfer function
SNR	signal-to-noise ratio
TDC	time-to-digital converter
PVT	process, supply voltage and temperature
MSB	most significant bit
LSB	least significant bit
RMS	root-mean-square
PSD	power spectral density
AZ	auto-zeroing
ZCB	zero-crossing based
CLS	correlated level shifting
PSRR	power supply rejection ratio
OSR	oversampling ratio
PSS	periodical steady-state
PXF	periodical transfer function

SA	succesive-approxiamation
ENOB	effective number of bits
SNDR	Signal-to-noise and distortion ratio
CoI	cascade of integrators
FIR	finite impulse response
FPGA	field-programmable gate array
DEM	dynamic element matching
LDO	low-dropout regulators
ASM	asynchronous state machine
DFT	design-for-testability
DAQ	data-acquisition device
ESD	electrostatic discharge
GPIB	General Purpose Interface Bus
INL	integral nonlinearity
PCB	printed circuit board