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Characterization and Test of Intermittent Over RESET in RRAMs

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***Abstract*—Resistive Random Access Memories (RRAMs) are being commercialized with significant investment from several semiconductor companies. In order to provide efficient and high-quality test solutions to push high-volume production, a comprehensive understanding of manufacturing defects is significantly required. This paper identifies and characterizes the over-RESET phenomenon based on silicon measurements. In our case study, 30% cycles suffered from intermittent extremely high resistance state exceeding the high resistance state criteria. The paper shows the limitations of conventional defect modeling based on linear resistors. To address this challenge, the Device-Aware (DA) defect modeling method is applied; a model of the defective RRAM device is developed and calibrated using measurements to accurately describe the impact of the defect on the electrical behavior of the memory device. Afterward, fault analysis is performed based on the DA defect model, and appropriate fault models are introduced; they show that the DA defect model will sensitize deep (extremely high resistance) state faults. Finally, dedicated test solutions for over-RESET devices are proposed.**

***Index Terms*—RRAM test, device-aware defect model, fault modeling, Design-for-Testability (DfT)**

I. Introduction

Resistive Random Access Memory (RRAM) is a potential technology for the next generation of non-volatile memories, with benefits including high scalability, low access latency, and energy efficiency of AI computing [1]. However, due to the immaturity of the fabrication process, the mass production of RRAM is now facing considerable problems [2]. Defects and variations in device characteristics throughout the manufacturing process, as well as their impact on departing product quality, are widely recognized to be serious obstacles [3–5]. Furthermore, RRAM manufacturing involves additional steps and the use of new materials, which may result in new failure mechanisms [5, 6]. The traditional tests for current mainstream memory technologies are often complicated and not guaranteed to directly detect these RRAM-related faults [5]. Thus, understanding unique RRAM defects and modeling them accurately is of great importance for high-quality tests.

Several works have investigated defect/fault modeling and test generation for RRAMs. In 2012, Haron *et al.* designed a specific Design-for-Testability (DfT) scheme to detect undefined state faults [7]. In 2013, sneak-path testing for RRAMs was proposed to reduce the test time [8]. In 2015, Chen *et al.* reported a dynamic write disturbance fault, and a March test to cover it [9]. In 2022, Hou *et al.* developed a test algorithm to detect two functional faults in the RRAM-based spiking neural network [1]. In 2023, a DfT circuitry was designed to detect both conventional and unique faults [6]. Nevertheless, all these works only consider regular defects that can be modeled by *linear resistors*. Although this model may be good enough for interconnects and contacts, it is certainly insufficient to describe unique defects in the RRAM device itself since the device is inherently *non-linear*. To address the limitations of the conventional RRAM test method, the 'Device-Aware Test (DAT)' approach was proposed [5, 10, 11]. The DAT approach properly models physical defects, allowing for the exploration of realistic fault models and the development of high-quality test solutions. This has been shown to be very powerful for RRAM unique defects such as forming defects [5] and has also led to new test solutions [6]. Moreover, as RRAM is an immature technology, more unique defects are still waiting to be discovered, understood, and modeled in order to develop optimal test methods.

This paper identifies and characterizes the Over RESET (OR) in RRAMs. The OR causes a deep state exceeding the High Resistance State (HRS) criterion intermittently, which is unstable and affects the subsequent switching mechanism. Furthermore, we notice that the tunneling leakage current plays a big role when OR occurs; hence we investigate and model the leakage current based on measurements. The DAT method is applied to accurately model the defects, derive realistic fault models, and thereafter develop efficient test solutions. The main contributions of this paper are as follows:

- Discover an RRAM-specific intermittent OR based on measurements and analyze the physical roots.
- Incorporate the leakage current to improve the RRAM model and develop the DA defect modeling for defects.
- Perform DA fault modeling to develop realistic fault models and thereafter optimal test methods.

The remainder of this paper is organized as follows. Section II establishes the background on RRAM technology. Section III characterizes the OR based on measurements. Section IV incorporates the leakage current into the original RRAM model and proposes the DA defect modeling for the OR. The model is applied in Section V to perform fault modeling and analysis. Section VI develops the test solutions. Finally, Section VII concludes the paper.

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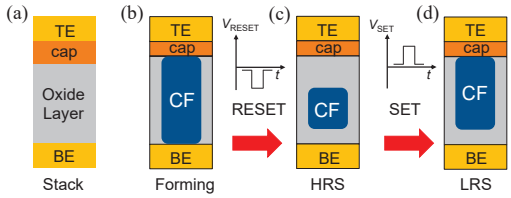


Fig. 1. Evolution of the conductive filament. (a) RRAM stack, (b) Forming, (c) RESET, (d) SET.

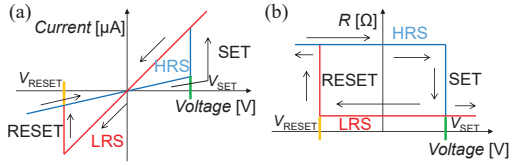


Fig. 2. RRAM electrical switching. (a) Simplified switching I-V curve (in the linear y-axis), (b) Simplified switching R-V curve.

II. Background

As schematically seen in Fig. 1a, an RRAM device is a Metal-Insulator-Metal (MIM) stack [4]. A middle metallic oxide is constructed between the Top Electrode (TE) and Bottom Electrode (BE), with an extra capping (cap) layer. RRAM devices need a forming process, which involves applying a high positive voltage (V_{forming}) between the TE and BE to dissociate a portion of the metal-oxygen ionic bonds [4]. Negatively charged oxygen ions (O^{2-}) are pulled out of the lattice towards the positive anode and accumulate at the cap/oxide interface. Fig. 1b shows a *Conductive Filament (CF)* consisting of positive charged oxygen vacancies (Vo), which is created in the insulator between two electrodes as a result of this localized deficiency.

The switching mechanism depends on the production and dissolution of the CF due to *stochastic* O^{2-} migration [4]. The CF length will increase with a positive voltage from TE to BE (V_{TE}) larger than the specified threshold ($V_{\text{TE}} \geq V_{\text{SET}}$), due to the generation of more Vo, as shown in Fig. 1d, which is called a SET operation [4]. The value of the resistance in SET is R_{SET}. Oppositely, when there is a negative voltage from TE to BE lower than the reset threshold ($V_{\text{TE}} \leq V_{\text{RESET}}$), some O^{2-} drift from the interface back into the bulk oxide to rupture the CF, as shown in Fig. 1c [4], which is called a RESET operation. The value of the resistance in RESET is R_{RESET}. Fig. 2a and Fig. 2b show the simplified I-V curve and the corresponding R-V curve.

The length of CF in the insulator affects the resistance states. For instance, a longer and a shorter CF corresponds to the Low Resistance State (LRS) (logic '1') and HRS (logic '0'), respectively. 'U' represents the intermediate undefined faulty state [7]. Besides, 'L' (the extremely low conductance state) and 'H' (the extremely high conductance state) stand for resistance values higher than an HRS and lower than an LRS, respectively. Therefore, RRAM as an analog device is divided into 5 resistance states (see Fig. 3a) [5, 7].

Fig. 3b illustrates two RRAM cell designs: 1-Resistor (1R) or 1-Transistor-1-Resistor (1T-1R). In Fig. 3b, BL, WL, and SL refer to the bit line, word line, and select line. They are set to appropriate voltages for operations. A sense amplifier (SA) senses the current through the RRAM device as a consequence of providing a read voltage to the cell being read out.

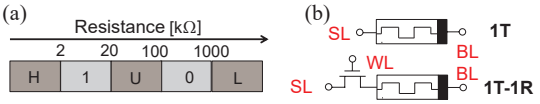


Fig. 3. RRAM technology. (a) RRAM resistance states, (b) 1R, 1T-1R cells.

III. Characterization of over RESET

First, we present the characterization of RRAM devices for the OR phenomenon. Secondly, an overview on the underlying physics and related fabrication processes is provided.

A. Characterization

We measured the electrical characteristics of a 7×7 1T-1R array during 936 RESET-SET cycles on a single wafer. The RRAM devices are manufactured by ST Microelectronics using their $130\,\text{nm}$ technology, with the following structure (BE/oxide/cap/TE) = (TiN/$10\,\text{nm}$ HfO_2/$10\,\text{nm}$ Ti/TiN). One ST Microelectronics in $130\,\text{nm}$ technology NMOS transistor is connected in series to regulate the current through the device. A probe card links the measured 1T-1R device to the Keysight B1500 semiconductor parameter analyzer. In the measurement setup, a $1\,\text{ms}$ DC staircase voltage sweep with a $20\,\text{mV}$ step is applied across the tested device, and the current flow is measured. Logic '1' is defined by the LRS with $2\,\text{k}\Omega < R_{\text{SET}} < 20\,\text{k}\Omega$, and logic '0' by the HRS with $100\,\text{k}\Omega < R_{\text{RESET}} < 1\,\text{M}\Omega$. The intermediate range $[20\,\text{k}\Omega, 100\,\text{k}\Omega]$ is referred to 'U' state. The remaining ranges are defined as 'L' and 'H' states.

While analyzing the measurements, we observe that some cycles of one device suffer from a faulty RESET processes, i.e., the extremely high resistance state after RESET. This occurs for approximately $30\,\%$ of the device's cycles. Fig. 4a represents the $\log(\text{R})$-V loop to characterize and compare defect-free and defective devices. The applied V_{TE} is swept from $0\,\text{V}$ to $-1.8\,\text{V}$ (①, ②), and back to $0\,\text{V}$ (③) for RESET; from $0\,\text{V}$ to $1.2\,\text{V}$ (④, ⑤) back to $0\,\text{V}$ (⑥) for SET. For the defect-free device, the RESET transition starts from $-0.75\,\text{V}$ with a constant LRS and ends at a nominal HRS (around $165\,\text{k}\Omega$). In the case of a defective device RESET switching, a similar transition performance is observed (①, ②). However, its resistance value increases to the extremely high resistance state at ③. Note that the resistance increases since the leakage current decreases as the applied voltage changes. The effect of leakage current is particularly non-negligible when the device is in an HRS (around one order of magnitude resistance increase, see Fig. 4a). The leakage current exists in both RESET and SET processes. The subsequent SET process follows the normal transition for both defect-free and defective devices, but the defective device shows a significantly increased V_{SET}.

Fig. 4b presents the on/off resistance window as a function of cycles for defect-free and defective devices. During the initial ≈ 100 cycles, devices exhibit erratic resistance states, also reported in [3]. After the initial few cycles, the variability of resistance values is low. It can be concluded that the

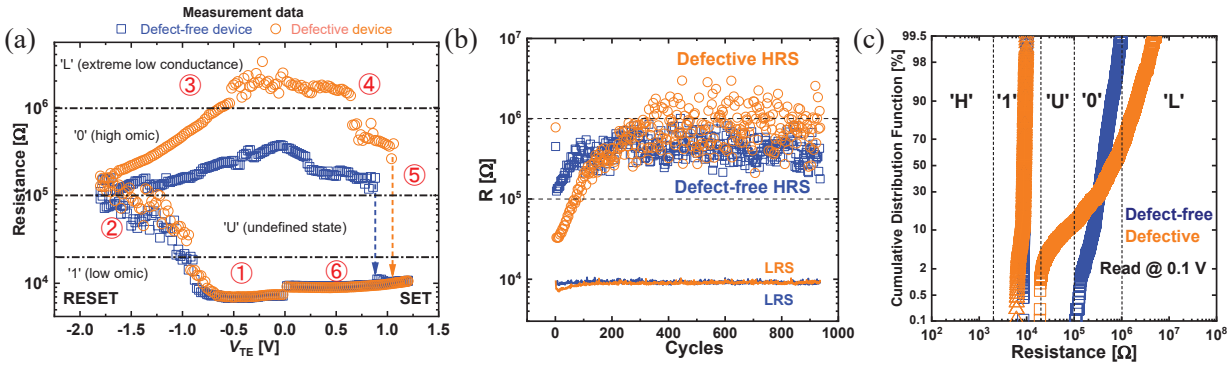


Fig. 4. Comparing defect-free and defective devices. (a) Measured R-V curve in the logarithmic y-axis, (b) Measured R_{RESET} and R_{SET} in multiple (936) cycles, (c) Lognormal distributions of R_{RESET} and R_{SET} in multiple (936) cycles (read at 0.1 V).

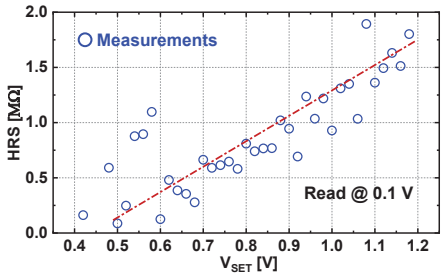


Fig. 5. Dependence of V_{SET} and HRS of the device during 936 cycles.

extremely high HRS occurs in multiple cycles. Fig. 4c presents the cumulative distributions of resistance for the RRAM device with 1T-1R structure. The distributions contain the measured resistance values (read using 0.1 V) from 936 consecutive RESET-SET cycles. The HRS distribution spread is more pronounced than LRS, which is also reported in other papers [12]. Around 30 % cycles of the defective device exceed the HRS resistance criterion of 1 MΩ, exhibiting the extremely high resistance state. Hence, the faulty behavior is intermittent, and it is a serious concern for RRAM devices.

Fig. 5 shows the dependence of measured HRS and subsequent V_{SET} during 936 cycles. For each V_{SET}, the mean of the HRS throughout numerous cycles is obtained in order to depict the trend clearly. It shows that a larger HRS usually corresponds to a larger V_{SET}. It can be explained that the V_{SET} is related to the amount of Vo and affected chemical potential [13]. For example, one reported experiment shows that the low oxygen absorption rate of the insulating TiO_x capping layer leads to high V_{SET} than the metallic Ta capping layer [13]. Therefore, the extremely high resistance fault is risky to cause transition faults during the SET process, especially for low voltage (power) applications.

B. Physical Explanation and Potential Causes

The RRAM switching mechanism is explained as the movement of O^{2-} to form and rupture the CF composed of Vo [4]. The same LRS values of defect-free and defective devices (see Fig. 4a, ①, ⑥) indicate that the same amount of O^{2-} is generated during the SET process. Hence, the extremely high HRS value after RESET must involve a reduced O^{2-} storage capability in the capping layer of the device with respect to the nominal case. A probable cause of the fault is an increase in layer length or a decrease in the cross-sectional area due to extreme process variation [14]. Furthermore, the doped oxygen leads to the high resistivity of the capping layer and provides more O^{2-}, which results in a deeper CF rupture [14]. Since the formation and rupture of a CF are *stochastic processes*, the precise number of O^{2-} fluctuates per write cycle, and hence the fault will not occur in every cycle [3]. Moreover, it is reported that the stochastic variability impacts HRS reliability [15], and hence the intermittent phenomenon.

C. Related Fabrication Processes

In this paper, we consider that the following fabrication processes affect the interface imperfections and can contribute to a shortage of O^{2-} storage capability of the cap.

1) Thickness variations of deposition: The deposition is possible to be conducted with different thicknesses. The thicker cap favors stable switching because of its decreasing work function and increasing oxygen affinity [16]. The proper barrier height formation at the cap/oxide interface is also related to the oxide layer [16]. For example, the over/deep unstable RESET could be observed in thicker oxide. Besides, the thicker oxide layer deposition makes it easy to have a stochastic CF formation process and can contribute to the intermittent behavior [17].

2) Annealing process: The proper annealing treatment can promote the improvement of the crystalline quality of the oxide bulk and increase oxygen content in the capping layer [18]. RRAM switching performance is shown to be related to variations in the hydroxyl group concentration [18]. It has been reported that significant dependence on annealing temperature is apparent at HRS [18]. Hence, inappropriate annealing may cause the deep HRS and unstable RESET process [15], i.e., intermittent OR phenomenon.

IV. Device-Aware Defect Modeling for OR Defect

In this Section, we first notice and incorporate the measured leakage current into the existing RRAM model to better calibrate the device behavior. Then, we analyze the OR-defective affected by the leakage current and apply the DA defect modeling approach to model the OR defect discussed in the previous section to calibrate with the measurements.

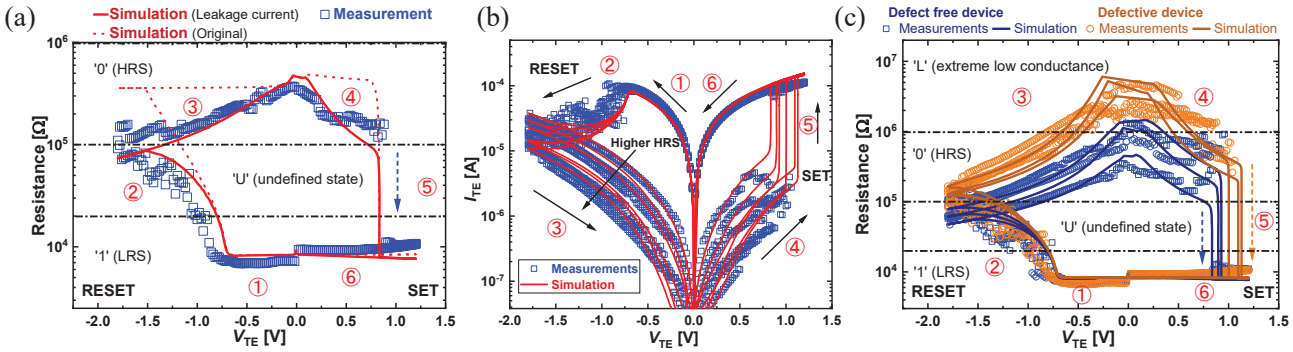


Fig. 6. Defect-free and defective device simulation and measurements. (a) The leakage current incorporated model fitting of the R-V curve, (b) Simulation vs. measurements of the I-V curve, (c) Simulation vs. measurements of the R-V curve.

TABLE I
MODEL PARAMETERS FOR JART VCM V1B [19].

Symbol	Value	Symbol	Value
T_0	0.293 K	ν_0	$1.6 \cdot 10^{13}$ Hz
ϵ_s	10	ΔW_A	1.35 eV
$\epsilon_{\phi_{Bn0}}$	4.5	R_{th0}	$6.5 \cdot 10^6$ K·W^{-1}
ϕ_{Bn0}	0.18 eV	r_{det}	50 nm
ϕ_n	0.1 eV	l_{cell}	2 nm
μ_{n0}	$3 \cdot 10^{-6}$ m^2/(Vs)	l_{det}	0.65 nm
$N_{disc,max}$	$5.3 \cdot 10^{25}$ m^{-3}	$R_{theff,scaling}$	1
$N_{disc,min}$	$2.5 \cdot 10^{23}$ m^{-3}	$R_{series,ICL}$	2050 Ω
N_{init}	$5.3 \cdot 10^{25}$ m^{-3}	R_0	750 Ω
N_{plug}	$5.3 \cdot 10^{25}$ m^{-3}	$R_{th,line}$	90 471.5 W·K^{-1}
a	0.54 nm	α_{line}	$3.92 \cdot 10^{-3}$ K^{-1}

A. Leakage Current Modeling and Incorporation

Section III characterized the leakage current, which affects the current flowing through the device, hence the read resistance states. The impact of the leakage current is noticeable, especially for extremely high resistance states. However, most of the existing RRAM compact models assume the device switches as long as the applied voltage reaches the threshold [4, 19]. After that, the states (resistance) are constant unless the device switches again. Hence, the simulation of extremely high resistance states is less accurate when tunneling currents are not taken into account. Besides, the magnitude of the leakage current is related to the amount of Vo and the resulting HRS, the root of which will be explained in Section IV-C.

In this paper, we apply the physics-based RRAM model, JART VCM v1b, from [19] to incorporate the leakage current and appropriately model the defects. The compact model is designed as the change of Vo (parameter N_{disc}) in the HfO_2 oxide layer. $N_{\text{disc,min}}$ and $N_{\text{disc,max}}$ are limiting parameters to keep N_{disc} between $N_{\text{disc,min}}$ and $N_{\text{disc,max}}$ in RESET and SET processes. To incorporate the leakage current into the model, we transform the leakage current to an equivalent current source, which is a function of applied voltages, and calibrate the current magnitude with measurements.

The leakage current between the cap and the oxide layer in the RRAM device is dominated by the Fowler-Nordheim tunneling mechanism, which is tunneling through an approximate triangle potential barrier. An expression for the current as a function of the applied voltage is [20]:

$$J_{\text{FN}} = \frac{q^3}{16\pi^2 \hbar \phi_b} F_{ox}^2 exp\left[-\frac{4}{3}\frac{\sqrt{2m_{ox}^*}\phi_b^{\frac{3}{2}}}{\hbar q}\frac{1}{F_{ox}}\right] \quad (1)$$

where q is the electron charge, $\hbar$ is Planck's reduced constant, m_{ox}^* is the electron effective mass in the insulator (for HfO_2 of $0.1m_0$ [4]), ϕ_b is the barrier height at the interface, and F_{ox} is the electric field cross the oxide (dependent on the V_{TE}).

The fitting of ϕ_b is carried out with the I-V measurements. We neglect the ionic hopping current caused by the minute amount of Vo and approximate the current flowing through the RRAM as a tunneling current. Table I lists the parameter values used in Fig. 6a for the JART VCM V1b model to calibrate the measurement data. Fig. 6a shows the fitting result and implies that the model is able to accurately describe the R-V loop caused by leakage current.

B. Defect Modeling for the Over RESET

Next, we perform the DA defect modeling for the OR defect by using the leakage current incorporated RRAM model. The DA defect modeling consists of the following three steps.

1) Physical Defect Analysis and Modeling: The physics of the defect must be investigated to comprehend its mechanism and determine its effect on one or more technology parameters of the RRAM device. As we analyzed in Section III, the shortage of the free oxygen affinity causes over RESET in devices, which leads to the extremely high resistance fault. Therefore, we include the faulty final resistance by changing the model parameter that affects the O^{2-} storage capability: the minimal Vo concentration in the oxide (disc). The lower this number, the higher the resistance value and thus the stronger extremely high resistance state faults.

2) Electrical Defect Modeling: Following the physical analysis, the electrical parameters (e.g., the Vo concentration) comprise the impacted physical properties (e,g., R_{RESET}, I_{TE}) in this stage. The Verilog-A-written compact model JART VCM v1b can be directly integrated into the circuit-level simulation. Hence, by connecting it to $N_{\text{disc,min}}$ utilizing model simulations, the electrical behavior of the defective device switching comprising current changes can be examined.

3) Fitting and Model Simulation: The fitting is carried out to match the I (R)-V measurements from Section III. The same parameter values listed in Table I other than $N_{\text{disc,min}}$ are used. In the simulation, the RRAM model is connected in series with a transistor that has the same dimensions as the devices used for characterization. Fig. 6b and Fig. 6c present the fitting results of I-V and R-V loops for both defect-free

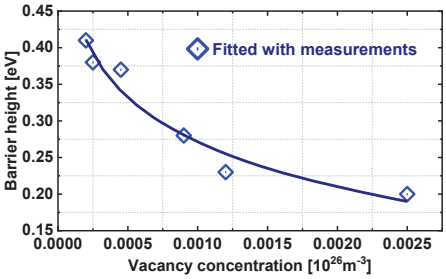


Fig. 7. Reduced tunneling barrier height caused by Vo concentration.

and defective devices. The applied voltage is ramped as in the characterization (① to ⑥), for a RESET-SET cycle. The circuit-level simulation results fit the measurements well.

C. Analysis of the Effective Height Barrier

Furthermore, we investigate the relationship between $N_{\mathrm{disc,min}}$ and ϕ_b, which are two key parameters determining the extreme state fault and the magnitude of the tunneling leakage current, respectively. The ϕ_b is affected according to the concentration of Vo. Six barrier heights (ϕ_b) are fitted to calibrate with measurements for the device that have different Vo concentrations (the measurements can be seen in Fig. 6b, c). Fig. 7 presents the ϕ_b as a function of Vo concentration. It indicates that Vo concentration at the interface reduces effective barrier height (ϕ_b), thus the tunneling current, which is also supported by measurements from other papers [16]. Therefore, the ϕ_b is related to the OR defect strength and its proper fitting is also important for the OR-defective modeling.

V. Fault Modeling and Analysis

In this section, we first define and classify the fault space. Then, the fault analysis based on the circuit simulation using the OR-defective models will be given.

A. Fault Space Definition and Classification

Memory faults can be classified as *Easy-to-Detect (EtD)* and *Hard-to-Detect (HtD)* faults. EtD faults can be *guaranteed* to be sensitized and detected by regular memory operations. HtD faults are those that are *not guaranteed* to be sensitized (e.g., random read) or do not result in any functional errors [5]. These faults can be systematically presented by the Fault Primitive (FP) notation, which is a three-tuple $\langle \mathrm{S/F/R} \rangle$ [21]. Here, S, F, and R denote the sensitizing operation, the faulty state of the cell after performing the operation, and the output if the final operation in S is a read operation, respectively. For example, $\langle 0\mathrm{r}0/\mathrm{U}/1 \rangle$ describes a 0r0 operation is applied on an HRS cell ($\mathrm{S} = 0\mathrm{r}0$), where the cell flips to an incorrect undefined state ($\mathrm{F} = \mathrm{U}$), the read output returns '1' ($\mathrm{R} = 1$) instead of the expected '0'.

B. Fault Analysis

1) Simulation Setup: We adopt Cadence Spectre to establish the simulation by using the Predictive Technology Model (PTM) 130-nm transistor library [22] and the RRAM compact model from [19]. Regular voltage-based SA is applied for reading operations [23]. We perform two experiments to analyze fault results.

TABLE II
Fault modeling results for OR defect.

$N_{\mathrm{disc,min}}[10^{26}\,\mathrm{m}^{-3}]$	R_{RESET}	Fault
0.0025	358.3 kΩ	Fault free
0.0009	1 MΩ	
0.00025	3.7 MΩ	$\langle 1\mathrm{w}0/\mathrm{L}/- \rangle$ HtD
0.0002	4.7 MΩ	
0.0001	7.2 MΩ	

The first experiment is built to validate faults with varying OR defect strengths to analyze the extremely high resistance fault. The defect injection is carried out by replacing the defect-free RRAM model with the model of the defective RRAM device obtained in Section IV. The voltage sweep is applied through the SL from 0 V to 1.8 V back to 0 V for RESET operation to sensitize the fault. The defect strength is governed by the varied $N_{\mathrm{disc,min}}$ (from $0.0025 \cdot 10^{26}\,\mathrm{m}^{-3}$ to $0.0001 \cdot 10^{26}\,\mathrm{m}^{-3}$) after the RESET.

The second experiment is based on the traditional defect models to validate whether they can model the unique OR defect. Traditionally, RRAM defects are modeled using linear resistors [21]. There are only two options for defect modeling: the resistor can either be in parallel or in series with the defect-free device. Hence, we inject resistors both in parallel and in series to validate the sensitized faults. The strength of a resistor defect is swept from 1 Ω to 100 MΩ.

2) Fault Modeling and Results: First, Table II shows the obtained results of the first experiment. We inspect the final resulting resistance (after RESET operation) to derive fault models. It can be seen that HtD faults ($\langle 1\mathrm{w}0/\mathrm{L}/- \rangle$) are sensitized when the $N_{\mathrm{disc,min}}$ decreases. A lower $N_{\mathrm{disc,min}}$ (a larger ratio $N_{\mathrm{disc,max}}/N_{\mathrm{disc,min}}$) gives more room for Vo to be recombined in the disc region, which makes it easier for the device to exhibit undesired RESET failure. Although no faults are sensitized by SET operation with OR defects, we still observe the V_{SET} delay as shown in Fig. 6b, c. That can be explained by the initial resistance state-dependent thermoelectric coupling during the SET process included in the used RRAM model, which reduces the transition delay time for lower initial HRS [19].

Next, we compare the static faults sensitized by conventional linear resistors and DA OR-defective models. Totally 6 static faults are sensitized by linear resistors: $\langle 1\mathrm{w}0/1/- \rangle$, $\langle 1\mathrm{w}0/\mathrm{U}/- \rangle$, $\langle 0\mathrm{w}1/0/- \rangle$, $\langle 0\mathrm{w}1/\mathrm{U}/- \rangle$, $\langle 0\mathrm{r}0/0/1 \rangle$, $\langle 1\mathrm{r}1/1/0 \rangle$. Clearly, neither parallel nor series resistors can sensitize the $\langle 1\mathrm{w}0/\mathrm{L}/- \rangle$ fault, which indicates the need for the OR-defective model. Furthermore, linear resistors sensitize faults that are unrealistic when modeling OR defects; hence, tests for them will lead to unnecessary yield loss.

VI. Test Development for OR defect

As explained in Section V, the targeted fault sensitized by the RESET operation is an HtD fault. Hence, a conventional March test cannot guarantee its detection. Reading this state will result in '0', the same as the normal HRS. To detect those HtD faults, DfT schemes can be applied. For example, we can design different references composed of RRAM devices, so that the SA can identify states between 'L'/'0' instead of

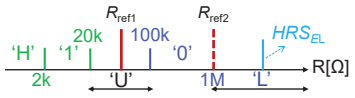
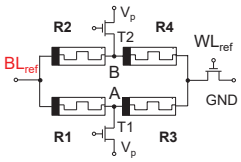


Fig. 8. Resistances for faulty RRAM state.



	R1, R2	R3, R4
Regular	**100kΩ**	**20kΩ**
DfT	**1MΩ**	**1MΩ**

Fig. 9. Modified reference cells.

identifying only the regular '0'/'1'. The shifted reference DfT concept is illustrated in Fig 8. For regular SA, R_{ref1} is typically set to $(\mathrm{HRS}+\mathrm{LRS})/2$ to distinguish '1' and '0'. To detect the 'L' state (HRS_{EL}), another reference (R_{ref2}) needs to be set to the maximum value of the defined '0' range. Besides, due to the intermittent nature of the OR phenomenon, the proposed DfT scheme will only *probabilistically* detect the fault. Hence, repeated 1w0 (to sensitize) and read (to detect) operations are required to enhance the detection probability. If we assume the occurrence possibility of OR is P_{OR}, then the detection probability is: P_{d}=$1-(1-P_{\mathrm{OR}})^{k}$, k indicates the number of times the sequence is applied. In our case of P_{OR}=30 %, k=13 is required to realize 99 % fault coverage.

Based on the concept, we develop an adaptable reference tunable structure that is compatible with normal read operations. Fig. 9 illustrates the two RRAM devices connected in series and parallel with two other RRAM devices connected in series, together with two extra transistors (T1, T2), for providing tunable reference cells. In Fig. 9, R1 to R4 are set to different states for regular (R_{ref1}) or DfT (R_{ref2}) purposes. In the regular case, R1, R2 are set to normal HRS while R3, R4 are set to normal LRS. In the DfT case, all 4 cells need to be set as the upper bound of the HRS region (1 MΩ) to detect 'L'. T1 and T2 are used as switches to control whether voltage pulses (i.e., V_{P}) can be applied at nodes A and B to program the reference cells. For example, when the T1 is conducting, V_{p} can be applied on node A, switching the state of R1.

The DfT scheme is implemented by establishing a Cadence Spectre-based simulation including a 1T-1R cell and SA. First, the defect-free circuit is validated to be correct. Next, we replace the defect-free cell with the OR defective model. After applying the regular 0r0 operation using R_{ref1}, the faulty 'L' is read as an incorrect value '0'. By tuning the reference cell from R_{ref1} to R_{ref2}, the 'L' state can be correctly distinguished from the normal HRS by the readout value.

Other specific DfTs can be used to further reduce the test time. For example, a weak or fast write operation can be performed by the DfT scheme based on low write voltage or short write duration [7]. This will result in an insufficient RESET, which decreases the final RESET resistance of the faulty 'L' device to correct '0' state and be easily detected. The limitation of this scheme is a resulting lower R_{SET} for defect-free devices, which increases energy consumption.

VII. Conclusion

This work presents the power of the DAT approach in identifying and modeling the intermittent (30 % cycles) OR phenomenon in an appropriate manner. As devices scale down, complex and additional manufacturing steps in RRAMs could cause new defect mechanisms that are not investigated completely yet. Therefore, this requires a deeper understanding of emerging defect mechanisms, as well as improved fault modeling and testing methods.

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References

[1] K.-W. Hou *et al.*, "Fault Modeling and Testing of Memristor-Based Spiking Neural Networks," in *ITC*, 2022.

[2] E. I. Vatajelu *et al.*, "Challenges and Solutions in Emerging Memory Testing," *TETC*, vol. 7, no. 3, 2019.

[3] N. Xiao *et al.*, "Resistive Random Access Memory Cells with a Bilayer TiO_2/SiO_x Insulating Stack for Simultaneous Filamentary and Distributed Resistive Switching," *AFM*, vol. 27, no. 33, p. 1 700 384, 2017.

[4] S. Yu *et al.*, "On the Stochastic Nature of Resistive Switching in Metal Oxide RRAM: Physical Modeling, Monte Carlo Simulation, and Experimental Characterization," in *IEDM*, 2011.

[5] M. Fieback *et al.*, "Device-Aware Test: A New Test Approach Towards DPPB Level," in *ITC*, 2019.

[6] T. S. Copetti *et al.*, "Evaluating a New RRAM Manufacturing Test Strategy," in *LATS*, 2023.

[7] N. Z. Haron *et al.*, "DfT Schemes for Resistive Open Defects in RRAMs," in *DATE*, 2012.

[8] S. Kannan *et al.*, "Sneak-Path Testing of Crossbar-Based Nonvolatile Random Access Memories," *TN*, vol. 12, no. 3, pp. 413–426, 2013.

[9] Y.-X. Chen *et al.*, "Fault Modeling and Testing of 1T1R Memristor Memories," in *VTS*, 2015.

[10] L. Wu *et al.*, "Electrical Modeling of STT-MRAM Defects," in *ITC*, 2018.

[11] S. Hamdioui *et al.*, "Device Aware Test for Memory Units," *Patent No. NL 2023751*, 2021.

[12] H. Aziza *et al.*, "STATE: A Test Structure for Rapid and Reliable Prediction of Resistive RAM Endurance," *TDMR*, vol. 22, no. 4, pp. 500–505, 2022.

[13] W. Y. Park *et al.*, "Improvement of Sensing Margin and Reset Switching Fail of RRAM," *SSE*, vol. 156, pp. 87–91, 2019.

[14] C.-W. Zhong *et al.*, "Effect of ITO Electrode with Different Oxygen Contents on the Electrical Characteristics of HfO_x RRAM Devices," *SURF COAT TECH*, vol. 231, pp. 563–566, 2013.

[15] N. Raghavan *et al.*, "Stochastic Variability of Vacancy Filament Configuration in Ultra-Thin Dielectric RRAM and Its Impact on OFF-State Reliability," in *IEDM*, 2013.

[16] J. J. Yang *et al.*, "Memristive Switching Mechanism for Metal/Oxide/Metal Nanodevices," *Nat. Nanotechnol.*, vol. 3, no. 7, pp. 429–433, 2008.

[17] N. Raghavan *et al.*, "Stochastic Failure Model for Endurance Degradation in Vacancy Modulated HfO_2 RRAM Using the Percolation Cell Framework," in *IRPS*, 2014.

[18] Z. Shen *et al.*, "Effect of Annealing Temperature for Ni/AlO_x/Pt RRAM Devices Fabricated with Solution-Based Dielectric," *Micromachines*, vol. 10, no. 7, p. 446, 2019.

[19] F. Cüppers *et al.*, "Exploiting the Switching Dynamics of HfO_2-based ReRAM Devices for Reliable Analog Memristive Behavior," *APL Mater.*, vol. 7, no. 9, p. 091 105, 2019.

[20] Z. Weinberg, "On Tunneling in Metal-Oxide-Silicon Structures," *JAP*, vol. 53, no. 7, pp. 5052–5056, 1982.

[21] S. Hamdioui *et al.*, "An Experimental Analysis of Spot Defects in SRAMs: Realistic Fault Models and Tests," in *ATS*, 2000.

[22] ASU, *Predictive Technology Model (PTM)*, 2012.

[23] W. Zhao *et al.*, "Synchronous Non-Volatile Logic Gate Design Based on Resistive Switching Memories," *T CIRCUITS-I*, vol. 61, no. 2, pp. 443–454, 2014.