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Structured electronic design of high-pass $\Sigma\Delta$ converters and their application to cardiac signal acquisition

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***Abstract*—Achieving an accurate sub-Hz high-pass (HP) cut-off frequency and simultaneously a high accuracy of the transfer function is a challenge in the implementation of analog-to-digital converters for biomedical ExG signals. A structured electronic design approach based on state-space forms is proposed to develop HP$\Sigma\Delta$ modulators targeting high accuracy of the HP cut-off frequency and good linearity. Intermediate transfer functions are mathematically evaluated to compare the proposed HP$\Sigma\Delta$ topologies with respect to dynamic range. Finally, to illustrate the design method, an orthonormal HP$\Sigma\Delta$ modulator is designed to be implemented in 0.18 μm technology which achieves a linearity of 12-bits.**

I. Introduction

To meet the growing demand of the geriatric population, there is a need for light and inexpensive home health-care devices that enable continuous, reliable and longterm ECG monitoring to detect cardiac arrhythmias that manifests themselves aperiodically. With the bandwidth of the ECG signal extending from sub-Hz to 200 Hz [1], a major challenge for an ECG readout system lies in implementing the sub-Hz HP cut-off frequency as this translates into the realization of large time constants on-chip. To realize large time constants in the order of a few seconds, there exist techniques that employ pseudo-resistors [2] or g_m blocks [3]. Although these techniques realize large time constants in an area and power efficient manner, they are heavily limited in both linearity and accuracy. Also, they are not very robust to PVT variations. Hence, when better linearity and accuracy are required, alternative techniques need to be developed.

In this paper, a synthesis procedure for developing HP$\Sigma\Delta$ converters suitable for designing the analog front-end for ECG signal acquisition which incorporates HP filtering is proposed. $\Sigma\Delta$ ADCs take advantage of their noise shaping property to achieve low quantization noise and the use of 1-bit digital-to-analog converter ensures inherent linearity. As opposed to conventional low-pass $\Sigma\Delta$ converters, a signal transfer that accommodates a general filter transfer is considered. Intermediate transfer function analysis evaluates the signal handling capabilities and the noise contributions of each of the integrators and thus helps in the overall ranking of the developed HP$\Sigma\Delta$ topologies.

In Section II, the proposed methodology to develop HP$\Sigma\Delta$ converters is presented. The method is illustrated through two design examples. In order to qualitatively and quantitatively assess the topologies, an intermediate function analysis is presented in Section III. In Section IV, the circuit implementation and simulation results of the developed HP$\Sigma\Delta$ topology are described. Finally, conclusions are given in Section V.

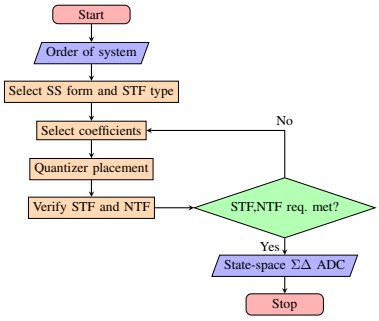

Fig. 1: Flowchart of the state-space based approach for $\Sigma\Delta$ topologies

II. Proposed methodology

Designing a system that incorporates filtering and digitization using an orthogonal design methodology allows us to systematically arrive at different topologies while optimizing the performance metrics relevant to low voltage and low power designs such as dynamic range and sensitivity to coefficient variations. In this procedure, a general signal transfer function (STF) is considered and standard state-space (SS) forms are used to develop the HP$\Sigma\Delta$ ADC topologies. For a given SS form, the coefficients are evaluated for their contributions to the signal and noise transfer requirements. Here, the STF is generalized to include low-pass, high-pass, bandpass or a notch filter. In the targeted application, viz. a cardiac signal readout system, an HP STF is required. The quantizer is placed such that the noise transfer is satisfied. For the sake of clarity and simplicity, a 3rd order system is considered. However, the method can be extended to higher orders as well.

Fig. 1 shows the design procedure that is used to develop the desired HP$\Sigma\Delta$ ADCs. As an example, an **orthonormal** HP$\Sigma\Delta$ ADC is developed that satisfies the signal and noise transfer requirements. Considering a 3rd order system, the requirements of the transfer functions are:

1) Signal transfer function (STF): a HP characteristic with at least 20 dB/dec roll-off wherein the location of the pole(s) can be set independently
2) Noise transfer function (NTF): a HP characteristic with at least 40 dB/dec slope in the signal band

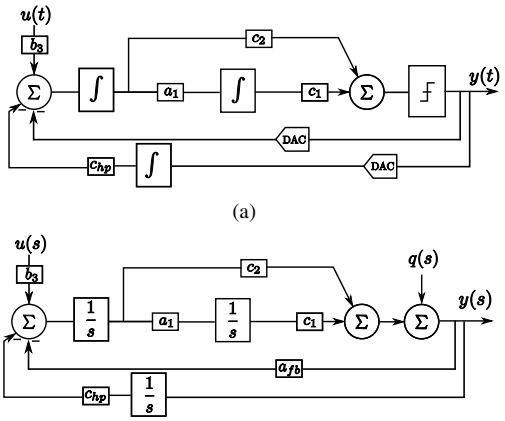

Fig. 2: Orthonormal HPΣΔ ADC topology (a) Block diagram (b) Linear model

TABLE I: Coefficients of the HPΣΔ topologies

Coeff.	Orthonormal HPΣΔ	Coeff.	Observable canonical HPΣΔ
a_1	1	p_1	0.5
b_3	0.5	p_2	0
c_1	1	q_1	1
c_2	2	q_2	2
c_{hp}	0.0005	q_0	0.0005

The state-space form of the orthonormal ladder filter [4] results in the orthonormal HPΣΔ ADC shown in Fig. 2(a). The linear model of the proposed topology is shown in Fig. 2(b). From (1) and (2), it is observed that the STF has one zero at DC which ensures a 20 dB/dec roll-off, and the NTF has three zeros at DC, ensuring proper noise shaping. The STF and the NTF equations can be written as

$$STF = \frac{y(s)}{u(s)} = \frac{sb_3k_2(c_2s + a_1k_1c_1)}{s^3 + k_1a_{fb}c_2s^2 + k_2k_1a_{fb}a_1c_1s + k_1k_2k_3a_1c_1c_{hp}} \quad (1)$$

$$NTF = \frac{y(s)}{q(s)} = \frac{s^3}{s^3 + k_1a_{fb}c_2s^2 + k_2k_1a_{fb}a_1c_1s + k_1k_2k_3a_1c_1c_{hp}} \quad (2)$$

respectively, where k_1, k_2 and k_3 are time constants of the first, second and the HP integrators. For frequencies close to DC, the characteristic equation of (2) can be approximated as

$$s \approx -\frac{c_{hp}k_3}{a_{fb}} \Rightarrow f_{hpf} = \frac{1}{2\pi}\frac{c_{hp}k_3}{a_{fb}}f_s \quad (3)$$

Sampling frequency f_s = 128 kHz, scaling coefficient c_{hp} = 0.0005 and k_3 = a_{fb} = 1 result in an HP cut-off frequency f_{hpf} of 10 Hz, which is selected to observe the slope change clearly. f_{hpf} can be set by appropriately selecting c_{hp}. The STF and NTF of the orthonormal HPΣΔ ADC are plotted in Figs. 3(a) and 3(b), respectively.

As a second example of the design methodology, the linear model of an **observable canonical** HPΣΔ ADC is shown in Fig. 4. The STF and NTF are given by the equations

$$STF = \frac{y(s)}{u(s)} = \frac{s(p_2k_2s + p_1k_1k_2)}{s^3 + k_2q_2s^2 + k_1k_2q_1s + k_1k_2k_3q_0} \quad (4)$$

$$NTF = \frac{y(s)}{q(s)} = \frac{s^3}{s^3 + k_2q_2s^2 + k_1k_2q_1s + k_1k_2k_3q_0} \quad (5)$$

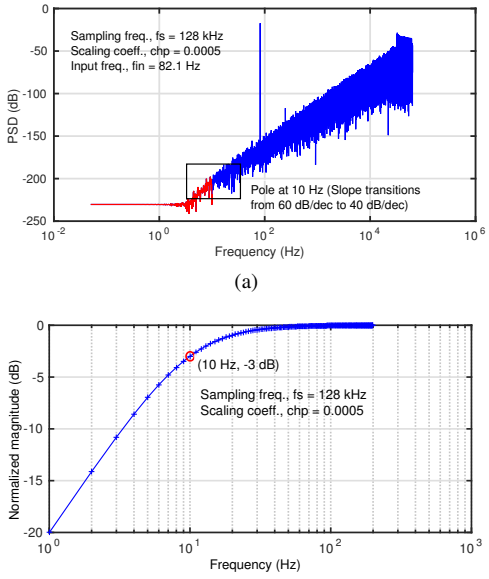

Fig. 3: System level plots of the orthonormal HPΣΔ topology (a) NTF (b) STF

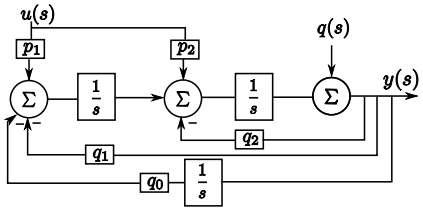

Fig. 4: Linear model of the observable canonical HPΣΔ ADC

From (4) and (5), we see that the transfer function requirements are satisfied. Although the transfer requirements of both the topologies are satisfied, the two structures differ in terms of coefficients. Since also the interconnections between the integrators vary among the topologies, it is expected that this would lead to varying noise performance and dynamic range, which we will examine in the next section.

III. Intermediate Functions

In order to compare the noise performance of the topologies, a set of intermediate functions (IF) from the input of the integrators to the output of the system, **g**(s), and the input of the system to the output of the integrators, **f**(s), are derived, defined as

$$f_i(s) \triangleq \frac{x_i(s)}{u(s)}; \qquad g_i(s) \triangleq \frac{y(s)}{n_i(s)}; \quad (6)$$

where $u(s)$ and $y(s)$ denote the input and the output of the system, and $n_i(s)$ and $x_i(s)$ represent the input thermal noise source and output of the i^{th} integrator, respectively.

f(s) of the orthonormal HPΣΔ modulator consists of a set of functions $\{f_1(s), f_2(s), f_3(s)\}$ given by (7), (8) and (9) as

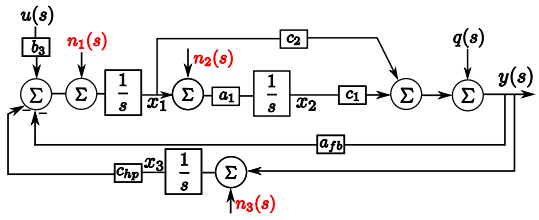

Fig. 5: Thermal noise sources in the orthonormal HPΣΔ ADC

follows:

$$f_1(s) = \frac{k_1 b_3 s^2}{s^3 + k_1 c_2 a_{fb} s^2 + (k_1 a_1 a_{fb} c_1 + k_1 k_3 c_{hp} c_2)s + c_{hp} a_1 c_1 k_1 k_3} \tag{7}$$

$$f_2(s) = \frac{k_1 a_{21} b_3 s}{s^3 + k_1 c_2 a_{fb} s^2 + (k_1 a_1 a_{fb} c_1 + k_1 k_3 c_{hp} c_2)s + k_1 k_3 c_{hp} a_1 c_1} \tag{8}$$

$$f_3(s) = \frac{k_1 k_3 b_3 (c_2 s + a_{21} c_1)}{s^3 + k_1 c_2 a_{fb} s^2 + (k_1 a_1 a_{fb} c_1 + k_1 k_3 c_{hp} c_2)s + k_1 k_3 c_{hp} a_1 c_1} \tag{9}$$

$\mathbf{g}(s)$ of the orthonormal HPΣΔ modulator consists of a set of functions $\{g_1(s), g_2(s), g_3(s)\}$ given by (10), (11) and (12) as follows:

$$g_1(s) = \frac{k_1 (c_2 s + a_1 c_1) s}{s^3 + k_1 a_{fb} c_2 s^2 + (k_1 a_{fb} a_1 c_1 + k_1 k_3 c_{hp} c_2)s + k_1 k_3 c_{hp} a_1 c_1} \tag{10}$$

$$g_2(s) = \frac{c_1 a_1 s^2}{s^3 + k_1 a_{fb} c_2 s^2 + (k_1 a_{fb} a_1 c_1 + k_1 k_3 c_{hp} c_2)s + k_1 k_3 c_{hp} a_1 c_1} \tag{11}$$

$$g_3(s) = \frac{k_1 k_3 c_{hp} (c_2 s + a_1 c_1)}{s^3 + k_1 a_{fb} c_2 s^2 + (k_1 a_{fb} a_1 c_1 + k_1 k_3 c_{hp} c_2)s + k_1 k_3 c_{hp} a_1 c_1} \tag{12}$$

From (10), (11) and (12), the noise from the first and second

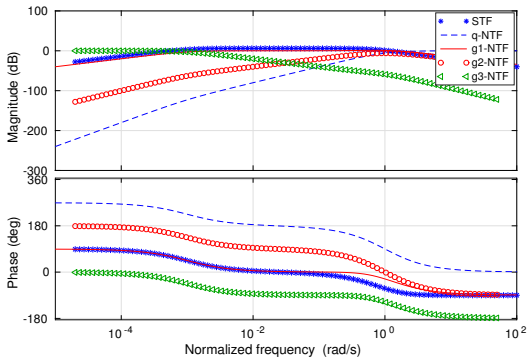

Fig. 6: Frequency response of the IF-**g**(s) thermal noise transfer functions of the orthonormal HPΣΔ topology

integrator (n_1 and n_2) is first and second order HP shaped, respectively, whereas the noise from HP integrator (n_3) is low-pass filtered, which is also demonstrated in Fig. 6. As can be seen, the input signal has a slope of 20 dB/dec; the quantization noise initially begins with a slope of 60 dB/dec, but transitions to 40 dB/dec after encountering the pole responsible for the HP cut-off frequency. A similar set of IF's for the observable HPΣΔ is derived and calculated, but is not shown here due to space constraints. The next step in the IF analysis is to quantitatively evaluate the performance of the ΣΔ modulators, which necessitates a mathematical norm that measures the

TABLE II: L_2-norm calculations of orthonormal HPΣΔ topology

Int.	Before scaling $\|f_i\|_2$	Before scaling $\|g_i\|_2$	Factor α_i	After scaling $\|f_i\|_2$	After scaling $\|g_i\|_2$
Int 1	2.500312e-01	1.118062e+00	3.9995	1	2.795504e-01
Int 2	2.499063e-01	5.000624e-01	4.0015	1	1.249688e-01
Int HP	1.581336e+01	1.581336e-02	0.0632	1	2.500625e-01

magnitudes of the signal levels at the output. Assuming a white input signal, the root-mean-square value of the output power spectrum is given by the L_2-norm. For a signal $v(t)$, the L_2-norm is defined as

$$\|v\|_2 = \left(\int_0^\infty v(t)^2 dt \right)^{\frac{1}{2}} \tag{13}$$

The dynamic range, given by the ratio of the maximum signal handling capability and the minimum level as determined by the internally generated noise can be optimized through scaling of the integrators. Integrator scaling is the process of readjusting the internal gain coefficients in order to adjust the internal signal swing to a range appropriate to the supply voltage such that the overall transfer function from the input to the output remains unchanged. The L_2-norms of the set of IF's **f**(s) and **g**(s) are calculated and are tabulated in Table II. A scaling factor, α_i, is calculated for each integrator, given by

$$\alpha_i = \frac{M}{\|f_i\|_2} \tag{14}$$

where M is the maximum acceptable signal magnitude at the integrator outputs. After **f**(s) has been scaled, **g**(s) is scaled by the inverse factor $(\frac{1}{\alpha_i})$ as given in Table II. The total noise power of the integrators, given by $\sum_i \|g(j\omega)\|_2^2$, can be evaluated and used as a figure of merit [5] for comparing the noise performance of the HPΣΔ topologies. The total noise power for a 3rd order system given by $\sum_{i=1}^{3} \|g_i(j\omega)\|_2^2$ for the orthonormal HPΣΔ is 0.15629688 which is slightly smaller than that of the observable HPΣΔ which is 0.15632816. Therefore, the orthonormal HPΣΔ is a preferred choice for circuit implementation. The noise performance of both HPΣΔ topologies can further be improved by balancing the integrator noise contributions better, i.e., making the individual g_i equal. From system simulations, it follows that the difference between the noise performance of these types of filters becomes more pronounced for higher orders, in favor of the orthonormal HPΣΔ modulator topology.

IV. Circuit Implementation and Results

A simplified top level schematic of the proposed orthonormal HPΣΔ modulator is illustrated in Fig. 7. To achieve high linearity, opamp-RC integrators are chosen. In order to drive relatively large capacitances, a two-stage amplifier topology is used. A multiple - input dynamic comparator is used to realize the summer and the quantizer. A very large time-constant, parasitic-insensitive and area-efficient switched-capacitor integrator as shown in Fig. 8 [6] is used to realize the HP integrator in the feedback loop. The input voltage is attenuated and then integrated onto the large capacitor C_2. The unity gain frequency, f_u of the integrator is given by [6]

$$f_u = \frac{1}{2\pi} \frac{1}{\left[1 + \frac{C_3}{C_2}\right]} \frac{C_1}{C_2} \frac{C_3}{C_2} f_{clk} \tag{15}$$

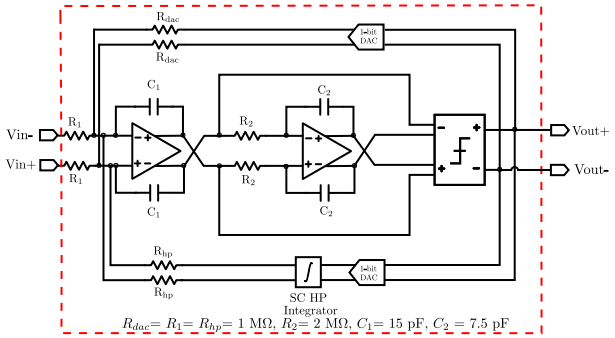

Fig. 7: Top level circuit block diagram of the CT orthonormal HPΣΔ modulator

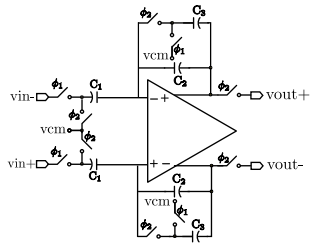

Fig. 8: SC Nagaraj integrator (HP) [6]

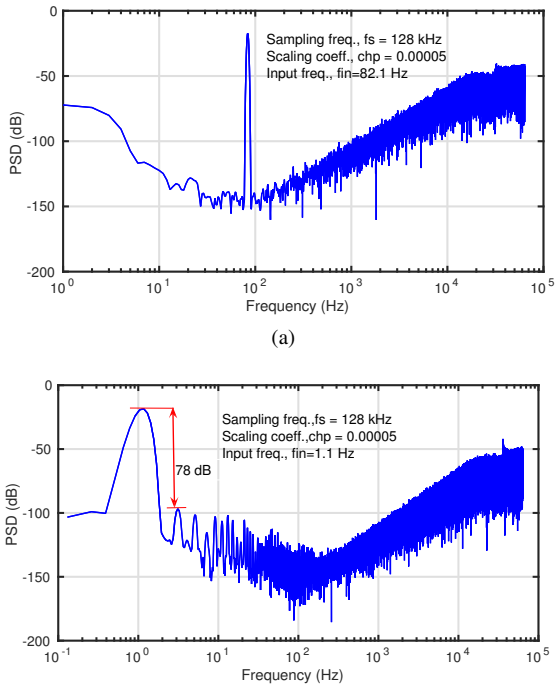

Fig. 9: Orthonormal HP ΣΔ ADC circuit simulations (a) Output spectrum for f_{in} = 82.1 Hz (b) Output spectrum for f_{in} = 1.1 Hz

where f_{clk} is the clock frequency and is equal to the sampling frequency of the ΣΔ modulator. To avoid long simulation times, f_{hpf} is set at 1 Hz and the circuit is tested for linearity at the same frequency. Lower f_{hpf} can be realized by appropriately selecting the values of capacitances and the clock frequency, at the cost of larger area and power. To obtain a cut-off frequency of 1 Hz, C_1 = 0.5 pF, C_2 = 45 pF and C_3 = 0.2 pF are chosen to realize a scaling coefficient of $5{\cdot}10^{-5}$ that follows from (3) and (15). In the designed modulator, the HP cut-off frequency is implemented using ratios of capacitors which are more accurate and robust to PVT variations as compared to pseudo-resistors or g_m based techniques. Designed and simulated in AMS 0.18 μm CMOS IC technology, the orthonormal HPΣΔ ADC achieves 12-bit linearity. The output spectrum of the orthonormal HPΣΔ ADC for input frequencies of 82.1 Hz and 1.1 Hz are plotted in Fig. 9(a) and 9(b), respectively. Table III summarizes the performance of the designed CT HPΣΔ modulator.

V. Conclusion

In this paper, a structured methodology is proposed to develop HPΣΔ ADC topologies. By the state-space approach, ΣΔ converters with arbitrary signal and quantization noise transfer functions can be synthesized. State-space techniques allow dynamic range optimization of the ΣΔ converters with respect to signal swing and noise through state and noise scaling, respectively. This also minimizes the sensitivity of the topology to component variations [7]. From the IF analysis, it is seen that the noise and harmonics from the HP integrator are low-pass filtered. Also, from the L_2-norm calculations, it is observed that the orthonormal HPΣΔ gives slightly better SQNR than the observable HPΣΔ. Finally, circuit simulations of the circuit design in AMS 0.18 μm CMOS IC technology verify the findings and match the system level results.

TABLE III: Performance of the CMOS orthonormal HPΣΔ modulator

Technology	0.18 μm AMS
Supply voltage	1.8 V
Sampling frequency	128 kHz
Signal Bandwidth	1 - 200 Hz
SNDR	76 dB
ENOB	12 - bit
Total capacitance	148.4 pF
Total power consumption	146μW

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