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DOI
10.1016/j.solmat.2019.01.039

Publication date
2019

Document Version
Final published version

Published in
Solar Energy Materials and Solar Cells

Solar Energy Materials and Solar Cells 194 (2019) 28–35

Contents lists available at ScienceDirect

Solar Energy Materials and Solar Cells

journal homepage: www.elsevier.com/locate/solmat

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ARTICLE INFO

Keywords:
Poly-silicon passivating contacts
Amorphous silicon
Ion-implantation
Silicon solar cells

ABSTRACT

In this work we develop a rear emitter silicon solar cell integrating carrier-selective passivating contacts (CSPCs) with different thermal budget in the same device. The solar cell consists of a B-doped poly-Si/SiO_x hole collector and an i/n hydrogenated amorphous silicon (a-Si:H) stack acting as electron collector placed on the planar rear and textured front side, respectively. We investigate the passivation properties of both CSPCs on symmetric structures by optimizing the interdependency among annealing temperature, time and environment. The optimized B-doped poly-Si/SiO_x reaches a saturation current density of ~10 fA/cm^2 on n-type wafers and an implied open circuit voltage (iV_{OC}) of 716 mV. Furthermore, the i/n a-Si:H stack shows an effective carrier lifetime above 4 ms and iV_{OC} of ~705 mV for cell-relevant layers thickness. After a post-deposition annealing in H_2, lifetime is above 10 ms and iV_{OC} = 708 mV. Finally, we optimize the optoelectronic properties of indium-based transparent conductive oxide (Indium Tin Oxide ITO and hydrogenated indium oxide IO:H) to reduce parasitic absorption with a gain in short circuit current density of 0.23 mA/cm^2. In conclusion, the optimized layer stacks are implemented at device level obtaining a device with V_{OC} = 704 mV, fill factor of 73.8%, a short circuit current of 39.7 mA/cm^2 and 21.0% aperture-area conversion efficiency.

1. Introduction

In homojunction crystalline silicon (c-Si) solar cells, the high surface recombination velocity at the Si/metal interface prevents devices from achieving high conversion efficiencies (η) owing to consistent open-circuit voltage (V_{OC}) losses [1]. A possible solution to reduce contact recombination is to restrict metal contact area at the rear side, employing the so-called passivated emitter rear contact (PERC) approach [2]. Since metal contact fraction is strongly limited, this leads to higher series resistance. The optimization requires a trade-off between recombination losses (detectable in V_{OC}) and fill factor (FF) [3,4]. Moreover, fabrication process requires an additional patterning step that increases the manufacturing costs. The use of carrier-selective passivating contacts (CSPCs) has been proposed to cope with V_{OC} limitation [5]. It consists in inserting a material that can concurrently act as passivation and contact layer to separate the metal contact from c-Si absorber to overcome the V_{OC} losses. In silicon heterojunction (SHJ) solar cells [6], the growth of intrinsic and doped hydrogenated amorphous silicon (a-Si:H) stacks on both c-Si wafer surfaces enables extremely high V_{OCs} up to 750 mV [7]. With this device concept, Kaneka has reported conversion efficiency (η) above 25% for a front and back-contacted (FBC) scheme [8] and recently η = 26.7% in interdigitated back-contacted (IBC) devices [9]. Besides the advantages of using a-Si:H passivation contacts [10–12] and their limited thickness, intrinsic and doped a-Si:H layers placed on the front side of a SHJ cell suffer from high parasitic absorption losses due to high defect density within the material and high absorption coefficient owing to the quasi-direct bandgap of a-Si:H [13]. Therefore, part of the photo generated carriers is parasitically absorbed without contributing to the carrier collection [14]. Additional source of current loss comes from the use of transparent conductive oxide (TCO) layer, such as indium tin oxide (In_2O_3:Sn, ITO), to solve lateral conductivity issues of a-Si:H. To improve the near-infrared transparency, hydrogenated indium oxide (IO:H) has been developed with much reduced optical parasitic losses [15]. The higher contact resistance at the IO:H/metal interface is mitigated by inserting a thin ITO buffer layer as suggested by Barraud et al. [16]. In total, more than 2 mA/cm^2 in photocurrent density is estimated to be lost in the front layer stack of a typical SHJ solar cell. Furthermore, SHJ fabrication process is temperature-limited. In fact, passivation properties of a-Si:H layers strongly degrade for T > 250 °C [13], therefore dedicated back-end processes, such as TCO depositions and metallization need to be carefully developed.

A very promising contact scheme, originally proposed by Yablonovitch et al. [17], consists of an ultra-thin silicon oxide layer

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https://doi.org/10.1016/j.solmat.2019.01.039
Received 31 August 2018; Received in revised form 17 January 2019; Accepted 29 January 2019
Available online 08 February 2019

(SiO_2 < 2 nm) [18] coated with doped poly-Si layer grown by either low pressure- or plasma-enhanced chemical vapour deposition (LP/PE-CVD) methods [19,20]. This passivation scheme involves fabrication processes in the range of 900 °C; therefore, it is compatible with standard solar cell manufacturing. The presence of an ultra-thin SiO_2 layer reduces the defect density at c-Si surface providing simultaneously surface passivation, and a tunnel barrier that allows only majority carriers to be collected at poly-Si contact [21,22]. Possible mechanisms of transport from crystalline silicon into poly-Si across SiO_2 are based on tunnelling [23,24], mediated by pin-holes [25] or both. After annealing and hydrogenation steps, recombination current densities (J_0) below 1 fA/cm^2 and ~10 fA/cm^2 for n-type and p-type poly-Si/SiO_2 junctions, respectively [26]. A conversion efficiency of 25.8% has been recently achieved applying this selective layer at the backside of the solar cell, while keeping a classic homojunction contact at the front side [27]. A wide range of device architectures has been exploited, such as IBC [28–30], semi-industrial bi-facial Passivated Emitter Rear Polysilicon (PERPoly) [31] and FBC solar cells. Furthermore, poly-Si can be alloyed with oxygen or carbon during the deposition process to enhance material stability and render these contacting materials more transparent owing to a larger band gap. They have been applied in FBC devices either in a selective front surface field (FSF) [32] or at the planar back side of FBC devices in combination with a-Si:H-based CSPCs coating the textured front side [33], a so-called *hybrid* device. The simplest architecture combines SiO_2/poly-Si on both sides of the wafer in a front/rear contacted solar cell as done by Feldmann et. al. [34] and Luxembourg et. al. [35]. Nonetheless, high absorption coefficient of the relatively thick (~ 20 nm) front poly-Si limits short-circuit current density (J_{SC}) of the solar cells. Therefore, it is necessary to mitigate these parasitic absorption losses while still employing excellent passivation quality and keeping the manufacturing process as simple as possible. In this work, we present an optimization study of CSPCs with different thermal budgets for solar cells with a rear emitter configuration consisting in poly-Si/SiO_2 hole-selective contact and an i/n a-Si:H stack acting as electron-selective contact at the front side. The hole collector has been located at the rear side to maximize collection of holes and to ensure more flexibility with the front structure [32,36]. We investigate the passivation properties of both CSPCs on symmetric structures by optimizing the interdependency among annealing temperature, time and environment. Post-deposition annealing and layers stability are investigated to further improve the passivation quality at the c-Si/a-Si interface. Furthermore, we present a comparison between ITO and IO:H/ITO bilayer to improve the opto-electrical performance on the illuminated side of the device. Finally, the optimized layers are combined and embedded in silicon solar cells with aperture-area efficiency up to 21%.

2. Experimental details

For preparing symmetric samples and solar cells we used 4 in. n-type float zone (FZ) silicon wafers (c-Si) with polished < 100 > oriented surfaces, a resistivity of 2.5 Ω·cm and initial thickness of 280 μm. Before processing, the c-Si substrates were cleaned in a nitric acid (99% HNO_3) bath for 10 min at 20 °C, followed by a dip in 69.5% HNO_3 at 110 °C to remove, respectively, organic residuals and metallic contaminations. Some samples were chemically textured in a solution containing TMAH, AlkaText® surfactant and H_2O to obtain random pyramids on both sides of the wafer and < 111 > oriented facets. Afterwards, they were cleaned with nitric acid oxidation cycle (NAOC) procedure [10]. To obtain 1-side-textured substrates we used 100-nm thick SiN_x layer to protect the polished side during the etching. Prior Si layer deposition, the wafers were dipped in 0.55% HF for 4 min and then rinsed in DI water for 5 min to remove the thin native oxide layer. Three dedicated symmetric samples for carrier lifetime investigation were fabricated as depicted in Fig. 1.

Samples (a) consist of an i/n a-Si:H (4.5 / 6 nm) stack deposited on both sides by plasma enhanced chemical vapour deposition (PECVD). A gas mixture of SiH_4 diluted in H_2 and PH_3 gas was used to obtain n-doped films. Some of these test samples were completed with 75-nm thick TCO layers on both sides (ITO or IO:H/ITO) deposited by RF sputtering with Ar as carrier gas during deposition (sample (b) in Fig. 1). The ITO was sputtered at 110 °C and it consisted of a thin buffer layer deposited at low power (20 W) and of a bulk layer deposited at high power (200 W). The aim of this approach is to protect the a-Si:H layer stack by potential sputter damage [37]. The IO:H film was instead deposited at room temperature in amorphous phase. A thin buffer layer is deposited also at low power (20 W) to minimize sputtering damage. Afterwards, samples (a) and (b) were annealed to further improve passivation [38] and to recover from sputtering-induced damage in air atmosphere or in 200 sccm H_2 flow at 180 °C for 30 min. In the case of IO:H sample, the annealing was performed also to crystallize the layer [15]. To fabricate samples (c), a wet-chemical SiO_2 layer is grown on the c-Si surface according to the NAOS procedure described in [39] with a nominal thickness of 1.5 nm. Subsequently, a 250-nm thick a-Si layer is deposited via LPCVD at 580 °C with SiH_4 flow of 45 sccm and pressure of 150 mTorr. The samples (c) were then p^+-doped via ex-situ B-implantation by a Varian EHP500 implanter (BF_3 source, dose of $5{\cdot}10^{15}$ ions/cm^2 and energy of 5 keV). Afterwards, these samples were annealed at 950 °C for 5 min to crystallize the a-Si film and simultaneously activate and diffuse the dopants atoms within poly-Si layer. Finally, annealing in forming gas (FG, 10% H_2 in N_2) at 400 °C for 2 h was performed. Quasi-steady-state photoconductance (QSSPC) lifetime measurements [40] were performed using a Sinton Instruments WCT-120 on the symmetric test samples after each abovementioned fabrication steps. Effective lifetime (τ_{eff}), implied open-circuit voltage (iV_{OC}) and J_0 were extracted from the measured curves. Furthermore, B-implanted samples (In Fig. 1(c)) were characterized via electro-capacitance voltage (ECV) to measure active doping concentration profile in the structure. ITO and IO:H/ITO stack were deposited on glass substrates with a nominal thickness of 129 nm and 117 nm / 12 nm, respectively (Fig. 1(d) and (e)) to reproduce the typical, single-layer anti-reflection coating, 75-nm thick layer on textured Si, considering area factor [41]. The optical characterization was carried out using a Lambda Parker spectrophotometer and measuring reflectance (R) and transmittance (T). Carrier concentration and mobility were measured by an Ecopia 5500 Hall setup. Solar cells were fabricated combining the layer stacks described above in the proposed configuration. Fig. 2 summarizes the fabrication steps followed in this work to obtain the final device. Firstly, the SiO_2/p-type poly-Si stack, (high thermal budget) is deposited on the both sides of the c-Si wafer. Then, the backside of the wafer is covered with SiN_x to perform front-side random texturing that results in etching of the bare LPCVD intrinsic amorphous silicon.

The front side was processed by depositing the i/n a-Si:H stack on the textured c-Si surface (Fig. 2(b)). A post-deposition annealing at 190 °C was carried out to further improve passivation quality [6] and the TCO layer was sputtered with a thickness of 75 nm to minimize reflection losses (Fig. 2(c)). The last step is the metallization (Fig. 2(d)) with a rear metal contact consisting of a stack of Ag / Cr / Al (200 nm / 30 nm / 2000 nm) thermally evaporated though a metal mask to define the cell area. The front side contact of some devices was completed with a 2-μm thick full-area e-beam evaporated Al layer afterwards patterned in grid by photolithographic process and lift-off. For some other cells, the front grid was deposited via Ti-Cu plated contacts. The process consists of several steps, similar to the method reported in [42]. A 300 nm-thick Ti layer was e-beam evaporated on the full area and structured by photolithography to obtain a grid pattern and act as seed-layer for the Cu electro-plating. After copper electro-plating (1.4 A direct current for 1500 s), we performed photoresist removal and Ti seed layer etching in H_2O/NH_4O_4. To assess the quality of the fabrication process, lifetime measurements were carried out after each fabrication step. The solar cells were characterized using a class AAA Wacom WXS-

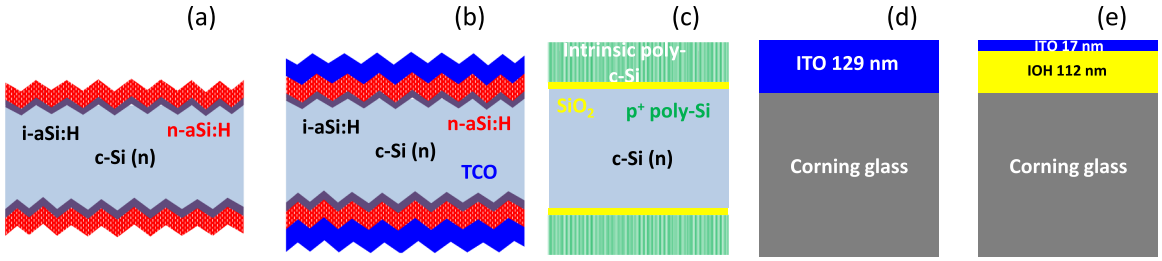

Fig. 1. Cross-sectional sketch of symmetric lifetime samples: i/n a-Si:H (3.5 or 4.5/6 nm) stack without (a) and with (b) with 75-nm thick ITO; (c) p^+-poly-Si/SiO_2 (250 nm / 1.5 nm); (d) 129-nm thick single layer ITO on corning glass; (e) IO:H/ITO (112 nm / 17 nm) stack on corning glass.

156S solar simulator to extract cells' external parameters: V_{OC}, fill-factor (FF), short-circuit current density (J_{SC}) and efficiency (η). Precisely-cut metallic masks were used to properly illuminate the device. Sinton SunsV_{OC} setup allowed to measure pseudo parameters, such as pseudo-FF (p-FF), which excludes the series resistance contribution.

3. Results and discussion

3.1. Carrier-selective contacts passivation quality tests

Low-thermal budget electron selective contact based on a-Si:H CSPC has been characterized from different perspectives. Fig. 3(a-d) summarize the passivation properties of the i/n a-Si:H stack on symmetric structures fabricated on double sided textured wafers. Fig. 3(a) shows the effect of the i-layer thickness on the effective lifetime and implied open circuit voltage. In the as-deposited condition, the two FSF stacks exhibited a τ_{eff} of ~2 ms and ~4 ms for the 3.5 nm and 4.5 nm, respectively. There is a clear i-layer thickness dependence on the passivation quality that is enhanced by a post-deposition annealing in H_2 environment at 190 °C for 30 min. Lifetime increases from ~ 2 ms to ~5 ms in the case of 3.5 nm / 6-nm i/n a-Si:H and from ~ 4 ms to ~ 12 ms in case of 4.5 nm / 6 nm i/n a-Si:H stack. Looking at the iV_{OC} in the same Fig. 3(a), we measure an increase from 695 mV to 705 mV and from 704 mV to 708 mV for 3.5 nm and 4.5 nm i-layer, respectively. Post-deposition annealing further improves chemical passivation of c-Si/a-Si interface [37,43]. For the sample with 3.5 / 6-nm thick i/n a-Si:H we further investigated the post-deposition annealing conditions as time and temperatures (150 °C, 190 °C and 230 °C). The outcomes are reported in Fig. 3(b).

The lowest temperature of 150 °C has only a limited effect on passivation reaching a saturation at ~3.5 ms after 20 min treatment. Low annealing temperature (T = 150 °C) has a weak effect on passivation because it does not change defect density at the interface [44]. Increasing the annealing temperature, the passivation quality improves with the highest τ_{eff} ~ 6 ms obtained at T of 230 °C for 10 min. Similar results have been achieved in [45], for even higher annealing temperature. For longer treatment time the passivation performances progressively degraded to 4 ms after 50 min. For the intermediate temperature of 190 °C, τ_{eff} increases with the treatment time in the first 30 min; above this threshold the measured lifetime stays constant at 5.5 ms. Furthermore, we investigated the stability of the annealed samples at 190 °C for 30 min and 230 °C for 20 min after exposing them to air for 48 h as depicted in Fig. 3(c). Both samples have a comparable initial and post-deposition annealing lifetime, but the degradation effect is different. The sample treated at lower temperature 190 °C has a lifetime twice greater than the one annealed at 230 °C with corresponding loss in τ_{eff} by 60% after 48 h. In [46,47], slower degradation is observed. The mechanism for this phenomenon is not entirely understood. A possible explanation could be a different re-arrangement of hydrogen atoms into a-Si structure respect to the annealing temperature [48]. Finally, we investigated the effect of the annealing environment on passivation quality. The annealing in air is compared to the H_2 atmosphere in Fig. 3(d). As found in [49], we expect that the H_2 gas improves the surface passivation quality by providing additional H^+ atoms that can diffuse from the ambient to the i-layer saturating dangling bonds at the (i) a-Si / c-Si interface [50]. The annealing in air instead restructures Si-H bonds rupture at interface a-Si/c-Si [38]. The results confirm the expectations with an increase in lifetime from ~3.5 ms up to ~ 5.5 ms and iV_{OC} improvement from 695 mV to 705 mV. Since the TCO layer is implemented only on the front side of the investigated device (see cell sketch in Fig. 2), we monitor the effective carrier lifetime of textured wafer passivated by 4.5-nm /6-nm thick i/n a-Si:H stack covered on both sides with IO:H/ITO bilayer after the sputtering deposition. This is done to identify eventual sputtering damages. As Table 1 reports, when TCO is deposited on a-Si:H, the effective lifetime decreases from 4.1 ms in the case of a-Si:H passivation to 3.8 ms. After annealing at 180 °C for 30 min, lifetime increases up to 4.8 ms, confirming that sputtering damage has been completely recovered and more H^+ atoms diffused to the c-Si/a-Si interface, thus improving passivation. This result confirms that 180 °C for 30 min is the optimal annealing recipe to recover from induced damage due to ion bombardment during sputtering process [51]. Nonetheless, during the low-thermal budget fabrication of the this solar cell, annealing at 190 °C for 30 min is performed straight after a-Si:H deposition. Then, a second annealing to recover from TCO damage at 180 °C for 30 min is performed. This action does not affect passivation properties since a

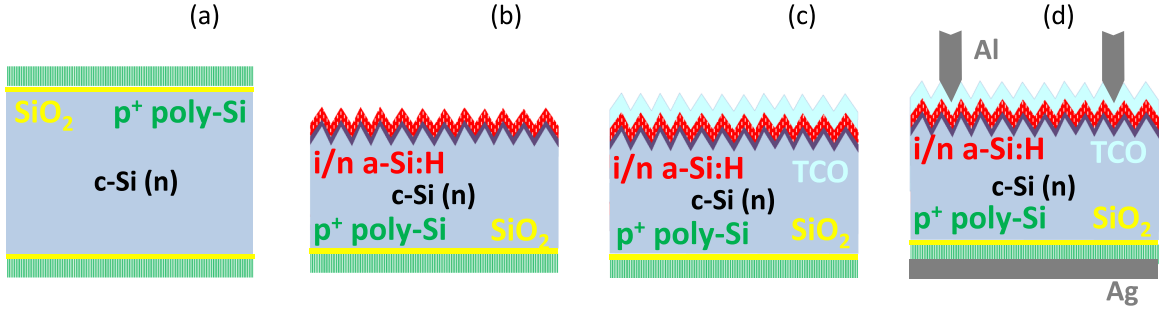

Fig. 2. Main processing steps of our solar cells: (a) Double side polished wafer coated by SiO_2 / p-type poly-Si; (b) front texturing and i/n a-Si:H deposition; (c) front TCO deposition; (d) finished cell with front/rear metallization.

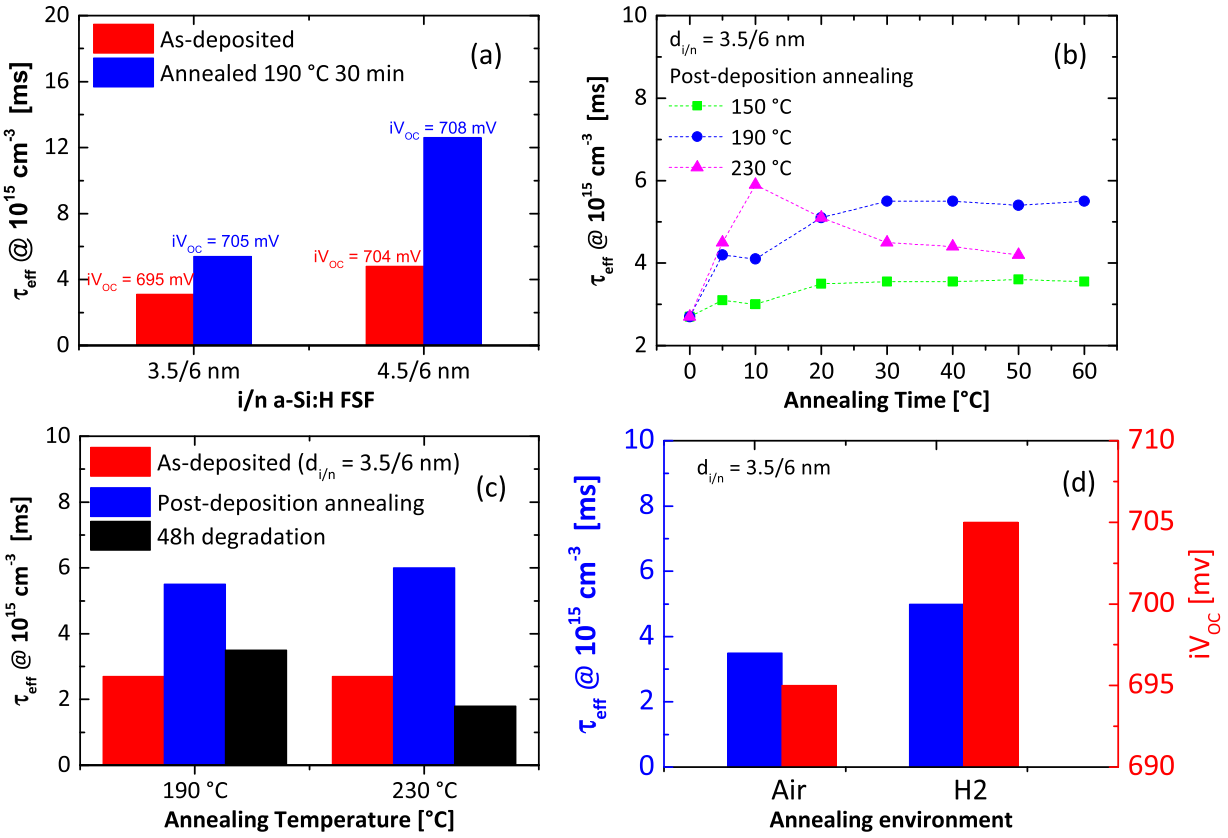

Fig. 3. (a) Passivation quality of double sided textured wafer passivated with 3.5 nm / 6 nm or 4.5 nm / 6 nm i/n a-Si:H stack. (b) Effective lifetime at minority carrier density of 10^{15} cm^{-3} versus post-deposition annealing time in air at different temperatures for a double sided textured wafer passivated by 3.5 nm / 6 nm i/n a-Si:H. (c) Degradation of lifetime against two different post-deposition annealing temperatures for a double sided textured wafer passivated by 3.5 nm/6 nm i/n a-Si:H. (d) Lifetime and iV_{OC} versus two different annealing environments for a double sided textured wafer passivated by 3.5 nm /6 nm i/n a-Si:H.

Table 1
Passivation quality of double sided textured wafer passivated by 4.5 nm /6 nm i/n a-Si:H stack and covered by sputtered 65 nm / 10 nm IO:H/ITO.

	τ_{eff} @ 10^{15} cm^{-3} [ms]	J_0 [fA/cm^2]
i/n a-Si:H passivation	4.1	12
IO:H/ITO sputtering	3.8	15
IO:H/ITO annealed	4.8	8

prolonged annealing at similar temperature as 190 °C leads to a saturation of carrier lifetime as shown in Fig. 3(b). Another reason for which lifetime is weakly affected by IO:H / ITO sputtering is that, as mentioned in the experimental details section, deposition power is very low (20 W) for the first few nanometres of deposition.

High thermal budget CSPC SiO_2 / p-type poly-Si has been also characterized in a symmetric test sample as shown in Fig. 1(c). Fig. 4(a) describes effective lifetime and J_0 after dopant activation and after hydrogenation step. After annealing, for dopant diffusion and activation, τ_{eff} is ~4 ms and J_0 is around 20 fA/cm^2. In this case, iV_{OC} is 704 mV. By applying FG annealing at 400 °C for 2 h the J_0 decreased to ~10 fA/cm^2, indicating that the hydrogenation improves the chemical passivation by driving H^+ ions to the SiO_2/c-Si interface [52]. In this respect, effective lifetime increased to ~5 ms and iV_{OC} reached 716 mV.

Active doping distribution in the structure was measured before FG annealing, as rep orted in Fig. 4(b). It is worth to note that a boron doping concentration of 10^{20} atoms/cm^{-3} is confined into the poly-Si layer surface with a progressive decreasing tail into c-Si bulk down to 10^{16} atoms/cm^{-3} at a depth of ~ 300 nm. This doping difference between poly-Si and c-Si is responsible for field-effect passivation because it induces a strong electrical field across the junction that attracts only holes in this case while repelling electrons. Since the hydrogenation treatment is performed at low temperature (400 °C), the doping distribution is given by the annealing step at 950 °C is not expected to change.

3.2. Transparent conductive oxide material optimization

In this section, we report on optical and electrical quality of 129-nm thick sputtered ITO and IO:H/ITO deposited on glass substrates. It is important to note that 129-nm thick TCO layer is obtained on flat glass using the same recipe to achieve 75 nm-thick on textured silicon. Fig. 5 shows the difference in absorptance between two TCOs developed in this work. The IO:H film absorbs less in ultra-violet range than ITO as already reported in literature [15]. The difference in transparency, at short wavelength, is ascribed to different bandgap of these two materials [53–55]. In the long wavelength range, we observe a comparable behaviour in terms of absorption between ITO and IO:H/ITO stack. If measured absorption is integrated with AM1.5 global spectrum [56], it can be translated directly into a gain in photo-generated current of 0.23 mA/cm^2 when IO:H/ITO stack is employed. This result demonstrates how different is the absorption in 129-nm thick TCOs. By employing 75 nm-thick TCO on textured Si, absolute absorption will be lower but the relative difference would be similar.

Fig. 6 reports carrier density and mobility of ITO and IO:H/ITO stack in as-deposited condition and after annealing at 180 °C for 30 min. For the case of ITO, carrier density in as-deposited condition is $1.2{\cdot}10^{20}$ cm^{-3}. After annealing, it increases to ~$2{\cdot}10^{20}$ cm^{-3}. Instead mobility shows the opposite trend, it decreases from ~30 to ~20 cm^2/Vs after post-sputtering annealing. Bilayer IO:H/ITO stack has instead a carrier density in as-deposited condition of $2.4{\cdot}10^{20}$ cm^{-3} and it halves when

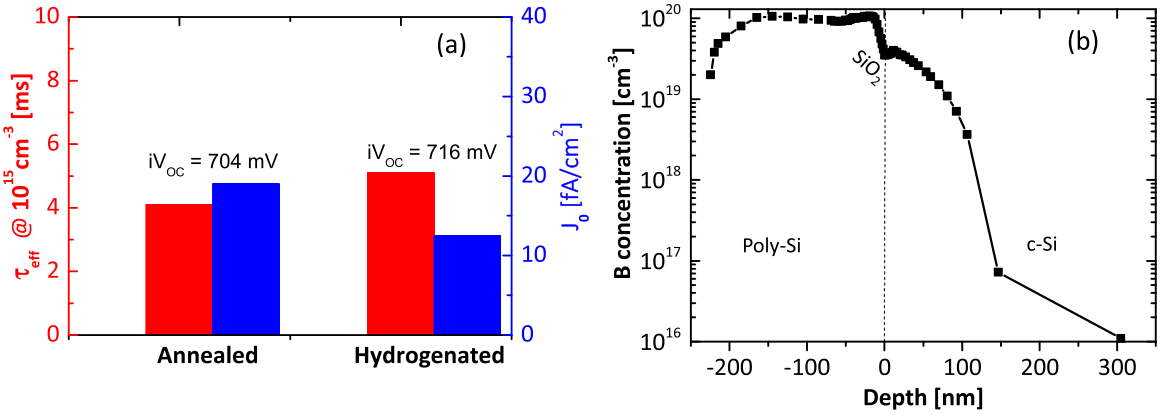

Fig. 4. (a) Effective lifetime (at injection level of 10^{15} cm^{-3}) and extracted J_0 measured on B-doped poly-Si symmetric sample in different conditions as specified. The annealing is performed at 950 °C for 5 min and hydrogenation is performed in FG at 400 °C for 2 h, (b) ECV doping profile measured on the same B-doped poly-Si symmetric sample as shown in the inset in (a) before the annealing in FG.

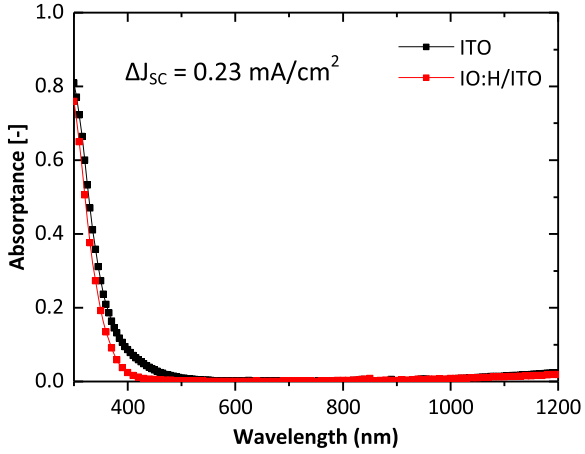

Fig. 5. Absorptance (1-R-T) curves of 129 nm-thick ITO and 117 nm / 12 nm-thick IO:H/ITO layer stack deposited on glass substrates (sketch in Fig. 1(d) and (e)).

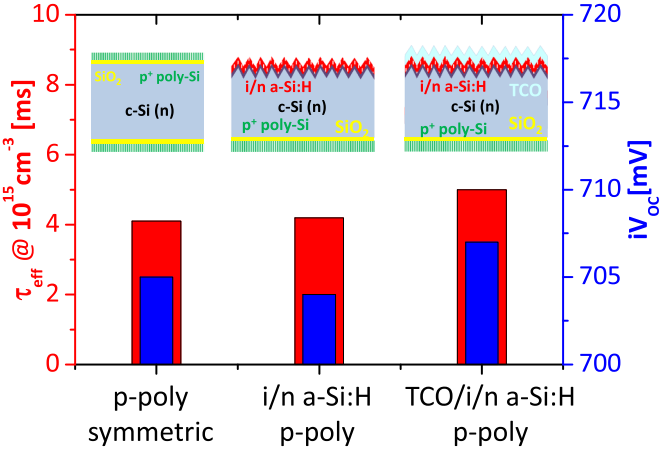

Fig. 7. Effective lifetime and iV_{OC} measurement after each step of solar cell fabrication. In the inset, each fabrication step prior metallization is depicted.

annealing is performed. Mobility shows again the opposite trend, increasing from 60 cm^2/Vs in as-deposited state to up to 120 cm^2/Vs after the post-sputtering annealing. As expected, when carrier concentration is increasing, mobility is decreasing and vice versa [57]. Post-sputtering annealing is performed in both cases to know how the TCO will behave while simulating the recover from sputter-induced damage [51]. In case of IO:H/ITO bilayer, the post-sputtering annealing plays also the crucial role of transforming the IO:H film from its amorphous phase to poly-crystalline [15]. Measured values are well in accordance to state-of-the-art results [58,59], also with respect to resistivity (ρ_{ITO} = 1.5·10^{-3} Ω·cm, $\rho_{IO:H/ITO}$ ~5.4·10^{-4} Ω·cm after annealing).

This analysis shows a representative range of values for 75-nm thick TCO on textured Si since its thickness dependence is weak in the range 70–140 nm [60,61].

3.3. Solar cell demonstrators

The optimized layer stacks discussed so far were combined in solar cells following the fabrication process described in Fig. 2. Fig. 7 reports

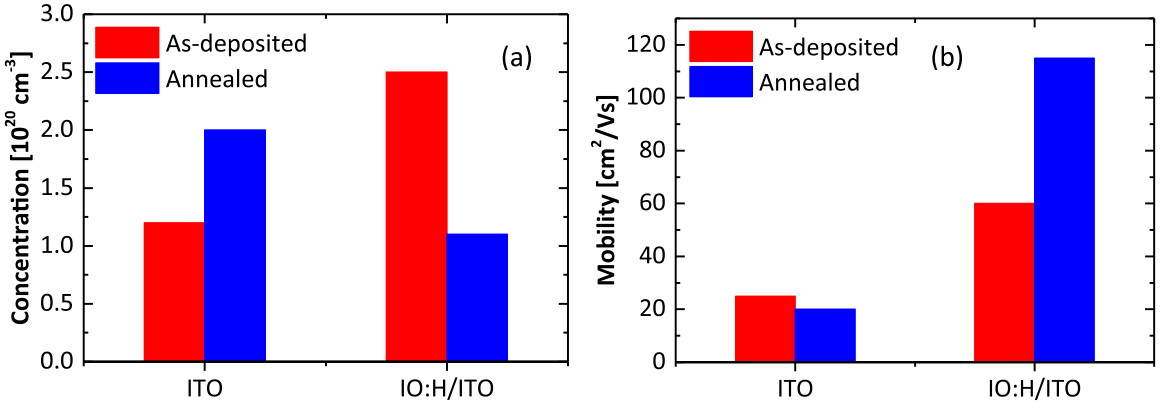

Fig. 6. (a) Carrier concentration and (b) mobility of samples in Fig. 1(d) and (e) with ITO or IO:H/ITO stacks before and after annealing at 180 °C for 30 min.

Table 2
External parameters of solar cells, (*) indicates that no annealing has been performed after a-Si:H deposition, (**) indicates that SC5 is the same as SC4 but with Ti-Cu plated front contacts.

	Area [cm^2]	$d_{i/n}$ [nm]	$d_{IO:H/ITO}$ [nm]	V_{OC} [mV]	J_{SC} [mA/cm^2]	FF [%]	Metal fraction [%]	$\eta_{aperture}$ [%]	pFF [%]
SC1*	7.84	4.5/6	0/75	695	36.5	71.0	5.0	19.0	81.0
SC2	7.84	3.5/6	65/10	703	37.0	71.2	5.0	19.4	81.0
SC3	9.00	4.5/6	65/10	707	39.7	72.0	2.64	20.7	82.1
SC4	9.00	4.5/6	0/75	704	39.5	73.8	2.64	21.0	81.6
SC5**	9.00	4.5/6	0/75	694	36.2	74.1	2.64	19.1	83.0

effective lifetime and iV_{OC} after each fabrication step.

As reported in Fig. 7, our process does not harm the passivation quality. Following all the steps described in Fig. 2, the effective lifetime lies above 4 ms and the iV_{OC} above 705 mV. This means that no contamination is introduced during our process and eventual damage due to sputtering has been recovered. For the particular solar cell shown in Fig. 7, we employed annealing at 190 °C for 30 min after a-Si:H deposition and we deposited IO:H / ITO stack (solar cell SC2 in Table 2). The measurement shown here is performed after post-TCO sputtering annealing at 180° for 30 min. Table 2 reports solar cells external parameters for different devices with variable intrinsic a-Si:H thickness. For SC1, which did not undergo any post-deposition annealing, the V_{OC} lies below 700 mV, while J_{SC} is 36.5 mA/cm^2 and FF is 71.6%. The J_{SC} is affected by parasitic absorption into i-layer. For this reason, we fabricated SC2 with a 3.5-nm thick i-layer. By employing IO:H/ITO stack, J_{SC} is established to 37 mA/cm^2. J_{SC} is 0.5 mA/cm^2 higher because of two factors: (i) 1 nm thinner intrinsic a-Si:H and (ii) improved TCO transparency due to IO:H. In SC2, V_{OC} is 703 mV due to post- a-Si:H deposition annealing and FF is limited 71%. This limitation comes from the front grid design. In fact, by passing to a larger area and a different front design (9-cm^2 wide square shaped with bus bars outside the active area and 2.64% metal shading), SC3 exhibits a higher J_{SC} up to 39.7 mA/cm^2 and FF = 72%. With such front contact design and device area, if only ITO is employed as in SC4, FF increases up to 73.8% because of a better band alignment at a-Si/ITO interface compared to IO:H/ITO stack [62]. This is due to higher carrier concentration in ITO that results in lower work-function than IO:H/ITO [63], therefore a more favourable condition for n-type contact. Nonetheless, J_{SC} decreases of 0.2 mA/cm^2 compared to SC3 because of higher parasitic absorption in the ITO TCO while V_{OC} is kept at 704 mV. Finally, the overall aperture-area efficiency of SC3 is 20.7% and, for SC4, it is 21.0%. Ti-seeded Cu-plated contacts have been employed at the front side of SC5. This contact formation technology enables a 0.3% absolute higher FF compared to SC4. However, as the process is not fully optimized yet, Cu is grown outside the designated area, costing a loss of 10 mV in V_{OC} and affecting also the J_{SC}. This effect is known as background plating [64] and solar cells performance might have been hindered due to Cu contamination [65]. Looking at the pFF column in Table 2, all our devices exhibit values > 81% and up to 83%. This implies that our process is not fundamentally flawed but rather limited by (i) the rear metallization, (ii) the possible dis-uniformity of the tunnelling oxide at the rear side and (iii) the conductivity of the front TCO.

4. Conclusion

In this work we applied carrier-selective passivating contacts with different thermal budgets to obtain a low thermal budget device. It consists in a rear p-type poly-Si/SiO_2 emitter deposited at temperatures up to 950 °C, followed by a low thermal budget deposition (~200 °C) of an intrinsic/n-type doped a-Si:H stack / TCO on the illuminated front side. We firstly investigated passivation properties of these CSPCs in dedicated symmetric samples. The poly-Si/SiO_2 passivation contact benefits from hydrogenation process with J_0 ~ 10 fA/cm^2 owing to improved chemical passivation at SiO_2/c-Si interface. Concerning the i/n a-Si:H stack, we observed that post-deposition annealing improves passivation quality with an optimum annealing temperature of 190 °C. This effect is due to a redistribution of hydrogen atoms into the film and at the c-Si/a-Si:H interface. Furthermore, we showed that annealing in H_2 leads to improved chemical passivation of the same surface. A series of annealing temperatures was made and 190 °C was found to be the most performing if 48 h degradation is considered. Moreover, also annealing environment is important. Indeed, annealing in H_2 has a better performance than conventional oven-based annealing. Moreover, we show the use two different TCO layer stacks consisting of either a single layer of ITO or a bi-layer of IO:H/ITO. Optical absorption measurement showed that the use of IO:H improves the transparency in the short-wavelength range with respect the ITO. Measured mobility is much higher for the IO:H/ITO stack (~120 cm^2/Vs) than ITO (~20 cm^2/Vs) and resistivity is lower in case of IO:H/ITO (ρ_{ITO} = $1.5 \cdot 10^{-3}$ Ω·cm, $\rho_{IO:H/ITO}$ ~$5.43 \cdot 10^{-4}$ Ω·cm after annealing). Post-sputtering annealing not only recovers from sputtering-induced damage, but also increases the mobility of our bi-layer TCO. In this paper we have demonstrated that at cell level, we keep high V_{OC} > 700 mV if annealing after a-Si:H deposition is performed. Then, changing front design with relatively low metal coverage (2.6%), J_{SC} increases up to ~40 mA/cm^2 and FF is 72% for the case of IO:H/ITO stack and 73.8% in the case of ITO only (up to 74.1% with Cu-plated front contact). Such FF value, together with a V_{OC} = 704 mV and a J_{SC} = 39.5 mA/cm^2 gives an aperture area efficiency of 21.0%. Few processing issues (Cu-plating, backside edge isolation, rear metallization, front TCO, etc.) still hold better performance, which targets an efficiency well beyond 22.5% in short term (V_{OC} > 705 mV, J_{SC} > 40.5 mA/cm^2, FF > 79%).

Acknowledgment

The authors would like to thank Mr. John Anker from ECN – Part of TNO to provide help with ECV measurement, Mr. Stefaan Heirman and Mr. Martijn Tijssen from PVMD group at Delft University of Technology for their technical help with PECVD reactor and metal evaporator. The authors would like to thank Advanced Dutch Energy Materials (ADEM) program for funding this research under the grant number TUDP18.

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