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LNA and Square Law Detector at 60 GHz for Passive Radiometers

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DELFT UNIVERSITY OF TECHNOLOGY
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LNA AND SQUARE LAW DETECTOR AT 60 GHz FOR PASSIVE RADIOMETERS
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Abstract

Millimeter-wave passive radiometers have earlier been designed in III-V integrated circuit (IC) technologies, due to their higher carrier mobility when compared to silicon, resulting in higher transit frequencies (f_T) thereby enabling to operate at higher frequencies. However, increased f_T in SiGe BiCMOS technology has generated interest for passive radiometer realization in these technologies. This thesis focusses on the design of low noise amplifier (LNA) and square law detector meant for realizing a 60 GHz RF-front end for passive radiometer application using 0.25 μm BiCMOS technology. The design details of the LNA including the influence of layout parasitic are described. In particular, a detailed discussion on the LNA layout at 60 GHz and the need for electromagnetic (EM) verification simulation is presented. To this end, a design procedure of LNA is presented which takes into account the layout parasitics at the early stages of the design.

Two LNA designs are discussed. The first LNA is designed to drive the detector input impedance and the second one is designed with a tapped capacitive transformer for output matching. The LNA driving the detector impedance achieves a post layout simulation gain of 21.3 dB of gain, 4.8 dB of noise figure at 63 GHz while the LNA designed for output matching achieves 19.6 dB and a noise figure of 4.8 dB at 63 GHz. The design of square law detectors using standard bipolar configurations is also presented in this thesis and are benchmarked for performance in terms of the detector specifications.

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List of Abbreviations

| | |
|---------|---|
| AC | Alternating Current |
| A/D | Analog-to-Digital |
| ADS | Advanced Design System (<i>Agilent EEsof</i>) |
| BEOL | Back-End-Of-the-Line |
| BiCMOS | Bipolar CMOS |
| CC | Common Collector |
| CB | Common Base |
| CE | Common Emitter |
| CMOS | Complementary Metal Oxide Semiconductor |
| DC | Direct Current |
| DTI | Deep Trench Isolation |
| EM | Electromagnetic |
| FCC | Federal Communications Commission |
| GHz | Giga Hertz |
| IR | Infra-Red |
| ISM | Industrial, Scientific and Medical |
| LNA | Low Noise Amplifier |
| LO | Local Oscillator |
| MAG | Maximum Available Gain |
| MIM | Metal Insulator Metal |
| MHz | Mega Hertz |
| MM-wave | Millimetre-wave |
| NF | Noise Figure |
| NEP | Noise Equivalent Power |
| NETD | Noise Equivalent Temperature Difference |
| RF | Radio Frequency |
| SiGe | Silicon Germanium |
| WPAN | Wireless Personal Area Networks |

List of symbols

| | |
|----------------|-----------------------------------|
| I_C | Collector current |
| V_{BE} | Base-to-emitter voltage |
| \mathfrak{R} | DC responsivity |
| τ | Integration time |
| B_{RF} | RF Bandwidth |
| B_{LF} | Post-detection Bandwidth |
| C_π | Total base-emitter capacitance |
| C_μ | Base-collector capacitance |
| C_{je} | Base-emitter junction capacitance |
| C_{diff} | Diffusion capacitance |
| C_{int} | Inter-stage node capacitance |
| β_{dc} | Current gain |
| g_m | Transconductance |
| f_T | Transit frequency |
| T_B | Brightness temperature |
| T_A | Antenna temperature |
| T_R | Receiver temperature |
| T_{SYS} | System temperature |
| k | Boltzmann constant |

Chapter 1

Introduction

The availability of the frequency spectrum has always played an important role in the development and expansion of wireless communication. This has led to the emergence of various standards and numerous applications employing the allocated spectrum. Of particular interest in the available frequency spectrum are the unlicensed frequency bands, which has resulted in innovative wireless solutions and have helped leverage the cost free usage of the spectrum. The term unlicensed frequency band refers to the range of frequencies in which no usage fee is levied on the transmission of signal. The federal communications commission (FCC) made available the industrial, scientific and medical (ISM) bands at 460 MHz, 910 MHz, 2.4 GHz etc., in 1985 for unlicensed usage [1.1]. Typical applications in the ISM band includes wireless voice and video applications in a consumer electronics context such as wireless personal area networks (WPAN) and BluetoothTM for handheld devices and personal computers. However, performance in these bands is restricted by congestion and limited available bandwidth, which is typically narrowband (on the order of a few megahertz (MHz)). The 57-64 GHz millimeter wave frequency band, relaxed by FCC for unlicensed usage, provides two key advantages.

- Firstly, the large available bandwidth close to 6-7 GHz can help boost the data rate significantly and provide sufficient bandwidth for narrowband applications even at 10% of the operating frequency of 60 GHz.
- Secondly, operation at higher frequencies reduces component size, thus increasing the possibilities of system (i.e., co-integration between circuits and antenna) integration. For instance, an array of antennas [2] can be employed by virtue of its scaled size resulting from the higher operating frequency. For example, a 4x4 array with $\lambda/2$ element size and $\lambda/2$ spacing between the antenna elements at 2 GHz would turn out to be much bigger than compared to at 60 GHz.

The aforementioned advantages of large bandwidth and reduced component size at millimeter-wave frequencies has also led to realization of passive radiometers ([1.4]-[1.5]). Radiometers have been widely used in a range of scientific applications such as remote sensing, radio astronomy etc.,.

Of particular interest in this thesis is the human presence detection system using radiometers. The focus here is on measuring the electromagnetic radiation emitted by objects, given that its intensity is proportional to the brightness temperature T_B (Planck's law), which can be done in the infrared (IR) and millimeter wave region. To this end, emissivity of the object can be defined as the measure of the radiation efficiency of a body. In the IR region, a human body is a near-ideal radiator due to its high emissivity and hence an IR-based detection works better in nocturnal environments where presence of a human body can be easily detected with good thermal contrast. However daylight conditions limit thermal contrast and hence detection. Further, due to short IR wavelength, penetration through large volume objects such as the human body is attenuated greatly, rendering the object appear opaque and hence detection becomes difficult. On the other hand, millimeter waves due to their longer wavelengths can penetrate large volume objects and detection becomes easier. For instance, a human body can be easily detected in the vicinity of a small lamp since millimeter waves can penetrate the body due to its relatively larger volume and hence a larger emissive area. Therefore, a millimeter-wave passive radiometer system can be envisioned. The goal of the thesis is the design of circuit blocks at 60 GHz for passive radiometer aimed at human presence detection in indoor environments. The choice of 60 GHz as the operating frequency is motivated by the possibilities of component size reduction and hence better integration of the entire system. Although the attenuation caused due to oxygen absorption peaks at 60 GHz, the proposed application targets detection within small distances between the objects, thus not affecting the system performance. The next section (section 1.1) provides a brief overview of the passive radiometer and the challenges (section 1.2) for its design.

1.1 Proposed Application

The circuit blocks designed in this thesis are intended to provide the enabling technology to realize the millimeter-wave passive radiometer designed for presence detection in indoor environments.

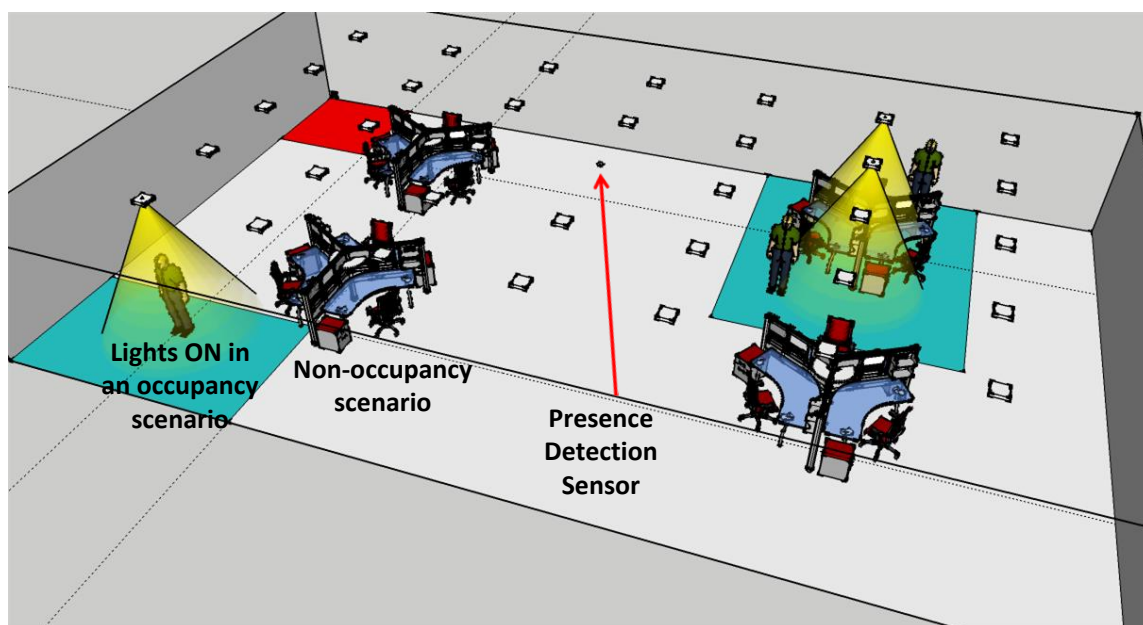


Fig. 1.1 Pictorial representation of the proposed application

Fig. 1.1 shows the proposed application in which the presence detection sensor can be used for automatic power turn-on of lights (and other systems) in case of occupancy. The proposed passive radiometer can thus be envisioned in scenarios such as “smart buildings” i.e., buildings employing sensor technology for reducing their energy footprint.

1.2 Passive Radiometer Overview

Passive radiometry focusses on measuring the thermal radiation emitted by objects (which is proportional to their brightness temperature). A radiometer effectively measures equivalent noise power of the area received by the antenna which can be

related to the object temperature by the well-known expression of the black body radiation i.e., $N = kTB$. The radiometer can generate images or detect objects in a scene of observation which depends on the emissivity of the objects and the background.

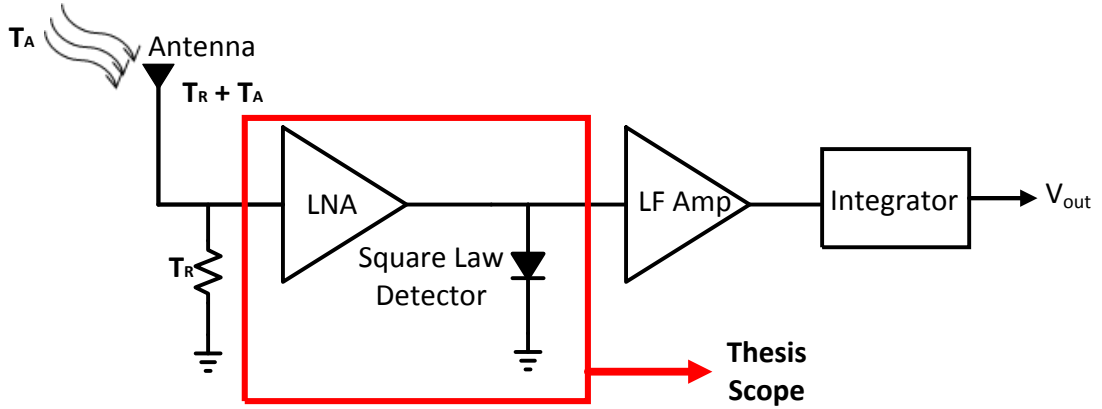


Fig. 1.2 Passive radiometer system block diagram [1.4]

Fig.1.2 shows a simplified block diagram of a passive radiometer system [1.4] where T_A and T_R are the antenna and receiver temperature, respectively. The antenna receives noise power, proportional to target object's radiation intensity. A high gain low noise amplifier (LNA) amplifies the received input in order to produce a useful measurable output. The output power from the LNA is fed to the square law detector, thus generating a DC output, proportional to the input power. Following the detector a low frequency amplifier is used to produce the right signal amplitude for detection to reduce the noise of the analog-to-digital (A/D) converter.

The overall noise of the contribution of the LNA is given by its noise figure (NF) and the noise contribution of the detector stage is specified in terms of the noise equivalent power. To this end, first we define the DC responsivity of a detector, which is essentially a detector gain is given by [1.4]

$$\mathfrak{R} = \frac{V_{outDC}}{P_{in}} \quad (1.1)$$

where P_{in} is the input power and V_{outDC} is the DC output voltage. Further, the noise equivalent power (NEP) is given by the ratio of the output rms noise voltage within the low frequency output bandwidth B_{LF} (which is the bandwidth of the integrator), to the DC responsivity (\mathfrak{R}) and written as [1.4]

$$NEP = \frac{v_n}{\mathfrak{R}} = \frac{v_n}{V_{outDC}/P_{in}} \quad (1.2)$$

It is clear from (1.2) that the detector design efforts should aim to lower output noise voltage and maximize \mathfrak{R} for a lower NEP. To this end, the resolution of the radiometer system can be related to the NEP, given by the noise equivalent temperature difference ($NETD$) and can be written as [1.4]

$$NETD = \sqrt{\left(\frac{2T_S^2}{B_{RF}} + \left(\frac{NEP}{kGB_{RF}}\right)^2\right) \frac{1}{2\tau}} \quad (1.3)$$

where T_S is the system noise temperature, NEP is the noise equivalent power, G is the gain of LNA, k is the Boltzmann constant, B_{RF} is the bandwidth and τ is the integration time. For a better temperature resolution, one can infer from (3) that a lower NEP and a large bandwidth are required.

1.2.1 Passive against Active Imaging

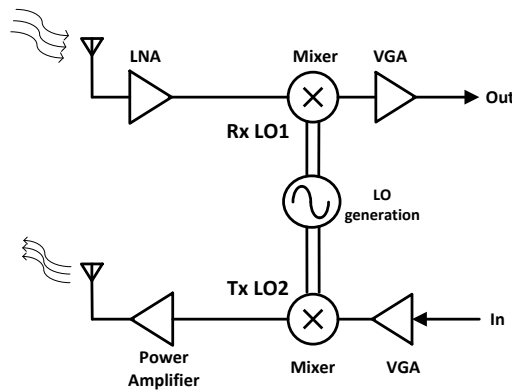


Fig. 1.3 Example of a direct conversion transceiver

Passive radiometers differ from their active counterpart since the former does not transmit any energy and it only receives energy (i.e., noise power), while the latter

transmits power to the target and receives a reflected echo. For this reason active radiometers employ a transmitter, thus increasing system complexity. Fig. 1.3 shows an example of a direct conversion transceiver which can be used for an active radiometer and consists of transmit-receive blocks with a local oscillator (LO) signal generation block for the upconversion and downconversion of the signal. The power consumption of the system increases as well. Other problems include the leakage of the LO signal through the receiver antenna. Shown in fig. 1.4, the LO signal can leak through the antenna and may saturate the LNAs in other receiver circuits operating in the zero-IF band [1.6].

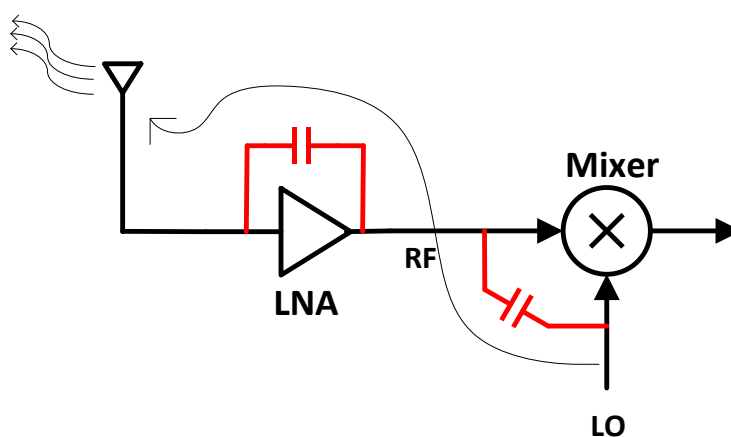


Fig.1.4 Problem of LO leakage [1.6]

On the other hand passive radiometer systems shown in Fig. 1.2 requires a detector for signal downconversion, thus avoiding the need for a transmitter and the complex LO circuitry for signal downconversion since the detector output signal is a DC signal which can be realized using square law region of the transistor i.e., the region in which output voltage is proportional to input power. Thus, passive radiometer imaging is preferred over the active imaging due to reduced circuit complexity, lower power consumption and ease of implementation.

1.2.2 Integrated Circuit Realization

The integration of the LNA and the downconverter helps in minimizing the board components, reduces the number of on and off chip connections and provides the opportunity to interface LNA with the downconverter. Further, a low cost BiCMOS technology (for example, bigger process nodes of 0.25 μm) can help reduce the costs since the bandwidth of the demodulated signal in the proposed radiometer is very small.

1.2.3 Enabling Technology

Millimeter-wave circuits designed using III-V semiconductors have been reported extensively ([1.8]-[1.10]). This is motivated by the fact that III-V semiconductors have greater carrier mobility compared to silicon besides lower noise and higher transit frequencies (f_T). However, recent advancements in silicon in addition to its better yield have slowly shifted the interest from traditional III-V based mm-wave systems to silicon [1.2]. The evolution of silicon germanium (SiGe) technology has resulted in increased f_T , exceeding 300 GHz [1.10]. This has paved the way for operation of circuits well beyond 30 GHz. Further, the advantages of SiGe bipolar transistors such as higher transconductance, higher breakdown voltages and low $1/f$ noise [1.11] have renewed interests in the advantages bipolar transistors offer when compared to metal-oxide semiconductor (MOS) transistors in terms of parameters such as noise and power consumption. One of the first papers reported by Floyd, et al [1.12] demonstrated a transceiver circuit designed in a 0.12 μm SiGe BiCMOS technology and operating at 60 GHz. Since then, BiCMOS circuits for mm-wave have been reported for various applications. The fact that SiGe-based circuits can be easily integrated with the CMOS analog and digital circuitry makes it more interesting from an economic standpoint, especially in cases where silicon is envisaged for volume productions. In this thesis, the technology for circuit analysis and design is supplied by NXP Semiconductors' 0.25 μm QUBIC4xi™ BiCMOS [1.13].

1.3 Thesis Motivation and Objectives

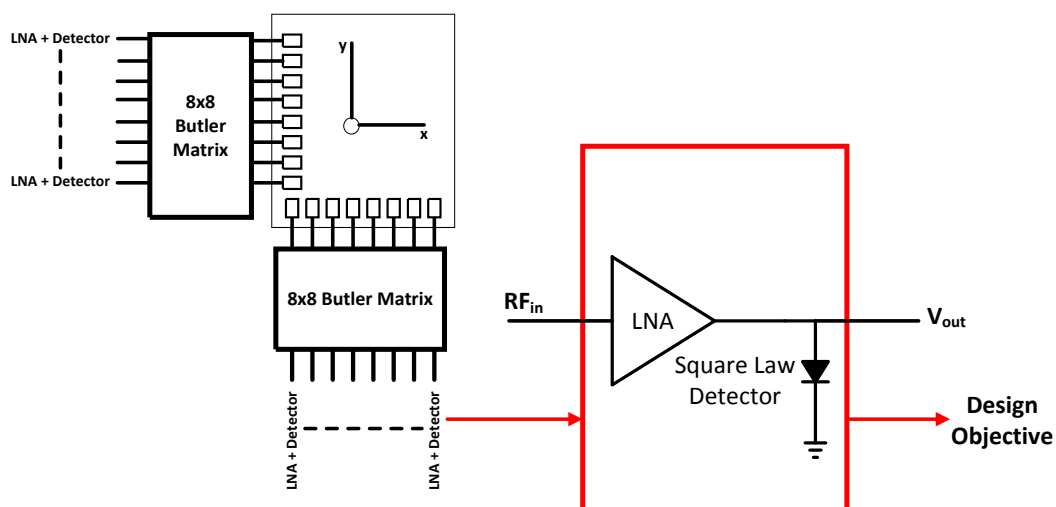


Fig. 1.4 Passive radiometer system showing butler matrix and LNA+ Detector arrangement

The objective of this thesis is to investigate the design of a low complexity RF front-end system at 60 GHz which comprises of a low noise amplifier (LNA) and a square law detector. The building block developed in this thesis work is intended to be combined with the 8x8 butler matrix array designed in [1.14], enabling the realization of a passive radiometer system aimed at presence detection in indoor environments (see Fig.1.5).

Following are the goals of the thesis:

- Co-integration of the LNA with the square law detector on the same chip and hence reduce the component size and reduce on-chip to off-chip connections.
- Performance optimization of the LNA with the high input impedance of the square law detector.

- Low power consumption of the LNA and detector. For instance, for presence detection application regulation of a 6 Watts light must not be made feasible with a radiometer which consumes 10 Watts of power or more.

1.3.1 Design Challenges at Millimeter Wave Frequencies

The idealized schematic-level performance changes considerably during the layout phase of the design. As the frequency increases, the effect of the capacitive and inductive impedance significantly influences the LNA performance. For example, an interconnect line of 10 pH inductance corresponds to a reactance of 3.76 ohms at 60 GHz. One can observe performance degradation due to the effect of these parasitics on performance metrics such as gain, noise figure and stability of the amplifier. Therefore, design at millimeter frequencies requires careful considerations towards the final circuit. Some of the design challenges are listed below:

- At higher frequencies, the wavelength of the signals become shorter. If metal lines (for routing signal around the chip) become comparable to the signal wavelength lines, the distributed effects of the lines needs to be taken into account [1.15]. As an example, the wavelength of the guided wave at 60 GHz in free space is 5mm and reduces even further when it travels through a medium with higher dielectric constants such as silicon dioxide (2.5mm) and silicon (1.45mm). As a rule of thumb, any line on the order of one-tenth of the wavelength should considered as distributed [1.16]. To this end, commercially-available electromagnetic (EM) simulators (such as Agilent Momentum™, Ansoft HFSS) are used to account for such effects on the circuit performance.
- The on-chip ground plane impedance may affect the amplifier performance parameters such as gain. An estimate of this impedance can be arrived at with the use of EM simulators and can be accounted for in the design.

- The stability of the amplifier is another concern, which needs to be considered in the verification phase. The amplifier may oscillate due to the presence of the reactive parasitics. For instance, inductance metal interconnects at the base terminal of a bipolar transistor may transform to the emitter terminal as a negative resistance, which can trigger oscillatory conditions in the circuit. Hence, great care needs to be taken in minimizing the effect of these parasitics to achieve overall amplifier stability.
- Careful floorplanning is required in order to achieve a compact, area efficient layout. For instance, magnetic coupling may persist between on-chip inductors and metal interconnects in close proximity. EM simulators are needed to account for the extent of the coupling in such cases and an estimate of the safe distance must be arrived at, based on these simulations.

1.4 Organization of the Thesis

Chapter 2 presents an detailed overview of the passive radiometer, which includes a discussion at the system level and the design metrics of LNA and the square law detector. A literature study of the LNA is also presented in this chapter.. Chapter 3 presents the design procedure of the LNA which includes the influence of layout parasitics. Chapter 4 presents the design and analysis of square law detector with standard bipolar transistor configurations. Chapter 5 presents a detailed discussion of the LNA layout and also the lumped element modelling of the single ended monolithic inductors and pi-equivalent modelling of the interconnect, followed by the post layout performance results. Conclusions and future work are presented in chapter 6.

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Chapter 2

Passive Radiometer Background

This chapter presents a background theory of the passive radiometer for detection applications and its performance metrics. The performance metrics of the LNA and square law detector are discussed from the passive radiometer context and a link budget analysis is presented to illustrate the required specifications of the LNA for the chosen application. Finally, a background study of LNAs reported in literature is presented.

2.1 Millimeter-Wave Radiometer

Passive radiometry relies on the natural emission of thermal radiation by an object. At the frequency of interest f , assuming ideal blackbody isotropic radiation the thermal radiation is related to the brightness B_f by Planck's radiation law, given by:

$$B_f = \frac{2hf^3}{c^2(e^{hf/kT}-1)} \quad (2.1)$$

where k is Boltzmann constant, h is Planck's constant and T is the temperature of the object. For $hf \ll kT$, the second argument in the denominator can be expanded using Taylor series, thus reducing (2.1) to the Rayleigh-Jeans approximation for brightness B_f given by [2.1]:

$$B_f = \frac{2f^2kT}{c^2} = \frac{2kT}{\lambda^4} \quad (2.2)$$

where B_f is proportional to the fourth power of wavelength. It is instructive compare the approximation with Planck's radiation law as the frequency of operation is increased.

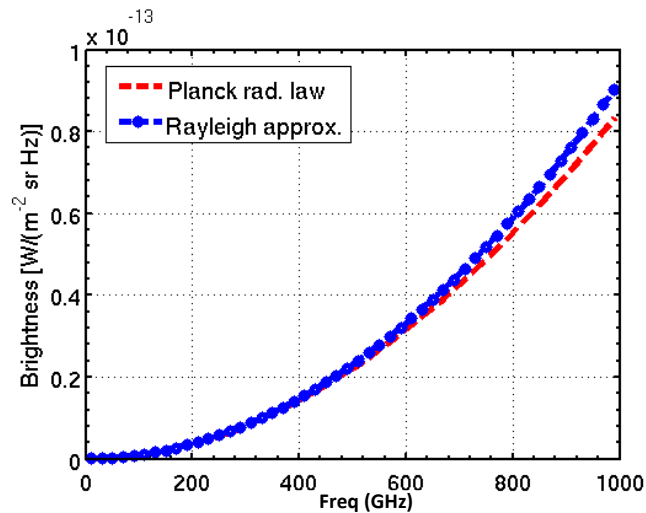


Fig. 2.1 Brightness of an ideal black body as a function of frequency at T=300K

Fig. 2.1 provides a comparison of the equations (2.1) and (2.2), showing a close fit at millimeter-wave frequencies (from 30 GHz) at 300 K, though deviations can be observed at very high frequencies. It can then be inferred that for passive millimeter-wave radiometers, Rayleigh-Jeans approximation is valid, thus ensuring the validity for the chosen application of isotropic radiation.

2.1.1 Direct-detection Radiometer with Preamplification

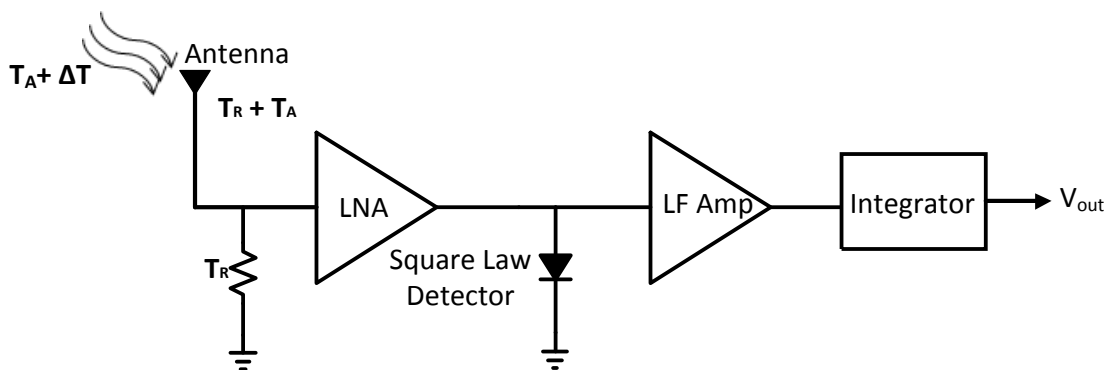


Fig. 2.2 Simplified block level view of passive radiometer system [2.4]

Fig. 2.2 shows the direct-detection radiometer with preamplification, the working of which was briefly introduced in chapter 1. It is instructive at this point to study the underlying working principle of this radiometer in more details. The noise temperature of the system is given by

$$T_{sys} = T_A + T_R \quad (2.3)$$

where T_A is the antenna noise temperature and T_R is the receiver noise temperature. The total noise power referred to the antenna can be written as [2.2] :

$$P_{tot} = kT_{sys}B_{RF} \quad (2.4)$$

where B_{RF} is the pre-detection bandwidth. It is important to note that (2.4) does not take into account the signal noise power which is proportional to the change in the target noise temperature, given by [2.2] :

$$P_{sig} = k\Delta TB_{RF} \quad (2.5)$$

The signal power received by the antenna (given by 2.5) is fed to the LNA which amplifies the signal to a measurable output while minimizing the added noise due to its circuit elements. The output power is fed to the square law detector, which generates a DC output proportional to the input power, given by:

$$V_{outDC} = \Re P_{IN} \quad (2.6)$$

where \Re is the DC responsivity (V/W) [2.4] and is also the measure of the detector gain. For a sinusoidal input $V_{IN} = A \cos \omega t$, the corresponding output signal is obtained as a sum of the DC component and a second harmonic (at 2ω) and (2.6) is modified as :

$$V_{out} = \Re V_{IN}^2 [(1 + \cos 2\omega t)/2] \quad (2.7)$$

The DC term V_{outDC} from (2.7) can be obtained by averaging the signal with an integrator with an integration time $\tau = 1/B_{LF}$ where B_{LF} is the post-detection bandwidth of the integrator.

The sensitivity of the direct detection radiometer can be then defined for an ideal square law detector, as the minimum temperature that can be resolved at the system input (or NETD) is given by [2.4] :

$$NETD = T_S \sqrt{\frac{2B_{LF}}{B_{RF}}} \quad (2.8)$$

However, (2.8) does not take into account the noise of the detector and the performance of the LNA (i.e. gain). A more complete expression of $NETD$ to account for the detector and LNA performance is given by :

$$NETD = \sqrt{\left(\frac{2T_S^2}{B_{RF}} + \left(\frac{NEP}{kGB_{RF}}\right)^2\right) \frac{1}{2\tau}} \quad (2.9)$$

where NEP is noise equivalent power and G is the LNA gain. For applications such as presence detection and imaging for security purposes, it is desired to have a fine temperature resolution (or minimum possible NETD). From (2.9), it can be shown that to achieve a finer temperature resolution, the available system bandwidth must be maximized and also gain of the LNA, which is critical to suppressing the noise contribution of the detector.

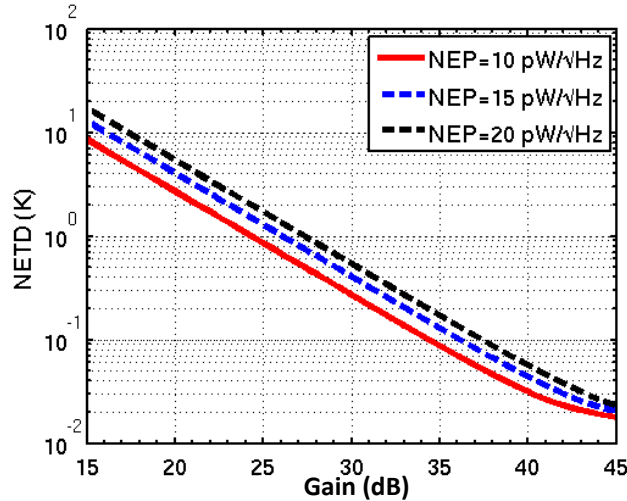


Fig. 2.3 NETD as function LNA gain for increasing detector NEP

Fig. 2.3 shows the effect of increasing NEP on the system resolution computed for $\tau = 100 \text{ ms}$ and $B_{RF} = 6 \text{ GHz}$ i.e., 10 % of the operating frequency (of 60 GHz). It is

clear from Fig. 2.3 that for a given NETD, increase in NEP requires higher LNA gain or alternately a higher LNA gain is required to suppress detector noise.

LNA Gain and Noise Figure

In a typical receiver system, the LNA is the first circuit block in the system chain. The reason for this can be easily explained by looking at the overall noise of a cascaded block of gain stages i.e., using Friis formula. Fig. 2.4 shows a cascaded system (for e.g. a receiver chain) with gain of each block given by G_i and a noise factor F_i .

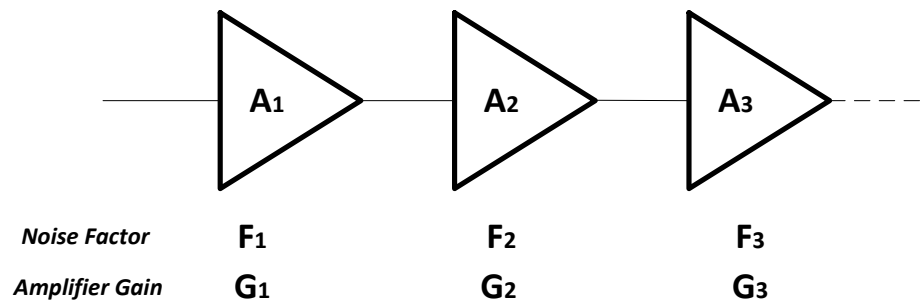


Fig. 2.4 Cascaded system showing gain and noise factor

The total noise factor of the cascaded chain is given by [2.3]

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} + \dots + \frac{F_N - 1}{G_1 G_2 G_3 \dots G_{N-1}} \quad (2.10)$$

(2.10) indicates that the gain of the first stage (given by G_1) is crucial in minimizing the overall noise factor of the system. A similar argument applies to the radiometer receiver chain in which the high gain of the LNA helps suppress the noise contribution of the detector, which is quite significant given the large noise floor of the detector [2.5]. Further, it is also important to look at the noise contribution of the LNA itself. The noise floor at the LNA input determines how small a signal a receiver handle. Thus, the LNA noise contribution needs to be minimized as well so that the signal to be detected is well above the noise floor.

Detector Responsivity and NEP

The detector performance is characterized by its DC responsivity (\mathfrak{R}) and the NEP. A higher responsivity is desired or alternately, a higher DC component of the output signal needs to be obtained. From (1.2), it can be seen that a higher \mathfrak{R} suppress the detector output noise. Alternately, it can also be said that increase in \mathfrak{R} reduces the signal power required. As can be seen from (2.9), a higher NEP degrades the system NETD and hence it needs to be minimized. It is important to note both \mathfrak{R} and NEP are strong functions of the circuit design aspects [2.4] and the accuracy of these design metric numbers largely depends on the simulation methodology.

Integration time

The signal processing task, post-detection is carried out by the low frequency (LF) amplifier which in turn, feeds the signal to the integrator for averaging over the post-detection bandwidth B_{LF} . From (2.9), it can be seen that a larger integration time (τ) results in a better NETD. However, a larger τ also translates to a slower system.

2.2 Link Budget Analysis

The presence detection application requires the system to be able to detect small variations in temperature, thus the system must aim at a low NETD. To achieve this goal, the focus of the circuit design will be to minimize the noise contribution of the circuit blocks in the radiometer front-end chain. In this section, we present a simple link budget analysis to derive suitable design metric numbers, taking into account the following considerations:

- The radiometer system for this project targets an NETD of 1K with an integration time of 100 ms.
- The antennas for this radiometer system, designed in [2.6] limits the bandwidth of the system which is about 6 GHz with a centre frequency of 63 GHz (i.e. 10 %).

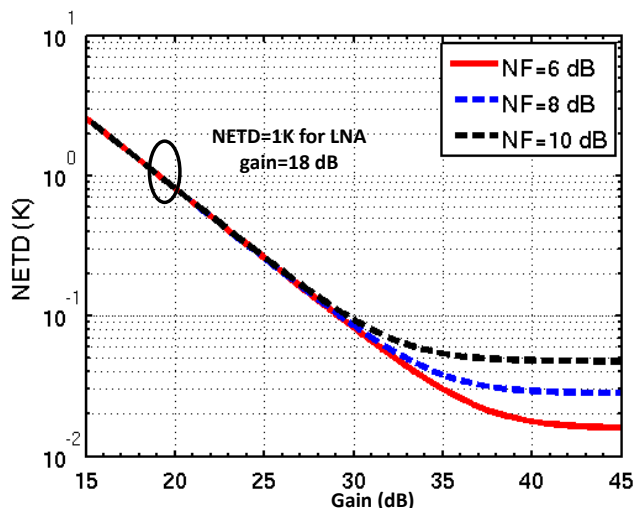


Fig. 2.4 NETD calculation for different LNA noise figure values using [2.9]

First, NETD of 1K translates to 10 dB of total system noise figure. Out of 10 dB NF, the noise due to antenna and the butler matrix account for 3 dB [2.6]. The LNA noise figure can now be calculated from (2.10), which is about 6.7 dB. From (2.9), we can arrive at the LNA gain using the aforementioned considerations of RF bandwidth and the integration time, which can help achieve the target NETD of 1K. Fig. 2.5 shows the plot for NETD as a function of the LNA gain for different noise figure values which shows a gain requirement in the vicinity of 18-19 dB for NETD=1 K.

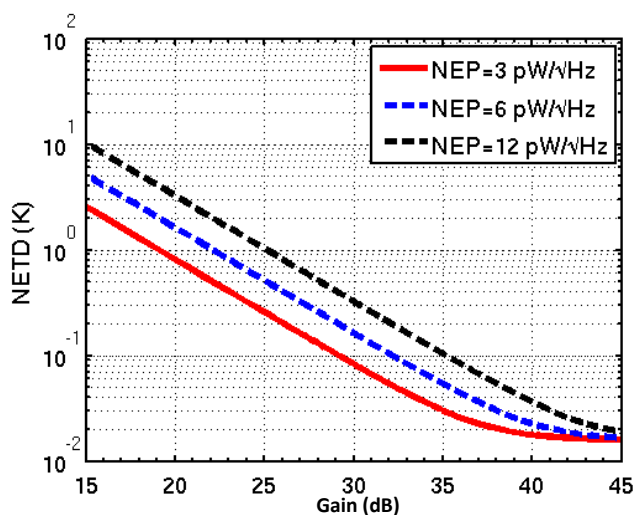


Fig. 2.5 NETD calculation for different LNA noise figure values

Fig. 2.5 shows the variation of NETD as a function of the LNA gain for different values of detector NEP. To obtain the required NETD, given a LNA gain of 18 dB, an NEP of $3 \text{ pW}/\sqrt{\text{Hz}}$ should be achieved. A summary of the proposed specifications of the LNA is provided in Table 2.1.

Table 2.1 Proposed LNA specification

| LNA Performance Parameter | Specifications |
|--------------------------------------|----------------|
| Gain (dB) | ~18-19 |
| Noise Figure (dB) | 6-7 |
| Bandwidth (GHz) | 6 |
| Integration time (ms) | 100 |
| NEP ($\text{pW}/\sqrt{\text{Hz}}$) | 3 |

2.3 LNA Literature Review

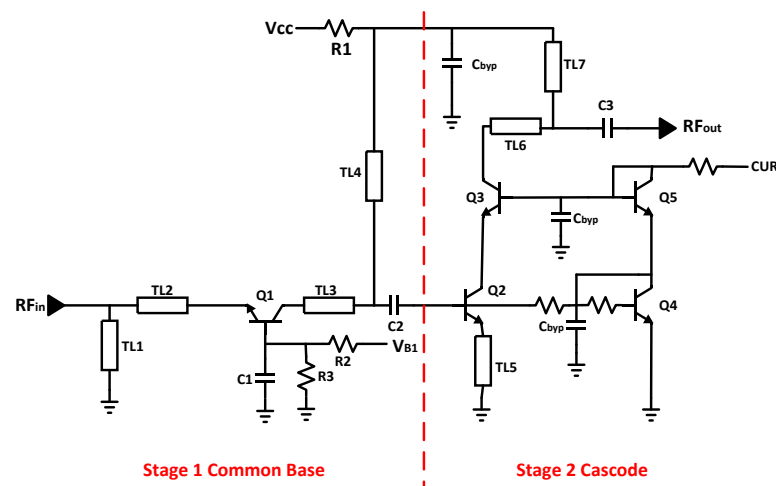


Fig. 2.6 60-GHz low noise amplifier [2.7]

In this section, LNA circuit topologies reported in the literature are reviewed. Fig. 2.6 shows one of the first silicon implementation of an LNA at 60 GHz, reported by Floyd et al [2.7]. The absence of miller capacitance in the 1st-CB stage (i.e., Q₁) helps achieving better reverse isolation.

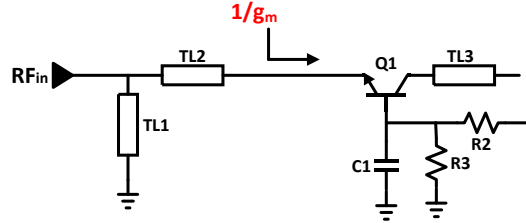


Fig. 2.7 1st stage CB amplifier showing input impedance seen at the emitter node

Another advantage of CB stage is the input matching. Shown in Fig. 2.7, the 1st stage CB has a low input impedance which helps in input matching by setting transconductance (g_m) of the stage as $1/g_m=50 \Omega$. However, the g_m (and hence the matching) of this stage is strongly traded off with the noise figure since the latter is also strong function of the collector current I_C . Further, Z_{opt} of the bipolar transistor is given by [2.10]

$$Z_{opt} \approx \left(\frac{\omega_T}{\omega} \right) \sqrt{\frac{2(r_B+r_E)}{g_m}} + \frac{j}{\omega(C_\pi+C_\mu)} \quad (2.11)$$

(2.11) shows that if input impedance Z_{in} is set as $1/g_m=50 \Omega$, then the real part of Z_{opt} cannot be equal to this value. This suggests that the CB stage suffers from poor noise match or poor input match [2.10]

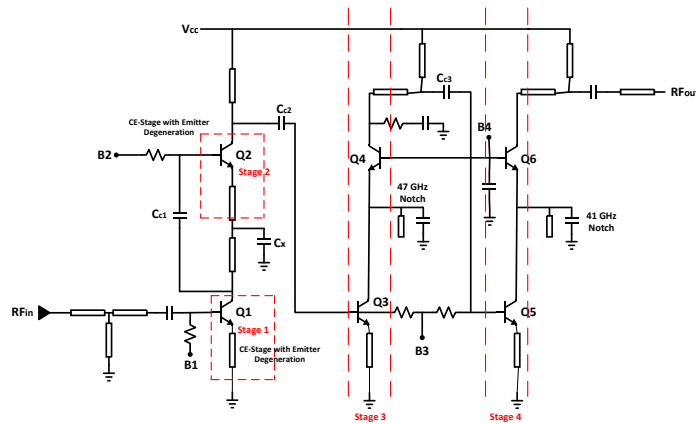


Fig. 2.8 4-stage 60-GHz LNA with current reuse technique [2.8]

Fig. 2.8 shows a 60 GHz LNA implemented in 0.13 μm BiCMOS technology [2.8]. Stages 1 and 2 are implemented as CE stages with emitter degeneration. Further, the 2nd stage CE is stacked above the 1st stage CE for DC current reuse. The signal at the collector of Q_1 is ac-coupled to the base of Q_2 and the capacitor C_x is used for ac-grounding of the Q_2 emitter. The idea is to use the DC current for the 2 stages which helps reducing the power consumption and provides the same gain as the 2-stage cascaded CE amplifier's. Stages 3 and 4 have been implemented as cascode amplifiers to obtain additional gain. The use of DC current reuse though, may not alleviate the problem of reverse isolation needed at high frequencies which will cause stability issues in the design.

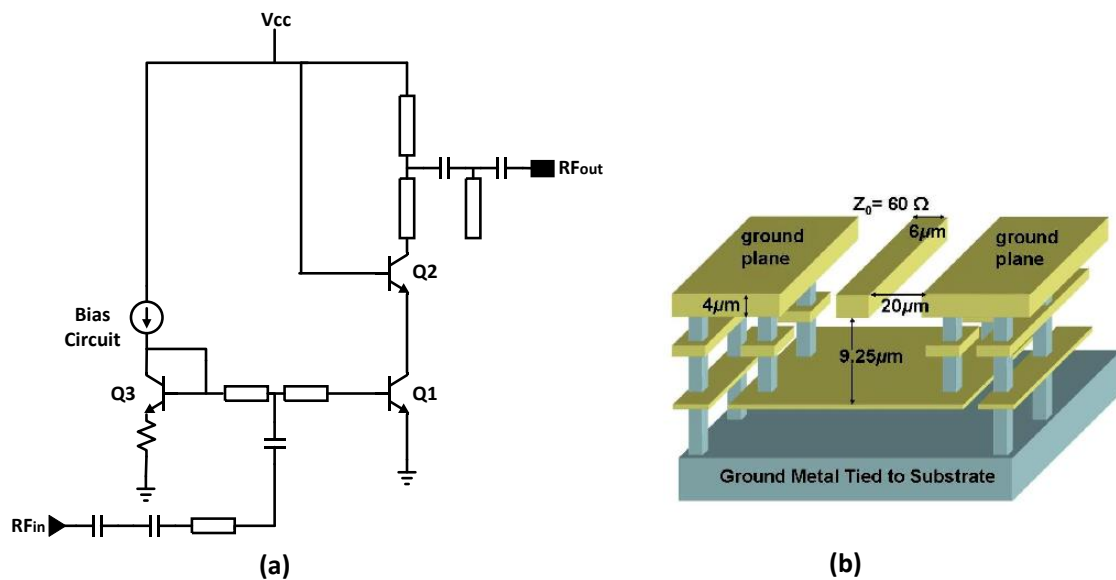


Fig. 2.9 (a) 60-GHz cascode LNA and (b) the layout approach for the ground plane [2.9]

Fig. 2.9 (a) shows a single stage cascode LNA at 60 GHz [2.9]. The circuit design is more layout intensive and the authors have stressed the need for a uniform ground plane from the top metal down to the substrate (see Fig. 2.10 (b)). Further, grounded substrate contacts have been placed near the active components as well as the use of deep trench isolation (DTI), thus minimizing the path to AC ground and reducing noise injection.

Table 2.2 60 GHz LNA performance comparison

| Specifications | [2.7] | [2.8] | [2.9] |
|------------------------------|-------------------------|-------------------------|-------------------------|
| Frequency (GHz) | 61.5 | 60 | 59 |
| Technology | 0.12 μm SiGe | 0.13 μm SiGe | 0.12 μm SiGe |
| Gain (dB) | 15 | 20 | 14.5 |
| Noise Figure (dB) | 4.5 | 5-6.2 | 4.1 |
| Input matching S_{11} (dB) | -10 | -12 | <-20 |
| Power Consumption (mW) | 10.8 | 27 | 8.1 |

A summary of the performance specifications of the LNAs discussed is provided in Table 2.2. From the above discussion, we observe the following:

- Cascode topology can be used to obtain higher gain at millimeter-wave frequencies. For instance, in [2.7], the cascode topology is employed in the 2nd stage for obtaining higher gain while in [2.8], 2nd and 3rd stage have cascode configuration for additional gain.
- DC current reuse topology helps achieve lower power consumption by stacking CE transistors. For example, a cascade of 2 CE stages may require 5 mA current in each stage i.e., a total current of 10 mA. On the other hand, current reuse uses the same current (of 5 mA) to bias both the stages, thus reducing the power consumption [2.8]. However, it does not alleviate the problem of reverse isolation which is critical to stability at millimeter wave frequencies.
- Layout techniques play a very important role in the LNA design since circuit grounding and substrate losses significantly influence the LNA performance.

2.4 Conclusions

A detailed overview of the passive radiometer system was presented. A system link budget analysis was discussed and the specifications for the LNA design was derived. A short literature review was also presented.

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Chapter 3

Design of 63 GHz Low Noise Amplifier

This chapter presents the design procedure of the 63 GHz 2-stage LNA carried out in this thesis project. Based on the design procedure, two LNA designs are analysed; the first LNA drives a high impedance load (i.e., 400 Ω) while the second drives a 50 Ω load through a tapped capacitive transformer. A summary of the LNA performance results is provided in the conclusions section.

3.1 SiGe Technology

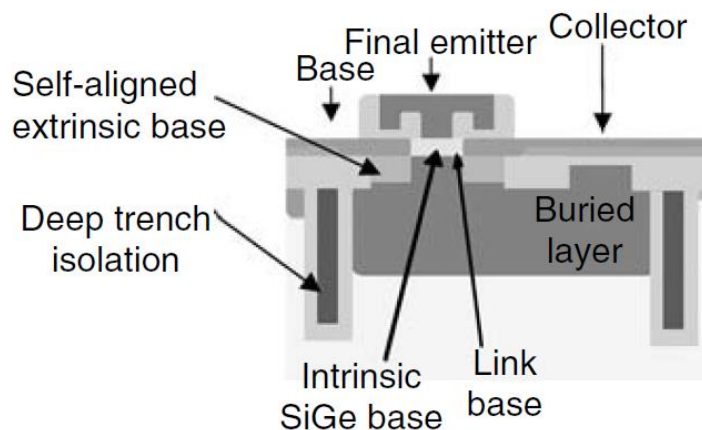


Fig. 3.1 SiGe npn transistor cross section [3.1]

Fig. 3.1 shows a cross section of the SiGe npn transistor showing buried n-layer and deep trench isolation (DTI), for isolating NPN collectors and to decrease the NPN collector-substrate capacitance. The transit frequency (f_T) of the SiGe transistors available in QUBIC4xi are 175 GHz (for the BNA model) and 193 GHz (for the BNY model) with a maximum supply voltage (V_{CC}) capability of 2.5 V [3.2].

3.2 Transistor Analysis

In this section, the SiGe transistor is used for analysis in terms of its transit frequency (f_T) and the minimum noise figure (NF_{\min}), as a function of the collector bias current I_C . The f_T of the transistor is defined as the frequency at which the magnitude of current gain of the transistor becomes unity, given by [3.2]

$$f_T = \frac{g_m}{2\pi(C_\pi + C_\mu)} \quad (3.1)$$

where g_m represents the transconductance. The capacitance C_π is a combination of two capacitances: base-emitter junction capacitance C_{je} and the diffusion capacitance C_{diff} . In order to help understand the relations between f_T and NF_{\min} with the transistor parameters, it is useful to review its small signal model.

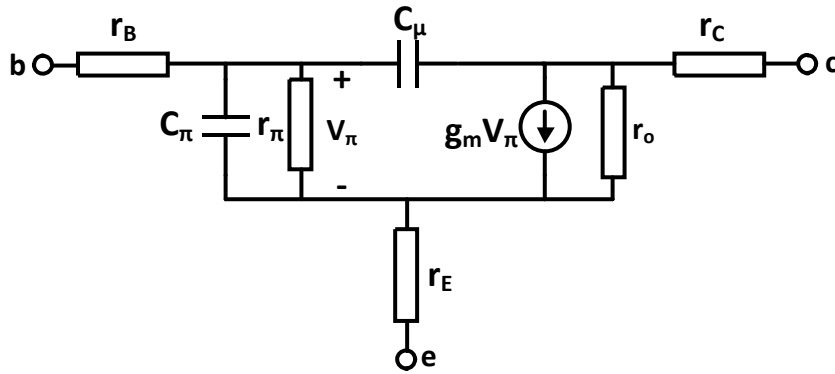


Fig. 3.2 Simplified small signal model

Fig. 3.2 shows the simplified small signal model of the transistor. The series resistances of the base, emitter and collector intrinsic to the transistor are shown respectively as r_B , r_E and r_C . The values of r_E and r_C are low because of highly doped emitter region and due to a buried layer in the collector, respectively [3.3]. The base resistance r_B is larger (compared to r_E and r_C) and hence plays a critical role since its noise contribution adds directly to the overall noise figure (NF). Table 3.1 shows the value of the resistances for the QUBIC4xi transistor.

Table 3.1 BJT intrinsic resistances values

| BJT Resistances | Value |
|---------------------|----------------|
| Base (r_B) | 210.7 Ω |
| Emitter (r_E) | 10.87 Ω |
| Collector (r_C) | 8.462 Ω |

The base-emitter (C_π) and base-collector (C_μ) capacitances are a sum of the total parasitic capacitances presented in the complete model and are directly related to the transit frequency (f_T), which determines the operational limit of the transistors in the circuit.

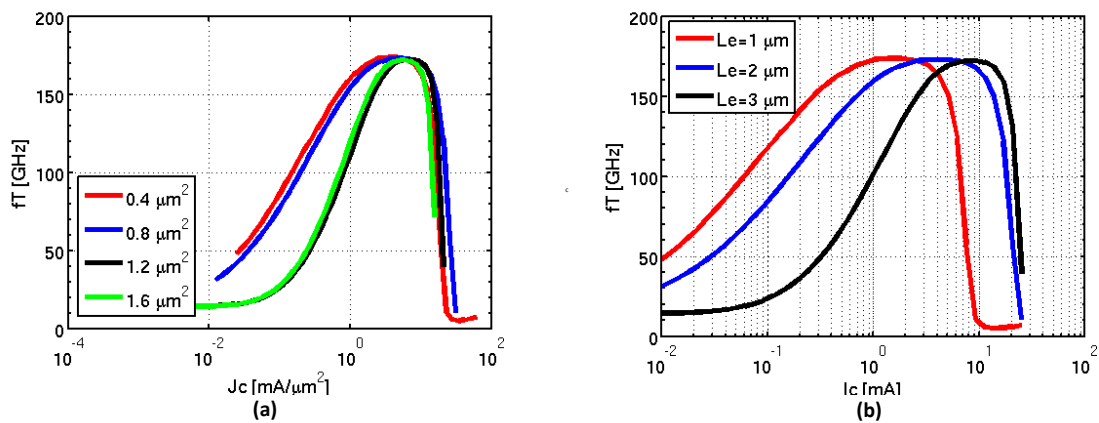


Fig. 3.3 f_T as a function of (a) current density J_C and (b) as function of I_C alone for different L_e

Fig. 3.3(a) shows the plot of f_T as a function of current density J_C , indicating that f_T is nearly independent of size for the same J_C . However, f_T is a strong function of the increasing emitter length (L_e) and hence the collector current I_C . Fig. 3.3(b) shows the f_T curve for different emitter lengths for the SiGe transistor.

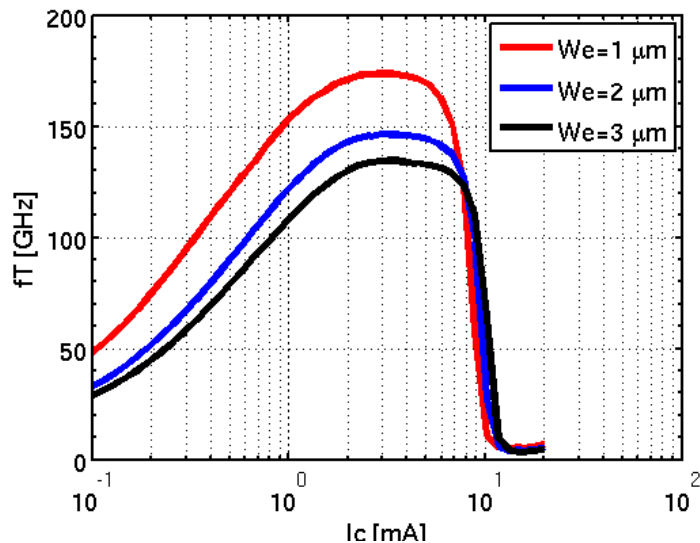


Fig. 3.4 f_T as a function of I_C for different emitter widths

Fig. 3.4 shows the f_T plot for different W_e values, keeping L_e fixed at $1 \mu\text{m}$. The peak f_T of the transistor decreases for the same I_C with increasing W_e values (due to increase in the value of C_{μ} , thus implying that W_e should be kept at its minimum value fixed by the technology. The NF_{\min} of a bipolar transistor also depends on small signal parameters and is given by [3.4]

$$NF_{MIN} = 1 + \frac{n}{\beta_{dc}} + \sqrt{\frac{2I_C}{v_T} (r_E + r_B) \left(\frac{f^2}{f_T^2} + \frac{1}{\beta_{dc}} \right) + \frac{n^2}{\beta_{dc}}} \quad (3.2)$$

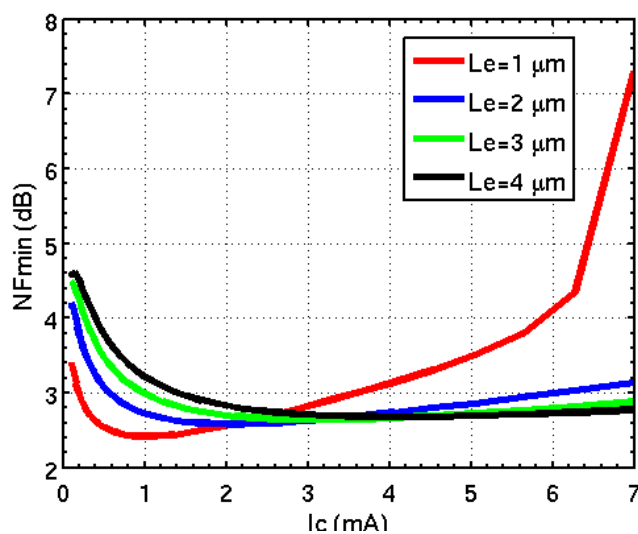


Fig. 3.5 NF_{\min} for different emitter lengths (L_e)

where n is the junction grading factor ($\sim 1-1.2$) and β_{dc} is the current gain. Fig. 3.5 shows the NF_{min} plot as a function of the bias current for different L_e values. Comparing (3.2) and Fig.3.5, it can be said that the increase in L_e increases the dc bias current which helps in lowering the transistor NF_{min} . It is also important to note that the collector current shot noise (i_{cn}) dominates for lower current values i.e., below 1 mA (see Fig. 3.5) and the base shot noise (i_{bn}) dominates for higher collector current values i.e., above 4 mA (see Fig. 3.5). By comparing Fig. 3.3 and Fig. 3.5, the transistor can be biased at a constant J_C close to peak f_T and the corresponding NF_{min} can be obtained from Fig. 3.5 by scaling the transistor L_e accordingly. For example, a J_C of $2 \text{ mA}/\mu\text{m}^2$, which is close to peak f_T and an NF_{min} of 2.7 dB can be obtained.

3.3 CE and Cascode Topology

Various circuit topologies are available for LNA which includes CE amplifier with transformer feedback [3.5], differential cascode stages [3.6], current-reuse technique to name a few. Of particular interest in this thesis is the single-ended cascode topology, which is quite popular in RF circuits for its properties such as high reverse isolation and increased gain at higher frequencies. First, we will review the CE transistor topology with respect to gain and reverse isolation.

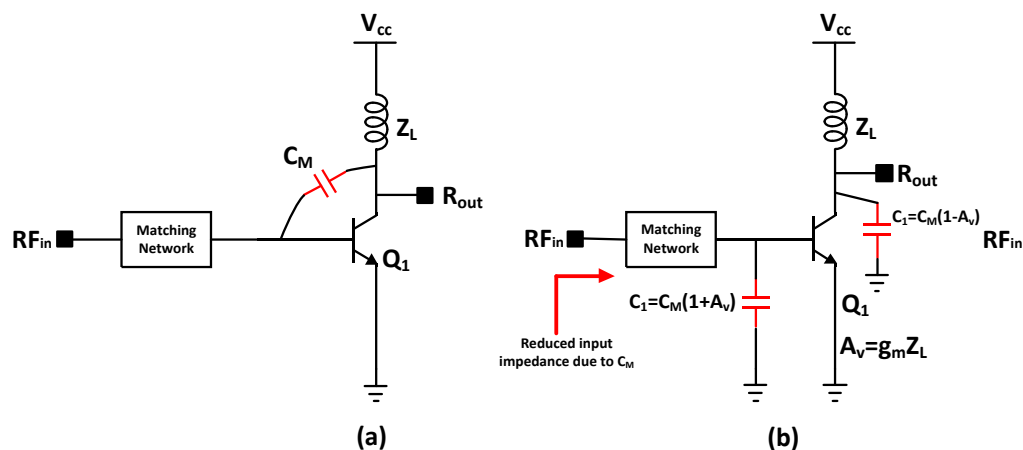


Fig. 3.6 Miller effect in CE amplifier

Fig. 3.6 (a) shows the Miller capacitance C_M in a CE amplifier, which provides direct signal path. Due to the gain of the transistor, the capacitance seen from input node to ground, increases by a factor $(1+A_V)$ which reduces the input impedance and also affects the input matching (see Fig. 3.6 (b)).

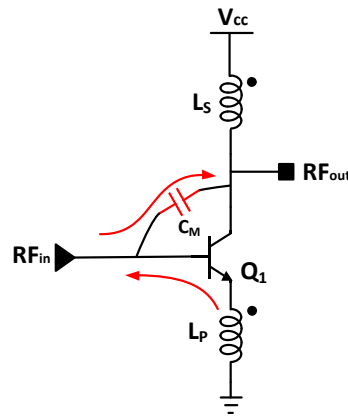


Fig. 3.7 Unilateralization technique using transformer [3.5]

Fig. 3.7 shows a technique of cancelling the effect for C_M using transformer feedback technique [3.5]. The magnetic coupling between the coils at collector and emitter terminals provide negative feedback, which feeds a portion of the signal to the input as shown in Fig. 3.7, thus minimizing the signal flow through C_M and cancelling the transistor's feedback effect. However, this neutralization technique depends strongly on the coupling coefficient k [3.5] and in turn, a transformer design suitable to this technique may depend on the back end of the line (BEOL) metal features of a given technology. This suggests that a transformer with a lower k -factor may not completely cancel the effect of the feedback capacitance. Further, the gain at milli-meter wave frequencies is limited and a transformer design limited by the BEOL features may affect the required gain.

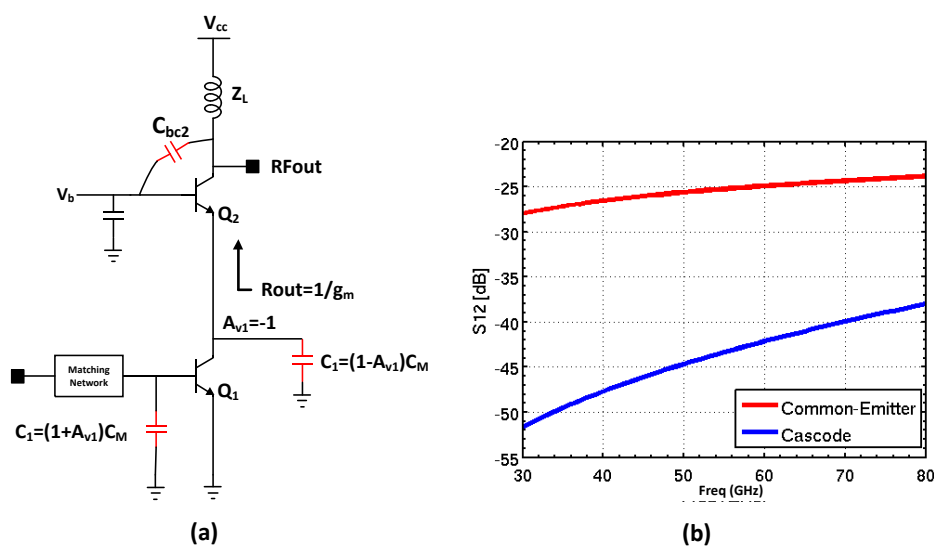


Fig. 3.8 (a) Miller effect in cascode and (b) the plot showing reverse isolation for CE and cascode

Another technique employed for reducing the Miller effect is cascoding the CE stage with a CB transistor, which results in unity voltage gain for the input transistor. Thus, cascoding reduces the dependence of the CE transistor's input impedance on gain, which helps achieving input matching, better reverse isolation due to absence of miller capacitance in the CB transistor. Fig. 3.8 (b) shows the plot of S_{12} against frequency for the single CE stage and cascode topology showing considerable improvement in the reverse isolation.

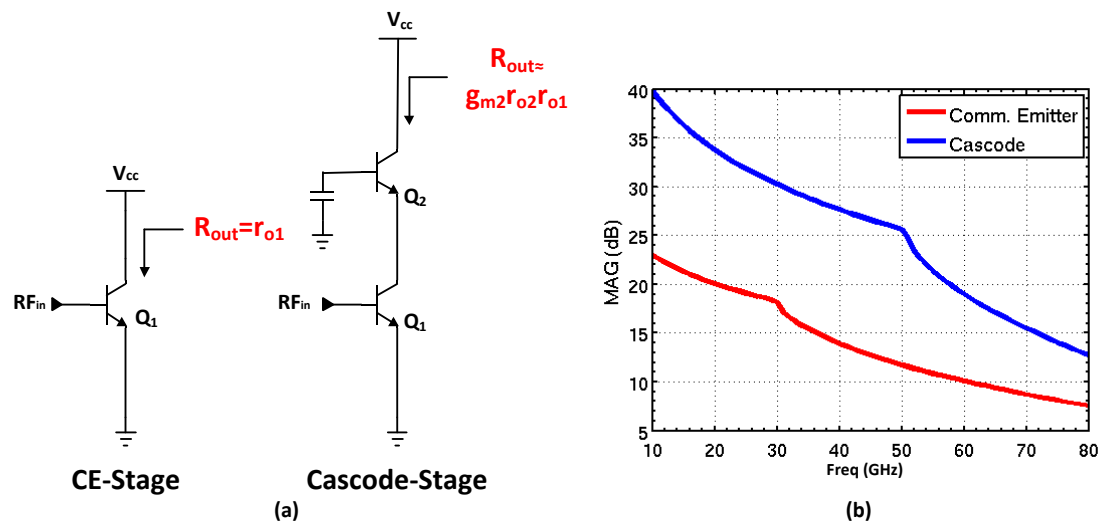


Fig. 3.9 (a) R_{out} and (b) maximum available gain (MAG) plot for CE and cascode stage

The increased gain at higher frequencies is attributed to its increased output impedance (R_{out}) by a factor of the intrinsic gain of the transistor (Q_2) due to the presence of the degenerated output resistance (r_{o1}) of Q_1 [3.8] (see Fig. 3.9 (a)). Fig. 3.9 (b) shows the maximum available gain (MAG) plot for common emitter and cascode stages of the bipolar transistor showing the increase in the gain of the cascode stage due to the increased R_{out} .

3.4 LNA Design Procedure for High Impedance Load

The design procedure for the LNA driving an high impedance load is presented here. This can represent the LNA in its final application environment i.e., LNA followed by a square law detector. The detector, which will be presented in chapter 4, provides a high impedance ($\sim 400 \Omega$ at 60 GHz). First, the ideal components are used to explain the steps in the design procedure to obtain the required 2-stage LNA performance

specifications. Then, the layout parasitics and bondpads are included in order to account for their effect on the circuit performance and re-tune the circuit.

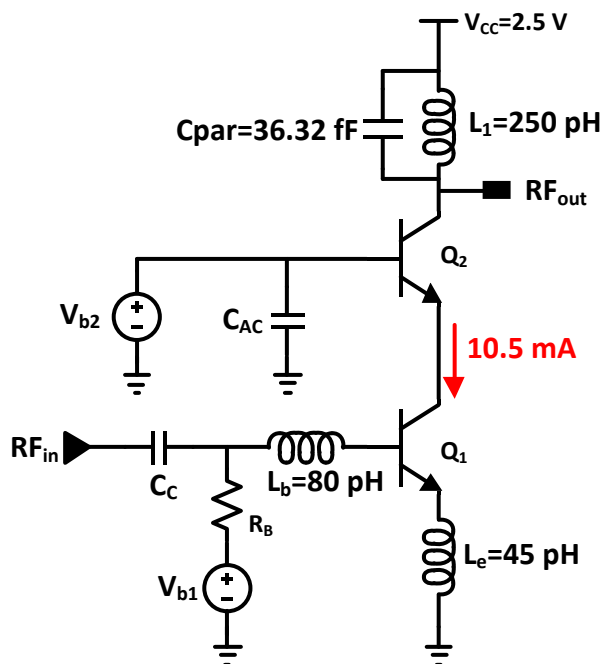


Fig. 3.10 Input stage cascode

3.4.1 Input Stage Design

Fig. 3.10 shows the input stage cascode of the 2-stage LNA. Firstly, biasing of the transistors of the two transistors is done in order for them to operate in the active region.

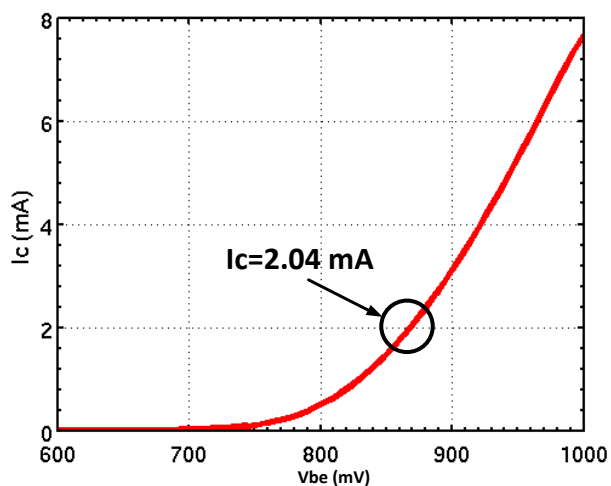


Fig. 3.11 I_C - V_{BE} plot for the input stage

Fig. 3.11 shows the I_C - V_{BE} curve of the input stage. The objective is to bias the stage close to peak f_T for maximum speed. From the f_T characteristics presented in Fig. 3.2 and from Fig. 3.11, biasing of the stage is set close to peak f_T at 2.049 mA with the transistors emitter lengths (L_e) of Q_1 and Q_2 set to minimum at 1 μm , following the analysis from Figs. 3.3 and 3.5.

Noise Figure

The next step is to scale emitter length L_e to obtain the optimum noise figure at which the real part of source impedance (i.e., 50 Ω) is equal to the real part of the noise source impedance. Fig. 3.12(a) shows the noise figure for different L_e values. At 63 GHz, the optimum noise figure is reached at an emitter length of 5 μm where the real part of the optimum noise impedance is near 50 Ω source impedance, as shown in Fig. 3.12 (b). The value of the L_e for transistors Q_1 and Q_2 is fixed at $L_e=5 \mu\text{m}$ as increasing the emitter length further does not result in any improvement in the noise figure i.e., optimum length for which the minimum NF is obtained is 5 μm .

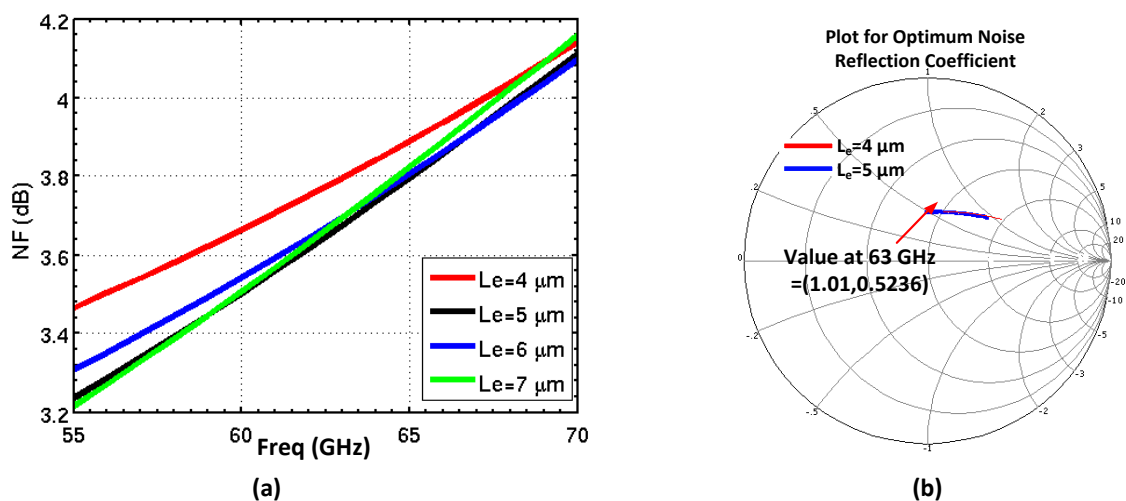


Fig. 3.12 (a) Noise figure and (b) corresponding noise reflection coefficient plot on smith chart for different L_e

Impedance and Noise Matching

The next step is to match the input impedance of the LNA. Simultaneous impedance and noise match is employed with inductors at emitter (L_E) and base (L_B) of the input CE transistor [3.9]. The value of L_E is set to match the real part of the input to 50 Ω s

and L_B is used to cancel the imaginary part of the input impedance at the frequency of interest.

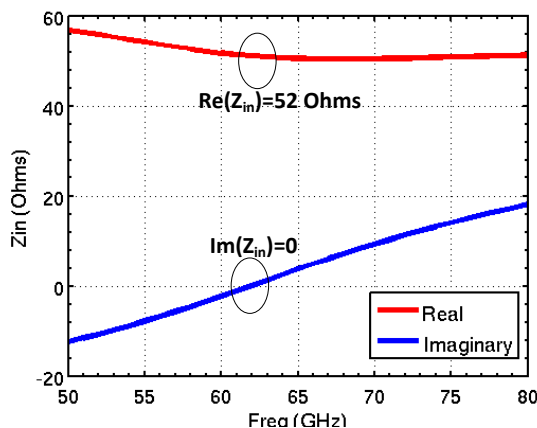


Fig. 3.13 Input impedance of the LNA after impedance matching

Fig. 3.13 shows the plot for the input impedance of the LNA showing the real part of the input impedance as 52Ω and that of the imaginary set to zero at 63 GHz.

Input Stage Gain

The final step in the procedure is to achieve a high gain of the single stage LNA by using an inductive load at the cascode output node. The inductive load resonates parasitic capacitance at the collector node of Q_2 (see Fig. 3.10). Using an ideal inductor, a value of 250 pH is chosen to maximize the gain with a band pass response.

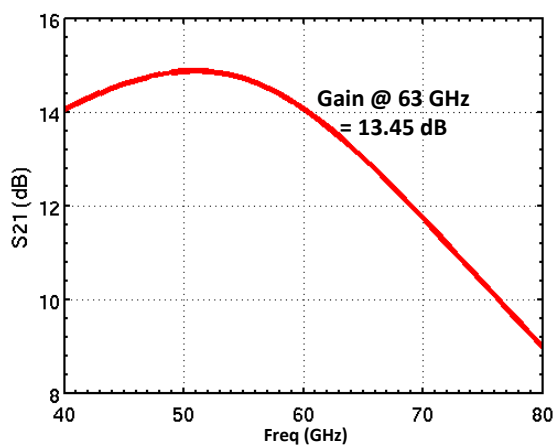


Fig. 3.14 Gain plot for the input stage

Fig. 3.14 shows the gain (S_{21}) obtained for the first stage. It is important to note that the resulting gain is obtained, given a fixed I_C (and g_m) thus fixing the noise figure. The idea is to maximize the gain at the desired frequency. In order to do this, the value of the load inductor can be increased. However, doing so would shift the gain at the desired frequency (at 63 GHz) to lower values.

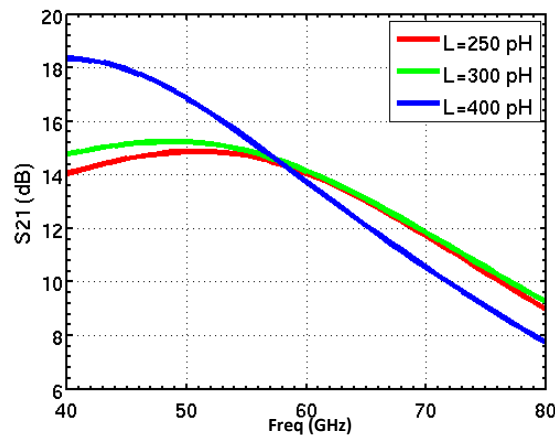


Fig. 3.15 Gain variation with the load inductance

Fig. 3.15 shows the effect of increasing the load inductor value on gain. The peak gain shifts to lower frequencies with increase in inductor value and the gain at 63 GHz gets reduced as well since the roll-off occurs for lower gain values. Further, a different capacitance at the output node to get the desired gain would require to change the transistor size which, in turn would change the noise figure of the stage.

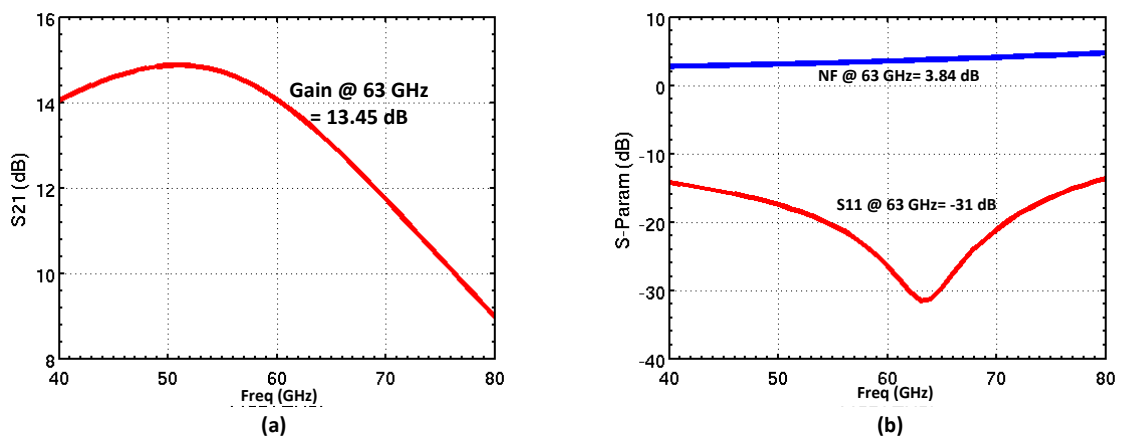


Fig. 3.16 Overall input stage performance results

Fig. 3.16 summarizes the performance results of the input stage. The next step is the design of the second stage cascode to achieve higher gain and reach the design specifications.

3.4.2 Output Stage Design

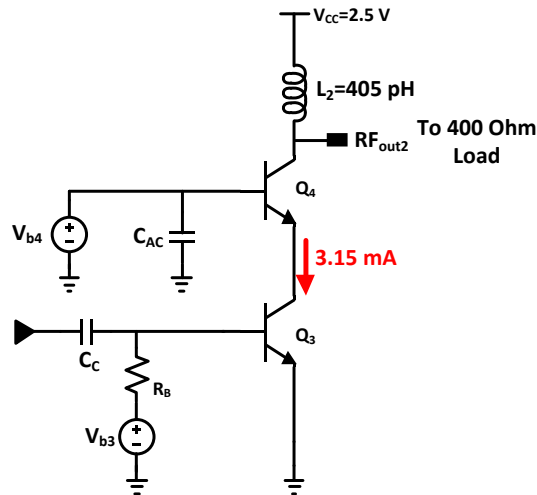


Fig. 3.17 Output stage cascode

Fig. 3.17 shows the idealized schematic for the 2nd cascode stage. The values of L_c for the transistors Q_3 and Q_4 are chosen in order to bias the stage at peak f_T i.e., at 3.15 mA, which is similar to the biasing of the input stage (which is biased at 10.5 mA for $L_c=5 \mu\text{m}$). Further, since the LNA will drive the square law detector's input impedance ($\sim 400 \Omega$), the output stage is designed for driving a high load impedance (see chapter 4). The parasitic capacitance at the collector node of Q_4 is resonated out with the load inductor L_2 to maximize the gain.

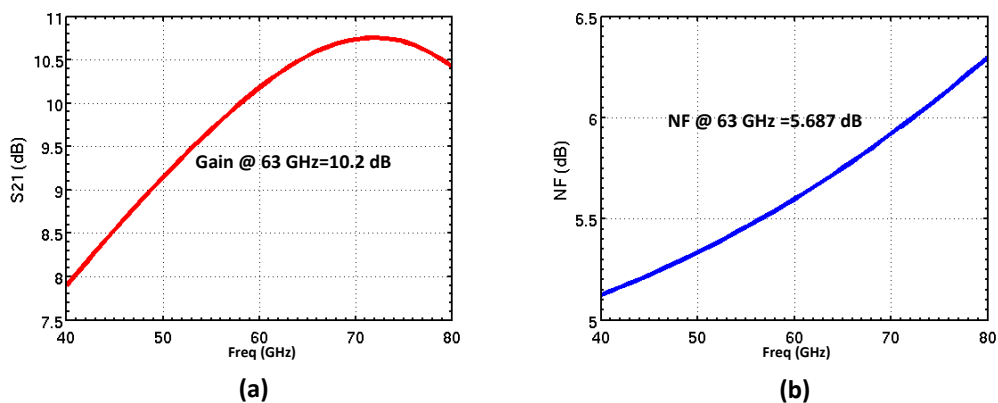


Fig. 3.18 (a) Gain and (b) noise figure plot for the output stage

The stage is not optimized for minimum noise performance and is solely designed as an additional gain stage. Figs. 3.18(a) and 3.18(b) shows the plot for gain and noise figure of the output stage, respectively. The gain obtained from the input stage can thus be combined with this output stage to form an overall band pass response i.e., using 2 LC-resonators to form band pass characteristics [3.8]. The noise contribution is suppressed by the gain obtained in the input stage (as discussed in chapter 2 with Friis' relation for noise factor). From equation (2.10), we rewrite the equation for 2-stage as

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} \quad (3.3)$$

The noise figure of the 2nd stage is suppressed by the 13.45 dB obtained in the second stage gain of the 1st stage i.e., the noise contribution of the overall stage from (3.3), calculated using the noise figure and gain values of the input stage and the noise figure of the 2nd stage (which 5.687 dB) comes out to be 4.09 dB. The next step is to combine input and output stages to realize a 2-stage cascode LNA.

3.4.3 Combined Input-Output Cascode Stage Performance

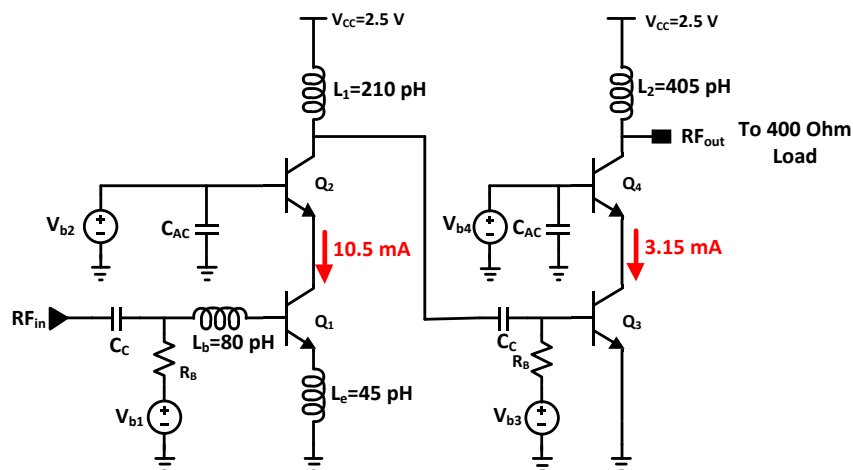


Fig. 3.19 2-Stage cascode LNA realized by combining input and output stages

Fig. 3.19 shows the 2-stage cascode LNA realized by ac-coupling the input and output stage cascode LNAs presented in sections 3.3.1 and 3.3.2, respectively.

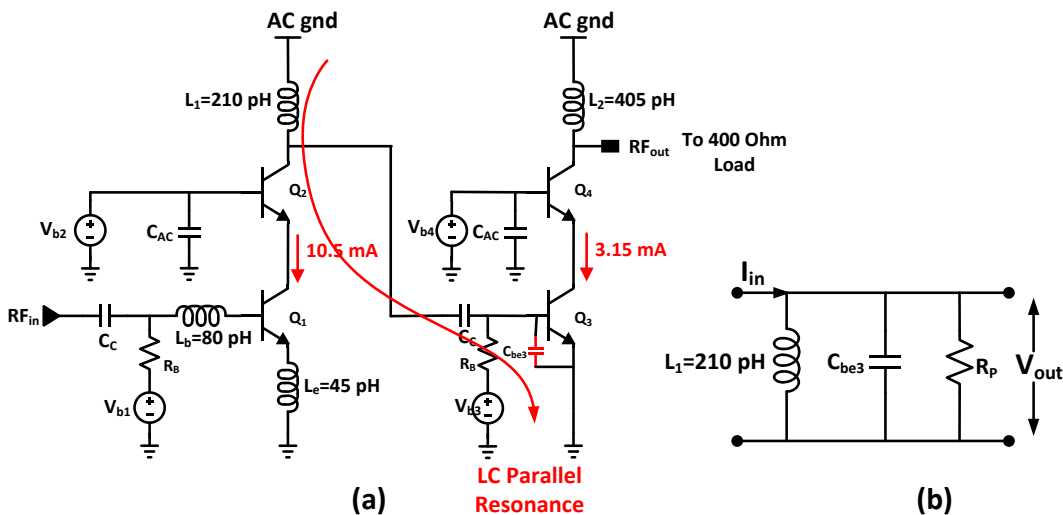


Fig. 3.20 (a) Parallel resonance L and C at the interstage node and (b) corresponding equivalent LC tank circuit

The voltage swing at the inter-stage node of the two stages is maximized by resonating the load inductance (L_1) of the input stage with the base-emitter capacitance (C_{be3}) of the input transistor of the second stage. Towards this end, the value L_1 is retuned from 250 pF (as used in the input stage) to 210 pF. Fig. 3.20(a) shows the scenario in which both L_1 and C_{be3} are connected to the ac ground, thus forming parallel LC tank which is used to maximize the voltage swing at the interstage node through a high quality factor (Q) of the tank . Fig. 3.10 (b) shows the equivalent LC tank circuit showing the voltage swing V_{out} , showing dependence on the tank Q [3.3].

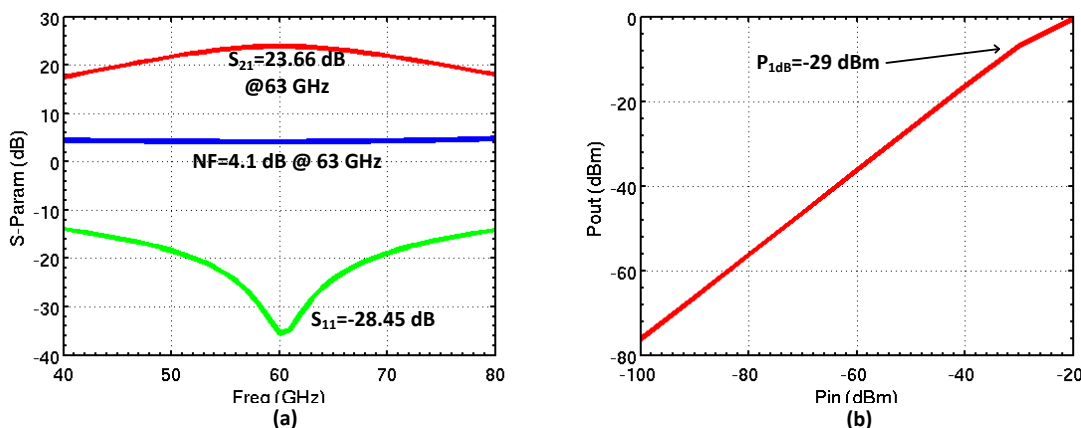


Fig. 3.20 2-stage cascode LNA performance results

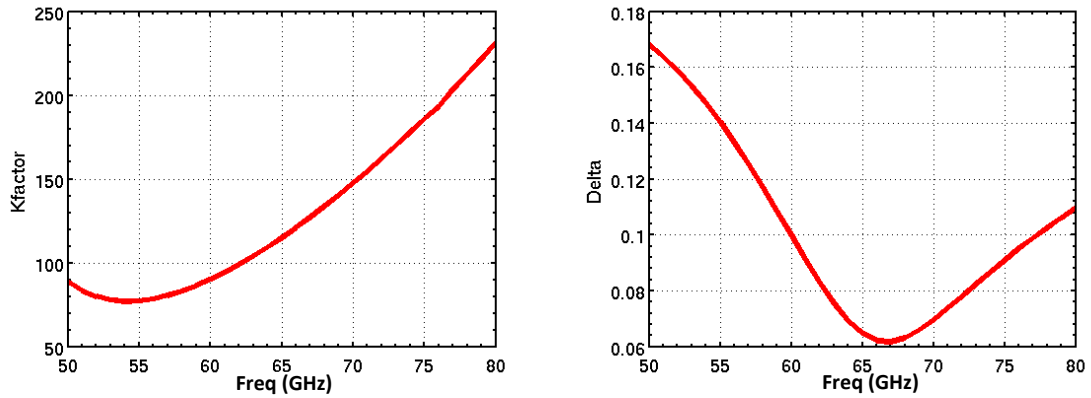


Fig. 3.21 Overall (a) K-Factor and (b) delta

Figs. 3.21 and 3.22 summarize the simulation results for the 2-stage LNA showing overall amplifier performance.

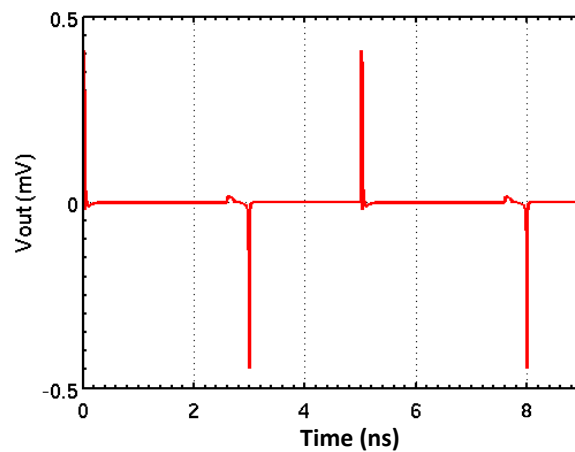


Fig. 3.22 Step response of the 2-stage LNA

Fig. 3.22 shows the step response of the amplifier. It can be inferred that the amplifier settles to its final value without any ringing in its response. Fig. 3.21 shows the simulation results for the LNA designed with ideal passive components. The transistor sizes used for the design are shown in Table 3.1.

Table 3.2 Final transistor sizes for the 2-stage cascode LNA

| Transistor | L_e (μm) | W_e (μm) |
|----------------|-------------------------|-------------------------|
| Q ₁ | 5 | 0.4 |
| Q ₂ | 5 | 0.4 |
| Q ₃ | 1.5 | 0.4 |
| Q ₄ | 1.5 | 0.4 |

3.4.4 Layout Optimization of Cascode Stage

The LNA designed in the previous section is idealized at the schematic level and does not include the effect of bondpads and layout parasitics. It is important at this point to review some of the important layout parasitics which affects the LNA performance at millimeter wave frequencies.

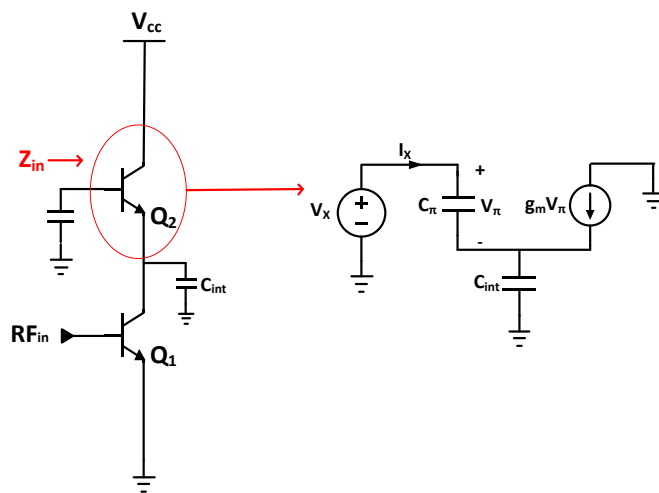


Fig. 3.23 Cascode stage showing the CB transistor's Z_{in} as seen from base node

Fig. 3.23 shows the cascode configuration with the input impedance Z_{in} (as seen from the base of Q_2). The small signal equivalent of Q_2 shown on the right side can be used to compute the expression for Z_{in} , which is given by [3.9]

$$Z_{IN} = \frac{1}{C_{\pi}} + \frac{1}{C_{int}} - \frac{g_m}{\omega^2 C_{\pi} C_{int}} \quad (3.4)$$

where C_{int} is the interstage parasitic capacitance, C_{π} is the base-emitter capacitance of Q_2 and g_m is the Q_2 transconductance. The third argument in (3.3) suggests that impedance seen from the Q_2 base can become negative and lead to oscillatory conditions in the amplifier.

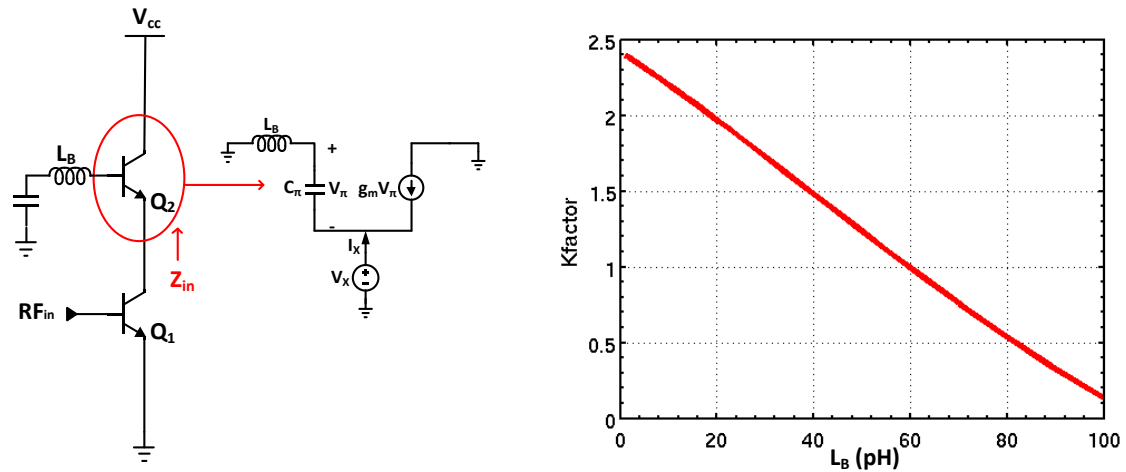


Fig. 3.24 Cascode stage showing the CB transistor's Z_{in} from emitter node and its K-factor

Similarly, Fig. 3.24 shows the input impedance looking into the emitter node of Q_2 . The input impedance sees a parasitic inductance (from the interconnect leads) transformed into a negative impedance [3.10]. The parasitic inductance L_B introduces negative resistance (or oscillatory conditions), again leading to stability issues. The influence of these parasitics underlines the importance of including their effects at the schematic level itself. Also shown in Fig. 3.24 is the value at which the K-factor of the cascode stage goes below 1 i.e., L_B beyond 60 pH, thus indicating oscillatory conditions. To this end, modelling of the parasitics is required using standard verification tools for parasitic extraction as well EM verification of the interconnects at millimeter wave frequencies. First, the layout of the single cascode stage is done followed by its physical verification using Cadence Assura™.

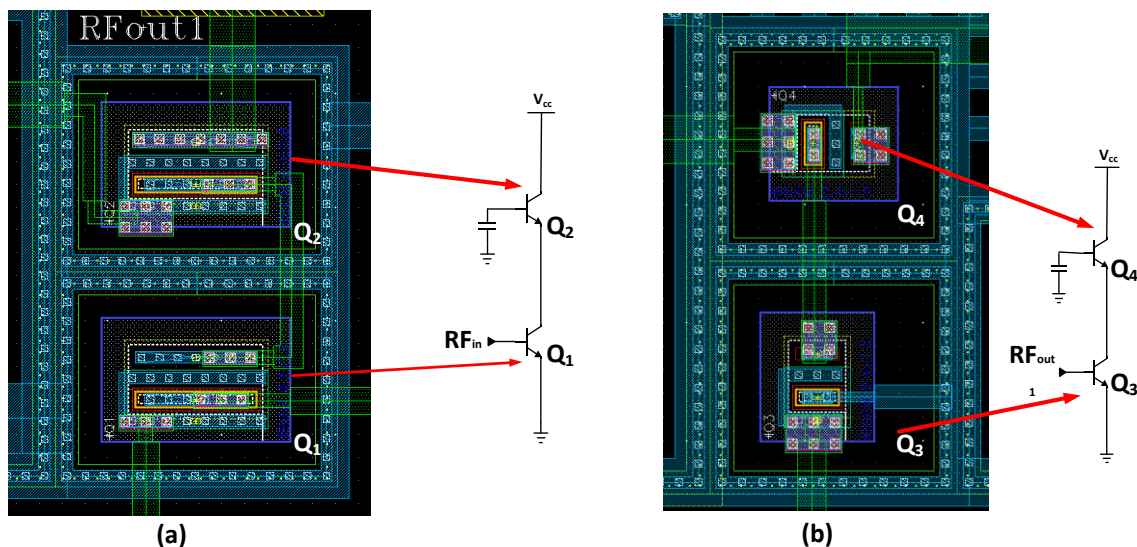


Fig. 3.25 (a) Input stage and (b) output stage cascode layout

Figs. 3.25 (a) and 3.25 (b) shows the layout of the input and output cascode stages, respectively with their corresponding schematic. Secondly, a post layout parasitic RC extraction of the cascode layout is performed using Cadence Assura™.

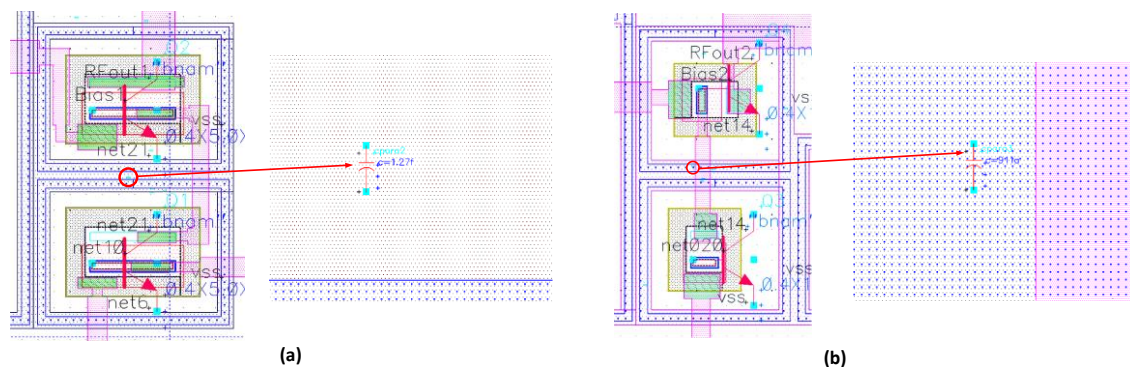


Fig. 3.26 (a) Input stage and (b) output stage parasitic extracted view

Figs. 3.26(a) 3.26(b) shows the parasitic extracted view of the input and output cascode stages and their corresponding parasitic capacitances. Thirdly, inductive parasitics of the interconnects are estimated using Agilent Momentum™ electromagnetic (EM) simulator. The Momentum™ EM simulator solves Maxwell's equations using the method of moments numerical method and the inductance values are extracted using s-parameters simulation data of the interconnects. To this end, a back end of the metal line (BEOL) stack of the QUBIC4xi technology is created in Momentum™.

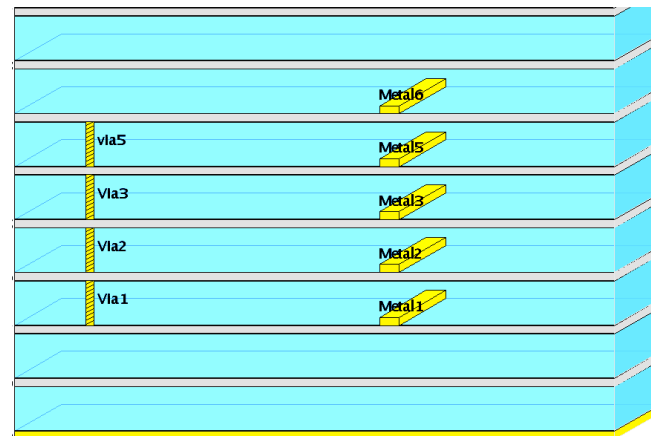


Fig. 3.27 BEOL of QUBIC4xi technology in Momentum

Fig. 3.27 shows the QUBIC4xi BEOL stack used for extracting crucial interconnect parasitics (such as those discussed in 3.3.1) for the schematic level as well as during the final layout stage (chapter 5). From the EM simulations, an estimated inductance value $1\text{pH}/\mu\text{m}$ is obtained for metal 3 line of length $10\ \mu\text{m}$ and width $1\ \mu\text{m}$.

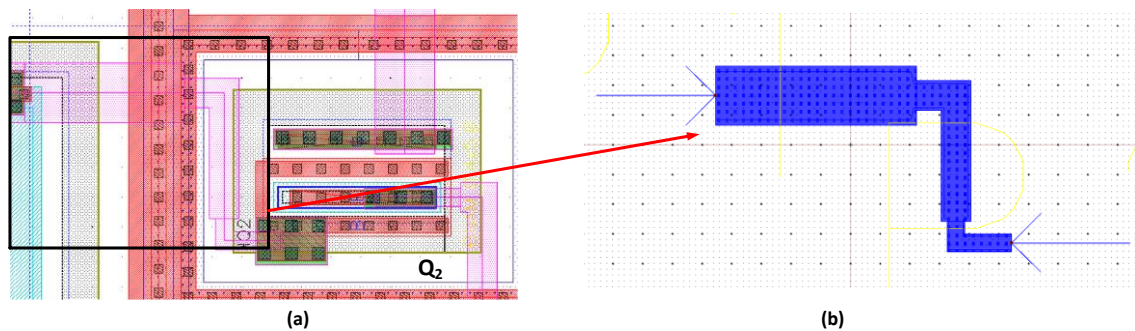


Fig. 3.28 A layout example showing (a) cascode layout from cadence and (b) extracted layout in Momentum

Fig. 3.28 shows an example of the interconnect at the base of the CB transistor and its corresponding extracted layout in Momentum™ for EM verification. Finally, the extracted parasitics are annotated back to the circuit schematic shown in Fig. 3.19.

3.4.5 LNA with Parasitic Back Annotation

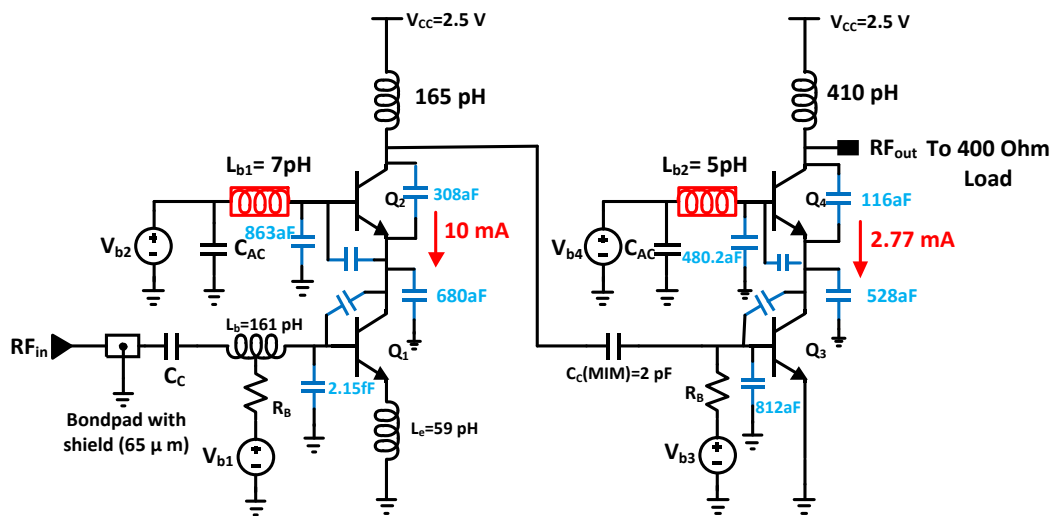


Fig. 3.29 LNA schematic with layout parasitics annotated

Fig. 3.29 shows the LNA circuit schematic annotated with parasitics in which the parasitic capacitances and inductances have been extracted using Momentum™. The ideal load and matching inductors were replaced with those available in the QUBIC4xi library. The inductors (L_B and L_E) were retuned and the bondpad capacitance from the technology library was also included as part of the matching network.

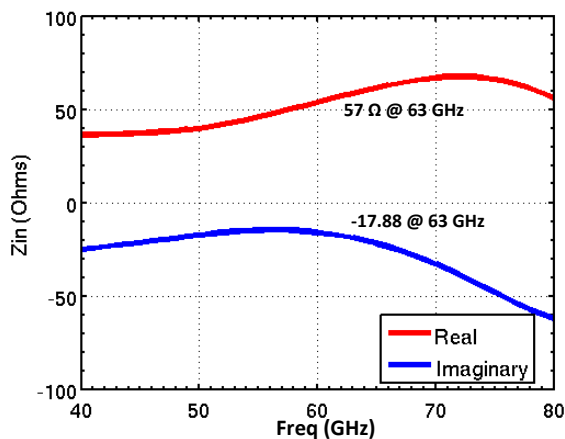


Fig. 3.30 Input impedance plot with real and imaginary parts

Fig. 3.30 shows the input impedance plot after the inclusion of layout parasitics, input bondpad and library inductors at the input of the LNA. The real part of the impedance is close to 50 Ω source impedance at 63 GHz. However, the imaginary part of the impedance is not at zero due to the extracted parasitic capacitance of the transistor,

library inductor and the capacitance from the bondpad is 31fF for a pad size of 65 μm . Therefore, the resulting S_{11} has now changed to -14.48 dB at 63 GHz (see Fig. 3.22).

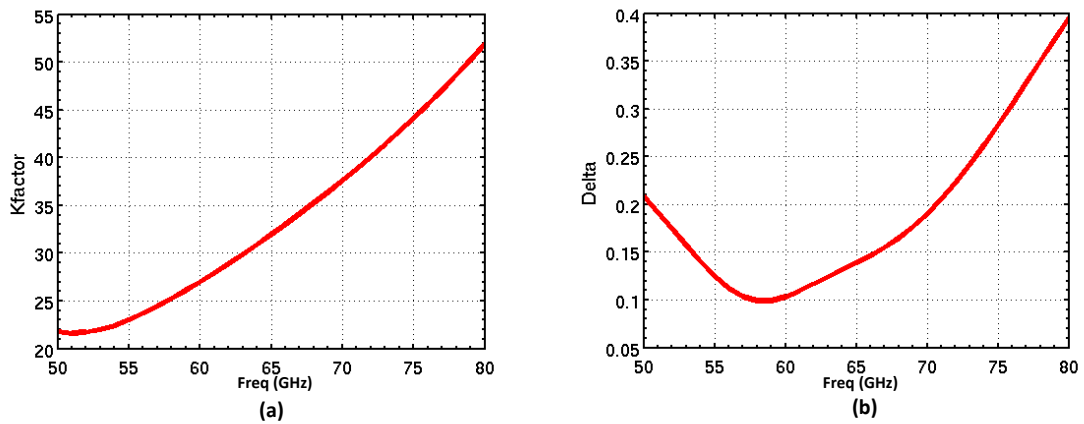


Fig. 3.31 Overall (a) K-Factor and (b) delta for the parasitic annotated LNA

Figs. 3.31(a) and 3.31(b) shows the overall K-factor and Delta which is around 29.5, at 63 GHz and ranges from 27 to 32 for 6 GHz bandwidth (60 GHz-65 GHz), which shows the 2-stage amplifier is unconditionally stable within the bandwidth of interest.

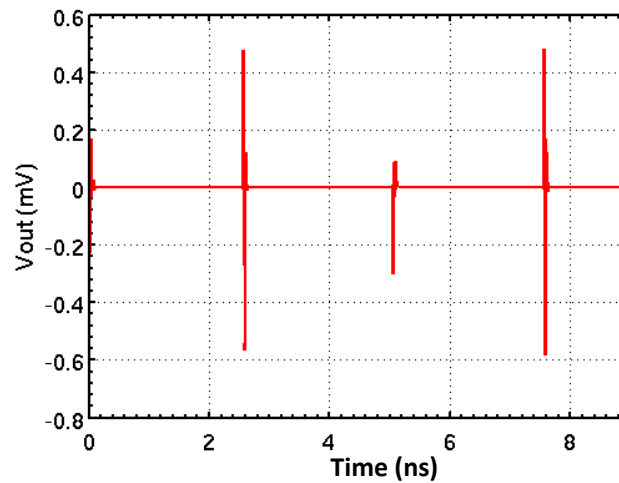


Fig. 3.32 Step response of parasitic annotated LNA

Fig. 3.32 shows the step response of the parasitic annotated LNA. It can be inferred that the amplifier settles to the final value without any ringing in its response.

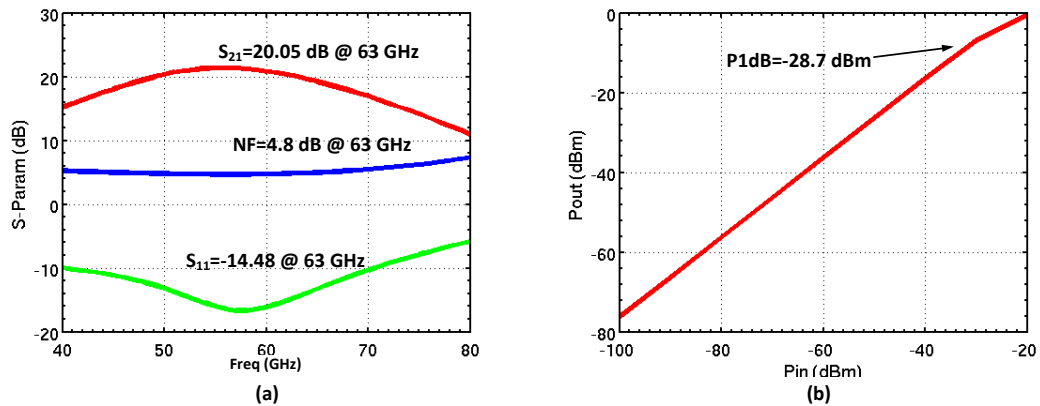


Fig. 3.33 Simulation results of the parasitic annotated LNA

Fig. 3.33 summarizes the simulation results of the parasitic annotated LNA in shown in Fig. 3.29. The inclusion of layout parasitics and bondpads in the schematic gives thus gives the idea of the shift in specifications the designer can expect before going to the final layout stage. Hence, this design procedure proves crucial in the final stages of circuit design and may reduce unnecessary iterations since some important parasitics influencing noise and stability have already been accounted for at this stage of the design.

3.5 LNA Design with Tapped Capacitive Transformer Output Match

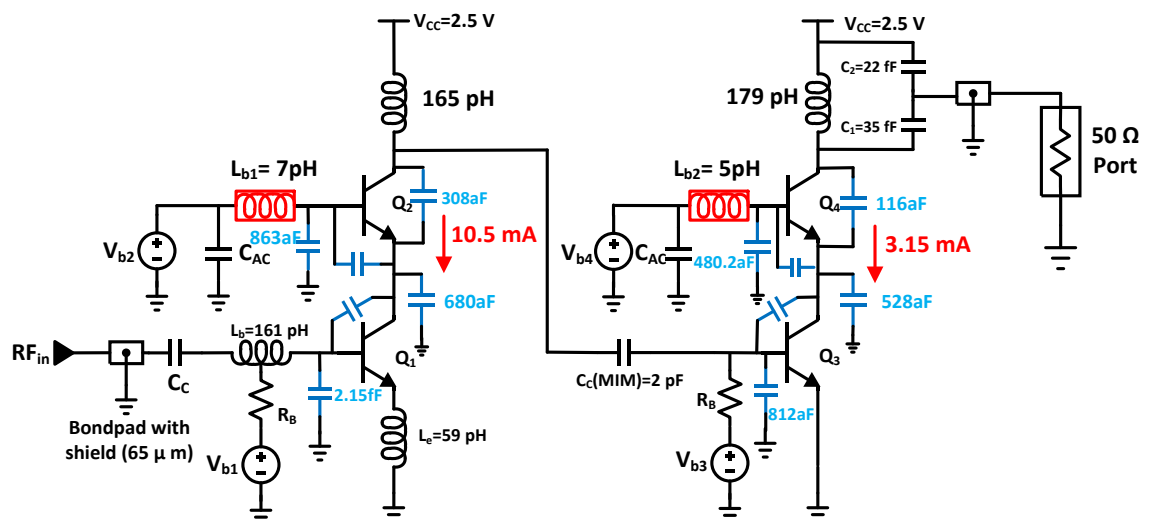


Fig. 3.34 LNA with Tapped Capacitive Transformer

Fig. 3.34 shows the LNA designed for an output impedance of 50Ω using a tapped capacitive transformer. The tapped capacitive transformer is chosen for its easy implementation in the sense that it simultaneously allows resonant tuning and impedance transformation [3.11]. Further, it is easy to implement from a layout perspective compared to compared to T-matching and π -matching network since additional inductors occupy more chip area.

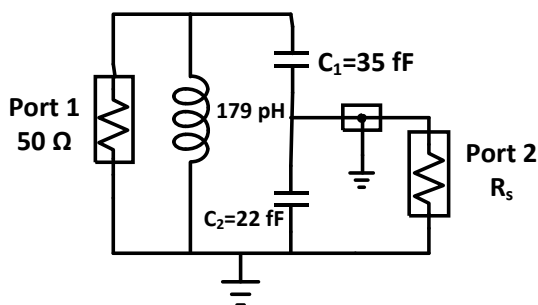


Fig. 3.35 Simulation results of the parasitic annotated LNA

Fig. 3.35 shows the s-parameter set up for the matching network. The impedance looking into the port 2, which is equivalently the impedance seen by the 50Ω port at the LNA output (Fig. 3.33) is determined by the ratio of the capacitance C_1 and C_2 , given by [3.12]

$$R'_S = R_S(1 + C_2/C_1)^2 \quad (3.5)$$

where R_S is 50Ω . Thus, a high impedance is seen by the LNA output node which can be set by choosing the value of C_1 and C_2 appropriately. The value of $C_1=35$ fF and $C_2=22$ fF is used in (3.5) and results in the R'_S value of 133Ω .

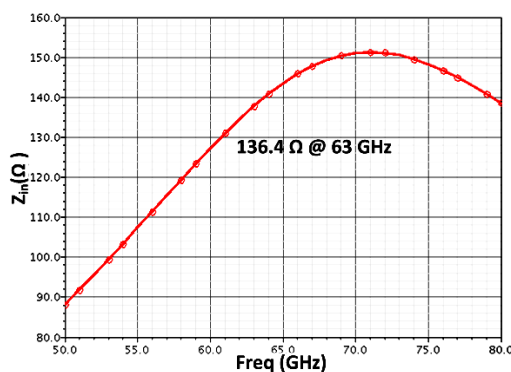


Fig. 3.36 Plot for Z_{in} as a function of frequency

Fig. 3.36 shows a the plot of Z_{IN} , i.e., impedance showing close approximation with the calculated value using (3.5).

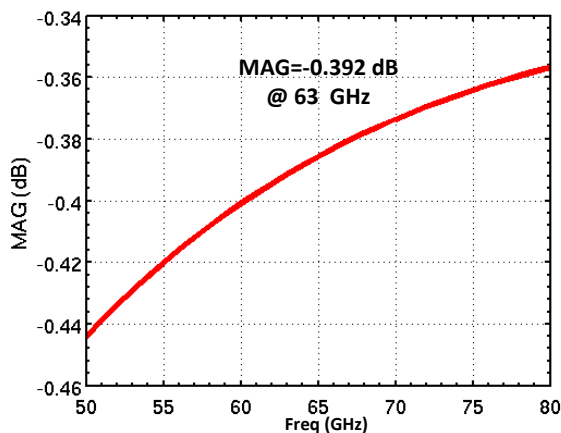


Fig. 3.37 MAG of the matching network against frequency

It is instructive to show the reduction of gain for the 63 GHz LNA due to the use of this passive divider at the LNA output. Fig. 3.37 shows the MAG of the matching network which was simulated as shown in Fig. 3.35. The loss incurred by this matching network is -0.392 dB and the LNA gain must reduce by the same amount as well from the gain obtained and section 3.3 for the LNA driving the 400 Ω impedance. Further, the load inductor of the output is optimized for matching with the capacitive divider, thus retuned value of 179 pH (see Fig. 3.34).

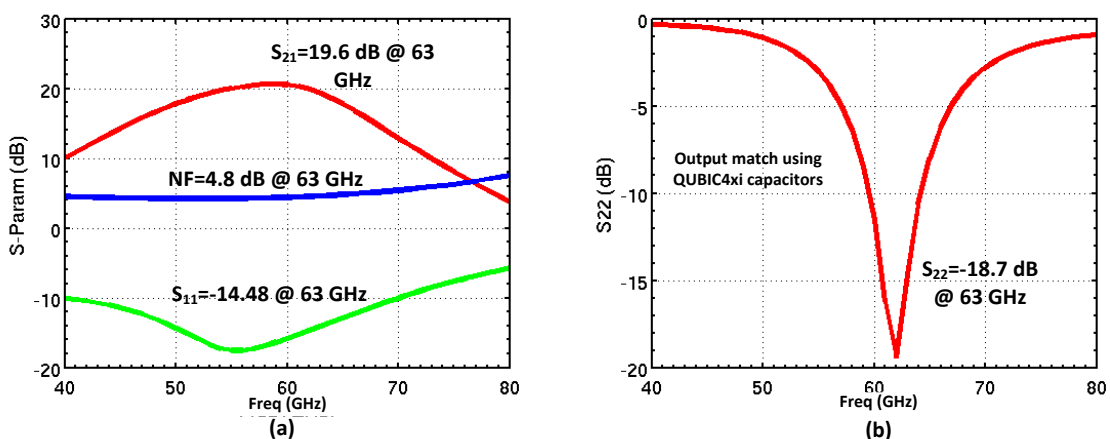


Fig. 3.38 Simulation results of LNA with tapped capacitance output match

Fig. 3.38 shows the final simulation results of the LNA. As expected, the tapped capacitance match reduces the LNA gain by 0.392 dB (losses from the matching network, see Fig. 3.36) to 19.6 dB (shown in Fig. 3.26(a)). Fig.3.37 (b) shows the output match of the LNA with its $S_{22}=-18.7$ dB at 63 GHz, achieved using QUBIC4xi library capacitors (C_1 and C_2).

3.5 Conclusions

The design procedure for the 63 GHz LNA was presented. Towards this end, two amplifiers were designed. The first LNA design drives a 400 Ω impedance and second LNA is designed with its output matched to 50 Ω . A summary of specifications achieved is provided in Table 3.3.

Table 3.3 63 GHz LNA performance comparison

| Specifications | LNA with 400 Ω load | LNA with Output Match |
|-----------------------------|--|------------------------------|
| Gain- S_{21} (dB) | 20.55 | 19.6 |
| Noise Figure (NF) | 4.8 | 4.8 |
| S_{11} (dB) | -14.48 | -14.48 |
| S_{22} (dB) | NA | -18.7 |
| Gain variation over BW (dB) | 1 | 1.2 |
| NF variation over BW (dB) | 0.39 | 0.39 |
| Supply voltage (V) | 2.5 | 2.5 |
| DC power consumption (mW) | 34.65 | 34.65 |

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Chapter 4

Design of Square Law Detector

This chapter presents the design of square law detector using the bipolar transistor configurations namely, common-emitter (CE), emitter follower (CC), common-base (CB) and cascode topologies. A summary of each detector's performance is provided at the end of the chapter.

4.1 Square Law Detection

The square law detector implements the function in which output DC voltage is proportional to the input power, given by

$$V_{out,DC} = KV_{IN}^2 \quad (4.1)$$

The collector current I_C of the transistor can be written as

$$I_C = I_S \exp\left(\frac{V_{IN}}{V_T}\right) \quad (4.2)$$

(4.2) can be expanded by Taylor series expansion (assuming a sinusoidal excitation of $V_{IN} = A \sin \omega t$), given by

$$I_C = I_S \left[\left(1 + \frac{1}{4} \left(\frac{A}{V_T}\right)^2\right) + \left(\frac{A}{V_T} + \frac{1}{8} \left(\frac{A}{V_T}\right)^3\right) \sin(\omega t) + \left(\frac{1}{4} \left(\frac{A}{V_T}\right)^2 - \frac{1}{48} \left(\frac{A}{V_T}\right)^4\right) \cos(2\omega t) \right] \quad (4.3)$$

From (4.3), the DC component of the signal current is given by

$$I_{C,DC} = I_S \left(1 + \frac{1}{4} \left(\frac{A}{V_T}\right)^2\right) \quad (4.4)$$

(4.4) shows the second argument, which represents input power. The corresponding DC component of the output voltage can be obtained by the voltage drop across the resistor.

4.2 Common-Emitter Based Square Law Detector

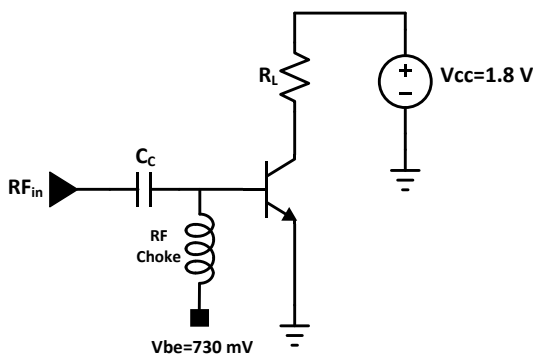


Fig. 4.1 Common-Emitter (CE) based square law detector

Fig. 4.1 shows the square law detector circuit employing a common-emitter configuration. The biasing of the transistor is the first important step in realizing the square law functionality as well as a high input impedance of the detector, which will be driven by the 63 GHz LNA designed in chapter 3, thus doing away with need for impedance matching at the LNA-detector interface. The input impedance of the CE transistor is given by [4.2]

$$Z_{\pi} = \frac{\beta}{g_m} \parallel \frac{1}{X_{C\pi}} \quad (4.5)$$

indicates that impedance is bias dependent and hence the biasing point needs to be chosen accordingly for the required detector input impedance needed (at the frequency of interest) and for the square law functionality. Increasing the bias current may result in transistor operation in the linear region than in the square law region.

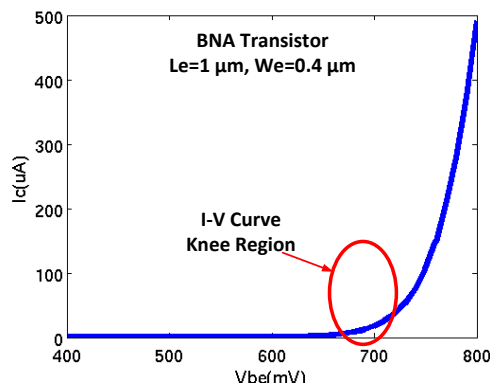


Fig. 4.2 I_C - V_{BE} characteristics for the CE-based detector

Fig. 4.2 shows the I_C - V_{BE} characteristics for the minimum-sized ($L_e=1 \mu\text{m}$, $W_e=0.4 \mu\text{m}$) BNA transistor. The transistor is biased in the exponential region of the characteristics (see Fig.4.2) at which the non-linearity of the transistor can be used to obtain an output signal proportional to input power [4.1] as explained by Equations (4.3) and (4.4).

4.2.1 Design

The performance characteristics are given by the DC responsivity \mathfrak{R} (Equation 1.1) and the noise equivalent power i.e., NEP (Equation 1.2). The DC responsivity depends on the value of the load resistance R_L and the size of the transistor. As the value of the load resistance is increased, the DC responsivity increases since the incremental voltage at the output node increases.

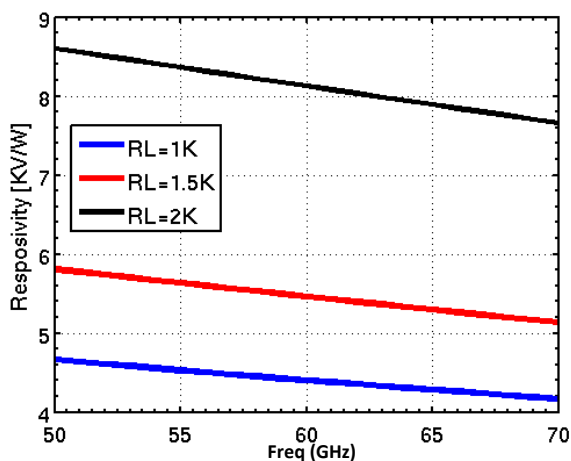


Fig. 4.3 CE transistor DC responsivity for different load resistor values

Fig. 4.3 shows the plot for DC responsivity of the CE transistor versus frequency for increasing values of the load resistor. However, the polysilicon resistors available exhibit $1/f$ noise and thermal noise [4.3] associated with it. Hence, increase in the load resistance increases the contribution of the resistor noise. Other options can be resistors made with metal lines available in the BEOL, which does not contain $1/f$ noise.

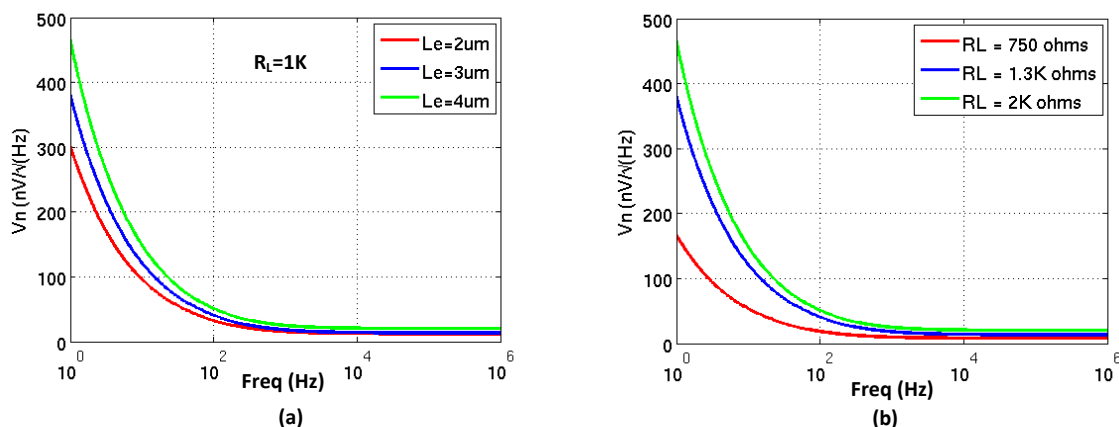


Fig. 4.4 (a) Output voltage noise for different values of L_e and (b) R_L

Fig. 4.4 shows the output noise voltage for different values of R_L . The integrated output noise voltage (noise integrated for an integration time of 100 ms) increases due to the thermal and flicker noise of the poly resistor used. Thus the NEP increases and offsets the improvement in \mathfrak{R} . Thus, the value of the load resistor needs to be chosen for optimizing \mathfrak{R} and NEP.

Another parameter of interest is the emitter length (L_e) of the transistor. The increase in the L_e of the bipolar transistor will increase the DC responsivity due to increase in the voltage at the output node, providing a similar improvement to that of increasing R_L . Moreover, increasing L_e will increase the output noise and due to an increase in the output noise current, the NEP increases. Therefore, a trade-off between the R_L , bias current (I_C) and L_e for the optimization of the detector performance characteristics exists.

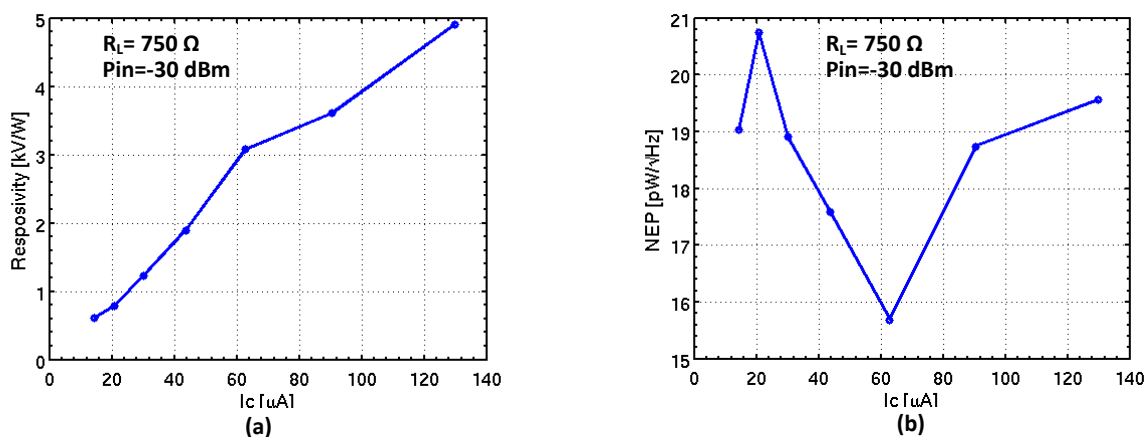


Fig. 4.5 Variation of (a) DC Responsivity and (b) NEP with the bias current

The simulations were performed using Cadence RF Spectre™ with a power level of -30 dBm for a 63 GHz input signal. Periodic steady state (PSS) option was used for analysing the DC output response across the frequency band and periodic noise (PNOISE) option was used for calculating the output noise voltage. All simulations were performed for an integration time (τ) of 100 ms.

As a starting point for choosing an optimum bias point, the detector is analysed with the R_L value of 750Ω and an input power of -30 dBm for its \mathfrak{R} and NEP variation with I_c . Figs. 4.5 (a) and 4.5 (b) shows the \mathfrak{R} and the NEP variations, respectively for increasing values of I_c . The responsivity linearly increases with I_c , as expected. On the other hand, the NEP of the circuit, depends on the thermal and $1/f$ noise contributions from R_L and the transistor current noise due to I_c . The NEP initially increases due to lower \mathfrak{R} at lower current levels, reaches a minimum and starts to increase at higher current levels (which is due to increase in the collector current thermal noise). This suggests that an optimum exists where a minimum NEP can be found with a corresponding \mathfrak{R} which can lower the NEP.

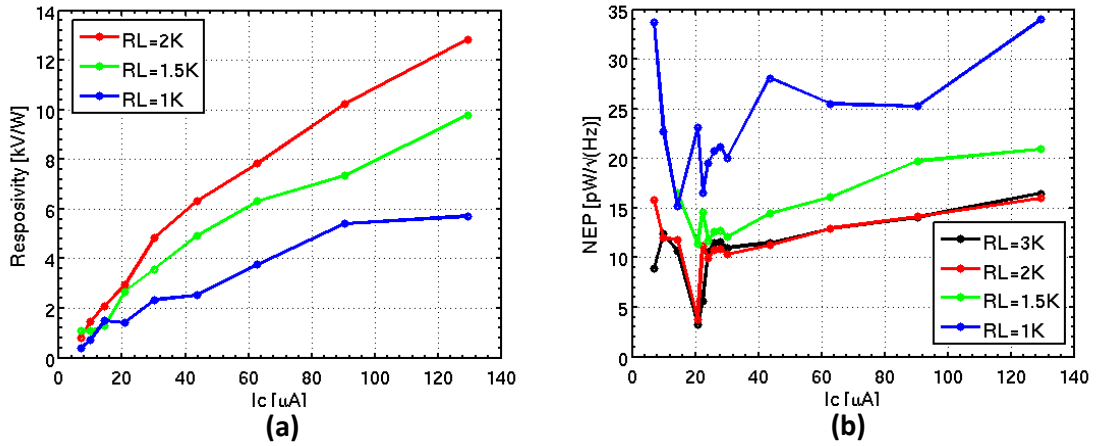


Fig. 4.6 (a) DC Responsivity and (b) NEP as a function of I_C for different R_L values

Fig. 4.6 (a) shows the variation of \mathfrak{R} as a function of the I_C for different values of R_L with a fixed L_e of $3\mu\text{m}$. An improvement in \mathfrak{R} can be seen as the value of R_L is increased. Fig. 4.7 (b) shows the NEP variation as function of I_C . The NEP is proportional to the noise contribution at V_{out} , which can be written as (ignoring $1/f$ noise) [4.1,4.3]

$$V_{out,n}^2 = 2qI_C + 4KTR_L \quad (4.6)$$

where the first argument of the (4.6) is the collector current shot noise and the second argument is the thermal noise from R_L . Equation 4.6 indicates that the $V_{out,n}$ increases with increasing R_L . However from Fig. 4.7 (b), it can be inferred that a higher R_L value results in a higher \mathfrak{R} which lowers the overall NEP. Beyond $R_L=2\text{ k}\Omega$ no further improvement in the NEP can be noted as the noise contribution of R_L increases with its increasing values.

Further, it can be seen from figure 4.6 that the transistor needs to be biased at I_C levels at which a \mathfrak{R} and low NEP can be obtained. However, I_C and L_e also affect the detector performance as shown in Figs. 4.4 and 4.5. Therefore, simulations are performed for arriving at the effect of different L_e values on the \mathfrak{R} and the NEP as I_C is varied.

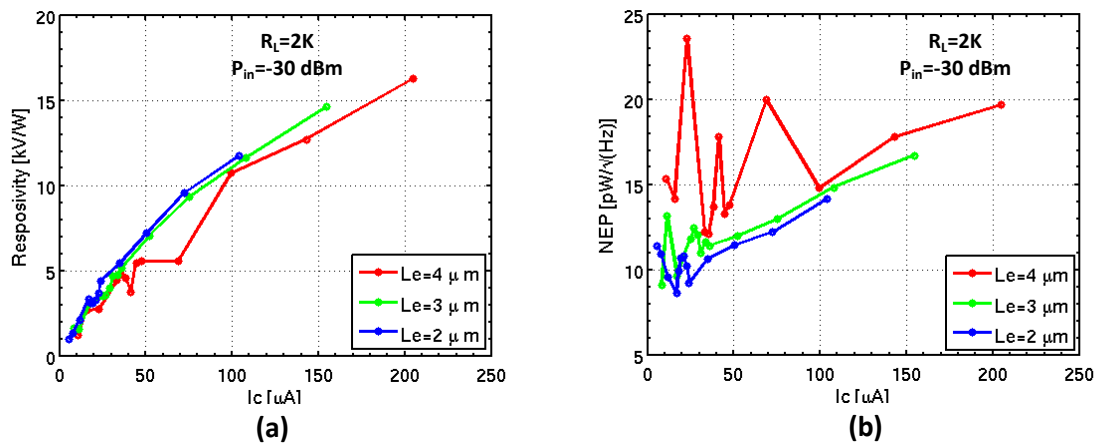


Fig. 4.7 7 (a) DC Responsivity and (b) NEP as a function of I_C for different R_L values

Figs. 4.7(a) and 4.7(b) shows the simulation results for the \mathfrak{R} and NEP, respectively for different L_e values. It can be inferred that for different L_e values, responsivity remains almost same for lower levels of I_C and increases for higher I_C values as L_e is increased. Fig. 4.7 (b) shows the red curve for $L_e = 4\ \mu\text{m}$ which shows an increase in the NEP at higher current levels. Based on this analysis, $R_L = 2\ \text{k}\Omega$ and $L_e = 3\ \mu\text{m}$ were chosen and the transistor was biased for $I_C = 85\ \mu\text{A}$.

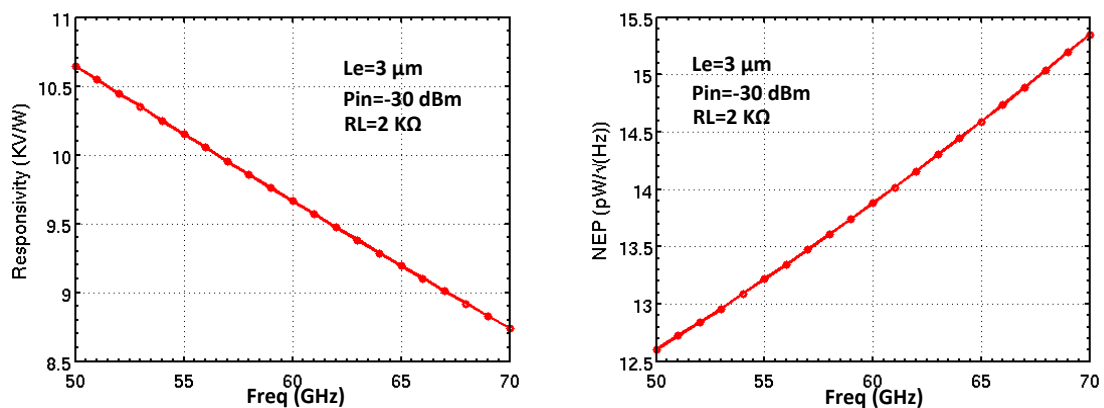


Fig. 4.8 (a) DC Responsivity and (b) NEP against frequency for $L_e = 3\ \mu\text{m}$ $R_L = 2\ \text{K}\Omega$

Figs. 4.8(a) and 4.8(b) shows the simulation results showing achieved responsivity of $9.6\ \text{KV/W}$ and NEP of $14.3\ \text{pW}/\sqrt{\text{Hz}}$.

4.3 Emitter Follower based Square Law Detector

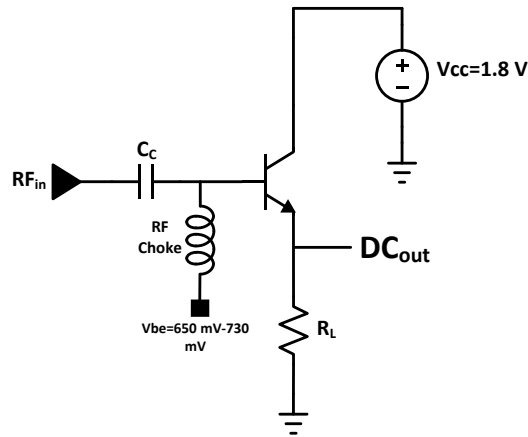


Fig. 4.9 Emitter follower based detector circuit

Fig. 4.9 shows the emitter follower based square law detector. The output is taken from the emitter node and hence the DC responsivity and NEP of the circuit depends on the load resistor R_L .

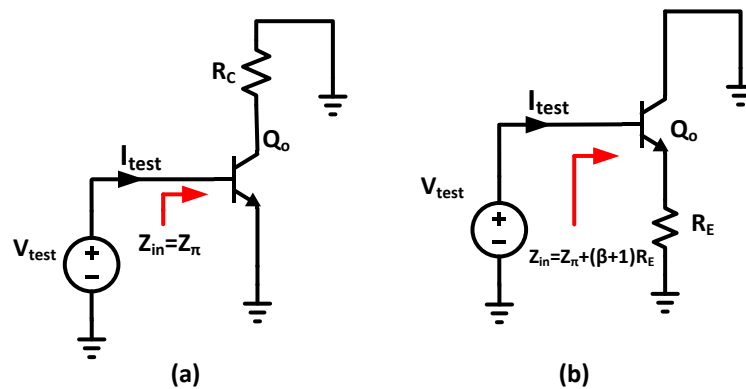


Fig. 4.10 Input impedance seen from base (a) for CE stage and (b) for emitter follower stage

It is instructive at this point to look at the input impedance of the detector. The input impedance of the CE transistor is given by Z_π . On the other hand, the input impedance of the emitter follower transistor increases by the factor $(\beta + 1)R_E$ due to the presence of the resistance at the emitter node.

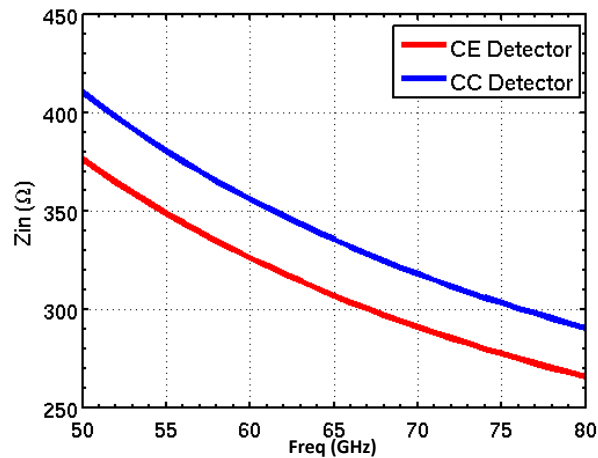


Fig. 4.11 Plot for input impedance for CE and Emitter Follower stage

Fig 4.11 shows the input impedance plot for the CE and the emitter follower transistors at the frequency of interest (at 63 GHz) which clearly shows an increase in the follower's input impedance. This indicates that the input impedance is now coupled with detector's DC responsivity and the NEP. Hence, any change in the load resistance to set the input impedance changes the detector's performance, thus making it difficult to adjust the required impedance (to be driven by the preceding LNA stage).

4.3.1 Design

The detector performance trade-offs are similar to that of the CE stage presented in section 4.1 i.e., DC responsivity depends on the values of I_C , L_e and R_L and so does the NEP. The responsivity (and hence the NEP) of the detector circuit needs requires an $R_L (=750 \Omega)$ value and transistor size ($L_e=2 \mu\text{m}$) for benchmarking its performance with the CE-based detector. The simulation set up is also similar to that of CE detector stage i.e., $P_{in} = -30 \text{ dBm}$ for a 63 GHz input signal using PSS and PNOISE simulation options with an integration time of 100 ms.

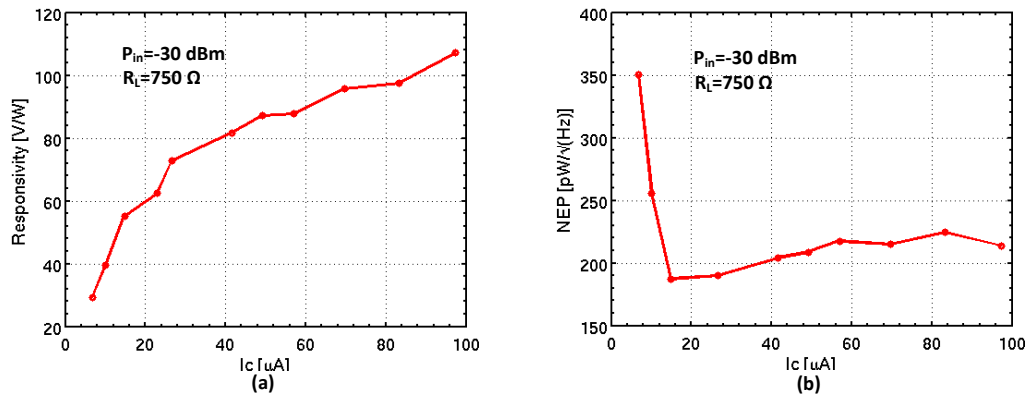


Fig. 4.12 Plot of (a) responsivity and (b) NEP for the emitter follower detector

Figs. 4.12 (a) and 4.12 (b) show the DC responsivity and NEP variation as a function of current. When compared to CE based detector, it shows poor DC responsivity and NEP. These reduced performances are due to the fact that the effective load impedance at the output node is dominated by $1/g_m$, which appears in parallel with R_L (see Fig. 4.13).

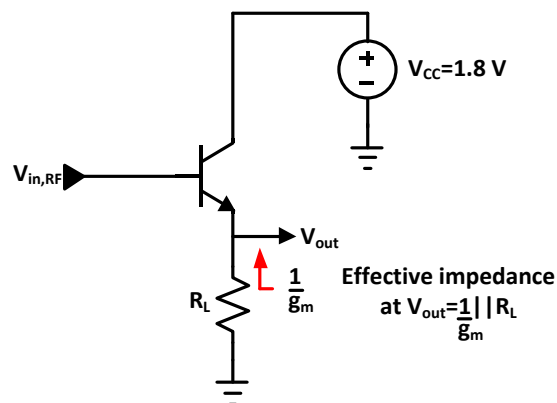


Fig. 4.13 Effective load impedance at the output node

For instance, a collector current of $125 \mu\text{A}$ translates to a $1/g_m$ value of 208Ω and hence significantly decreases the intended R_L of 750Ω resistor. Hence the responsivity is reduced to the transconductance that the transistor exhibits at mm-wave frequencies depends on $1/g_m$ and hence the increase in the NEP. The analysis detailed in the design of CE-based detector was done for the emitter-follower based detector as well in order to reach an optimal performance level.

The simulation set up for the analysis is the same as mentioned in section 4.1.1. An R_L of 500Ω and a bias current of $25 \mu\text{A}$ and minimum transistor size ($W_e=0.4 \mu\text{m}$, $L_e=1 \mu\text{m}$) were chosen in order to mitigate the influence of the $1/g_m$.

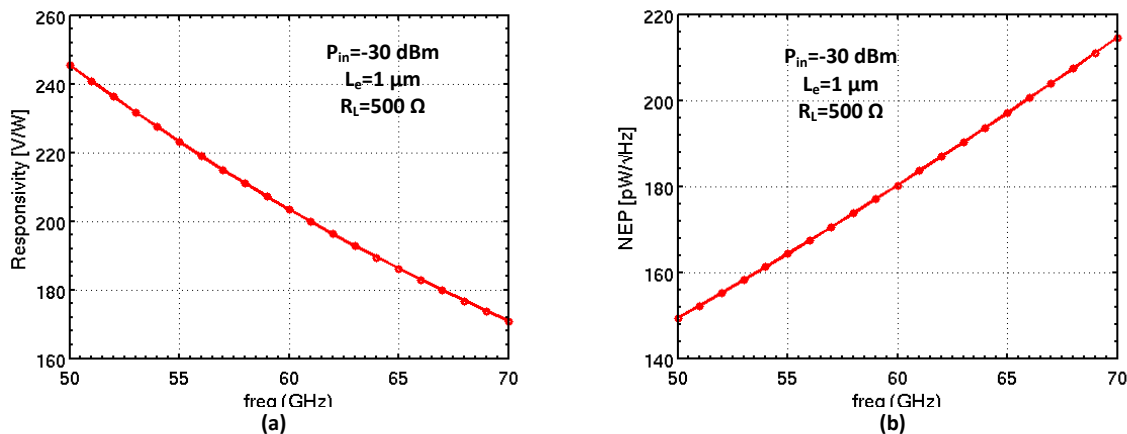


Fig. 4.14 (a) DC responsivity and (b) NEP against frequency for Emitter-Follower detector

Figs. 4.14 (a) and the 4.14 (b) shows the achieved \mathfrak{R} of 192 V/W and NEP of $185 \text{ pW}/\sqrt{\text{Hz}}$ emitter follower based square law detector.

4.4 Common Base (CB) Square Law Detector

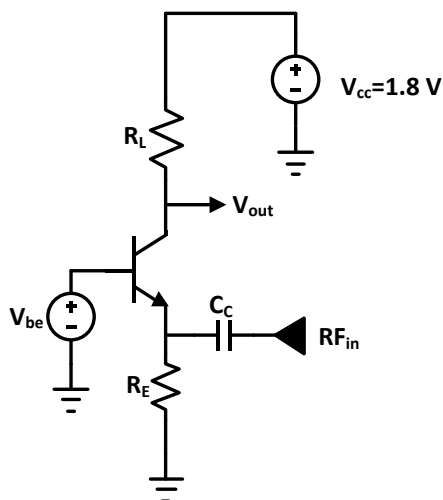


Fig. 4.15 Common base square law detector

Fig. 4.15 shows the square law detector designed using common base configuration. The resistance R_E at the emitter node enables the path of the DC current to ground and the 63 GHz signal is capacitively coupled to the emitter node.

4.4.1 Design

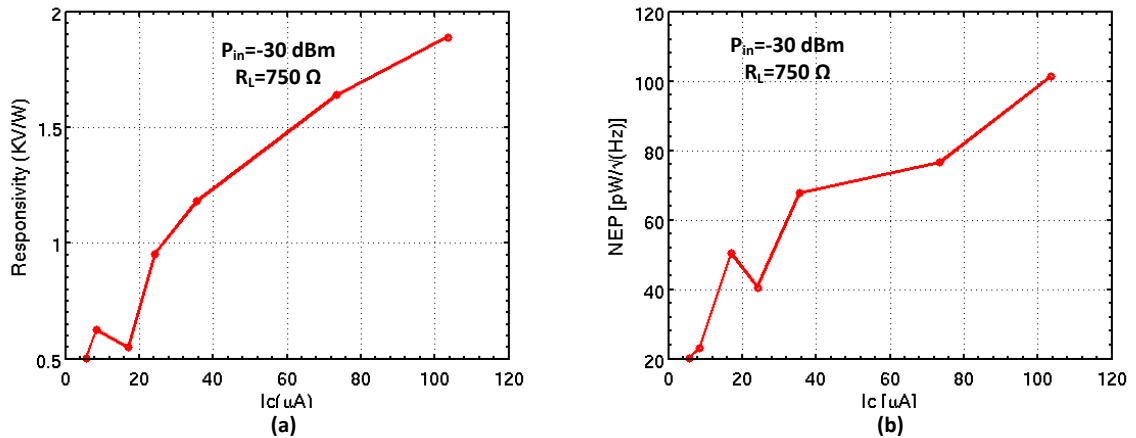


Fig. 4.16 (a) DC responsivity and (b) NEP against I_C CB-based detector

In order to analyse the design trade-offs for the CB detector, R_L and R_E are fixed at 750Ω and 100Ω , respectively with an input power of -30 dBm and $L_e = 2 \mu\text{m}$ (same as that of the previous detectors in order to benchmark their performance for the same R_L and L_e values). All simulations are performed using PSS and PNOISE analysis in Spectre™ for an integration time of 100 ms. Figs. 4.16(a) and 4.16(b) show the variation of \mathfrak{R} and NEP against I_C , respectively. The responsivity increases with increasing I_C , which is as expected. However, the achieved responsivity is lower (and hence a higher NEP) since a fraction of the input signal current also flows through the R_E . The NEP of the detector increases as the I_C increases. This is due to the thermal noise added by the resistance R_E to the overall noise contribution and also due to lower responsivity achieved for the detector.

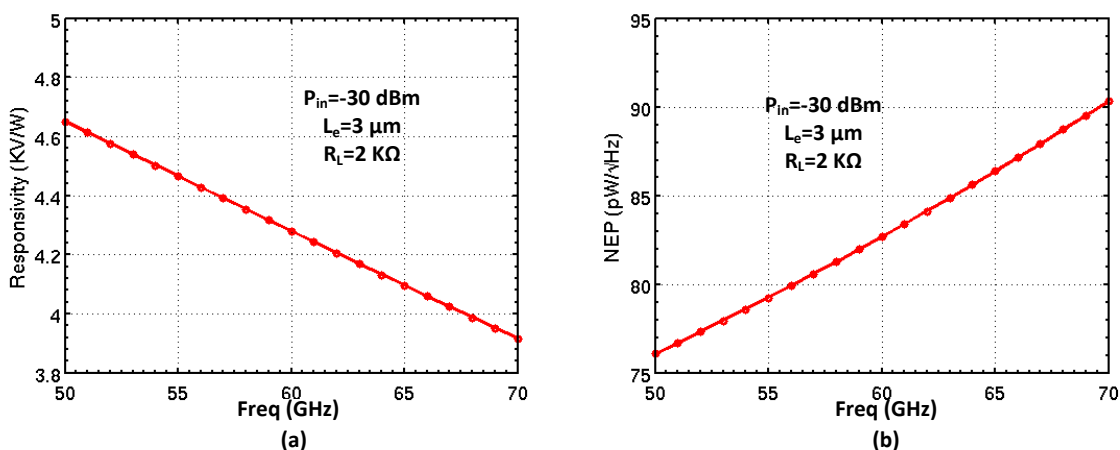


Fig. 4.17 (a) DC responsivity and (b) NEP against frequency for CB-based detector

The circuit analysis is similar to that of the CE and emitter follower detectors. An R_L value of 2 K Ω and L_e of 3 μ m was chosen for high responsivity as well as for lower NEP along with an I_C value of 82 μ A. The value of R_E is fixed at 200 Ω in order to reduce its noise contribution to the overall NEP as well as minimize its effect on the responsivity since it acts as degenerating resistor, thus reducing I_C . The detector achieves \mathfrak{R} of 4.2 KV/W and NEP of 85 pW/ \sqrt Hz (see Fig. 4.17).

4.5 Cascode Square Law Detector

Fig. 4.18 shows the cascode based square law detector. Both the input device (CE) and the cascode transistor are biased for the square law behaviour. The detector performance of the cascode topology are the same as that of the CE stage and provides an additional benefit of high reverse isolation which motivates its choice as the detect

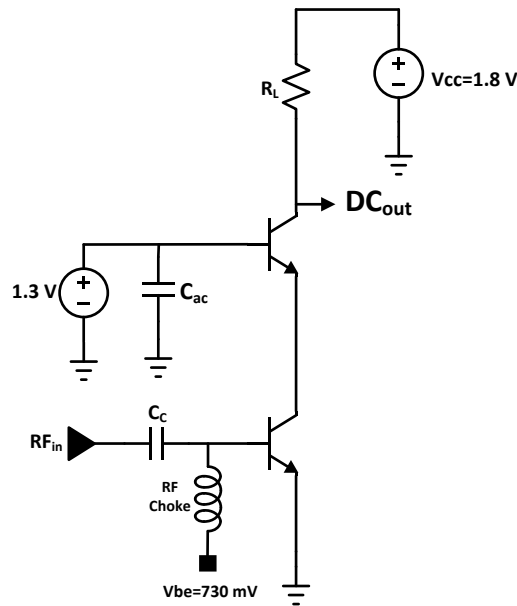


Fig. 4.18 Cascode-based square law detector

Fig. 4.19 shows the scenario in which the 63 GHz LNA directly drives the CE-based detector. The base-to-collector capacitance (C_{bc}) provides a direct path from the detector's input [4.5]. For example, a C_{bc} of 10 fF at 63 GHz translates to an impedance of 250 ohms. Thus, the signal from the LNA output may leak directly to the output of the detector. Using a cascode topology alleviates the problem of isolation due to absence of miller capacitance in the CB transistor [4.4].

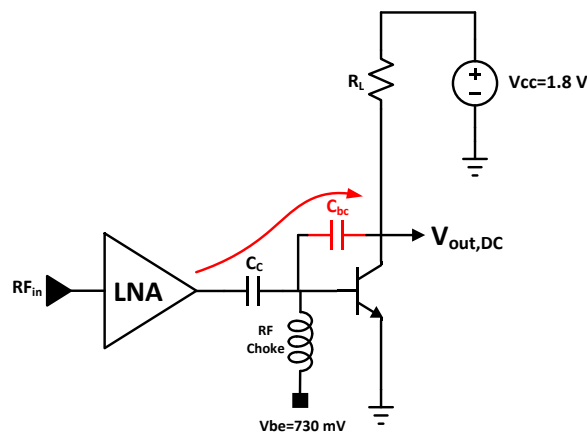


Fig. 4.19 Problem of reverse isolation in using a CE-based detector

The achieved specifications are similar to those of the CE-based detector presented in section 4.2. Since the same amount to current is needed in the cascode topology for square law operation and the performance specifications DC responsivity and NEP are governed by the same trade-offs between bias current, emitter length and load resistance value.

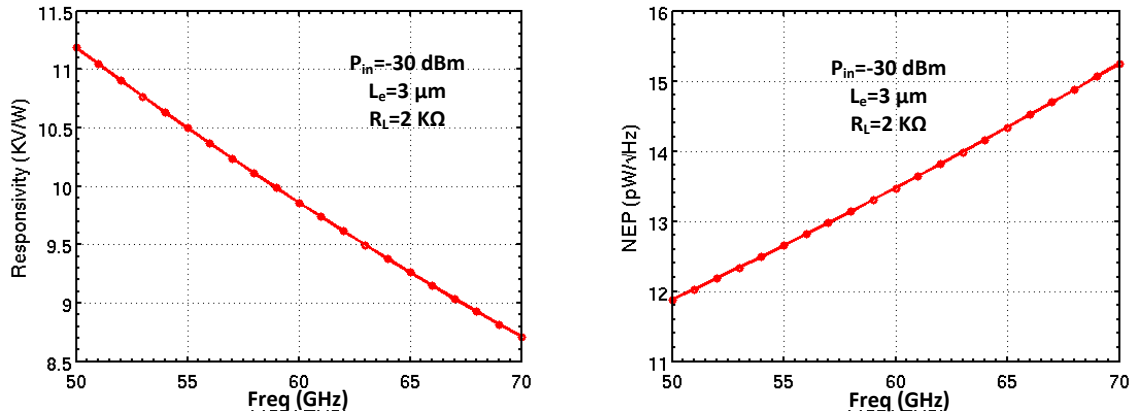


Fig. 4.20 (a) DC responsivity and (b) NEP against frequency for cascode detector

Figs. 4.20 (a) and 4.20 (b) shows the achieved DC responsivity and the NEP of the cascode detector against the frequency, respectively.

4.6 Conclusions

Square law detectors were designed using basic transistor topologies in order to assess the performance of each detector based on the DC responsivity and NEP. Design trade-offs were discussed based on transistor size, bias current and load resistance for all the topologies and the findings were validated with simulation results. Table 4.1 provides a comparative summary of the achieved detector specifications for all the detector schemes. From Table 4.1, it can be said that CE topology is more suitable for detector implementation due to its high \mathfrak{R} and low NEP compared to the emitter-follower (CC) and CB- based detector topologies.

Table 4.1 Performance comparison of square law detectors

| Parameter | Common Emitter | Emitt. Follower | Common Base | Cascode (CE+CB) |
|------------------------|----------------|-----------------|-------------|-----------------|
| DC Responsivity | 9.6 KV/W | 192 V/W | 4.2 KV/W | 9.6 KV/W |
| Noise Equivalent Power | 14.3 pW/√Hz | 185 pW/√Hz | 85 pW/√Hz | 14.3 pW/√Hz |
| Supply Voltage | 1.8 V | 1.8 V | 1.8 V | 1.8 V |
| Power Consumption | 153 μ W | 45 μ W | 147 μ W | 153 μ W |

However, the cascode topology, while providing the same detector performance as the CE topology prevents the 60 GHz signal from leaking to the output due to its good reverse isolation [4.4,4.5].

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Chapter 5

LNA Layout and Post Layout Simulation Results

This chapter presents the final layout of the LNA. Floorplanning considerations for the LNA layout are presented. The top cell of the LNA layout is discussed followed by a brief overview of the layout of the individual cascade stages. Lumped element modelling inductors and π -model of the interconnect is also included. Post layout simulation results of the LNA are discussed in the last section.

5.1 60 GHz LNA Floor Planning

The influence of parasitic elements on the circuit performance becomes significant at higher frequencies. Thus, careful floor planning is required towards the final LNA layout. The issues pertaining the LNA floorplanning are discussed as below:

Signal routing: The reactive parasitics associated with the metal interconnects provide a finite impedance in the signal path at millimeter-wave frequencies, which may reduce signal amplitude and affect LNA performance characteristics such as gain and noise figure. Therefore, efforts have been made to minimize the signal path across chip. This includes the signal path from the RF input bondpad to the actual LNA input. Similarly, the interconnects between the LNA output and the RF output bondpad are also taken into account.

Ground plane: At the schematic level, the LNA design assumed ideal behaviour for the ground i.e., zero impedance. In reality, at higher frequencies the parasitic effects of the ground provide a finite impedance to the RF signals. The problem exacerbates at millimeter-wave frequencies as the parasitic inductance of the ground (for example, a value of 25 pH in Fig. 5.1) provides considerable impedance at signal frequency of interest.

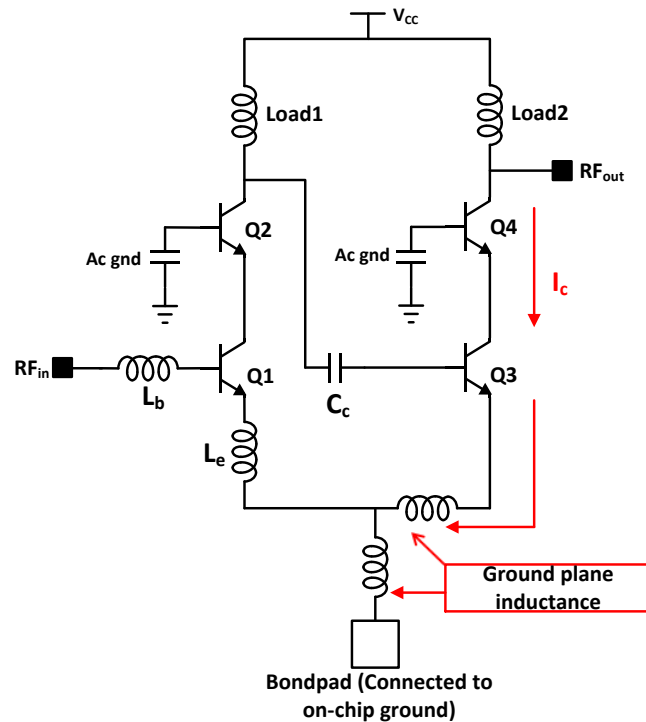


Fig. 5.1 Effect of ground plane inductance on the 2-stage cascode amplifier (biasing not shown)

Fig 5.1 shows the 2-stage cascode LNA with finite inductive reactance due to the local (or on-chip) ground. Since the signal current flows in loops, it needs a return path as well. The finite inductance of the ground plane acts as a degenerating impedance connected to the emitter node of the circuit. This reduces the signal amplitude levels which degrades the amplifier gain and the noise figure. In order to reduce the effect of the ground parasitics, a ground plane should be made as uniform and continuous as possible. Such an approach helps in providing to the signal a low inductance path to ground.

Decoupling capacitors: For a DC decoupling capacitor, one terminal is connected to the RF path of the circuit while the other terminal is grounded. Taking advantage of the uniform ground plane mentioned above, the grounded terminal can be connected with this ground plane thus providing a low inductance path to the RF signal via ground plane. To this end, decoupling capacitors are distributed around the chip and are placed as close as possible to the bias points and supply lines.

For instance, as explained in chapter 3, DC decoupling capacitors must be placed as close as possible to the cascode transistor in order to minimize the effect of parasitic inductance at the base node, which can cause oscillatory conditions in the circuit. Care is taken in the two cascade stages to minimize this parasitic inductance.

Bondpads: Bondpads around the chip periphery connect the chip to the outside world. Normally, for greater flexibility of the chip measurement, it is desired to have more tuning points (via bondpads). Further, for better grounding of the LNA additional bondpads can help in reducing the effect of the bondwire/probe inductance along with a uniform ground plane. However, additional ground pads may pose a limit on the chip area. Hence, during the layout, approach is to achieve a compact, area efficient chip while incorporating adequate ground pads at the chip boundary.

Other Considerations: The layout of the individual cascode stages of the LNA is also crucial towards the final chip layout. For instance, the ac grounding of the cascode stages needs to be connected to the common ground plane (section 5.3.1). Further, extensive EM simulations are required as part of the overall layout and post-layout iterations in order to account for coupling between various parts of the circuits, for e.g. magnetic coupling between adjacent metal lines and inductors and arrive at a safe distance by assessing the extent of coupling between them. Similarly, distance between adjacent inductors must be taken into account as well and a safe distance must be identified by using 2.5 D EM simulators. Finally, the layout and schematic level design iterations must be done concurrently by taking into account all possible non-ideal aspects from the layout. Thus, back annotation of the modelled parasitics forms a critical part of design procedure.

5.2 LNA Layout

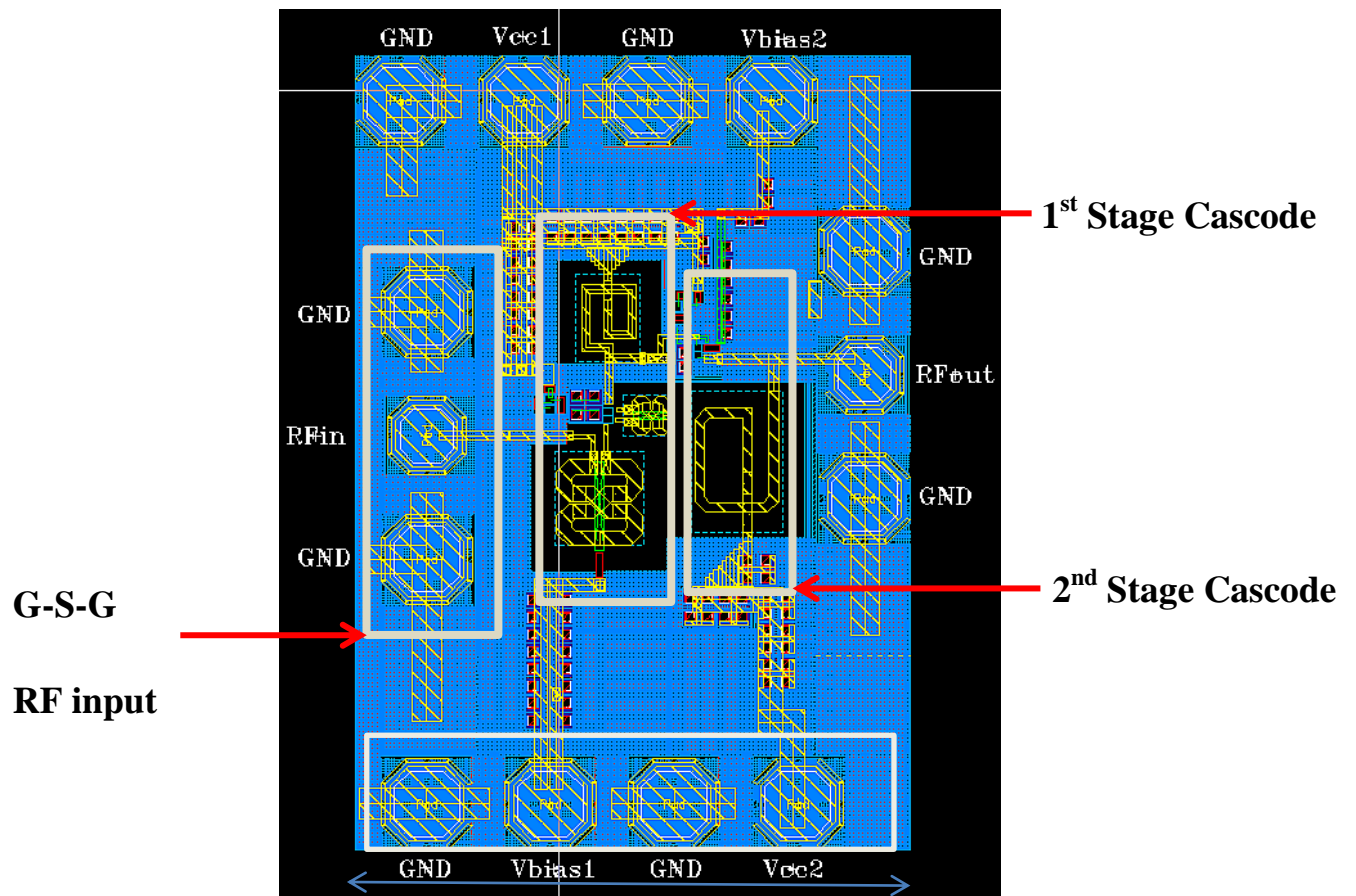


Fig. 5.2 LNA topcell layout

Fig. 5.2 shows the final LNA topcell layout including the bondpads and the decoupling capacitors around the supply and biasing lines. The area of the LNA is $0.964 \times 0.672 \text{ mm}^2$.

5.2.1 Ground Plane

As mentioned in section 5.2, ground plane impedance due to the presence of reactive parasitics affects the LNA performance. Towards this end, a continuous ground plane is made which runs through the chip area thus providing the current a low impedance path to ground.

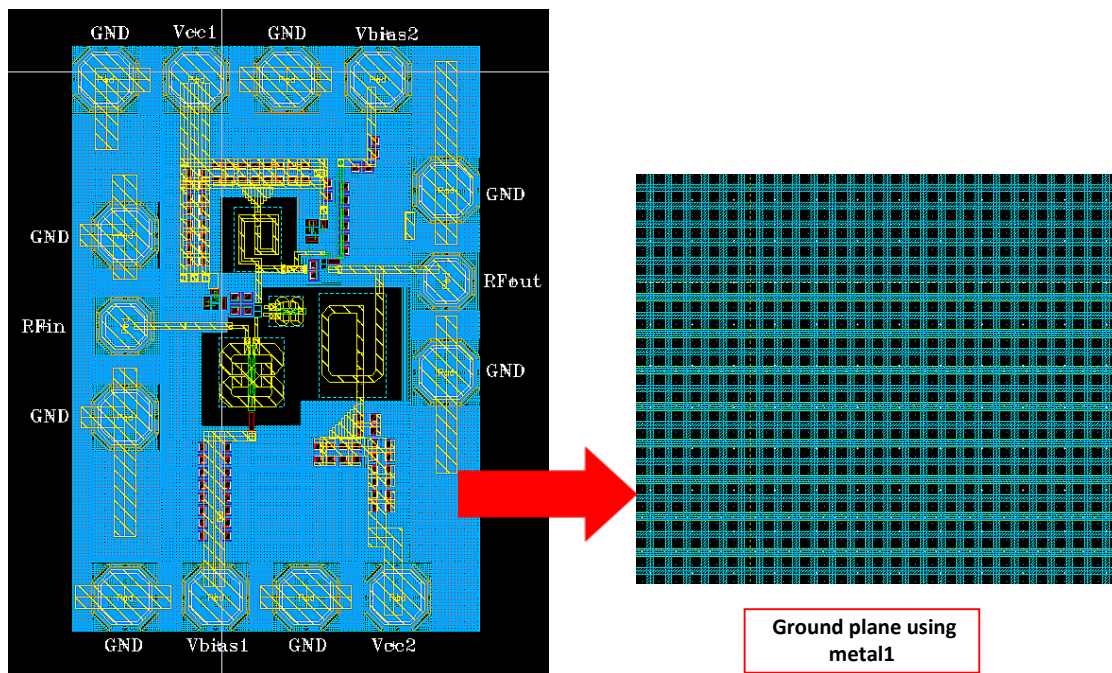


Fig. 5.3 LNA layout showing continuous ground plane made with metal1

Fig. 5.3 shows the ground plane made of metal1. A meshed ground plane is made in accordance with the metal density rules of the QUBIC4xi technology, given by line width to spacing ratio of $1\ \mu\text{m}/1\ \mu\text{m}$ for at least 50 % metal density coverage [5.2]. To this end, the ratio of $0.8\ \mu\text{m}/1.4\ \mu\text{m}$ for more than 50 % coverage. The benefits of the extended ground plane are apparent as the RF circuitry can be connected directly to it, henceforth providing a low impedance path to ground in close proximity.

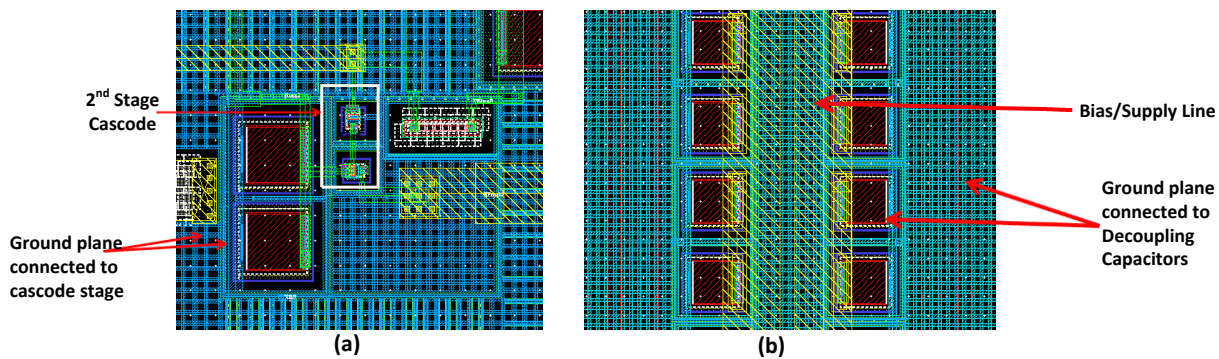


Fig. 5.4 Ground plane connection to (a) cascode stage and (b) decoupling capacitors

Shown in Fig. 5.4 (a) and Fig 5.4 (b), the cascode stage and the decoupling capacitors, respectively, connect directly to the ground plane. Such an arrangement ensures that the path for the signal current to ground is wider due to its uniformity throughout the chip and hence providing less reactive parasitics.

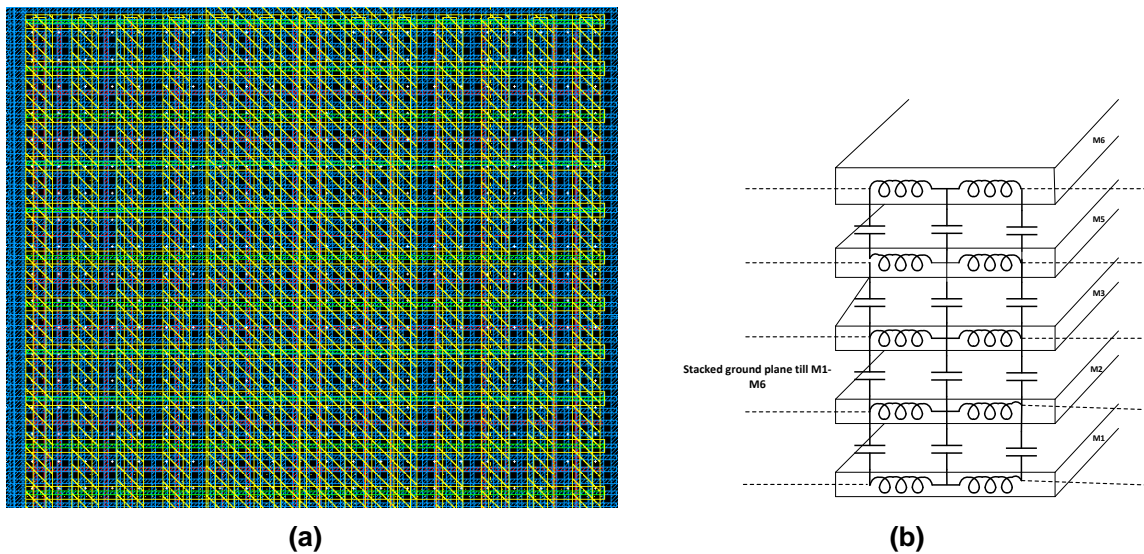


Fig. 5.5 (a) Layout view ground plane with stacked metals (M1-M6) and (b) the equivalent 3-D representation showing parasitics

Since the ground plane made on metal1 has a higher capacitance to substrate, a stacked grounding approach has been employed in which all available metals (metal1 till metal6) and vias are used which reduces the inductance while keeping the capacitance unaffected. Shown in Fig. 5.5, such an approach reduces the effective inductance of the ground plane due to inductance of the stacked metals appearing in parallel. Further, since all metal layers are shorted with vias to the on-chip ground, the capacitance between the metal layers gets shorted and hence becomes ineffective. In order to verify the reduction in effective inductance, an EM simulation of the ground plane with single metal1 and the other using the stacked metal layer approach was performed with an area of $100 \times 100 \mu\text{m}^2$.

Table 5.1 Ground plane comparison

| Ground Plane Type | Area (mm ²) | Inductance (pH) |
|-------------------|-------------------------|-----------------|
| Metal 1 Only | 100μm×100μm | 32.53 |
| Stacked (M1-M6) | 100μm×100μm | 24.36 |

Table 5.1 shows the results obtained from the EM simulations. The effective inductance of the stacked metal ground plane reduces by 25%, due to the parallel combination of the inductances of all the metal layers against the inductance of the ground plane made of single metal. In the final layout, stacked metal approach ground plane has been employed wherever possible. Care is taken not to bring the stacked ground plane close to the biasing and signal routing interconnects (which is done with metal6 interconnects), in order to avoid magnetic coupling between them.

5.2.2 Cascode Stage Layout

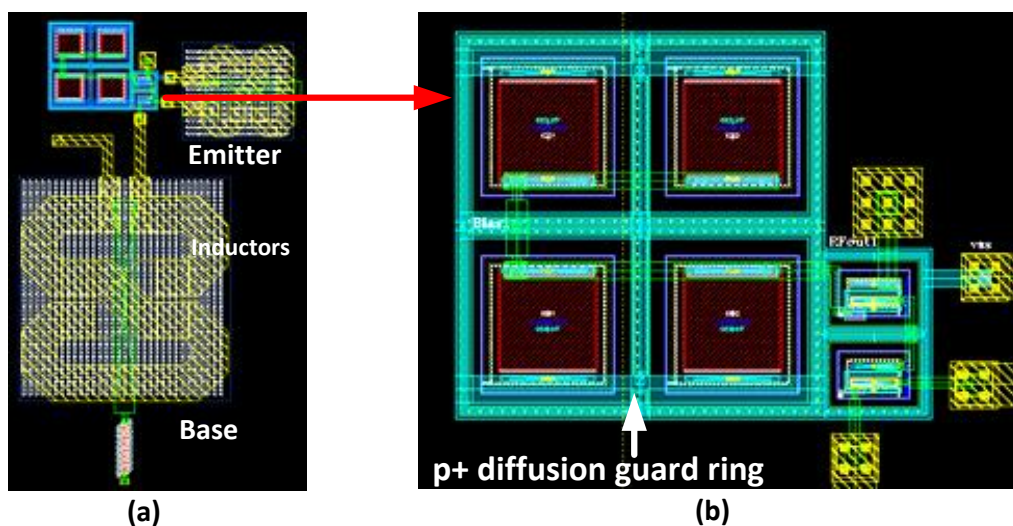


Fig. 5.6 (a) 1st stage cascode layout and (b) part of (a) showing the cascode transistors

Fig. 5.6 (a) shows the layout of the 1st cascode stage. It also shows the base and emitter inductors (from the library) used for simultaneous impedance and noise matching. Fig 5.6 (b) shows the enlarged view of the cascode stage in Fig 5.6 (a) showing the cascode stage and the poly capacitors used for ac ground at the base of the cascode transistor. Circuit components have been placed as close as possible for an area efficient layout. A guard ring (p⁺ diffusion) is placed around the transistors in order to prevent the substrate noise.

currents from reaching the RF cascode stage [1]. Further, the guard ring is connected to the uniform ground plane made from metal1. The p⁺ diffusion ring is also used to connect to the metal1 ground plane thus providing a low impedance for ground for the current.

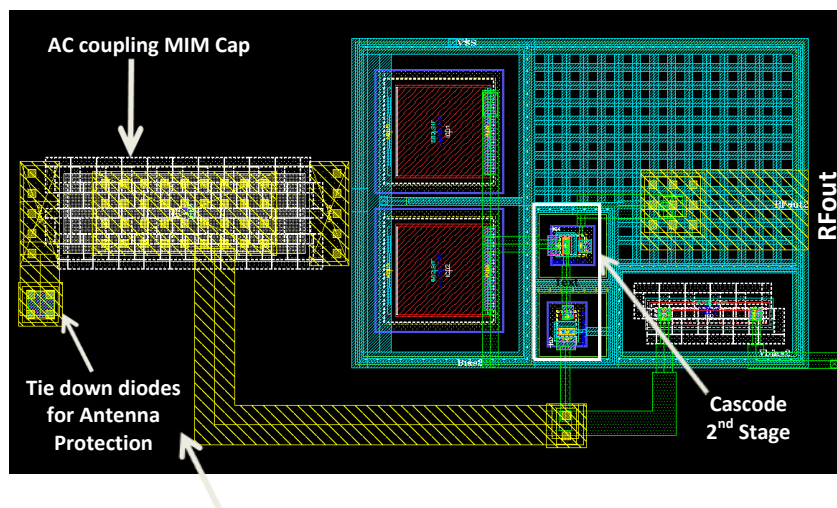


Fig. 5.7 Cascode 2nd stage layout

Fig 5.7 Shows the 2nd cascode stage layout which consists of an AC coupling metal-insulator-metal (MIM) capacitor (for signal coupling with 1st stage of the capacitor). During IC fabrication, floating conductive surfaces exposed to the plasma and connected to an oxide may amplify the tunneling current provided by the plasma, if the area of the conductor is larger than that of the oxide. Since the metal6 connecting the 1st stage and the MIM capacitor is larger than that of the oxide, it results in antenna effect [2] (see Fig. 5.7). To this end, antenna protection diodes are used for reducing the voltage across the oxide below the tunneling threshold as per guidelines provided in the design manual [2].

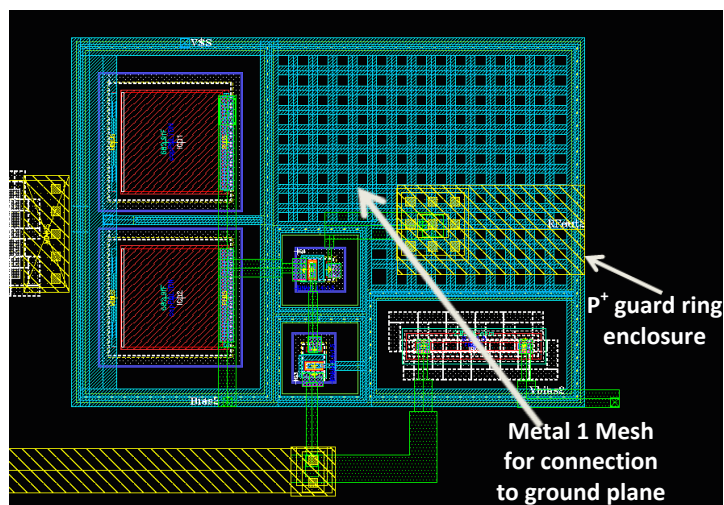


Fig. 5.8 Cascode 2nd stage core showing guard ring and metal 1 ground

Similar layout approaches are used for the 2nd stage, i.e., an enclosure of p+ guard ring around the transistors and capacitors and placement of the components as close as possible (see Fig. 5.8). The remaining space is filled with the metal1 ground and is connected to the uniform ground plane (discussed in section 5.3.1). AC ground capacitors for the 1st and 2nd stage cascode stage were laid out separately (section 5.3.3) using QUBIC4xi poly capacitors for ease of implementation of the LNA top cell layout. In chapter 3, the stability of the cascode amplifier was discussed and possible instability conditions due to interconnect parasitic connecting the ac ground capacitance and the base of the cascode (common-base) transistor was presented.

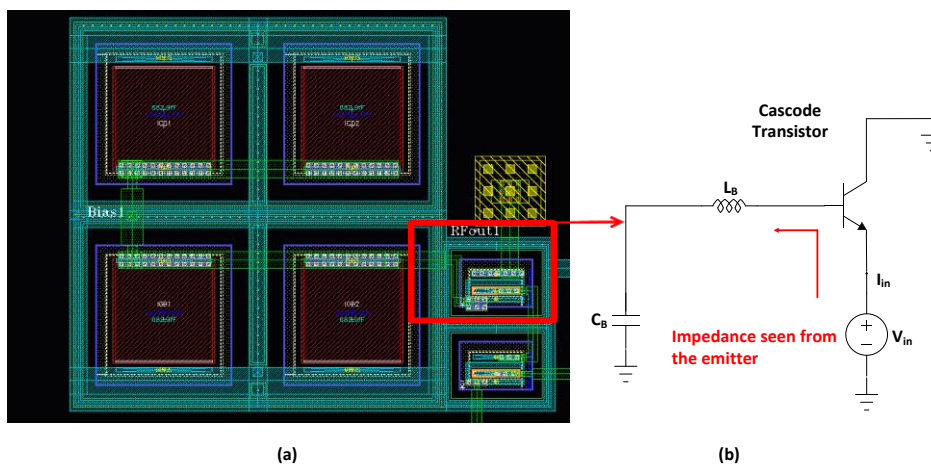


Fig. 5.9 (a) 1st stage cascode layout and (b) the its incremental equivalent circuit

Fig. 5.9 (a) shows the layout of the 1st stage highlighting the cascode transistor and the interconnect which can be schematically represented as shown in Fig. 5.9 (b). Here, L_B represents the inductance associated with the interconnect. The impedance looking into the emitter has a negative resistance which becomes more negative at higher frequencies [5.3] and may result in oscillation. Towards this end, the layout has been optimized taking into consideration the effect of the parasitic inductance (of the value of 7 pH, mentioned in chapter 3) due to the interconnect. Similar approach is followed for the 2nd stage cascode.

The placement of vias and upper metals over the transistor terminals is also of particular interest. As the current flowing out of transistors are extracted through a higher metal layer, use of vias and metal stacks introduces additional parasitic capacitances. For instance, via and metal stack formed over the transistors may introduce additional junction capacitances at base-emitter and base-collector junctions.

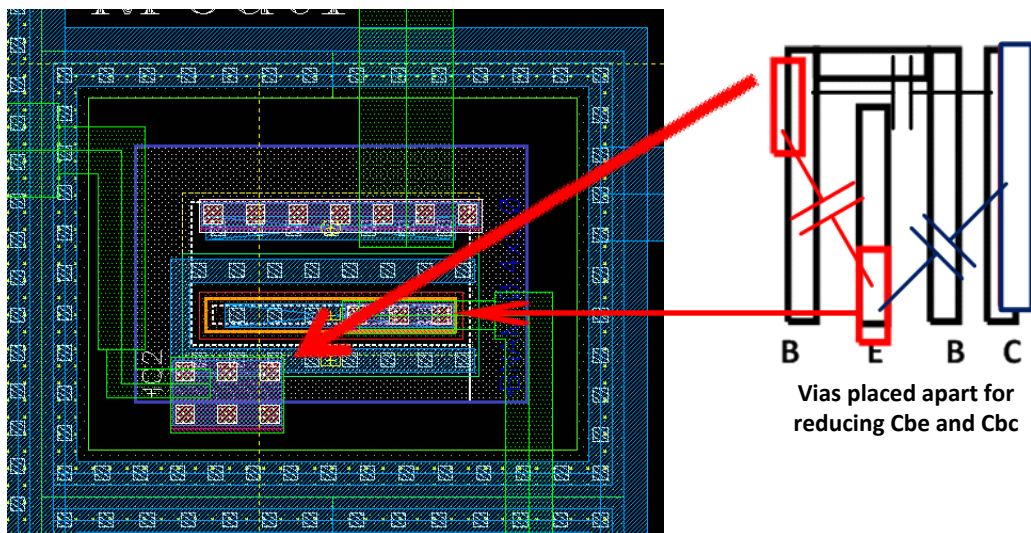


Fig. 5.10 Example of metal layers and vias over transistors for reducing parasitics

Fig. 5.10 shows the example of the 1st cascode stage where the parasitics due to the via stack may add capacitances. In order to reduce the same, vias can be placed apart within the design rule limits and hence parasitic capacitance due to the metal-via stack can be reduced.

Table 5.2 EM simulation comparison for metal-via arrangement over transistors

| Metal line arrangement | Capacitance value |
|---|-------------------|
| When placed symmetrically over Tr. contacts | 6.139 fF |
| When placed apart | 3.391 fF |

This approach has been applied to the two cascode stages so as to minimize the impact such layout parasitics. Table 5.2 summarizes the results for the case when metal-vias are placed symmetrically over the transistors contacts and the approach shown in Fig. 5.10.

5.2.3 Decoupling Capacitor Cell Layout

Decoupling capacitors were separately laid out as different cells, each cell having capacitance value of 2 pF. Shown in Fig. 5.11, the cell consists of four poly capacitors available from the QUBIC4xi design kit each valued at 500 fF. The design of this cell takes into consideration the V_{CC} lines and biasing lines.

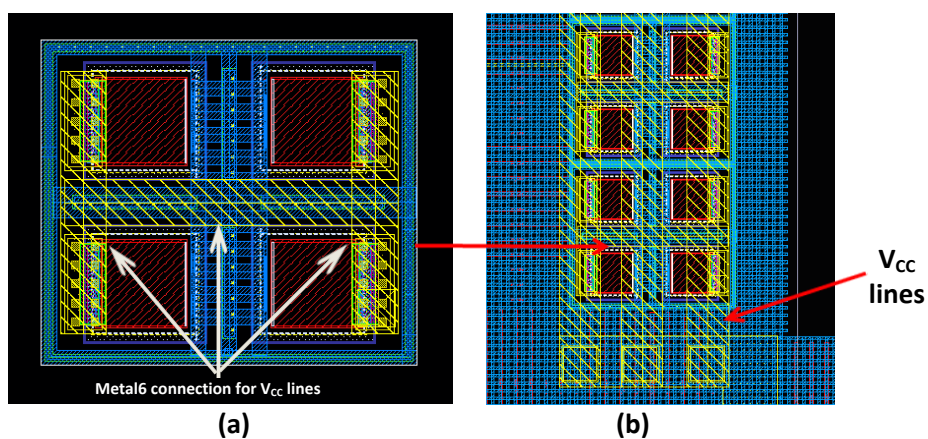


Fig. 5.11 (a) Decoupling capacitor cell using QUBIC4xi Poly Capacitors and (b) their placement in the final layout

Shown in Fig. 5.11 (b), the VCC line are distributed over 3 metal lines in order to reduce any inductance as much as possible. As per the initial floorplanning consideration of making the chip area efficient, the decoupling capacitor layout is done separately so as to embed the same under the bias lines using metal6, thus saving area.

Table 5.3 V_{CC} line EM simulation comparison

| V _{CC} line | Line length | Inductance value |
|----------------------------|------------------|------------------|
| Single metal6 line | 95 μm | 80.043 pH |
| 3 metal6 lines in parallel | 95 μm | 51.21 pH |

Table 5.3 shows the EM simulation results for the single metal6 and 3 parallel metal6 lines showing reduction in inductance.

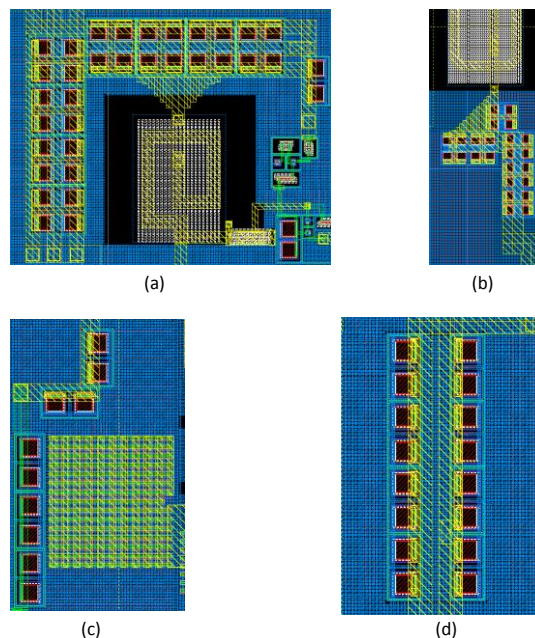


Fig. 5.12 (a) Decoupling capacitor arrangement at (a) Vcc1, (b) Vbias2, (c) Vbias1 and (d) Vcc2

Fig 5.12 shows the overall final arrangement of decoupling capacitors around various biasing and supply lines.

5.2.4 Interconnects

The interconnects are modeled as lumped π -equivalent. To this end, the lumped model was benchmarked with Momentum™ extracted layout of the interconnect in terms of its series impedance. The interconnects for the LNA are laid as per the electromigration rules documented in the design manual [2].

Table 5.4 QUBIC4xi DC current capacity

| Layer | Junction temperature ^{b)} | | | | Peak | Unit |
|--------------------------------|------------------------------------|-----------------------|-----------------------|-----------------------|---------------|------|
| | 70°C | 100°C | 125°C | 150°C | | |
| Poly - Silicided | $3 \times W$ | $3 \times W$ | $3 \times W$ | $3 \times W$ | $3 \times W$ | mA |
| Poly - Unsilicided | W | W | W | W | W | mA |
| METAL1 | $16.6 \times (W-0.06)$ | $5.3 \times (W-0.06)$ | $2.3 \times (W-0.06)$ | $1.1 \times (W-0.06)$ | ^{c)} | mA |
| METAL2 | $16.6 \times (W-0.06)$ | $5.3 \times (W-0.06)$ | $2.3 \times (W-0.06)$ | $1.1 \times (W-0.06)$ | ^{c)} | mA |
| METAL3 | $16.6 \times (W-0.06)$ | $5.3 \times (W-0.06)$ | $2.3 \times (W-0.06)$ | $1.1 \times (W-0.06)$ | ^{c)} | mA |
| METAL5 | $36.4 \times W$ | $11.5 \times W$ | $5.0 \times W$ | $2.4 \times W$ | ^{c)} | mA |
| METAL6 | $65.5 \times W$ | $20.6 \times W$ | $9.0 \times W$ | $4.3 \times W$ | ^{c)} | mA |
| CONTACT ^{d)} | 4.37 | 1.38 | 0.6 | 0.29 | ^{c)} | mA |
| VIA1, VIA2, VIA3 ^{d)} | 4.37 | 1.38 | 0.6 | 0.29 | ^{c)} | mA |
| VIA5 ^{d)} | 42.96 | 13.53 | 5.9 | 2.84 | ^{c)} | mA |

Table 5.4 shows the current capacity of the interconnects where W indicates the width of the metal lines. For example, a metal3 interconnect of width $1.5 \mu\text{m}$ corresponds to a current capacity of 23 mA. The current routing outside the RF circuitry is done with the top metal considering its better current handling (minimum metal6 width = $5 \mu\text{m}$) and also considering the fact that current extracted from stage 1 travels a certain distance before it reaches the 2nd stage.

Since the bipolar transistor used for the design in this technology have their base, emitter and collector terminals contacted to metal1, the current through the device is extracted out of the transistors using a higher metal3 interconnect (shown in Fig. 5.14), in order to reduce the capacitance to substrate. Further, it is recommended in this technology to extract current out flowing out of the transistor at a higher metal for higher frequency operation and thus enabling to carry twice as much current in Table

5.4 for a given width. All interconnect parasitics were modeled with a lumped- π model comprising of series resistance and inductance and the capacitance to ground. The lumped model was then verified with the EM simulation using Momentum. Fig. 5.13 shows the example of an interconnect modelling, where Fig. 5.13 (c) shows the close approximation of the respective (lumped and layout extracted) impedance values.

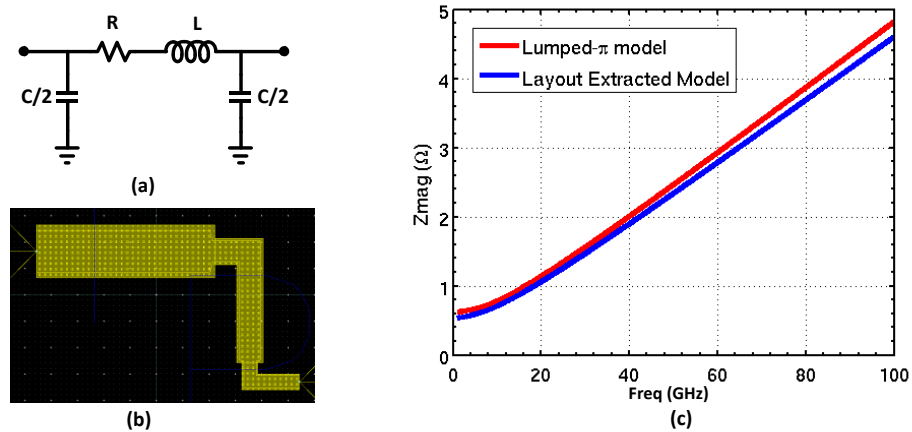


Fig. 5.13(a) Lumped- π model (b) equivalent Momentum layout and (c) Lumped element-layout comparison

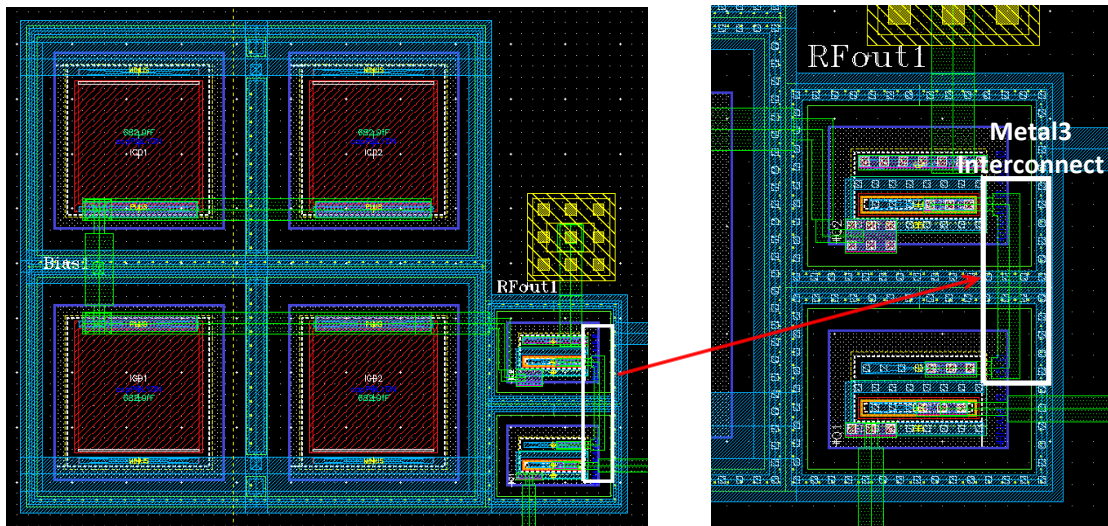


Fig. 5.14 Sample layout of the interconnect in stage 1 cascode using metal3

Other approaches towards the interconnect layout include the increasing the width of the interconnect as it extracts current and carries it to the next. Shown in Fig. 5.15, the

width of the interconnect is increased as the interconnect extracts current out of *transistor1* since it needs to carry current over a certain distance before being narrowed to the original dimension as it connects *transistor2*. However, it is important to note that any increase in metal width will increase the capacitance to the substrate and influence the signal flow due to the charging of this parasitic capacitance. Hence, the large interconnect width has been limited to signal routing outside the components in order to reduce DC resistance and the associated parasitic inductance to the signal.

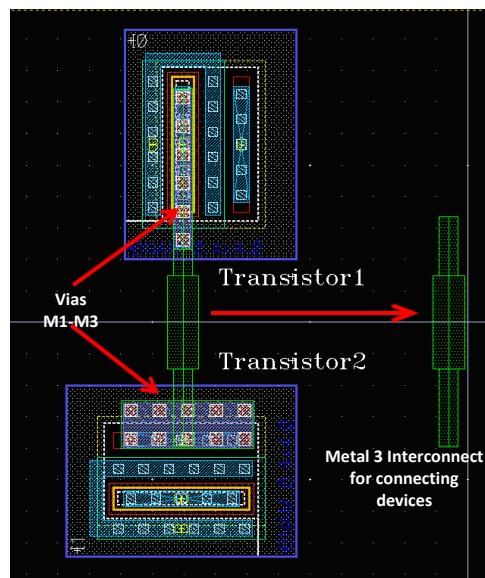


Fig. 5.15 Example of an interconnect layout for connecting circuit components

.In section 5.3.3, layout and placement of the decoupling capacitors was discussed. These decoupling capacitors are connected to the V_{CC} lines for a low impedance path to ground for the signal current. It is important to note that the interconnect joining the inductive loads of the two cascode stages to the supply lines adds additional inductance at the frequency of interest, thus changing the effective inductance value required to achieve the desired gain.

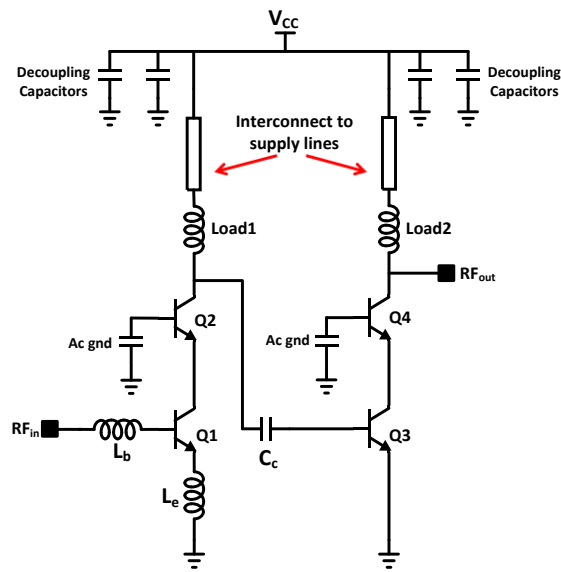


Fig. 5.16 Example of an interconnect layout for connecting circuit components

Fig. 5.16 shows the LNA with interconnects joining 1st and 2nd stage inductor loads to the supply and the decoupling capacitors which provides the AC ground path for the signal current. An estimate of the interconnect inductance can be arrived at using the EM simulations for the same and the load inductance can be optimized by absorbing the amount of interconnect inductance or by making the . Another approach is to use a step-line configuration, called *Manhattan* lines.

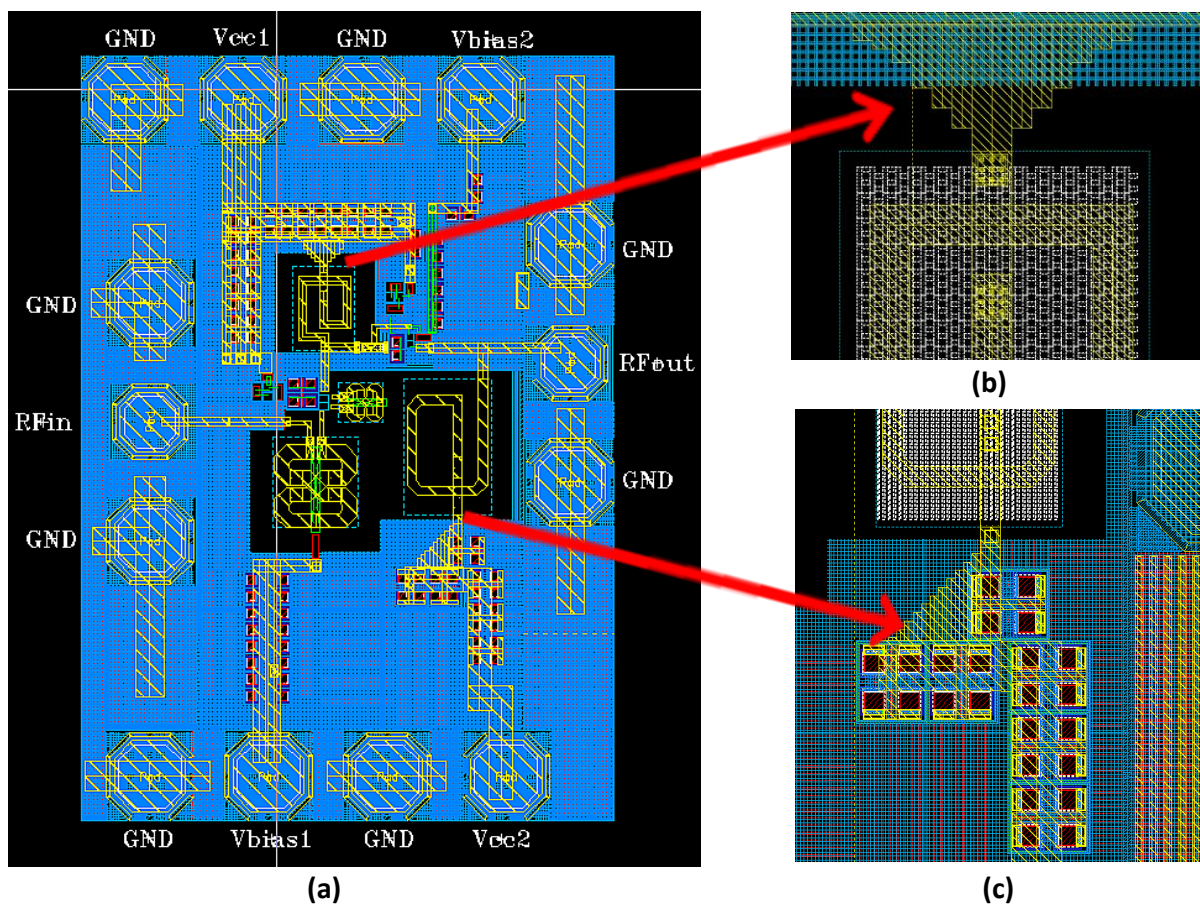


Fig. 5.17 (a) LNA layout showing Manhattan lines at collector ac ground nodes (b) 1st cascode stage and (c) 2nd cascode stage

Figs. 5.16 (a) and 5.16 (b) show the ac grounded collector nodes of the two cascode stages. The use of Manhattan lines reduces the inductance effective width increases towards the V_{CC} at the ac grounded collector nodes reduces the inductance due to increase in effective inductance.

Table 5.5 EM simulation results for AC ground connection shown in Fig. 5.17

| AC ground connection | Simulated inductance |
|------------------------------|----------------------|
| With a single Metal6 line | 18 pH |
| With a Manhattan arrangement | 12 pH |

5.3.5 Single-ended Inductor Layout

Figs. 5.18 (a) and 5.18(b) show the layout of the single-ended inductors for the 1st and 2nd stage, respectively.

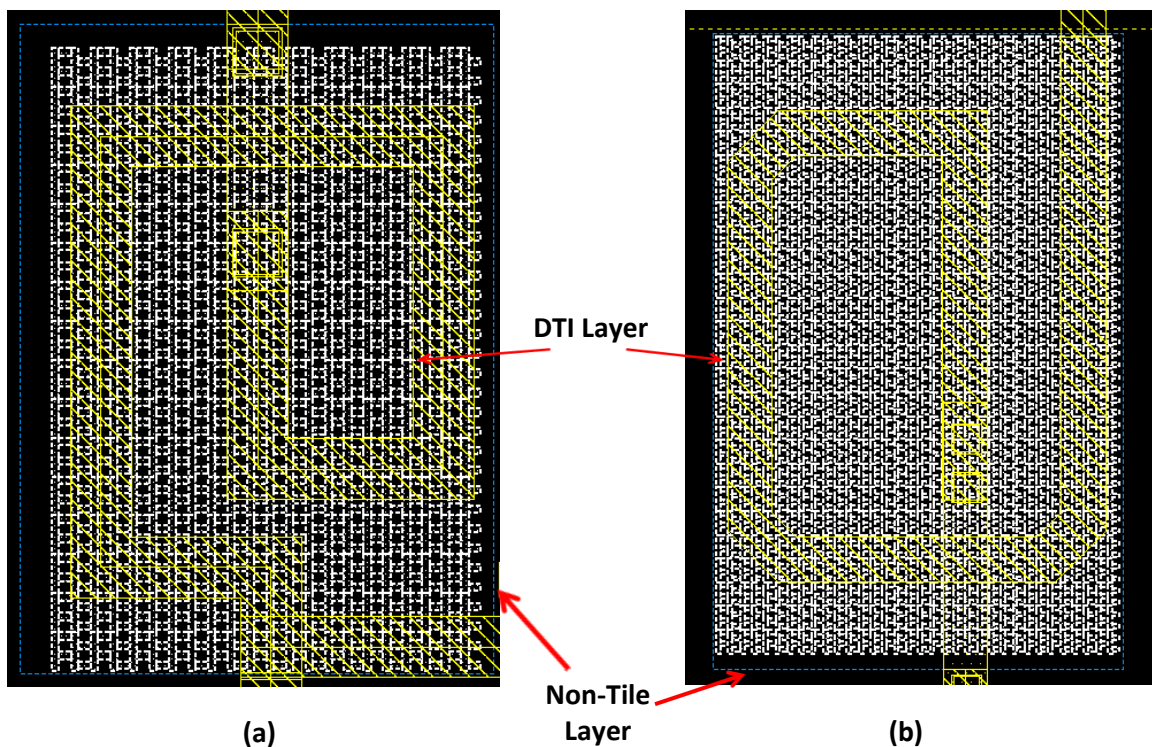


Fig. 5.18 (a) 1st stage load inductor layout and (b) 2nd stage load inductor layout

Further, deep trench isolation (DTI) layer is used for reducing the capacitance to substrate and is enclosed in non-tile layer as per the layout guidelines documented in the technology manual.

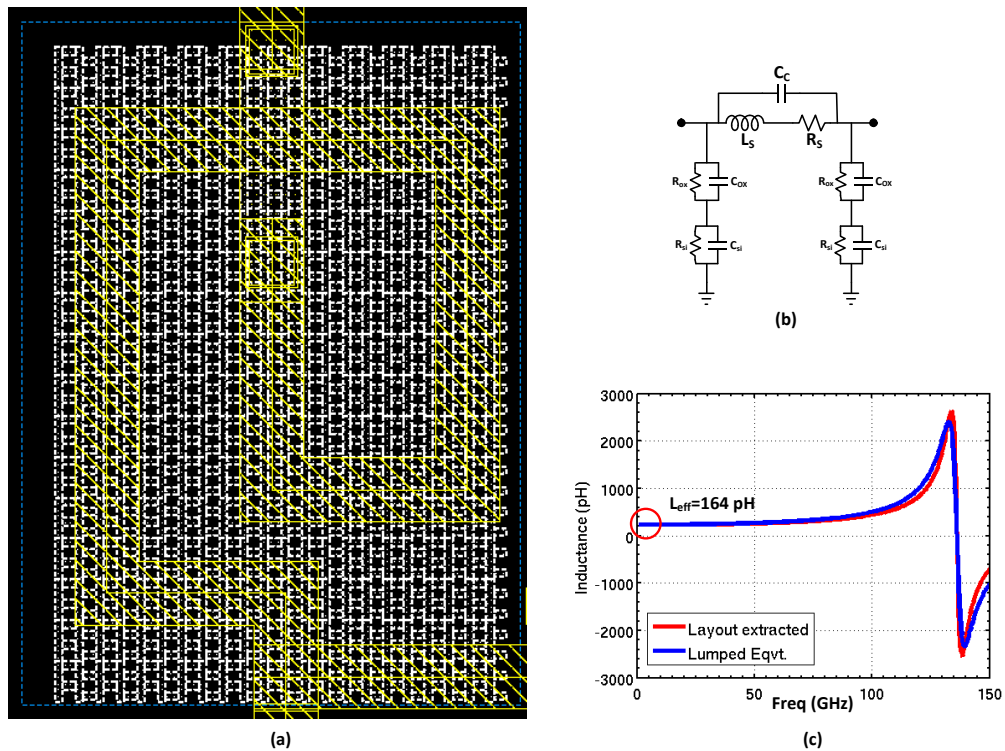


Fig. 5.19 (a) 1st stage load inductor layout (b) equivalent lumped model and (c) comparison of inductance value from (a) and (b)

The load inductors used for the design were verified with the lumped element model. Fig. 5.19 shows the model for the load inductor of the 1st stage which was done using ADS Momentum. Fig. 5.20 shows the same lumped element modelling approach for the 2nd stage load inductors. A good approximation of the inductance value is obtained.

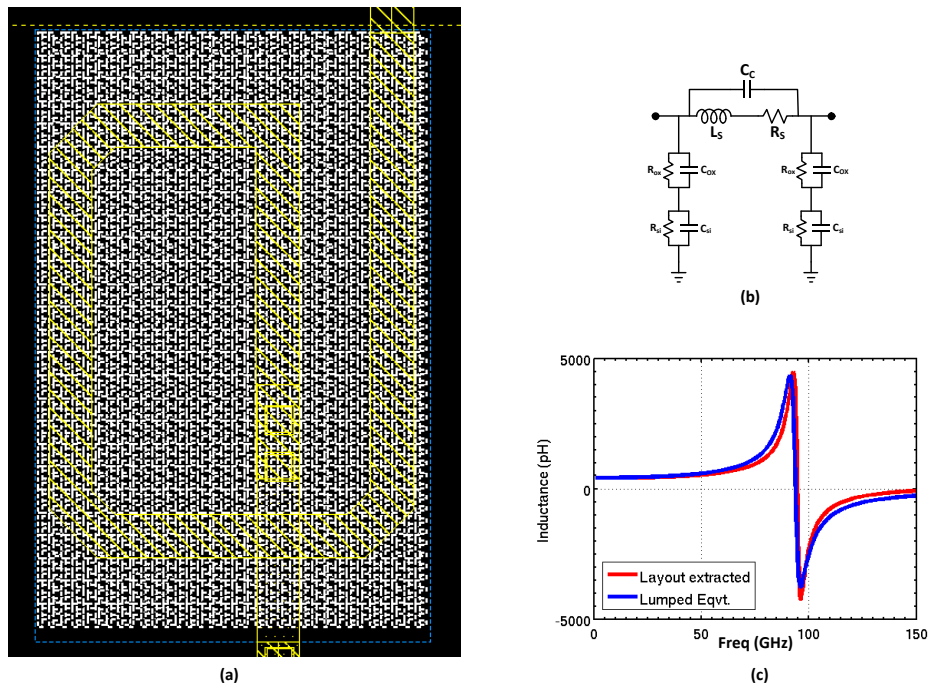


Fig. 5.20 a) 2nd stage load inductor layout (b) equivalent lumped model and (c) comparison of inductance value from (a) and (b)

5.3.6 Bondpads

The bondpads were used from the design kit. RF bondpads of size $65\ \mu\text{m}$ are used while the ground pad size is $80\ \mu\text{m}$. As mentioned in section 5.2, additional bondpads pose a limit on the chip area and may increase the distance between the LNA input and output, thus requiring longer interconnects. Therefore, additional ground bondpads have been employed in order to improve the on-chip and at the same time ensuring that the chip area is kept within reasonable dimensions. A center-to-center pitch distance of $150\ \mu\text{m}$ is maintained between the pads for measurement purposes.

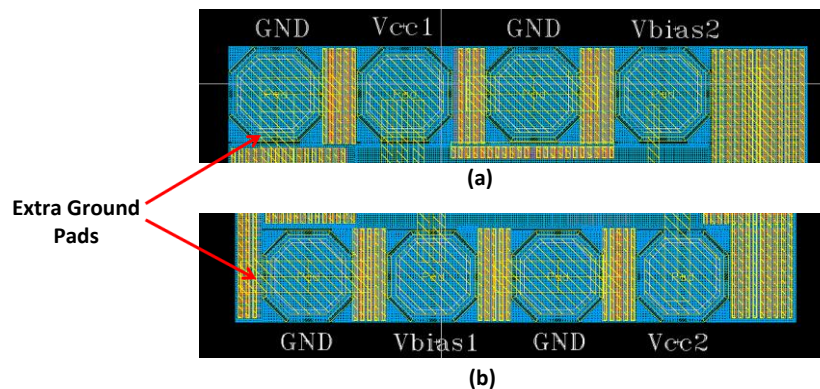


Fig. 5.21 (a) Bondpad arrangement for the upper half and (b) lower half

Figs 5.21 (a) and (b) shows the bondpad arrangement for the top and lower part of the chip with extra bondpads for better grounding.

5.4 Post Layout Results

This section presents the performance results of the LNA post layout. A brief discussion of the back-annotated schematic is followed by the summary of the post layout results of for a range of temperature and those with the effect of the bondwire inductance.

5.4.1 Parasitic Back-annotated Schematic

The layout parasitics (for the interconnects and the decoupling capacitors) simulated and verified through EM simulations are back annotated in the LNA schematic in order to account for the same and assess the change in the performance characteristics. The idea is to emulate the LNA layout as close as possible with the schematic level simulation environment. To this end, the lumped- π model of the interconnects was used for annotation of the parasitics into the schematic. Further, the bondpad arrangements were made exactly as the one in the layout.

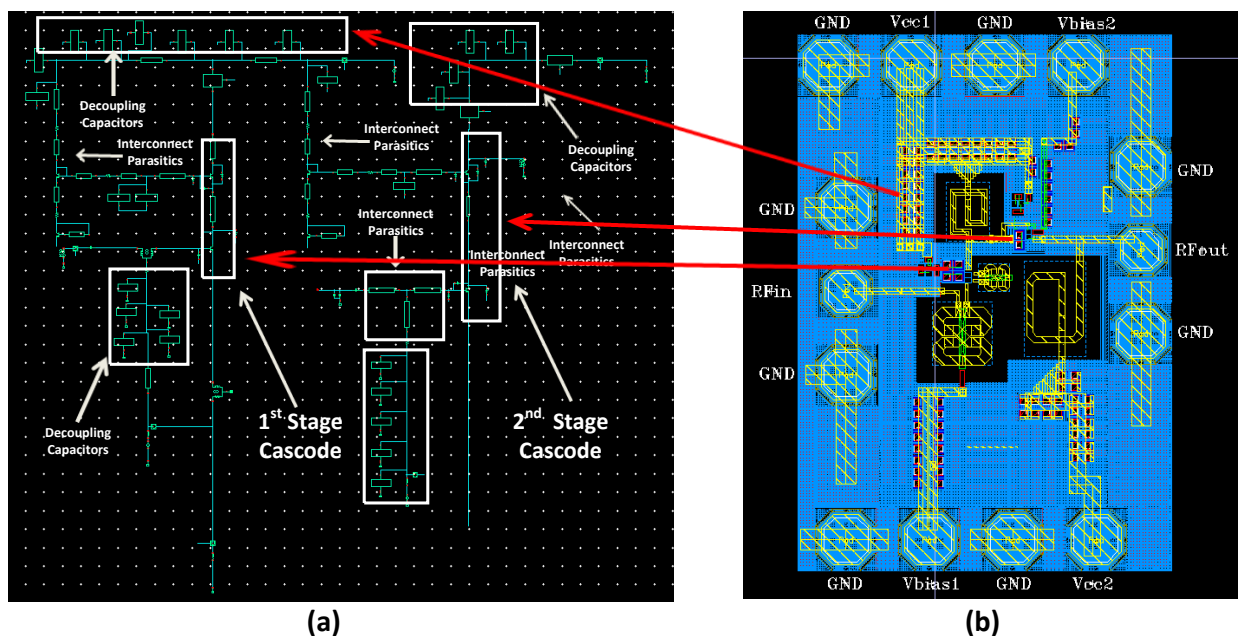


Fig. 5.22 Post layout schematic with annotated parasitics and decoupling capacitors

Decoupling capacitor cells were used as in the layout for supply (V_{CC}) and the bias lines. Fig. 5.22 (a) shows the post-layout schematic which corresponds to the final layout in Fig. 5.22 (b) as per the chip floorplan. The post-layout circuit was simulated for its performance against the idealized schematic environment. The results are summarized in the following section.

5.4.2 LNA Performance Results

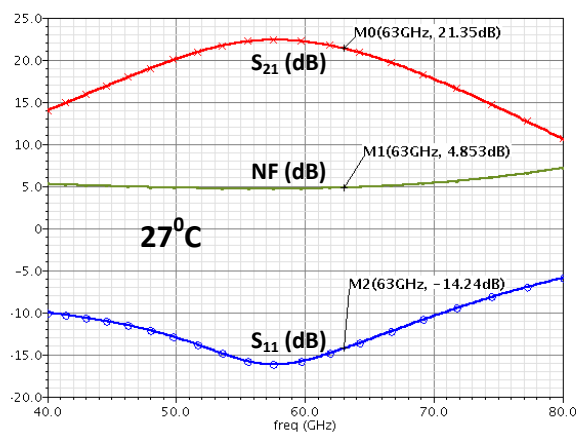


Fig. 5.23 Post layout performance results for the 63 GHz

The LNA circuit was simulated for its performance at a nominal temperature of 27°C . Fig. 5.23 shows the performance results for the gain, noise figure and the input reflection coefficient. The post-layout simulated gain is 21.88 dB, noise figure of 4.85 dB and S_{11} of -14.2 dB.

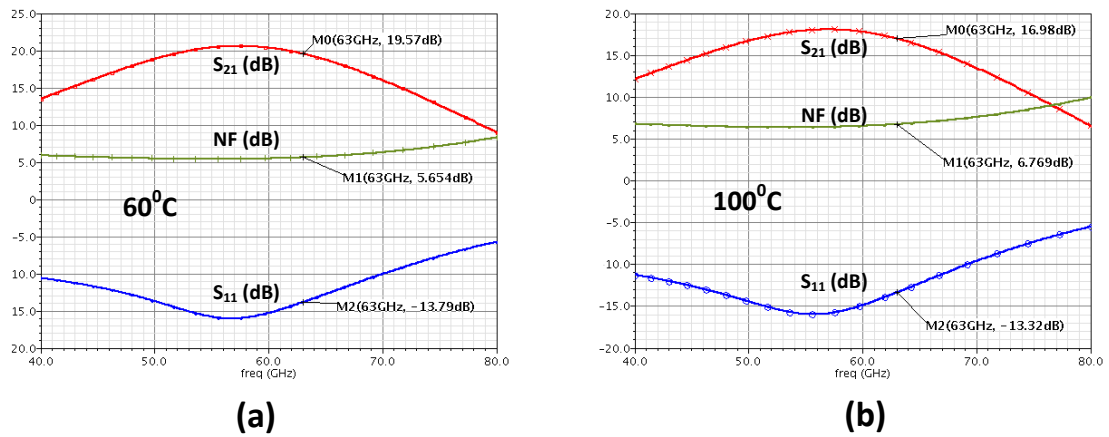


Fig. 5.24 LNA performance results for (a) 60°C and (b) 100°C

The transconductance (g_m) of the bipolar transistor is a strong function of the thermal voltage (V_T). This in turn, affects the LNA performance results directly, especially the gain and noise figure. Therefore, it is very important to assess the effect of temperature beyond nominal values and the reliability of the circuit under extreme temperature conditions. To this end, post layout simulations were performed for the temperature corners at 60°C and 100°C. Figs. 5.24 (a) and 5.24 (b) shows the simulation results obtained for 60°C and 100°C, respectively. At 60°C, the 63 GHz post layout simulated gain is 19.57 dB, noise figure of 5.65 dB and S_{11} of -13.79 dB. At 100 °C, post layout simulated gain is 16.98 dB, noise figure of 6.76 dB and S_{11} of -13.32 dB.

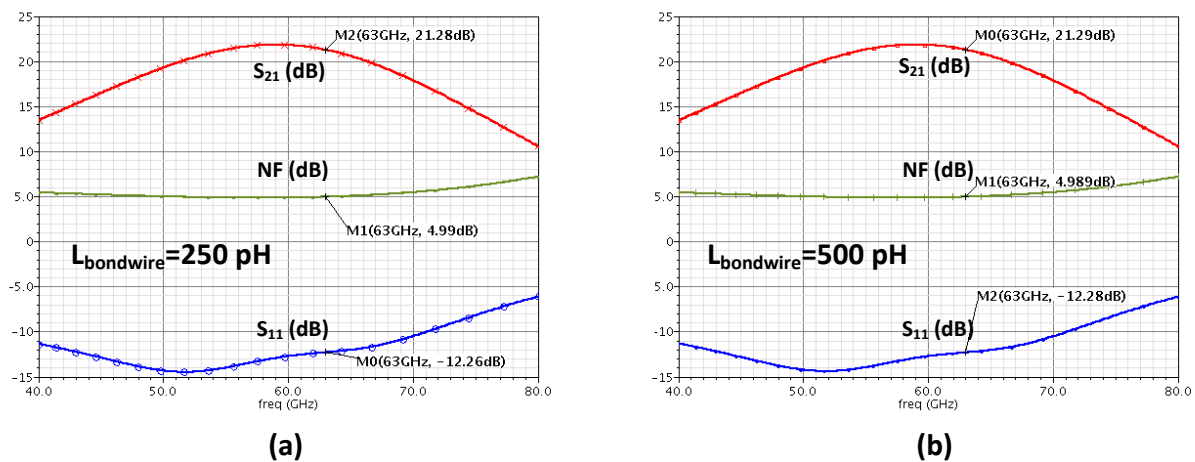


Fig. 5.25 Bondwire inductance effect on LNA performance with values (a) 250 pH and (b) 500 pH

The ground pads for the biasing lines are bondwired outside of the chip for measurement purposes. This effect can affect the circuit performance as the bondwire inductance appears in parallel with the on-chip ground inductance. To this end, a continuous ground plane and additional bondpads were added in order to reduce the on-chip ground inductance and hence reduce the influence of the bondwire. The LNA was simulated taking into account the effect of the bondwire inductance with values 250 pH and 500 pH.

Figs. 5.25 (a) and 5.25 (b) shows the post layout results taking into account a bondwire inductance of 250 pH and 500 pH, respectively. The results show only marginal impact on the performance metrics by adding additional ground pads as done in the final layout.

5.5 Conclusions

The layout of the LNA designed at 63 GHz was presented in this chapter. A detailed discussion on the floorplanning followed by the layout approaches of the individual stages was presented which included the ground plane, cascode stage and the layout of the decoupling capacitors and the interconnects. Post layout simulation results showed the LNA performance metrics for different temperatures and in the presence of bondwire. Tables 5.6 and 5.7 shows the summary of the post layout results.

Table 5.6 LNA performance results for different temperature corners

| LNA Parameters | 27 ⁰ C | 60 ⁰ C | 100 ⁰ C |
|----------------------|-------------------|-------------------|--------------------|
| Gain (dB) | 21.35 | 19.57 | 16.98 |
| NF (dB) | 4.853 | 5.654 | 6.769 |
| S ₁₁ (dB) | -14.24 | -13.79 | -13.32 |

Table 5.7 LNA performance results with different bondwire inductance values

| LNA Parameters | $L_{\text{bond}}=0$ pH | $L_{\text{bond}}=250$ pH | $L_{\text{bond}}=500$ pH |
|-----------------------|--|--|--|
| Gain (dB) | 21.35 | 21.28 | 21.29 |
| NF (dB) | 4.853 | 4.99 | 4.989 |
| S_{11} (dB) | -14.24 | -12.26 | -12.28 |

References

- [5.1] S. Bronckers, G.V.D. Plas, G. Vandersteen, Y. Rolain, “ Substrate Noise Coupling in Analog/RF Circuits”, Artech House, 2010.
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Chapter 6

Conclusions

6.1 Summary

The main objective of this thesis was to design an LNA and square law detector circuit which could be integrated with a Butler matrix to realize a passive radiometer system for human presence detection. To this end, the goal was to integrate the LNA and the detector in a single chip and also avoid need for impedance matching at the LNA-detector interface, thus reducing the component count.

Chapter 1 explained the choice of frequency band (60 GHz) for the application and motivation for passive radiometer system. A brief overview of the design challenges at mm-wave frequencies was also documented.

A detailed radiometer background was presented in chapter 2 in which detection principle was explained for the direct detection radiometer. To this end, the need for preamplification (with LNA) in the radiometer was highlighted and the specifications of the detector i.e., the responsivity and NEP were explained. A link budget analysis of the radiometer receiver chain was presented in order to arrive at the design specifications of the LNA. An NETD of 1 K was chosen for the application with a temperature of 300 K and bandwidth of 6 GHz. The losses of the Butler matrix were also taken into account for the budget analysis. The resulting design specifications of the LNA were set with a target gain of 18-19 dB and noise figure 6-7 dB in order to achieve the required resolution.

Chapter 3 presented the design procedure for the 63 GHz LNA. Two LNA designs were discussed. The first LNA was designed to drive the high input impedance of the detector. The design with ideal components was showed followed by inclusion of bondpads and layout parasitics in the schematic. The final design achieves a gain 20.55 dB, noise figure of 4.8 dB and S_{11} of -14.48 dB with a power consumption of 34.65 mW.

The second LNA was designed with its output matched using a tapped capacitor transformer. A similar design approach was followed and it achieves a gain 20.55 dB, noise figure of 4.8 dB and S_{11} of -14.48 dB and S_{22} of -18.7dB with a power consumption of 34.65 mW.

The design of square law detectors using standard bipolar transistor configurations was presented in chapter 4. The main objective in this chapter was the circuit analysis of standard topologies and benchmark the same in terms of detector performance metrics. The CE-based detector showed better performance results compared to other configurations.

Chapter 5 presented a detailed discussion of the 63 GHz LNA layout. Floorplanning considerations were presented and the layout of individual stages was presented and the stability considerations discussed in chapter 3 i.e., the influence of parasitic inductance was also presented in the layout. The lumped- π model of the interconnects was presented as well as for the load inductors used for the two cascode stage. Post layout results for performance across different temperature corners as well as the influence of bond wire inductance on the circuit performance were documented in the concluding section.

6.2 Future Work

The layout of the LNA and detector for the single chip solution needs to be done. To this end, the floorplanning needs to be reworked for accommodating the detector circuit with existing LNA layout. Further, the detector circuit needs to be laid out separately in order to characterize the standalone detector performance. Measurements tasks would include the performance measurement of LNA+ detector chip and the standalone detector and subsequent integration of the circuit blocks with the Butler matrix, thus resulting in a complete passive radiometer realization.